

MAINTENANCE MANUAL
 SYSTEM CONTROL/SYNTHESIZER BOARD
 CMC-386
 FOR
 NLSH040
 TWO-WAY MOBILE RADIO COMBINATIONS

PRELIMINARY

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DESCRIPTION

The System Control/Synthesizer Board (A801) for the NLSH040 two-way mobile FM radio, controls the radio by providing all necessary digital processing, tones and control functions. The logic circuitry of this board controls channel acquisition, RF frequency selection, tone generation and detection, timing functions and operator interface functions. Interface functions include control panel displays and switch panel controls, microphone hookswitch and programming functions. The frequency synthesizer generates the transmitter output frequency and the receiver first mixer injection frequency. The Control/Synthesizer Board contains the following:

- Microprocessor
- External memory EPROM for the microprocessor
- The programmable personality EEPROM
- Four octal latches for the I/O microcomputer interface
- Transmit and receive audio processing circuitry

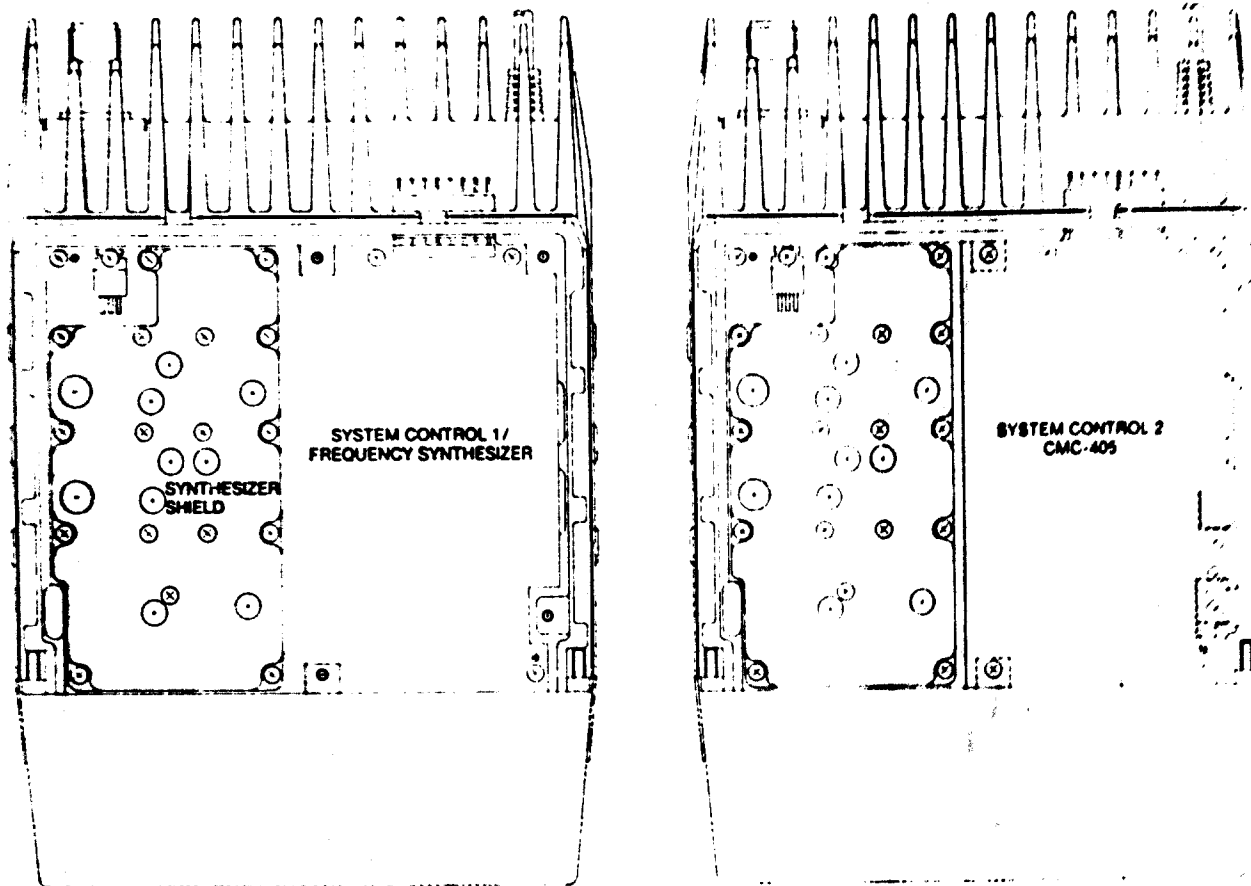
The Control/Synthesizer Boards (CMC-386 & CMC-405) mount in the top section of the frame assembly as shown in Figure 1 - System Control/Synthesizer Board Location.

System Control 1/Synthesizer Board CMC-386 provides the microprocessor and control logic. This board also provides the synthesizer circuit for generating operating frequencies. The Control 2 Board (CMC-405) provides the audio processing for both the transmit circuit and the receive circuit. It also provides power distribution for the other circuits.

CIRCUIT ANALYSIS

Power Distribution

Power connections to the radio from the vehicle battery (+13.8 Volts nominal) is connected to transmit/receive connector J3. This connection is made through power cable ZC805 and connector P2. The battery input is filtered by capacitors C47, C48, C49 and surge protector CD6 and is applied to J10-1. Reverse polarity protection is provided by diode CD7.



RC-5447

Figure 1 - System Control/Synthesizer Location (Top View)

The 13.8 Volts from J101-1 is applied to J705-1. This input is applied to the power on-off relay K601 through J601. A continuous 13.8 Volts supply is applied to the Power Control circuit (IC607, IC611) and 5-Volt regulator IC606.

Pressing in the power-on switch energizes power relay K601. Energizing this relay applies a switched 13.8 Volts to 5-volt and 9-volt regulators IC101, IC207, IC501, IC607 and IC608. Switched 13.8 Volts is also applied to Audio PA module IC603.

Digital Processing

The digital processing circuitry consists of microprocessor IC701, octal latches IC702, IC706, IC707 and IC709, EPROM IC703 and EEPROM IC704. IC703 is an 8K X 8-Bit EPROM and is used by the microcomputer to control all radio and system functions. Crystal X701 and inverter IC710 provide the time base to sequence the microcomputer through an internal software program, allowing it to execute the program stored in the program memory (refer to Figure 2 - System Control 1 Block Diagram).

EEPROM IC704 contains all data unique to the radio and is referred to as the "Personality" PROM. Information stored in the Personality PROM includes data for RF channels and Channel Guard tones as well as all radio options (e.g. carrier control timer,...etc.).

Operation:

Octal Latches IC702, IC706, IC707 and IC709

Octal latches IC702, IC706, IC707 and IC709 are used to exchange data passing between microprocessor IC701 and the memory and control circuits respectively. Octal latch IC709 provides the interface between the microprocessor and the control panel switches. IC709 is connected so that the latch function is disabled (the "G" input IC709-11 is connected to +5 volts) and the octal latch operates as a buffer for the microprocessor input.

Latch IC706 provides an output interface for the microprocessor. This latch controls the DPTT, watchdog timer, electronic volume control, RX MUTE and squelch switching. The "G" latch control input is connected to decoder IC705-10.

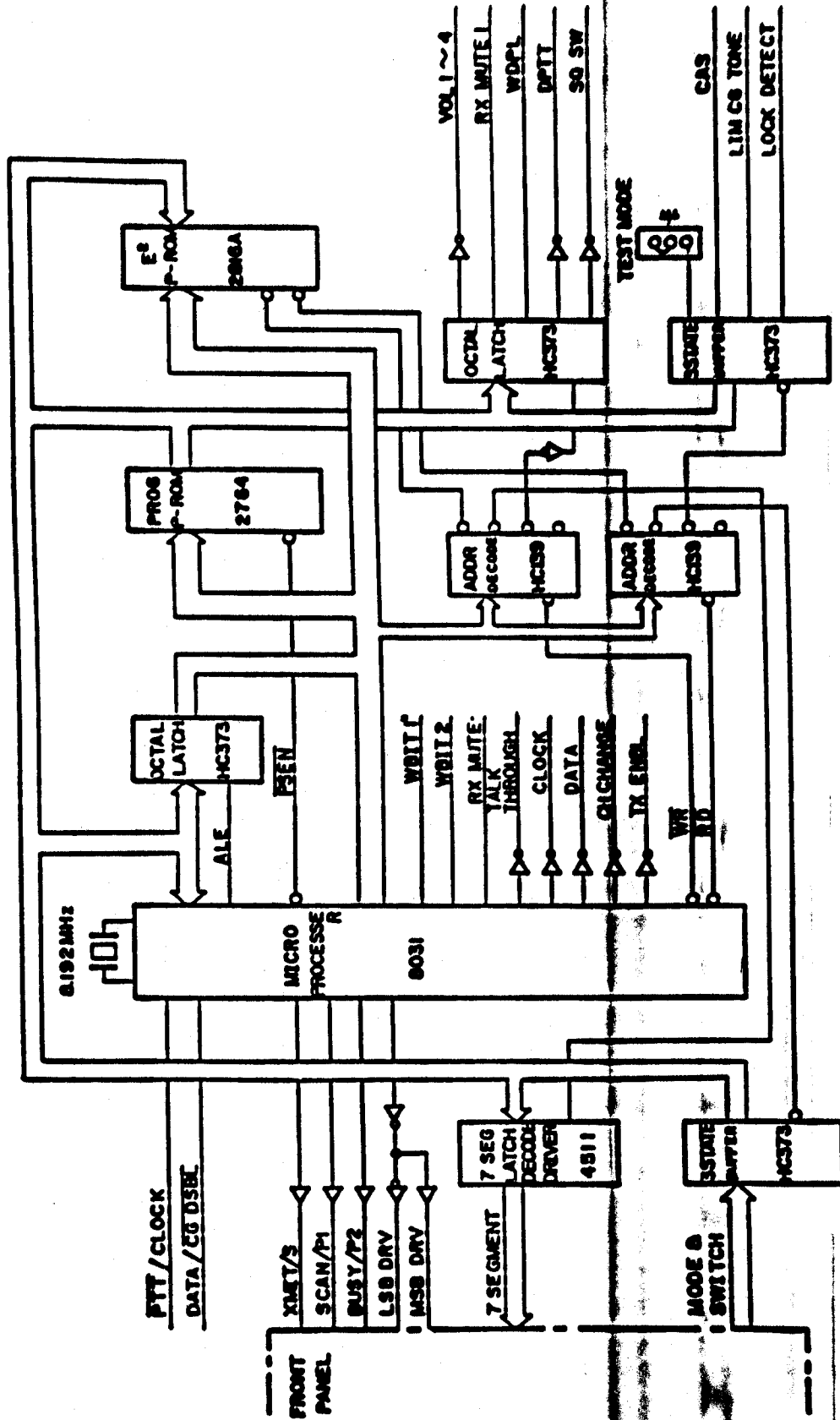


Figure 2 - System Control 1 Block Diagram

Octal latch IC702 has the "G" input connected to the Address Latch Enable (ALE) output of the microprocessor to provide a latched address interface between the microprocessor and program memory IC703.

Reset/Memory Backup

The microprocessor reset circuit consists of 5-volt regulator IC608, zener diode CD604, switching transistors TR603 and TR605 and pass transistor TR604. Microprocessor IC701 is reset by switched A+ (13.8 volts) on/off, watchdog timer reset. The microprocessor resets when +5 volts is applied to IC701-9 (RST) input from regulator IC608 through pass transistor TR604.

When the radio is turned on (A+ SW on) zener diode CD604 conducts, turning on TR603. Transistor TR603 turning on, turns TR605 and TR604 off. When the voltage at IC701-9 becomes "0" volts, the microprocessor starts executing program memory.

Watchdog Timer

The watchdog timer circuit consists of switch transistor TR606 and timer IC609. The timer monitors the operation of microprocessor IC701 and generates a watchdog pulse if the microprocessor fails to function properly. When the microprocessor is operating properly, watchdog pulses from octal latch IC706-15 are applied to the base of switch TR606 through a delay network consisting of resistors R645, R646 and capacitor C624. Turning on TR606 applies +5 volts to IC609-2,6. This holds the clock timer output of IC609-3 low, which holds the microprocessor reset line to the base of pass transistor TR604 high, turning off TR604. Turning off TR604 grounds the microprocessor input at IC701-9, keeping microprocessor IC701 in the operating state.

When the microprocessor is not operating properly, the reset pulses from IC706-5 are not present. Transistor TR606 will turn off and timer IC609 will generate a square wave output at IC609-3 to reset the microprocessor.

Microprocessor

Microprocessor IC701 directly interfaces with and controls the operation of all the digital processing circuitry. It also interfaces with the radio and control panel functions through octal latch IC709 and external buffer stages. Microprocessor IC701 responds to manual initiated functions of Push-To-Talk (PTT), frequency selection (ADD, DELETE), MONITOR, VOLUME and SCAN ADD and DELETE through octal latch IC709. Other

functions are performed automatically by the microprocessor.

The microprocessor controls the operation of the radio by performing the following major functions:

- System Timing
- Frequency Selection
- Receiver Scan (16 channels)
- Two-Channel Priority
- Tone Generation and Detection
- Transmit/Receive Control
- Front Panel Controls and Displays
- Audio Routing and Mute Control

Microprocessor IC701 is sequenced through its program by an internal 8.192 MHz oscillator controlled by crystal X701. The microprocessor accesses its program from EPROM IC703. Reading of the stored program at IC703 occurs when the PSEN line of IC701 is low. The upper eight address lines of IC701 (A8 through A15) are stationary during this access time. The lower eight address lines of IC701 (AD0 through AD7) are captured by octal latch IC702 and held stationary. ALE (IC701-30) is used to latch the lower eight address lines. The output of IC703 is then read into the data bus (AD0 through AD7) of IC701.

The microprocessor interfaces with the microphone through MIC PTT and LOGIC HKSU. It also interfaces with Suitcase Programmer TQ2310 through HKSU, MIC PTT, SER DAT and STORE, and with Personality EEPROM IC704. The microprocessor control signals include the following:

- EA - When this Enable line is low, allows the microcomputer to retrieve all instructions from external memory.
- $\overline{\text{RST}}$ - Resets the microcomputer to beginning of the software program when switched A+ is turned off, immediately following power interruptions or with low battery voltage.
- SYN DATA - Data transferred to synthesizer representing RF frequencies.
- SYN CLOCK - Timing output to synthesizer.
- SYN LOCK - A status input signal from the synthesizer to indicate frequency lock status of VCO.

- RX MUTE** - Receiver Mute turns receiver audio off while operating in the trunked mode during channel acquisition (idle and wait mode) and when transmitting.
- DPTT** - Delayed PTT energizes the antenna relay. DPTT low switches off the bilateral audio gates on the System Control/Synthesizer Board in the transmit and receive mode.
- TX ENBL** - TX ENBL low turns transistor TR105 on and applies 9 volts to the exciter.
- MIC PTT** - The microprocessor monitors the status of the switched PTT lead from the microphone. It also receives clock data on this line while the radio is being programmed.
- RD, WR** - Read, Write allows the microprocessor to read/write data to/from EEPROM IC704 and read/write from/to digital processor IC705.
- PSEN** - Program Send Enable allows the processor to read instructions from program memory IC703.
- ALE** - Address Latch Enable allows the microcomputer to hold the eight least significant lines (AD0 through AD7) stable by using octal latch IC702. This is necessary when reading from program memory IC703 or reading/writing from/to EEPROM IC704.
- A8 - A15** - Eight significant address lines. These lines are used to address and access program memory IC703 and EEPROM IC704. Octal latch IC702 holds the outputs stable.

Push-To-Talk

Pressing the PTT switch on the microphone applies a ground through J701-2 on the System Control 1 Board (CMC-404) to microprocessor IC701. The ground on IC701-10 causes the DPTT output at IC701-1 to go low and the RX MUTE output at IC701-2 to go high.

The low DPTT output of IC706-16 is applied to the input of inverter IC710-13 and the input of inverter transistor

TR711. The high output at IC710-12 becomes the low outputs DPTTI and DPTT through inverter transistors TR709 and TR710 respectively. The high output of TR711 becomes DPTT. DPTTI and DPTT are applied to the synthesizer, exciter/PA board and the audio circuitry. The low output at TR710 is applied to the exciter/PA board from J705-7 and operates antenna relay K1. The DPTT output and the DPTTI output are supplied to the synthesizer circuit to turn the RX VCO off and TX VCO on. Also the low DPTTI output at TR709 is added to the bilateral switch IC604 in the audio circuit to change the operating mode from receive to transmit. TX ENBL is low and through J705-8 is connected to the exciter/PA board to apply 9 volts to the exciter and key the transmit circuit.

Channel Select

When a channel is selected and the bit stream is loaded into the synthesizer, a strobe pulse is applied to the Phase-Lock-Loop (PLL) module to allow the synthesizer to generate the correct RF frequency. The microprocessor immediately begins monitoring the LOCK DET LINED to verify that the synthesizer is "on" frequency. If the synthesizer is not locked on the correct frequency, a low on the LOCK DET line will cause the microprocessor to reload the synthesizer in an attempt to lock it on frequency. If the synthesizer is locked on the correct frequency and MIC PTT is low, the microprocessor applies the high to the input of inverter transistor TR713. The low output of TR713 (TX ENBL) is connected to the exciter/PA board through J705-8 to key transmit circuit.

Monitor

Pressing the MONITOR pushbutton applies a low to the microprocessor through octal latch IC709-13. This low causes the microprocessor to open the receive so the channel can be monitored.

Channel Guard

In the encode mode, the microprocessor selects the assigned Channel Guard tone information from the EEPROM memory for each transmit and receive channel and generate the Channel Guard signal. This signal is applied as Walsh Bits "1" and "2" to summing amplifier IC610-D. These two bits are summed together and filtered to provide a smooth sine wave for Tone Channel Guard.

The output of IC610-D is applied to low-pass filter (Voice Reject) HC602. This filter shunts all frequencies above 300 Hz to ground, preventing those frequencies from interfering with the encoded signal.

In the decode mode, the DPTT input to bilateral switches IC604 is high, changing the switches to the receive mode. Audio and tone from RX AUDIO at J601-24 is applied to low-pass filter (Voice Reject) HC602 through buffer amplifier IC610-A. This signal is filtered and only the Channel Guard tone (if present) is applied to hard limiter IC610-B.

The square-wave output of IC610-B is connected to transistor switch TR609 and the Channel Guard tone is applied to the microprocessor for comparison to determine if the Channel Guard tone is correct. If the tone is correct the microprocessor causes the RX MUTE line to go low at J601-12, turning the receiver audio on so that the message can be heard in the speaker.

Carrier Control Timer

The Carrier Control Timer (CTT) is contained in and controlled by the microcomputer. Each time the PTT switch is activated an internal counter begins to count down. If the counter times out, a 500 Hz tone is heard in the speaker for five (5) seconds or until the microphone PTT is released. The timing cycle is programmable from 30 seconds to three (3) minutes in 30-second increments.

EEPROM "WRITE" Control

The EEPROM "WRITE" (WR) control consists of transistors TR715 and TR716. When address bit A9 or A10 from the microprocessor is high, TR716 turns on and TR715 turns off. This applies +5 volts to the WR input which disables the "WRITE" function to protect the channel frequency information. When the address bit A9 or A10 goes low, TR716 turns off and TR715 turns on. This applies a low to the WR input, enabling the "WRITE" function (if EEPROM WR is low from the decoder) which allows data to be written to the EEPROM. To WRITE to the memory, the WR input must be low and the OE input must be high. In the RD (Read) mode, WR is high, OE is low and CS is low. The WR function can also be enabled by a low from Suitcase Programmer TQ2310 through SP STORE.

Audio Circuitry

Transmit and receiver audio signals are routed to and from the Control 2 (CMC-405) Board through three-stage bilateral switches IC604-C (refer to Figure 3 - System Control 2 Block Diagram). The switches are controlled by the RX MUTE 1 output of microprocessor IC701. In the transmit mode, the RX MUTE 1 from IC708 is high, TR610 turns on, bilateral switch IC604 control lead is low, switching the stages to the transmit

mode as shown on the Control 2 Board Schematic Diagram. When the PTT switch is released, the switches revert back to the normal receive mode (DPTT high).

The +5 volts from regulator IC607 is applied to voltage divider resistors R649 and R650. The +4.5-volt output of the voltage dividers establishes the reference voltage for the operational amplifiers. Capacitor C630 provides an AC ground at the summing input of operational amplifier IC610-C.

Transmit Audio

Audio from the microphone at J701-3, 4 (MIC H, 10) is coupled through capacitor C258 and Audio Processor IC208-B and applied to a high-pass filter. The filter output is coupled through capacitor C230 and Modulation Adjust potentiometer RV201 to the next stage.

The Channel Guard tone (if present) from Voice Reject Filter HC602 is coupled through bilateral switch IC604-A and applied to the CG input of Channel Guard Modulation Adjust potentiometer RV202. The Channel Guard tones and audio are combined and applied to summing amplifier IC208-A.

Receive Audio

In the receive mode, the PTT input to the System Control/Synthesizer Board goes low, switching antenna relay to the receive mode. The RX MUTE lead remains high, keeping the audio amplifier turned off.

If the channel being received has been programmed for Channel Guard, the received CG tone is coupled through bilateral switch IC604-B and buffer amplifier IC610-D to low-pass filter (Voice Reject) HC602. The filtered tone output is coupled through IC610-A, limiter IC610-B and transistor TR609 to the microprocessor.

Received audio from the receiver is applied to the input of buffer amplifier IC601-A. The audio out from IC601-A is applied to the volume control circuit (IC602 and IC601-C) through tone reject filter HC601, audio gate IC604-C and audio pre-amplifier IC601-B. The audio output from the volume control circuit is applied through the de-emphasis network, consisting of resistors R628 and R618 and capacitors C609 and C605, to audio amplifier IC603 which provides up to 4-watts of audio output power to 4-ohm speaker SP801, located in the front panel.

When the radio is squelched, the Carrier Activated Switch (CAS) signal to the microprocessor through J706-5, goes

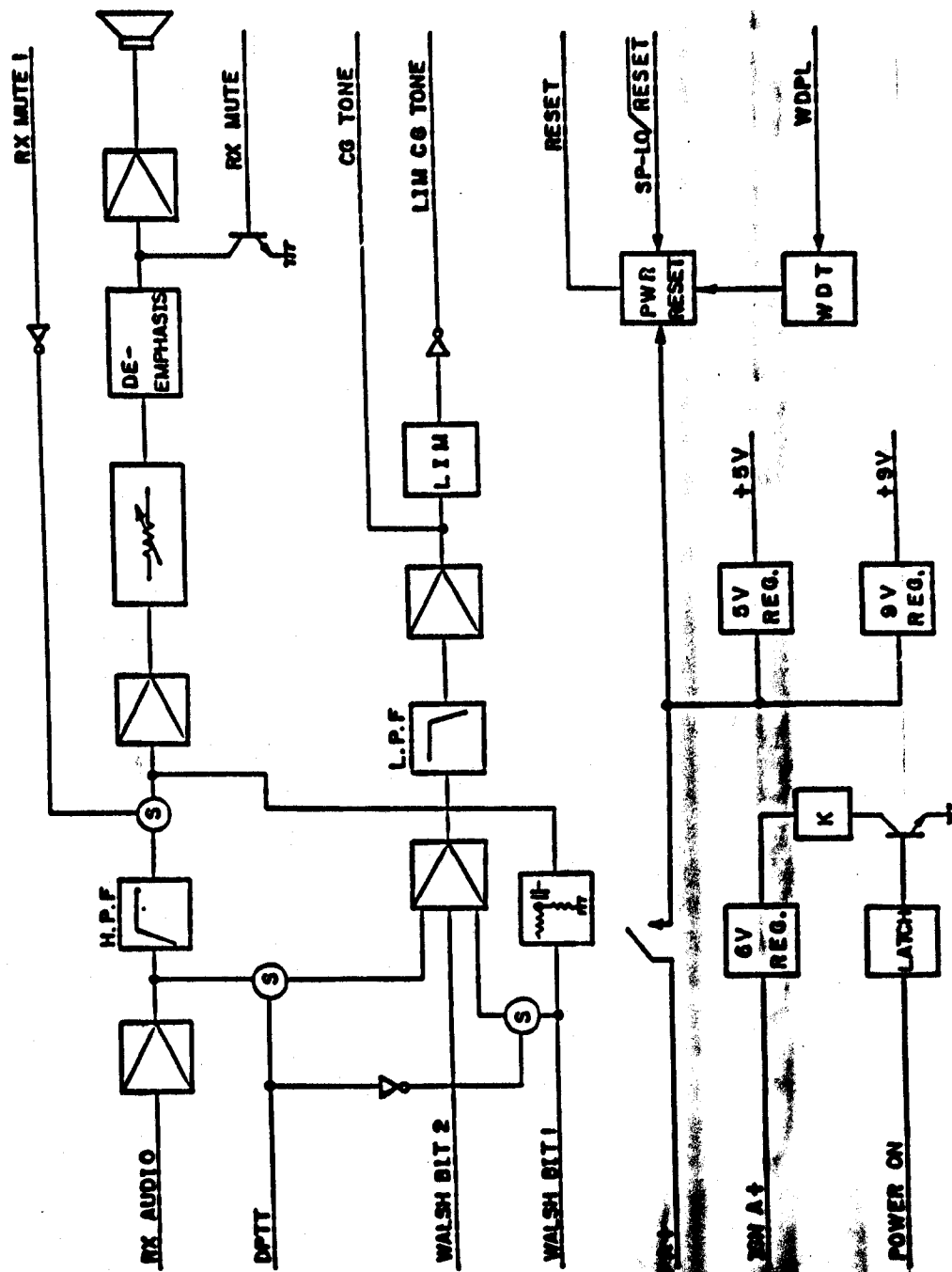


Figure 3 - System Control 2 Block Diagram

low. The microprocessor outputs the RX MUTE and RX MUTE 1 signals. The RX MUTE signal turns bilateral switch IC604-C off and mutes the audio signal. The RX MUTE signal turns transistor TR601 off and mutes the audio signal from IC601-C.

9-Volt Regulator

The 9 volt regulator provides power for the audio circuits on the System Control/Synthesizer Boards. The regulator operates from the 13.8-volt ignition switch voltage. The 9 volts DC output of the regulator is applied to the microphone through J701-3, 4 (MIC HI, LO) on the System Control/Synthesizer Boards.

Frequency Synthesizer

The frequency synthesizer circuit consists of reference oscillator XU201, synthesizer chip IC201, dual modulus pre-scaler IC202, TX and RX Voltage-Controlled Oscillators (VCO's), transistors TR202 and TR209, a loop filter and associated circuitry (refer to Figure 4 - Synthesizer Block Diagram).

Reference oscillator XU201 operates at a frequency of 12.8 MHz and is temperature compensated to provide a frequency stability of ± 5 PPM. Voltage for the oscillator is supplied by 9-Volt regulator IC207 and 4-Volt zener diode CD201. The oscillator output is applied to synthesizer chip IC201-2 (refer to Figure 5 - Synthesizer IC201).

Synthesizer IC201 consists of a programmable reference oscillator (divider $\div R$), phase detector and programmable VCO dividers ($\div N, A$).

When the PTT switch is pressed (transmit) or released (receive) new frequency data is received on the clock, data and enable lines and the synthesizer immediately begins generating the new RF frequency. This serial data determines the VCO frequency by setting the internal dividers. The reference oscillator frequency applied to the programmable reference oscillator divider is divided down to some lower frequency as indicated by the input data and applied to the internal phase detector. The phase detector compares this signal with the output of the internal programmable VCO dividers. The output of the programmable VCO dividers is a function of the RF frequency which is divided down by the dual modulus pre-scaler and the programmable VCO dividers. When operating on the correct frequency, the inputs to the phase detector are identical and the output voltage of the phase detector is constant. Under these conditions, the VCO is stabilized or locked on frequency.

If the compared frequencies (phases) differ, an error voltage is generated and applied to the VCO through the frequency acquisition circuit, causing the Phase-Lock-Loop (PLL) to acquire the new frequency.

The LOCK DETECT (LD) line provides the PLL lock status information to the microcomputer. When the PLL is out of lock, the LOCK DETECT lead is low. When locked on frequency the lead is high.

DC offset buffers TR202, TR204 and TR205 receive the error voltage from the synthesizer and increases this level by 1.8 VDC to extend the operating range of the high current buffers. When the PLL is off frequency due to a channel change or frequency drift the error voltage from the synthesizer (APD) rises or falls turning TR202 on or off. TR202 controls the DC offset buffers TR205 and TR204 and high current buffers TR203 and TR201. TR203 and TR201 complete a high current rapid charge path for C206-C208. TR204 and TR205 provide the rapid discharge path.

As the error voltage decreases TR202, TR205 and TR204 turn on completing a discharge path for C206-C208 through bilateral switches IC203. When the error voltage goes positive TR202, TR204 and TR205 are turned off, allowing C206-C208 to charge through TR203 and R205-R206. IC203 is turned on for 15 milliseconds each time a channel is changed in receive or when changing from transmit to receive. The time is 15 milliseconds when in transmit.

The loop filter consists of R205-R207, and C206-C208. This filter controls the bandwidth and stability of the synthesizer loop. Bilateral switch IC203 is controlled by the 15 milliseconds, 9-volt channel change pulse. When the channel change pulse is present the bilateral switch shorts out the low pass filter greatly increasing the loop bandwidth to achieve the 35 milliseconds channel acquisition time required for PSLM. The low pass filter removes noise and other extraneous signals internal to the synthesizer chip.

The output of the filter is applied to the varicaps in the transmit and receive VCO's to adjust or correct the VCO frequency.

The Receiver VCO consists of a low noise JFET oscillator, TR206, followed by high gain buffer IC205. This buffer prevents external loading and improves power gain. The VCO is a Colpitts oscillator with the varicap capacitors and inductor forming the tank circuit. Capacitor CV201 allows manual adjustment of the VCO across the frequency split. The varicap provides voltage controlled

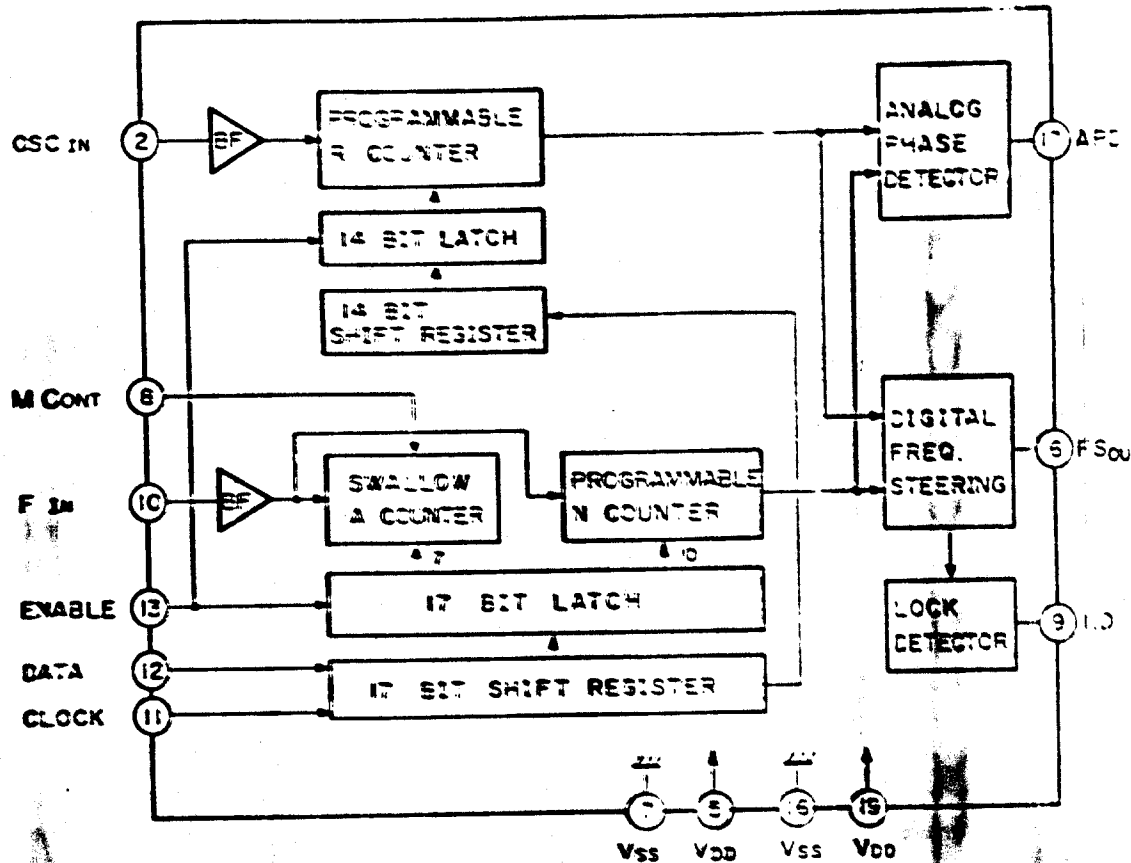


Figure 5 - Synthesizer IC201

frequency adjustment of about 3 MHz. The VCO is switched on and off under control of the DPTT line. When the DPTT line is high the Receiver VCO is turned on (TR207 is on). The RX injection output is typically 0 dBm. RX VCO lock time is 15 milliseconds maximum.

The transmit VCO is basically the same as the Receiver VCO except that capacitor CV202 is turned to provide an operating range of approximately 10 MHz, depending on which frequency split the radio is operating on. The varicap provides a voltage controlled adjustment range of approximately 6 MHz. The TX injection provides a typical output of 0 dBm. Transmit audio is applied to modulation adjustment control RV201. Deviation is set for 4.5 KHz. TX VCO lock time is 15 milliseconds maximum.

TX VCO control switch TR210 turns the Transmit VCO on when DPTT is high. TR210 is on.

The use of two VCO's allows rapid independent selection of transmit and receive frequencies across the frequency split.

VCO Characteristics:

The synthesizer has two VCO's, the frequency of which is directly related to a control voltage generated by the synthesizer circuitry and must remain within specified limits for the synthesizer to function properly. The RX VCO typically will increase in frequency about 3 MHz when the control voltage moves from its lower limit to its upper limit. The TX VCO moves about 6 MHz for the same situation. By tuning the variable capacitor in the VCO, the same control voltage frequency spread can be moved up or down through the full range of frequencies that the radio operates on.

In order to maintain the selectivity and hum and noise performance of the radio, the frequency range that the VCO's can be voltage tuned must be kept to a minimum. This requires that all the available voltage range be fully utilized. The alignment procedure, therefore, instructs the user to accurately set the control voltage to the upper limit of the voltage range at the highest frequency channel.

NOTE

Going too high with the voltage setting at the highest frequency channel may cause problems over temperature extremes as the VCO's will drift slightly. Set the voltage too low and you may not remain within the required lower voltage limit as you cover the radio's maximum two frequency spread.

If the required frequency spread is less than the maximum two frequency spread, then there are no restrictions on setting the lowest and highest frequencies within the required voltage limits.

The minimum tuning requirement of the VCO's is to cover the proper frequency range. For instance, to cover 160 to 166 MHz the VCO must be tunable such that at 160 MHz the control voltage is at least greater than or equal to the lower voltage limit, and at 166 MHz the voltage must be less than the upper limit. If the control voltage can be tuned higher than the lower limit at 160 MHz, this simply means that you can program channels below 160 MHz until you finally run into the lower voltage limit. When tuning the VCO's to a channel close to 166 MHz, the control voltage may not reach the upper control voltage limit. This is normal for some radios and is due to the tolerances on the many capacitors in the VCO. Even though it takes very little change in capacitance to shift the VCO frequency range a few megahertz, this variation has been carefully compensated for by increased tuning range for the VCO. Therefore, if you tune to 174 MHz, you may not achieve the maximum control voltage for all radios, but you will always be greater than the lower voltage limit.

Feedback Buffers:

The RX injection and TX injection voltage output from the RX VCO and TX VCO are supplied to the receiver mixer and the exciter respectively and to the feedback buffer. Buffering is provided by IC204 and the output applied to dual modulus prescaler IC202.

The dual modulus prescaler completes the PLL feedback path from the synthesizer to loop filter, to the VCO's and feedback buffer and then back to the synthesizer through the prescaler. The prescaler divides the VCO frequency by 64 or 65 under control of N Cont from the synthesizer. The output of the prescaler is applied to the synthesizer where it is divided down to 5 or 6.25 MHz by an

internal N, A counter and compared in frequency and phase with the divided down frequency from the reference oscillator. The result of this comparison is the error voltage used to maintain frequency lock. The N, A counter is controlled by data received from the microcomputer. Depending on the operating frequency, the IC voltage at TP201 should be within the range 3.5 and 7.5 VDC when the PLL is locked.

The audio processor provides audio pre-emphasis with amplitude limiting and post limiter filtering and a total gain of approximately 27 dB. Approximately 30 dB gain is provided by IC208B and 4 dB by IC208A and -7 dB by R246, R249.

The 9-Volt regulator IC207 powers the audio processor and applies regulated 9 volts to a voltage divider consisting of R245 and R246. The +4.5 V output from the voltage divider establishes the operating reference point for operational amplifiers IC208B and IC208A. C261 provides an AG ground at the summing input of both operational amplifiers.

When the input signal to IC208B-6 is of a magnitude such that the amplifier output at IC208B-7 does not exceed 5 volts PP, the amplifier provides a nominal 0 dB gain. When the audio signal level at IC208B-7 exceeds 5 volts PP, the amplification gain is reduced to 1. This limits the audio amplitude at IC208B-7 to 5 volts PP.

Resistors R242, R243 and Capacitor C258 comprise the audio pre-emphasis network that enhances the signal-to-noise ratio. R243 and C258 control the pre-emphasis curve below limiting. R242 and C258 control the cut-off point for high frequency pre-emphasis. As high frequencies are attenuated, the gain of IC208 is increased.

Audio from the microphone is coupled to the audio processor through R242 and C254.

The amplified output of IC208B is coupled through R248, R250, R252 and R253 to a second operational amplifier IC208A. TR215 is controlled by the DPTT line so that TX audio is transmitted only when the PTT is depressed.

The Channel Guard tone input is applied to IC208A through CG Mod Adjust RV202, C262 and C254. The CG tone is then combined with the microphone audio at IC208A. IC208A provides a signal gain of approximately 12 dB.

A post limiter filter consisting of IC208A, R250-R253, C262 and C265 provide 12 dB per octave roll-off. R248 and C260 provide an additional 15 dB per octave roll-off for a total of 18 dB. The

output of the post limiter filter is coupled through Mod Adjust RV201 to the transmitter VCO.

TX enable switch TR215 shorts out operational amplifier IC208-A when the radio is in the receive mode. The DPTT signal is generated by the microcomputer when the PTT switch is released and is 9 VDC in the receive mode.

SCAN Operation:

The scan operation is controlled by the microprocessor, and provides for scanning any or all of up to 16 channels. The scanned channels may be located anywhere within the frequency band of the radio, and can include two priority channels (P1 and P2).

If desired, all 16 channels can be scanned with or without priority level.

Example 1: (More than four non-priority channels, i.e., six channels)

P1-P2-S1-S2-S3-S4-P1-P2-S5-S6-S1-S2-P1-P2-S3-S4-S5-S6-P1-P2-...

Example 2: (Four or less non-priority channels, i.e., three channels)

P1-P2-S1-S2-S3-P1-P2-S1-S2-S3-P1-P2-S1-S2-S3-P1-P2-S1-S2-S3-...

Therefore, the scan sequence is: Scan P1 and P2 if programmed. Then scan up to four non-priority channels before scanning P1 and P2 again. If more than 4 non-priority channels exist, then scan will wrap around, continuously scanning four channels of the non-priority list between each P1, P2 scan sequence. If the number of non-priority channels is less than or equal to four, then all non-priority channels will be scanned between each P1, P2 scan.

As an added example, consider channels 1-8 to be the scanned channels, with P1 being Channel 1 and P2 being Channel 8. The scanning order then would be:

S1-S2-S3-S4-P1-P2-S5-S6-S1-S2-P1-P2-S3-S4-...
7 6 5 4 1 8 3 2 7 6 1 8 5 4

Since it takes approximately 50 to 450 milliseconds to scan each channel, then each Priority channel is sampled every 0.3 to 2.7 seconds and the Non-Priority channels are sampled at least once every 0.4 to 3.6 seconds. If Channel Guard is programmed for a channel but no carrier is detected, the scan time for that channel is 50 milliseconds.

SCANNING (Stopped On A Valid SCAN Channel):

Once a carrier is detected, the Receive Channel display will light up, indicating that channel. If the channel is a Non-Priority channel, and there are no Priority channels, then scanning is halted. If only a Priority 2 (P2) channel is present, then it is scanned every 5 seconds if it has Channel Guard programmed and carrier is detected, and every second otherwise. If there is only a Priority 1 (P1) channel, then it is sampled every 2.5 seconds if it has Channel Guard 1 (P1) and carrier is detected, and every 500 milliseconds otherwise. If there are P1 and P2 Priority channels, the sample rate will vary.

In order to show the various scan conditions, the following conditions are used:

NOTE

The following conditions are shown while listening to a non-priority channel.

CONDITION 1: P1 And P2 Have Channel Guard Programmed

a. No carriers detected

P1-P1-P2-P1-P1-P2-P1-P1-P2-...

tb (time between samples) = 500 msec
 ts (time of sample) = 100 msec

Note: ts is the hole time placed in the signal being heard.

b. Carrier on P1 detected/wrong Channel Guard

P1-P2-P2-P2-P2-P2-P1-P2-P2-P2-P2-P2-P1-P2-...

tb = 1 second
 ts = 100 msec for P2
 250-500 msec for P1

c. Carrier on P2 detected/wrong Channel Guard

P1-P2-P1-P1-P1-P1-P1-P1-P1-P1-P1-P2-P1-...

tb = 500 milliseconds
 ts = 100 milliseconds for P1
 250-500 milliseconds for P2

d. Carrier on P1 and P2 detected/both wrong Channel Guard

P1-P1-P2-P1-P1-P2-P1-P1-P2...

tb = 2.5 seconds
 ts = 250-500 msec

e. Carrier on P1 and right Channel Guard

Stop scan, display P1

f. Carrier on P2 and right Channel Guard

Display P2, scan P1

P1-P1-P1-P1-P1-P1-...

tb = 500 msec
 ts = 100 msec

g. Carrier on P2 with right Channel Guard, carrier/wrong Channel Guard P1

P1-P1-P1-P1-P1-...

tb = 2.5 seconds
 ts = 250-500 msec

CONDITION 2: Priority 1 Has Channel Guard Programmed, PRI 2 Does Not

a. No carriers detected

P1-P1-P2-P1-P1-P2-P1-P1-P2-...

tb (time between samples) = 500 msec
 ts (time of sample) = 100 msec

b. Carrier on P1 detected/wrong Channel Guard

P1-P2-P2-P2-P2-P2-P1-P2-P2-P2-P2-P2-P1-P2-...

tb = 1 second
 ts = 100 msec for P2
 250-500 msec for P1

- c. Carrier on P1 detected/right Channel Guard
Stop on P1, stop scan
- d. Carrier on P2
Stop on P2, scan P1
P1-P1-P1-P1-...
tb = 500 msec
ts = 100 msec
- e. Carrier on P2 and P1 with wrong Channel Guard on P1
Stop on P2, scan P1
P1-P1-P1-P1-P1-P1-...
tb = 2.5 seconds
ts = 250-500 msec

CONDITION 3: P2 Has Channel Guard, P1 Does Not

- a. No carriers detected
P1-P1-P2-P1-P1-P2-P1-P1-P2-...
tb (time between samples) = 500 msec
ts (time of sample) = 100 msec
- b. Carrier on P2 detected/wrong Channel Guard
P1-P2-P1-P1-P1-P1-P1-P1-P1-P1-P1-P2-P1-...
tb = 500 milliseconds
ts = 100 milliseconds for P1
250-500 milliseconds for P2
- c. Carrier on P2 detected/right Channel Guard
Stop on P2, scan P1
P1-P1-P1-P1-P1-P1-...
tb = 500 msec
ts = 100 msec
- d. Carrier on P1 detected
Stop on P1, stop scan

CONDITION 4: P1 And P2 With No Channel Guard

- a. No carriers detected
P1-P1-P2-P1-P1-P2-P1-P1-P2-...
tb (time between samples) = 500 msec
ts (time of sample) = 100 msec
- b. Carrier on P2
Display P2, scan P1
P1-P1-P1-P1-P1-...
tb = 500 msec
ts = 100 msec
- c. Carrier on P1
Stop on P1, stop scan

Hang Time:

If the carrier on a Non-Priority channel disappears before a carrier is detected on a Priority channel, then a 5-second hang time is applied before Non-Priority scanning is resumed. However, during this time the Priority channels are still being sampled. The hang time is provided to prevent fades from causing big gaps in the audio signals. The transmitter may be keyed at any time during the hang time. The hang time is restarted when the transmitter is unkeyed.

If a carrier (or Channel Guard tone if programmed) is detected on a Priority channel during the sample period, then the channel is immediately switched to the Priority channel, and either the PRI-1 or PRI-2 indicator will turn on. If the carrier is on Priority 1 channel, scanning is stopped until the carrier goes away (plus the five second hang time). If the carrier is on the P2 channel, then P1 is still sampled every 500 milliseconds if no Channel Guard, and every 2.5 seconds if Channel Guard is programmed. If there is no P1 channel, then scanning is stopped until the carrier disappears (+5 seconds). Once a carrier is detected on the P1 channel, the channel is switched to Priority 1 regardless of what is being received on another channel (Non-Priority or P2).

Other Characteristics:

When the microphone is removed from the hookswitch, scanning will stop and revert to the Pre-Scan selected channel if the scan has not stopped on any channel. The scan light will blink. Transmit (if a valid TX frequency is programmed) is possible on the pre-scan

channel while off-hook. The channels can be changed during this mode, but when the microphone is returned to the hookswitch, hang time occurs on the pre-scan selected channel.

If a channel has been detected and the radio is hanging on this channel, then scanning stops and the radio will sit on the Received scan channel until the microphone is placed on the hookswitch or scan is disabled by pressing the SCAN button. If the microphone is replaced on the hookswitch scanning will resume five seconds later. Channel changes are allowed until the microphone is replaced in the hookswitch. When scan is disabled, the radio automatically reverts to the Pre-scan selected channel.

When the PTT is pressed, the channel that the scan was hanging on when the microphone was removed from the hookswitch will be the transmit channel. This is the displayed channel. If the PTT is pressed while on-hook and is SCAN, the transmitter is disabled until scan stops on a valid channel or scan is disabled.

Once stopped on a channel and the microphone removed from the hookswitch, the Channel Guard decode function is disabled until the microphone is returned to the hookswitch.

When in the scan mode and the channel display blinks while displaying a channel number, this indicates that one of the scan channels is not locking on frequency (not properly programmed, radio not properly aligned, etc.). Slowly stepping through the channels with scan disabled will reveal the bad channel because the channel display will blink on the bad channel only.

GENERAL ELECTRIC COMPANY • MOBILE COMMUNICATIONS DIVISION
WORLD HEADQUARTERS • LYNCHBURG, VIRGINIA 24502 U.S.A.

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COMPONENT SIDE

LEAD IDENTIFICATION
FOR TRANSISTORS
(TOP VIEW)



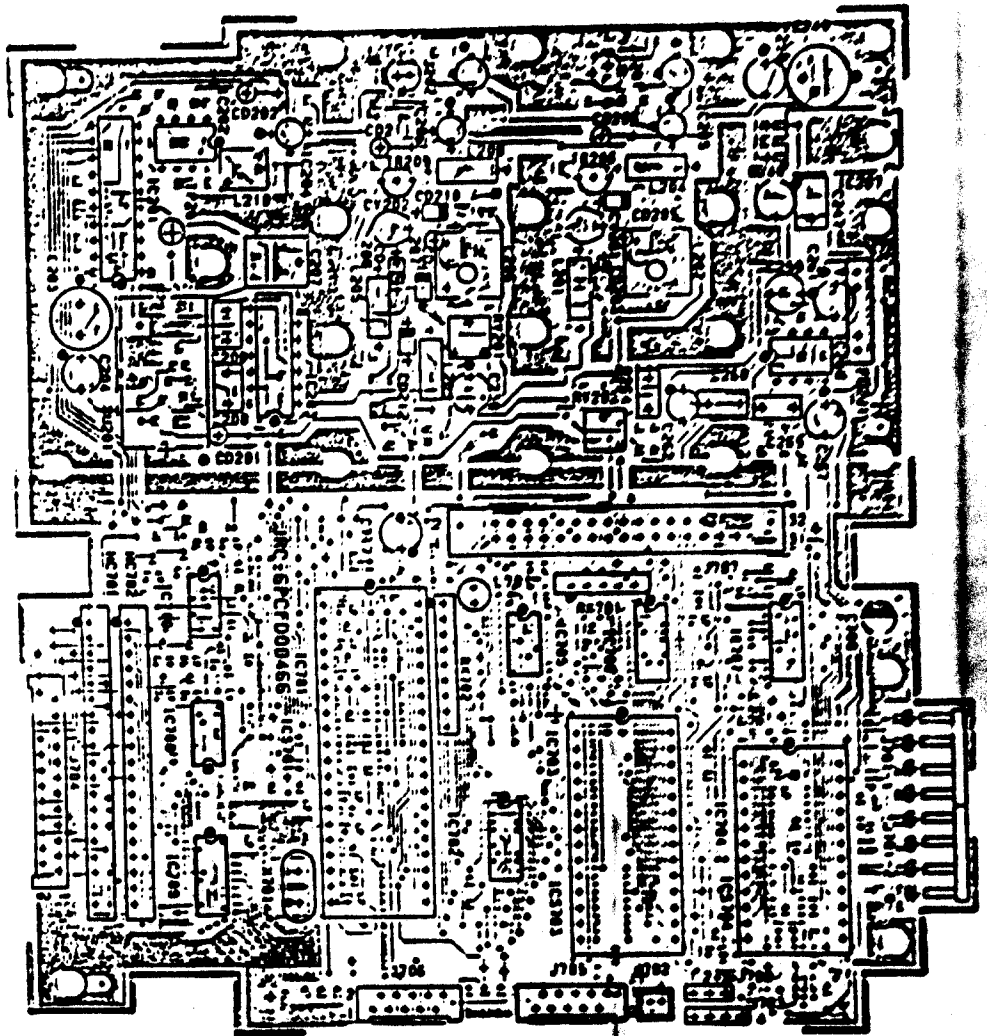
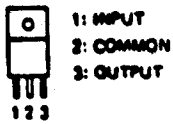
LEAD IDENTIFICATION
FOR DIODES
(TOP VIEW)



LEAD IDENTIFICATION
FOR RV201, RV202
(TOP VIEW)



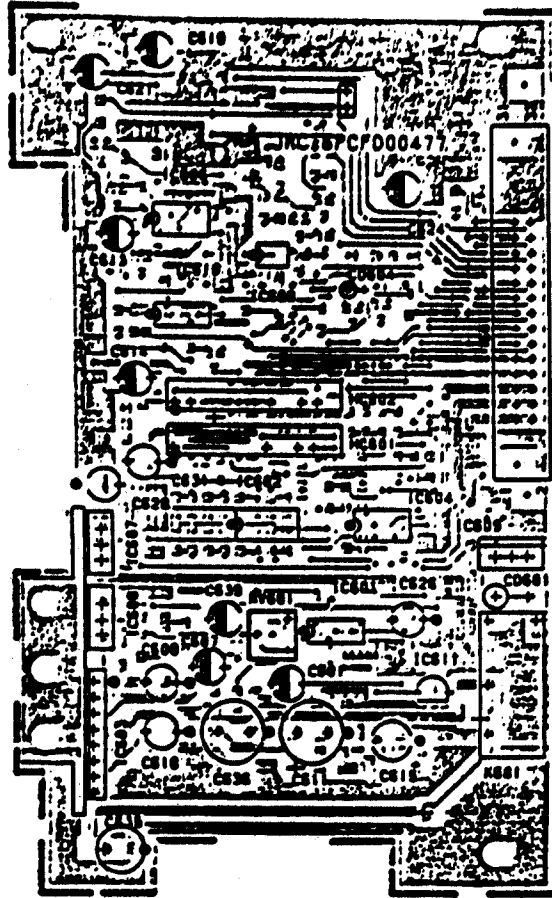
LEAD IDENTIFICATION
FOR IC206
(TOP VIEW)



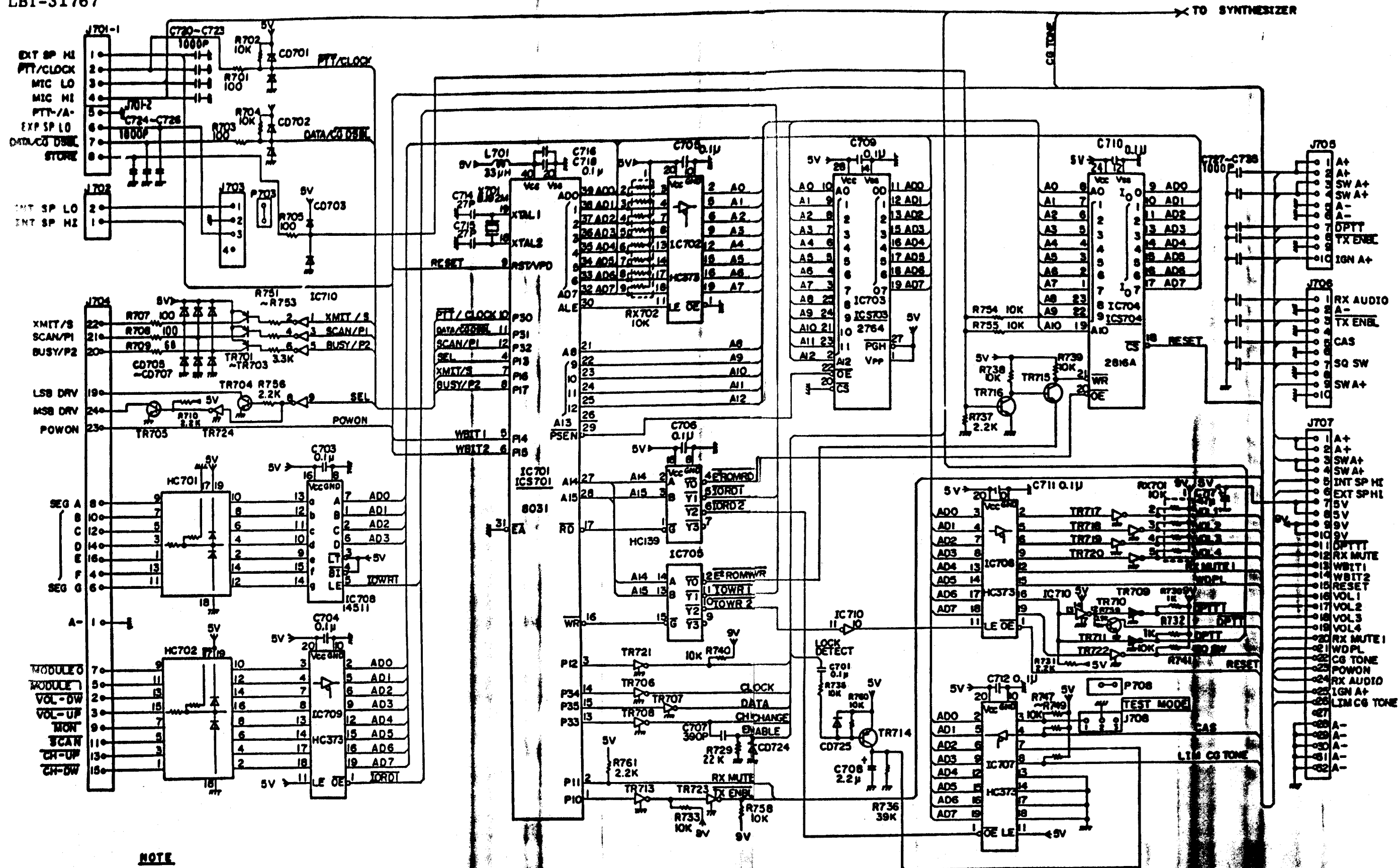
OUTLINE DIAGRAM

CONTROL 1/SYNTHESIZER BOARD

COMPONENT SIDE



OUTLINE DIAGRAM
CONTROL 2 BOARD
Issue 1 17

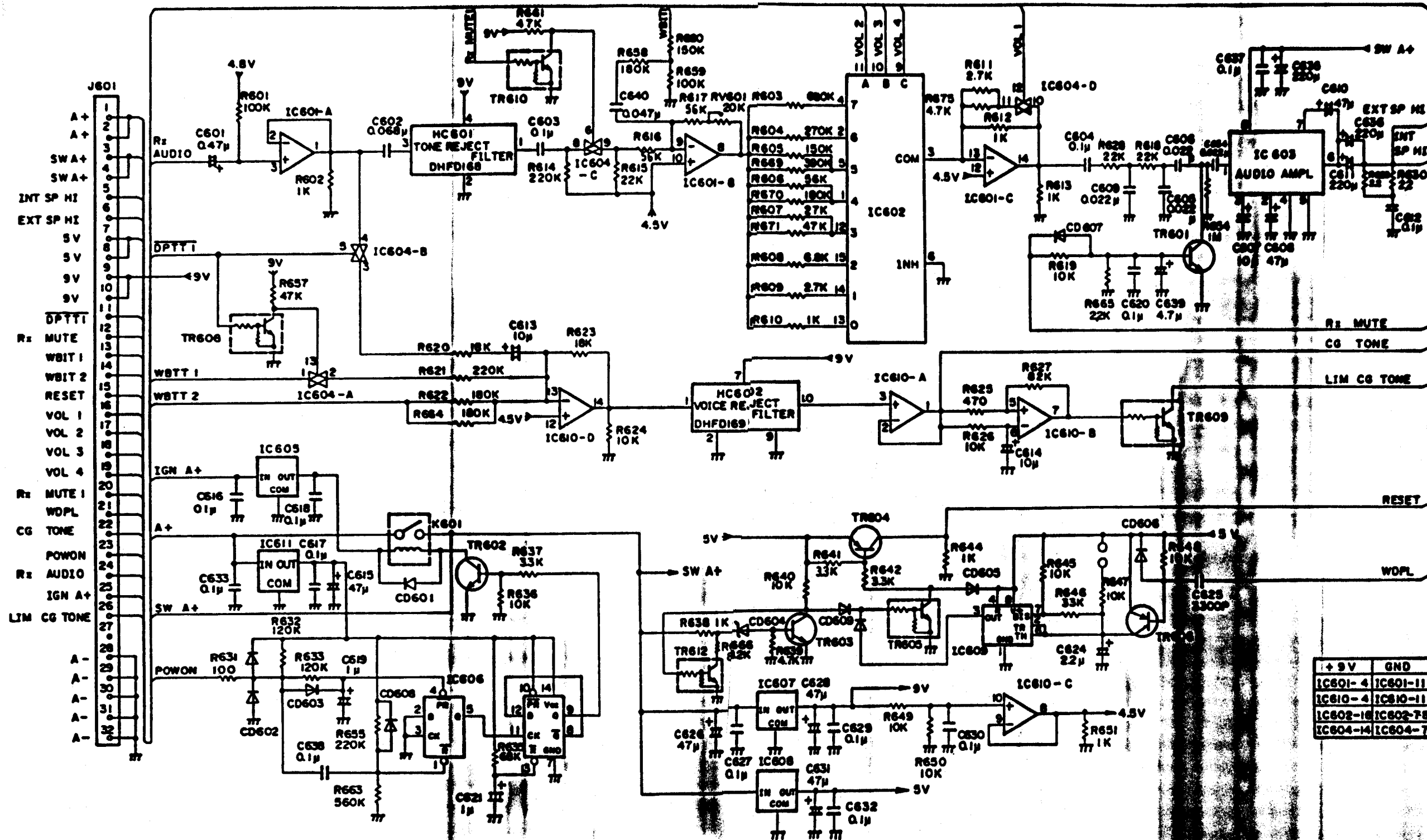


NOTE



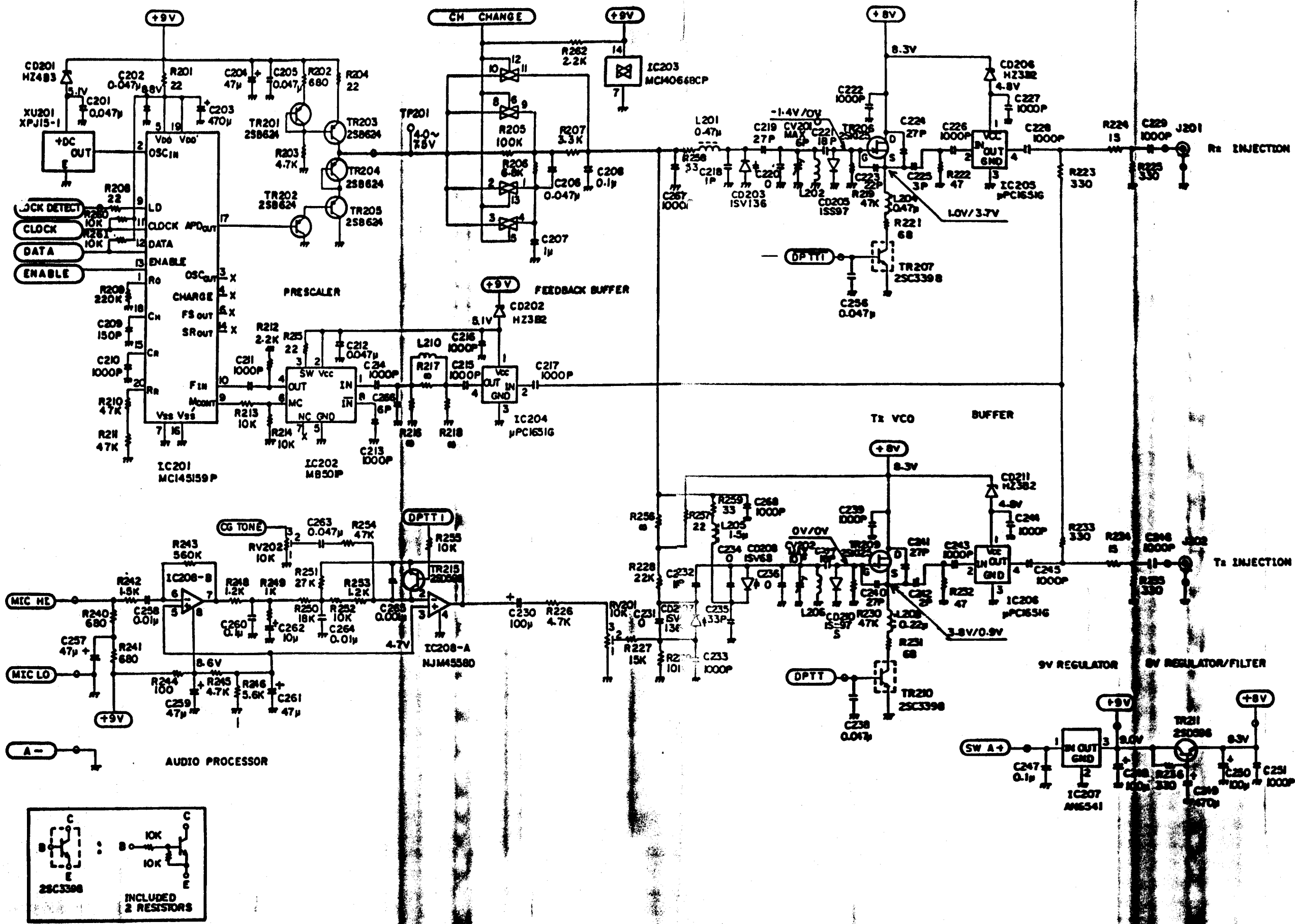
SCHEMATIC DIAGRAM

System Control 1
(DD00-CMC-386-1)



+ 9V	GND
IC601-4	IC601-11
IC610-4	IC610-11
IC602-16	IC602-78
IC604-14	IC604-7

SCHEMATIC DIAGRAM
 System Control 2
 (DD00-CMC-405)
 Issue 1 19



SCHEMATIC DIAGRAM
 150.8 -174 MHz Frequency Synthesizer
 (DD00-CMC-386-2)