Maintenance Manual

EDACS®

TEST AND ALARM UNIT (TAU)

ERICSSON

Ericsson Inc.
Private Radio Systems
Mountain View Road
Lynchburg, Virginia
1-800-528-7711 (Outside USA, 804-528-7711)

Printed in U.S.A.

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SYSTEM DESCRIPTION

INTRODUCTION

The Enhanced Digital Access Communications System (EDACS) Test and Alarm Unit (TAU) is an optional unit at the site which performs three functions for the EDACS system:

- Remote channel monitoring and testing of EDACS stations.
- Remote reporting of inputs from user-supplied alarm sensors.
- Remote control of relays which operate user-supplied devices.

Two functional units make up the TAU: the Alarm and Control Unit (ACU) and the Test Unit (TU). The ACU reports alarm and status input information for control of user-supplied devices, while testing of the EDACS stations is accomplished by the TU. The TAU is directed by the Site Controller. A block diagram of the TAU and Site Controller interconnections is shown in Figure 1.

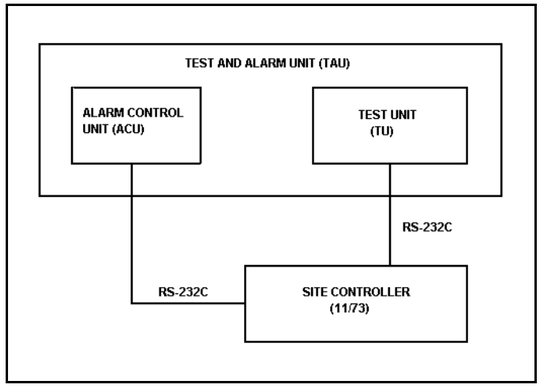


Figure 1 - Test and Alarm Unit

GENERAL DESCRIPTION

Most of the modules making up the TAU are located in a 19-inch equipment rack. A typical rack installation is shown in Figure 2. Mounted on the front panel of the TAU is the Display Assembly, consisting of a polycarbonate display panel, metal panel frame, Display Board, and associated hardware. The front panel is swung down to gain access to the Control Unit (such as an S-550 EDACS), which is mounted on a bracket attached to the rear of the front panel.

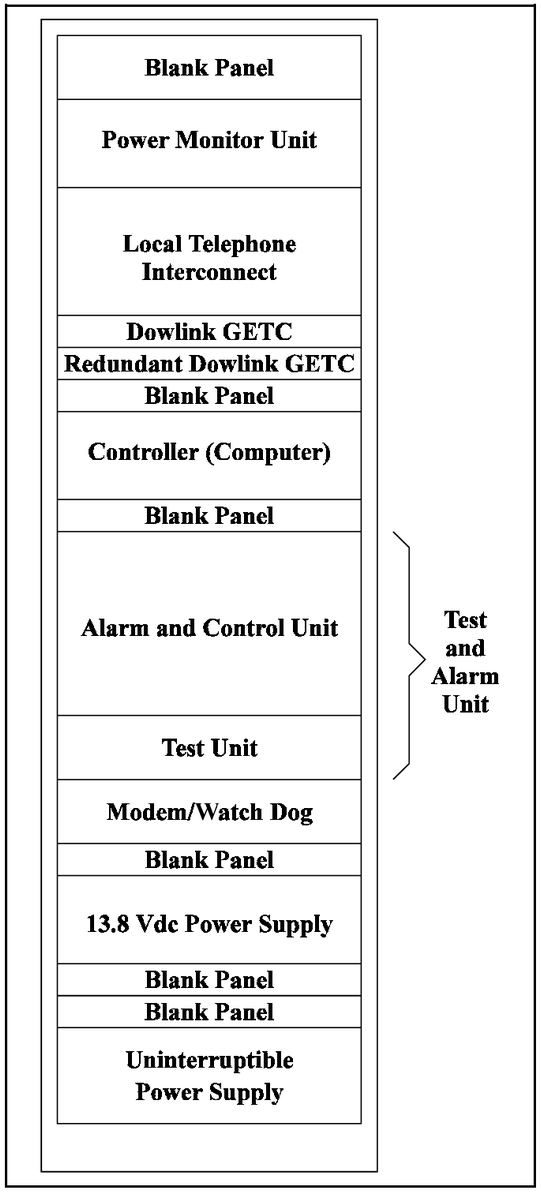


Figure 2 - Typical TAU Rack Installation

When a second swing-down assembly is lowered, access is gained to the Serial Interface Board and the Logic Board. Access is also gained to the Regulator Board which is mounted in a shielded enclosure on the inside of the rear housing of the TAU. The Alarm/Control Interface Board, Heat Sink Assembly, and the Rear Bulkhead Panel are all accessible from the rear of the TAU. The TU is a mobile radio (such as a RANGR EDACS) which is mounted on a shelf.

ALARM/CONTROL INTERFACE BOARD (A1)

Interfacing between the ACU Logic Board and the user-supplied alarms and sensors at the site, is performed by the Alarm/Control Interface Board. This board is mounted at the rear of the ACU card cage.

DISPLAY ASSEMBLY (A12)

The Display Assembly is located on the front of the TAU. A Display Panel, Panel Frame, Display Board, and associated hardware make up this assembly. The Display Board is the active part of the assembly used to present indications in response to commands from the Logic Board.

LOGIC BOARD (A4)

The Logic Board controls the operation of the ACU functions within the TAU. It contains an 8032 microprocessor which communicates with the Site Controller over an RS-232C link and controls ACU circuitry. Also contained on the board are the interface, addressing, and memory circuitry required to support the microprocessor.

SERIAL INTERFACE BOARD (A13)

Interfacing between the ACU Logic Board and the Site Controller, and between the TU and the Site Controller, is provided by the Serial Interface Board. This board provides level conversion between the Site Controller RS-232C levels and the open-collector or TTL levels used by the ACU and TU. Switching of the TU between the Site Controller and the Control Unit (such as an S-550 EDACS is also handled by this board.

MOBILE RADIO

A mobile radio (such as a RANGR EDACS), with special firmware, performs all the Test Unit functions. Interfacing between the mobile radio and the Site Controller or the Control Unit, is handled by the Serial Interface Board.

CONTROL UNIT

When the mobile radio is used in the user-call mode or normal voice operation, instead of as a test unit, the Control Unit and microphone are used. The Control Unit connects to the Serial Interface Board, which provides the required signals and power between the mobile radio and the Control Unit.

REGULATOR BOARD (A7) AND HEAT SINK ASSEMBLY (A8)

Regulated +10 and +5 Volts is provided by the Regulator Board. The Regulator Board obtains power from the EDACS station power supply (nominally 13.8 Vdc), and performs the required voltage regulation and filtering. Only the +5 volt supply is used in EDACS applications. Heat sink assembly A8 provides the required surface area for dissipating the heat produced by pass transistors Q1 and Q2.

REAR BULKHEAD PANEL

A Rear Bulkhead Panel is provided for connecting power to the TAU, and connecting serial links between the Site Controllers and the ACU and TU.

POWER-ON RESET BOARD (A10)

The Power-On Reset Board (A10) is a plug-in module that connects to the Alarm/Control Interface Board (A1) via J2-13 thru 18. This board prevents voltage transients from toggling the magnetic latching relays on A1 when power is applied to the TAU. The function is performed by holding MR (Master Reset) at ground potential for approximately 200 to 400 ms after power is applied, to allow the power source to stabilize.

CONTROL OF THE TAU

Operation of the TAU is normally controlled by the Site Controller over a 19.2 kilobaud serial data link. Each function of the TAU (ACU and TU) has its own serial link with the Site Controller, and is controlled and operated separately. In addition, each function has a separate serial link with the backup Site Controller. The TU is responsible for switching between the master and backup serial link for both the TU and the ACU. When the TAU is not in service, it may be controlled locally.

TEST UNIT OPERATION

This section describes Test Unit Operation. The TU performs the test call function and control-channel monitoring.

CONTROL CHANNEL MONITORING

Monitoring of the control channel at the EDACS site is a primary function of the TAU. When the TU is performing this function it is in the monitor state. The TU is normally in the monitor state whenever it is not performing another task. When in the monitor state, the Site Controller issues commands which tell the TU the channel number of the control channel. The Site Controller then directs the mobile radio to tune to the control channel and monitor the messages being transmitted. Control channel monitoring consists of the following:

- Obtaining sync on the control channel.
- Monitoring the outbound control channel for correctly received messages.
- Verifying the site ID.

When the TU detects a control channel fault, it sends a message to the Site Controller indicating the type of fault which has occurred. At the Site Controller, the faults are logged and the appropriate action is taken. When the Site Controller decides to bring up a new control channel, a command is issued to the TU giving the number of the new control channel. The TU then attempts to obtain sync on the new control channel, and if successful, begins monitoring the new channel.

TEST CALL

When the MOBTX command is issued from the Site Controller, the TU performs the Test Call. The Test Call tests the control channel and the working channel in a simulated mobile-originated, channel-request sequence. It also checks the high-speed and low-speed data transmitted over the working channel. The major steps in the sequence are:

- Site Controller directs the TU to request a channel assignment.
- The TU goes to the control channel, acquires sync, and requests an individual call.
- As directed by the Site Controller, the control channel transmits the assigned working channel.
- The TU receives the channel assignment, goes to the working channel, and monitors the high speed data for a channel confirmation.
- The TU sends the high-speed key message followed by the low-speed data.
- The working channel detects the messages from the TU, and transmits low speed data.
- The TU switches to receive and correctly detects the low-speed data.
- The working channel transmits the drop-channel message after two seconds of no transmit activity on channel.
- The TU receives the drop channel message, returns to the monitor state, and resumes control channel monitoring.
- The TU keeps track of the progress of the Test Call, and sends the results when it exits the test-call state.

ACU OPERATION

The ACU samples and debounces its alarm inputs and reports changes to the site controller. Additionally, the ACU will set or reset any combination of its eight relays upon command of the site controller. The ACU contains a serial interface board (also used by the TU) and a Control Unit (used exclusively by the TU). Alarm and relay status are presented on the front display panel.

ALARM REPORTING

Alarm reporting is one of the functions of the ACU. User-supplied alarm sensing devices may be connected to J4 and J5 on the Alarm/Control Interface Board.

Each of the 32 alarm inputs is continually sampled and debounced, and changes are reported immediately to the site controller through the status message. The status message is also sent anytime the ACU is polled by the site controller.

There are three alarm masks provided by the site controller. These masks define the reporting of the alarms as follows:

- Enable/disable - A 32-bit mask. A one in any position represents an alarm which the ACU should monitor. Only changes in state of enabled alarms will be reported to the site controller.
- Active high/low - A 32-bit mask. A one in any position represents an active-high alarm input, and a zero in any position represents an active-low alarm input.
- Major/Minor alarm - A 32-bit mask. A one in any position represents a major alarm input, and a zero in any position represents an minor alarm input.

All disabled alarms are set to inactive and held there until the alarm is enabled by the site controller. Any changes in state of a disabled alarm are not reported by the ACU. Also, any active high/low or major/minor designation are ignored for disabled alarms.

CONTROL OUTPUT RELAYS

Operating the control output relays is the other main function of the ACU. The control outputs provide relay contact which may be connected to user-supplied devices at the EDACS site. The relays are under remote control from the Site Controller and are set or reset when the SET RELAYS message is sent by the site controller. The relay states are returned to the Site Controller through the status message.

The output relays are magnetic latching so that power loss will not cause them to change state. Output relays are activated by commands from the Site Controller. The current state of both the alarm inputs and control outputs can be determined at any time by executing the appropriate command at the System Manger. The ACU also compares the current state of the relays to their desired state. If the state is incorrect, an error is displayed on the ACU display panel.

DIAGNOSTIC SELF TESTS

Both the ACU and the TU perform diagnostic self tests after a reset. If a problem is detected, the ACU or TU will send a message to the Site Controller, which will log the problem and take the appropriate action. Since the TAU is a multifunction device, a fault may only partially disable the TAU. Only the function affected will be disabled by the Site Controller.

DISPLAY ASSEMBLY

The ACU Display assembly (Figure 3) shows the status of 32 alarm inputs (ALARM INPUTS), eight relays (CONTROL OUT), system information (SYS STATUS), and ACU status (ALARM UNIT STATUS). When an enabled alarm is active, the corresponding alarm state indicator is lit. The CONTROL OUT indicators are turned on when the relay is set (closed). Information from the site controller is displayed by the SYS STATUS indicators as follows:

MAIN CNTRL ACTIVE	Indicates the main site controller is active.
BACKUP CNTRL ACTIVE	Indicates the backup site controller is active.
ANT PWR FAIL	Antenna power failure detected by the PMU.
CHN PWR FAIL	Channel power failure detected.
GETC FAIL	GETC logic failure detected.
CHANNEL SETTINGS	Indicates GETC switch settings are incorrect.
INTERCONNECT FAIL	Interconnect system failure detected.
BACKUP LINK FAIL	Indicates failure of backup serial or frame sync link.

System status information is given to the ACU in the system status byte each time the site controller is contacted. If the ACU has not received a message after a specified time interval, the ACU will turn off the MAIN CNTRL ACTIVE and the BACKUP CNTRL ACTIVE indicators.

The eight SYS STATUS indicators display the internal status of the ACU and are continuously updated. Status information is displayed as follows:

MAJOR ALARM	Indicates a major alarm is active.
MINOR ALARM	Indicates a minor alarm is active.
ACU ERROR	Logic error detected.
RELAY ERROR	Indicates current relay states do not match designated states.
READY	Indicates ACU has received initial alarm masks and relay settings from the site controller.
POLLED	Indicates the ACU has received a poll message from the site controller.
NOT READY	Lit after ACU power-up or reset. Remains on until the ACU receives initial alarm masks and relay settings from the site controller.

This ACU status information is also sent to the site controller in the status byte of the status message.

USER CALL OPERATING INSTRUCTIONS

The mobile radio and Control Unit in the TU may be used to make calls similar to a normal EDACS mobile. Before a user call can be initiated, the TU must be in the user-call state.

PLACING A USER CALL

To make a user call:

a. Place the Serial Interface board switch in the SERV position.

b. Wait for the S-550 EDACS Control Unit display to illuminate.

c. Proceed with normal mobile operation.

NOTE

If there is no PTT activity for several minutes, the TU will remove power from the Control Unit.

d. Return the microphone to the microphone bracket.

e. Return the slide switch on the Serial Interface Board to the NORM position.

SECTION II INSTALLATION INSTRUCTIONS

INSTALLATION OF UNIT INTO RACK

Installation of the TAU assembly into the equipment rack is as follows:

1. Mount the TAU in the cabinet. Figure 2 shows the standard location. (Use of standard locations for equipment assures that supplied cables will reach their desired connections.)

2. Connect a 19D903880P101 cable between Port 27 on the back of the Site Controller computer and J2 on the rear bulkhead panel of the Alarm and Control Unit.

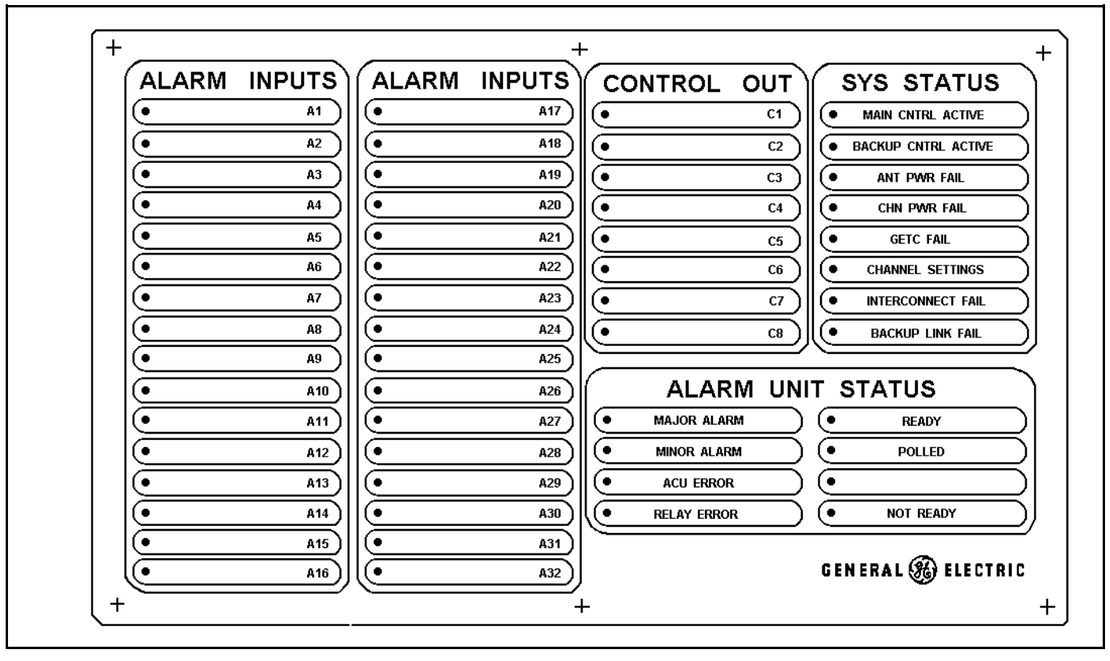


Figure 3 - ACU Display

3. Connect a 19D903880P101 cable between Port 28 on the back of the Site Controller computer and J1 on the rear bulkhead panel of the Alarm and Control Unit.

4. Connect a 19D903880P101 cable between Port 27 on the back of the backup Site Controller computer (if used) and J4 on the rear bulkhead panel of the Alarm and Control Unit.

5. Connect a 19D903880P101 cable between Port 28 on the back of the backup Site Controller computer (if used) and J3 on the rear bulkhead panel of the Alarm and Control Unit.

6. Connect P5 of existing 19A149357G2 power cable to J5 on the rear bulkhead panel of the Alarm and Control Unit.

7. Connect #8 red and #8 black wires of 19D901864G2 control/power cable to F801B on the 13.8 Vdc station power supply.

CONNECTION OF USER EQUIPMENT TO ALARM/ CONTROL INTERFACE

GENERAL PROVISIONS

The ACU provides eight control outputs and 32 alarm inputs for use with user-supplied control and alarm-sensing devices. The outputs are SPDT contacts of magnetic latching relays, controlled by commands from the Site Controller.

Alarm inputs are optically coupled for isolation, and are configured for use with a variety of sensing devices. Alarm status information presented to the inputs, is transmitted to the Site Controller for display at the System Manger. The ACU may be programmed to interpret the alarms as major or minor. The ACU may also be programmed to interpret either the on (logic 1) or the off (logic 0) state of an input as indicating an alarm condition. The status of the alarm inputs and control outputs is displayed on the front of the TAU.

Connections are made via 50-pin connectors on the rear bulkhead of the TAU. The connectors will accept standard 25-pair, telephone cable. Typically, a telephone cable will be brought out to a punch-block where connections to user-supplied devices are made. The connections for this arrangement are shown in Tables 1 and 2. The telephone cables and punch blocks are not provided with the TAU.

INPUT CONNECTIONS

NOTE

When the LED is active (conducting) the ACU will read the input as a logic 0.

A typical circuit of an alarm input is shown in Figure 4. All other inputs are identical. A jumper plug located on the TAU backplane is available for each input to alter the circuit configuration. When the jumper is between pins 1 and 2, as shown, the TAU provides 13.8 Vdc from its internal source to the anode of the LED in the optocoupler. A user-supplied contact closure between the cathode (C) and ground (G) input pins turns on the LED.

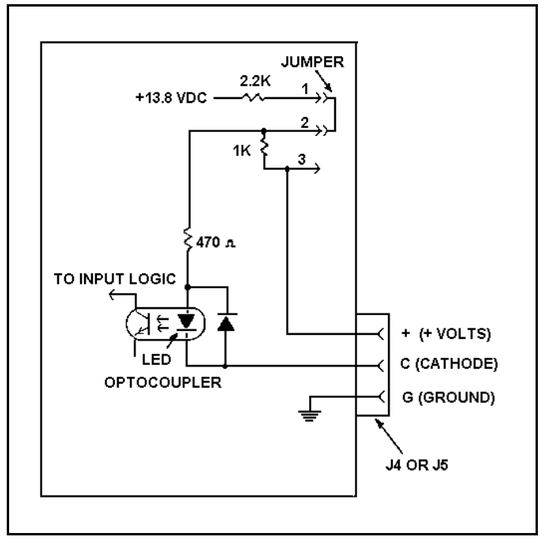


Figure 4 - Typical Alarm Input Circuit

The input may also be driven from an external voltage or current source applied between the + and C leads. When the LED is driven from an external source, the current applied to the LED must not exceed 32 mA. This condition will be met if:

a. The jumper is between pins 2 and 3, and the voltage between + and C is less than or equal to 16 Vdc.

OR

b. The jumper is removed, and the voltage between + and C is less than or equal to 48 Vdc.

Table 1 - Control Output Connections to J3

JACK PIN J3	WIRE COLOR BASE-TRACE	BLOCK PIN	OUTPUT NO.	FUNCTION
26	W-BL	11	1	NO
1	BL-W	21	1	C
27	W-O	31	1	NC
2	O-W	42	2	NO
28	W-G	52	2	C
3	G-W	62	2	NC
29	W-BR	73	3	NO
4	BR-W	83	3	C
30	W-SL	93	3	NC
5	SL-W	104	4	NO
31	R-BL	114	4	C
6	BL-R	124	4	NC
32	R-O	135	5	NO
7	O-R	145	5	C
33	R-G	155	5	NC
8	G-R	166	6	NO
34	R-BR	176	6	C
9	BR-R	186	6	NC
35	R-SL	197	7	NO
10	SL-R	207	7	C
36	BK-BL	217	7	NC
11	BL-BK	228	8	NO
37	BK-O	238	8	C
12	0-BK	24	8	NC
38	BK-G	25		+5V*
13	G-BK	26		+5V*
39	BK-BR	27		LOG GND
14	BR-BK	28		LOG GND
40	BK-SL	29		PWR GND
15	SL-BK	30		PWR GND
41	Y-BL	31		+13.8V**
16	BL-Y	32		+13.8V**
42	Y-O	33		
17	O-Y	34		
43	Y-G	35		
18	G-Y	36		
44	Y-BR	37		
19	BR-Y	38		
45	Y-SL	39		
20	SL-Y	40		
46	V-BL	41		
21	BL-V	42		
47	V-O	43		
22	O-V	44		
48	V-G	45		
23	G-V	46		
49	V-BR	47		
24	BR-V	48		
50	V-SL	49		
25	SL-V	50		

BL=BLUE O=ORANGE G=GREEN BR=BROWN SL=SLATE
W=WHITE R=RED BK=BLACK Y=YELLOW V=VIOLET

NOTES:

1. TABLE SHOWS CONNECTIONS FOR A 50 POSITION TYPE 66 PUNCH BLOCK CONNECTED VIA A STANDARD 25 PAIR CONNECTORIZED CABLE.
2. *REQUIRES JUMPER BETWEEN J38-1 AND J38-2 ON THE ALARM/ CONTROL INTERFACE BOARD.
3. **REQUIRES JUMPER BETWEEN J39-1 AND J39-2 ON THE ALARM/ CONTROL INTERFACE BOARD.

Table 2 - Control Input Connections to J4 and J5

JACK PIN J4/J5	WIRE COLOR BASE-TRACE	BLOCK PIN	ALARM NO. J4	ALARM NO. J5	FUNCTION
26	W-BL	1	1	17	+
1	BL-W	2	1	17	C
27	W-O	2	1	17	G
2	O-W	4	2	18	+
28	W-G	5	2	18	C
3	G-W	6	2	18	G
29	W-BR	7	3	19	+
4	BR-W	8	3	19	C
30	W-SL	9	3	19	G
5	SL-W	10	4	20	+
31	R-BL	11	4	20	C
6	BL-R	12	4	20	G
32	R-O	13	5	21	+
7	O-R	14	5	21	C
33	R-G	15	5	21	G
8	G-R	16	6	22	+
34	R-BR	17	6	22	C
9	BR-R	18	6	22	G
35	R-SL	19	7	23	+
10	SL-R	20	7	23	C
36	BK-BL	21	7	23	G
11	BL-BK	22	8	24	+
37	BK-O	23	8	24	C
12	O-BK	24	8	24	G
38	BK-G	25	9	25	+
13	G-BK	26	9	25	C
39	BK-BR	27	9	25	G
14	BR-BK	28	10	26	+
40	BK-SL	29	10	26	C
15	SL-BK	30	10	26	G
41	Y-BL	31	11	27	+
16	BL-Y	32	11	27	C
42	Y-O	33	11	27	G
17	O-Y	34	12	28	+
43	Y-G	35	12	28	C
18	G-Y	36	12	28	G
44	Y-BR	37	13	29	+
19	BR-Y	38	13	29	C
45	Y-SL	39	13	29	G
20	SL-Y	40	14	30	+
46	V-BL	41	14	30	C
21	BL-V	42	14	30	G
47	V-O	43	15	31	+
22	O-V	44	15	31	C
48	V-G	45	15	31	G
23	G-V	46	16	32	+
49	V-BR	47	16	32	C
24	BR-V	48	16	32	G
50	V-SL	49			G
25	SL-V	50			+13.8V*

BL=BLUE O=ORANGE G=GREEN BR=BROWN SL=SLATE
W=WHITE R=RED BK=BLACK Y=YELLOW V=VIOLET

NOTES:

1. TABLE SHOWS CONNECTIONS FOR A 50 POSITION TYPE 66 PUNCH BLOCK CONNECTED VIA STANDARD 25 PAIR CONNECTORIZED CABLE.
2. *FOR J4: REQUIRES JUMPER BETWEEN J40-1 AND J40-2 ON THE ALARM/CONTROL INTERFACE BOARD.

   *FOR J5 REQUIRES JUMPER BETWEEN J41-1 AND J41-2 ON THE ALARM/CONTROL INTERFACE BOARD.

The minimum LED current necessary to activate the optocoupler is typically about 7 mA (10 mA maximum). Thus the voltage ranges for these two cases are about 5 to 16 Vdc with the jumper in, and 15 to 48 Vdc with the jumper removed.

Current through the LED should drop to zero in the off state for reliable operation. It is recommended that the LED off condition be an open circuit.

Connections to the user-supplied devices must be configured to maintain the isolation of the TAU. This will insure adequate noise immunity and protection from voltage surges. When the internal 13.8 Vdc supply is used to drive the LED, the user-supplied contact closure must be isolated from the user equipment. A relay with contacts that do not connect to the user's equipment is normally adequate. When the user equipment provides the current to the LED, the optocoupler provides isolation, and connections should only be made to pins labeled + and C.

NOTE

Never make a direct connection between the ground or power circuits in user-supplied equipment and the TAU power terminals.

Typical connections between alarm inputs and user-supplied devices is shown in Figure 5.

OUTPUT CONNECTIONS

Connections to the control outputs must also maintain isolation between the TAU and user-supplied devices. The output relays provide isolation between their contacts and the TAU. Internal TAU power may be used to drive the load only when the load input circuit provides isolation (e.g., TAU power may be used with a control output to operate a relay). System power is available on the control output connector, however, the total current drawn from this source must not exceed one ampere. When the load power is derived from the load, the only connection to the TAU should be the relay contacts.

The ACU relay contacts are capable of switching resistive loads of up to one ampere. The user must provide protection for the contacts when reactive loads are to be switched. Inductive loads, such as a relay, should have a suppression diode across the coil. Typical connections of control outputs is shown in Figure 5.

NOTE

Never make a direct connection between the ground or power circuits in user-supplied equipment and the TAU power terminals.

PROGRAMMING

Control of the relay outputs and the interpretation of alarm inputs is determined by data stored in the data tables in the Site Controller. This data is down loaded to the ACU when the ACU is placed in service. The information field for each type of data is called a mask. The reported alarm condition is compared with these alarm tables to determine what action should be taken.

OUTPUT CONTROL

An eight-bit data field, called the output mask (OUTMSK) controls the relays. Each bit in the mask controls one output relay. The least significant bit (LSB) controls relay output number one, second LSB controls relay two, etc. When a bit in the mask is set to one, the corresponding relay is set (normally open contacts will close). When a bit in this mask is set to zero, the corresponding relay is reset (normally open contacts will open).

ALARM INTERPRETATION

The interpretation of the alarm inputs is controlled by three, 32-bit masks. In each mask, the least-significant bit corresponds to alarm input number one.

- Enable/disable - A 32-bit mask. A one in any position represents an alarm which the ACU should monitor. Only changes in state of enabled alarms will be reported to the site controller.
- Active high/low - A 32-bit mask. A one in any position represents an active-high alarm input, and a zero in any position represents an active-low alarm input.
- Major/Minor alarm - A 32-bit mask. A one in any position represents a major alarm input, and a zero in any position represents an minor alarm input.

SECTION III ALARM/CONTROL INTERFACE BOARD

INTRODUCTION

The Alarm/Control Interface board is used by the ACU function of the TAU. This board provides the interface between the ACU logic and the various user-supplied alarm and control devices.

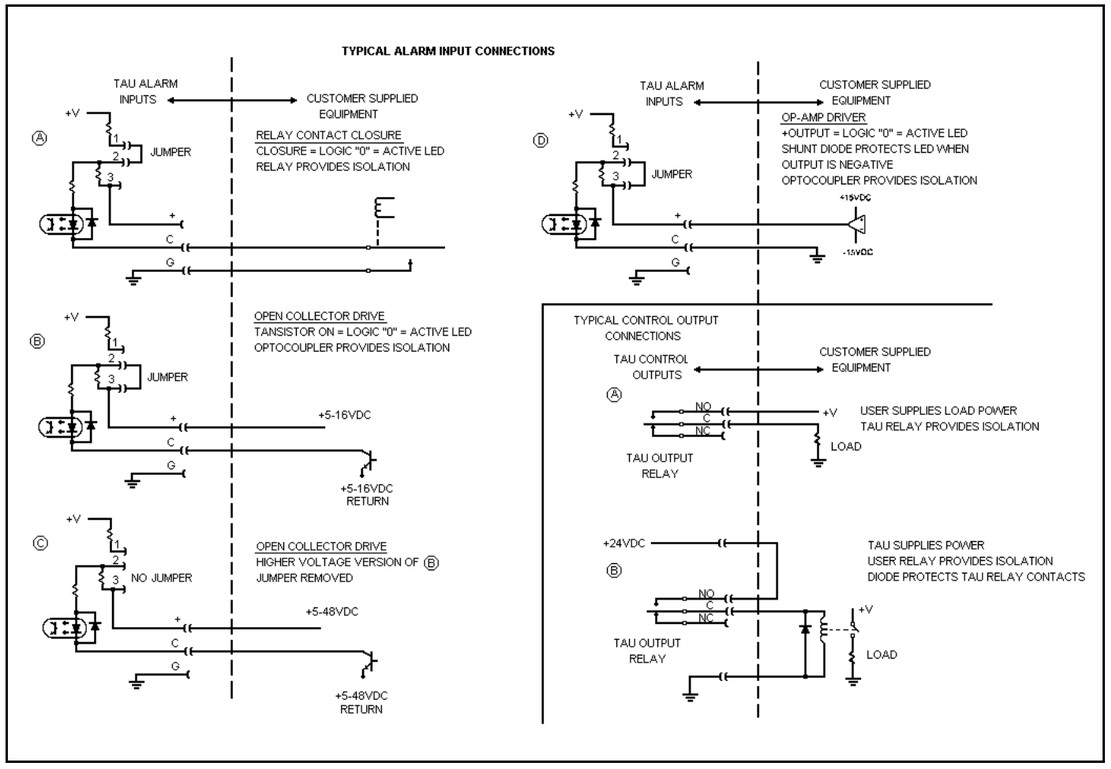


Figure 5 - Typical Alarm/Control Hookups

ALARM INPUT PROCESSING

There are 32 optically-isolated alarm input circuits, each identical. Each input circuit may be configured with a jumper to accept either a relay-contact closure, low-voltage (5-16 Vdc) drive, or a high-voltage (15-48 Vdc) drive.

Consider input circuit OC1 on the schematic diagram. The circuit consists of resistors R1, R17, and R33; diode D1, optocoupler Q1; and shunt P6. If P6 is connected between J6-1 and J6-2 as shown, a relay contact from external equipment can be connected between J4-1 and J4-27. Closure of this contact will activate the circuit consisting of R1, P6, R33, and Q1, causing Q1 to conduct.

If P6 is connected between J6-2 and J6-3, a dc voltage can be applied between J4-26 and J4-1 to activate Q1. Resistor R33 will limit the LED (Q1) current to permit operation in the 5-16 Vdc range. When P6 is removed entirely, R17 is added to the circuit. The additional resistance will allow the circuit to be drive from voltages in the 15-48 Vdc range. In all of the above cases, when the LED in Q1 lights, the associated transistor turns on. This produces a logic 0 at output pin 5 of the opto-coupler.

NOTE

Electrical isolation must be maintained between the TAU and user-supplied equipment.

The ACU microprocessor determines the status of the various alarm inputs by looking at bus DB0 thru DB7. The 32 alarm inputs are present at the input of octal, tri-state drivers (U8, U9, U5, and U6) on bus OC1 thru OC32 (optocoupler 1 through 32). When eight of the alarm inputs are to be sampled, the proper control work is written to decoder U10. The decoded output determines which of the bus drivers is enabled and which of the alarm states are placed on the data bus. The DB0 thru DB7 data lines are connected to the Logic Board through connector J1.

CONTROL OUTPUT PROCESSING

Eight DPDT latching relays (K1 thru K8) are used as alarm outputs to control user-supplied equipment. Each relay has a set and reset coil which determines the state of the relay contacts. One set of relay contacts is used to present alarm status to user-supplied equipment through connect J3, the other set of relay contacts reports the relay state back to the microprocessor. The state of the relays (K1 thru K8) is input to tri-state drive U6, and output to the data bus (DB0 thru DB7) when selected by U10. The check on relay status is desirable for several reasons:

a. It is proof that the relay does in fact change states when commanded to do so by the microprocessor.

b. Under certain circumstances, the system may "forget" the existing status of the relays, such as after a system reset or maintenance. A read of relay status after normal operation has resumed will quickly tell whether or not the relays are in the desired states. They can then be changed as necessary.

When a relay is to be set, the microprocessor places the proper command data on the data bus (DB0 thru DB7) and writes the proper control word (C1 thru C4) to decoder U10. This allows the SET flip-flop (U3) to latch the set relay pattern. The data is clocked out of U3 and turns on the corresponding transistors in U1 (an octal Darlington array), which energize the set coil of the proper relay.

After the relay has changed states (latched), the command word on the data bus is changed and the relay is no longer kept in its energized state. The process for placing the relay in the reset state is the same except that reset flip-flop U4 is selected by decoder U10.

Whenever the microprocessor is reset, master reset MR goes low, resetting flip-flops U3 and U4. This deenergizes the set/reset coils of all relays and is designed to protect the relays during system reset and start-up.

SECTION IV
TAU DISPLAY ASSEMBLY

INTRODUCTION

The Display Assembly, located on the front panel of the TAU, consists of the Display Panel, the Panel Frame, the Display Board, and associated hardware. The Display Panel provides an LED indication of alarm inputs, control outputs, and ACU and EDACS system status. The LEDs used are located on the Display Board, which is mounted directly behind the Display panel. There is a small window in the Display Panel in front of each LED so that the status of the LED may be seen from the front of the TAU.

OPERATION

The Display Board interprets commands from the microprocessor (on the ACU Logic Board) and turns on the appropriate indicator. There are 56 available LED indicators (H1 thru H56) for displaying status information. The LEDs are configured in groups of eight, each tied to the output of a D flip-flop (U1 thru U5, U11, and U12). The microprocessor control bus (C1 thru C4) is tied to the input of decoder U15.

When status information is to be displayed, the microprocessor places a command word on the data bus (DB0 thru DB7) indicating which of the indicators is to be turned on. A control work (C1 thru C4) is written by the microprocessor to decoder U15. The decoder enables the proper display flip-flop where the display information is latched.

Data to be displayed may come from user-supplied equipment connected to the Alarm/Control Interface Board or it may come via the serial data link, or be generated inside the ACU itself. During system reset, MR (master reset) goes low resetting all flip-flops and turning off all LEDs on the Display Board. After normal operation has resumed, the microprocessor will set the LEDs to their proper states.

SECTION V
SERIAL INTERFACE BOARD

INTRODUCTION

The Serial Interface Board is used by both the ACU and TU functions of the TAU. The main function of the Serial Interface Board is to provide serial links between the ACU logic board and the master (or backup) Site Controller, and between the TU and the master (or backup) Site Controller. This board also allows the TU to interface to the Control Unit, so it may be operated as a regular EDACS mobile. The Serial Interface Board receives 13.8 Vdc from the external power supply, and distributes the power to other boards and assemblies in the TAU.

POWER CONNECTIONS

Power (13.8 Vdc) is received from the external power supply via the Rear Bulkhead Panel. The Serial Interface Board then distributes the power to the Regulator Board, the Display Assembly, and the Alarm/Control Interface Board. Power is also supplied to the TU mobile and to the Control Unit. A 2 amp fuse in the mobile and Control Unit line provides protection against high currents, while allowing the ACU functions to still operate.

SERIAL LINK

The Serial Interface Board receives four independent serial communications links on connector J6. Two links are from the master Site Controller, while the other two links are from the backup Site Controller. Each link consists of a transmit, receive, and ground line.

The Serial Interface Board provides the necessary level translations required between the RS-232C levels used by the Site Controllers and the open-collector or TTL levels used by the ACU and TU. Chip U2 is the RS-232C line driver, while chip U3 is the RS-232C line receiver. Timer U1 is operated as a dc voltage inverter to provide -10 Vdc for chip U2.

ACU SERIAL LINK

The ACU TXD is the transmit serial data line from the microprocessor on the ACU Logic Board, while ACU RXD is the receive serial data line. The ACU TXD line enters the Serial Interface Board on J5-8, and the signal is routed to both U2A and U2B for level conversion. From U2A the signal goes to J6-5, which is the receive data line to the master Site Controller for the ACU. From U2B the signal goes to J6-11, which is the receive data line to the backup Site Controller for the ACU. Signals from the ACU are received by both the master and backup Site Controllers.

Serial data transmitted from the master Site Controller for the ACU enter via J6-4, and go to U3A for level conversion. Transmitted serial data from the backup Site Controller for the ACU enter via J6-10 and go to U3B. The outputs from U3A and U3B are connected together, and go to ACU RXD on pin J5-9. Either U3A or U3B is enabled at any given time by the TU AUX line from the mobile.

The TU AUX line enters the Serial Interface Board on J2-6, and then splits to go to inverting buffers U4A and U4C. The output of U4A passes through inverting buffer U4B to the enable pin of U3A. The output of U4C goes to the enable pin of U3B. When TU AUX is at a high logic level, U3A is enabled and ACU RXD receives serial data from the master Site Controller. When TU AUX is at a low logic level, U3B is enabled and ACU RXD receives serial data from the backup Site Controller.

TU SERIAL LINK

The TU TXD is the transmit serial data line from the microprocessor on the TU mobile, while TU RXD is the receive serial data line for the TU. Multiplexer U6 controls the serial data link connections for the TU. The TU may communicate with the master Site Controller, the backup Site Controller or the Control Head.

The TU TXD enters the Serial Interface Board via J2-9, passes through buffer U5A, and goes to Y OUT (IN) of U6. Outputs Y2 and Y3 (U6) are cconnected together and to U2C and U2D for level translation. The output of U2C goes to J6-8 for receive serial data from the TU to the master Site Controller, while the output of U2D goes to J6-14, for receive serial data for the backup Site Controller. Again, both the master and backup Site Controllers receive the serial data from the TU.

Serial data transmitted from the master Site Controller for the TU enter the Serial Interface Board via J6-7, pass through U3C for level conversion and go to X2 of U6. Transmitted serial data from the backup Site Controller enter via J6-13, pass through U3D for level conversion, and go to X3 of U6. The X OUT of U6 passes through buffer U5F to TU RXD (J2-8).

Again, TU AUX selects between the master and backup Site Controllers. After passing through U4A, the signal goes to the A SELECT pin of U6. The inputs and outputs enabled by TU AUX are given in Table 3. The state of TU AUX is controlled by the TU.

CONTROL UNIT INTERFACE

The Serial Interface Board also allows the TU to be operated as a regular EDACS mobile. Serial transmit data from the Control Unit, CTL HD TXD, enter the Serial Interface Board on J1-4, pass through buffer U5B, and go to both X1 and X0 of the multiplexer U6. Outputs Y1 and Y0 of U6 are coupled together, pass through buffer U5E, and go to J1-5, the receive serial data for the Control Unit (CTL HD RXD).

The TU SER RQST line from the TU enters via J2-4. The signal then passes through buffer U5C to the B SELECT pin of U6. When B SELECT is high, the Site Controller serial data lines are connected to the TU. When B SELECT is low, the control unit serial data lines are connected to the TU (Table 4). However, when B SELECT is low, TU AUX is still able to select between the master or backup Site Controller for the ACU.

The TU SER RQST also enables power to be provided to the Control Unit. After the signal passes through buffer U5C, it also passes through inverting buffer U4D to the base of transistor Q1. When TU SER RQST is low, the output of inverting buffer U4D is high, and Q1 is turned on. This allows current to flow through the coil of relay K1, and the normally open contacts will close, providing 13.8 Vdc at J1-2 (SW A+/CTL HD PWR). When TU SER RQST is high, the output of U4D is low and Q1 is turned off. The relay then returns to its normally open state. Diode D4 discharges any capacitance from relay K1.

When the DPDT slide switch on the Serial Interface Board is placed in the CTL HD position, 13.8 Vdc is connected to IGN A+ on J2-7, which connects to the TU. This allows the TU to operate as a EDACS mobile. The TU will then cause TU SER RQST to go low.

The speaker on the Serial Interface Board receives its signals from the mobile via J2-10 and 11.

SECTION VI LOGIC BOARD

DESCRIPTION

The Logic Board directs and coordinates the operation of the ACU function of the TAU. During normal operation, the microprocessor (U1) accepts commands from the Site Controller, issues instructions to other ACU circuitry, and sends an acknowledgment signal back to the site controller. If a particular command requires certain data, the microprocessor collects the required data, makes necessary decisions based on the results, and sends a response back to the Site Controller.

The Logic Board consists of an 8032 microprocessor, support circuitry for the 8032, and circuitry required to interface the 8032 with the following boards and/or assemblies for the TAU:

- Serial Interface Board
- Alarm/Control Interface Board
- Display Assembly

Logic Board operation is most conveniently described by using the segments above as a guideline. Refer to Figure 6 and the schematic diagrams.

CIRCUIT ANALYSIS

8032 MICROPROCESSOR

The 8032 microprocessor contains:

a. 256 bytes of internal RAM.

Table 3 - TU Aux States

TU AUX STATE	INPUT ENABLED	OUTPUT ENABLED
High	X2-MASTER TXD	Y2-MASTER & BACKUP RXD
Low	X3-BACKUP TXD	Y-3 MASTER & BACKUP RXD

Table 4-A And B Select Line States

B SELECT STATE	A SELECT STATE	INPUT ENABLED	OUTPUT ENABLED
Low	Low	X0-CTL HD TXD	Y0-CTL HD RXD
Low	High	X1-CTL HD TXD	Y1-CTL HD RXD
High	Low	X2-MASTER TXD	Y2-MASTER & BACKUP RXD
High	High	X3-BACKUP TXD	Y3-MASTER & BACKUP RXD

b. 32 I/O lines, each of which can be dynamically configured to serve as an output or input. Some can additionally generate secondary functions such as RD, WR, etc.

c. Three counter/timers which can be made to operate in numerous modes.

d. A six-source, two-priority-level interrupt system with nesting capability.

e. A serial I/O port for multiprocessor communications, I/O expansion, or UART operation.

f. On-chip oscillator and clock circuits.

A description of the microprocessor signal lines used in this application is given in Table 5.

MICROPROCESSOR SUPPORT CIRCUITRY

The support circuitry consists of the following:

- Address latch
- Program and Data Memory

Table 5 - Microprocessor Signal Lines

SIGNAL NAME	DESCRIPTION
P00-P07	An eight-bit port used for low-order addressing and data bus.
ALE	Address-Latch Enable output used to latch the low-order address byte from P07-P00 into an external latch.
P20-P27	High-order address byte.
PSEN	The Program Store Enable output is made active during access to program memory. Allows separation of data and program memory. The 8032 can address up to 64K of program memory and up to 64K of data memory. This dual-address structure simplifies address decoding.
RD	Read strobe used to place data from data memory (including memory-mapped I/O) onto the microprocessor data bus (P07-P00).
WR	Write strobe used to latch data from the microprocessor into data memory (including memory-mapped I/O).
RESET	Resets the microprocessor.
TO	Configured as an output line, TO generates a periodic pulse to keep the watchdog timer alive.
RXD	Serial data input line which accepts 19.2 kilobaud, asynchronous data from the Serial Interface Board.
TXD	A 19.2 kilobaud, asynchronous serial output line from the microprocessor to the Serial Interface Board.
P11	Configured as an input line connected to S2-SW2 (not used).
P12	An input line connected to S2-SW3 (not used).
XTL 1 & 2	Connections for the 11.52 MHz crystal.
EA	In this application EA is permanently tied low.

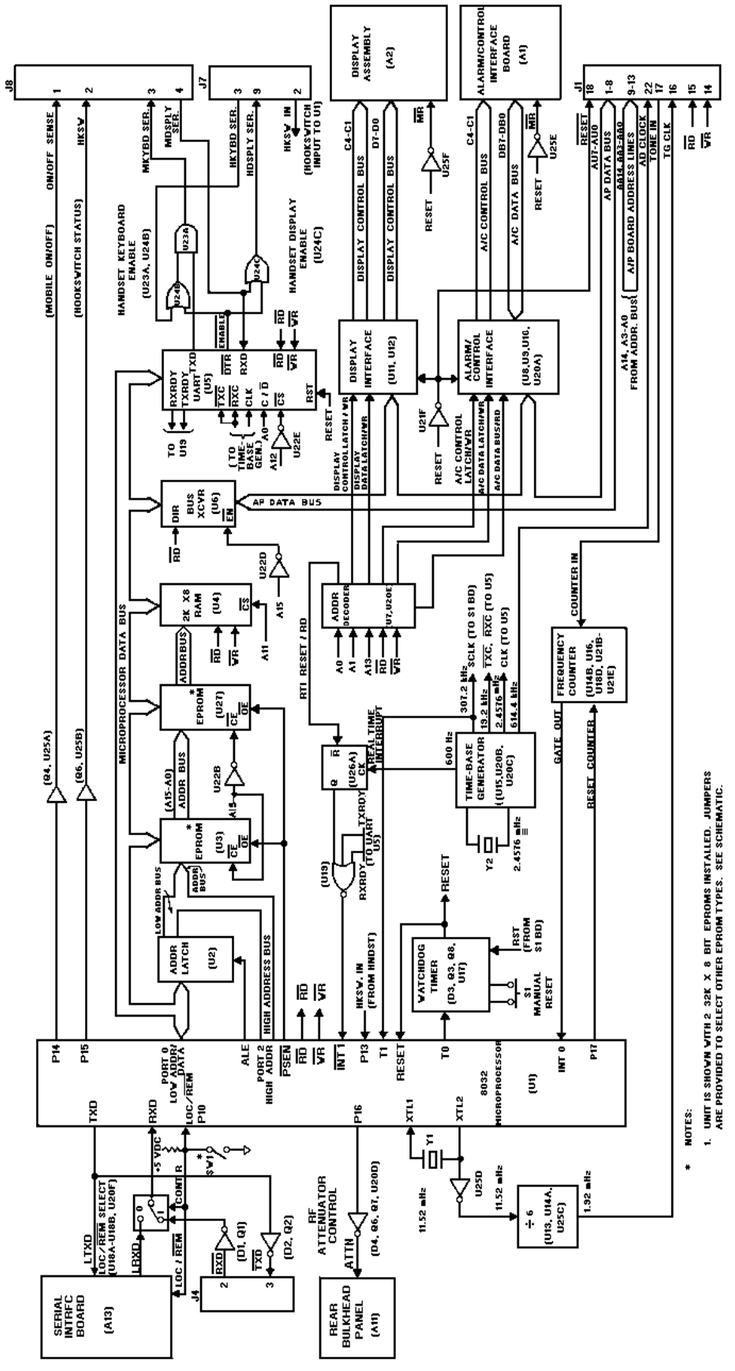


Figure 6 - Logic Board Functional Diagram

- Bus Transceiver
- Address Decoder
- Watchdog Timer

Address Latch

Port 0 (P07-P00) of the 8032 is time multiplexed, permitting it to generate the low-order address byte and to serve as the data bus. Octal latch U2, clocked by the ALE signal, latches the low-order address byte onto the microprocessor bus.

Program And Data Memory

The 8032 microprocessor uses a dual-addressing structure. By using separate read strobes for program memory and for data memory (PSEN is used for program memory and RD for data memory), a dual address map from 0000-FFFF Hex is created.

For example, if the 8032 executes a program instruction read at 0100 Hex the following occurs:

a. The low-order address byte appears on P07-P00 and is latched onto the address bus by U2.

b. The high-order address byte appears on P27-P20, which is part of the address bus.

c. PSEN goes low enabling the output of the addressed EPROM to the data bus.

d. The microprocessor reads the data.

When the 8032 reads RAM at 0100 Hex a similar process occurs, except that PSEN remains inactive and RD goes low. This enables the RAM at that address, while the corresponding EPROM remains disabled.

The Logic board data memory consists of U4, a 2K x 8 bit RAM (at 0000-07FF Hex), and various memory-mapped I/O devices.

Bus Transceiver

Octal bus transceiver U6 is enabled by address bit A15. The direction of the bus transceiver is controlled by RD. When A15 is high (at address

8000 Hex and above) the Microprocessor Data Bus is connected to the AP Data Bus. The AP Data Bus is used to communicate with the:

- Display Board interface circuitry
- Alarm/Control Interface Board interface circuitry

Address Decoder

When the microprocessor reads from or writes to external data memory or memory-mapped I/O, the proper address is placed on the address bus. A RD or WR strobe is then issued to enable the data transfer between the microprocessor and the addressed device. The Address Decoder accepts the appropriate address bits and insures that the device addressed is activated when the RD or WR strobe is asserted. The circuits controlled by the Address Decoder and their addresses are listed in Table 6.

Table 6 - Addresses And Controlled Circuits

HEXADECIMAL ADDRESS	READ/WRITE STATUS	FUNCTION
A800	Write	Load A/C Interface Board data latch U9.
A801	Write	Load A/C Interface Board control latch U8.
A802	Write	Load Display Board control latch U11.
A803	Write	Load Display Board data latch U12.
A800	Read	Enable A/C Data bus to microprocessor via U10.

The Address Decoder consists of U7 (dual 1-of-4 decoder) and U20E. A decoder is active, when the logical AND of its two enable inputs (EA1 and EA2 for side A; EB1 and EB2 for side B) produces a logic one. For example, when the microprocessor loads U9 with a data byte, a write to address A800 Hex (binary 1010 1000 0000 0000) is issued. Since A15 equal one, the bus transceiver is enabled and data can be transferred from the microprocessor to U9. Since A13 equals one, EA1 and EB1 are both active, but since EA2 and EB2 are inactive, the decoders are disabled. Note that U7-13 (A0) and U7-3 (A1) are both low. Because A1 and A0 are both low, the QA0 output of U7 will follow WR low. Pin U9-11 is the clock input to an octal latch (rising edge trigger), which is connected to QA0. When WR again goes high, QA0 and U9-11 follow, latching the data into the latch as desired. In the previous example, A11 was set to one keeping RAM U4 disabled, preventing a bus-contention problem.

Watchdog Timer

A watchdog timer and reset circuit is formed around D3, Q8, and U17. The circuit allows external and manual microprocessor-reset capability. An astable multivibrator is formed from a 555 timer (U17). If allowed to run freely, a square wave having a period of about 1.5 seconds on output pin U17-3 is generated. This pin is connected to RESET pin 9 of the microprocessor. During the 1.5 second period, the voltage on U17-2 and U17-6 is varying between 3.33 volts and 1.67 volts. If the voltage at pins 2 and 6 is held above 3.33 volts, U17-3 will remain low and the microprocessor will not reset. If pins 2 and 6 are pulled below 1.67 volts, U17-3 goes high and the microprocessor will reset.

During normal operation, the microprocessor pulses its TO pin periodically. The pulse passes through C22 and turns on transistor Q3 charging capacitor C21. The pulsing keeps the voltage at pins 2 and 6 above 3.33 volts, keeping the microprocessor out of reset. If the microprocessor malfunctions, the pulsing of TO will stop and U17 will start. When U17-3 goes high, the microprocessor is reset. Since U17 is free running, after a short time U17-3 will go low again, removing the reset from the microprocessor. If the microprocessor is reinitialized, TO will again pulse, keeping the microprocessor reset.

The watchdog circuit also has the following capabilities:

a. Manual Reset - When S1 is closed, the voltage at U17-2 and U17-6 is pulled below 1.67 volts, resetting the microprocessor.

b. Watchdog-Timer Disable - Placing a jumper between J9-1 and J9-2 will cause the voltage at pins 2 and 6 to stay above 3.33 volts, disabling the watchdog timer. The circuit will still respond to external and manual resets. This disabling feature is intended as an aid in servicing and should never be used during normal operation.

INTERFACE CIRCUITRY

Serial Interface Board

When LOCAL-REMOTE switch 52-SW1 is closed, the Logic Board is placed in the remote mode. Serial information can then pass between the Site Controller and the Logic Board, via the Serial Interface Board.

Serial data (LRXD) from the Serial Interface Board, enters the Logic Board via J3-8 and passes through NAND gates U18A and U18B to RXD pin 10 of the microprocessor. Serial data from the microprocessor passes from TXD pin 11 to the Serial Interface Board via J3-7.

User RS-232C Terminal (Future Option)

As a future option in the local mode (S2-SW1 open), a user-supplied RS-232 terminal can be connected via J4 to check out the ACU. Serial data from the terminal enters the Logic Board via J4-2. Data then passes through inverting level-shifter Q1 and NAND gates U18C and U18B, to the RXD pin of the microprocessor. Data to be sent to the terminal originates at the microprocessor TXD pin. Data then passes through inverting level shifter Q2 and connector J4-3 to the terminal.

The Control Interface Board

The Alarm/Control Interface Board interface circuitry consists of control latch U8, tri-state data latch U9, and bus driver U10, each of which can be selected via the Address Decoder. Transfer of data to and from the Alarm/Control Board is accomplished by writing the appropriate control information into control latch U8. The data written into the latch has the following significance:

BITS	FUNCTION
0-2	Select the particular device on the Alarm Control Board to be accessed.
3	Enables the Alarm Control Board decoder.
7	Places the data in U9 onto the Alarm Control data bus.

To read data from the Alarm/Control Interface Board, the following procedure can be used:

a. Execute a write to A801 Hex to activate bus transceiver U6 and load control latch U8. Set the data to be loaded as follows; bits 0-2 as required, bit 3 to 1, and bit 7 to 0. At the conclusion of the write, alarm/status information from the Alarm/Control Interface Board will be present on the Alarm/Control data bus DB7-DB0.

b. Execute a read to A800 Hex to activate U6 and bus driver U10. The alarm/status information on the Alarm/Control data bus then passes through U10 to the AP data bus, and through U6 to the Microprocessor Data Bus.

A typical write to the Alarm/Control Interface Board can be performed as follows:

a. Execute a write to A800 Hex to activate bus driver U6 and load tri-state data latch U9. The data latched into U9 will be the actual data sent to Alarm/Control Interface Board.

b. Execute a write to A801 Hex to activate U6 and load control latch U8. Set data bits 0-2 as required, bit 3 to 1, and bit 7 to 1 (to place the contents of U9 onto the Alarm/Control data bus).

c. Execute a second write to A801 Hex in exactly the same fashion as in step b, except bit 3 = 0 in this case. This latches the data into the selected device on the Alarm/Control Board, completing the data transfer.

Display-Assembly

The Display-Assembly interface circuitry consists of control latch U11 and data latch U12, each of which is selected by the Address Decoder. Since data is only written to (and never read from) the Display Assembly, operation is simpler than the Alarm/Control Board interface, though the two cases are quite similar.

A typical data write to the Display Assembly can be done as follows:

a. Execute a write to A803 Hex to load data latch U12 with the data to be transferred to the board.

b. Execute a write A802 Hex to load control latch U11 with the correct control data (bits 0-2 set as required, but 3 set to 1, bits 4-7 set to any state).

c. Execute a write to A802 Hex as in step b, except bit 3 = 0. This latches the data into the selected device, completing the data transfer.

SECTION VII
REGULATOR BOARD

INTRODUCTION

The Regulator Board (A7) consists of three separate regulators: a 16 Vdc pass regulator (U3), a 10 Vdc switching regulator (U1), and a 5 Vdc pass regulator. In EDACS applications, only the 5 Vdc output is required to power the logic circuits; the 16Vdc and 10Vdc outputs are not used. The EDACS station power supply provides 13.8Vdc (nominal) for the source voltage to the Regulator Board.

16 VDC PASS REGULATOR

An adjustable three-terminal voltage regulator (U3) provides 16 Vdc at 100 mA from a 24 Vdc source. When the 13.8 Vdc source is used, the output is about 11.8 Vdc. The input to the IC is connected to the +13.8 Vdc line through current-limiting resistor R16 and pin 3 of J1. Diode D1 is a 39-volt transient protector connected between the circuit side of R16 and ground. This diode shunts any high-voltage spikes that may appear on the +13.8 Vdc line.

Diode D4 discharges any capacitance on the output of U3 if input accidentally shorts to ground. This prevents damage to the IC due to back-bias overvoltage. Capacitors C16, C17, C20, and C23 act as filter and bypass capacitors. Resistors R21 and R22 adjust the output voltage of the IC according to the following formula:

$$V_{out} = 1.25(1 + R1/R2)$$

10 VDC SWITCHING REGULATOR

Regulator U1 is a regulating pulse-width modulator (PWM) IC. This PWM, along with power Darlington transistors Q1 and Q2 are used to provide regulated +10 Vdc at three amps. This power is available at J2-1 thru 4 and J3-3 (for the 5-volt regulator).

The emitters of transistors Q1 and Q2 are supplied +13.8 Vdc through filtering and bypassing components C11, L1, C10, C3, C1, and C25. Transient suppression is provided by D1 and R16, and overload shutdown by SCR D6.

The on and off times of Q1 and Q2 are controlled by PWM U1 through base resistors R9 and R10. Base pull-up resistors R11 and R12 ensure that the transistors are cut off when drive is removed. Both transistors (Q1 and Q2) are driven 180 degrees out of phase.

Pulse-width modulator U1 varies the conduction cycle of Q1 and Q2 to maintain a constant output voltage, independent of load and input voltage variations. When either transistor is on, power is drawn from the +13.8 Vdc line and supplied to the load through L2 at +10 Vdc. During conduction, the voltage at J4-5 is approximately 13.8 Vdc, D3 is reverse biased, and C12 is charging. When the transistor turns off, inductor L2 supplies back emf causing the voltage at J4-5 to go negative. Diode D3 will start conducting and the load current will flow through D3 and L2. The voltage at J4-5 is smoothed by the filtering and bypassing components L2, C12, L3, C13, C18, and C21 to give a clean +10 Vdc output.

The conduction cycle is controlled by U1. The pulse width depends on the voltage level at the input to the PWM error amp (U1-1). Output voltage is sampled at voltage divider R7 and R3. Pulse-width modulator U1 will change the pulse width (changing the conduction time of Q1 and Q2) to keep the voltage on pin 1 equal to the reference voltage on pin 2. The voltage on pin 2 is set to 2.5 Vdc by voltage divider R1 and R2. A +5 Vdc on-chip voltage regulator at pin 16 feeds the voltage divider. The frequency of the pulse width modulator is set by C5 and R4. Components R6, R8, and C24 are used to phase-compensate and stabilize the feedback control system.

5 VDC PASS REGULATOR

An adjustable three-terminal voltage regulator IC, mounted on an external heat sink assembly (A8), is used to provide 5 Vdc AT 1.3A from the +10 Vdc supply. The input of the regulator is connected to +10 Vdc through J3-3. Capacitors C14, C15, C19, and C22 are used to filter and bypass. Resistors R29 and R18 set the regulator output voltage according to the formula: Vout (1 + R18/R19).

SECTION VIII
TEST AND CHECKOUT

SCOPE

This section describes how to checkout and test the TAU. Test procedures are divided up into ACU and TU portions of the TAU. These test procedures are provided as an aid in troubleshooting and as a checkout to verify proper operation after a repair is made.

ACU

The ACU functions of the TAU are controlled by the Logic Board. Primary functions are to report the state of the 32 alarm inputs to the Site Controller and to set or reset the eight control relay outputs upon command from the Site Controller. The secondary functions of the ACU are to display the status of the alarm inputs and control outputs on the front display panel of the TAU, as well as display the ACU status and site equipment status.

TESTING

The ACU functions of the TAU are tested by the following actions.

- The power-up sequence of the ACU is verified and status response is sent to master Site Controller serial link.
- An external digital controller (see equipment list) sends an ACU DIAGNOSTIC command message to the ACU over master Site Controller serial link.
- The ACU will perform a series of tests on the front panel LEDs. These LEDs are observed for correct indications.
- The ACU will set and reset the relays, and their control outputs are monitored.
- The ACU will monitor the alarm inputs, and contact closures are applied to the alarm inputs. The ACU will turn on an alarm LED when its corresponding alarm input optocoupler is conducting.

MESSAGE INTERPRETATION

When interpreting ACU response messages, all bytes of the message must match the expected response. If any byte does not match, it is interpreted as a test failure.

FRONT PANEL LEDS

Follow the FRONT PANEL INDICATOR TEST explained in Table 7.

DIGITAL CONTROLLER & COMMUNICATIONS PROTOCOL

In order to test the TAU, a device must be used that can send and receive hexadecimal command strings at RS-232C levels. A digital controller (such as a protocol analyzer) or a computer with software that allows generation and interpretation of the command strings may be used. The term "digital controller" is used throughout this manual to refer to any device capable of sending and receiving the required hexadecimal codes.

The Hex command string (shown as hex command in the procedure) must be entered. Communications protocol is as follows:

Interface type RS-232C

Data rate 19.2K baud

Data format 1 start bit, 8 data bits, 1 stop bit

MESSAGE FORMAT

FRAME START BYTE(AA)	MESSAGE START BYTE	DATA BYTES	PARITY BYTE

The parity byte is determined by taking the inverse of the exclusive-OR of the message start byte with all the data bytes.

TEST PROCEDURES

EQUIPMENT REQUIRED

QUANTITY	EQUIPMENT TYPE
1	HP 6286A (or equivalent) DC Supply with current limit
1	Triplett VOM Model 630-PL type 5 (or equivalent)
1	HP 4953A or 4951 C Protocol Analyzer, computer with software to allow generation and reception of hexadecimal command strings equivalent digital controller
2	50-Pin, type 66 punch block or equivalent

TEST SETUP

Before testing the ACU, the following setups must be made:

1. Set S2-1 on the Logic Board to the closed (on) position.
2. Jumper pins 1 and 2 for J6 thru J37 on the Alarm/Control Board.
3. Connect the 16 contact closures for alarms 1 thru 16 to J4 on the Alarm/Control Interface Board.
4. Connect the 16 contact closures for alarms 17 thru 32 to J5 on the Alarm/Control Interface Board.
5. Open all connections to the alarm inputs.
6. Monitor continuity for the relay control outputs at J3 on the Alarm/Control Interface Board.
7. Connect the digital controller to J1 on the Rear Bulkhead panel as follows:

   TXD pin on digital controller to J1-3

   RXD pin on digital controller to J1-2

   GND pin on digital controller to J1-7.
8. Connect the power supply minus (-) lead to J5-1 on the Rear Bulkhead panel.
9. Connect the power supply positive (+) lead to J5-2 on the Rear Bulkhead panel.
10. Turn on power supply and adjust to +13.8 Vdc.
11. Turn off power supply and proceed with test procedure in Table 7.

Table 7 - ACU Test/Checkout Procedure

STEP	PROCEDURE	TEST/MEASUREMENT POINT	OBSERVATION
	NOTE Diagnostics my be exited at any time by giving the RESET (AA 81 01 7F) command.		
	CURRENT CHECK		
1.	Turn on power supply	J5-2	Current less than 2 amps
	VOLTAGE CHECK		
2.	Monitor voltage at Rear Bulkhead connector using voltmeter.	J2-4 J2-5 J2-6 J2-7 J2-8 J2-9 J2-12	+3.0 to +5.5 Vdc +13.8 Vdc ±20% +3.0 to +5.5 Vdc -0.5 to +0.8 Vdc +3.0 to +5.5 Vdc +3.0 to +5.5 Vdc -0.5 to +0.8 Vdc
	REGULATOR BOARD CHECK		
3.	Monitor voltage at rear bulkhead connector using voltmeter.	J2-4 J2-6	+3.0 to +5.5 Vdc +3.0 to +5.5 Vdc
4.	Set power supply to +11.0 Vdc and monitor voltage using voltmeter.	J2-4 J2-6	+3.0 to +5.5 Vdc +3.0 to +5.5 Vdc
5.	Set power supply to +16.0 Vdc and monitor voltage using voltmeter.	J2-4 J2-6	+3.0 to +5.5 Vdc +3.0 to +5.5 Vdc
6.	Return power supply to +13.8 Vdc		
7.	Turn off the power supply.		
	ACU RESET AND INITIALIZATION		
8.	Turn on the power supply.		Verify status response message <AA 81 00 00 00 00 XX 08 YY> to digital controller. Where XX is the state of the relays on power-up (any value), and YY is the parity byte.

STEP	PROCEDURE	TEST/MEASUREMENT POINT	OBSERVATION
9.	Issue the RESET command <AA 81 01 7F> through the digital controller.		Verify that all front panel indicators are lit. After 2 or 3 seconds, all indicators should turn off and the NOT READY indicator will light. Verify the ACU gives the status response message <AA 81 00 00 00 00 XX 08 YY>. Where XX is the state of the relays on power-up (any value), and YY is the parity byte.
FRONT PANEL INDICATOR TEST			
10.	Issue the DIAGNOSTICS command <AA 8679> through the digital controller.		a. Verify each indicator is turned on/off (in approximately 2-second intervals) in the following order: A1 thru A16 A17 thru A32 C1 thru C8 MAIN CNTRL ACTIVE thru BACKUP LINK FAIL MAJOR ALARM thru RELAY ERROR READY thru NOT READY b. Verify that the following groups of eight indicators are turned on/off. A1 thru A8 A9 thru A16 A17 thru A24 A25 thru A32 C1 thru C8 MAIN CNTRL ACTIVE thru BACKUP LINKFAIL MAJOR ALARM thru NOT READY

STEP	PROCEDURE	TEST/MEASUREMENT POINT	OBSERVATION
	CAUTION Any equipment connected to the relay outputs will be affected by the relay test.		
	NOTE Each relay will be activated for approximately 2 seconds. The RELAY ERROR indicator will light if the ACU detects a relay in the wrong state.		
RELAY TEST (ALARM OUTPUT)			
11.	Connect a punch block to J3 as explained in Table 8 or make connections directly to J3. Measure relay resistance between NO and C. Open resistance should be >15 ohms, and closed resistance should be <15 ohms.		a. Verify that relay 2 is closed and the rest are open. Verify that CONTROL OUT C2 is lit. b. Verify that relay 1 is closed and the rest are open. Verify that CONTROL OUT C1 is lit. c. Verify that relay 3 is closed and the rest are open. Verify that CONTROL OUT C3 is lit. d. Verify that relay 4 is closed and the rest are open. Verify that CONTROL OUT C4 is lit. e. Verify that relay 5 is closed and the rest are open. Verify that CONTROL OUT C5 is lit. f. Verify that relay 6 is closed and the rest are open. Verify that CONTROL OUT C6 is lit. g. Verify that relay 7 is closed and the rest are open. Verify that CONTROL OUT C7 is lit. h. Verify that relay 8 is closed and the rest are open. Verify that CONTROL OUT C8 is lit. i. Verify that all relays are open. Verify that all CONTROL OUT C1 thru C8 are off.

STEP	PROCEDURE	TEST/MEASUREMENT POINT	OBSERVATION
	ALARM INPUTS TEST		
	NOTE A punch block as described in Table 9 maybe used to make connections to the alarm inputs.		
12.	Jumper J4-1 and J4-27 are alarm 1.		Verify that only indicator A1 is lit.
13.	Remove jumper for alarm 1 and jumper J4-28 and J4-3 for alarm 2.		Verify that only alarm indicator A2 is lit.
14.	Remove jumper for alarm 2 and jumper J4-4 and J4-30 for alarm 3.		Verify that only alarm indicator A3 is lit.
15.	Remove jumper for alarm 3 and jumper J4-31 and J4-6 for alarm 4.		Verify that only alarm indicator A4 is lit.
16.	Remove jumper for alarm 4 and jumper J4-7 and J4-33 for alarm 5.		Verify that only alarm indicator A5 is lit.
17.	Remove jumper for alarm 5 and jumper J4-34 and J4-9 for alarm 6.		Verify that only alarm indicator A6 is lit.
18.	Remove jumper for alarm 6 and jumper J4-10 and J4-36 for alarm 7.		Verify that only alarm indicator A7 is lit.
19.	Remove jumper for alarm 7 and jumper J4-37 and J4-12 for alarm 8.		Verify that only alarm indicator A8 is lit.
20.	Remove jumper for alarm 8 and jumper J4-13 and J4-39 for alarm 9.		Verify that only alarm indicator A9 is lit.
21.	Remove jumper for alarm 9 and jumper J4-40 and J4-15 for alarm 10.		Verify that only alarm indicator A10 is lit.
22.	Remove jumper for alarm 10 and jumper J4-16 and J4-42 for alarm 11.		Verify that only alarm indicator A11 is lit.
23.	Remove jumper for alarm 11 and jumper J4-43 and J4-18 for alarm 12.		Verify that only alarm indicator A12 is lit.
24.	Remove jumper for alarm 12 and jumper J4-19 and J4-45 for alarm 13.		Verify that only alarm indicator A13 is lit.
25.	Remove jumper for alarm 13 and jumper J4-46 and J4-21 for alarm 14.		Verify that only alarm indicator A14 is lit.
26.	Remove jumper for alarm 14 and jumper J4-22 and J4-48 for alarm 15.		Verify that only alarm indicator A15 is lit.
27.	Remove jumper for alarm 15 and jumper J4-49 and J4-24 for alarm 16.		Verify that only alarm indicator A16 is lit.
28.	Remove jumper for alarm 16 and jumper J5-1 and J5-27 for alarm 17.		Verify that only alarm indicator A17 is lit.
29.	Remove jumper for alarm 17 and jumper J5-28 and J5-3 for alarm 18.		Verify that only alarm indicator A18 is lit.
30.	Remove jumper for alarm 18 and jumper J5-4 and J5-30 for alarm 19.		Verify that only alarm indicator A19 is lit.
31.	Remove jumper for alarm 19 and jumper J5-31 and J5-6 for alarm 20.		Verify that only alarm indicator A20 is lit.
32.	Remove jumper for alarm 20 and jumper J5-7 and J5-33 for alarm 21.		Verify that only alarm indicator A21 is lit.
33.	Remove jumper for alarm 21 and jumper J5-34 and J5-9 for alarm 22.		Verify that only alarm indicator A22 is lit.
34.	Remove jumper for alarm 22 and jumper J5-10 and J5-36 for alarm 23.		Verify that only alarm indicator A23 is lit.
35.	Remove jumper for alarm 23 and jumper J5-37 and J5-12 for alarm 24.		Verify that only alarm indicator A24 is lit.
36.	Remove jumper for alarm 24 and jumper J5-13 and J5-39 for alarm 25.		Verify that only alarm indicator A25 is lit.
37.	Remove jumper for alarm 25 and jumper J5-40 and J5-15 for alarm 26.		Verify that only alarm indicator A26 is lit.
38.	Remove jumper for alarm 26 and jumper J5-16 and J5-42 for alarm 27.		Verify that only alarm indicator A27 is lit.
39.	Remove jumper for alarm 27 and jumper J5-43 and J5-18 for alarm 28.		Verify that only alarm indicator A28 is lit.
40.	Remove jumper for alarm 28 and jumper J5-19 and J5-45 for alarm 29.		Verify that only alarm indicator A29 is lit.
41.	Remove jumper for alarm 29 and jumper J5-46 and J5-21 for alarm 30.		Verify that only alarm indicator A30 is lit.
42.	Remove jumper for alarm 30 and jumper J5-22 and J5-48 for alarm 31.		Verify that only alarm indicator A31 is lit.
43.	Remove jumper for alarm 31 and jumper J5-49 and J5-24 for alarm 32.		Verify that only alarm indicator A32 is lit.
44.	Remove jumper for alarm 32.		Verify that all indicators are off.

STEP	PROCEDURE	TEST/MEASUREMENT POINT	OBSERVATION
45.	When testing is complete, issue RESET command <AA 81 01 7F> through the digital controller.		
	BACKUP SERIAL LINK CHECK		
46.	Disconnect the digital controller cable from rear bulkhead connector J1 (master serial link) and move to J3 (backup serial line).		
47.	Apply 0 V to J1-6 on the Mobile Interface Connector Board on the Rear Bulkhead Panel.		
48.	Issue the RESET command <AA 8101 7F>		Verify the ACU gives the status response <AA 81 00 00 00 00 XX 08 YY> through the digital controller. Where XX is the state of the relays on power-up (any value), and YY is the parity byte.

Table 8 - Control Output Connections To J3

JACK PIN J4/J5	WIRE COLOR BASE-TRACE	BLOCK PIN	OUTPUT NO.	FUNCTION
26	W-BL	1	1	NO
1	BL-W	2	1	C
27	W-O	3	1	NC
2	O-W	4	2	NO
28	W-G	5	2	C
3	G-W	6	2	NC
29	W-BR	7	3	NO
4	BR-W	8	3	C
30	W-SL	9	3	NC
5	SL-W	10	4	NO
31	R-BL	11	4	C
6	BL-R	12	4	NC
32	R-O	13	5	NO
7	O-R	14	5	C
33	R-G	15	5	NC
8	G-R	166	6	NO
34	R-BR	176	6	C
9	BR-R	186	6	NC
35	R-SL	197	7	NO
10	SL-R	207	7	C
36	BK-BL	217	7	NC
11	BL-BK	228	8	NO
37	BK-O	238	8	C
12	O-BK	24	8	NC
38	BK-G	25		+5V*
13	G-BK	26		+5V*
39	BK-BR	27		LOGGND
14	BR-BK	28		LOG GND
40	BK-SL	29		PWRGND
15	SL-BK	30		PWRGND
41	Y-BL	31		+13.8 V**
16	BL-Y	32		+13.8 V**
42	Y-O	33		
17	O-Y	34		
43	Y-G	35		
18	G-Y	36		
44	Y-BR	37		
19	BR-Y	38		
45	Y-SL	39		
20	SL-Y	40		
46	V-BL	41		
21	BL-V	42		
47	V-O	43		
22	O-V	44		
48	V-G	45		
23	G-V	46		
49	V-BR	47		
24	BR-V	48		
50	V-SL	49		
25	SL-V	50		

BL=BLUE O=ORANGE G=GREEN BR=BROWN SL=SLATE
W=WHITE R=RED BK=BLACK Y=YELLOW V=VIOLET

NOTES:

1. TABLE SHOWS CONNECTIONS FOR A 50 POSITION TYPE 66 PUNCHBLOCK CONNECTED VIA A STANDARD 25 PAIR CONNECTORIZED CABLE.
2. * REQUIRES JUMPER BETWEEN J38-1 AND J38-2 ON THE ALARM/CONTROL INTERFACE BOARD.
3. **REQUIRES JUMPER BETWEEN J39-1 AND J39-2 ON THE ALARM/CONTROL INTERFACE BOARD.

Table 9 - Alarm Input Connections to J4 and J5

JACK PIN J4/J5	WIRE COLOR BASE-TRACE	BLOCK PIN	ALARM NO. J4	J5	FUNCTION
26	W-BL	1	1	17	+
1	BL-W	2	1	17	C
27	W-O	3	1	17	G
2	O-W	4	2	18	+
28	W-G	5	2	18	C
3	G-W	6	2	18	G
29	W-BR	7	3	19	+
4	BR-W	8	3	19	C
30	W-SL	9	3	19	G
5	SL-W	10	4	20	+
31	R-BL	11	4	20	C
6	BL-R	12	4	20	G
32	R-O	13	5	21	+
7	O-R	14	5	21	C
33	R-G	15	5	21	G
8	G-R	16	6	22	+
34	R-BR	17	6	22	C
9	BR-R	18	6	22	G
35	R-SL	19	7	23	+
10	SL-R	20	7	23	C
36	BK-BL	21	7	23	G
11	BL-BK	22	8	24	+
37	BK-O	23	8	24	C
12	O-BK	24	8	24	G
38	BK-G	25	9	25	+
13	G-BK	26	9	25	C
39	BK-BR	27	9	25	G
14	BR-BK	28	10	26	+
40	BK-SL	29	10	26	C
15	SL-BK	30	10	26	G
41	Y-BL	31	11	27	+
16	BL-Y	32	11	27	C
42	Y-O	33	11	27	G
17	O-Y	34	12	28	+
43	Y-G	35	12	28	C
18	G-Y	36	12	28	G
44	Y-BR	37	13	29	+
19	BR-Y	38	13	29	C
45	Y-SL	39	13	29	G
20	SL-Y	40	14	30	+
46	V-BL	41	14	30	C
21	BL-V	42	14	30	G
47	V-O	43	15	31	+
22	O-V	44	15	31	C
48	V-G	45	15	31	G
23	G-V	46	16	32	+
49	V-BR	47	16	32	C
24	BR-V	48	16	32	G
50	V-SL	49			G
25	SL-V	50			+13.8V*

BL=BLUE O=ORANGE G=GREEN BR=BROWN SL=SLATE
W=WHITE R=RED BK=BLACK Y=YELLOW V=VIOLET

NOTES:

1. TABLE SHOWS CONNECTIONS FOR A 50 POSITION TYPE 66 PUNCH BLOCK CONNECTED VIA STANDARD 25 PAIR CONNECTORIZED CABLE.

2. *FOR J4: REQUIRES JUMPER BETWEEN J40-1 AND J40-2 ON THE ALARM/CONTROL INTERFACE BOARD.

   *FOR J5 REQUIRES JUMPER BETWEEN J41-1 AND J41-2 ON THE ALARM/CONTROL INTERFACE BOARD.

TU

The TU is tested in two stages. First the mobile radio (which is part of the TU) is tested as a standard mobile radio. Once proper operation of the radio has been determined, the TU interface circuits are tested.

Test the mobile radio by removing the personality EPROM and replacing it with a standard mobile radio personality EPROM. Then test the radio using its standard test procedure. Refer to the applicable mobile radio Maintenance Manual for details on replacing the EPROM and test procedure.

GENERAL REQUIREMENTS

The TU functions of the TAU are controlled by the System Board in the mobile radio. The primary function of the TU is to monitor the signalling on the control channel and report failures to the Site Controller. A secondary function of the TU is to permit the mobile radio, when operated in the user-call state, to be operated as a standard mobile radio.

The TU functions of the TAU are tested by the following actions:

- The digital controller sends command messages to the TU over the master Site Controller to the TU serial communications link.
- The TU sends response messages to the digital controller over the same link. These response messages must be monitored and interpreted.
- The TU is placed in its user-call state, and a mobile call is placed and received.

MESSAGE INTERPRETATION

When interpreting TU response messages, all bytes of the message must match the expected response. If any byte does not match, it is interpreted as a test failure.

DIGITAL CONTROLLER & COMMUNICATIONS PROTOCOL

In order to test the TAU, a device must be used that can send and receive hexadecimal command strings at RS-232C levels. A digital controller (such as a protocol analyzer) or a computer with software that allows generation and interpretation of the command strings maybe used. The term "digital controller" is used throughout this manual to refer to any device capable of sending and receiving the required hexadecimal codes.

The Hex command string (shown AS hex command in the procedure) must be entered. Communications protocol is as follows:

Interface type	RS-232C
Data rate	19.2K baud
Data format	1 start bit, 8 data bits, 1 stop bit

MESSAGE FORMAT

FRAME START BYTE(AA)	MESSAGE START BYTE	DATA BYTES	PARITY BYTE

The parity byte is determined by taking the inverse of the exclusive-OR of the message start byte with all the data bytes.

EQUIPMENT REQUIRED

QUANTITY	EQUIPMENT TYPE
1	MASTR® II Station Power Supply (19D430272G2), or equivalent
1	Triplett VOM Model 630-PL type 5 (or equivalent)
1	HP 4953A or 4951C Protocol Analyzer, computer with software to allow generation and reception of hexadecimal command strings equivalent digital controller

TEST SETUP

Before TU tests are performed, the mobile radio must have the proper software installed, and the radio must be completely functional. Refer to the mobile radio Maintenance Manual for complete test procedures and maintenance information.

1. Attach connector P1 of the mobile power and control cable to J1 (if RANGR EDACS) of the mobile radio. Connect P2 to J1 of the mobile interface connector board, located on the rear bulkhead panel.

2. Connect an antenna to the mobile radio.

3. Connect the TXA+ lead of the mobile power and connector cable to the positive (+) terminal of the power supply. Connect the TX A- lead of the cable to the minus (-) terminal of the power supply.

4. Place switch S1 on the Serial Interface Board in the NORM (open) position.

5. Connect the digital controller to J2 on the rear bulkhead panel as follows:

   TXD pin of digital controller to J2-3
   RXD pin of digital controller to J2-2
   GND pin of digital controller to J2-7

6. Connect the minus lead of the power supply to J5-1 on the rear bulkhead panel. plus lead of the power supply to J5-2 on the rear bulkhead panel.

7. Perform the TU test procedure in Table 10.

Table 10 - TU Test/Checkout Procedure

STEP	PROCEDURE	TEST/MEASUREMENT POINT	OBSERVATION
CURRENT CHECK			
1.	Turn on power supply.		
2.	Monitor voltage using VOM.	J2-7	Verify 0 Vdc
POWER-UP AND INITIALIZATION			
3.	Issue the RESET command <AA FD 02> through the digital controller.		Verify TU gives status response of <AA 91 8000 EE>.
4.	Issue the STATUS REQUEST command <AA 07 F8> through the digital controller.		Verify TU gives status response of <AA 91 81 00 EF>.
5.	Issue the status request command <AA 07 F8> through the digital controller.		Verify TU gives status response of <AA 91 82 00 EC>.
USER-CALL STATE			
	NOTE This test requires the use of the EDACS system and one other trunked radio. The TU and trunked radio must be configured for the system used for the test.		
6.	Turn on the trunked radio, and select the proper System and Group.		
7.	Place S1 on Serial Interface Board in the SERV (closed) position.		a. Verify TU gives status response of AA 91 90 00 F4. b. Verify the Control Unit is on and the SYSTEM and GROUP displays are lit.
8.	Select the proper System and Group on the S-550 EDACS Control Unit		
USER-CALL STATE (CONTINUED)			
9.	Press the PTT button on the TU radio, and wait for the beep and busy indicator to light.		Audio should be heard from the trunked radio.
10.	Release the PTT button.		
11.	Press the PTT button on the trunked radio, and wait for the beep and busy indicator to light.		Audio should be heard from the TU radio (Serial Interface Board speaker).
12.	Release the PTT button.		
13.	Place S1 on Serial Interface Board in the NORM (open) position.		a. Verify that the Control Unit displays are off. b. Verify the TU gives a status response of <AA 91 82 00 EC>.
CONTROL CHANNEL MONITORING			
14.	Issue the MONITOR command <AA 08 XX 01 00 00 00 00 00 YY> through the digital controller. Where XX is the control channel for the test system, and YY is the parity byte.		
15.	Press RESET button on control-channel GETC.		Verify the TU gives the fail response: AA 94 XX is 20, 40, or 80 ZZ is control channel number YY is parity
SC STEERING			
16.	Issue the SC STEERING command <AA 0201 FC> with the backup Site Controller selected.		
17.	Move the digital controller from J2 (Master serial link) to J4 (Backup serial link) on the rear bulkhead panel.		
18.	Issue the status request command <AA 07 F8> through the digital controller.		Verify the TU gives the status response <AA 91 C2 AC>.
19.	Issue the RESET COMMAND <AA FD 02> through the digital controller or turn power off to exit test.		

PARTS LIST

SERIAL INTERFACE BOARD
19D901848G1

ISSUE 1

SYMBOL	GE PART NO.	DESCRIPTION
		------ SPEAKERS ------
B1	19B801457G1	Speaker.
		------ CAPACITORS ------
C1	19A701534P8	Tantalum: 22 uF ±20%, 16 VDCW.
C2	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
C3	T644ACP210K	Polyester: .0010 uF ±10%, 50 VDCW.
C4 thru C6	19A701534P8	Tantalum: 22 uF ±20%, 16 VDCW.
C7	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
C8	19A701534P8	Tantalum: 22 uF ±20%, 16 VDCW.
C9 thru C11	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
		------ DIODES ------
D1 thru D3	19A700028P1	Silicon, fast recovery: fwd current 75 mA, 75 PIV; sim to Type 1N4148.
D4	T324ADP1041	Rectifier, silicon; general purpose.
		------ FUSES ------
F1	19A701881P28	Cartridge, quick blow: 2 amps; sim to Bussmann AGC2.
		------ JACKS ------
J1	19A116659P107	Connector, printed wiring: 8 contacts rated at 5 amps; sim to Molex 09-60-1081.
J2	19A116659P111	Connector, printed wiring: 12 contacts rated at 5 amps; sim to Molex 09-60-1121.
J3	19A116659P100	Connector, printed wiring: 2 contacts rated @ 5 amps; sim to Molex 09-60-1021.
J5	19A116659P108	Connector, printed wiring: 9 contacts rated at 5 amps; sim to Molex 09-60-1091.
J6	19A116659P114	Connector, printed wiring: 15 contacts rated @ 5 amps; sim to Molex 09-60-1151.
		------ RELAYS ------
K1	19C300957P2	Enclosed: 185 ohms ±10% coil res, 12 v 1.5 w, 4 form C contacts; sim to Allied Control T154X-316.
		---- TRANSISTORS ----
Q1	19A702503P2	Silicon, NPN.
		----RESISTORS ----
R1	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R2	H212CRP322C	Deposited carbon: 22K ohms ±5%, 1/4 w.
R3 thru R10	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R11	H212CRP227C	Deposited carbon: 2.7k ohms ±5%, 1/4 w.
		---- SWITCHES ----
S1	19A702244P1	Slide switch: DPDT, contact rating 1 mA @ 10 VDC; sim to Alps SSS02200.
		---- INTEGRATED CIRCUITS----
U1	19A701865P1	Linear, 555 TIMER.
U2	19A116704P1	Linear/Digital: QUAD DTL LINE DRIVER.
U3	19A116704P2	Linear/Digital: QUAD DTL LINE RECEIV.
U4	19A116180P75	Digital: HEX BUFFER INVERTER (OPEN COLLECTOR).
U5	19A700037P417	Digital: LOW POWER SCHOTTKY HEX BUFFER.
U6	19A700029P37	MOS, Digital: Differential 4-Channel Multiplexer.
		------ SOCKETS ----
XK1	5491595P7	Relay: 10 contacts; sim to Allied Control 30054-4.
		-------- MISCELLANEOUS ----
	19A116688P1	Fuse clip: sim to Littelfuse, Inc. 102071.
	5491595P9	Retainer: spring; sim to Allied Control 30040-2. (Used with K1).

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES.

PST TEST/ALARM UNIT
19D901365G2

ISSUE 2

SYMBOL	GE PART NO.	DESCRIPTION
A1	19D901331G3	ALARM/CONTROL INTERFACE BOARD
A4	19D901330G3	LOGIC BOARD.
A7	19D901039G1	REGULATOR BOARD.
A8	19B801132G1	HEAT SINK ASSEMBLY.
A10	19C851501G1	POWER-ON RESET BOARD.
A11	19C851141G3	BULKHEAD PANEL.
A12	19C851341G2	TEST ALARM UNIT DISPLAY.
A13	19D901848G1	SERIAL INTERFACE BOARD.
		-------- CABLES --------
W9	19D901915G1	Harness.
		-------- MISCELLANEOUS --------
	19D901042P1	Support. (Used with release latch).
	19B801028P1	Hinge.
	19A703359P1	Support. (Used with A11).
	19B801092G1	Cover, regulator.
	19B801061P1	Release latch. (Used with A11).
	19B801061P3	Release latch knob. (Secures main board).
	19B801061P4	Release latch knob. (Used with A11).
	4035664P8	Nut, self locking.
	19B201074P305	Tap screw, Phillips POZIDRIV: No. 6-32 x 5/16. (Used with A7).
	5490407P11	Grommet. (Used with A7).
	19A116773P206	Screw, thd. forming: No. M4.2-1.4 x 10. (Secures Display).
	19A148780P1	Nameplate.
	19A116496P1	Cable clip.
	19C851087G2	Housing.
	19C851097G3	Door.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES.

POWER ON RESET BOARD
19C851501G1

ISSUE 3

SYMBOL	GE PART NO.	DESCRIPTION
		-------- CAPACITORS --------
C1	19A703314P10	Electrolytic: 10 uF -10+50% tol, 50 VDCW; sim to Panasonic LS Series.
		-------- DIODES --------
D1	19A700025P12	Silicon, zener: 400 mW max; sim to BZX55-C15.
D2	19A702015P1	Silicon; sim to IN458A.
		-------- PLUGS --------
P1	19A116659P6	Connector, printed wiring: 6 contacts rated @ 5 amps: sim to Molex 09-52-3061.
		-------- TRANSISTORS --------
Q1	19A700022P1	Silicon, PNP; sim to Type 2N3906.
Q2 and Q3	19A700023P2	Silicon, NPN: sim to 2N3904.
		-------- RESISTORS --------
R1	H212CRP422C	Deposited carbon: 0.22M ohms + or -5%, 1/4 w.
R2	H212CRP310C	Deposited carbon: 10K ohms + or - 5%, 1/4 w.
R3	H212CRP347C	Deposited carbon: 47K ohms + or -5%, 1/4 w.
R4	H212CRP327C	Deposited carbon: 27K ohms + or -5%, 1/4 w.
R5	H212CRP147C	Deposited carbon: 470 ohms + or -5%, 1/4 w.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES.

PARTS LIST

LOGIC BOARD
19D901330G3

ISSUE 1

SYMBOL	GE PART NO.	DESCRIPTION
		- - - - - - - - - - CAPACITORS - - - - - - - - - -
C1 thru C15	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
C16	19A701534P9	Tantalum: 47 uF ±20%, 6.3 VDCW.
C17 thru C20	19A701624P119	Ceramic, disc: 30 pF ±5%, 500 VDCW, temp coef N80 PPM ±30.
C21	19A701534P7	Tantalum: 10 uF ±20%, 16 VDCW.
C22	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
C23	19A701534P9	Tantalum: 47 uF ±20%, 6.3 VDCW.
C24	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
		- - - - - - - - - - - - DIODES - - - - - - - - - -
D1 thru D4	19A700028P1	Silicon, fast recovery: fwd current 75 mA, 75 PIV; sim to Type 1N4148.
		- - - - - - - - - - - - JACKS - - - - - - - - - -
J4	19B209727P17	Power receptacle: 25 contacts, sim to amp 205738-2.
		- - - - - - - - - - TRANSISTORS - - - - - - - - - -
Q1	19A700023P2	Silicon, NPN: sim to 2N3904.
Q2 and Q3	19A700022P2	Silicon, PNP: sim to 2N3906.
Q4 and Q5	19A700023P2	Silicon, NPN: sim to 2N3904.
Q6	19A115300P2	Silicon, NPN; sim to Type 2N3053.
Q7	19A700022P2	Silicon, PNP: sim to 2N3906.
Q8	19A700023P2	Silicon, NPN: sim to 2N3904.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1 and R2	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R3 and R4	H212CRP322C	Deposited carbon: 22K ohms ±5%, 1/4 w.
R5	H212CRP247C	Deposited carbon: 4.7K ohms ±5%, 1/4 w.
R6	H212CRP127C	Deposited carbon: 270 ohms ±5%, 1/4 w.
R7	H212CRP222C	Deposited carbon: 2.2K ohms ±5%, 1/4 w.
R8 and R9	19A701537P1	Composition: 10M ±5%, 250 VDCW, 1/4 w.
R10	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R11	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R12	H212CRP339C	Deposited carbon: 39K ohms ±5%, 1/4 w.
R13	H212CRP322C	Deposited carbon: 22K ohms ±5%, 1/4 w.
R14	H212CRP410C	Deposited carbon: 0.1M ohms ±5%, 1/4 w.
R15	H212CRP222C	Deposited carbon: 2.2K ohms ±5%, 1/4 w.
R16	19A701630P1	5 Network: 10K ohms ±2% each @ 50 VDC; sim to Bourns 4306R0101-103.
R17 and R18	H212CRP247C	Deposited carbon: 4.7K ohms ±5%, 1/4 w.
R19	H212CRP222C	Deposited carbon: 2.2K ohms ±5%, 1/4 w.
R20	H212CRP010C	Deposited carbon: 10 ohms ±5%, 1/4 w.
R21	H212CRP147C	Deposited carbon: 470 ohms ±5%, 1/4 w.
R22	H212CRP233C	Deposited carbon: 3.3K ohms ±5%, 1/4 w.
R23	H212CRP127C	Deposited carbon: 270 ohms ±5%, 1/4 w.
R25	H212CRP233C	Deposited carbon: 3.3K ohms ±5%, 1/4 w.
R26 thru R30	H212CRP222C	Deposited carbon: 2.2K ohms ±5%, 1/4 w.
		- - - - - - - - - - SWITCHES - - - - - - - - - -
S1	19A701324P1	Push: contacts rated 1 mA at 10 volts; sim to IEE/Schadown 210091.
S2	19B800010P3	Push, 4 stations, contacts rated 25 mA at 24 VDC; sim to CTS 206-4.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - - -
U1	19A703714P1	Microcomputer: HMOS, 8-BIT.
U1	19A700037P415	Digital: (OCTAL TRANSPARENT LATCH TRI-STATE).
U3	19A704436G5	Integrated Circuit.
U3	19A705307G1	PROM Kit.
U4	19A702934P1	READ/WRITE MEMORY, sim to Hitachi HM6116LPI-4.
U5	19A704209P1	Interface, TR: sim to Intel ID8251A.
U6	19A700037P409	Digital: (OCTAL BUS TRANSCEIVER).
U7	19A700037P363	Digital: (DUAL 2-LINE-TO-1-LINE DECODER/DEMULTIPLEXER).
U8	19A700037P411	Digital: DF-F WITH CLEAR.
U9	19A700037P416	Digital: (OCTAL DF-F TRI-STATE).
U10	19A700037P408	Digital: (OCTAL TRI-STATE DRIVER).
U11 and U12	19A700037P411	Digital: DF-F WITH CLEAR.
U13	19A700037P370	Digital: (FULLY SYNCHRONOUS 4-BIT COUNTER).
U14	19A700037P335	Digital: DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESENT & CLEAR.
U15 and U16	19A700029P28	Digital: 12 STAGE BINARY RIPPLE COUNTER.
U17	19A701865P1	Linear, 555 TIMER.
U18	19A700037P301	Digital: QUAD 2-INPUT POSITIVE-NAND GATE; 74LS00.
U19	19A700037P319	Digital: TTL, LOW POWER SCHOTTKY, NOR GATE.
U20	19A703995P1	Digital: HEX UNBUFFERED INVERTER.
U21	19A700037P313	Digital: HEX SCHMITT-TRIGGER INVERTER.
U22	19A700037P305	Digital: HEX INVERTERS.
U23	19A700037P307	Digital: QUAD 2-INPUT POSITIVE-AND GATE.
U24	19A700037P322	Digital: QUAD 2-INPUT POSITIVE-OR GATE.
U25	19A700037P313	Digital: HEX SCHMITT-TRIGGER INVERTER.
U26	19A700037P335	Digital: DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOP WITH PRESENT & CLEAR.
U27	19A704385G3	Programmable Memory.
		- - - - - - - - - - CABLES - - - - - - - - - -
W1 thru W9	19A700184P1	Jumper.
		- - - - - - - - - - SOCKETS - - - - - - - - - -
XU1	19A700156P5	Socket, integrated circuit: 40 contacts; sim to Augat 340-AG39D.
XU3	19A700156P3	Integrated circuit: 28 contacts; sim to AMP 640362P3.
XU5	19A700156P3	Integrated circuit: 28 contacts; sim to AMP 640362P3.
XU27	19A700156P3	Integrated circuit: 28 contacts; sim to AMP 640362P3.
		- - - - - - - - - - CRYSTALS - - - - - - - - - -
Y1	19A702511G5	Quartz, 11.520000 MHz.
Y2	19A702511G7	Quartz: 2.457600 MHz.
		- - - - - - - - - - MISCELLANEOUS - - - - - - - - - -
	19A703248P2	Contact, electrical. (Used with TP1-TP13, J1, J3, & J9)
	19A701785P2	Contact, electrical; sim to Molex 08-50-0404. (Used with J2, J5-J8).
	19A703597P1	Spacer. (Supports board). (Quantity 5).
	19B209727P10	Screwlock; female, sim to Amp 205-817-1. (Used with J4).
	19B209727P13	Connector, plug. (Used with J4).
	19A701332P4	Insulator, washer: nylon. (Used with Q6).

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES.

PARTS LIST

REGULATOR BOARD
(A7 MOBILE - A7 STATION)
19D901039G1
ISSUE 4

SYMBOL	GE PART NO.	DESCRIPTION
		- - - - - - - - - - CAPACITORS - - - - - - - - - -
C1	19A700233P7	Ceramic: 1000 pF ±20%, 50 VDCW.
C3	19A702250P113	Polyester: .1 uF ±10%, 50 VDCW.
C4	19A701534P5	Tantalum: 2.2 uF ±20%, 35 VDCW.
C5 and C6	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
C7	19A701225P5	Electrolytic: 680 uF, -10+50%, 35 VDCW.
C9	19A702250P113	Polyester: .1 uF ±10%, 50 VDCW.
C10	19B800858P1	Electrolytic: 4700 uF - 10+30%, 35 VDCW.
C11 and C12	19B800858P2	Electrolytic: 1000 uF - 10+30%, 50 VDCW.
C13	19B800858P1	Electrolytic: 4700 uF - 10+30%, 35 VDCW.
C14	19A702250P113	Polyester: .1 uF ±10%, 50 VDCW.
C15	19A701534P5	Tantalum: 2.2 uF ±20%, 35 VDCW.
C16	19A702250P113	Polyester: .1 uF ±10%, 50 VDCW.
C17	19A701534P5	Tantalum: 2.2 uF ±20%, 35 VDCW.
C18 thru C20	19A702250P113	Polyester: .1 uF ±10%, 50 VDCW.
C21 thru C23	19A700233P7	Ceramic: 1000 pF ±20%, 50 VDCW.
C24	19A701534P6	Tantalum: 4.7 uF ±20%, 35 VDCW.
		- - - - - - - - - - - - DIODES - - - - - - - - - - - -
D1	19A703588P5	Zener: sim to 1N6285A.
D2 and D3	19A703638P3	Rectifier, fast recovery: sim to MR822.
D4	T324ADP1041	Rectifier, silicon; general purpose.
D5	19A116783P2	Silicon: sim to MR756.
		- - - - - - - - - - - - JACKS - - - - - - - - - - - -
J1	19A116659P180	Printed wire: 3 contacts rated @ 5 amps, sim to Molex 09-88-2031.
J2	19A116659P165	Printed wire, 12 contacts rated @5 amps., sim to Molex 09-88-2121
J3	19A116659P101	Connector, printed wiring: 3 contacts rated at 5 amps; sim to Molex 09-60-1031.
J4	19A703248P2	Contact, electrical. (Quantity 4).
		- - - - - - - - - - - - COILS - - - - - - - - - - - -
L1	19B801134G1	Coil.
L2	19B801134G2	Coil.
L3	19B801134G1	Coil.
		- - - - - - - - - - TRANSISTORS - - - - - - - - - -
Q1 and Q2	19A143972P1	Silicon, PNP; sim to Motorolla MJ900.
		- - - - - - - - - - - - RESISTORS - - - - - - - - - - - -
R1 thru R3	19A701250P265	Metal film: 4.6K ohms ±1%, 1/4 w.
R4	19A701250P261	Metal film: 4.22K ohms ±1%, 1/4 w.
R6	H212CRP415C	Deposited carbon: 0.15M ohms ±5%, 1/4 w.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES.

SYMBOL	GE PART NO.	DESCRIPTION
R7	19A701250P317	Metal film: 14.7K ohms ±1%, 250 VDCW, 1/4 w.
R8	H212CRP147C	Deposited carbon: 470 ohms ±5%, 1/4 w.
R9 and R10	19A700111P65	Composition: 1.2K ohms ±5%, 2 w.
R11 and R12	H212CRP127C	Deposited carbon: 270 ohms ±5%, 1/4 w.
R15	5493035P53	Wirewound: 18 ohms ±5%, 5 w.
R16	5493035P14	Wirewound: 0.1 ohm ±10%, 7 w.
R18	19A701250P189	Metal film: 825 ohms ±1%, 250 VDCW, 1/4 w.
R19	19A701250P141	Metal film: 261 ohms ±1%, 250 VDC, 1/4 w.
R20	5493035P14	Wirewound: 0.1 ohm ±10%, 7 w.
R21	19A701250P249	Metal film: 3.16K ohms ±1%, 1/4 w.
R22	19A701250P141	Metal film: 261 ohms ±1%, 250 VDC, 1/4 w.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - - -
U1	19A703102P1	VOLTAGE REGULATOR, sim to Silicon General SG2524J
U3	19A701989P1	Linear, Positive Voltage Regulator; sim to LM3177.
		- - - - - - - - - MISCELLANEOUS - - - - - - - - -
	19B801061P2	Release latch.
	19B801061P5	Release latch knob.
	19B232801P2	Support. (Mounts U3).
	19B801133G1	Heat sink. (Used with Q1 and Q2).
	4029974P1	Insulator, plate: aluminum. (Used with Q1 and Q2).
	19A703632P1	Insulator, bushing. (Used with Q1 and Q2).
	19A700068P1	Insulator, bushing. (Used with U3).
	19A700115P3	Insulator, plate. (Used with U3).

PARTS LIST

HEAT SINK ASSEMBLY, AS
19B801132G1

ISSUE 2

SYMBOL	GE PART NO.	DESCRIPTION
		- - - - - - - - - - - - PLUGS - - - - - - - - - - - -
P3		Connector. Includes:
	19A116668P16	Shell.
	19A116781P4	Contact, electrical: wire range No. 22-26 AWG; sim to Molex 08-50-0107. (Quantity 3).
		- - - - - - - - - INTEGRATED CIRCUITS - - - - - - - -
U1	19A134768P1	Linear. 3 AMP POSITIVE REGULATOR.
		- - - - - - - - - - MISCELLANEOUS - - - - - - - - - -
	19A703624G1	Heat sink.
	4029974P1	Insulator, plate: aluminum.
	19A134260P1	Insulator cover.
	19A115222P3	Washer, shield.
	4036835P9	Solderless terminal. (Located at U1-1, U1-2).
	4036634P1	Contact, electrical. (Quantity 2).

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES.

ALARM/CONTROL INTERFACE BOARD
19D901331G3

ISSUE 2

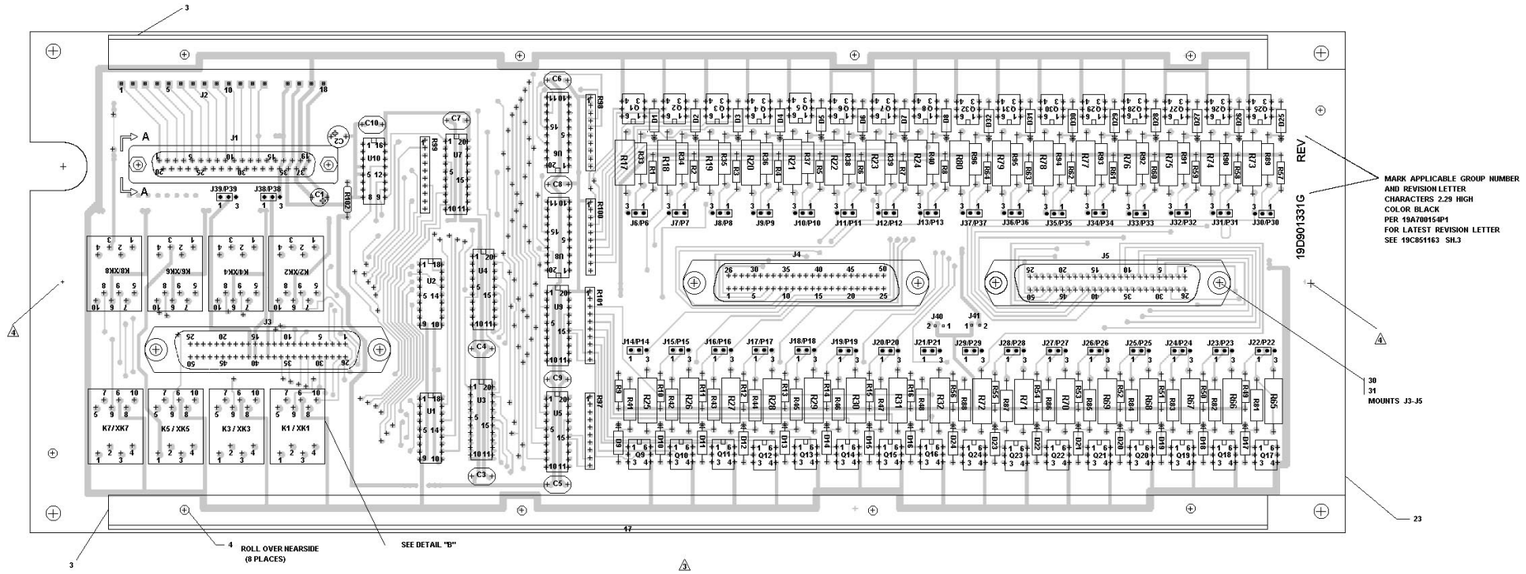
SYMBOL	GE PART NO.	DESCRIPTION
		- - - - - - - - - - CAPACITORS - - - - - - - - - -
C1	19A701534P6	Tantalum: 4.7 uF + or -20%, 35 VDCW.
C2	19A701534P9	Tantalum: 47 uF + or -20%, 6.3 VDCW.
C3 thru C10	19A702250P113	Polyester: 0.1 uF + or -10%, 50 VDCW.
		- - - - - - - - - - - DIODES - - - - - - - - - - -
D1 thru D32	T324ADP1041	Rectifier, silicon; general purpose.
		- - - - - - - - - - - JACKS - - - - - - - - - - -
J1	19B209727P24	Plug, power: 37 contacts, sim to AMP 205714-1.
J2	19A701785P2	Contact, electrical; sim to Molex -08-50-0404.
J3 thru J5	19B800935P3	Rectangular: 50 position; sim to Amp 552118-1.
J6 thru J41	19A703248P2	Contact, electrical.
		- - - - - - - - - - - RELAYS - - - - - - - - - - -
K1 thru K8	19B209487P1	Enclosed: 134 ohms + or - 10%, 13.6 VDC nominal, 2 form C contact; sim to Allied Control T351-X-34.
		- - - - - - - - - - - PLUGS - - - - - - - - - - -
P6 thru P39	19A702104P1	Receptacle: 2 position, shorting, rated at 3 amps; sim to Berg 65474-002.
		- - - - - - - - - - TRANSISTORS - - - - - - - - - -
Q1 thru Q32	19A701766P1	Coupler, optoelectronic.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1 thru R16	19A700106P71	Composition: 2.2K ohms + or -5%, 1/4 w.
R17 thru R32	19A700112P63	Composition: 1K ohms + or - 5%, 1 w.
R33 thru R48	19A700113P55	Composition: 470 ohms + or - 5%, 1/2 w.
R49 thru R64	19A700106P71	Composition: 2.2K ohms + or -5%, 1/4 w.
R65 thru R80	19A700112P63	Composition: 1K ohms + or - 5%, 1 w.
R81 thru R96	19A700113P55	Composition: 470 ohms + or - 5%, 1/2 w.
R97 thru R101	19A701630P5	9 Network: 100K ohms + or - 2% each @ 50 VDC; sim to Bourns 4310R-101-104.
R102	H212CRP210C	Deposited carbon: 1K ohms + or -5%, 1/4 w.
		- - - - - - - - - INTEGRATED CIRCUITS - - - - - - - - -
U1 and U2	19A134693P2	Interface: sim to ULN-2803A.
U3 and U4	19A700037P411	Digital: DF-F WITH CLEAR.
U5 thru U9	19A700037P408	Digital: (OCTAL TRI-STATE DRIVER).
U10	19A700037P358	Digital: TTL, LOW POWER SCHOTTKY, DECODER DEMULTIPLEXER.
		- - - - - - - - - - SOCKETS - - - - - - - - - -
XK1 thru XK8	19C851320P3	2 Pole PWB Socket.
		- - - - - - - - - - MISCELLANEOUS - - - - - - - - - -
	19B801240P1	Support.
	19B800608P154	Rivet, tubular.
	19C851320P5	Socket, relay: sim to T-00102. (Used with K1-K8).
	19B209727P10	Screwlock; female, sim to Amp 205-817-1. (Used with J1).
	19B209727P13	Bushing, standoff. (Used with J1).

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES.

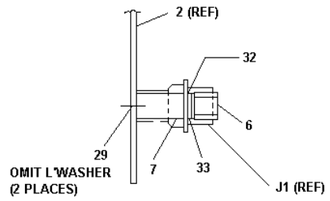
DISPLAY ASSEMBLY
19C851341G1

ISSUE 3

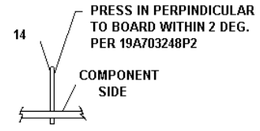
SYMBOL	GE PART NO.	DESCRIPTION
		DISPLAY BOARD 19D901320G1
		-- ---------- CAPACITORS ----------
C1	19A701534P7	Tantalum: 10 uF ±20%, 16 VDCW.
C2 thru C6	19A700121P6	Ceramic: 0.1 uF ±20%, 50 VDCW.
C7	19A701534P6	Tantalum: 4.7 uF ±20%, 35 VDCW.
C8 thru C10	19A700121P6	Ceramic: 0.1 uF ±20%, 50 VDCW.
		-- ---------- DIODES -- ----------
H1 thru H14	19A134354P5	Diode, optoelectronic: red; sim to Hew. Packard 5082-4693.
H16 thru H32	19A134354P5	Diode, optoelectronic: red; sim to Hew. Packard 5082-4693.
H33 thru H40	19A134354P4	Diode, optoelectronic: Green; sim to Hew. Packard 5082-4992.
H41 thru H56	19A134354P8	Diode, optoelectronic: yellow; sim to Hew. Packard 5082-4592.
		-- ---------- JACKS -- ----------
J1	19A701785P2	Contact, electrical; sim to Molex -08-50-0404. (Quantity 16).
		-- ---------- RESISTORS -- ----------
R1 thru R56	19A700113P73	Composition: 2.7K ohms ±5%, 1/2 w.
		-- ---------INTEGRATED CIRCUITS -- --------
U1 thru U5	19A700037P411	Digital: DF-F WITH CLEAR.
U6 thru U10	19A134693P2	Interface: sim to ULN-2803A.
U11 and U12	19A700037P411	Digital: DF-F WITH CLEAR.
U13 and U14	19A134693P2	Interface: sim to ULN-2803A.
U15	19A700037P358	Digital: TTL, LOW POWER SCHOTTKY, DECODER DEMULTIPLEXER.
		-- --------- MISCELLANEOUS -- ---------
	N80P13010J2	Machine screw, pan head. (Secures Display Board & Panel).
	N402P7J2	Washer, plain: No. 6. (Secures Display Board & Panel).
	19A701235P15	Spacer.
	19D901319P1	Display panel frame.
	19C851322P1	Display panel.



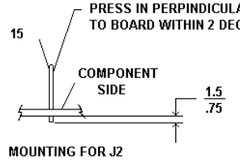
(19D901331, Sh. 2, Rev. 2)
(19D705359, Sh. 1, Rev. 0)



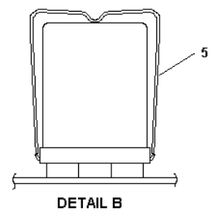
SECTION A - A



MOUNTING FOR 76 - J41



MOUNTING FOR J2

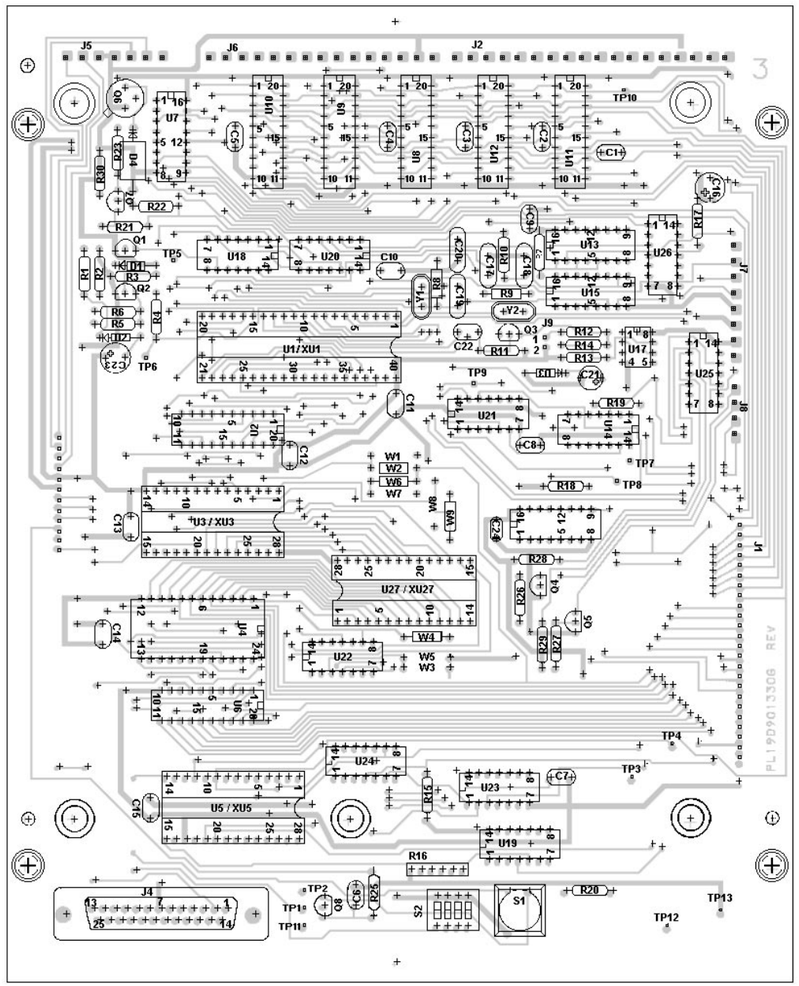


DETAIL B
K1/XK1 - K8/XK8

22 NOTES:

1. SOLDER ALL ELECTRICAL CONNECTIONS.
2. COMPONENT LEADS TO PROTRUDE 1.6 MAX. BELOW SOLDER SIDE OF BOARD.
3. INDICATES FRONT OF COMPONENT AUTO INSERTION MACHINES.
4. BOARD ERROR CORRECTION HOLES.

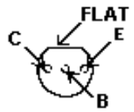
ALARM/CONTROL INTERFACE BOARD
19D901331G3



(19D901329, Sh. 1, Rev. 4)
(19A704066, Sh 1, Rev. 3)

LOGIC BOARD
19D901330G3

LEAD IDENTIFICATION
FOR Q1-Q5, Q7 & Q8

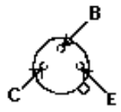


IN - LINE

TOP VIEW

NOTE: CASE SHAPE IS DETERMINING FACTOR FOR LEAD IDENTIFICATION.

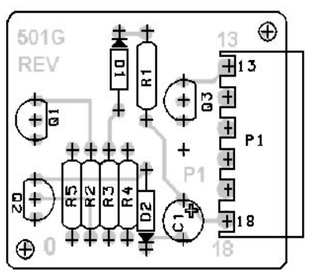
LEAD IDENTIFICATION
FOR Q6



TRIANGULAR

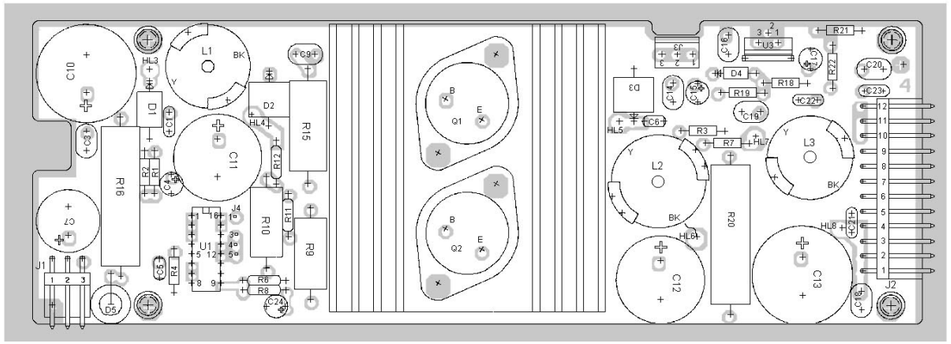
TOP VIEW

NOTE: LEAD ARRANGEMENT IS DETERMING FACTOR FOR LEAD IDENTIFICATION.



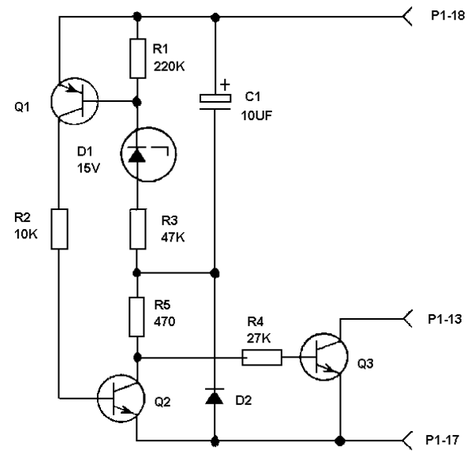
(19C851503, Rev. 0)
(19A704861, Sh. 1, Rev. 0)

POWER-ON RESET BOARD
19C851501G1



REGULATOR BOARD
19D901039G1

(19D901040, Sh. 1, Rev. 2)
(19A703354, Sh. 1, Rev. 4)



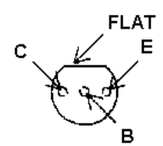
NOTES:

1. ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED. RESISTOR VALUES IN ⎍ UNLESS FOLLOWED BY MULTIPLIER K OR M. CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER U, N OR P.

MODEL NO.	REV LETTER
PL19C851501G1	

(19B801395, Sh. 1, Rev. 0)

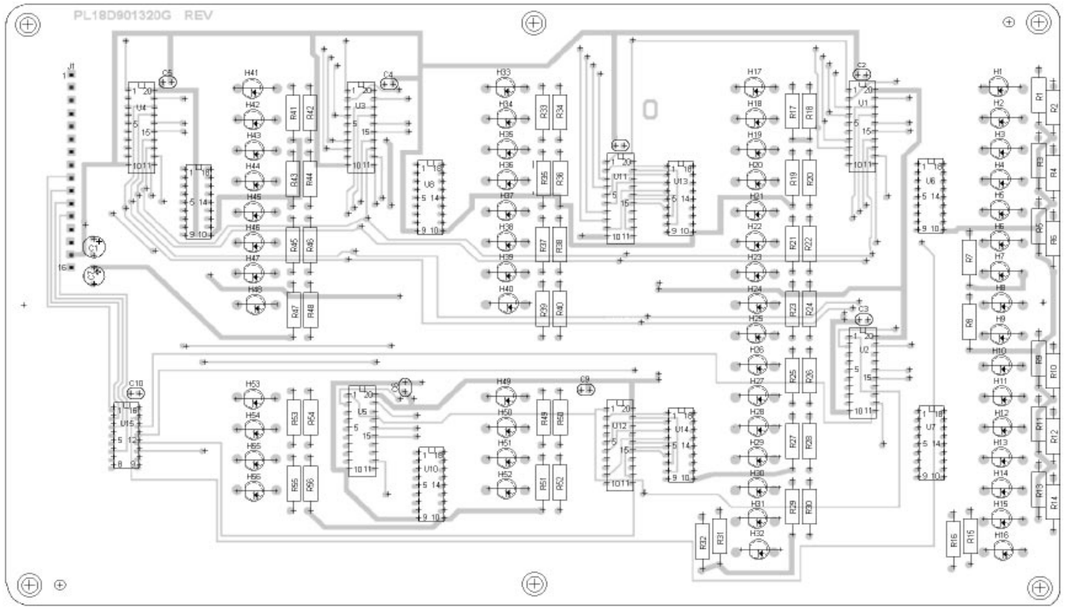
LEAD IDENTIFICATION
FOR Q1 - Q3



IN-LINE

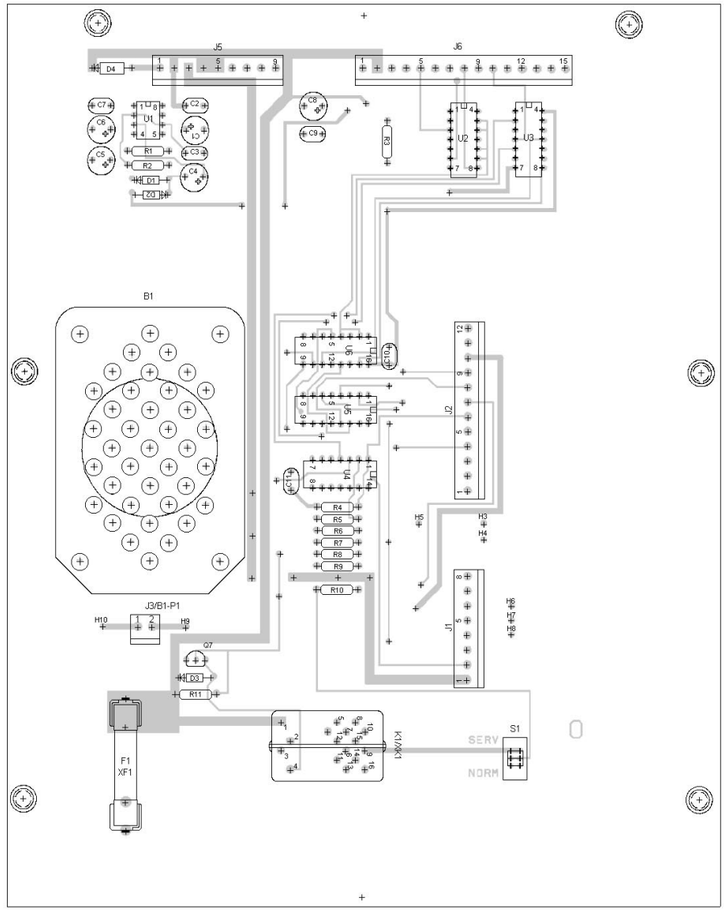
TOP VIEW

NOTE: CASE SHAPE IS DETERMINING FACTOR FOR LEAD IDENTIFICATION.



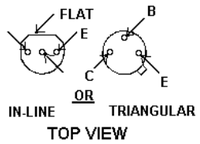
(19D901322, Rev. 0)
(19A704042, Sh. 1, Rev. 0)

DISPLAY BOARD
19D901320G1



(19D901849, Sh. 1, Rev. 0)
(19A705098, Sh. 1, Rev. 0)

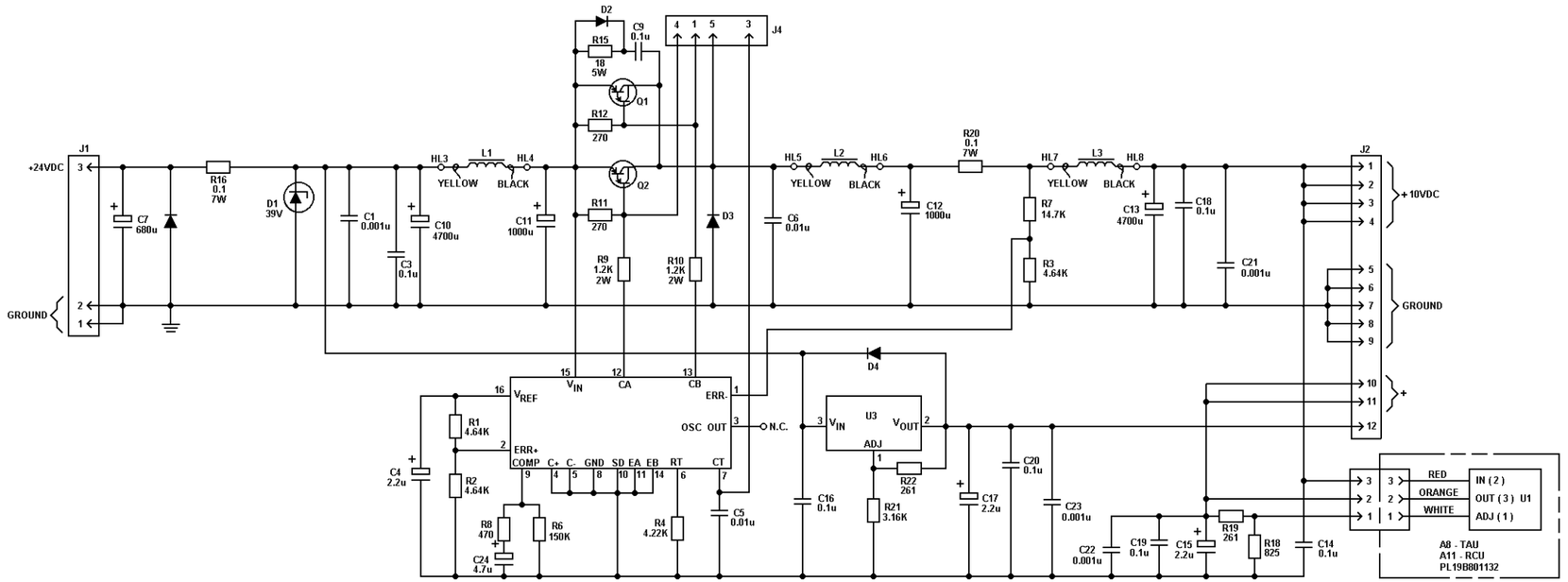
LEAD IDENTIFICATION
FOR Q1



TOP VIEW

NOTE: LEAD ARRANGEMENT, AND NOT CASE SHAPE, IS DETERMINING FACTOR FOR LEAD IDENTIFICATION.

SERIAL INTERFACE BOARD
19D901848G1

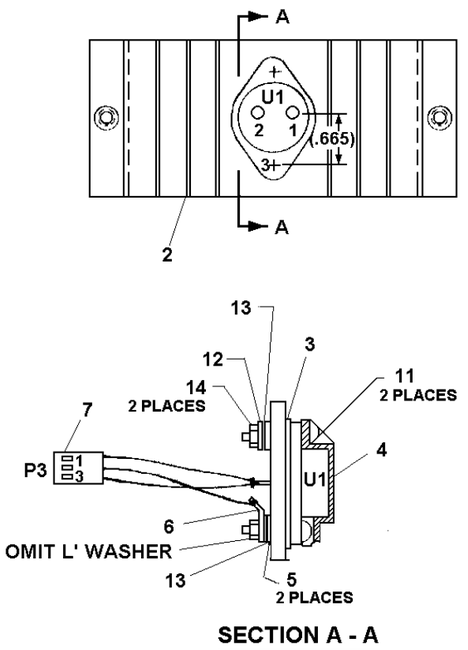


ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED.
RESISTOR VALUES IN Ω UNLESS FLOWWED BY MULTIPLIER k OR M.
CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER µ,n OR p.
INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER m OR µ.

THIS ELEM DIAG APPLIES TO	
MODEL NO.	REV LETTER
PL19D901039G1	

(19D901176, Rev. 2)

REGULATOR BOARD
19D901039G1



SECTION A - A

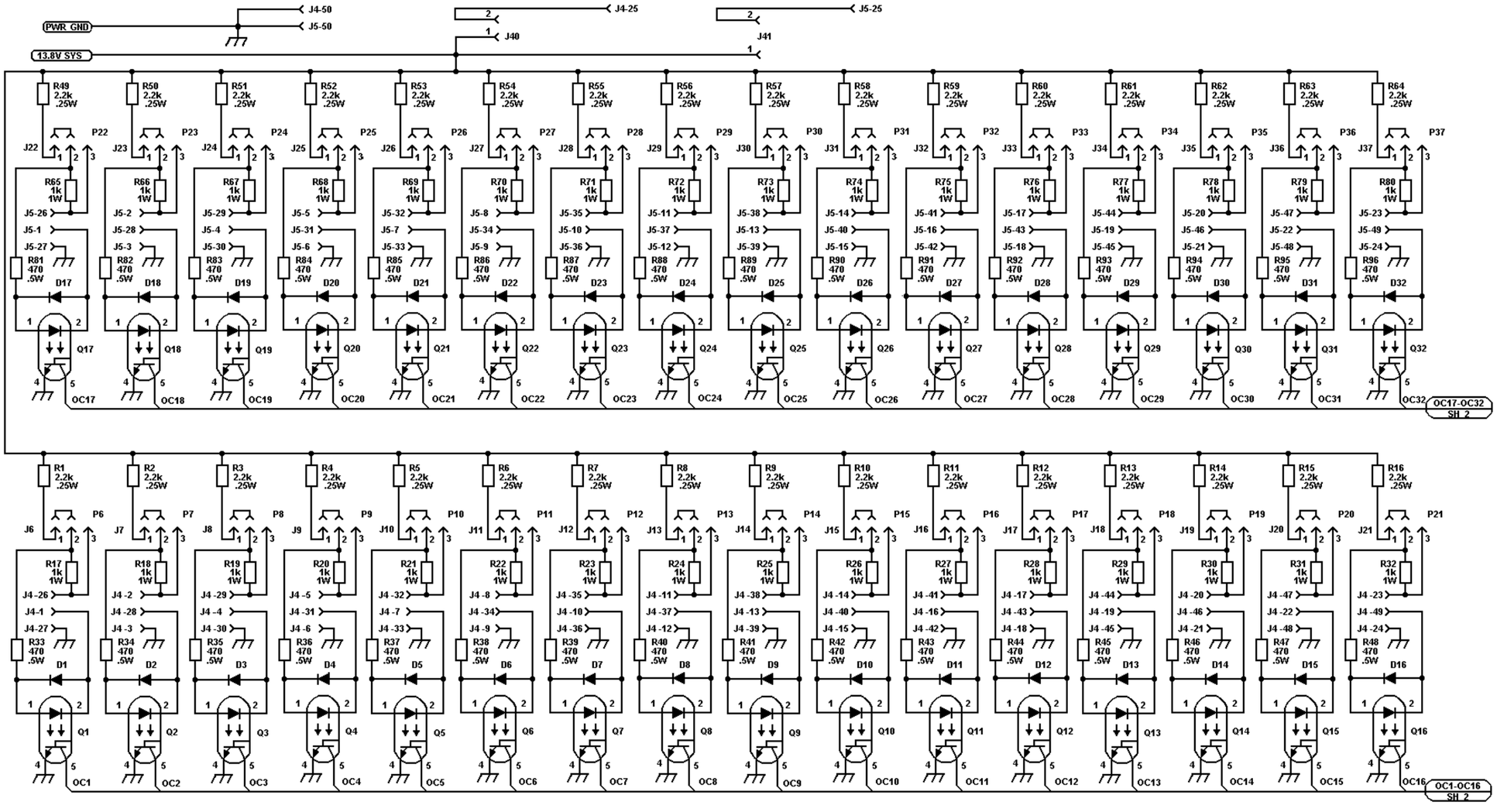
1 **NOTES:**

1. SOLDER ALL ELECTRICAL CONNECTIONS.
2. SOLDER ITEM 10 TO U1-1 & 2.

CONNECTIONS CHART				
FROM	TERM	WIRE	TO	TERM
U1-1	ITEM 10	SF22-W	P3-1	ITEM 8
U1-3	ITEM 6	SF22-O	P3-2	ITEM 8
U1-2	ITEM 10	SF22-R	P3-3	ITEM 8

(19B801132, Rev. 2)

HEAT SINK ASSEMBLY
19B801132G1



NOTE:

⚠ RELAYS ARE SHOWN IN RESET POSITION.

RESISTOR VALUES IN Ω UNLESS FOLLOWED BY MULTIPLIER k OR M.
CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER μ, n OR p.
INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER m OR μ.

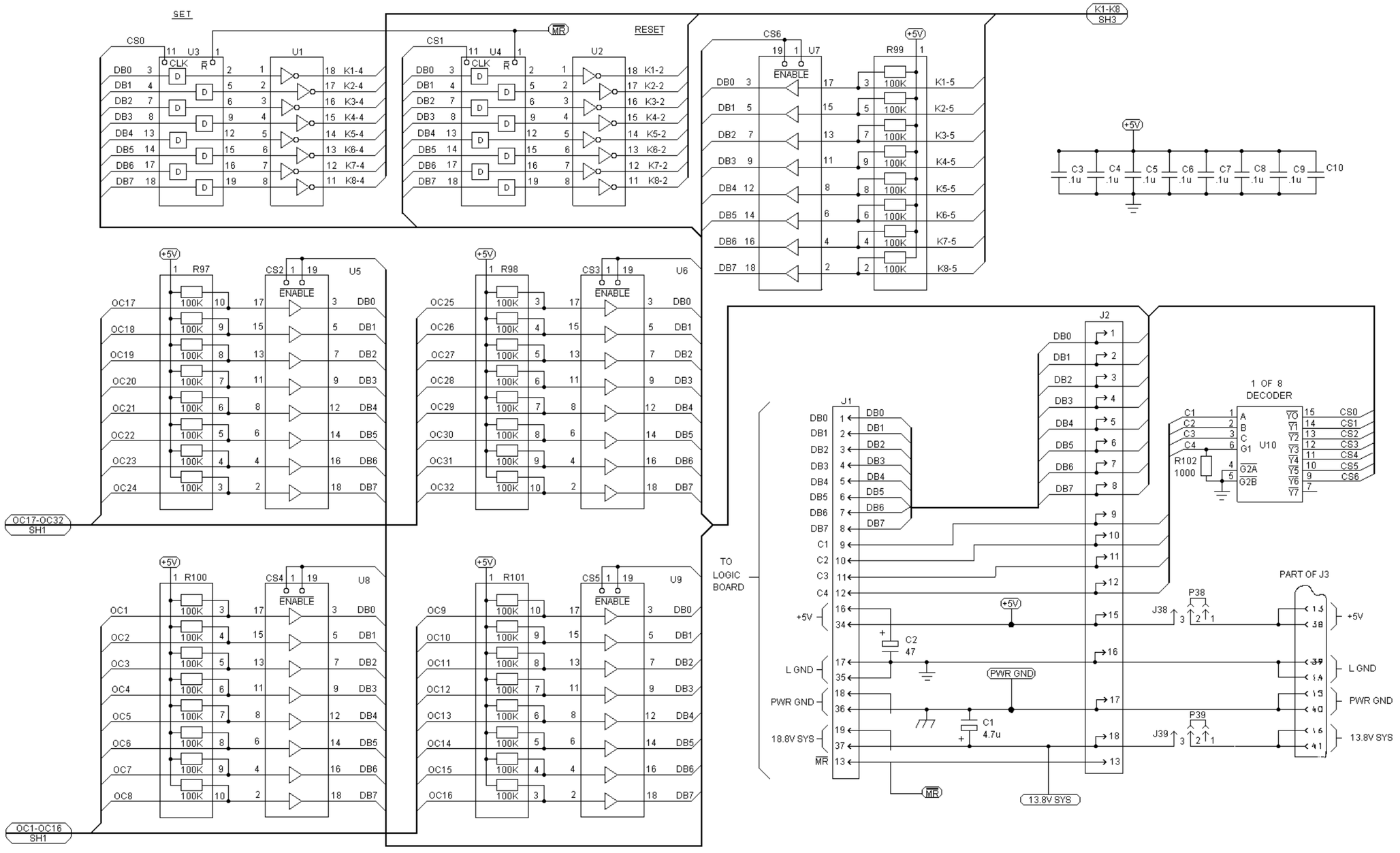
MODEL NO.	REV. LETTER
PL19D901331G3	
PL19D901331G4	

PWR AND GND CONNECTIONS

DEVICE	+5V VCC PIN NO	+24 VCC PIN NO	LOG GND PIN NO	PWR GND PIN NO
U1, U2		10		9
U3-U9	20		10	
U10	16		8	

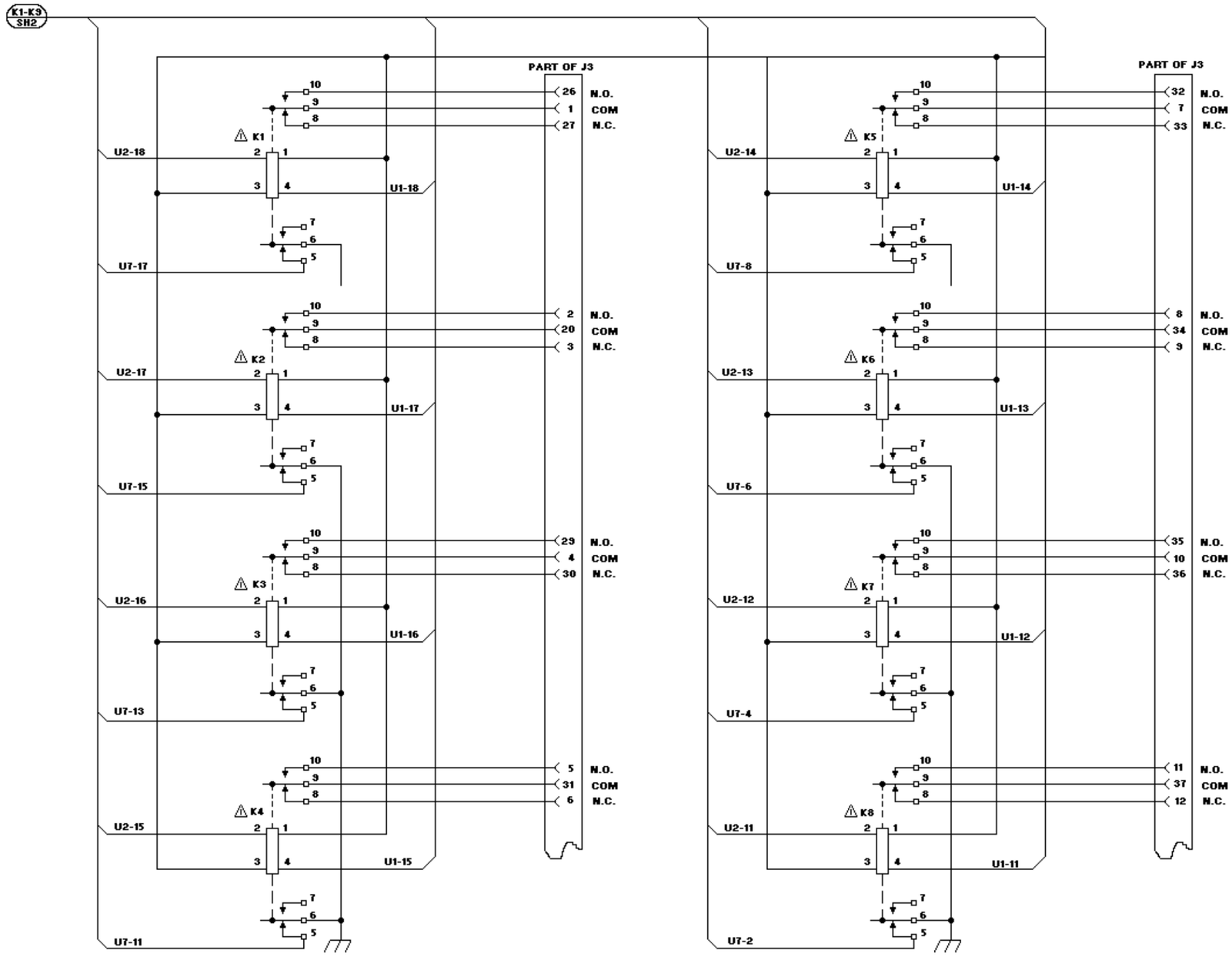
ALARM/CONTROL INTERFACE BOARD
19D901331G3

(19D901976, Sh. 1, Rev. 1)



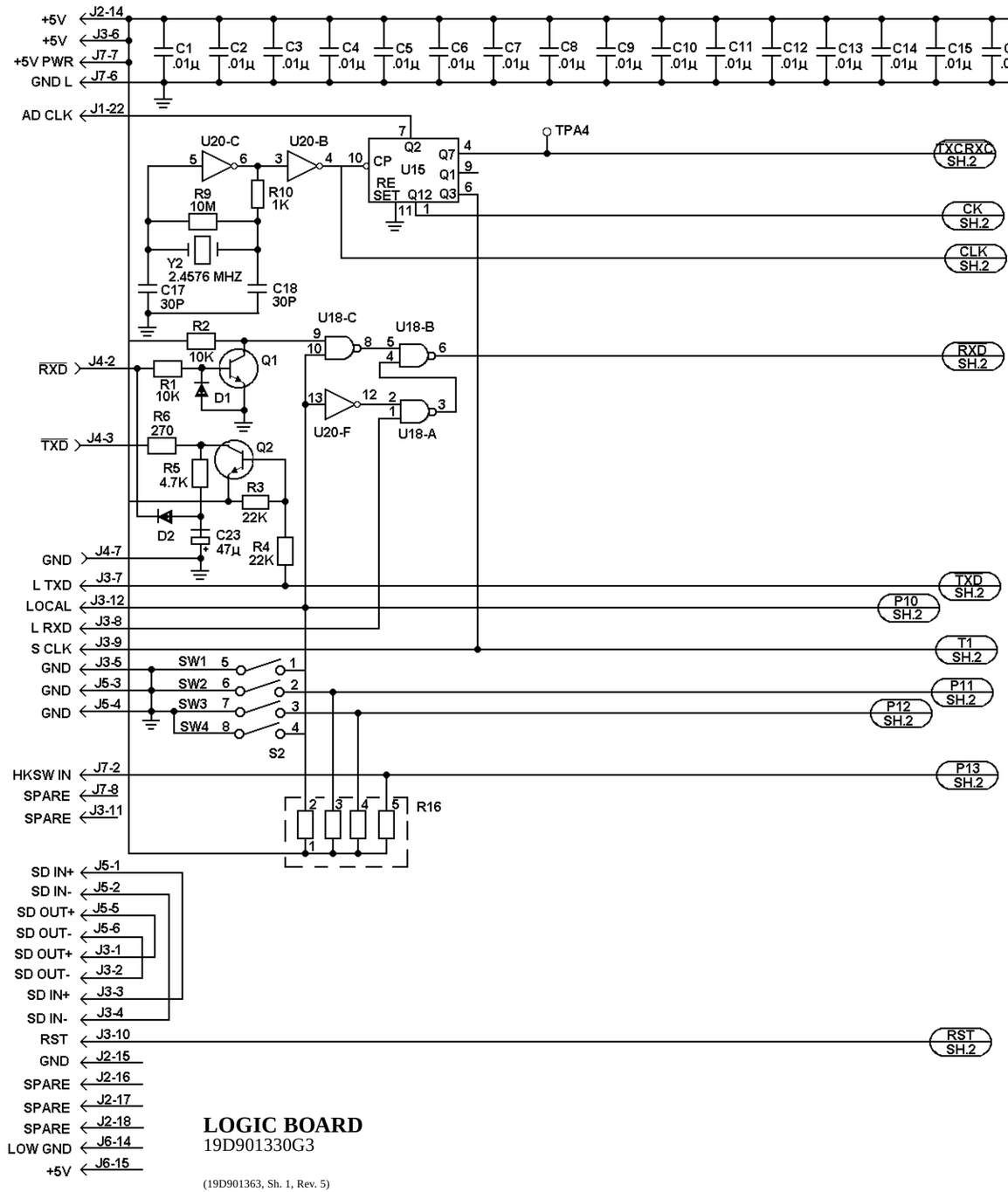
ALARM/CONTROL INTERFACE BOARD
19D901331G3

(19D901976, Sh. 2, Rev. 1)



ALARM/CONTROL INTERFACE BOARD
19D901331G3

(19D901976, Sh. 3, Rev. 1)



LOGIC BOARD
19D901330G3

(19D901363, Sh. 1, Rev. 5)

PWR & GND CONNECTIONS

DEVICE	VCC (+5V) PIN NO.	GND PIN NO.
U1	40	20
U2	20	10
U3	28	14
U4	24	12
U5	26	4
U6	20	10
U7	16	8
U8-12	20	10
U13	16	8
U14	14	7
U15	16	8

DEVICE	VCC (+5V) PIN NO.	GND PIN NO.
U16	16	8
U17	8	1
U18-U23	14	7
U24	14	7
U25	14	7
U26	14	7
XU27	28	14

SPARE GATES

DEVICE	INPUT PIN NO.	OUTPUT PIN NO.
U19		
U21	1,3	2,4
U22	1,5,13	2,6,12
U23	4,5,9,10	6,8
	12,13	11
U24	1,2,12,13	3,11
U26-B		

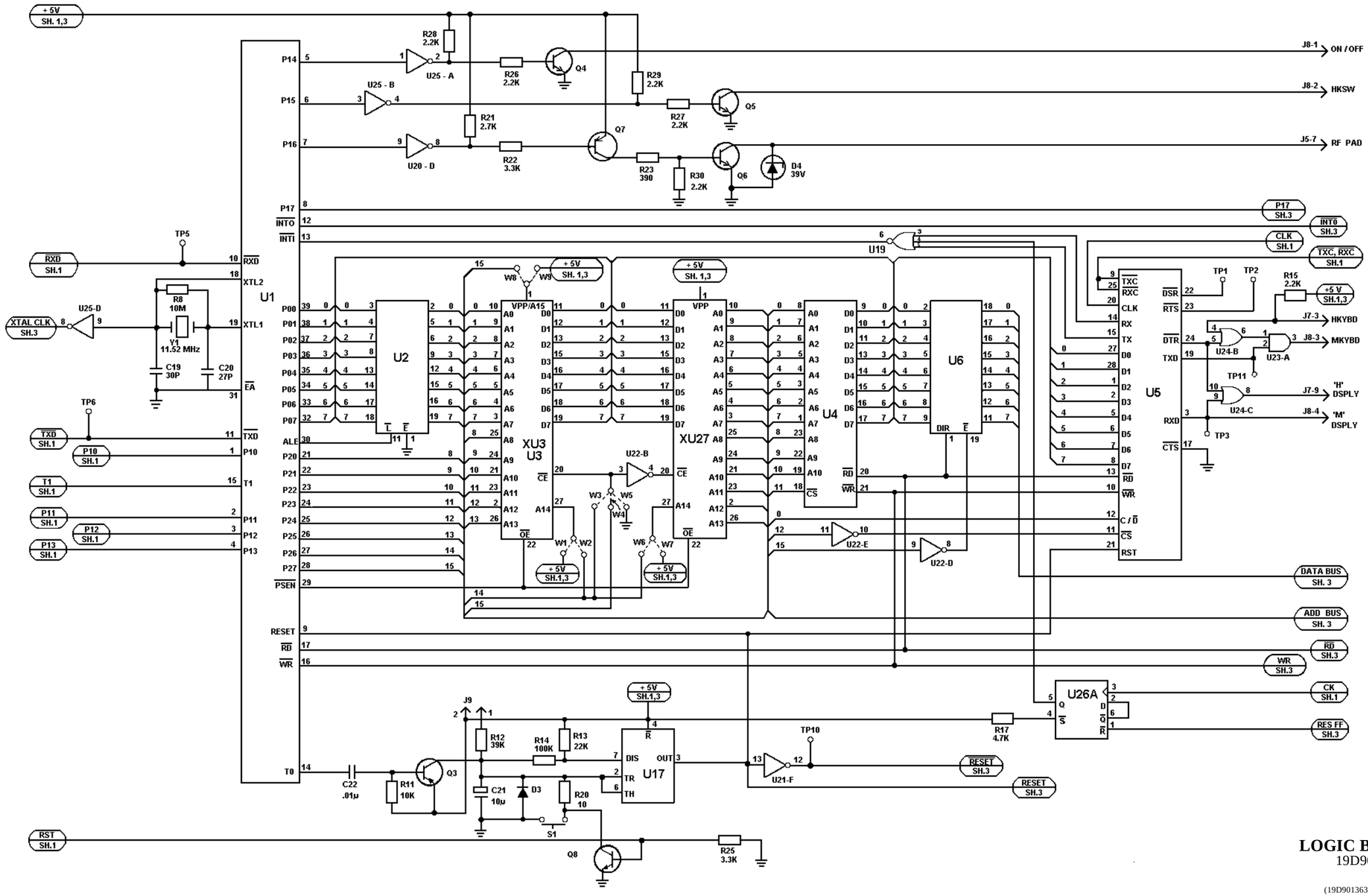
JUMPER CONFIGURATION FOR 27128/27256

* U27 NOT USED IN GROUP 3

	U3	*U27	JUMPER W1/W2	JUMPERS W3/W4/W5	JUMPERS W6/W7	JUMPERS W8/W9
ONE 16K 27128	$\overline{CE}$ = GND A14 = VCC		W1	W5		W9
ONE 32K 27256	$\overline{CE}$ = GND A14 = AB14		W2	W5		W9
TWO 16K 27128	$\overline{CE}$ = AB14 A14 = VCC	$\overline{CE}$ = AB14 A14 = VCC	W1	W3	W7	W9
TWO 32K 27256	$\overline{CE}$ = AB15 A14 = AB14	$\overline{CE}$ = AB15 A14 = AB14	W2	W4	W6	W9
ONE 64K 27512	$\overline{CE}$ = GND A14 = AB14		W2	W5		W8

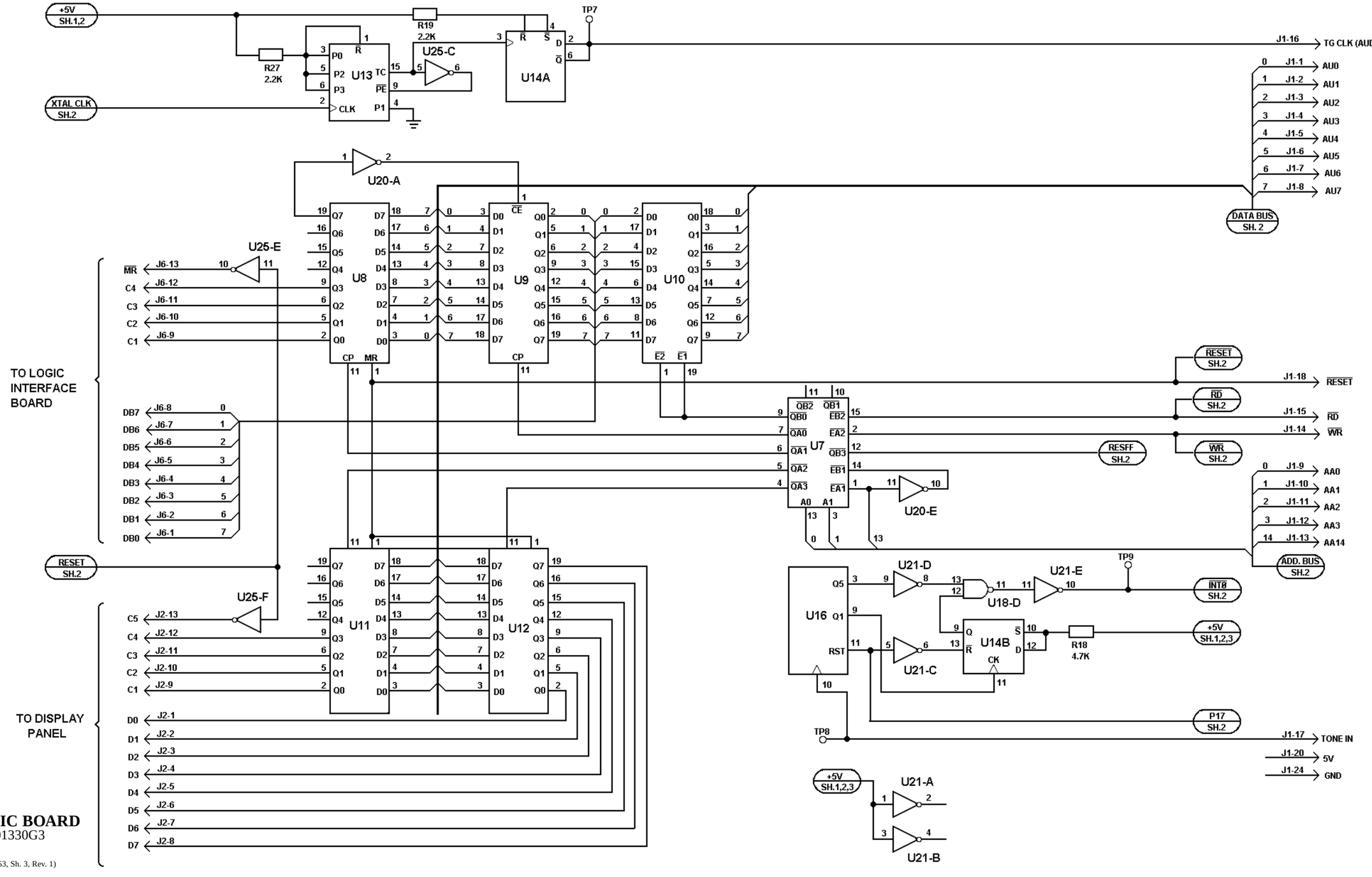
ALL RESISTORS ARE 1/2 WATT UNLESS OTHERWISE SPECIFIED.
RESISTOR VALUES IN Ω UNLESS FOLLOWED BY MULTIPLIER k OR M.
CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER µ, n OR p.
INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER m OR µ.

MODEL NO.	REV LETTER
PL19D901330G1	D
PL19D902330G3	



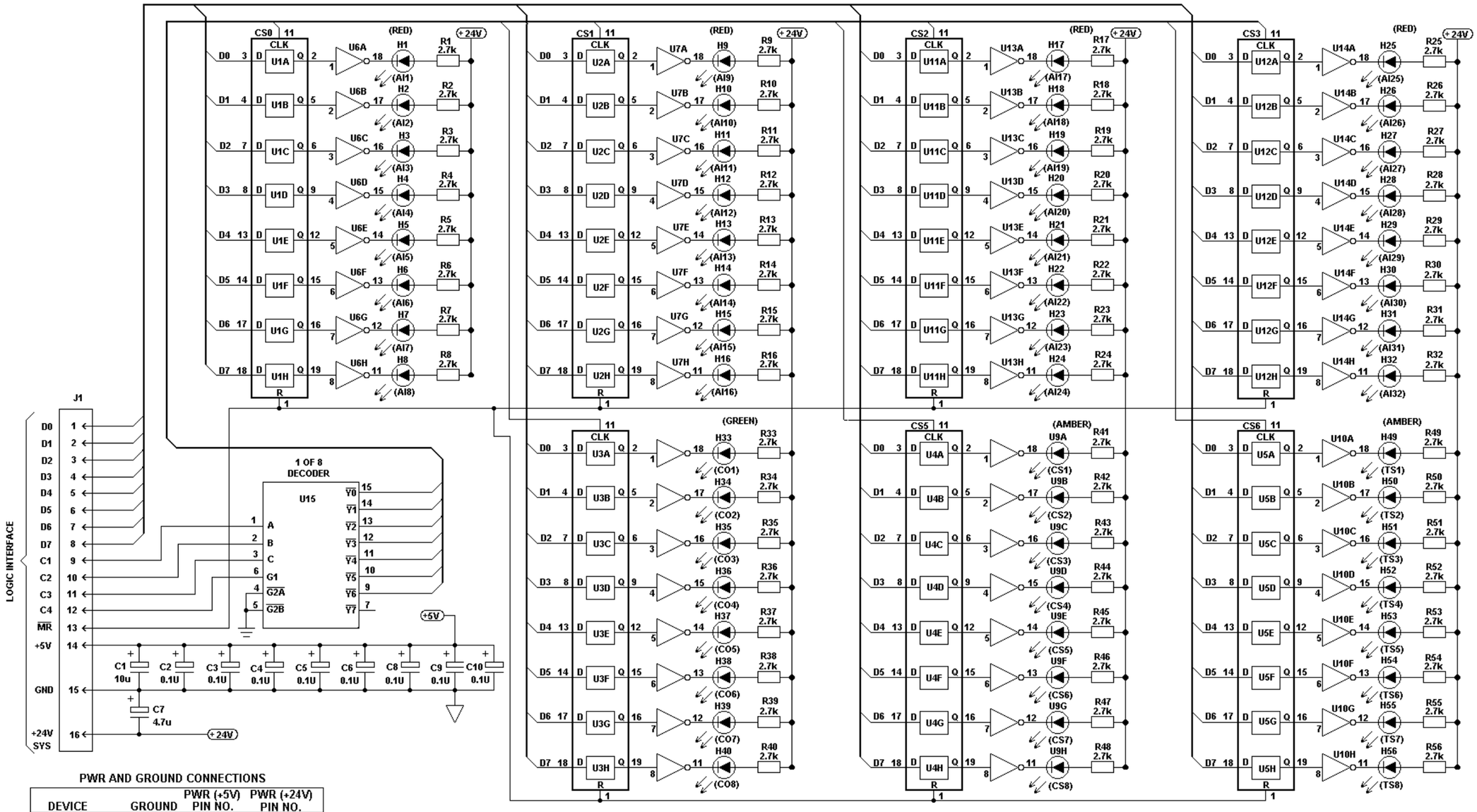
LOGIC BOARD
19D901330G3

(19D901363, Sh. 2, Rev. 1)



LOGIC BOARD
19D901330G3

(19D901363, Sh. 3, Rev. 1)



PWR AND GROUND CONNECTIONS

DEVICE	GROUND	PWR (+5V) PIN NO.	PWR (+24V) PIN NO.
U1,2,3,4,5,11,12	10	20	
U6,7,8,9,10,13,14	9		10
U15	8	16	

ALL RESISTORS ARE 1/2 WATT UNLESS OTHERWISE SPECIFIED.
RESISTOR VALUES IN Ω UNLESS FOLLOWED BY MULTIPLIER k OR M.
CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER µ, n OR p.
INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER m OR µ.

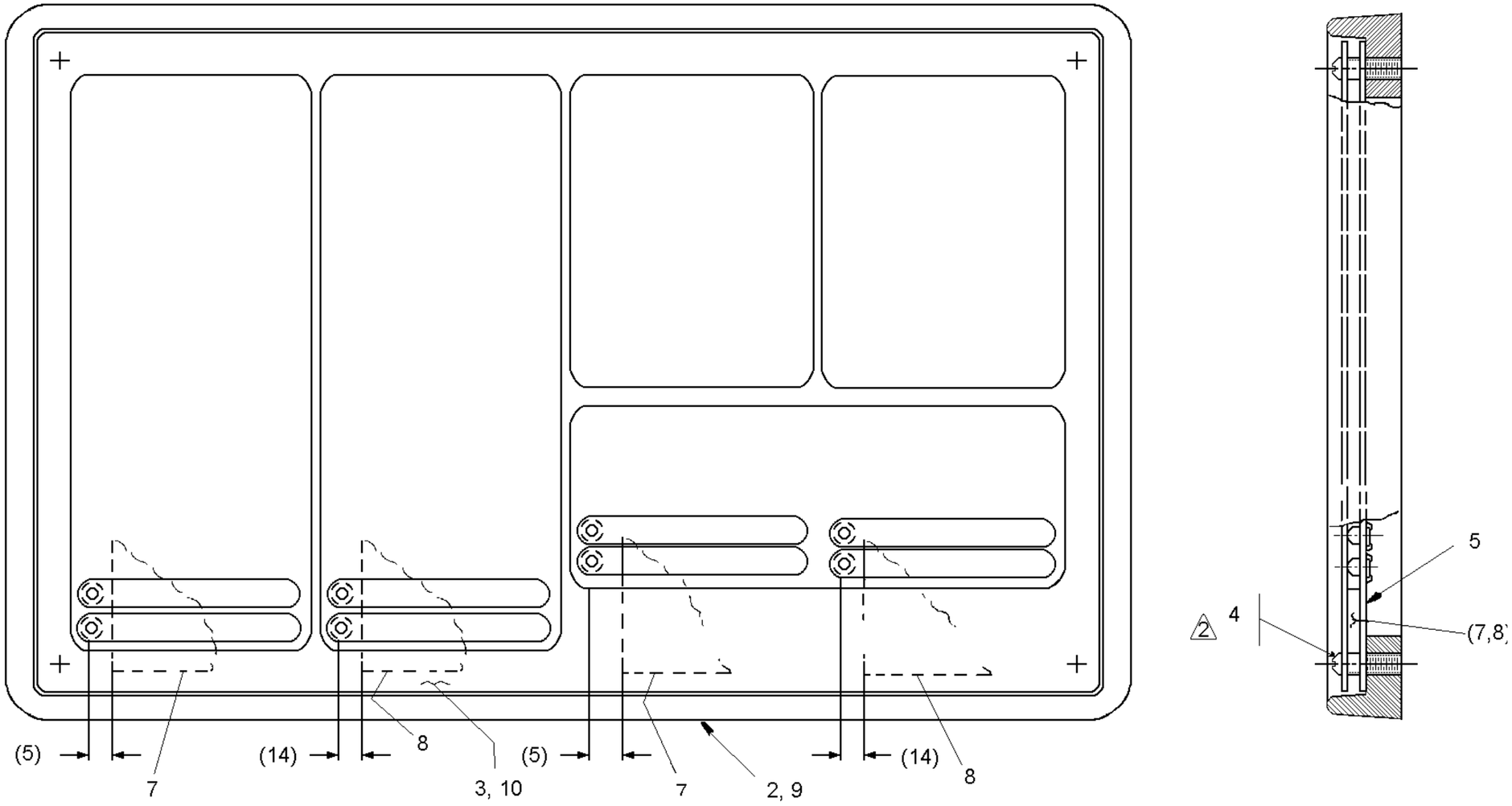
MODEL NO.	REV. LETTER
PL19D901320G1	

(19D901362, Sh. 1, Rev. 2)

LED DESIGNATIONS

FUNCTION	LED'S USED
ALARM INPUT (1-32)	H1-H32
CONTROL OUT (1-8)	H33-H40
CSC STATUS	H41-H48
TAU STATUS	H49-H56

DISPLAY BOARD
19D901320G1



NOTE:

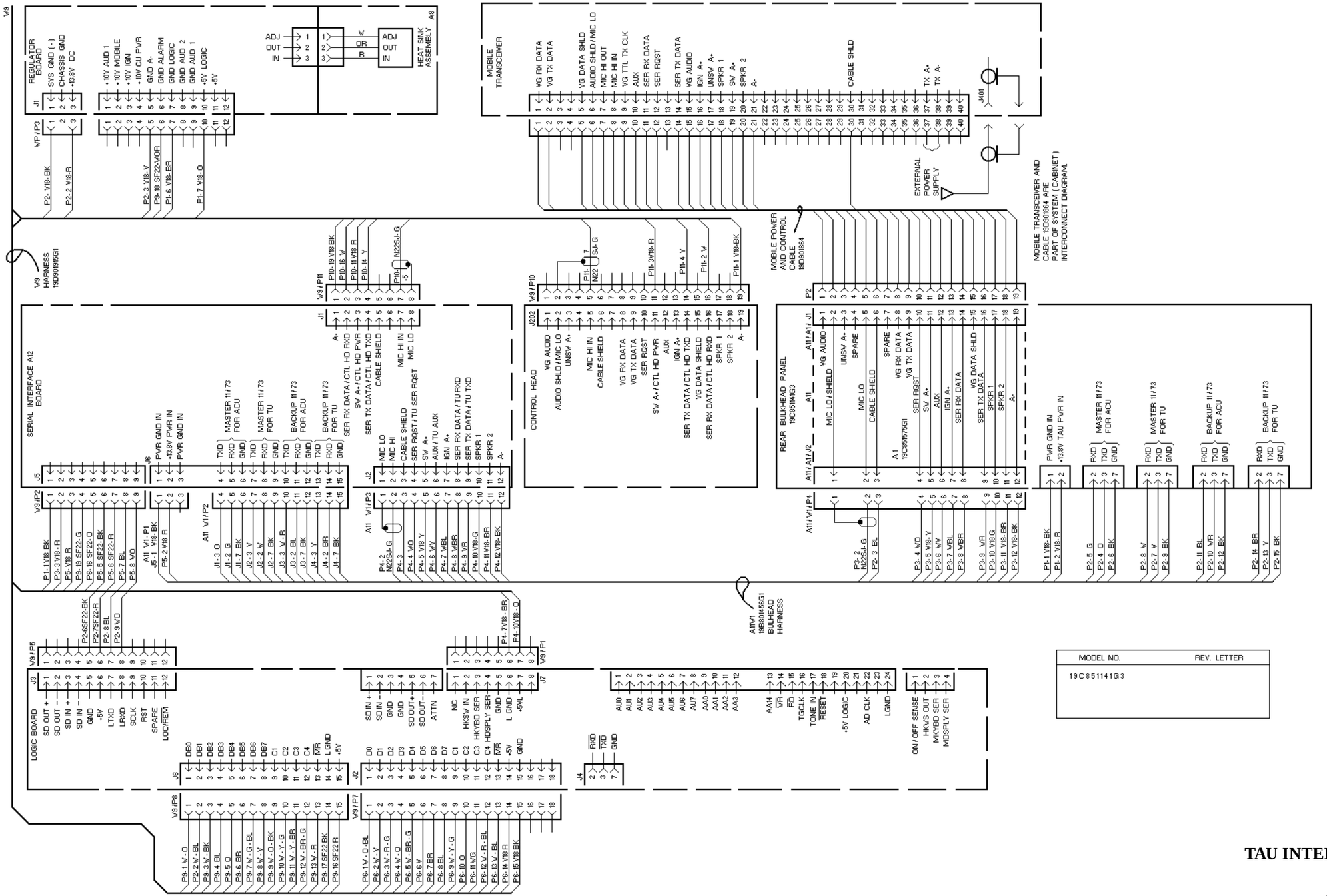
1. ASM ITEMS 7 & 8 TO THIS SIDE OF ITEMS AS SHOWN UP (5MM) FROM EDGE OF ITEM 5.

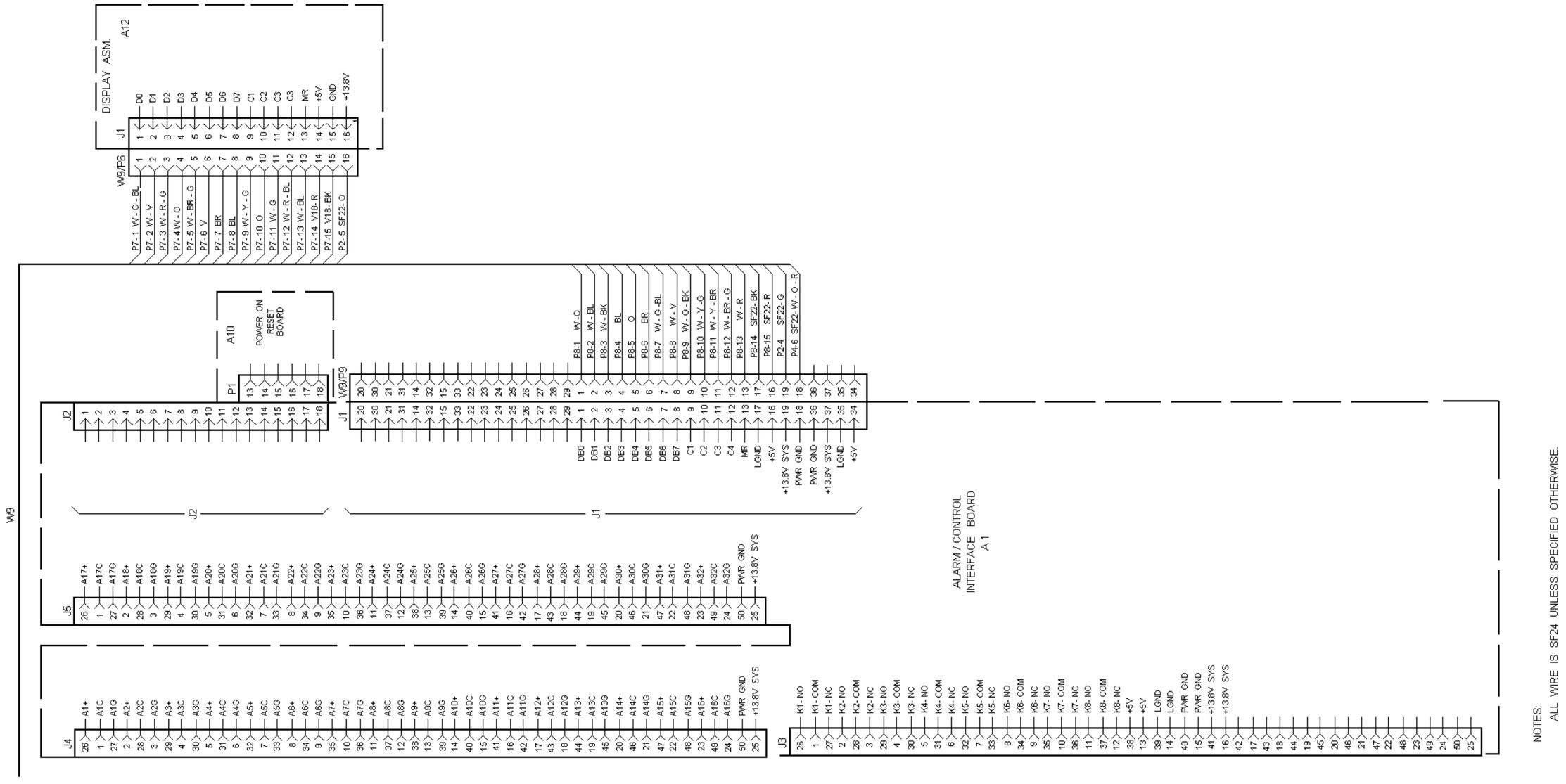
△2 STAKE SCREW, THEN TIGHTEN WITHOUT DAMAGING ITEM 3 OR 10.

1

DISPLAY ASSEMBLY
19C851341G2

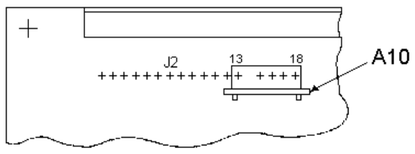
(19C851341, Rev. 4)


REGULATOR BOARD
HEAT SINK ASSEMBLY A8
MOBILE TRANSCEIVER
EXTERNAL POWER SUPPLY
J401
MOBILE POWER AND CONTROL CABLE 19D901864
MOBILE TRANSCEIVER AND CABLE 19D901864 ARE PART OF SYSTEM (CABINET) INTERCONNECT DIAGRAM.
V9 HARNESS 19D901915G1
SERIAL INTERFACE A12 BOARD
CONTROL HEAD
REAR BULKHEAD PANEL 19C851141G3
LOGIC BOARD
A11 BULKHEAD HARNESS 19B801456G1
MODEL NO. REV. LETTER
19C851141G3
TAU INTERCONNECT
19D901365G2
(19D901898, Sh. 1, Rev. 2)

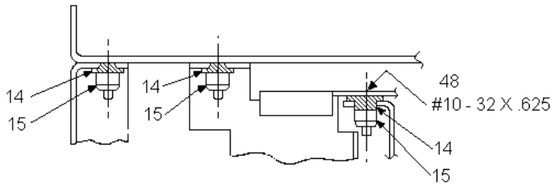


TAU INTERCONNECT
19D901365G2

(19D901898, Sh. 2, Rev. 1)

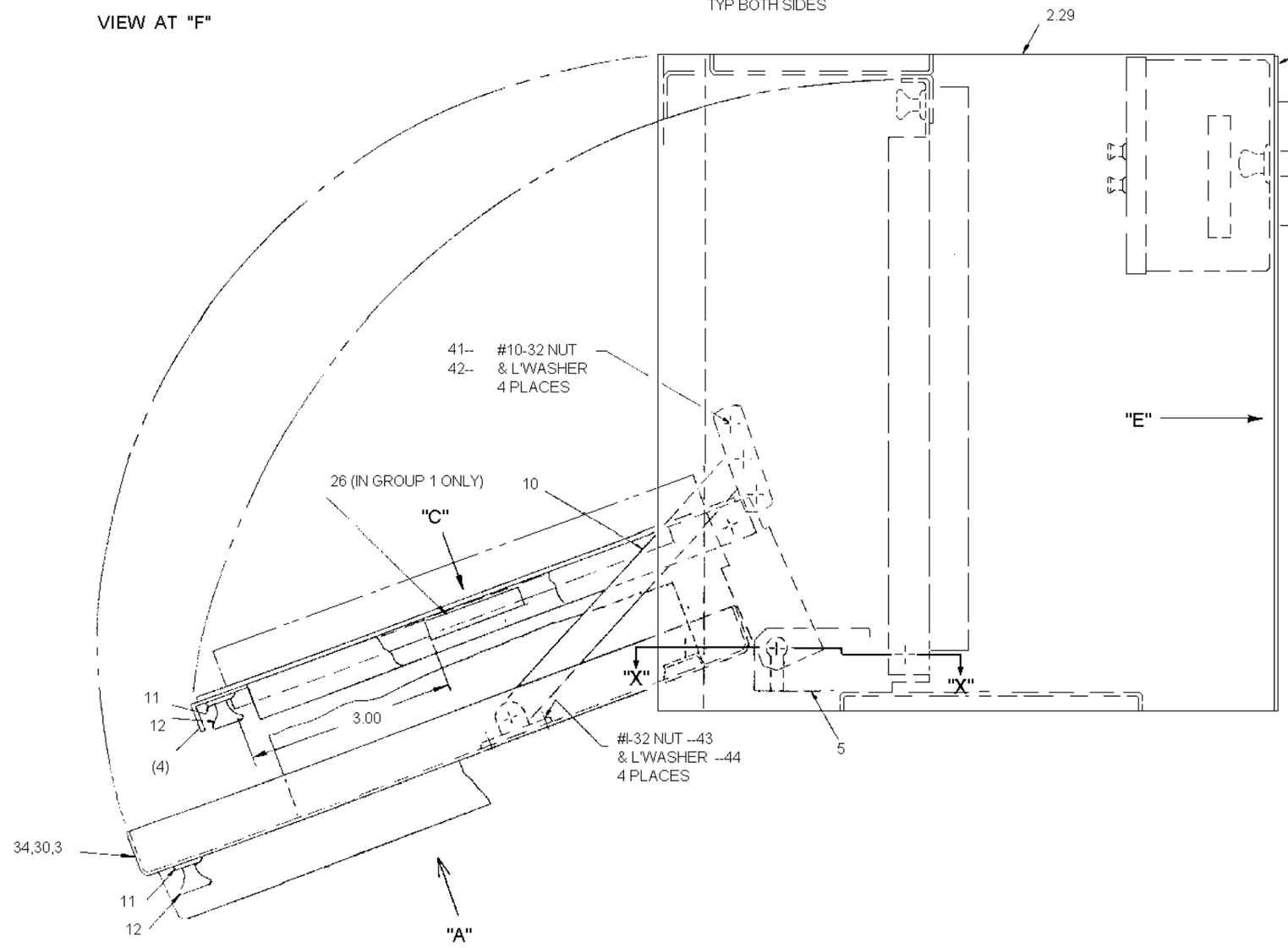


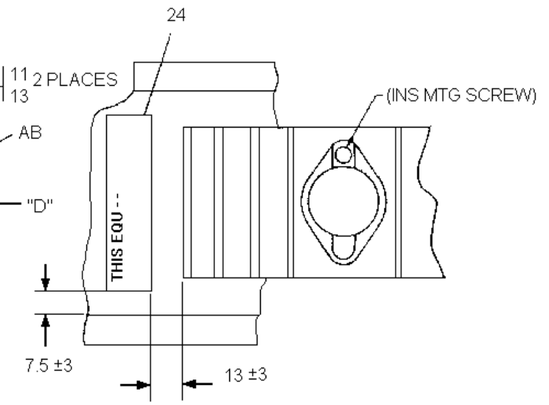
VIEW AT "F"



SECTION "X - X"

TYP BOTH SIDES





VIEW AT "D"

(1) NOTES:

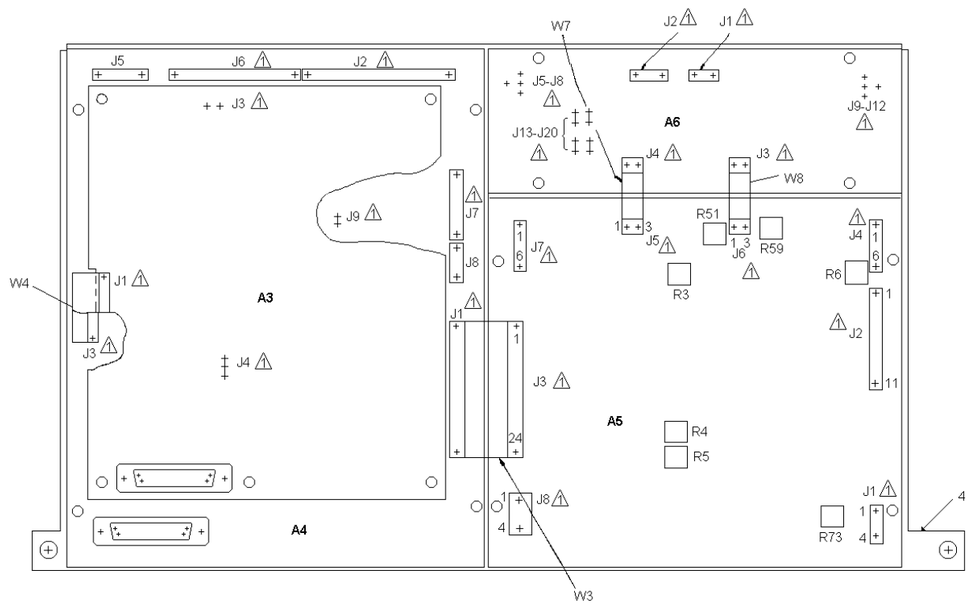
⚠1 APPLY LUBRICATION TO FOLLOWING CONNECTORS PER PROCESS PG4-EA122P1.

A1-J2, J6-J41
A2-J1
A3-J1, J3, J4
A4-J1, J2, J3, J5-J9
A5-J1-J8
A6-J1-J4, (J5-J20 INDIVIDUAL PINS)

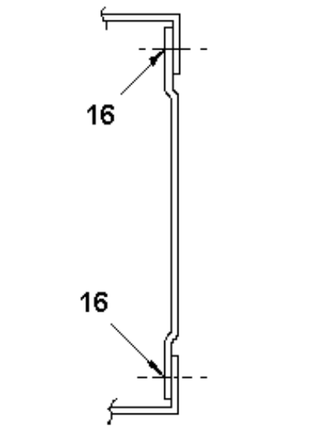
2. ATTENUATOR KIT (ITEM 27) TO BE PACKAGED AND SHIPPED WITH T.A.U. ASSEMBLY.

TAU ASSEMBLY
19D901365G1/G2

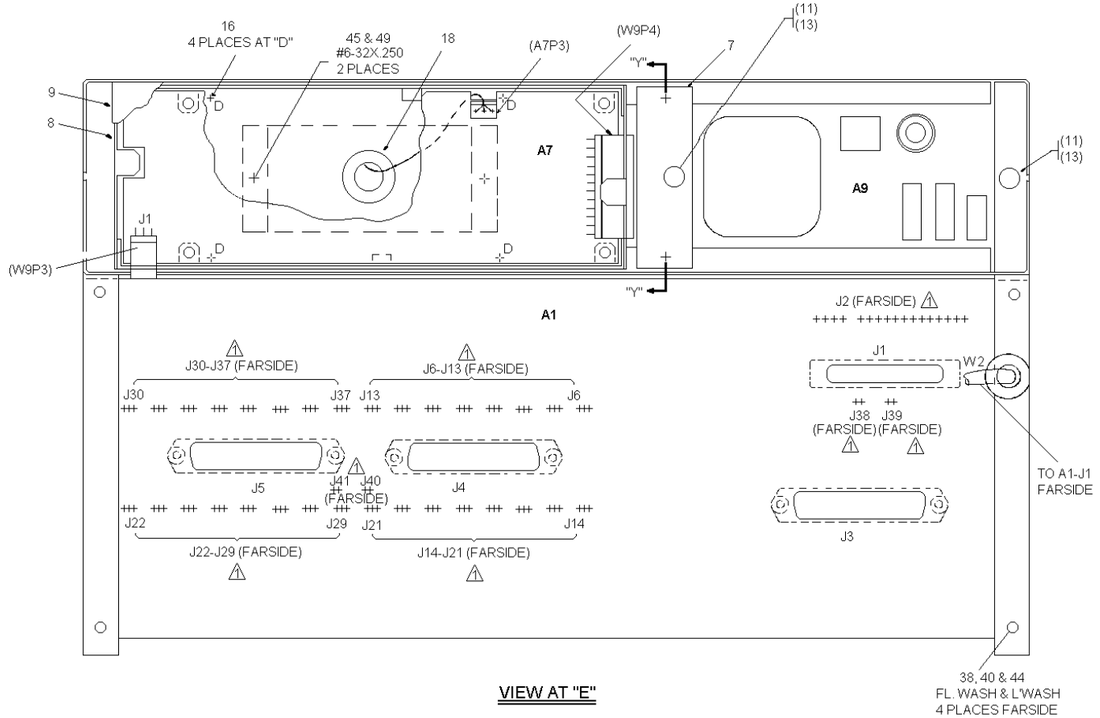
(19D901365, Sh. 1, Rev. 10)



VIEW AT "C"



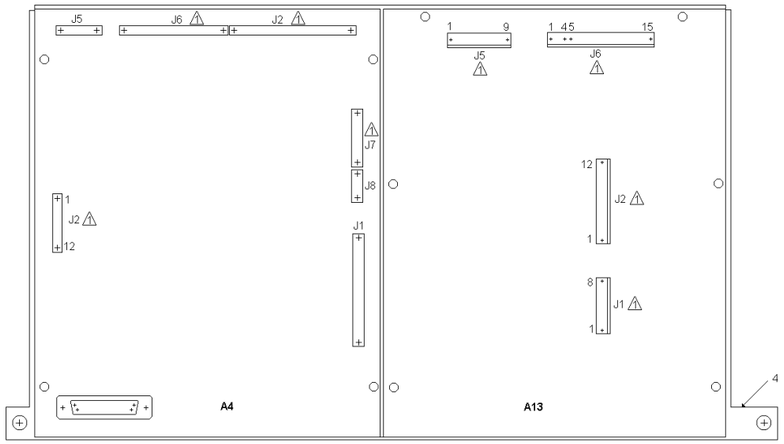
SECTION "Y - Y"



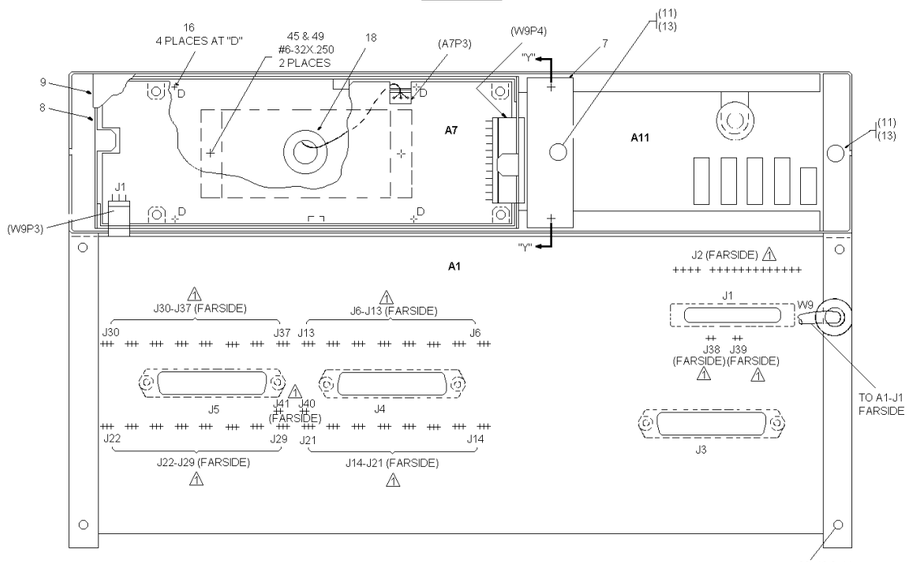
VIEW AT "E"

TAU ASSEMBLY
19D901365G1

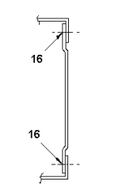
(19D901365, Sh. 2, Rev. 3)



VIEW AT "C"



VIEW AT "E"

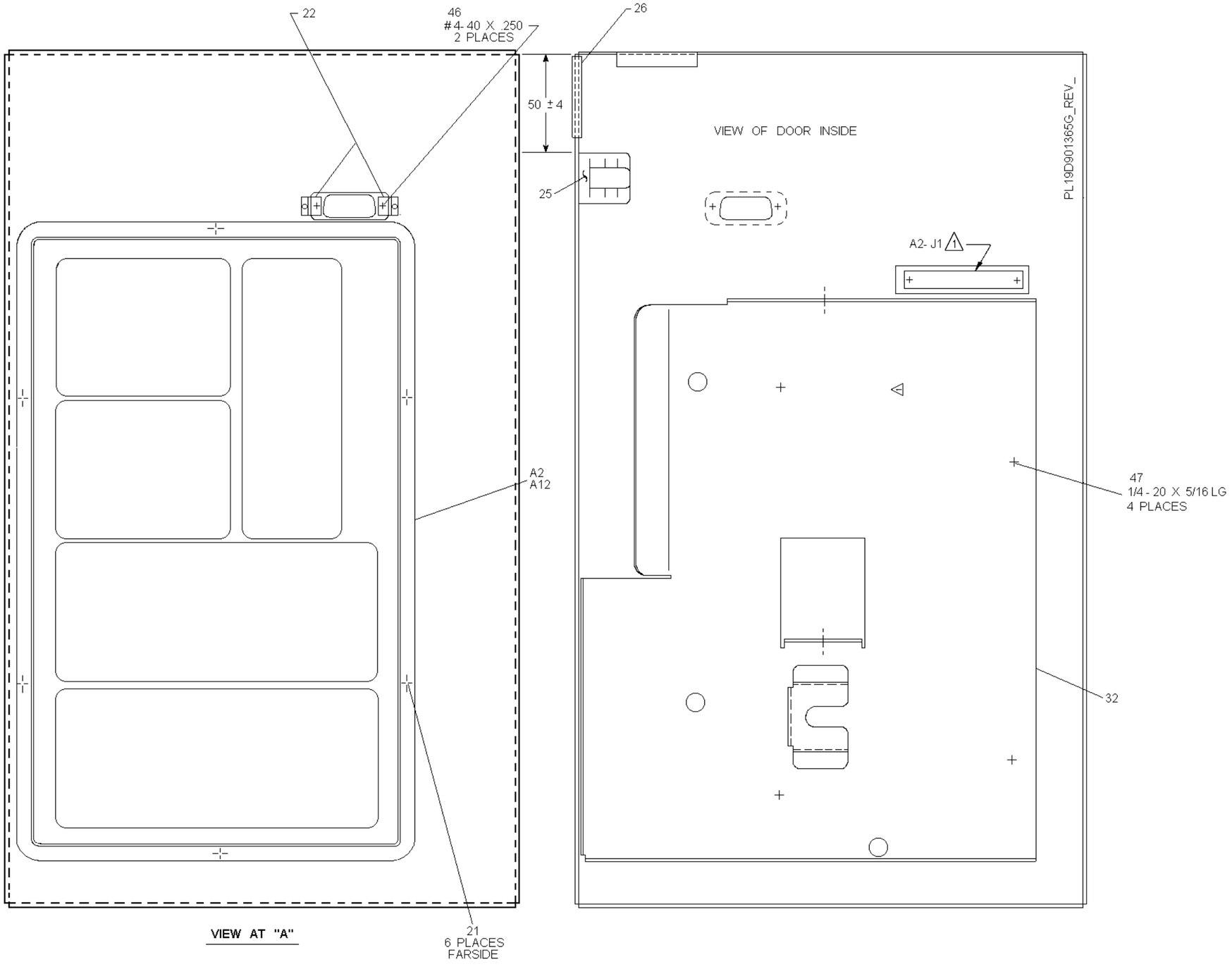


SECTION "Y - Y"

(28) EXCEPT AS SHOWN SAME AS PART 1
NOTES:
1. APPLY LUBRICATION TO FOLLOWING CONNECTORS PER PROCESS P6A-EA122P1.
   A1-J2, J6-J41
   A4-J2, J3, J6, J7
   A12-J1
   A13-J1, J2, J5, J6

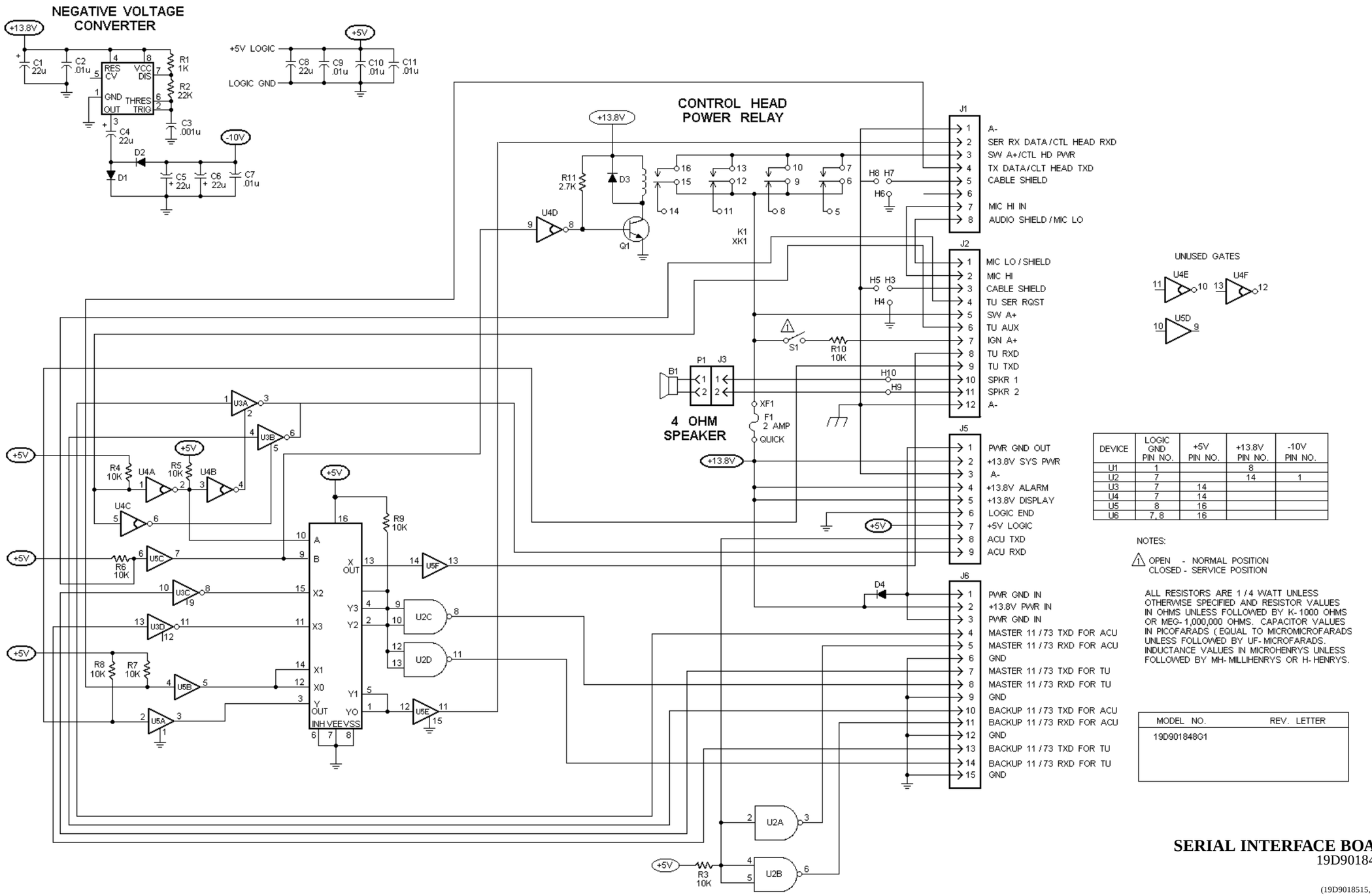
TAU ASSEMBLY
19D901365G2

(19D901365, Sh. 2A, Rev. 3)



TAU ASSEMBLY
19D901365G1/G2

(19D901365, Sh. 3, Rev. 7)



DEVICE	LOGIC GND PIN NO.	+5V PIN NO.	+13.8V PIN NO.	-10V PIN NO.
U1	1		8	
U2	7		14	1
U3	7	14		
U4	7	14		
U5	8	16		
U6	7, 8	16		

NOTES:

1. OPEN - NORMAL POSITION
   CLOSED - SERVICE POSITION

ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY K- 1000 OHMS OR MEG- 1,000,000 OHMS. CAPACITOR VALUES IN PICOFARADS (EQUAL TO MICROMICROFARADS UNLESS FOLLOWED BY UF- MICROFARADS. INDUCTANCE VALUES IN MICROHENRYS UNLESS FOLLOWED BY MH- MILLIHENRYS OR H- HENRYS.

MODEL NO.	REV. LETTER
19D901848G1	

SERIAL INTERFACE BOARD
19D901848G1

(19D9018515, Rev. 1,)