

**MAINTENANCE MANUAL  
PCS REAR ASSEMBLIES  
19D902175G1 (136-153 MHz)  
19D902175G2 (150-174 MHz)**

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**DESCRIPTION**

The PCS Portable Radio Rear Assemblies 19D902175G1 and G2 provide metal housings for RF Boards 19D438222G1 (136-153 MHz) and 19D438222G3 (150-174) respectively. The RF boards are the same except for certain frequency sensitive elements.

The RF boards consist of the following circuits:

- A frequency synthesizer for generating the transmit carrier frequency and the receive circuit first mixer injection frequency.
- The transmit circuit, receive circuit and TX/RX switch.
- A voltage regulator and low battery switch.

Refer to Figure 1 for a block diagram of the synthesizer circuit. Refer to Figure 2 for a transmit and receive circuit block diagram. Transmit circuit adjustments for frequency and power are accessible from the top side of the board, as are IF alignment, second oscillator and quadrature detector adjustments for the receiver circuit. Chip components on the bottom of the board provide optimum RF performance.

Selected use of sealed modules permits small board size as well as RF and mechanical protection for sensitive circuitry. Modules are NOT repairable and must be replaced if they are determined to be damaged. A single friction fit shield provides RF shielding.

## CIRCUIT ANALYSIS

### SYNTHESIZER CIRCUIT

The frequency synthesizer circuit generates all transmit and receive RF frequencies for the PCS Personal Radio. This circuit uses a phase-locked Voltage Controlled Oscillator (VCO) operating on the actual transmitter frequency (136-153 or 150-174 MHz) during transmit and 45 MHz above the actual receive frequency during receive. The synthesizer output signal is generated directly by VCO module U204 and fed through a low pass filter to a LO buffer, a PA buffer and a prescaler buffer.

The synthesizer frequency output is controlled by a microprocessor on the Audio Logic Board. Frequency stability is maintained by a temperature compensated crystal controlled oscillator (TCXO) module. The oscillator has a stability of 5 PPM over the temperature range of -30C to 60C and determines the overall frequency stability of the radio.

The VCO output is also buffered by transistor Q201 to feed divide by 64/65 dual modulus prescaler U205. The prescaler feeds the Fin input of Phase-Lock-Loop (PLL) chip U201. Within U201, the prescaler signal is further divided down to 5 KHz to be compared with a reference signal. This reference signal is derived from 12.8 MHz TCXO module U203. The PLL chip, U201, divides the 12.8 MHz TCXO down to the 5 KHz reference frequency. Divider circuits in U201 are programmed by three inputs from the Audio/Logic Board. These are **SYN ENABLE**, **SYN DATA** and **SYN CLOCK** lines. A **LOCK DETECT** line from the PLL chip to the audio board microprocessor for processing to prevent transmissions when the synthesizer is unlocked. A blinking **BAT** flag is displayed on the LCD and a pulsed beep will be sounded if this condition occurs.

Audio modulation from the Audio/Logic Board is applied to loop filter circuit board A201 in the synthesizer circuit. The audio is summed with the unfiltered control voltage and fed to operational amplifier U1 on the loop filter Board. Amplifier U1 is biased to produce gain variation with different control voltages. When the control voltage is below 1.7 volts, both diodes in diode package D1 are biased off. The operational amplifier gain is then one. As the control voltage rises above approximately 1.7 volts, one of the diodes (D1) is forward biased. This increases the operational amplifier gain to approximately 1.2. Further increases in the control voltage above approximately 2.5 volts turns both diode paths on, thus increasing the gain to about 1.4. Gain variation verses control voltage compensates for decreasing VCO gain and keeps the VCO gain constant at higher control voltages. The net effect of this is to linearize the loop response across the frequency

band to maintain relatively constant audio modulation and constant digital Channel Guard waveshape.

The synthesizer enable line also drives bilateral switches U2A and U2B on the loop filter board. The pulse applied to these gates, when channel changes occur, turns the gates on which shorts out resistors R11 and R12. This allows rapid channel acquisition.

At low control voltages, below approximately 0.9 volts, operational amplifier U1B is enabled by the pulse on the synthesizer enable line. This enables transistor Q1 for the duration of the channel change pulse. Transistor Q1 acts as a current sink for operational amplifier U1A which speeds up the slow rate on U1A at low voltages.

### TRANSMIT CIRCUIT

The transmit circuit consists of a transmit buffer amplifier, a 7-watt power amplifier (U101), a Power Control circuit (A101), a low pass filter circuit and a Tx/Rx switch. Transistors Q102 through Q105 switch power to the TX stages and drives the Disable Line of the Power Control Module.

#### Tx Buffer

Transmit buffer transistor Q101 is driven by the synthesizer VCO output at a level of approximately 0 dBm. Amplifier transistor Q101, in turn, drives power module U101 at approximately +3 dBm. DC power is applied to the buffer only in the transmit mode and is regulated to provide constant drive with decreasing battery voltage.

#### Power Module

Power module U101 is a three-stage broadband power amplifier with internal matching. This module mounts to the rear casting for heat sinking. Output power is controlled by varying the supply voltage to stage two of the module. Stage one and bias for stage two are supplied with the same regulated voltage as the transmit buffer. The final PA stage is supplied by the battery voltage in order to obtain maximum power. The final stage power feed is through inductor L103. The d.c. voltage drop across this coil provides the sense voltage for power control.

### Power Control Board

The power control circuitry, located on circuit board A101, has the task of sensing the d.c. drop across L103 and producing an output d.c. voltage to control stage two of the PA module. This feedback system holds the current to stage three of the PA module essentially constant as frequency, battery voltage, temperature and load varies. The output current level and output power are set by power adjusting potentiometer R119, located on the RF Board. A lower power level may be set by adjusting potentiometer R11, located on the Power Control Board. Transistor Q2 on the power control board must be turned ON to enable the R11 path. This transistor is in turn controlled by the microprocessor on the Audio/Logic Board to control high or low power operation.

The input voltages to the power control module are on Pins 7 and 8. These voltages are divided down by precision resistors to set input voltages to operational amplifier U1. The voltage on the positive terminal of U1 may be adjusted above and below the divider voltage on the negative terminal of U1. When the positive and negative terminals are at equal potentials, the output of U1 is about 5 volts (depending on battery voltage). As the voltage on the positive terminal is adjusted by potentiometer R11, the output of U1 moves higher or lower in potential by about 60 times the  $\Delta$  Vin. This output is buffered by emitter follower transistor Q3. The output voltage on Pin 2 is set by the resistor ratio  $R7+R8/R7$ . Current is supplied at this output mode by external transistor Q106.

#### Low Pass Filter

A six element low pass filter is provided to prevent excessive transmitter harmonics from being transmitted. This filter in conjunction with the matching circuitry in the PA module limits the conducted harmonic energy to less than -30 dBm.

#### Tx/Rx Switch

The Tx/Rx Switch consists of series **PIN** diode D101 and shunt **PIN** diode D102. Both diodes are off during receive and are therefore essentially open. This isolates the transmit circuit from the receive circuit while in the receive mode. During transmit, regulated voltage is switched to inductor L105. This produces a d.c. current through both D101 and D102, which transforms both diodes into RF shorts. This allows the PA output power to be conducted to the radio antenna. The RF short produced by D102 protects

the receiver but is still essentially an open to the transmitter. This is true because inductor L106 and part of capacitor C116 form a parallel resonant circuit across the transmit output.

#### Tx Switches

The transmit circuit is enabled by the **DPTT** line from the Audio/Logic Board. When the PTT button is activated, the **DPTT** line is pulled high. This turns transistor Q102 on and allows transistors Q103, Q104 and Q105 to conduct. The voltage on the emitter of transistor Q104 is approximately 0.7 volts (**VBE + VSAT**) below the regulated 5.4 Volts. The voltage at the collector of transistor Q105 is set by the  $(R117 + R118)/R117$  resistor ratio. This boosts the output voltage back to about 5.4 volts while allowing Q105 to supply the relatively high currents needed for the Tx Buffer, the PA module and the **PIN** diode switch.

The collector of transistor Q102 is also used to drive transmit disable transistor Q1 located on the power control module. When in the Rx state, the base of Q1 is biased on by a high voltage level at the collector of Q102. This in turn keeps the positive terminal of U1 sufficiently low to drive the output of U1 low enough to bias Q3 off. When Q102 is turned on by the **DPTT** line, transistor Q1 is biased off. This allows the normal Tx operation previously described.

### RECEIVE CIRCUIT

The dual conversion receive circuit consists of a receiver front end, a 45 MHz first IF and a 455 kHz second IF with an FM detector. All audio processing and squelch functions are accomplished on the Audio/Logic Board.

#### Front End

RF is coupled from antenna jack J1 to the RF Board through antenna clip connector J101. The receive signal is then conducted through the Tx low pass filter to receive preselector filter Z401. This is a fixed tuned 3-pole band pass filter covering the 136 to 153 or 150 to 174 MHz bands. Its output is matched to the input of RF amplifier transistor Q401. A fixed tuned 2-pole output filter is connected between the RF amplifier and double balanced mixer Z402. About 10 dB of RF gain is provided to the mixer input. The Local Oscillator (LO) port of the mixer (Pin 1) is driven by LO buffer transistor Q450. The filtered synthesizer output drives this buffer. The output of Q450 drives a 2-pole filter which couples the drive to the mixer at about +4 dBm.

**45 MHz IF**

The mixer output is connected to the Source of common Gate Field Effect Transistor (FET) Q501. This stage provides a low impedance input to match the mixer and a high impedance output to drive the 45 MHz 4-pole crystal filter. The crystal filter output is amplified by bipolar device transistor Q502. This IF amplifier output drives the Second Mixer circuit in Mixer/Limiter/FM Detector module U501. Crystal Y101 is an external crystal operating a 45.455 MHz. This crystal when coupled to the internal circuitry forms the second LO for the second mixer circuit. The frequency of the second LO is adjusted with inductor L505. The second mixer output is a 455 kHz IF and is filtered by a 4-pole ceramic filter. This output is further amplified and limited by U501. A quadrature detector circuit provides an audio output from U501. The quadrature detector coil is L506. The audio output is pre-filtered and connected to the Audio/Logic Board as VOL SQ HI.

**5.4 Volt Regulator**

The 5.4 volt regulator circuit supplies a regulated 5.4 volts to all circuits requiring a stable reference voltage. This regulated voltage is generated by voltage reference diode U801 and transistors Q801, Q802 and Q803. Diode U801 provides 2.5 volts which is stable with both temperature and

battery voltage. The 2.5 volt reference is fed to the base of Q802. Transistors Q802 and Q803 form a differential amplifier while Q801 acts as a pass transistor. The regulated 5.4 volts output on the collector of Q801 is divided by voltage divider resistors R805 and R806 to apply 2.5 volts to the base of transistor Q803. With this voltage on the base of Q803 the differential amplifier is balanced.

**Battery Indicator**

Transistor Q804 senses the battery voltage and compares it to the regulated 5.4 volts on the emitter. When the battery voltage drops to approximately 6.3 volts, Q804 is sufficiently on to produce about 0.4 volts on the battery indicator output (P801-1). This voltage is fed to the audio/logic board to drive an inverter which toggles a microprocessor port to provide a low battery indication.

Another effect at low battery voltage is produced by the voltage on the collector of Q804 driving Pin 6 of power control module U1. A slight increase of this voltage on the negative terminal of U1 causes the output of U1 to drop and the control voltage to be reduced. The final result is a slight drop in RF power output. Consequently, as the end of battery is approached, the RF power is throttled back. This gives the user additional transmit time before total loss of power due to low battery.

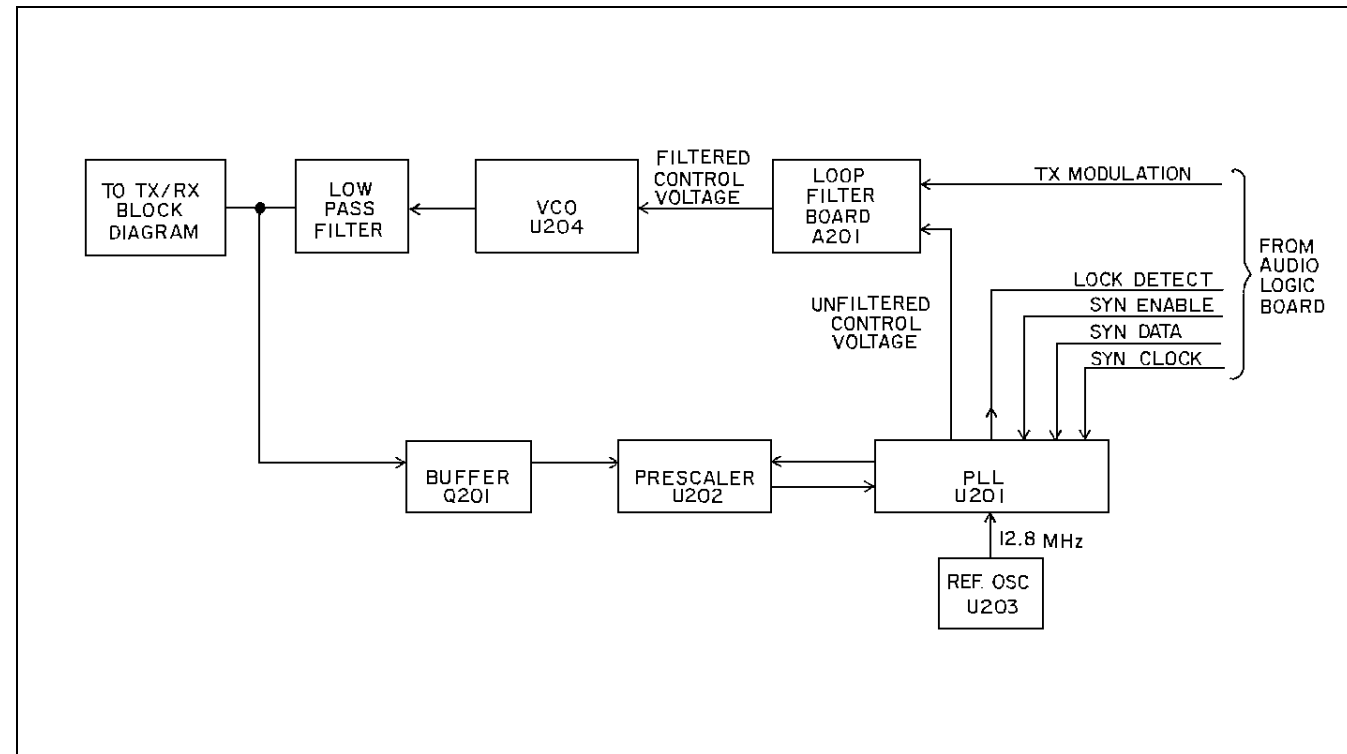


Figure 1 - Synthesizer Circuit

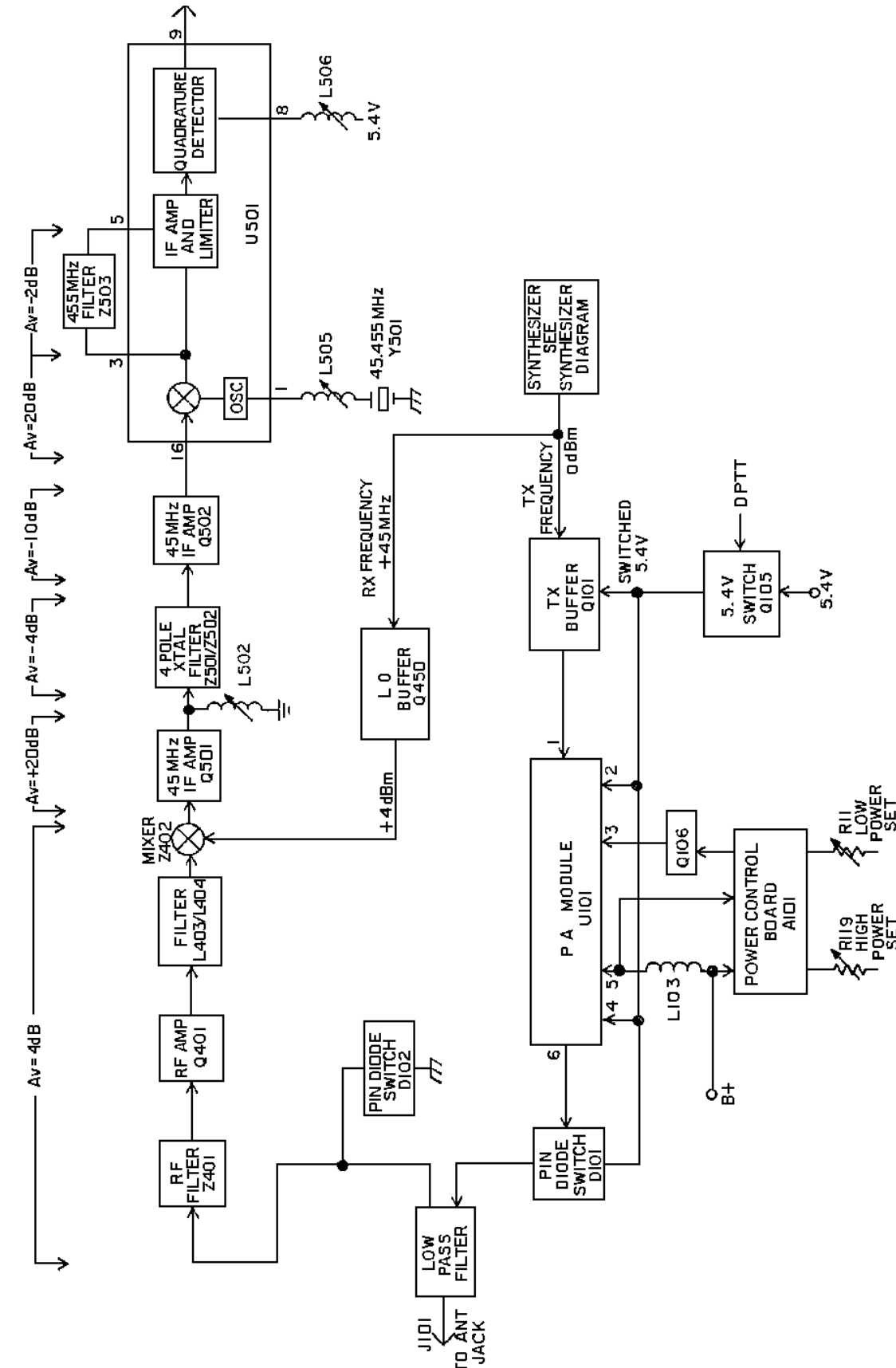
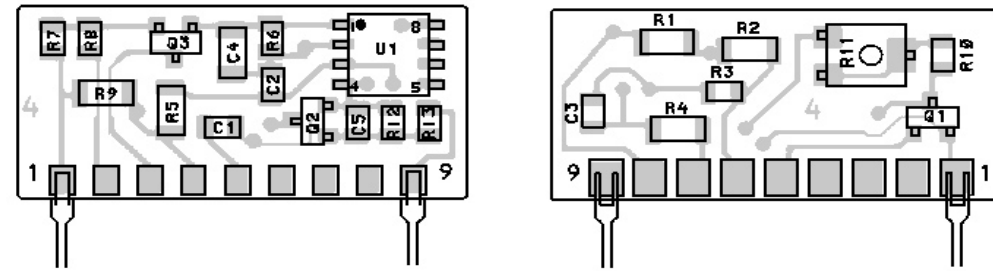


Figure 2 - Transmit And Receive Circuit

POWER CONTROL BOARD A101

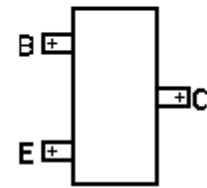
19B801519G1



COMPONENT SIDE

SOLDER SIDE

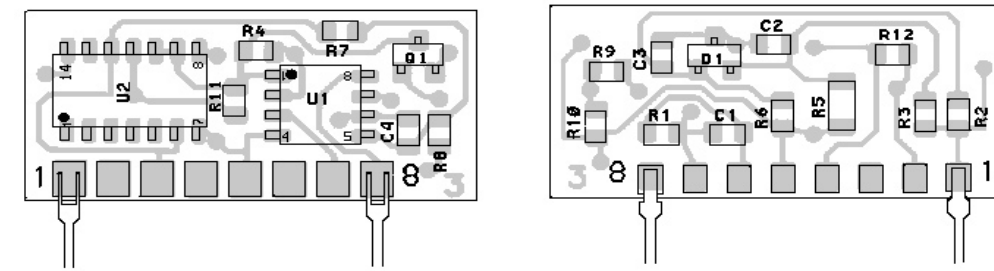
LEAD IDENTIFICATION FOR  
Q1, Q2, & Q3  
(TOP VIEW)



(19B801519, Sh. 1, Rev. 3)  
(19C851653, Component Side, Rev. 4)  
(19C851653, Solder Side, Rev. 4)

LOOP FILTER BOARD A201

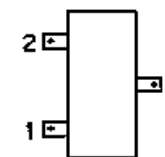
19C851646G1



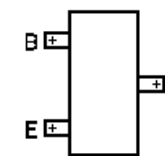
COMPONENT SIDE

SOLDER SIDE

LEAD IDENTIFICATION FOR  
D1  
(TOP VIEW)

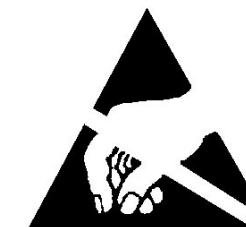


LEAD IDENTIFICATION FOR  
Q1  
(TOP VIEW)

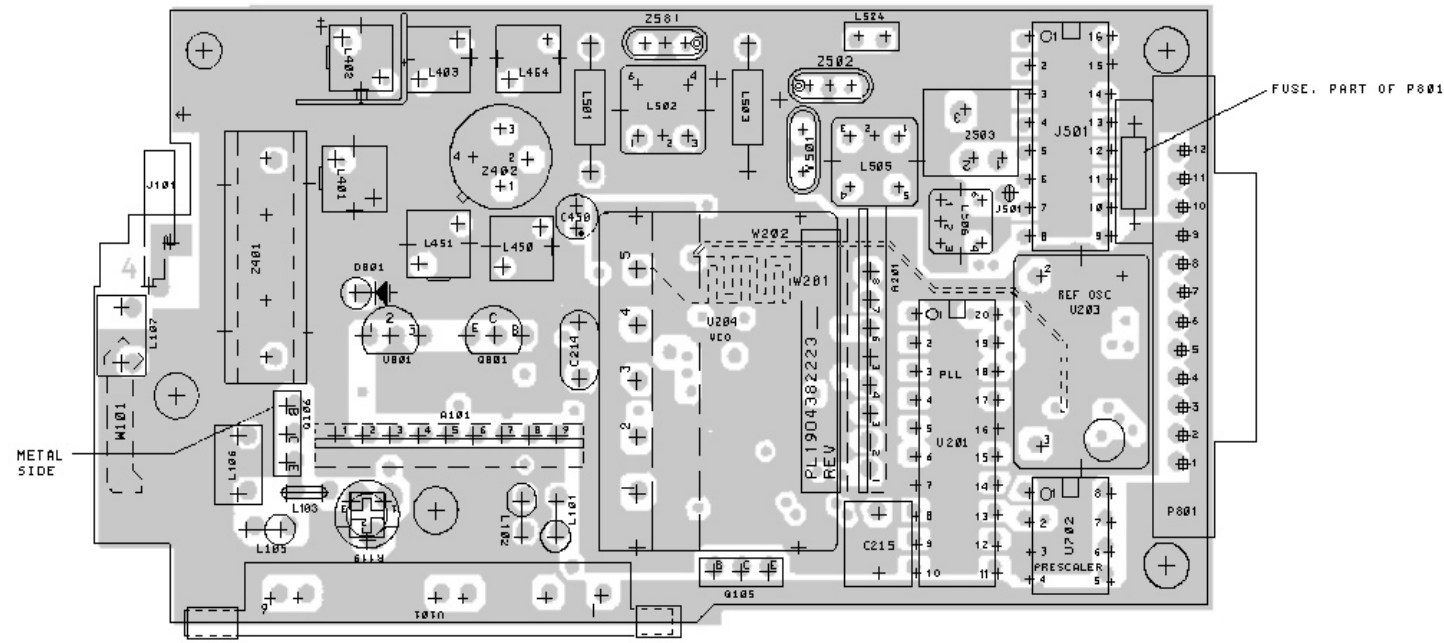


(19C851646, Sh. 1, Rev. 2)  
(19C851647, Component Side, Rev. 3)  
(19C851647, Solder Side, Rev. 3)

R  
E  
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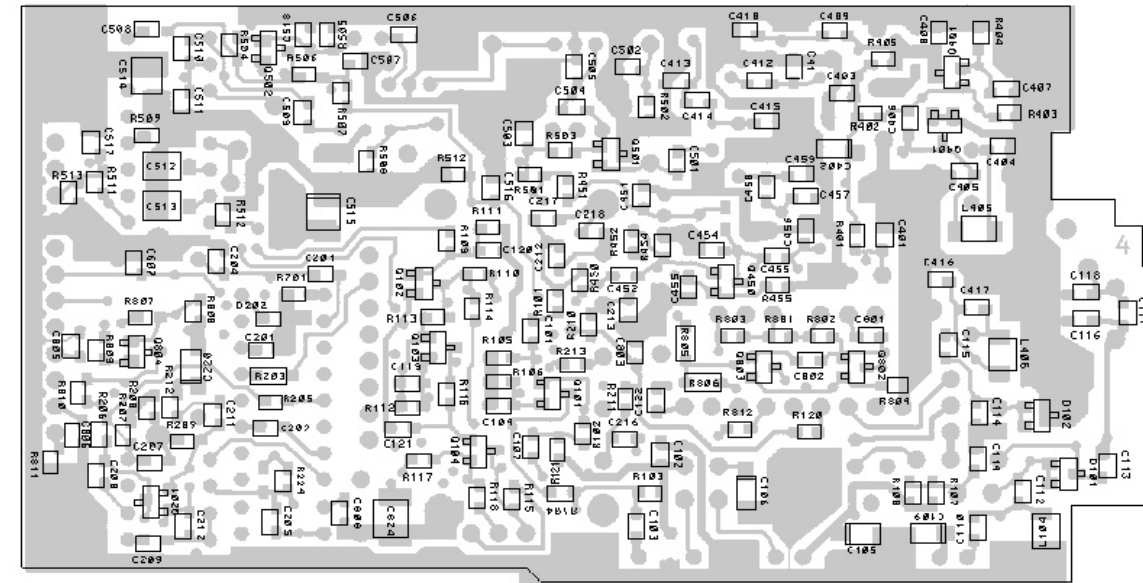


**CAUTION**  
OBSERVE PRECAUTIONS  
FOR HANDLING  
ELECTROSTATIC  
SENSITIVE  
DEVICES



COMPLEMENT SIDE

(19D438222, Sh.3, Rev. 3)  
 (19D902627, First Layer, Rev. 4)  
 (19D902627, Fourth Layer, Rev. 4)

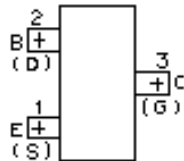


SOLDER SIDE

(19D438222, Sh. 4, Rev. 5)  
 (19D902627, Fourth Layer, Rev. 4)

LEAD IDENTIFICATION FOR (SOT) TRANSISTORS

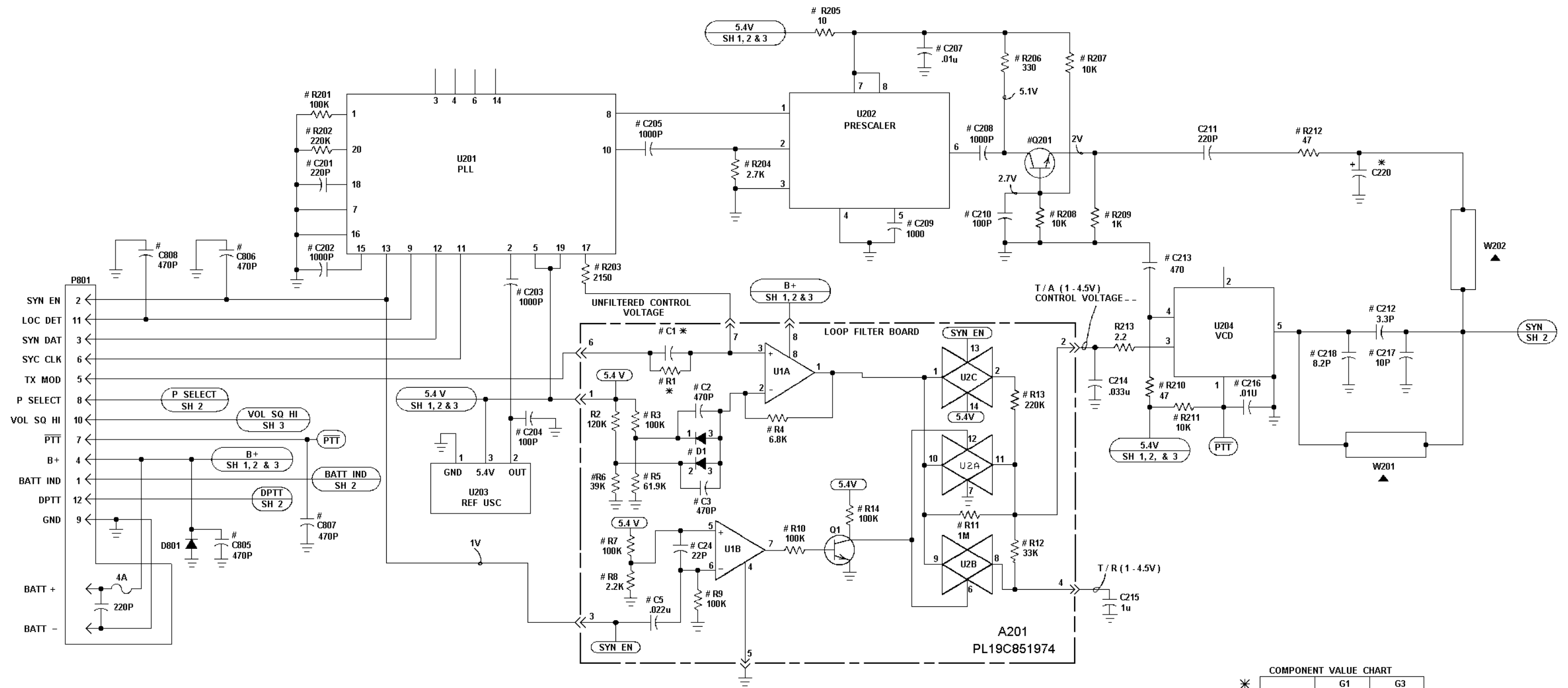
( TOP VIEW )



RF BOARDS  
 19D438222G1 & G3



**CAUTION**  
 OBSERVE PRECAUTIONS  
 FOR HANDLING  
**ELECTROSTATIC  
 SENSITIVE  
 DEVICES**



R  
E  
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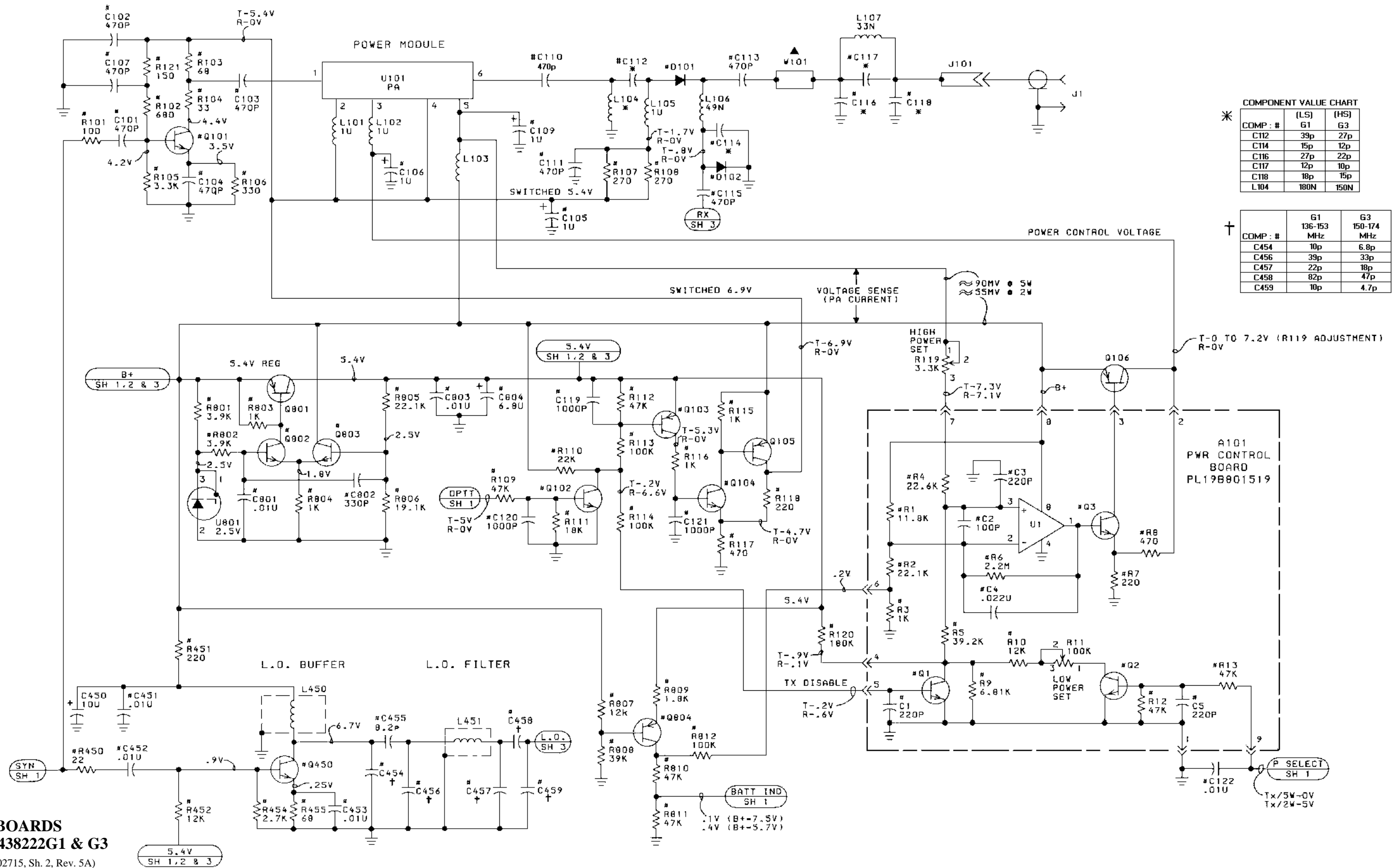
MODEL NO.	REV. LETTER
PL19D438222G1	D
PL19D438222G3	E

- NOTES:
1. ALL RESISTORS ARE .1 WATT UNLESS OTHERWISE SPECIFIED  
RESISTOR VALUES IN U UNLESS FOLLOWED BY MULTIPLIER K OR M.  
CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER U, N OR P.  
INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER M OR U.
  2. # INDICATES CHIP COMPONENTS
  3. ▲ PART OF PWB.
  4. ALL D.C. VOLTAGES ARE TAKEN AT B+ - 7.5V.

\* COMPONENT VALUE CHART

COMP: #	G1 136 - 153 MHZ	G3 150 - 174 MHZ
C20	—	1u
C1	.0068u	.022u
R1	160K	82K

**RF BOARDS**  
**19D438222G1 & G3**  
(19D902715, Sh. 1, Rev. 5A)

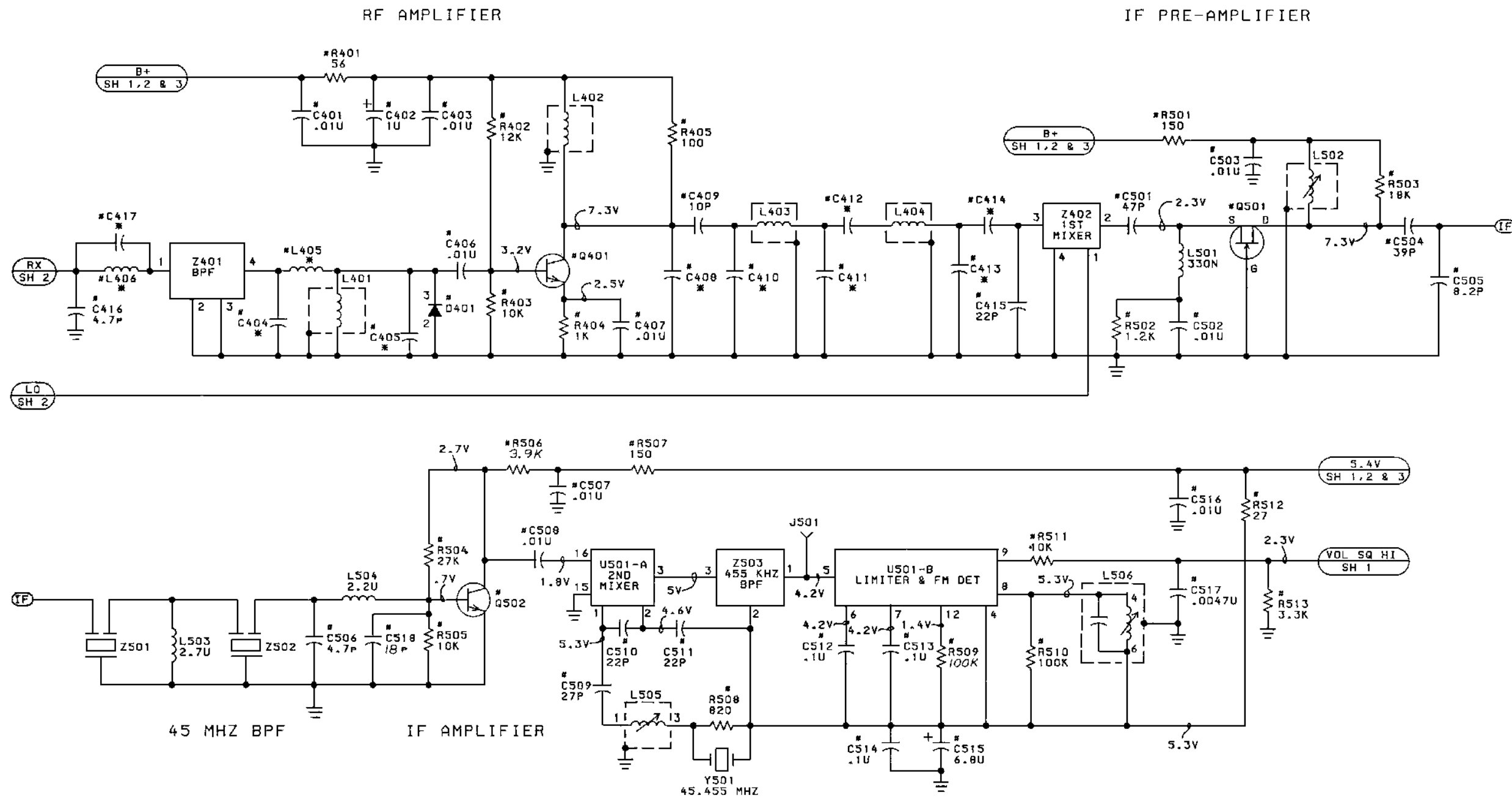


COMPONENT VALUE CHART

COMP: #	(LS)	(HS)
C112	39p	27p
C114	15p	12p
C116	27p	22p
C117	12p	10p
C118	18p	15p
L104	180N	150N

COMP: #	G1	G3
C454	10p	6.8p
C456	39p	33p
C457	22p	18p
C458	82p	47p
C459	10p	4.7p

**RF BOARDS**  
**19D438222G1 & G3**  
 (19D902715, Sh. 2, Rev. 5A)



COMPONENT VALUE CHART

COMP #	61 136-153 MHZ	63 150-174 MHZ
C404	3.9p	8.2p
C405	10p	4.7p
C408	15p	10p
C410	33p	22p
C411	150p	120p
C412	150p	120p
C413	22p	15p
C414	150p	82p
C417	220p	
L405	68n	82n
L406		15n

**RF BOARDS**  
**19D438222G1 & G3**  
 (19D902715, Sh. 3, Rev. 5A)





SYMBOL	PART NUMBER	DESCRIPTION
C410	19A702061P29	Ceramic: 22 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G3).
C411	19A702061P65	Ceramic: 150 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C. (Used in G1).
C411	19A702061P63	Ceramic: 120 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G3).
C412	19A702061P65	Ceramic: 150 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C. (Used in G1).
C412	19A702061P63	Ceramic: 120 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G3).
C413	19A702061P29	Ceramic: 22 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G1).
C413	19A702061P21	Ceramic: 15 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G3).
C414	19A702061P65	Ceramic: 150 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G1).
C414	19A702061P57	Ceramic: 82 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G3).
C415	19A702061P29	Ceramic: 22 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C416	19A702061P9	Ceramic: 4.7 pF ±0.5 pF, 50 VDCW, temp coef 0 ±60 PPM.
C417	19A702061P69	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G1).
C450	19A704879P5	Electrolytic: 10 uF ±20%, 16 VDCW.
C451 thru C453	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C454	19A702061P13	Ceramic: 10 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G1).
C454	19A702061P11	Ceramic: 6.8 pF ±0.5 pF, 50 VDCW, temp coef 0 ±60 PPM. (Used in G3).
C455	19A702061P12	Ceramic: 8.2 pF ±0.5 pF, 50 VDCW, temp coef 0 ±60 PPM.
C456	19A702061P41	Ceramic: 39 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G1).
C456	19A702061P37	Ceramic: 33 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G3).
C457	19A702061P29	Ceramic: 22 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G1).
C457	19A702061P25	Ceramic: 18 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C. (Used in G3).
C458	19A702061P57	Ceramic: 82 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G1).
C458	19A702061P45	Ceramic: 47 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G3).
C459	19A702061P13	Ceramic: 10 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. (Used in G1).
C459	19A702061P9	Ceramic: 4.7 pF ±0.5 pF, 50 VDCW, temp coef 0 ±60 PPM. (Used in G3).
		----- DIODES -----
D401	19A700155P2	Silicon, fwd current: 100 mA, 35 VIP. ----- INDUCTORS -----
L401	19B801493P6	Coil, RF; sim to Toko NE545GNAS-1130.
L402 thru L404	19B801493P3	Coil, RF; sim to Toko NE545GNAS-100127.
L405	19A705470P11	Coil, Fixed: 68 nH; sim to Toko 380NB-68nM. (Used in G1).
L405	19A705470P12	Coil, Fixed: 82 nH; sim to Toko 380NB-82nM. (Used in G3).
L406	19A705470P3	Coil, Fixed: 15 nH; sim to Toko 380NB-15nM. (Used in G3).
L450 and L451	19B801493P3	Coil, RF; sim to Toko NE545GNAS-100127.
		----- TRANSISTORS -----
Q401	19A704708P2	Silicon, NPN; sim to NEC 2SC3356.
Q450	19A704708P2	Silicon, NPN; sim to NEC 2SC3356.

SYMBOL	PART NUMBER	DESCRIPTION
		----- RESISTORS -----
R401	19B801251P560	Metal film: 56 ohms ±5%, 1/10 w.
R402	19B801251P123	Metal film: 12K ohms ±5%, 1/10 w.
R403	19B801251P103	Metal film: 10K ohms ±5%, 1/10 w.
R404	19B801251P102	Metal film: 1K ohms ±5%, 1/10 w.
R405	19B801251P101	Metal film: 100 ohms ±5%, 1/10 w.
R450	19B801251P220	Metal film: 22 ohms ±5%, 1/10 w.
R451	19B801251P221	Metal film: 220 ohms ±5%, 1/10 w.
R452	19B801251P123	Metal film: 12K ohms ±5%, 1/10 w.
R454	19B801251P272	Metal film: 2.7K ohms ±5%, 1/10 w.
R455	19B801251P680	Metal film: 68 ohms ±5%, 1/10 w.
		----- FILTER -----
Z401	19A705424P2	Printed mica; sim to SOSHIN BP136-153A1 (Used in G1).
Z401	19A705424P1	Printed mica; sim to SOSHIN BP150-174A1 (Used in G3).
Z402	19A705423P1	Mixer: Double (balanced); sim to Tele-Tech MT45.
		----- CAPACITORS -----
C501	19A702061P45	Ceramic: 47 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C502 and C503	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C504	19A702061P41	Ceramic: 39 pF ±5%, 50 VDCW, temp coef ±30 PPM.
C505	19A702061P12	Ceramic: 8.2 pF ±0.5 pF, 50 VDCW, temp coef 0 ±60 PPM.
C506	19A702061P9	Ceramic: 4.7 pF ±0.5 pF, 50 VDCW, temp coef 0 ±60 PPM.
C507 and C508	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C509	19A702061P33	Ceramic: 27 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C510 and C511	19A702061P29	Ceramic: 22 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C512 thru C514	19A702052P26	Ceramic: 0.1 uF ±10%, 50 VDCW.
C515	19A705205P14	Tantalum: 6.8 uF, 6 VDCW; sim to Sprague 293D.
C516	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C517	19A702052P10	Ceramic: 4700 pF ±10%, 50 VDCW.
C518	19A702061P25	Ceramic: 18 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
		----- JACKS -----
J501	19A701622P1	Cotter pin. ----- INDUCTORS -----
L501	19A700024P7	Coil, RF: 330 nH ±10%.
L502	19B801413P4	Coil, 39 MHz.
L503	19A700024P18	Coil, RF: 2.7 uH ±10%.
L504	19A705753P17	Coil, Toroidal: 2.2uH ±5%.
L505	19B801413P4	Coil, 39 MHz.
L506	19A703591P1	IF; sim to Toko America P5SVLC-A291EL.
		----- TRANSISTORS -----
Q501	19A702524P3	N-Type, field effect; sim to MMBFJ310.
Q502	19A704708P2	Silicon, NPN; sim to NEC 2SC3356.

SYMBOL	PART NUMBER	DESCRIPTION
		----- RESISTORS -----
R501	19B801251P151	Metal film: 150 ohms ±5%, 1/10 w.
R502	19B801251P122	Metal film: 1.2K ohms ±5%, 1/10 w.
R503	19B801251P183	Metal film: 18K ohms ±5%, 1/10 w.
R504	19B801251P273	Metal film: 27K ohms ±5%, 1/10 w.
R505	19B801251P103	Metal film: 10K ohms ±5%, 1/10 w.
R506	19B801251P392	Metal film: 3.9K ohms ±5%, 1/10 w.
R507	19B801251P151	Metal film: 150 ohms ±5%, 1/10 w.
R508	19B801251P821	Metal film: 820 ohms ±5%, 1/10 w.
R509 and R510	19B801251P104	Metal film: 100K ohms ±5%, 1/10 w.
R511	19B801251P103	Metal film: 10K ohms ±5%, 1/10 w.
R512	19B801251P270	Metal film: 27 ohms ±5%, 1/10 w.
R513	19B801251P332	Metal film: 3.3K ohms ±5%, 1/10 w.
		----- INTEGRATED CIRCUITS -----
U501	19A704619P1	Linear: Osc/Mixer/IF/Det/Amp; sim to MC3361AP. ----- CRYSTALS -----
Y501	19A705376P5	Crystal, Fixed Frequency: 45.455 MHz 10 PPM. ----- FILTER -----
Z501	19A705328P1	Monolithic Crystal: 45.000 MHz; sim to Toyocom 45E2B2.
Z502		Part of Z501.
Z503	19A702171P3	Bandpass: 455 1.5 KHz; sim to Murata CFU455F2. ----- REGULATOR -----
		----- CAPACITORS -----
C801	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C802	19A702061P73	Ceramic: 330 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C803	19A702052P14	Ceramic: 0.01 uF ±10%, 50 VDCW.
C804	19A705205P14	Tantalum: 6.8 uF, 6 VDCW; sim to Sprague 293D.
C805 thru C808	19A702061P77	Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM. ----- DIODES -----
D801	19A116585P1	Silicon, fast recovery, 600 mA, 50 PIV. ----- PLUGS -----
P801	19C851673P2	Connector. ----- TRANSISTORS -----
Q801	19A700026P2	Silicon, PNP; sim to BC369.
Q802 and Q803	19A700076P2	Silicon, NPN; sim to MMBT3904, low profile.
Q804	19A700059P2	Silicon, PNP; sim to MMBT3906, low profile. ----- RESISTORS -----
R801 and R802	19B801251P392	Metal film: 3.9K ohms ±5%, 1/10 w.
R803 and R804	19B801251P102	Metal film: 1K ohms ±5%, 1/10 w.
R805	19A702931P334	Metal film: 22.1K ohms ±1%, 200 VDCW, 1/8 w.
R806	19A702931P328	Metal film: 19.1K ohms ±1%, 200 VDCW, 1/8 w.
R807	19B801251P123	Metal film: 12K ohms ±5%, 1/10 w.
R808	19B801251P393	Metal film: 39K ohms ±5%, 1/10 w.
R809	19B801251P182	Metal film: 1.8K ohms ±5%, 1/10 w.

SYMBOL	PART NUMBER	DESCRIPTION
R810 and R811	19B801251P473	Metal film: 47K ohms ±5%, 1/10 w.
R812	19B801251P104	Metal film: 100K ohms ±5%, 1/10 w. ----- INTEGRATED CIRCUITS -----
U801	19A702939P2	Linear: Adjustable Shunt Regulator; sim to TL431CLP. ----- MISCELLANEOUS -----
	19D902174G1	Cover.
	19A702364P304	Screw, Machine.
	19B801572G1	Shield, RF.
	19A705732P329	Screw, Machine.
	19A705732P333	Screw, Machine.
	19B801492P2	Clip.
	19A705883P3	Crystal cushion.
	19B801657P1	Insulating plate.
	19B801655P1	Shield.

R  
E  
A  
R  
A  
S  
S  
E  
M  
B  
L  
Y

**PRODUCTION CHANGES**

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

**REV. A - RF BOARD 19D438222G1**

**REV. A - RF BOARD 19D438222G3**

To improve selectivity, changed IF bandpass filter Z503. To improve low level frequency stability, removed capacitor C206. To allow scan operation, changed loop filter module A201. Old part numbers were:

Z503 - 19A702171P1, Filter, Bandpass.

C206 - 19A702061P69, Ceramic: 220 pF ±5%, 50 VDCW temp coef 0 ±30 PPM,

A201 - 19C851646, Loop Filter Module.

**REV. B - RF BOARD 19D438222G3**

To improve radio performance changed C110, C112, L104 and U204. Old part numbers were:

C110 - 19A702061P77, Ceramic: 470 pF ±5%, 50 VDCW temp coef 0 ±30 PPM.

C112 - 19A702061P33, Ceramic: 33 pF 5±%, 50 VDCW temp coef 0 ±30 PPM.

L104 - 19A700024P2, Coil, RF; 120 nH.

U204 - 19A705628P2, Voltage Controlled Oscillator.

**REV. C - RF BOARD 19D438222G1 & G3**

To improve receiver adjacent channel selectivity, improve a receiver spur and resolve an out of lock condition the following were changed.

L104 changed to a surface mount component.

R213 was 1k ohms (19B801251P102).

C219 deleted.

C220 added (19A705205P2).

C808 added (19A702061P77).

**REV. D - RF BOARD 19D438222G1 & G3**

To improve impedance matching.

C110 in G3 was 22 pF (19A702236P34).

C112 in G3 was 22 pF (19A702236P34).

C112 in G1 was 27 pF (19A702061P33).

L103 was a coil (19A700024P1).

L104 was 56 NH (19A705470P10).

**REV. E - RF BOARD 19D438222G3**

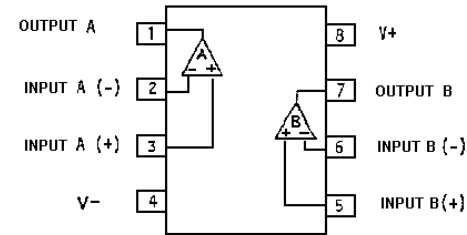
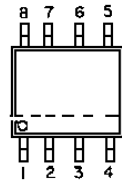
To improve frequency response.

C214 was 0.022uF (T644ACP322K).

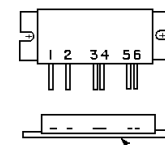
C1 was 0.01uF (19A702052P114).

R1 was 100K ohms (19B801251P104).

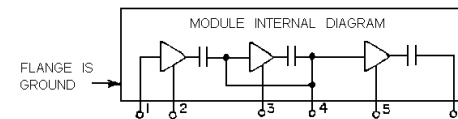
**OPERATIONAL AMPLIFIER U1  
19A702293P2**



**POWER MODULE U101  
19A705418P2**

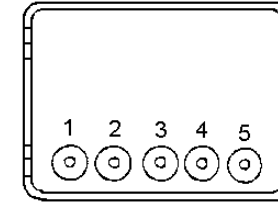


PIN	FUNCTION
1	RF INPUT
2	VS1 + DC
3	VS CONTROL+DC
4	VBIAS + DC
5	VS2 + DC
6	RF OUTPUT



FLANGE TO BE FLAT WITHIN +0.025 CONCAVE -0

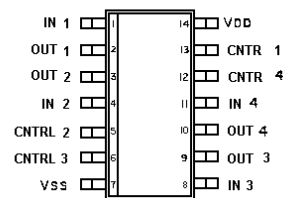
**VCO U204  
19A705628P2**



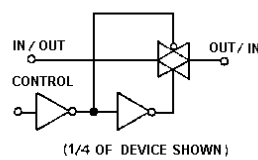
PIN	FUNCTION
1	TX / RX
2	N.C.
3	CONTROL
4	B+
5	OUTPUT

**BILATERAL SWITCH U2  
19A702705P1**

PIN CONFIGURATION

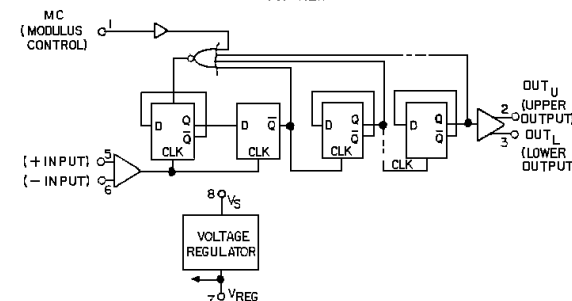
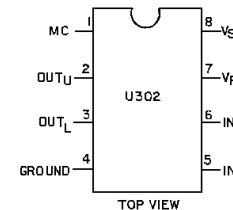


LOGIC DIAGRAM

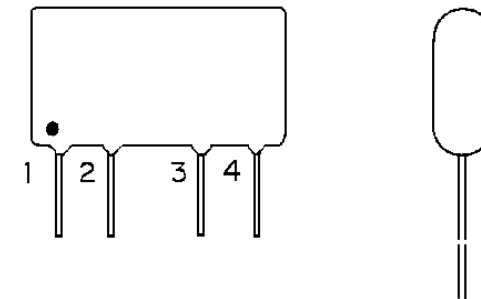


CONTROL	SWITCH
0	OFF
1	ON

**PRESCALER MODULE U202  
19A703091P1**



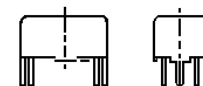
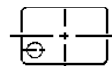
**BANDPASS FILTER Z401  
19A705424P1**



PIN CONNECTIONS:

- 1 - INPUT
- 4 - OUTPUT
- 2,3 - GROUND

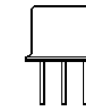
**REFERENCE OSCILLATOR U203  
19B801351P8**



PIN CONNECTIONS

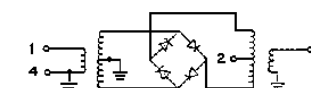
- 1. COMMON AND CASE
- 2. OUTPUT
- 3.+ V<sub>cc</sub>

**FIRST MIXER Z402  
19A705423P1**



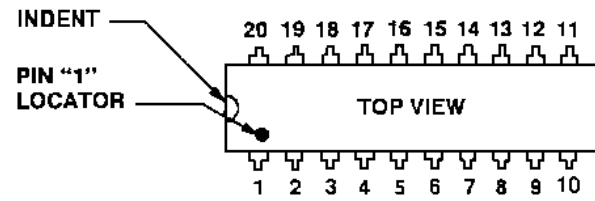
PIN CONNECTIONS

LOCAL OSC.	
RF	1
IF	2
GROUND & CASE	4



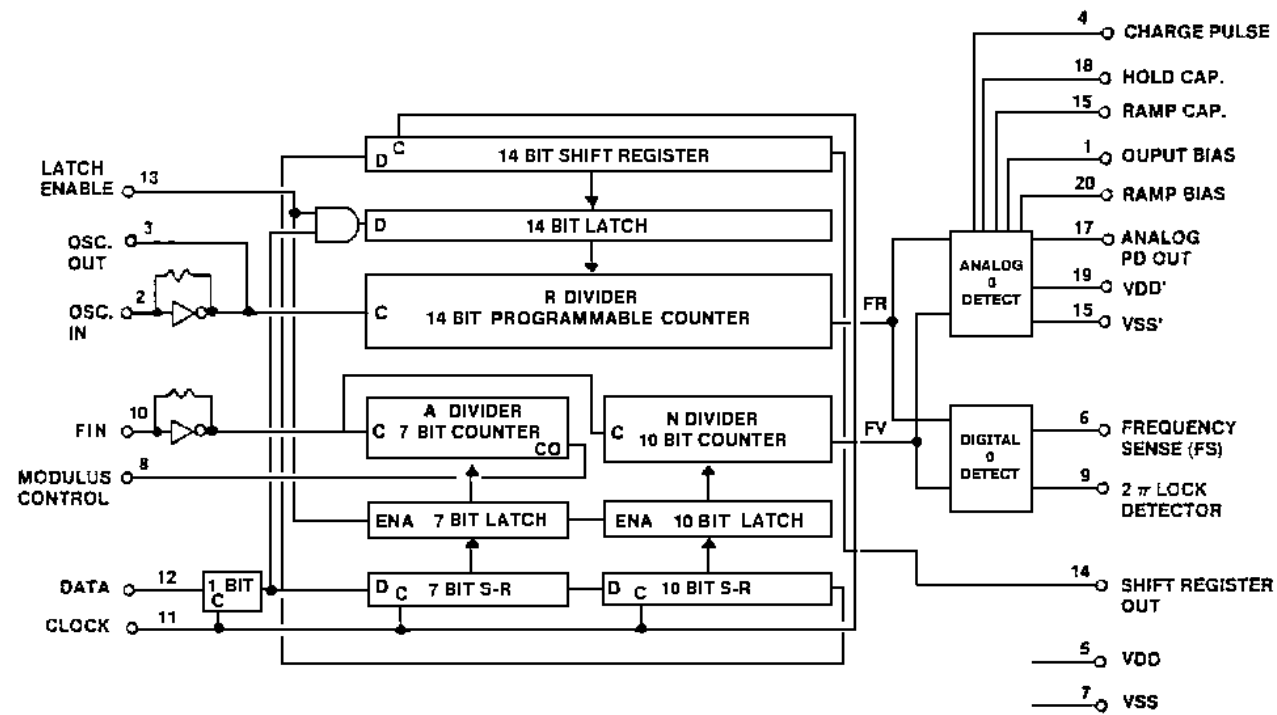
PLL MODULE U201  
19B800902P1

SECOND MIXER/LIMITER/FM DETECTOR U501  
19A704619P1

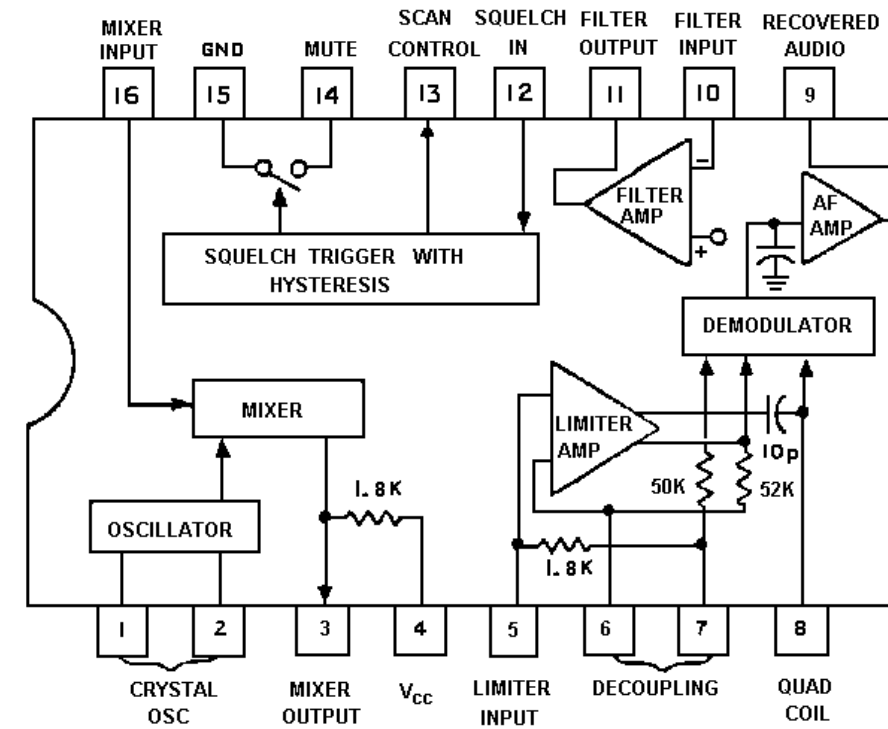
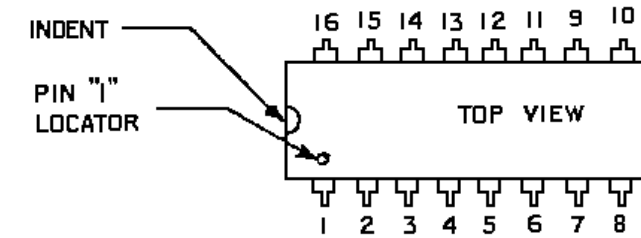


PIN DESCRIPTION

OUTPUT BIAS	1	TOP	20	RAMP BIAS
OSC. IN	2		19	VDD'
OSC. OUT	3		18	HOLD CAP.
CHARGE PULSE	4		17	ANALOG PD OUT
VDD	5		16	VSS'
(FS) FREQ. SENSE	6		15	RAMP CAP.
VSS	7		14	SHIFT REGISTER OUPUT
MODULUS CONTROL	8		13	LATCH ENABLE
2 π LOCK DETECTOR	9		12	DATA IN
FIN	10		11	CLOCK



PIN CONFIGURATION



BLOCK DIAGRAM

R  
E  
A  
R  
A  
S  
S  
E  
M  
B  
L  
Y