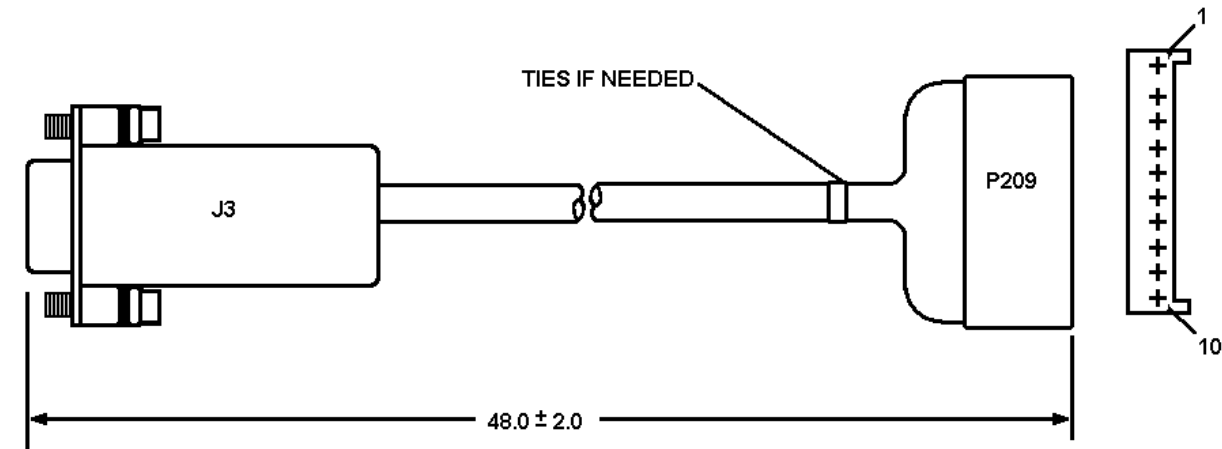


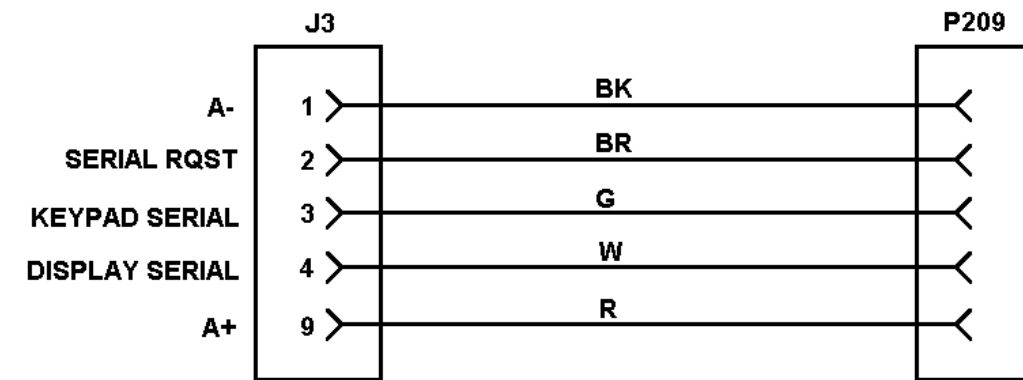
Installation/Maintenance Manual

RADIO DATA INTERFACE



CONNECTOR J3
WIRING SIDE
SHOWN

(19A705884, Sh. 11, Rev. 7)



CONNECTION CHART FOR PART 5.

2. CONNECTOR J3 TO BE 9 POSITION D'SUBMINIATURE RECEPTACLE HOUSING SIMILAR TO AMP. CAT. #205203-1 (GE 19B209727P18) OR EQUIVALENT. CONTACTS TO BE SIMILAR TO AMP CAT. #5-66504-9 OR EQUIVALENT. BACKSHELL TO BE AMP CAT. #207487-1 OR EQUIVALENT WITH #4-40 SCREWS SIMILAR TO AMP CAT. #205980-1 OR EQUIVALENT.

P209 HOUSING TO BE 10 POSITION MOLEX CAT. #22-0101205 OR EQUIVALENT CONTACTS TO BE RECEPTACLE CONTACTS SIMILAR TO MOLEX 08-55-0101 OR EQUIVALENT. CONTACTS TO BE GOLD PLATED 30 u" NOMINAL THICKNESS. OPEN POSITIONS HAVE NO CONTACTS.

(19A705884, Sh. 12, Rev. 7)

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NOTICE!

This manual covers Ericsson and General Electric products manufactured and sold by Ericsson Inc.

NOTE!

Repairs to this equipment should be made only by an authorized service technician or facility designated by the supplier. Any repairs, alterations or substitution of recommended parts made by the user to this equipment not approved by the manufacturer could void the user's authority to operate the equipment in addition to the manufacturer's warranty.

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SPECIFICATIONS*

Supply Voltage:	Range	10.7 to 16.6 Vdc
	Typical	13.6 Vdc
Current Drain		less than 100 mA
Serial Port		RS232 type
Radio Port		Serial type with (2) open collector option outputs and power input
Temperature Range		-30 to + 60 degrees Celsius
Dimensions		137 x 105 x 48 mm
Weight		10 ounces

* These specifications are intended primarily for the use of the service technician. Refer to the appropriate Specification Sheet for the complete specifications.

DESCRIPTION

The Radio Data Interface (RDI) is a protocol converter to allow a device to communicate with a mobile via an RS-232 interface and a sample protocol.

The Radio Data Interface (RDI) unit connects RS232 devices over an EDACS trunking system. It converts and buffers data between a standard asynchronous RS232 device such as a mobile data terminal (MDT) and the EDACS radio's serial control bus.

The RDI units mechanical construction includes a single printed circuit board housed in an ABS plastic case. The case is internally metallized to reduce RF emissions from the digital circuits inside. Two nine pin "D" type connectors are provided for connection to the radio and the RS232 terminal.

CAUTION

DO NOT connect the MDT directly to the EDACS radio. The RDI must be connected in series with and between the MDT and the radio's port for proper operation. Damage to the MDT and/or radio may result if the RDI is not interconnected between the two units. See the appropriate installation interconnection diagrams for further details on the MDT/RDI/EDACS interconnections.

OPTIONS

The RDI contains 4 option modes.

Printer Mode

This mode is intended to send data directly to a serial printer. As the radio receives data it starts sending it to the RDI which in turn sends it to the printer.

NOTE

This mode does NOT use the RDI 1.92 protocol (XFERB, etc.). Also the radio sends only correctly received contiguous data to the RDI. Therefore, if the receiver errors out half way through the data message, the first half will be printed and the second half will be lost.

AVL Mode

This mode is identical to the default "RDI mode, MDT has priority" except the address the RDI uses to communicate to the radio is different (AVL=15, RDI=6).

RDI Mode, RDI has priority

This mode uses the RDI 1.92 Protocol to send/receive data message to/from a data terminal. It assumes it has priority in the case of an XFERB collision. (See "RDI Interface Priority").

RDI Mode, MDT has priority

This is the factory default setting. This mode uses the RDI 1.92 Protocol with with the MDT having priority exactly the same as the old RDI (19A149657G3) prom.

FEATURES

Anti-biasing

Radio and base station receiver detection circuitry can become biased during a data call by the data pattern contained in the message. Once this occurs, the radio can no longer reliably tell the difference between a "1" bit and an "0" bit. The Enhanced RDI contains an anti-biasing algorithm known as BREN to alleviate this problem.

This algorithm adds 12.5% overhead to data sent over the air but is transparent to the user who can still send 512-byte data messages to the RDI. This will require that the EDACS Data Gateway (EDG) and mobiles with built-in RDI 1.92 functionality also support BREN for compatibility across all platforms. BREN is jumper selectable.

RDI Interface Priority

The RDI can now be configured so that it assumes priority on the RDI interface in the case of a collision. If the terminal and the RDI send XFERB messages at the same time, the terminal must back off and accept the inbound data transfer from the RDI. This prevents the application from wasting the air time spent in transmitting the inbound message to the RDI. Giving priority to the RDI also allows a more robust collision protection scheme as described in later sections. The RDI can be configured so that priority is given to the terminal to maintain compatibility with existing RDI protocol implementations.

Collision Protection

A collision occurs when the terminal is trying to send a message outbound at the same time the radio is trying to send a message inbound. The inbound and outbound message can collide either on the RDI interface or on the interface between the RDI and the mobile. In previous versions of the RDI, a collision generally resulted in the loss of one or both of the messages. Version 4.06 of RDI software has enhanced collision handling to prevent the loss of messages because of collisions. The collision handling scheme is different depending on whether the RDI or the terminal is given priority on the RDI interface. Each case is discussed below where an inbound message is from the network and an outbound message is from the data terminal.

XFERB Collision (Data Terminal has Priority)

This collision type occurs when the RDI and the data terminal both have messages to send. Figure 1 shows the possible timing scenarios for this collision type. When the collision occurs, the RDI responds to the data terminal's XFERB with an ACK0, stores the inbound message, and receives the outbound message from the terminal. Once the radio completes the transmission of the outbound message, the RDI sends the completion status (ACKA or ACK2) followed by the XFERB for the inbound message.

If the data terminal sends another XFERB before the RDI can send its XFERB, the RDI responds with ACK0 and then sends an ACKA immediately. Since the data terminal must wait 50 ms upon receiving the ACKA, the RDI has time to get its XFERB accepted by the terminal. In this situation, the RDI must abort any other inbound calls from the radio as long as it already has an inbound message.

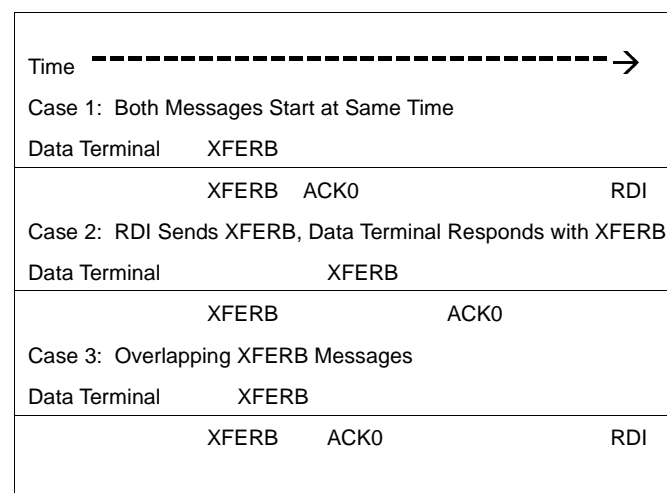


Figure 1 - XFERB Collision Timing Scenarios

Message Collision Inside RDI (Data Terminal has Priority)

A collision occurs inside the RDI when it is receiving data from the radio and the data terminal initiates an outbound message transfer. The RDI handles this in the same manner as described for the XFERB collision situation.

Pending Inbound Call Radio Collision (Data Terminal has Priority)

The radio waits for 256 bytes of data, or the entire message is less than 256 bytes, before sending in a channel request. In this situation, the RDI starts sending data to the radio. Before it can receive enough data to initiate a channel request, the radio receives a channel assignment for an inbound call. The radio aborts the outbound data transfer from the RDI and begins to accept the inbound message.

Even though the radio aborted the outbound message, the RDI continues to receive the message from the terminal. Once the terminal completes the transfer, the RDI sends an ACKA to the terminal and flushes the message. When the RDI has received all of the data from the radio, it sends an XFERB to the terminal to start the transfer of the inbound message.

Radio Already Receiving Call Collision (Data Terminal has Priority)

The radio is receiving an inbound message when the RDI requests to send the radio an outbound message. The radio aborts the outbound message transfer and continues receiving the inbound message. Meanwhile, the RDI finishes receiving the outbound message from the data terminal. Once the outbound message transfer is complete, the RDI aborts the call with an ACKA. The RDI sends an XFERB for the inbound message once it has received all the data from the radio.

If the radio initiates another outbound message transfer before the RDI receives all of the data from the radio, a collision occurs in the RDI which the RDI handles as described above.

XFERB Collision (RDI has Priority)

This collision type occurs when the RDI and the data terminal both have messages to send. Figure 2 shows the possible timing scenarios for this collision type. When the collision occurs, the data terminal must respond to the RDI with an ACK0 and accept the data from the RDI. Once the RDI has completed sending the inbound message, the terminal can initiate the transfer of the outbound message with a new XFERB command.

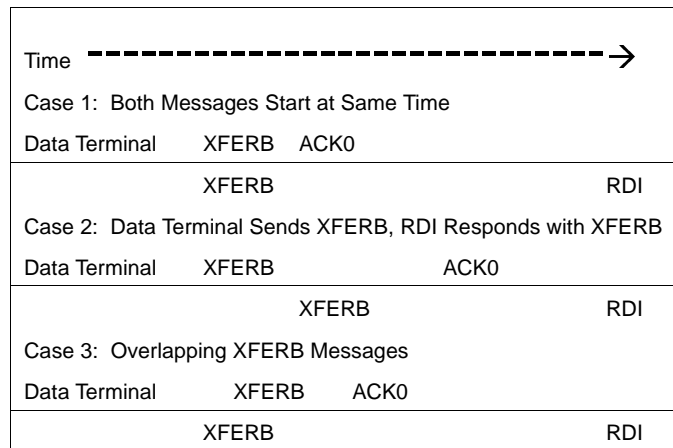


Figure 2 - XFERB Collision Timing Scenarios

Message Collision Inside RDI (RDI has Priority)

If a collision occurs in the RDI before it has sent its *XFERB*, the RDI receives the outbound message from the terminal and stores the inbound message from the radio. Once the radio completes the outbound message transfer, the RDI sends the completion code (*ACK2* or *ACKA*) followed by the *XFERB* for the inbound message. If the terminal tries to send a new message immediately after receiving the completion code, an *XFERB* collision occurs. The RDI handles the collision as described above.

Pending Inbound Call Radio Collision (RDI has Priority)

If the radio receives a channel assignment while receiving data from the RDI, it aborts the outbound data transfer and goes to the working channel. The RDI continues to receive the outbound message from the terminal storing it in a buffer, while receiving the inbound message from the radio. Once the inbound transfer from the radio to the RDI is complete, the RDI initiates the outbound message transfer to the radio. When the outbound call is complete, the RDI returns the completion code (*ACK2* or *ACKA*) to the terminal followed by an *XFERB* for the inbound message.

If the radio receives another channel assignment while receiving the outbound message from the RDI, it aborts the outbound data transfer again and goes to the working channel. The RDI, in turn, aborts the outbound message with an *ACKA* and sends an *XFERB* for the stored inbound message.

Radio Already Receiving Call Collision (RDI has Priority)

If the RDI initiates an outbound data transfer while the radio is receiving an inbound message, the radio aborts the outbound

data transfer. The RDI stores the outbound message in a buffer and waits for the inbound message from the radio. Once the radio completes the inbound data transfer, the RDI initiates the outbound message transfer to the radio. When the outbound call is complete, the RDI returns the completion code (*ACK2* or *ACKA*) to the terminal followed by an *XFERB* for the inbound message.

If the radio receives another channel assignment while receiving the outbound message from the RDI, it aborts the outbound data transfer again and goes to the working channel. The RDI, in turn, aborts the outbound message with an *ACKA* and sends an *XFERB* for the stored inbound message.

Double Buffering from Mobile

If a second data message is sent to a mobile immediately after the mobile has received a message, there may still be data in the RDI that is being transferred to the MDT. This occurs with data messages larger than 350 bytes. Previous RDI software would not accept the second message until it has finished sending the first message to the MDT and would force the mobile to abort the call.

By double buffering the messages from the mobile, the RDI can accept a second message while sending the first message to MDT. Because of setup times and other delays within the mobile, this double buffering allows back-to-back messages to be sent to the mobile from the host as soon as the mobile is available.

CIRCUIT ANALYSIS

The board circuitry includes the microprocessor circuits, serial radio port, asynchronous UART controlled RS232 port, clock generation sections and a regulated power source. A block diagram of the RDI unit is shown in Figure 3.

The RS232 device is connected to the nine pin female connector Serial Port P2. Data is received by RRXD and its handshake line RCTS. Data is transmitted from RTXD and its handshake line RRTS.

The radio is connected to the nine pin male connector Radio Port P3. Received serial data arrives at FSERRX and is transmitted from FSERTX. Handshaking is provided by the FSERQT signal. Also, two option signals to the radio (open collector pulldowns) are present on P3. Switched power for the unit is supplied through P3 from the EDACS radio.

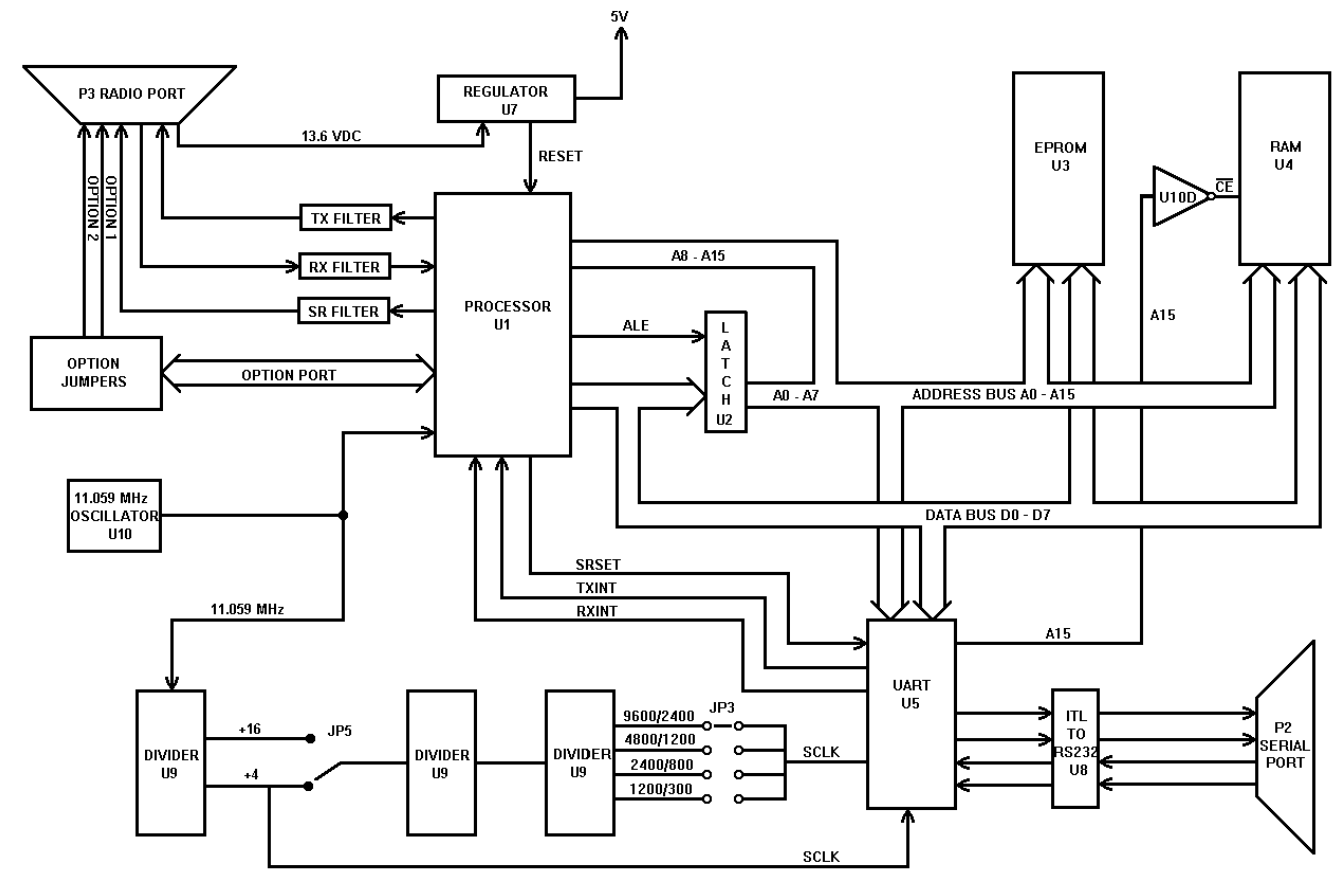


Figure 3 - Block Diagram

MICROPROCESSOR

Microprocessor U1 is an external program memory 80C31 system using EPROM U3. This IC contains the controlling program. The lower 8 address lines are latched in octal latch U2 via the ALE signal from U1. Resistor pack RP1 provides pullup for the data bus.

Integrated circuit U3, normally a 32k 27C256 EPROM, is configured by the hardwired jumper at JP2 and JP6. The EPROM is enabled by a low PSEN signal from the processor. Temporary memory is located in static RAM U4 and is normally configured for a 8K 6264 RAM by hardwired jumpers JP8 and JP7. See the CONFIGURATION section for other possible memory configurations.

Address line decoding for the RAM and UART is provided by U10D. When A15 is low (00007-FFF hex) the UART is selected. When A15 is high (8000-FFFF hex) the RAM is selected. The active low read (RD) and write (WR) lines are used by the RAM and UART for proper bus timing.

Processor port 1 is used to read configuration data from

the bank of jumpers at JP4. Bits 6 and 7 are configured for outputs and are buffered by Q6 and Q7. These open collector outputs are applied to connector P3.

RADIO PORT

Serial data at the Radio Port P3 is transferred using the processors internal UART. This port's baud rate is set by the processors read of the option port. See the CONFIGURATION section, OPTION JUMPERS, for details of the Radio Port's baud rates.

Serial data from P3 pin 4 arrives at RXD via the RX Data Line Filter. Diodes D1 and D2 and resistors R11 and R15 maintain the input SERRX signal within TTL logic levels.

Serial data is transmitted from TXD via the TX Line Filter to P3 pin 3. Transistors Q2 and Q4 and associated components provide buffering and filtering for the SERTX signal.

The Service Request signal at P3 pin 2 arrives from the processors T1 signal via the Service Request Line Filter. Transistor Q1 and associated components provide buffering and filtering for the SERRQT signal.

RS232 SERIAL PORT

The RS232 serial data at Serial Port P2 is transferred using the UART U5 and TTLRS232 level converter U6. Data is received by RRXD and its handshake line RCTS. Data is transmitted from the board by RTXD and its handshake line RRTS.

The Intel 8251 asynchronous UART provides the necessary serial to parallel and parallel to serial conversions from the RS232 serial port to the processor. The 8251's active low CTS line is tied to ground. The UART is software controlled by the 80C31 and it can be reset by the TO line from the processor. Inverter U10C and transistor Q5 invert the receive and transmit ready status lines from the 8251 to interrupt the 80C31.

Integrated circuit U6 is powered from the + 5 volt supply and has an internal RS232 level generator for the positive and negative RS232 power sources. Capacitors C1 1 through C14 are used for the conversion process. Resistor R24 pulls the RCTS line to the negative supply (not ready) when there is no connection to the serial port.

CLOCK CIRCUITS

The master oscillator U10A is set to 11.059 MHz by crystal Y1. Buffering for the processors XTAL input and divider U9 is provided by U10B.

Four bit counter U9A outputs a divided by 4 (2.765 MHz) clock, SCLK, and a divided by 16 (691.2 kHz) clock. The SCLK signal is applied to the UART's master CLK input.

The UART also needs a clock signal present on its TXCLK and RXCLK pins which is 16 times the intended baud rate. The 2.765 MHz and 691.2 kHz signals are applied to JP5 for baud rate selection. Further division and selection is accomplished by U8, U9B, U10E and U10F. Integrated circuit U8 functions as a divide by 9 circuit. The preset inputs are wired to load a nine into the IC and the borrow output resets\presets the counter via U10E and U10F. The borrow output also provides a clocking signal to four bit counter U9B. This IC outputs the clock signals to JP3 for jumper selection to the BCLK line. See the CONFIGURATION section for further details on selecting baud rates.

POWER SUPPLY

Switched power is supplied from the EDACS radio to the unit through Radio Port connector P3 pins 5 and 9. Also, pins 1 and 6 provide ground. Regulator U7 supplies the boards

digital logic with a + 5 volt DC source. This IC also supplies the reset pulse through Q3 to the microprocessor at power on.

CONFIGURATION

The unit is factory wired for proper memory types, baud rates, etc. and does not normally need a change in the configuration. Factory hardwired jumper configurations are indicated in the tables below by an "***" .

MEMORY JUMPERS

Installed memory types are selected by the installation of jumpers. Jumpers JP2, JP6 select proper EPROM types and JP7, JP8 select proper RAM types. The following tables indicate a presence of a jumper by an "X".

OPTION JUMPERS

The eight option jumpers at JP4 select system configurations. See Table 3.

BAUD RATE JUMPERS

The UART's baud rate can be selected by the positioning of two jumpers JP3 and JP5. The factory configuration is 9600 baud ("**"). See Table 4 for the indication of a jumper by an "X".

INSTALLATION

CAUTION

DO NOT connect the MDT directly to the EDACS radio. The RDI must be connected in series with and between the MDT and the radio's port for proper operation. Damage to the MDT and/or radio may result if the RDI is not interconnected between the two units. See the appropriate installation interconnection diagrams for further details on the MDT/RDI/EDACS interconnections.

Mechanical installation of the RDI in the mobile unit requires selecting an adequate location near the EDACS control unit and securing the RDI with hardware provided. The hardware consists of two #6 thread forming screws and two #6A sheet steel nuts.

Electrical installation in mobiles with EDACS S-550 control units requires connection of cable 19A705884P2 to the

Table 1 - EPROM Configuration

EPROM TYPE	SIZE	JP2 1-2	JP2 2-3	JP6 1-2	JP6 2-3
27C64	8K		X	X	
27C256**	32K	X		X	
27C512	64K	X			X

Table 2 - RAM Configuration

RAM TYPE	SIZE	JP7 1-2	JP7 2-3	JP8 1-2	JP8 2-3
6116	2K	X			X
6264**	8K		X	X	
62256	32K		X	X	

Table 3 - Option Jumper Settings

Jumper	Use	Configuration
JP4 1-2 JP4 3-4	Device Mode	0 = Printer mode 0
JP4 1-2 JP4 3-4		0 = AVL mode 1
JP4 1-2 JP4 3-4		1 = RDI mode, RDI has priority 0
JP4 1-2 JP4 3-4		1 = RDI mode, MDT has priority* 1
JP4 5-6	BREN	0 = Enabled 1 = Disabled*
JP4 7-8		1**
JP4 9-10		1**
JP4 11-12	RS232 Port Bits/Byte	1 = 8 Bits* 0 = 7 Bits
JP4 13-14 JP4 15-16	RS232 Port Parity	00= Even* 01 = Odd 10 = None 11 = Even
1 = Jumper Installed 0 = No Jumper		* factory settings ** do not remove

Table 4 - Baud Rate Jumper Settings

Baud Rate	JP3 1-2	JP3 3-4	JP3 5-6	JP3 7-8	JP5 1-2	JP5 2-3
300				X	X	
600			X		X	
1200		X			X	
2400	X				X	
4800		X				X
9600*	X					X
X = Jumper Installed				* factory settings		

RDI connector P3 and control unit J203. Also see the EDACS S-550 manual, LBI-31803.

Electrical installation in mobiles with EDACS FMD radios or EDACS S700 control units requires two interconnecting cables. They are 19A705864P1 for connection to the RDI connector (at P3) and cable 19C337129P2 for connection to the EDACS FMD connector (at ZC852) or the EDACS S-700 connector (at J604). Also see the EDACS FMD installation manual, LBI-38100, or EDACS S-700 installation manual, LBI-38145.

The MDT RS232 device connection will also be required. This cable must be supplied by the installer. See Figure 4.

Electrical installation of the RDI with the MTD Series radios requires installing the RDI cable 19A705884P3. This is done by disconnecting the microphone cable from J725 on the radio. Install the RDI cable between P3 on the RDI and J725 on the radio and reconnect the microphone cable to the RDI cable mic connector.

OPERATION

The RDI has no external user operating controls. Refer to the appropriate EDACS radio or MDT manual for operating details.

TESTING

The following test procedures assumes a partially functional (CPU, EPROM and UART) RDI unit. The unit must be configured by removing all jumpers from JP4 except JP4 11-12 (P1.5) and connected as shown in figure 4. The terminal must be configured as follows: 9600 baud, 8 bit data, even parity, 1 start bit and 1 stop bit. This functional test program is invoked when Service Request Line P3 pin 2 is connected to the Receive Data (P3-4) at powerup. See Figure 5 for Test Setup details.

After applying power to the RDI, the message "Power-Up Self Test OK" is displayed on the RS232 terminal. Any found failure will result in a display of an appropriate failure message. For example, a defective static RAM will result in the display of "Power-Up Self Test FAILED - "SRAM LOCATION xxxx".

If no keyboard key is pressed within one minute from power on, the unit will invoke an automatic test. This test should not be needed by the technician and should be terminated with an <ESC> if started.

The following commands in Table 5 can be executed from the terminal to further test various hardware and software of the unit.

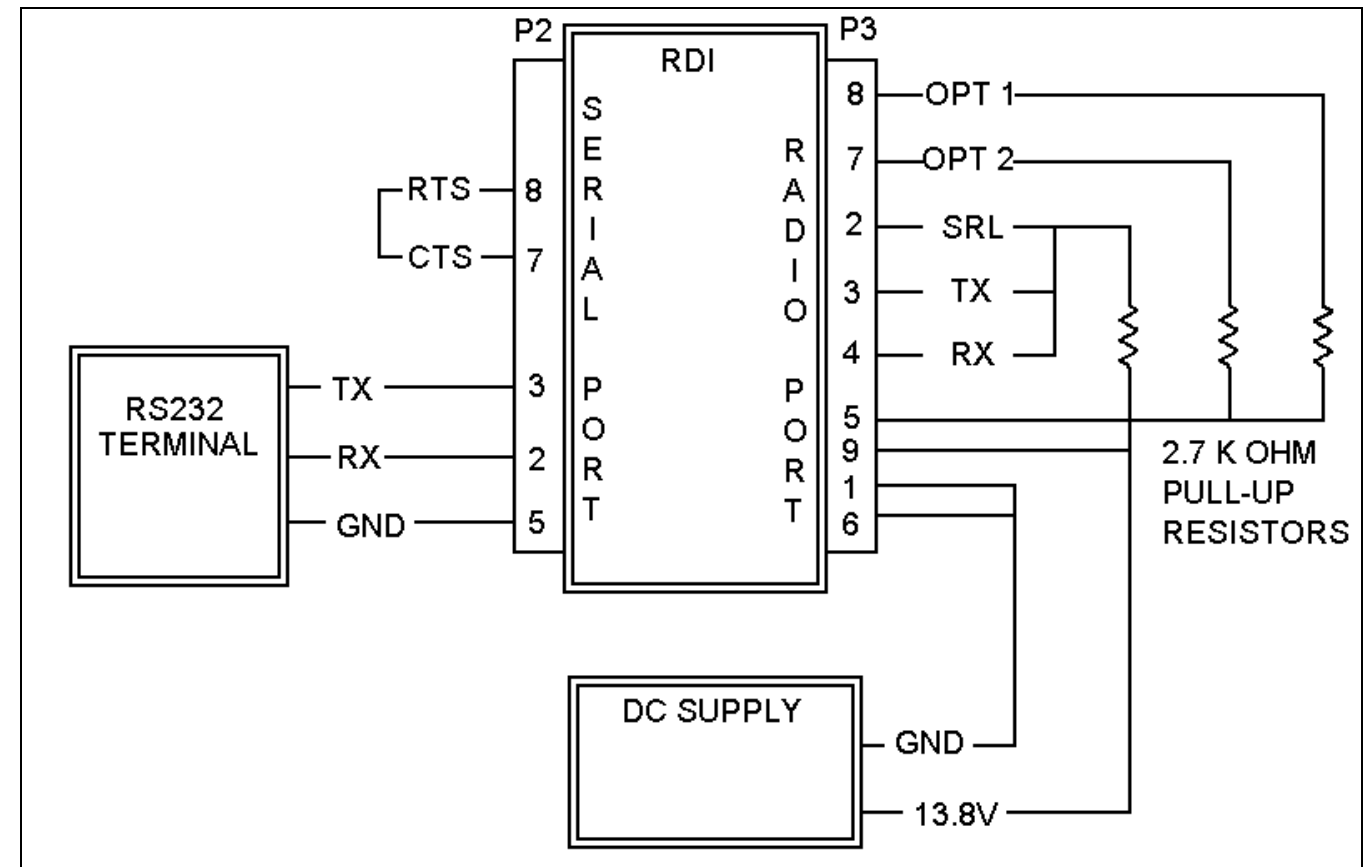


Figure 5 - Test Setup

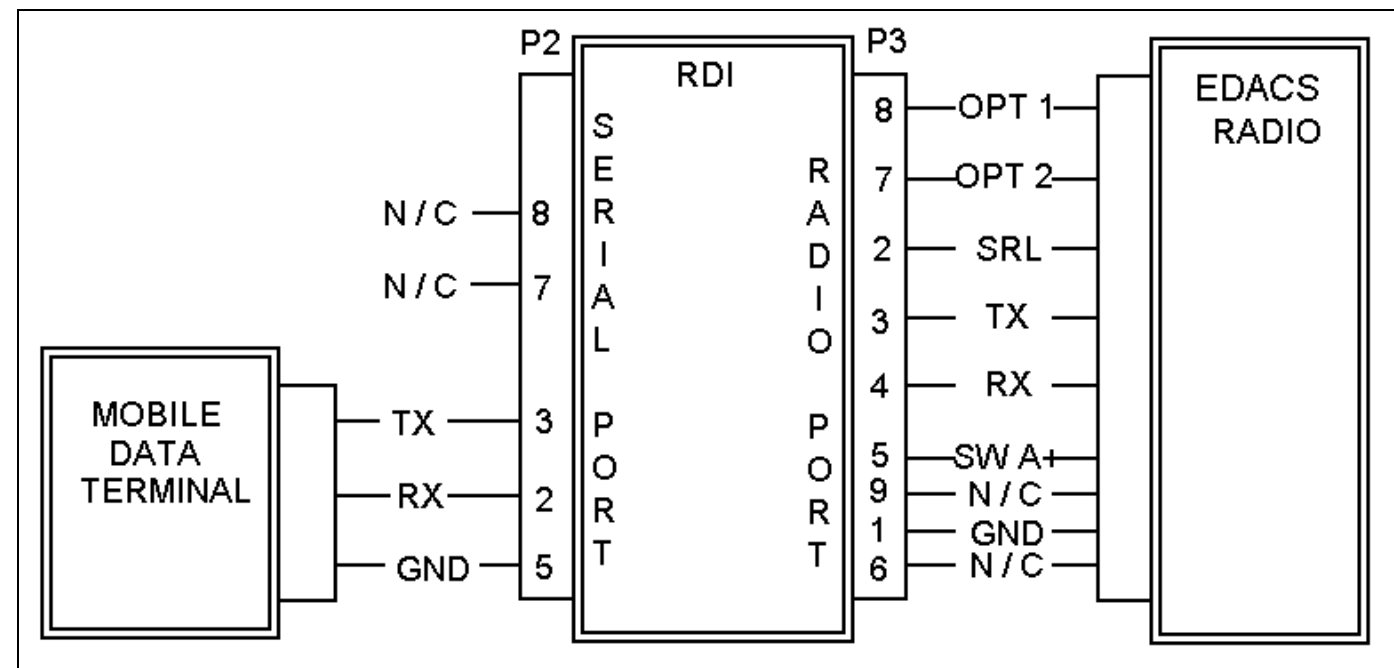


Figure 4 - Electrical Connections

Table 5 - RDI Test Commands

COMMAND <cr>	COMMENTS
CHK 0 - 7FFF	EPROM CHECKSUP ('0-7FFF' is for 32K EPROM). Displays "EPROM CHECKSUM VERIFIED OK" when successful. Displays "EPROM CHECKSUM FAILED" if not successful.
DOT A	Sends a 4800 Hz square wave (a continuous stream of ASCII U's) out MDT port TX, P2 pin 3. U's will be displayed on the RS232 Device. Use <ESC> to terminate.
DOT C	Sends a 4800 Hz square wave (a continuous stream of ASCII U's) out RADIO port TX, P3 pin 3. Use <ESC> to terminate.
DOT D	Initiates a toggle/loopback of RTS to CTS. Displays "RTS-CTS LOOPBACK - OK" when successful. Use <ESC> to terminate.
HEL	Prints help text on screen. This prompt screen may refer to certain test commands not explained in this document and are for Ericsson test use.
PAR	Reads the software part number from EPROM.
POR 3 = CF	Sets Service Request Line (SRL) high.
POR 3 = EF	Sets SRL low.
POR 1 = 3F	Sets OPTN01 and OPTN02 high.
POR 1 = BF	Sets OPTN01 low.
POR 1 = 7F	Sets OPTN02 low.
RCH	Reads software checksum from EPROM.

Table 5 (Continued) - RDI Test Commands

<u>COMMANDS <cr></u>	<u>COMMENTS</u>
RES	Resets RDI displays: "Power-Up Self Test - OK".
SEQ	A sequence of automatic (unattended) tests. Stops if an error is detected.
SRQ	Toggles SRL.
TMX E0000-FFFF	Static RAM test. Displays "PATTERN CHECK OK" for each successful pass. An example of a failed test pass message is: "LOCATION E0000 DATA EXPECTED = DF DATA READ = FF". 'E0000-FFFF' is for 8k SRAM; 'F800-FFFF' for 2k SRAM.
TST	Runs a sequence of tests in a semi-automatic (attended) fashion, prompting the technician and requiring him to confirm outputs via oscilloscope or voltmeter. Use <SPACE BAR> to confirm proper output actions from the RDI and continue test. Use <ESC> to abort "TST". This test sequence starts with the power-up self test and continues with memory checks, radio and RS232 port checks. Any error found by the RDI will be reported by "*** TEST FAILED - REJECT RDI ***" and one or more of the following messages: "Power-Up Self Test FAILED - EPROM CHECKSUM MISMATCH" "Power-Up Self Test FAILED - SRAM LOCATION xxxx" "Power-Up Self Test FAILED - USTART STATUS" "Power-Up Self Test FAILED - TIMER0 -vs- CYCLE TIME" "Power-Up Self Test FAILED - TIMER1 -vs- CYCLE TIME" "Power-Up Self Test FAILED - TIMER0 INTERRUPT FAILED" "Power-Up Self Test FAILED - TIMER0 INTERRUPT FAILED" "2 K RAM (F800-FFFF) PATTERN CHECK FAILED" "8 K RAM (E000-FFFF) PATTERN CHECK FAILED" "RADIO PORT LOOPBACK - FAILED" "RTS-CTS LOOPBACK - FAILED"
URT C	To run a timed loopback test on the radio port. DISPLAYS "RADIO LOOPBACK - OK" when successful
URT E	To run an echo test on the MDT port. Use <ESC> to terminate.
VER	Reads the software version number from EPROM

**RADIO DATA INTERFACE
(19A149654P2)**

The Radio Data Interface (19A149654P2) is used in PC programming applications with the DELTA and RANGR mobile radios and the VG-9600 Voice Guard modules. This provides RDI related information on these applications. EPROM U3 is now 19A149657G3 for PC programming applications.

The 19A149654P2 RDI is identical to the 19A149654P1 RDI except the units have different jumper configurations. Table 7 lists factory jumper configurations for both RDI's.

Table 6 - RDI and Cables

ORDER/OPTION NUMBER	PART NUMBER	DESCRIPTION	APPLICATION
DE1A (DE01*)	19A149654P1	Radio Data Interface	EDACS
TQ-3330	19A149654P2 19B235027P3	Radio Data Interface Cable: PC to RDI	PC Programming PC Programming
TQ-3331	19B234413G21	Cable: RDI to radio	PC Programming
TQ-3345	19B234413G22	Cable: RDI to VG-9600	PC Programming
* = Old Option Number			

TESTING THE RADIO DATA INTERFACE (19A149654P2)

To test the 19A149654P2 RDI, follow the procedures presented in the "TESTING" section of this manual for a 19A149654P1 RDI. Jumpers will have to be configured as presented to invoke the monitor test program. Terminal baud rate will be 9600. Test, troubleshoot and repair the RDI unit as necessary.

After complete operation of the RDI has been verified, reconfigure the unit to a P2 RDI (See Table 7). If the unit fails to program a radio properly, check for a 38.4 kHz (±3 Hz) signal at JP3 pin 5. This square-wave is the clock signal to the UART and it should be 16 times the intended baud rate. If this signal is not present, suspect a defective output from U9. If the signal is present, check for proper JP3 configuration (JP3 5-6 installed, no others). Also check the PC to RDI and RDI to radio connections.

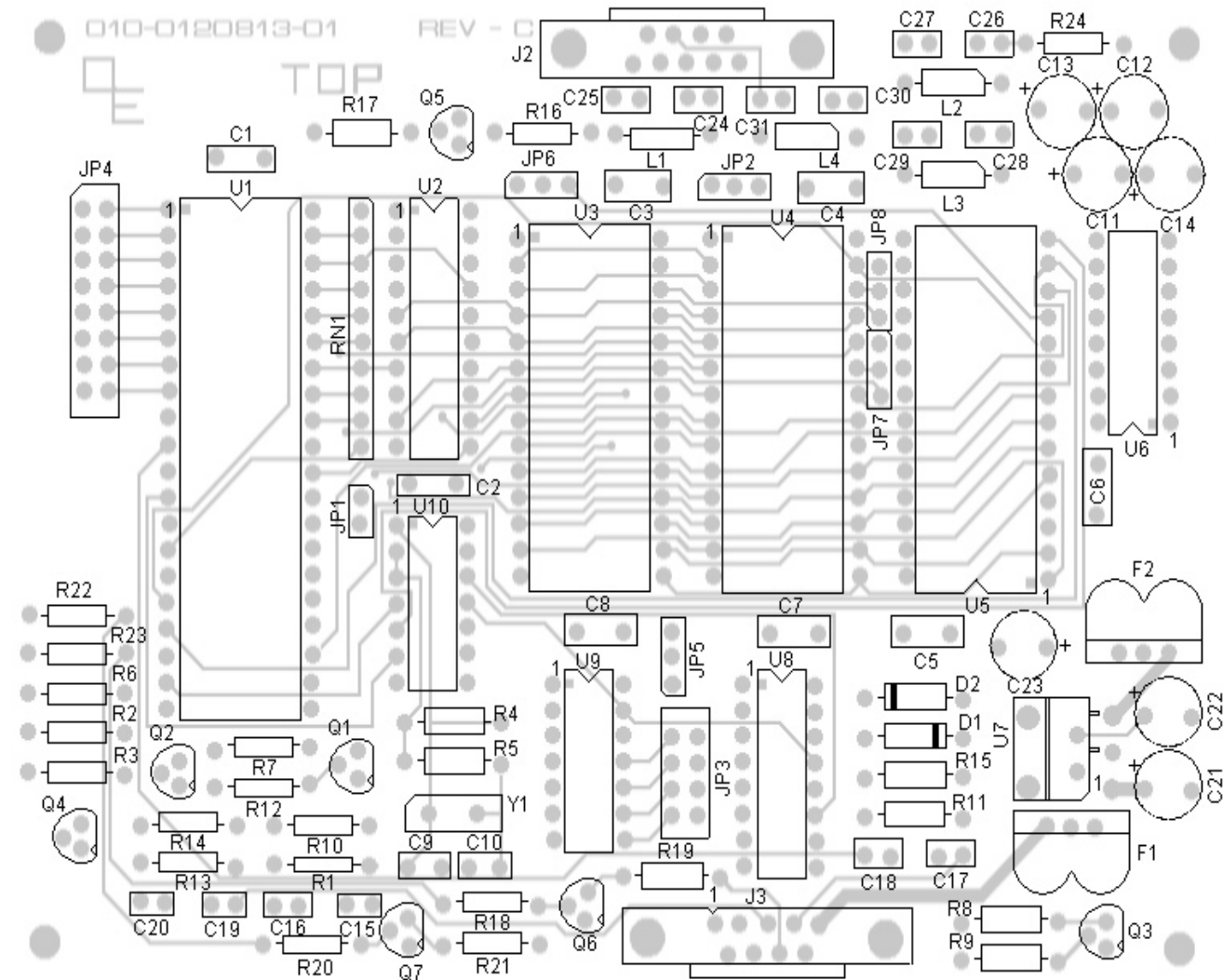
Table 7 - RDI Jumper Configuration

JUMPER	USE	19A149654P1	19A149654P2
JP1 1-2	EA Jumper	X*	X*
JP2 1-2	EPROM Type	X*	X*
JP2 2-3	EPROM Type		
JP3 1-2	Serial Baud Rate	X	
JP3 3-4	Serial Baud Rate		X
JP3 5-6	Serial Baud Rate		
JP3 7-8	Serial Baud Rate		
JP4 1-2	Device Type	X	X
JP4 3-4	Device Type	X	X
JP4 5-6	Unit ID (AVL)	X	X
JP4 7-8	Device Type	X	
JP4 9-10	Radio Baud Rate	X	X
JP4 11-12	Serial Bits/Byte	X	X
JP4 13-14	Serial Parity		
JP4 15-16	Serial Parity		
JP5 1-2	Serial Baud Rate	X	X
JP5 2-3	Serial Baud Rate	X*	X*
JP6 1-2	EPROM Type		
JP6 2-3	EPROM Type		
JP7 1-2	RAM Type		
JP7 2-3	RAM Type	X*	X*
JP8 1-2	RAM Type	X*	X*
JP8 2-3	RAM Type		

X = Jumper Installed
 X* = Jumper is part of Printed Wire Board

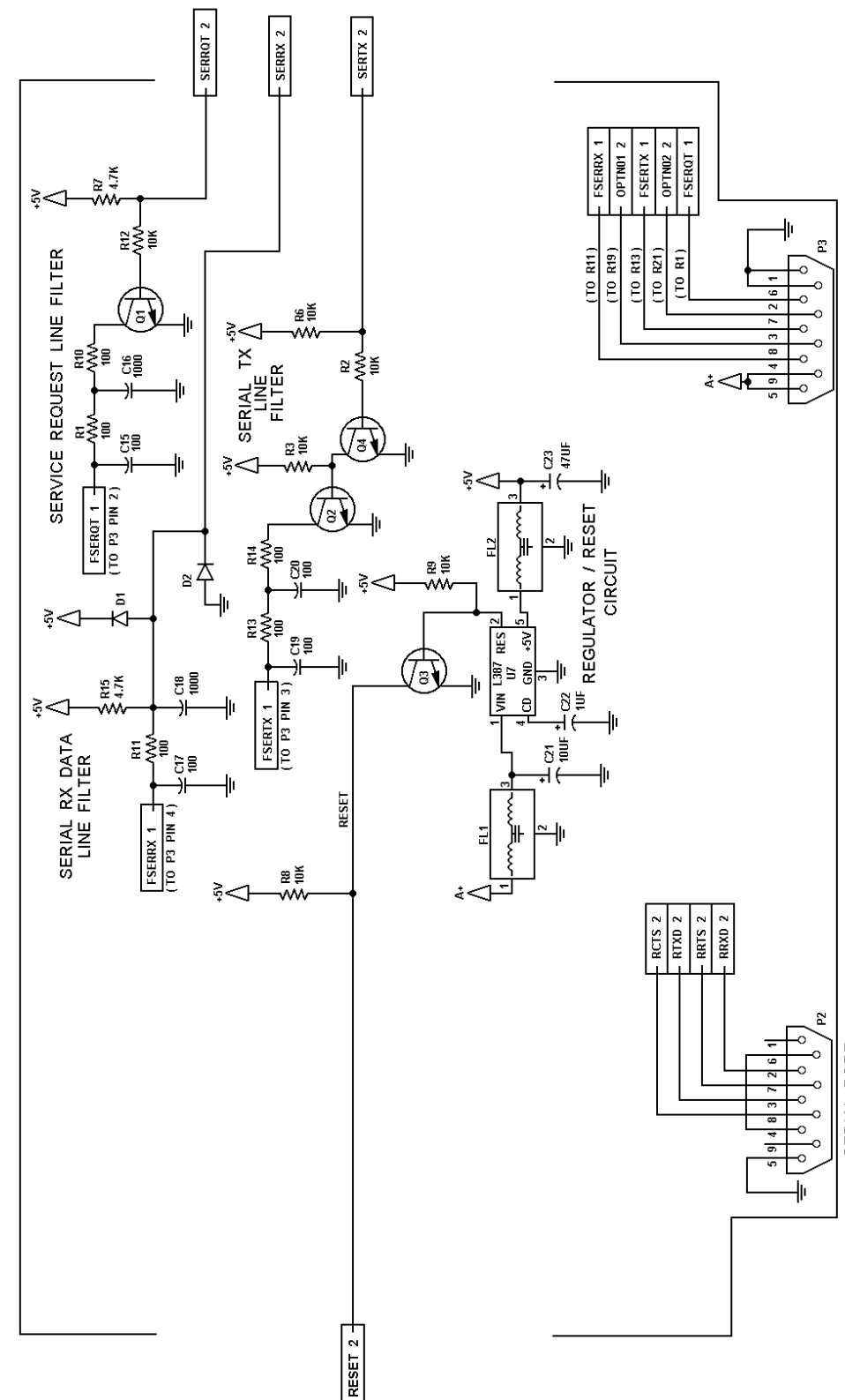
NOTE

As this is a multi-layer printed wire board, the inner traces - power and ground - are not shown. See the Schematic Diagram for power and ground connections.



**RADIO DATA INTERFACE
19D902301G1**

(048-0120813-01, Rev. C)
(010-0120813-01, Sh. 1, Rev. C)
(010-0120813-01, Sh. 4, Rev. C)

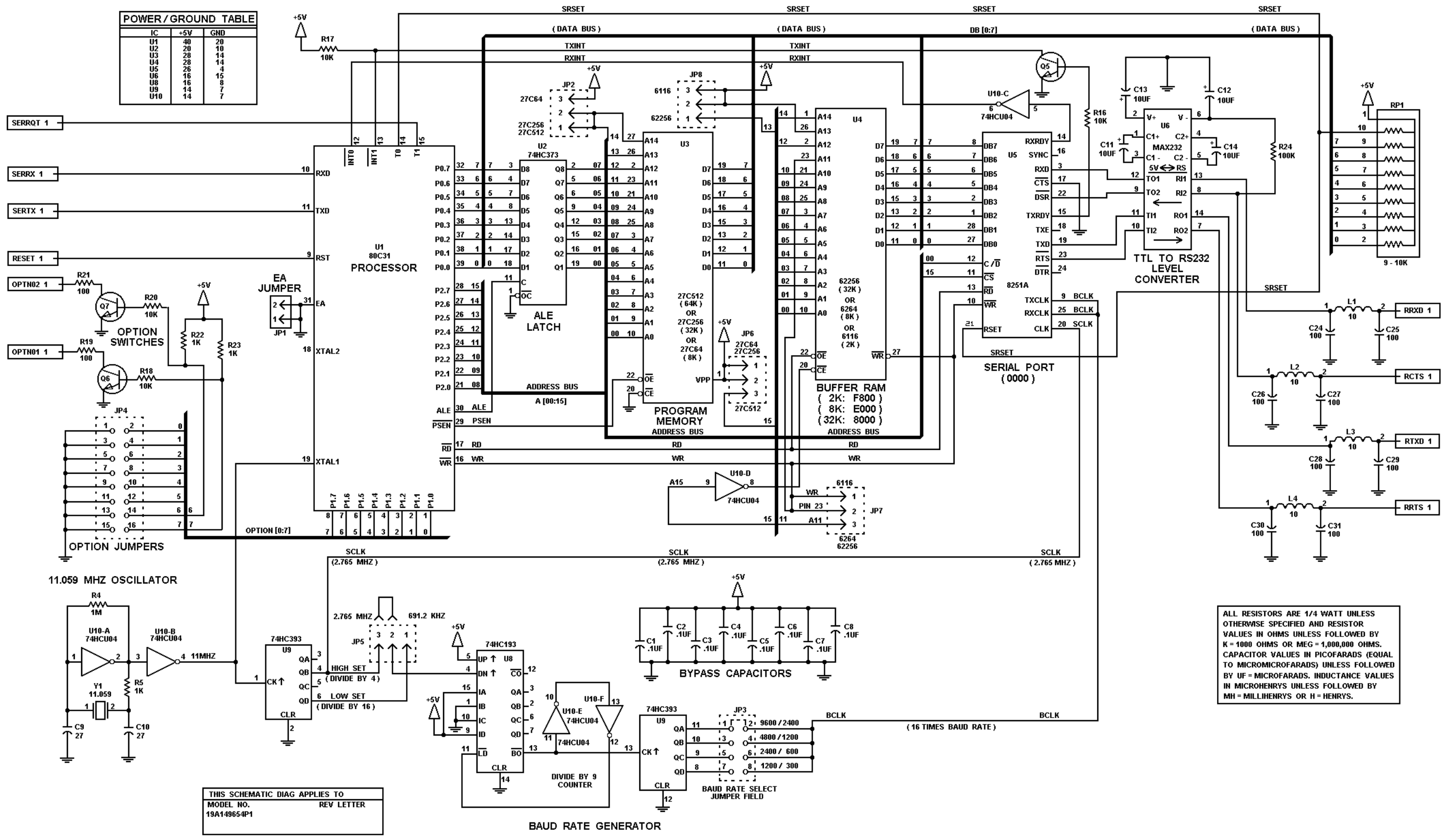


THIS SCHEMATIC DIAG APPLIES TO
MODEL NO. 19A14965AP1
REV LETTER

ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY K = 1000 OHMS OR MEG = 1,000,000 OHMS. CAPACITOR VALUES IN PICOFARADS (EQUAL TO MICROMICROFARADS) UNLESS FOLLOWED BY MICROFARADS. RESISTOR VALUES IN MILLIHENRYS OR H = HENRYS.

**RADIO DATA INTERFACE
19D902301G1**

(19D902302, Sh. 1, Rev. 1)



ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY K = 1000 OHMS OR MEG = 1,000,000 OHMS. CAPACITOR VALUES IN PICOFARADS (EQUAL TO MICROMICROFARADS) UNLESS FOLLOWED BY UF = MICROFARADS. INDUCTANCE VALUES IN MICROHENRYS UNLESS FOLLOWED BY MH = MILLIHENRYS OR H = HENRYS.

THIS SCHEMATIC DIAG APPLIES TO MODEL NO. 19A149654P1 REV LETTER

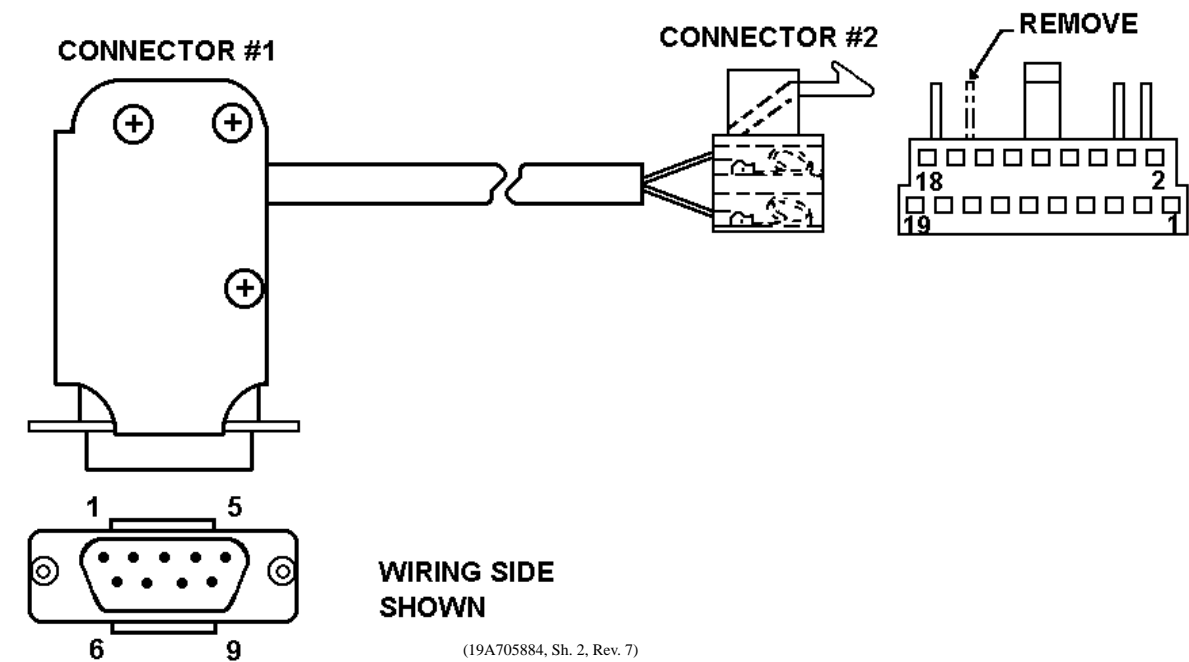
RADIO DATA INTERFACE 19D902301G1

(19D902302, Sh. 2, Rev. 1)

PARTS LIST
RADIO DATA INTERFACE OPTION
19A149654P1 & P2
ISSUE 2

SYMBOL	PART NO.	DESCRIPTION
		19D902301G1
		----- CAPACITORS -----
C1 thru C8	19A700121P6	Ceramic: 0.1 uF + or -20%, 50 VDCW.
C9 and C10	19A700231P44	Ceramic: 27 pF + or -5%, 100 VDCW.
C11 thru C14	19A703314P10	Electrolytic: 10 uF -10+50%, 50 VDCW; sim to Panasonic LS Series.
C15	19A700231P64	Ceramic: 100 pF + or -10%, 100 VDCW.
C16	19A700121P1	Ceramic: .001 uF + or -20%, 50 VDCW.
C17	19A700231P64	Ceramic: 100 pF + or -10%, 100 VDCW.
C18	19A700121P1	Ceramic: .001 uF + or -20%, 50 VDCW.
C19 and C20	19A700231P64	Ceramic: 100 pF + or -10%, 100 VDCW.
C21	19A703314P10	Electrolytic: 10 uF -10+50%, 50 VDCW; sim to Panasonic LS Series.
C22	19A703314P6	Electrolytic: 1 uF -10+50% tol, 50 VDCW; sim to Panasonic LS Series.
C23	19A703314P4	Electrolytic: 47 uF -10+50% tol, 16 VDCW; sim to Panasonic LS
C24 thru C31	19A700231P64	Ceramic: 100 pF + or -10%, 100 VDCW.
		----- DIODES -----
D1 and D2	19A700028P1	Silicon: 75 mA, 75 PIV; sim to 1N4148.
		----- FILTERS -----
FL1 and FL2	19A705217P1	Filter, EMI Suppression.
		----- JUMPERS -----
JP1	19A704852P1	Connector: 2 Pin Male Header.
JP2	19A704852P2	Connector: 3 Pin Male Header.
JP3	19A704852P3	##CONN PW
JP4	19A704852P7	##CONN PW
JP5 thru JP8	19A704852P2	Connector: 3 Pin Male Header.
		----- INDUCTORS -----
L1 thru L4	19A700024P25	Coil, RF: 10.0 uH + or - 10%, 3.70 ohms DC res max.
		----- PLUGS -----
P2	19B209727P37	Connector, plug: 9 contacts, sim to AMP 745781-4.
P3	19B209727P36	Connector, plug: 9 contacts, sim to AMP 747250-4.
		----- TRANSISTORS -----
Q1 thru Q7	19A700023P1	Silicon, NPN: sim to 2N3904.

SYMBOL	PART NO.	DESCRIPTION
		----- RESISTORS -----
R1	3R151P101J	Composition: 100 ohms + or - 5%, 1/8 w.
R2 and R3	3R151P103J	Composition: 10K ohms + or - 5%, 1/8 w.
R4	3R151P105J	Composition: 1 ohm + or -5%, 1/8 w.
R5	3R151P102J	Composition: 1K ohms + or - 5%, 1/8 w.
R6	3R151P103J	Composition: 10K ohms + or - 5%, 1/8 w.
R7	3R151P472J	Composition: 4.7K ohms + or -5%, 1/8 w.
R8 and R9	3R151P103J	Composition: 10K ohms + or - 5%, 1/8 w.
R10 and R11	3R151P101J	Composition: 100 ohms + or - 5%, 1/8 w.
R12	3R151P103J	Composition: 10K ohms + or - 5%, 1/8 w.
R13 and R14	3R151P101J	Composition: 100 ohms + or - 5%, 1/8 w.
R15	3R151P472J	Composition: 4.7K ohms + or -5%, 1/8 w.
R16 thru R18	3R151P103J	Composition: 10K ohms + or - 5%, 1/8 w.
R19	3R151P101J	Composition: 100 ohms + or - 5%, 1/8 w.
R20	3R151P103J	Composition: 10K ohms + or - 5%, 1/8 w.
R21	3R151P101J	Composition: 100 ohms + or - 5%, 1/8 w.
R22 and R23	3R151P102J	Composition: 1K ohms + or - 5%, 1/8 w.
R24	3R151P104J	Composition: 100K ohms + or -5%, 1/8 w.
		----- Resistive Network -----
RP1	19A701630P2	Resistor, network: 9 resistors rated 10K ohms + or -2%, 50 VDCW; sim to Bourns 4310R-101-103.
		----- INTEGRATED CIRCUITS -----
U1	19A704345P2	Microcomputer: CHMOS, 8 bit; sim to N80C51BH.
U2	19A703471P2	Digital: Octal Data Latch; sim to 74HC373.
U3	350A1352G1	Digital: 32K X 8 CMOS EPROM (programmed) (G1).
U3	19A149657G3	Digital: 32K X 8 CMOS EPROM (programmed) (G2).
U4	19A705558P1	Digital: 8K x 8 RAM; sim to MCM6064P-12.
U5	19A704209P2	Integrated Circuit, USART: sim to Intel ID8251A.
U6	19A149446P1	Digital: Transmitter/Receiver; sim to MAX232E.
U7	19A704970P1	Linear: 5 Volt Regulator with Reset Output; sim to SGS L387
U8	19A703987P12	DIGITAL LOGIC: Synchronous UP/DOWN Binary Counter, High Speed
U9	19A703987P13	Digital: Dual 4-Stage Binary Counter; sim to 74HC393.
U10	19A703995P1	Digital: Hex Unbuffered Inverter; sim to 74HC04
		----- SOCKETS -----
XU3	19A700156P3	Socket, IC: 28 Pins, Tin Plated.
		----- CRYSTALS -----
Y1		Quartz: 11.059200 19A702511G15
		----- MISCELLANEOUS -----
5	19B209727P10	Screwlock: No. 4-40; sim to AMP 205817-1.
6	19B235123P1	##SPT
7	19A702104P2	Connector: Shorting Jumper, Gold Plated.



(19A705884, Sh. 2, Rev. 7)

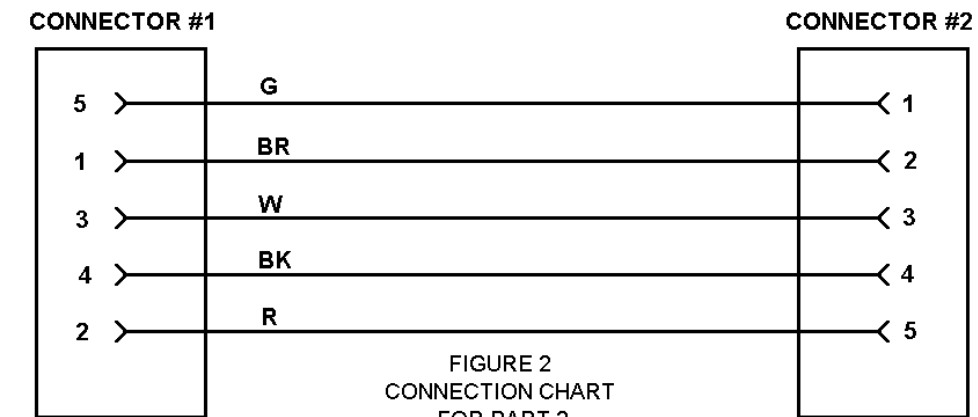
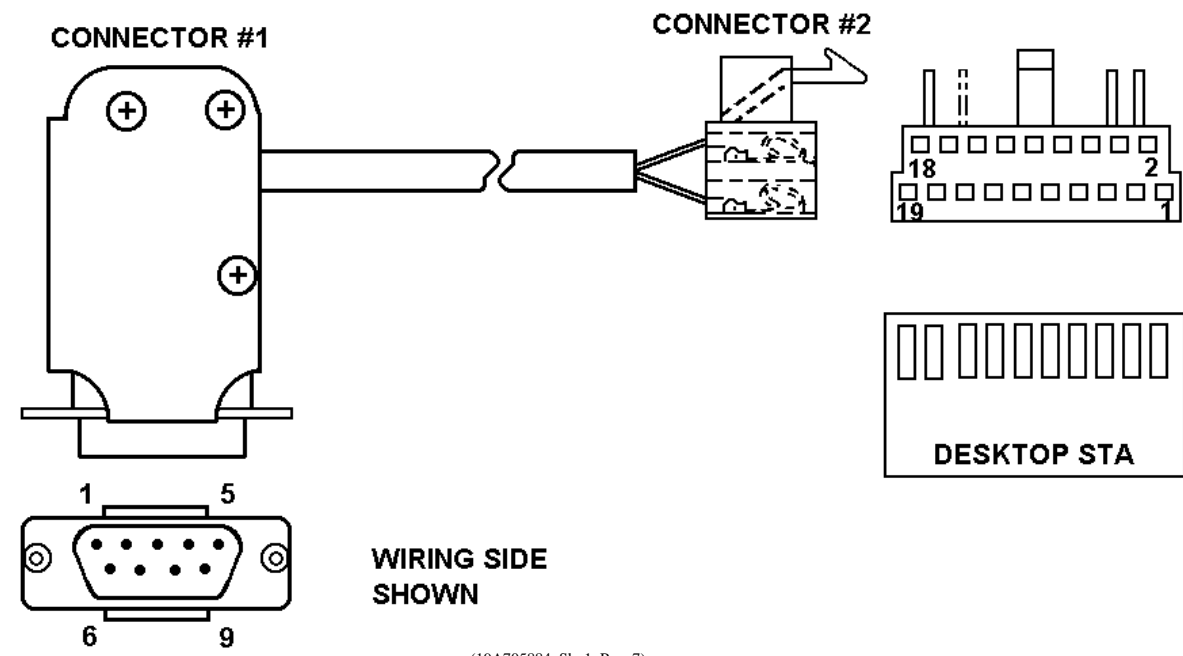


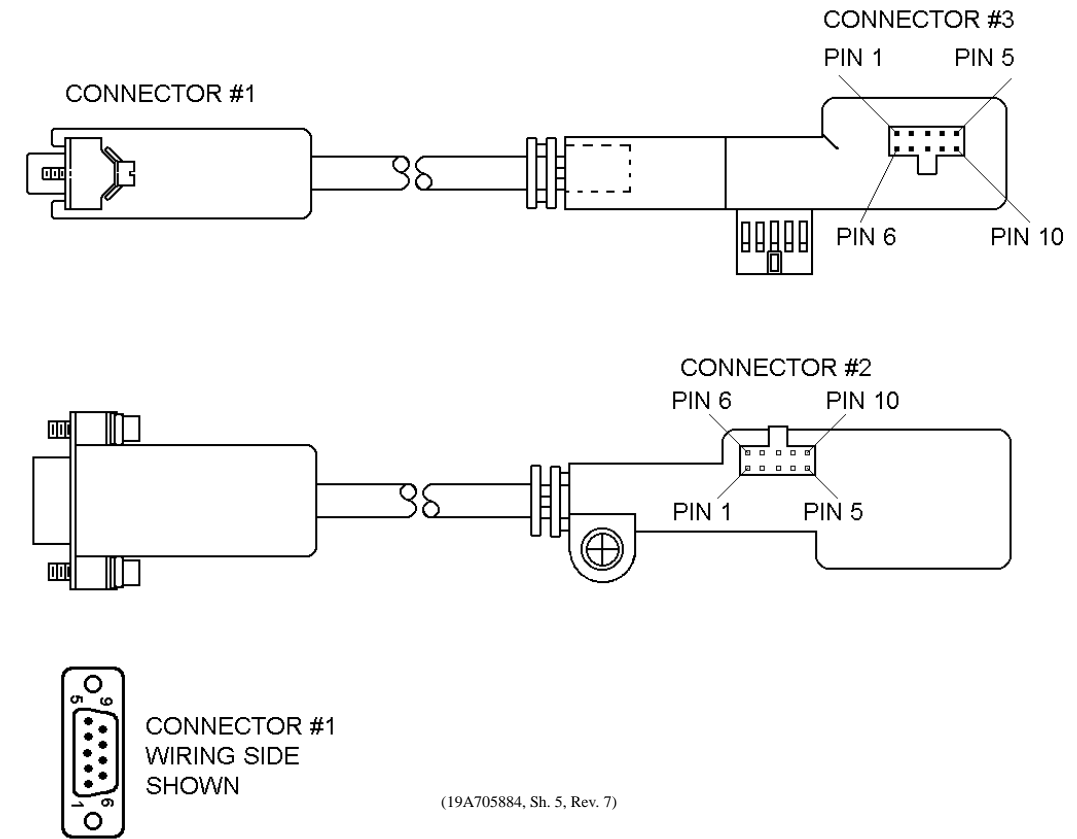
FIGURE 2
 CONNECTION CHART
 FOR PART 2

(19A705884, Sh. 4, Rev. 7)

EDACS S550 TO RDI INTERFACE CABLE
19A705884P2



(19A705884, Sh. 1, Rev. 7)



(19A705884, Sh. 5, Rev. 7)

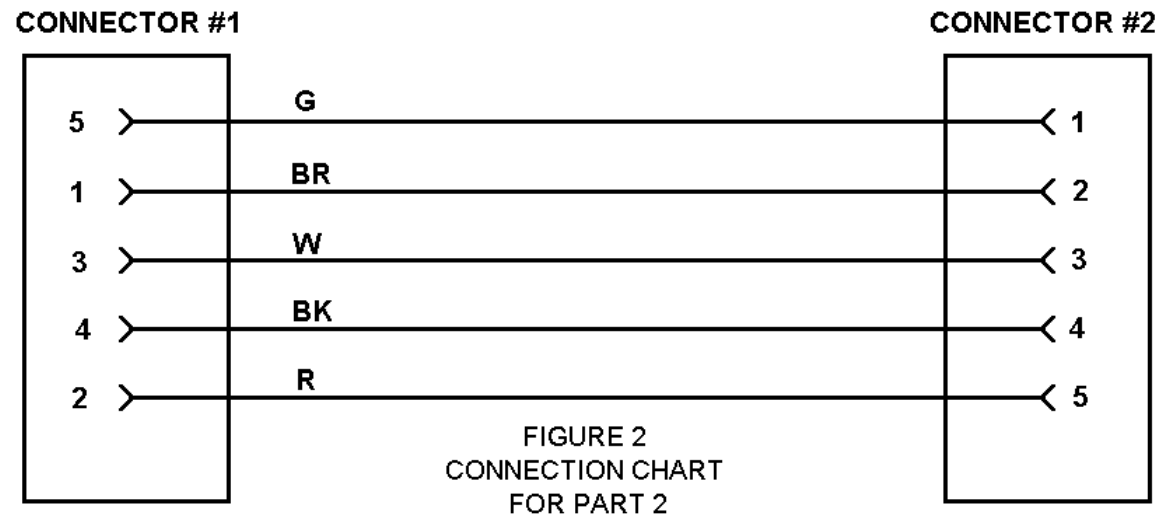


FIGURE 2
CONNECTION CHART
FOR PART 2

(19A705884, Sh. 4, Rev. 7)

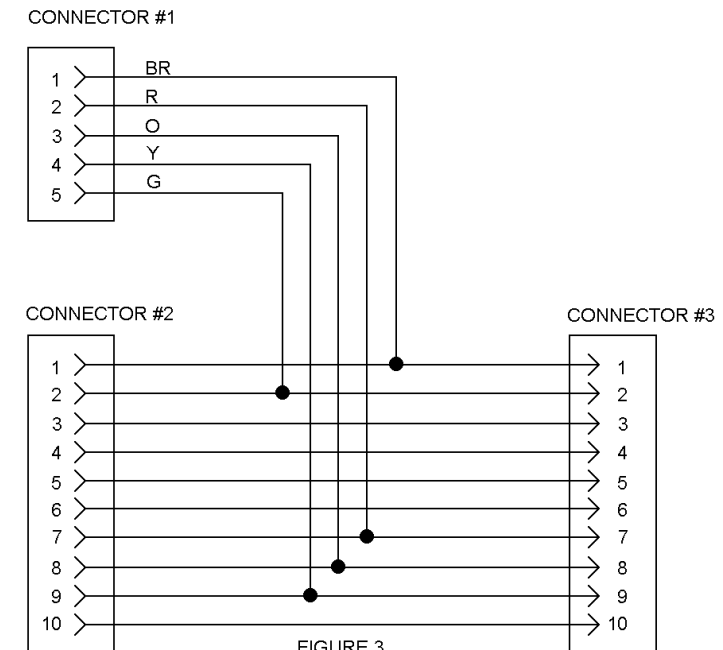
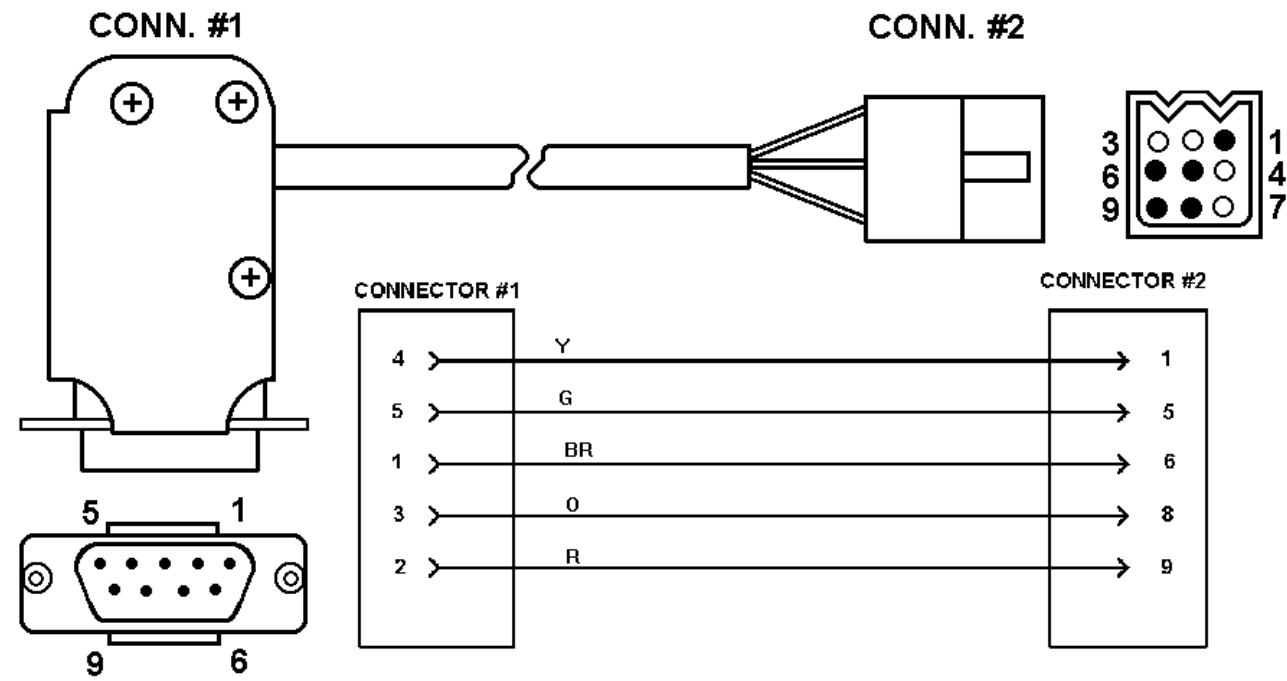


FIGURE 3
CONNECTION CHART
FOR PART 3

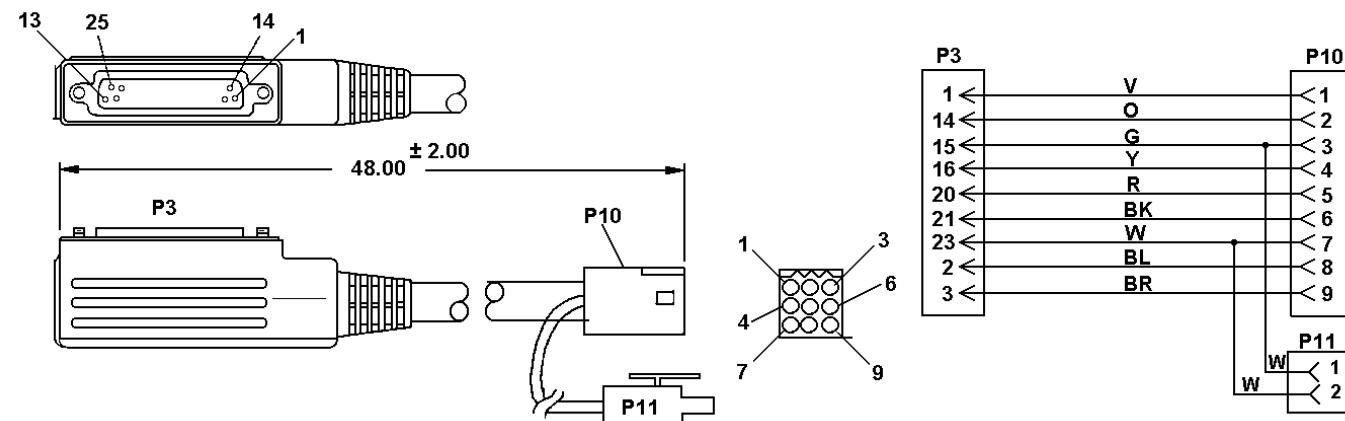
(19A705884, Sh. 7, Rev. 7)

EDACS DESKTOP STATION TO RDI INTERFACE CABLE
19A705884P1

MTD TO RDI INTERFACE CABLE
19A705884P3

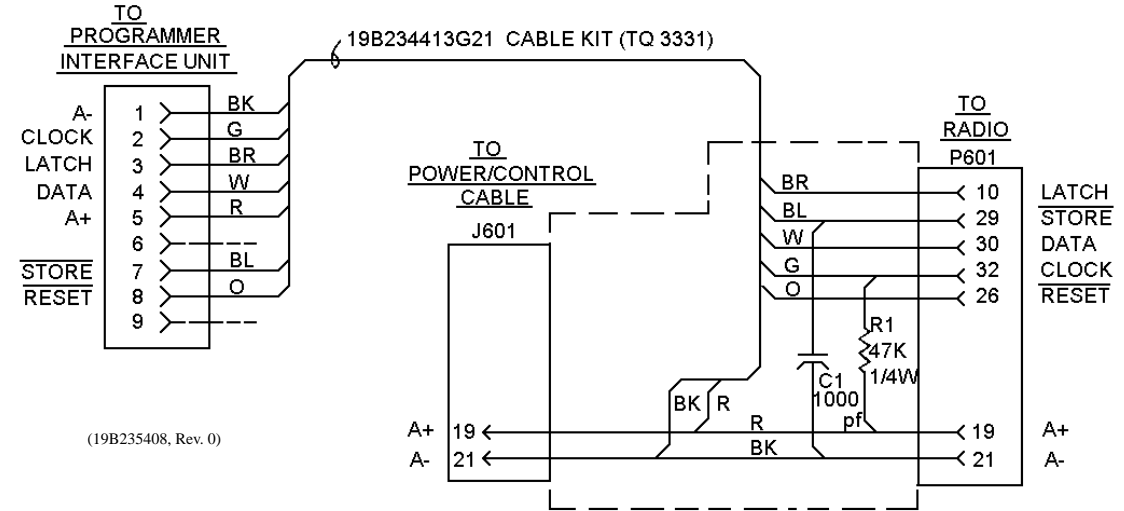
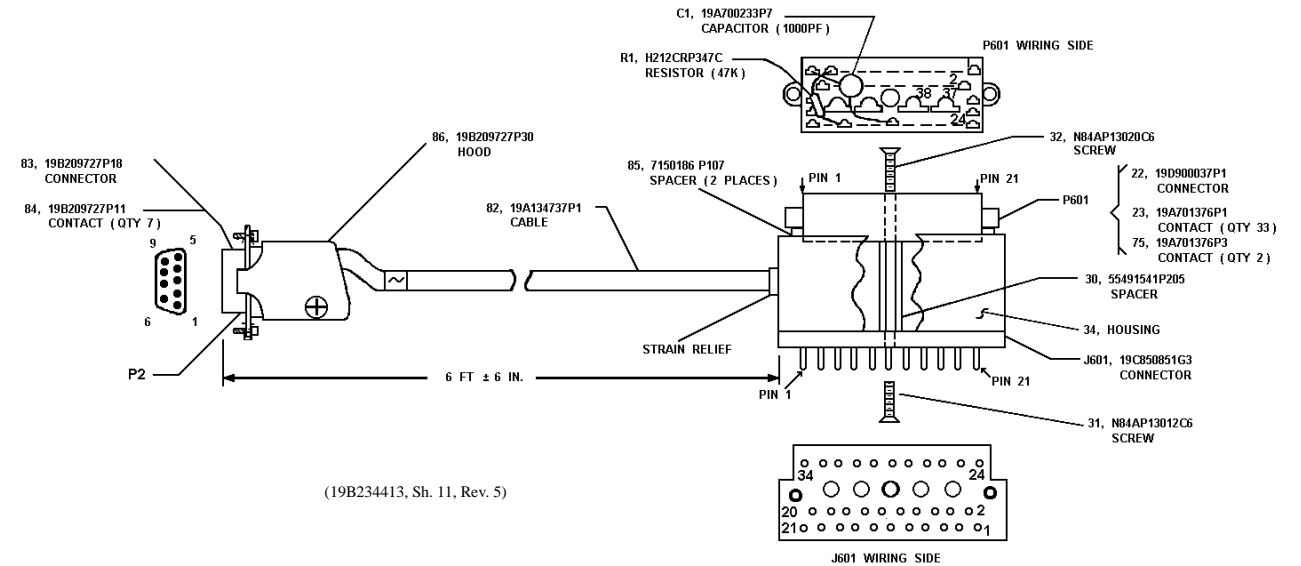


(19A705864, Sh. 1, Rev. 2)
(19A705864, Sh. 3, Rev. 2)



(19C337129, Rev. 5)

**EDACS FMD/S700 TO RDI INTERFACE CABLES
19A705864P1 & 19C337129P2**

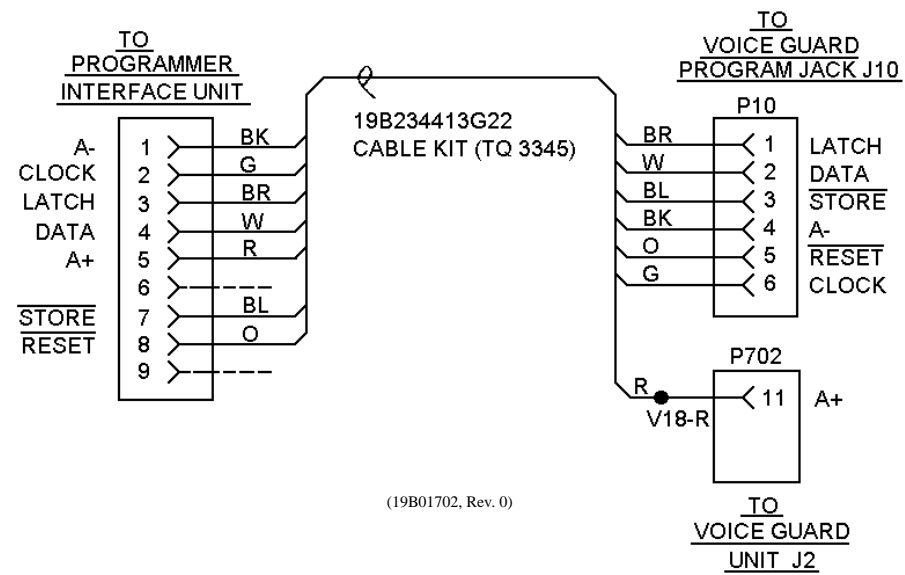
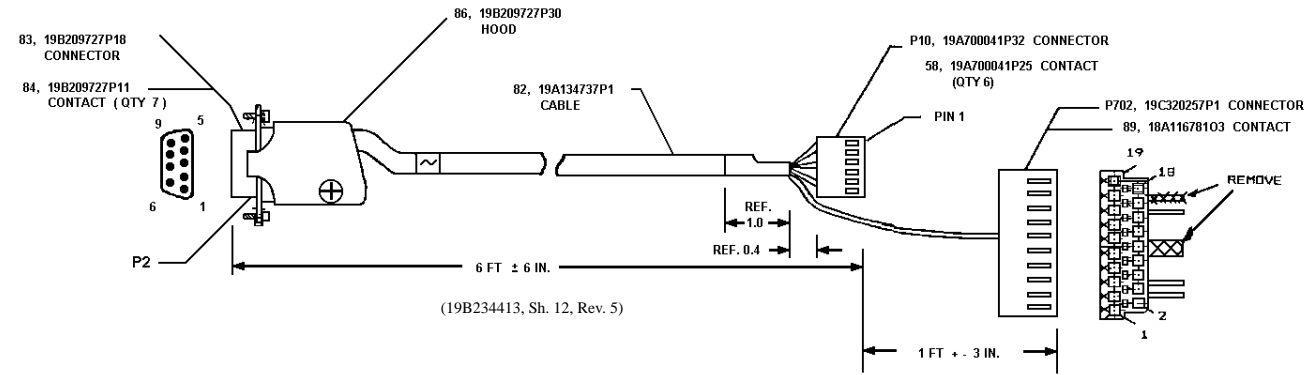


**PARTS LIST
RDI TO RADIO
19B234413G21
ISSUE 1**

SYMBOL	PART NO.	DESCRIPTION
C1	19A700233P7	----- CAPACITORS ----- Ceramic: 1000 pF + or - 20%, 50 VDCW.
J601	19C850591G3	----- JACKS ----- Connector, system:
3	19A701254P1	Contact, electrical: sim to Malco 009-0191-002.
5	19A701246G2	Connector.
	19A701254P2	Contact, electrical.
	19A702037P1	Insulator.
P2		----- PLUGS ----- CONSISTS OF ITEMS
83	19B209727P18	Connector: 9 contacts; sim to AMP 205203-1.
84	19B209727P11	Contact, electrical: sim to AMP 1-66504-0.
86	19B209727P30	Connector, plug, power.

SYMBOL	PART NO.	DESCRIPTION
P601		CONSISTS OF ITEMS
22	19D900037P1	Shell.
23	19A701376P1	Contact, electrical rated @ 4 amps; sim to AMP 350657-1.
75	19A701376P3	Contact, electrical rated @ 35 amps; sim to AMP 350655-1.
		----- RESISTORS -----
R1	H212CRP347C	Deposited carbon: 47K ohms + or - 5%, 1/4 w.
		----- MISCELLANEOUS -----
30	5491541P205	Spacer, threaded.
31	N84AP13012C6	Screw.
32	N84AP13020C6	Screw.
82	19A134737P1	Cable.
85	7150186P107	Spacer: No. 6 x 1/4.

**RDI TO RADIO PROGRAMMING CABLE
19B234413G21**

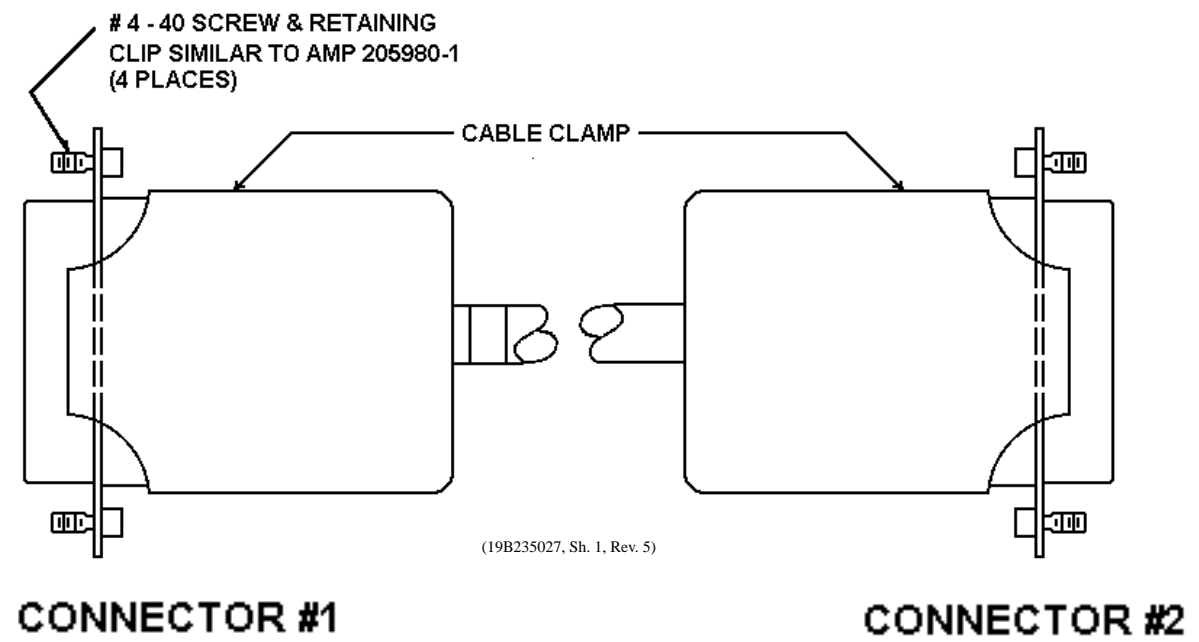


(19B01702, Rev. 0)

**PARTS LIST
PROGRAMMING CABLE
RDI TO VOICE GUARD MODULE
19B234413G22
ISSUE 1**

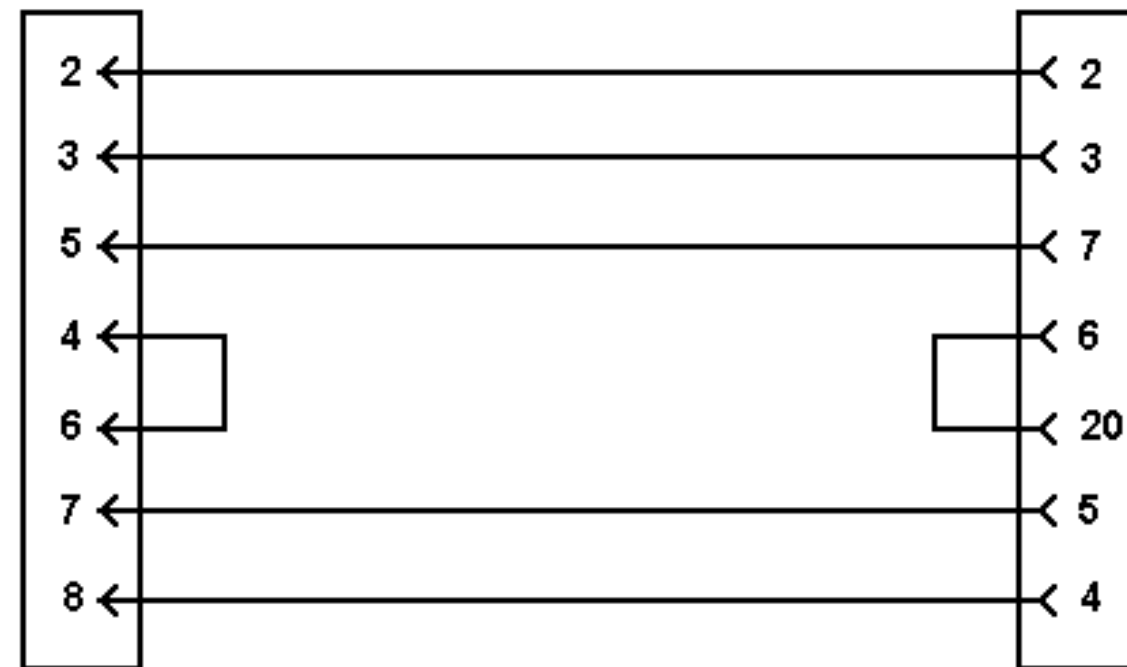
SYMBOL	PART NO.	DESCRIPTION
		----- PLUGS -----
P10	19A700041P32	Shell: 6-Position; sim to Molex 22-01-2065.
P702	19C320257P1	Shell: 19-Position; sim to Molex 15-04-0221.
58	19A700041P25	Contact; sim to molex 08-50-0114.
83	19B209727P18	Connector: 9 contacts; sim to AMP 205203-1.
84	19B209727P11	Contact, electrical: sim to AMP 1-66504-0.
86	19B209727P30	Connector, plug, power.
89	19A116781P3	Contacts: 16-20 AWG; sim to Molex 08-50-0105 (Qty. of 10).
		----- MISCELLANEOUS -----
82	19A134737P1	CABLE

**RDI TO VG-9600 PROGRAMMING CABLE
19B234413G22**



CONNECTOR #1

CONNECTOR #2



4 UNUSED WIRES

(19B235027, Sh. 3, Rev. 5)

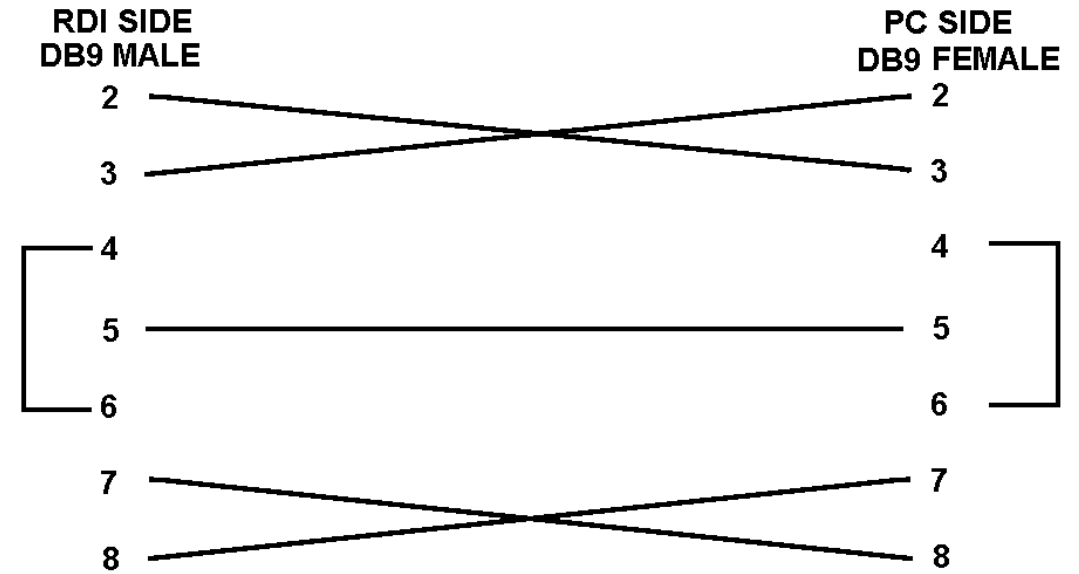
**RDI TO PC COMPUTER PROGRAMMING CABLE
19B235027P3**

Status Command Error Codes

Status Command Error Codes

RDI to PC Cables - There are two different cables to be used depending on the type of computer COM port, 9-pin or 25-pin. Here is a diagram showing the proper pin outs to build a cable:

9-PIN CONFIGURATION



25-PIN CONFIGURATION



RDI TO PC COMPUTER PROGRAMMING CABLE

00	No error.
10	Pending time-out. No assignment.
11	Dynamic regroup or system All-Call.
12	Declaring/Clearing Emergency.
13	Lost Synchronization on Control Channel.
14	Data Receiving Mobile (DRM) got request-to-send from host.
15	Convert to DRM.
16	System busy.
17	Retry limit. No assignment.
18	Generic UI radio busy error.
19	MDT timeout on RX calls.
20	Call denied.
21	PTT active.
22	Public Address (PA) mode.
23	Mobile disabled.
24	No-data state.
25	No synchronization on control channel.
26-2A	Call type not allowed.
27	MDT Convert to DRM. (Orion Only)
30	Receive pending.
31	Received assignment after pending.
32	Bridged data call.
33	Bad checksum.
34	Special code.
36	Bad packet - group call.
40	Data Originating Mobile (DOM) repeated data burst.
41	Got dropped from site.
42	Data burst after final ack.
43	Got abort from host.
44	No response from host.
45	DOM call time-out.
46	No initial synchronization on Data Channel.
47	No synchronization on Data Channel.
50	Wrong ID for DRM.

51	Wrong ID in site message.
52	Special drop from site.
53	Special drop. Not all data transmitted.
54	Got ackmap. Expected special drop.
55	Incorrect 1st data burst.
56	Message type not supported.
57	BER test.
60	Retry serial msg to/from RDI.
62	Que problems. Link error.
63	Que problems. Mobile received RTI, RST or issue.
64	Serial gives RTS, but no data in buffer.
65	Not valid Q message from mobile.
66-67	Repeat data burst error.
70	Received out of range byte from MDT/PC after Control D. (Aborts with no response.)
71	Received a 46 (retrans) from the radio. (Sends abort 43, treats message as if "aborted by radio".)
72	Waited 45 seconds for TXC or abort from radio after starting XFER to the radio. (RDI resets relevant variables and continues.)
73	Over-writing output port (TX to Radio). (RDI counts and continues.)
74	200 ms interbyte timing expired (RX from MDT/PC). (RDI aborts with no response.)
75	TX to Radio buffer full. (Accepts message from MDT/PC, but discards it.)
76	Waited 45 seconds for concluding XFER from Radio to RDI. (Resets relevant variables, discards message and continues.)
77	These are signatures, not counts and should not happen during operations. (Contact Ericsson Inc. for details.)
80	Receive message has sequence error.
81	Burst not recoverable.
82	Data call failed because of malloc error.
83	Data mode canceled by UI.
84	Three consecutive bad ack maps (all 0's).
85	Group call failed.
91	Voice convert to callee.