

# MAINTENANCE MANUAL

## UHF REAR COVER ASSEMBLY

### 19C337097G4 - G7, G11

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#### DESCRIPTION

The Rear Cover Assembly consists of the UHF RF Board, a die-cast aluminum case and the associated hardware. The RF Board assembly includes soldered-in modules, integrated circuits and surface-mounted components. This

double-sided printed-wire board is surrounded by a die-cast aluminum casting and mounted in the rear cover case. This arrangement provides excellent RF shielding between the various circuits and the outside environment. A cover shield provides shielding between the RF Board and the digital circuits located in the front cover.

Table 1 - Applications

OPERATING RF BAND (MHZ)	FACTORY TUNED FOR (MHZ)	REAR COVER ASSEMBLY	RF BOARD	PRODUCT
378 - 413	378 - 413	19C337097G11	19D902282G10	P400
403 - 440	403 - 423	19C337097G4	19D902282G1	M-PA
440 - 470	450 - 470	19C337097G5	19D902282G6	M-PA, MTL
470 - 494	470 - 492	19C337097G6	19D902282G3	M-PA
492 - 514	492 - 512	19C337097G7	19D902282G8	M-PA

## CIRCUIT ANALYSIS

The RF Board is electrically connected to the Control Board by two single-in-line connectors. Power supplies include 7.5 Vdc (battery power) and a regulated 5.4 Vdc supply from the Control Board located in the Front Cover Assembly.

Logic inputs from the Control Board include serial synthesizer loading data, power-save, and a switched 5.4 Vdc source to enable the transmitter and disable the receiver circuits. Other signals from the Control Board include modulating audio and the transmitter power level set line when a transmission is enabled.

The RF Board provides the FM demodulated audio and synthesizer lock status to the Control Board. During transmitter operation RF power appears at the top antenna jack or the UDC jack if an appropriate adapter is inserted.

### ANTENNA SWITCH AND LOW-PASS FILTER

The antenna switch, located at the top of the RF Board, selects the top mounted antenna or a UDC antenna option. A spring-loaded contact in the switch normally connects the low-pass filter to the top mounted antenna. When a UDC accessory (or an RF test plug) that utilizes the UDC antenna jack is installed, RF is routed to/from the UDC antenna jack instead of the top jack. Connecting an accessory to the UDC jack pushes the small gold plated center pin inside the unit, switching the filter from the top antenna jack to the UDC antenna jack.

Low-pass filter consists of capacitors C1 - C7, C14, C72 and inductors L1 - L4. L1 provides a dc path to ground for the antenna. This LC network rejects unwanted harmonics in the received and transmitted signal. The network has a rejection of more than 65 dB in the stopband. The filter has input and output impedances of 50 ohms.

### T/R SWITCH DIODES

Antenna T/R switch diodes connect the transmitter's output or the receiver's input to the low-pass filter (and antenna) during transmit and receive modes respectively. Two pin diodes are biased by the TX 5.4V line to route the RF properly.

When the radio is transmitting, the diodes are forward-biased by a high level (5.4 Vdc) on the TX 5.4V line. RF power from the transmitter (Power Controller module pin 14) passes through D1 to the low-pass filter network and the antenna. Forward-biased D2 prevents any transmit RF from entering the receiver by providing a low-impedance path to ground at the

receivers input. Network C36, C37 and L9 serves to attenuate transmitter power before it reaches D2. The two diodes are forward biased by the following dc path: TX 5.4V line, R53, R1, L5, D1, L9, D2 and ground.

In receive mode, with TX 5.4V low (both diodes off), RF from the antenna and is routed to the receiver's front-end.

### TRANSMITTER

The UHF transmitter circuit includes the Power Amplifier IC, the Power Controller module and support circuitry for these components. The Power Controller module regulates the radio's RF power by sampling the power being delivered to the antenna from the PA IC, and controlling the PA accordingly.

In order to transmit, the Control Board in the front cover must supply the following signals to the RF Board:

- the synthesizer must be loaded and locked with the proper TX frequency data via STROBE, DATA and ENABLE
- J101 pin 5 (TX 5.4V) must be high (5.4 Vdc)
- J101 pin 1 (PWR SET) must be set to a level corresponding to the programmed power level (high or low)
- modulating audio must be present on J102 pin 1

### Power Amplifier IC U4

Power Amplifier IC U4 is a four-stage device mounted to the "eggcrate" casting. This casting serves as a heat sink. U4 provides approximately 36 dB gain for the transmitter. RF drive is applied to pin 1 from the VCO. The IC's output is on pin 7.

Battery power for the PA is sourced from the 7.5V BATT line via L6, L7, L8, L16, L17, Q1 and Q4. The associated LC networks provide decoupling.

Transistor Q4 turns on when the radio is transmitting to supply 7.5 Vdc ( $\pm 20\%$ ) to U4 pins 2 and 4. Transistor Q1 supplies dc power to U4 pin 3. Q1 operates in a linear mode to regulate RF power as driven by the Power Controller.

### Power Controller Module A1

Power Controller A1 regulates the RF output power as set by the programmed power level. This module maintains constant output power despite battery voltage variations or tem-

perature related gain variations of the PA. Operating power for this module is supplied from the TX 5.4V line when a transmission is enabled.

RF enters A1 at pin 1 and exits at pin 14 at a loss of 0.1 dB. A microstrip directional-coupler inside the module samples the RF power. This signal is then rectified and compared to the PWR SET line from the Control Board; an error signal is produced which drives transistor Q1 to control the PA IC's gain. This feedback method of power control maintains constant RF output power as set by the digital-to-analog converter on the Control Board.

The PWR SET signal from J101 pin 1 is decoupled by R31, C83 and C65 and applied to the Power Controller at pin 12. This dc reference level varies from approximately 1 Vdc (low power) to 4 Vdc (high power). In receive mode, PWR SET is 0 Vdc.

#### NOTE

Outline and schematic diagrams for the modules are shown in the Service Section. The modules are not serviceable; schematics and outlines are given as a troubleshooting aid only.

### Harmonic Filter

Transmit VCO drive from A4 is connected to the PA by a harmonic filter network that has a rejection of more than 35 dB in the stopband. Capacitor C15 couples the drive to the PA module.

### RECEIVER

The receiver utilizes the dual-conversion superheterodyne technique to recover the desired signal. Low-side injection from the synthesizer circuit produces a high IF frequency of 45 MHz at the output of the first mixer. The second mixer uses high-side injection from a crystal oscillator to produce the desired second IF of 455 kHz. LC and crystal filters are incorporated throughout the receiver circuit. This arrangement produces excellent sensitivity, selectivity and image rejection.

### Front-End

Capacitor C35 couples RF from the low-pass input filter and T/R switch circuit to Bandpass Filter FL4. FL4 is a

passive LC network that provides front-end image frequency protection. The filter has an insertion loss of less than 4 dB in the passband. RF is then passed to RF Amp A6.

Module A6 is a common-emitter configured RF amplifier module that serves as a preamplifier before the mixer circuit. It provides approximately 8 dB of gain and has terminal impedances of 50 ohms. The module consumes less than 4 milliamperes of current from the decoupled supply on pin 5. A6's output is applied to FL1 pin 1.

Bandpass Filter FL1 is a three-pole LC device identical to FL4 (within each band-split). Both filters are factory tuned to cover the operating frequency range of the radio. See Table 1 for details.

RF from FL1 enters double balanced First Mixer U5 at pin 1. Synthesized VCO injection (at 7 dBm) from A4 pin 9 is applied to U5 pin 8. The 45 MHz converted signal appears on pins 3 and 4 at a maximum conversion loss of 7 dB. Impedances at all ports is 50 ohms. C45 and L13, series tuned to 45 MHz, couple the converted signal to the High IF Amp.

### High IF Amp, Crystal Filter and Buffer

High IF Amplifier A2 is a single transistor, common-base, non-tunable transistor amplifier module. Center frequency is 45 MHz and the IF signal is introduced on pin 2. This module has input and output impedances of 50 ohms. The amplified signal is applied to FL2 by pin 5.

High IF Filter FL2 is a monolithic crystal filter with a center frequency of 45 MHz. It has a 3 dB bandwidth of  $\pm 7.5$  kHz minimum and terminal impedances of 50 ohms. Loss in the passband is 4 dB maximum. The filter's output is coupled to IF Buffer Amp Q3 by C10. The LC network (L12//C57//C10) at pin 2 is tuned to the IF frequency.

High IF Buffer Amp Q3 is a common-base non-tunable amplifier stage. This stage matches the low impedance output of FL2 to the high impedance input of U6.

### Back-End

The back-end circuits perform second conversion and demodulation of the FM signal. Capacitor C56 couples the 45 MHz IF signal from Q3 to pin 16 of U6.

Integrated circuit U6 is a 16-pin DIP IC that contains an oscillator, mixer, limiter, demodulator and audio amplifier. Using external crystal Y1, a 45.455 MHz signal is generated in the IC for the second mixer high-side injection. Alignment for this 2nd LO is provided by coil T1.

The mixer's output from U6 pin 3 passes through 455 kHz filter FL3. This filter has an input and output impedances of approximately 1500 ohms with a stopband attenuation of 35 dB minimum. It has an insertion loss of 4 dB and a center frequency of 455 kHz  $\pm$  1.5 kHz. The 455 kHz output signal from FL3 is returned to U6's limiter input pin 5.

The limiter stage in U6 is internally connected to the demodulator stage. Alignment for the internal quadrature detector is provided by coil T2. The recovered audio is available on U6 pin 9. Audio is applied to J101 pin 4 for passage to the audio circuits in the Front Cover Assembly. Deemphasis is performed by C44 and R28.

## SYNTHESIZER

The microprocessor-controlled phased-locked loop (PLL) synthesizer produces the transmitter's drive and the receiver's first mixer injection. Primary components include a stable reference oscillator, a voltage-controlled oscillator (VCO), a dual-modulus prescaler chip and a serially-loaded synthesizer chip. A PLL filter module integrates the analog error signal from the synthesizer chip before it is passed to the VCO.

### Reference Oscillator U3

Reference Oscillator U3 produces a 13.2 MHz crystal reference frequency for the synthesizer chip. Capacitors C16 and C54 couple this reference signal to the synthesizer chip. The synthesizer chip phase compares this reference signal to the divided VCO signal; it produces an error signal which tunes the VCO. During a transmission, audio signals from TX AUDIO are ac coupled to U3 via C30. These audio signals frequency modulate the 13.2 MHz signal. Modulation Balance potentiometer R18 is adjusted for best low-frequency response with a 20 Hz, 1 Vp-p square-wave TX AUDIO input. TX AUDIO is also coupled to the VCO to provide modulation.

Regulated 5.4 Vdc is applied to pin 3 by R12. Capacitor C27 provides the necessary supply decoupling for the oscillator.

U3 has a small opening on the top which provides access to an internal frequency adjustment. This oscillator is factory aligned and it is highly stable. It should not normally need alignment in the field.

### Voltage-Controlled Oscillator Module A4

VCO module A4 is the largest and most complex module on the RF Board. This module has separate internal TX

and RX oscillators which generate the transmitter drive and receiver first LO injection signals. When TX 5.4V is high, the TX oscillator is enabled and the RX oscillator is disabled. Output frequency for both oscillators is controlled by the tuning voltage on pin 5. The VCO module is factory tuned to cover the operating frequency range of the radio.

A regulated power supply of 5.4 Vdc is delivered to A4 pin 7. This supply is developed from the regulator circuit in A5A. R32 and C52 decouple this supply.

The VCO also requires a negative power supply for operation. This supply is generated from the OSC OUT of U1. On the positive cycle of OSC OUT, C47 charges through R34 and D3 (pins 1 - 3). When OSC OUT returns low, C47 charges C48 via R34 and D3 (pins 2 and 3). R35 and C49 provide additional filtering. Approximately -3.7 Vdc is present on A4 pin 6.

In transmit mode the VCO is phased-locked to the TX channel's frequency. RF drive from A4 pin 1 is approximately 8 dBm. Table 2 lists tuning voltage data.

TX AUDIO frequency modulates the VCO. VCO Modulation potentiometer R19 sets the modulation level into the VCO from the TX AUDIO line. The pot is aligned so a 1 kHz, 600 mV rms TX AUDIO input will produce a deviation of 5.0 kHz.

In receive mode, the VCO is phased-locked 45 MHz below the RX channel's frequency. This LO signal is applied to the mixer and prescaler IC. Table 2 lists tuning voltage data.

Table 2 - VCO Tuning Voltage VS. VCO Output Frequency

TUNING VOLTAGE (AT A4 PIN 5)		2.5 VDC
TOLERANCE		$\pm$ 2.0 MHZ
378 - 413 MHz	TX RX	396.0 MHz 351.0 MHz
403 - 440 MHz	TX RX	413.0 MHz 368.0 MHz
440 - 470 MHz	TX RX	460.0 MHz 415.5 MHz
470 - 494 MHz	TX RX	482.0 MHz 437.0 MHz
492 - 514 MHz	TX RX	503.0 MHz 458.0 MHz

### Prescaler Stage

The VCO signal is buffered by common-emitter configured Q2 and applied to prescaler chip U2 via C20. Q2 prevents loading of the VCO by the prescaler chip. This dual-modulus prescaler divides the VCO signal by 128 or 129 according to the logic signal on the modulus control input (MC, pin 1). This modulus is controlled by U1; the chip divides-by 128 when the MC is high.

### Synthesizer IC U1

Integrated circuit U1 contains a reference frequency divider, variable frequency dividers and phase detectors for the synthesizer circuitry. This IC has an analog and a digital phase detector. The analog detector is incorporated in the main PLL and the digital detector output indicates lock status. Reference and variable frequency dividers are serially loaded by the clocked data line from the microprocessor. This IC controls the dividing factor of the prescaler by its modulus control (MC, pin 8) output.

Serial data from the microprocessor is shifted into U1 by the DATA line, J102 pin 10. Clocking is provided on the STROBE line, J102 pin 11, and the data is latched with the ENABLE pulse on J102 pin 9. When U1 pin 13 (LE) is high, data is transferred from the internal shift registers to the dividers; low inhibits the internal transfers. The tuning error signal from the analog phase detector appears on ALOG OUT, U1 pin 17. This tuning error signal is routed to PLL Filter A5B for additional filtering before it is applied to the VCO.

The digital phase detector's output on pin 9 is sent to the Control Board via J102 pin 8, LOCK DETect. The microprocessor checks this output to prevent transmission when the VCO is not locked. During an unlocked condition, LOCK DET is low or pulsing.

### Voltage Regulator / Loop Filter Module A5

Module A5 has two functions. It provides switched supplies to the RF Board and it contains circuitry which provides additional filtering for the VCO tuning signal. Regulated 5.4 Vdc from J102 pin 6 is applied to A5 pin 7 and 7.5 Vdc  $\pm$  20% (battery power) is applied to pin 11.

A5A supplies regulated 5.4 Vdc to the synthesizer's circuitry and the back-end circuits via pins 9 and 10 respectively. In addition, 7.5 Vdc is supplied to the RF and IF amplifier modules via A5A pin 12.

A5B provides further filtering of the tuning error signal from the synthesizer chip before it is applied to the VCO. Inside the module, an active filter circuit integrates the tuning error signal from the synthesizer chip. Pin 4 is driven by the ENABLE line. When high, the response time of the filter circuit is decreased. This allows the synthesizer to lock quickly when new data is loaded into U1. Capacitor C25 is the primary integrating capacitor and C26 on A5B's output provides further integration of the tuning error signal before it is applied to the VCO.



Table with columns: SYMBOL, PART NUMBER, DESCRIPTION. Rows include various ceramic capacitors (C80, C81), tantalum capacitors (C100\*), diodes (D1, D2, D3), filters (FL1, FL2, FL3, FL4), jacks (J101, J102), and inductors (L1, L2, L3).

Table with columns: SYMBOL, PART NUMBER, DESCRIPTION. Rows include various coils (L3-L19, L20), transistors (Q1, Q2, Q3, Q4, Q5\*), resistors (R1-R7), and other components.

Table with columns: SYMBOL, PART NUMBER, DESCRIPTION. Rows include various resistors (R8-R78), switches (SW1A, SW1B, SW1C), and other components.

Table with columns: SYMBOL, PART NUMBER, DESCRIPTION. Rows include transformers (T1, T2), integrated circuits (U1-U6), crystals (Y1), RF board miscellaneous parts (6-11), rear cover assembly miscellaneous parts (2, 3, 4, 5, 6, 7), and other miscellaneous components (12-14).

**REAR COVER  
19B801598G1  
ISSUE 2**

SYMBOL	PART NUMBER	DESCRIPTION
		--- MISCELLANEOUS ---
2	19B235075P2	Plate, Receptacle.
3	N327P9009Y6	Rivet. (Qty = 4)
4	19D902730P1	Gasket, Outer Seal.
5	19A705728P1	Screw, Machine: Torx T6 Oval Head; M2.6 x 14. (Secures Front and Rear Cover Assemblies, qty = 2).
6	19A705728P2	Screw, Machine: Torx T6 Oval Head; M2.6 x 23. (Secures Front and Rear Cover Assemblies, qty = 2).
7	19A701365P7	Washer. (Used with above Screws, qty = 4).
8	19C851743P1	Cover.

\* COMPONENTS, ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

**PRODUCTION CHANGES**

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

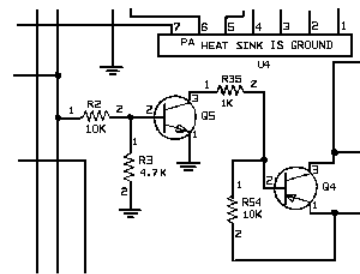
**REV. A - RF BOARD 19D902282G6**  
Incorporated changes necessary for the release of the 19D902282G1, G3 and G8 RF Boards.

**REV. A - REAR COVER ASSEMBLY 19C337097G7**  
**REV. A - RF BOARD 19D902282G8**  
To improve transmitter performance, made the following changes in the harmonic filter circuit between the VCO and PA IC: added C84 and deleted R4, R5, R6, R48 and R49. Earlier components were:  
R4 19B801251P182 Metal film: 1.8K ohms ±5%.  
R5 19B801251P5R6 Metal film: 5.6 ohms ±5%.  
R6 19B801251P182 Metal film: 1.8K ohms ±5%.  
R48 19B801251P182 Metal film: 1.8K ohms ±5%.  
R49 19B801251P182 Metal film: 1.8K ohms ±5%.

**REV. A - REAR COVER ASSEMBLY 19C337097G4 - G6**  
**REV. A - RF BOARD 19D902282G1 & G3**  
No changes.

**REV. B - REAR COVER ASSEMBLY 19C337097G4 - G7**  
**REV. B - RF BOARD 19D902282G1, G3, G6 and G8**  
To improve transmit power control circuitry, removed driver transistor Q5 and added diode D4. Also removed R2 and R3 and changed C65, C83 and R39. Earlier components were:  
C65 19A702052P14 Ceramic: 0.01 µF ±10%, 50 VDCW.  
C83 19A702052P14 Ceramic: 0.01 µF ±10%, 50 VDCW.  
Q5 19A700076P2 Silicon, NPN: sim to MMBT3904.  
R2 19B801251P103 Metal film: 10K ohms ±5%.  
R3 19B801251P472 Metal film: 4.7K ohms ±5%.  
R39 19B801251P102 Metal film: 1K ohms ±5%, 1/10 w.

Earlier (Rev. A) schematic was:



**REV. C - REAR COVER ASSEMBLY 19C337097G4 - G7**  
**REV. C - RF BOARD 19D902282G1, G3, G6 and G8**  
To improve squelch operation at high operating temperatures changed 455 kHz IF filter FL3 from 19B801021P2 to 19B801021P1.

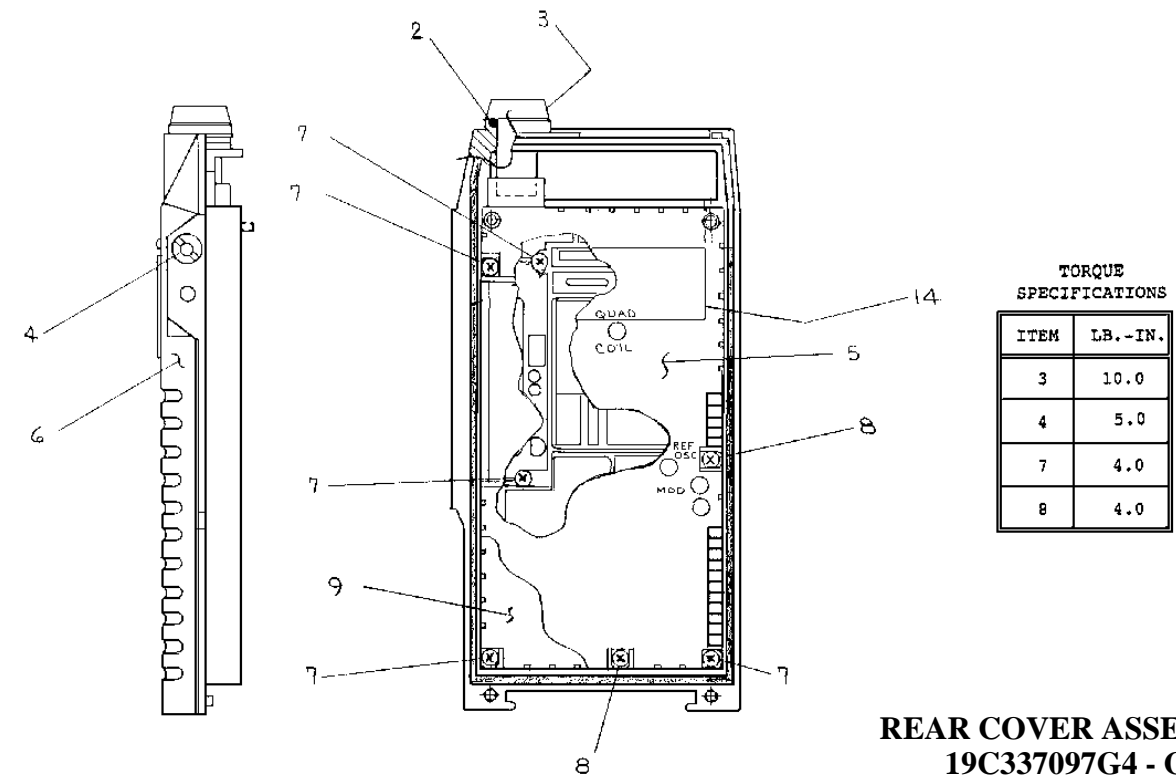
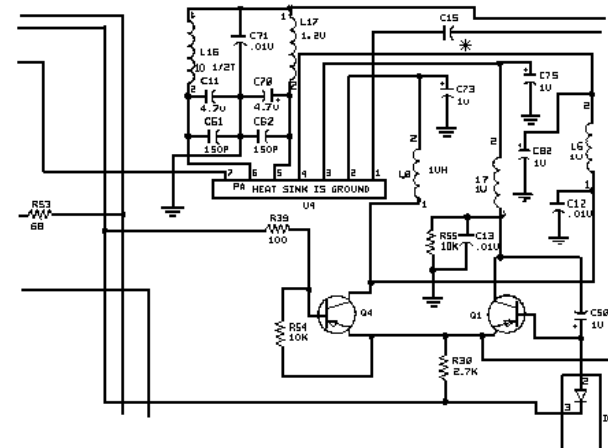
**REV. D - RF BOARD 19D902282G1, G3, G6 and G8**  
**REV. A - RF BOARD 19D902282G10**  
To improve production process, changed C17, C18, C49, C52, C63, C64, C73, C75 and C82 from polarized tantalum capacitors (19A705205P2) to non-polarized ceramic capacitors (344A3431P1). Also changed C41 - C43 from 19A702052P26 to 19A702052P34.

**REV. B - RF BOARD 19D902282G10**  
No change.

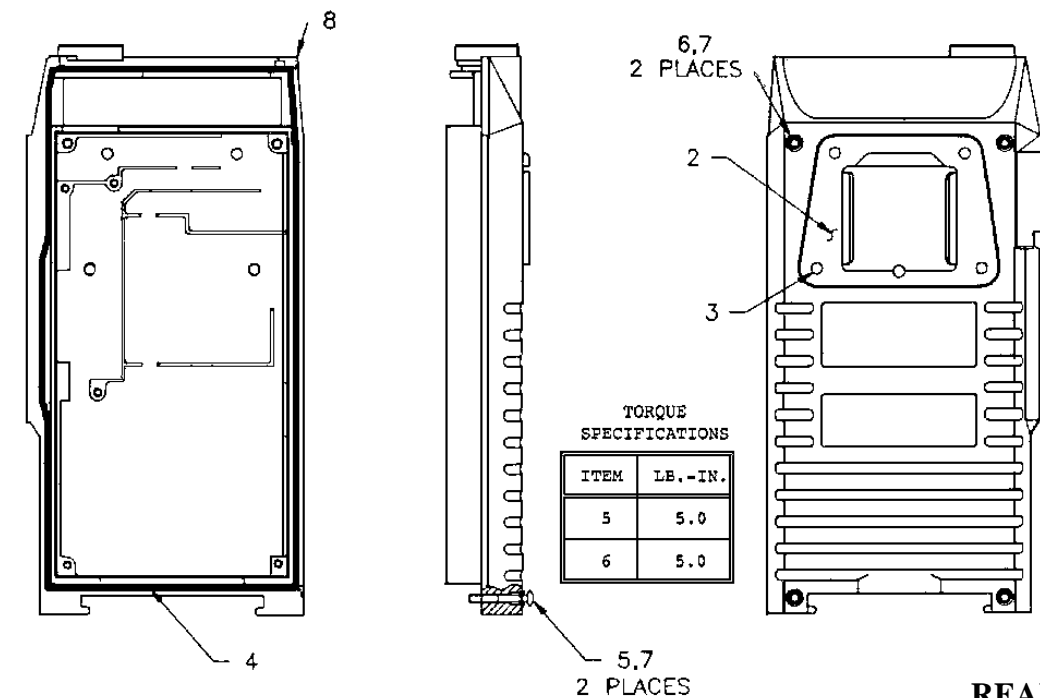
**REV. C - RF BOARD 19D902282G10**  
No change.

**REV. D - RF BOARD 19D902282G10**  
No change.

**REV. D - REAR COVER ASSEMBLY 19C337097G4 - G7**  
**REV. E - RF BOARD 19D902282G1, G3, G6, G8, G10**  
To improve operation, changed A5 from 19C852056G1 to 19C852056G3, changed C83 from 1000 pF (19A702052P5) to .1 µF (19A702052P34), added C100, deleted D4 (19A702525P2) and added Q5. Also changed R11 (G1 and G10 only) from 33K ohms (19B801251P333) to 100K ohms (19B801251P104), changed R11 (G3, G6 and G8 only) from 27K ohms (19B801251P273) to 100K ohms (19B801251P104), changed R30 from 2.7K ohms (19B801251P272) to 1K ohms (19B801251P102), and changed R39 from 100 ohms (19B801251P101) to 1K ohms (19B801251P102). In addition, added R75 - R78. Earlier transmit power control circuitry schematic was:

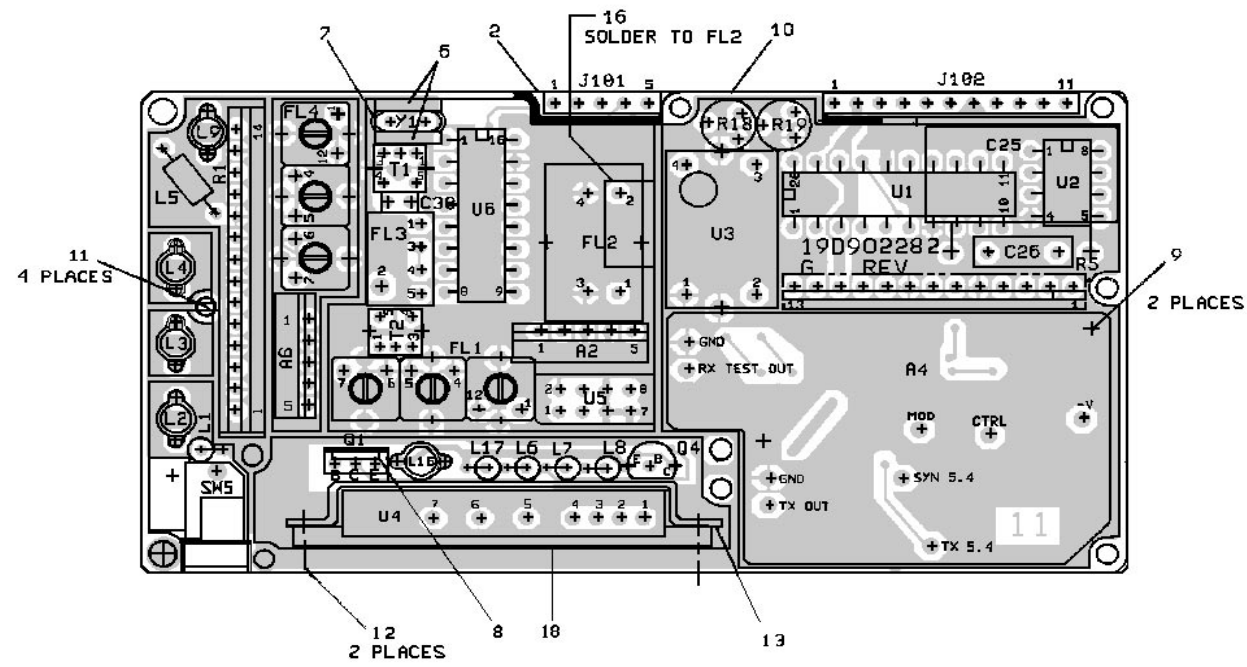


**REAR COVER ASSEMBLY  
19C337097G4 - G7, G11**  
(19C337097, Sheet 1, Rev. 6)

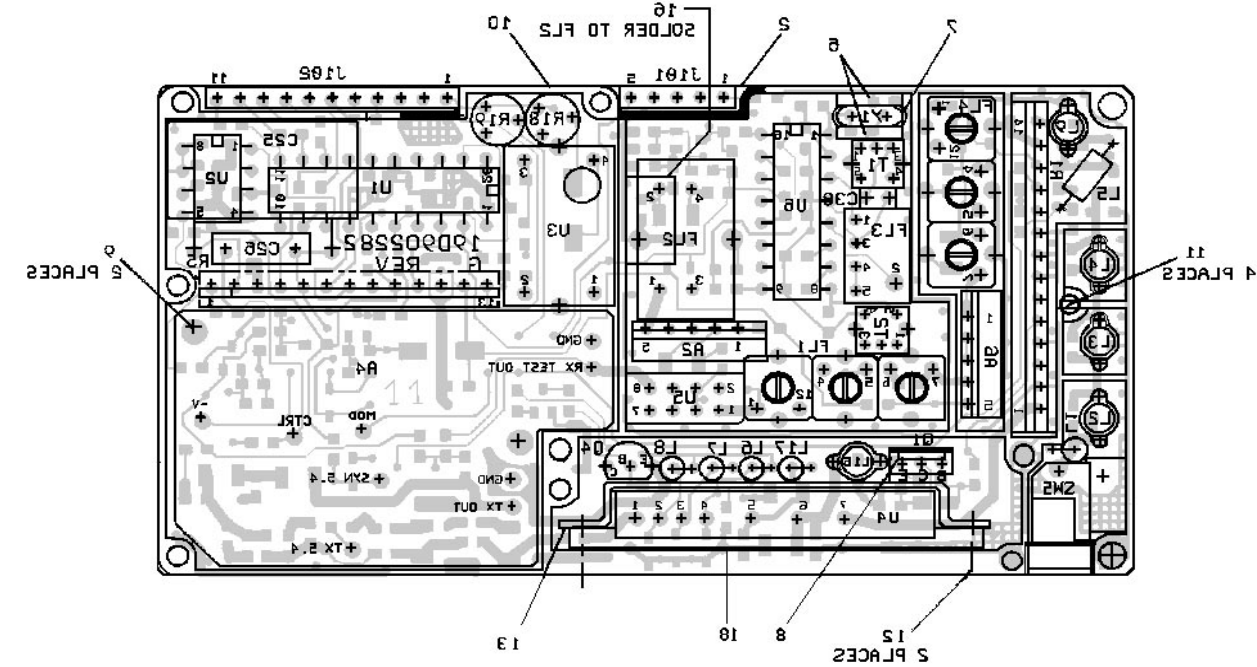


**REAR COVER  
19B801598G1**  
(19B801598, Sheet 1, Rev. 6)

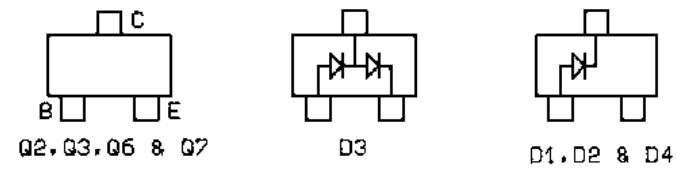
COMPONENT SIDE



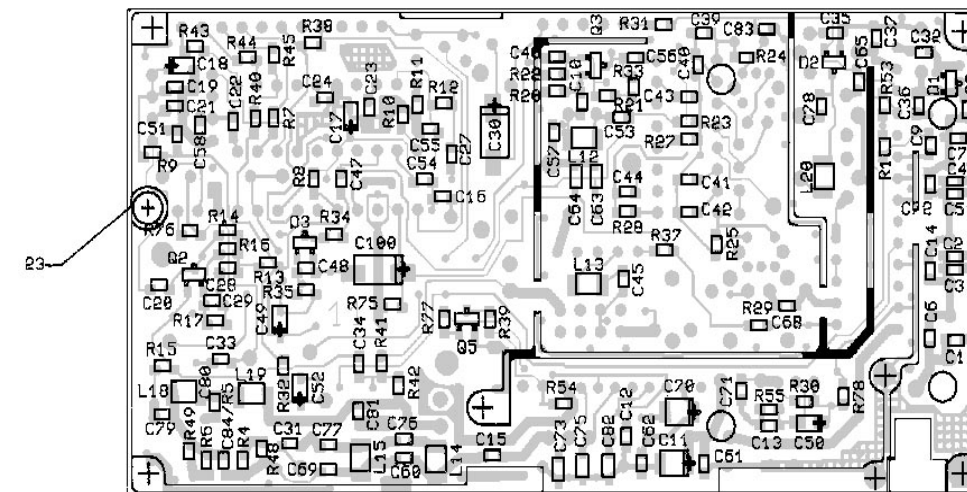
SOLDER SIDE



CHIP IDENTIFICATION TOP VIEW



SOLDER SIDE

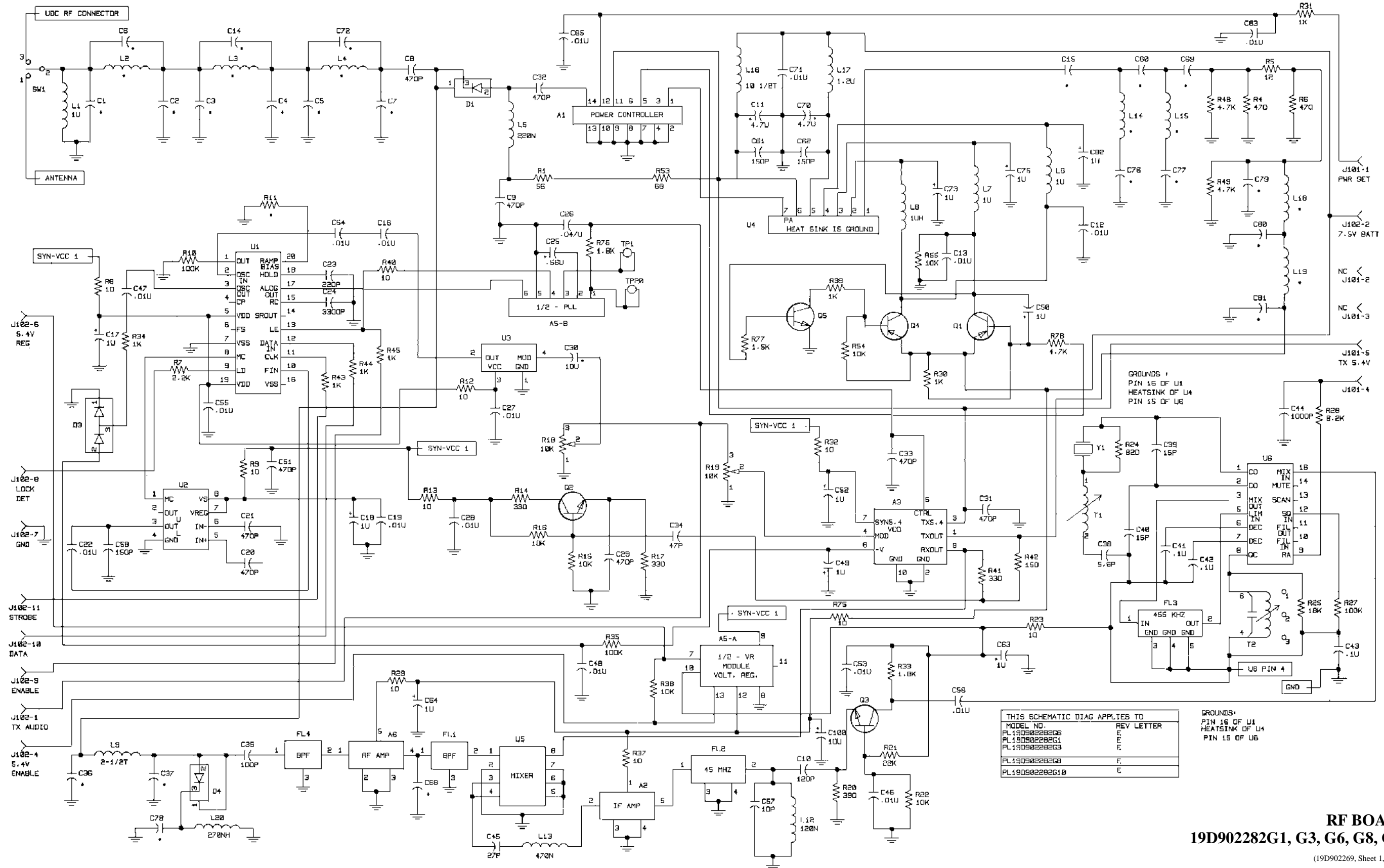


**RF BOARD**  
**19D902282G1, G3, G6, G8, G10**

(19D902282, Sheet 1, Rev. 5)  
(19D902283, Component Side, Rev. 11)  
(19D902283, Solder Side, Rev. 11)



**CAUTION**  
OBSERVE PRECAUTIONS  
FOR HANDLING  
ELECTROSTATIC  
SENSITIVE  
DEVICES



**RF BOARD**  
**19D902282G1, G3, G6, G8, G10**

(19D902269, Sheet 1, Rev. 8)