MAINTENANCE MANUAL
LOGIC BOARD
19D902172G1 & G2

TABLE OF CONTENTS

DESCRIPTION

Logic Boards 19D902172G1 and 19D902172G2 control the main operation of MDX, MDR and TMX radios. These boards also digitally process the receive and transmit audio. The G2 board differs from G1 only in having an adjustable simplex IF Offset control. This control is provided via jumper (J1) and related circuitry.

The logic board contains a microcomputer, digital signal processor, and external memory containing programming and radio personality parameters.

CIRCUIT ANALYSIS

Microprocessor U701

U701 is an 8-bit microprocessor that performs logical functions that provide control signals required in the radio. It controls the following:

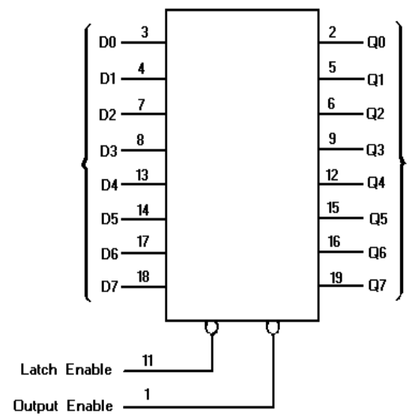
- Synthesizer
- Transmit Circuit
- Digital Signal Processor (DSP) U706
- Decoding of Channel Guard (tone or digital)
- Generation of Channel Guard (tone or digital)
- Audio gates on the Audio Board

Serial data is used for communication between the microprocessor and the Front Cap Assembly or Handset. U701 uses the **KEYPAD SERIAL** line to receive Control Panel commands from the microprocessor in the Front Cap Assembly or the Handset, U701 sends data back on the **DISPLAY SERIAL** line to update the LCD. Both serial lines normally rest at 5 volts with data causing the lines to go low.

An external 8.192 MHz crystal (Y701) is used for the clock. U702-A buffers the clock oscillator signal for DSP U706 and for U608 on the Audio Board.

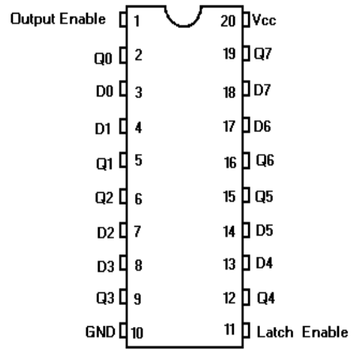
U707 OCTAL DATA LATCH

BLOCK DIAGRAM



Pin 20 = Vcc
Pin 10 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Output Enable	Latch Enable	D	Output
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

Ericsson Inc.
Private Radio Systems
Mountain View Road
Lynchburg, Virginia 24502
1-800-528-7711 (Outside USA, 804-528-7711)

Printed in U.S.A.

DIGITAL SIGNAL PROCESSOR (DSP) U706

DSP U706 is a programmed masked IC that operates under the control of microprocessor U701. The DSP processes the digitized receive and transmit audio from the Audio Board and performs the following functions:

- Busy tone notching
- Signalling tone detection
- Busy tone detection
- Alert tone generation
- Receiver volume control and muting
- Transmit audio limiting
- Busy tone injection
- Tone generation
- DTMF generation

ERASABLE PROM (EPROM) U703

EPROM U703 is a CMOS 32 kilobyte device containing all information required by microprocessor U701 for system operation. U703 uses latch U707 to demultiplex the address lines.

ELECTRICALLY ERASEABLE PROM (EEPROM) U704

EEPROM U704 is designated the "personality" PROM. This personality PROM stores all required customer information, including frequencies, tones, and options.

The EEPROM is programmed through the handset/microphone jack (J725). The serial data is routed through the Control Board or Handset Interface Board to the EEPROM on the Logic Board.

LATCH U708

Latch U708 is a CMOS, 3-state, non-inverting, D-type flip-flop with the following functions:

- To activate the BANDSWITCH line to the RF Board VCO.
- To function as a digital-to-analog converter (DAC) by generating sine wave Channel Guard tones using resistor network R713.

RELAY CIRCUIT

The relay circuit consists of NPN buffer transistor Q704 and NPN relay driver transistor Q705. The relay is activated by the microprocessor when a call is received. The circuit can handle up to 150 mA from an externally connected relay coil.

VOLTAGE REGULATOR

Voltage Regulator U705 supplies a regulated +5 Vdc to the Logic Board circuitry. A reset circuit is built into U705 to provide the microprocessor with a reset signal required during its power-up routine.

SIMPLEX INTERMEDIATE FREQUENCY OFFSET CONTROL (G2 ONLY)

For Simplex Radios, jumper J1(P1) on the G2 board is used to select the IF offset value for the radio (either 45.0125 MHz or 45.3000 MHz) that is encoded as part of the RF Board's synthesizer loading. To select the 45.3 MHz IF offset put J1 on J1-2 & 3. To select the 45.0125 MHz IF offset put J1 on J1-1 & 2.

SERVICE NOTES

1. Check for +5 ±0.25 Vdc on U701 pin 44. The 5 volt regulator (U705) receives +8 Vdc on J702-3 from the transmitter regulator on the RF Board.

2. See Figure 1 and check for the 20 ms wide reset pulse at U701 pin 10. Observe the reset pulse and the 13 volt supply simultaneously while triggering the scope on the 13 volt supply. Observe that pin 9 switches low about 20 ms after supply turns on (see Figure 1). If not present, check regulator U705 and transistor Q703.

Trigger Oscilloscope from 13.8 volts supply at power on.

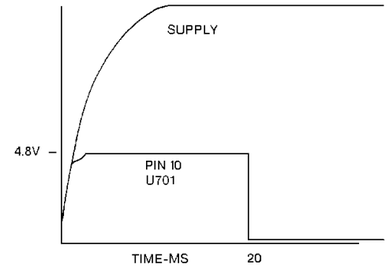


Figure 1 - Reset Wave Form

3. See Figure 2 and check for clock oscillator activity by examining the ALE on U701 pin 33 for 5 Vpp at 1.36533 MHz (clock crystal frequency divided by 6). If not present, examine the system clock on U701 pin 21 or the buffered output on J703-15 for 5 Vpp at 8.192 MHz. The presence of system clock but no ALE may indicate a bad U701. If the system clock is not present, suspect Y701 and related components.

4. Ensure the **DISPLAY SERIAL** and **KEYPAD SERIAL** lines are all normally high (+5 Vdc) while no switches are pushed and no LCD updates are occurring. Check for any shorts on the Logic or Control boards before suspecting the microprocessor.

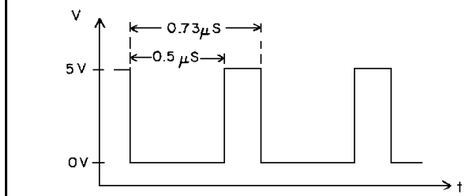
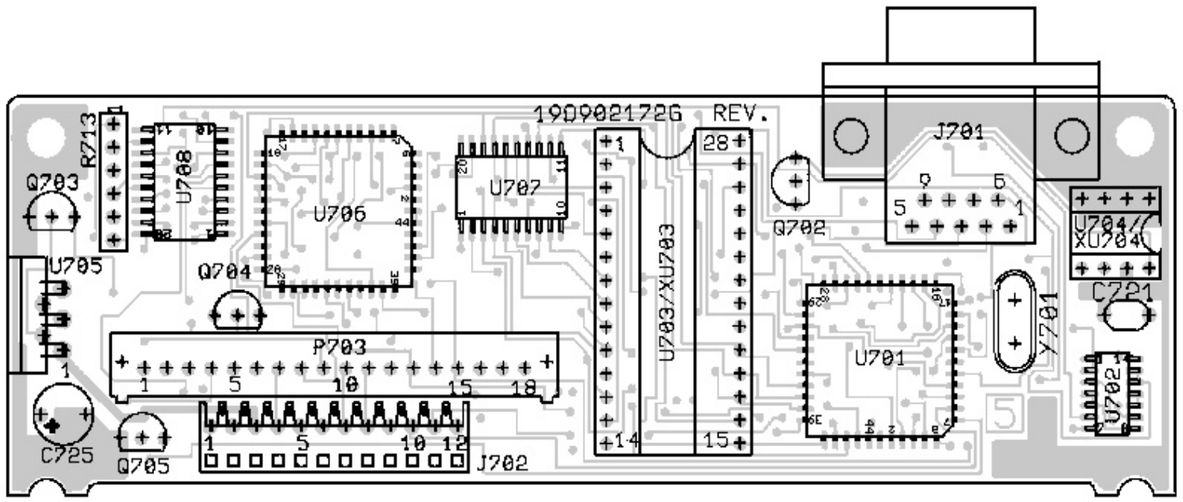


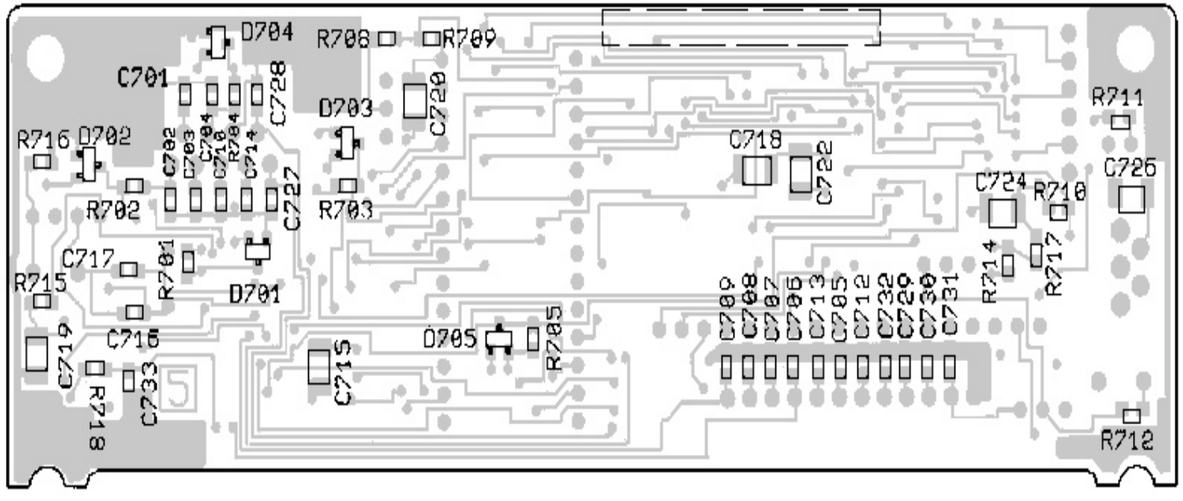
Figure 2 - ALE Clock

5. All output port lines from the microprocessor are pulled high to +5 volts through 50k ohm resistors inside the microprocessor. If a line is high you may ground that pin and monitor the results. However, if a line is low, the line **should not** be forced to +5 volts.

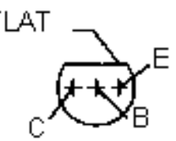
COMPONENT SIDE



SOLDER SIDE



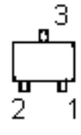
LEAD IDENTIFICATION
FOR Q702 - Q705



IN - LINE
TOP VIEW

NOTE: CASE SHAPE IS DETERMINING FACTOR FOR LEAD IDENTIFICATION

LEAD IDENTIFICATION
FOR D701 - D705



VIEW FROM SOLDER SIDE

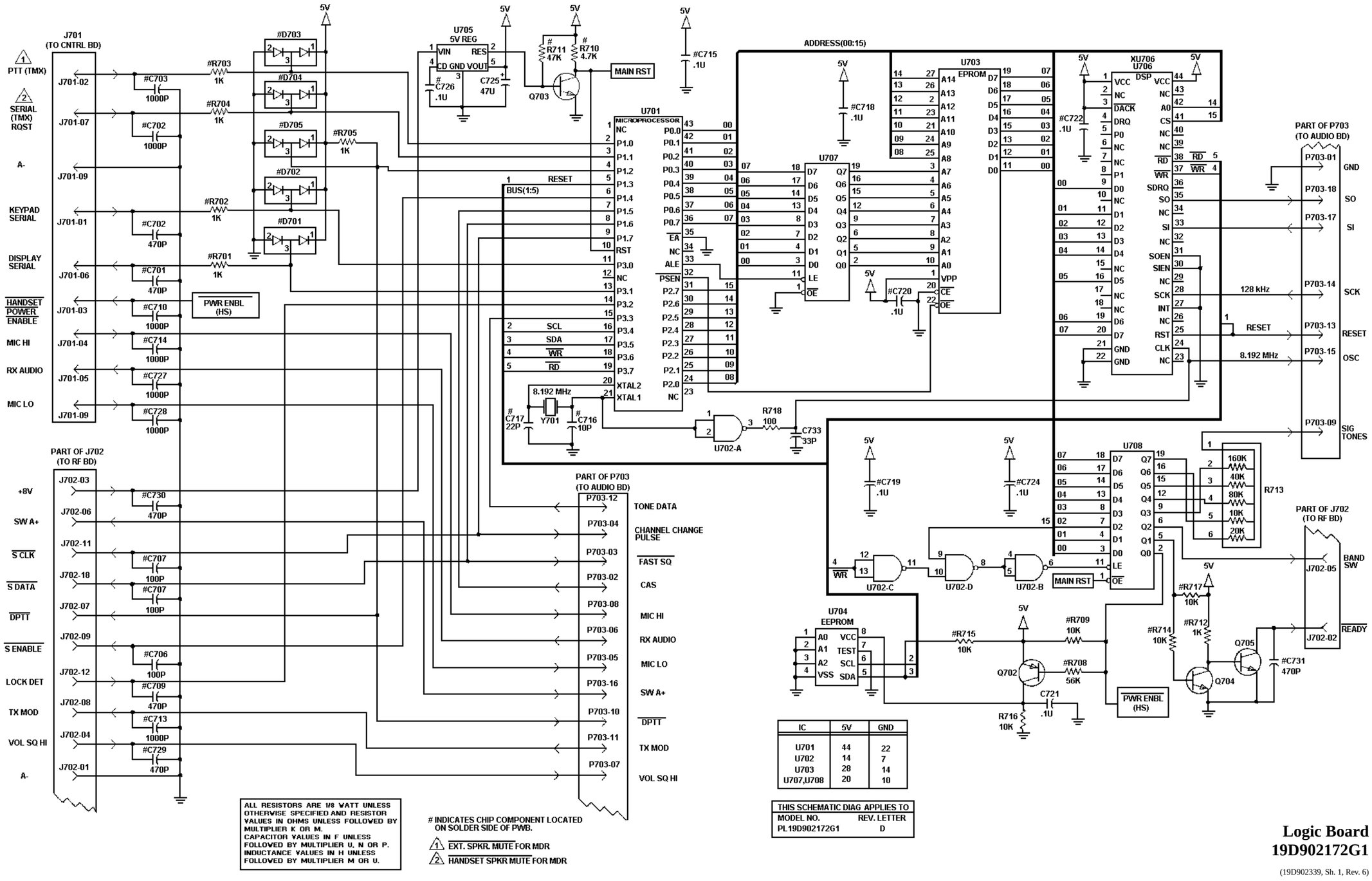
CAUTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES

Logic Board
19D902172G1

(19D902172, Sh. 1, Rev. 5)

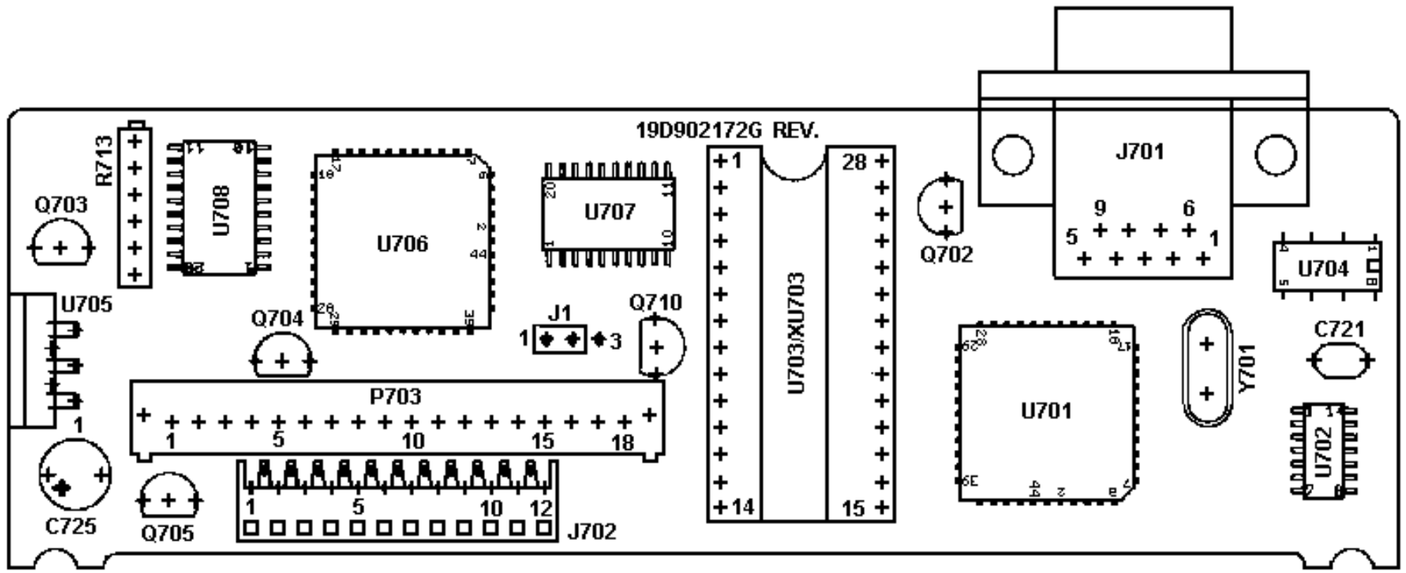
(19D902164, Component Side, Layer 1, Rev. 5)

(19D902164, Solder Side, Layer 4, Rev. 5)



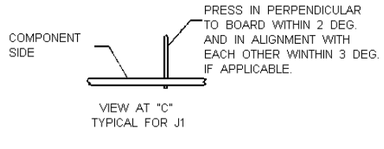
Logic Board
19D902172G1

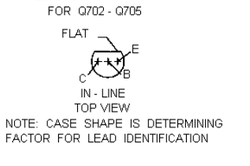
(19D902339, Sh. 1, Rev. 6)

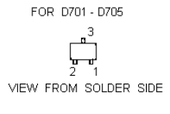


CAUTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES

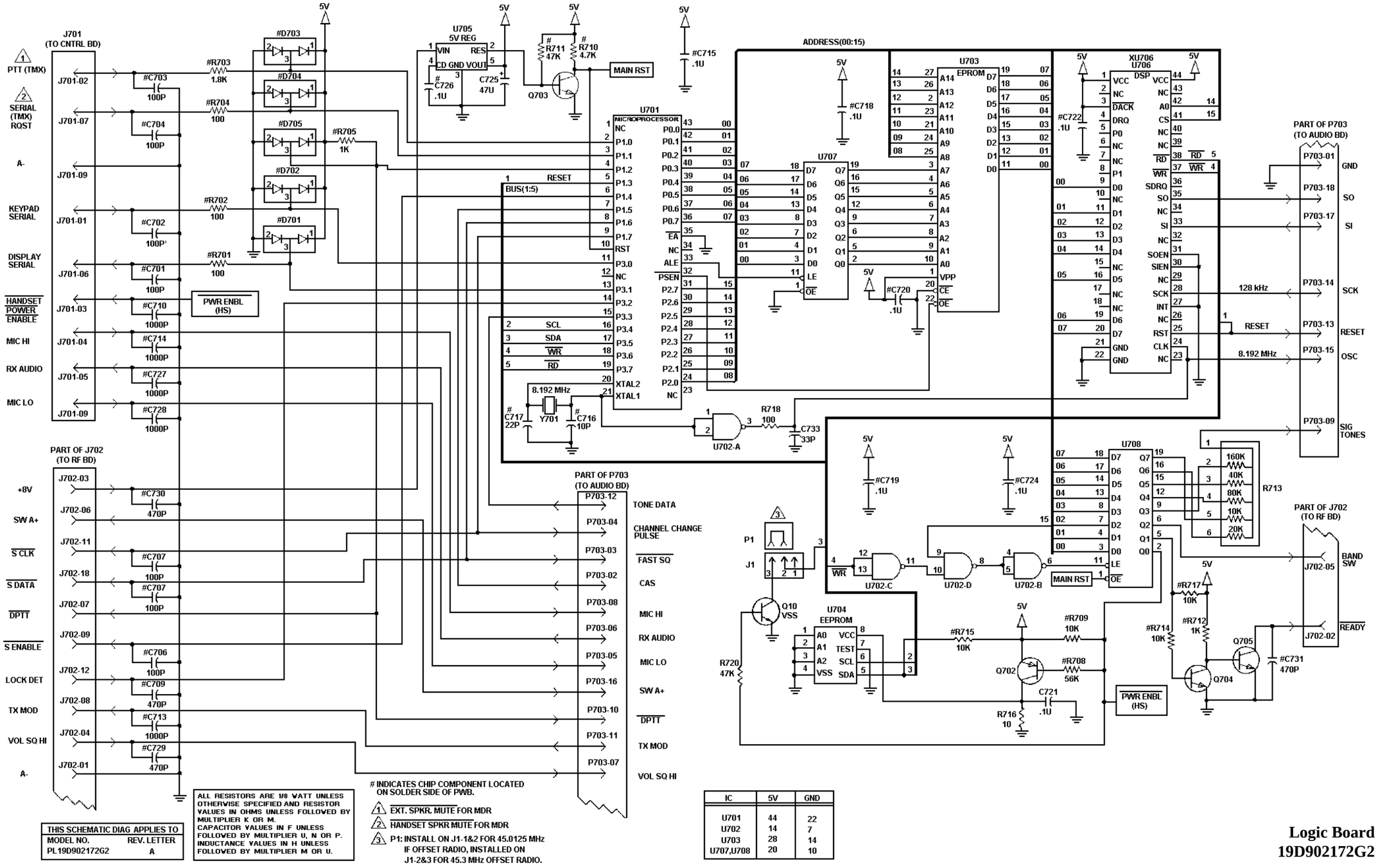
P1: INSTALLED ON J1 - 1 & 2 FOR 45.0125 MHz IF OFFSET RADIOS.
INSTALLED ON J1 - 2 & 3 FOR 45.3 MHz IF OFFSET RADIOS.







Logic Board
19D902172G2
(19D902172, Sh. 2, Rev. 0)



Logic Board
19D902172G2

(19D904841, Sh. 1, Rev. 0)

LOGIC BOARD 19D902172G1 & G2

SYMBOL	PART NO.	DESCRIPTION
		---------- CAPACITORS ----------
C701	19A702061P77	Ceramic: 470 pF ±5%, 50 VDCW, and temp coef 0 ±30 PPM (G1 only).
C702	19A702061P61	Ceramic: 100 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM (G2 only).
C703 and C704	19A702052P5 19A702061P61	Ceramic: 1000 pF ±10%, 50 VDCW (G1 only). Ceramic: 100 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM (G2 only).
C706 thru C708	19A702061P61	Ceramic: 100 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C709	19A702061P77	Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C710	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C713 thru C714	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C715	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C716	19A702061P13	Ceramic: 10 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C717	19A702061P29	Ceramic: 22 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C718 thru C720	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C721	19A700121P106	Ceramic: 0.1 µF ±20%, 50 VDCW.
C722, C724	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C725	19A701534P9	Tantalum: 47 µF ±20%, 6.3 VDCW.
C726	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C727, C728	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C729 thru C731	19A702061P77	Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C733	19A702061P37	Ceramic: 33 pF ±5%, 50 VDCW, temp coef 0 + or -±30 PPM/°C.
		---------- DIODES ----------
D701 thru D705	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99.
		---------- JACKS ----------
J1	19A703248P11	Connector, EI (G2 only).
J701	19B209727P40	Connector, Plug
J702	19A704779P11	Connector; sim to Molex 22-17-2122.
		---------- PLUGS ----------
P1	19A702104P2	Connector; 2-position shorting: sim to: AMP-530153-1 (G2 only).
P703	19A704874P1	Connector: sim to: Elco 00-9021-18-12-00-339.
		---------- TRANSISTORS ----------
Q702	19A700022P2	Silicon, PNP: sim to 2N3906.
Q703 and Q704	19A700023P2	Silicon, NPN: sim to 2N3904.
Q705	19A702503P2	Silicon, NPN: sim to 2N4401.
Q710	19A700023P2	Silicon, NPN: sim to 2N3904 (G2 only).
R701 thru R705	19B801251P102	---------- RESISTORS ---------- Metal film: 1K ohms ±5%, 1/10 w (G1 only).
R701,2,4	19B801251P101	Metal film: 100 ohms ±5%, 1/10 w (G2 only).
R703	19B801251P182	Metal film: 1.8K ohms ±5%, 1/10 w (G2 only).
R708	19B801251P563	Metal film: 56K ohms ±5%, 1/10 w., ±250 PPM/°C (G1 only).
R708	19B801251P473	Metal film: 47K ohms ±5%, 1/10 w., ±250 PPM/*C (G2 only).
R709	19B801251P103	Metal film: 10K ohms ±5%, 1/10 w.
R710	19B801251P472	Metal film: 4.7K ohms ±5%, 1/10 w.
R711	19B801251P473	Metal film: 47K ohms ±5%, 1/10 w.
R712	19B801251P102	Metal film: 1K ohms ±5%, 1/10 w.
R713	19A704885P5	Resistive Network: ±2%, 1/8 w.
R714 thru R717	19B801251P103	Metal film: 10K ohms ±5%, 1/10 w.
R718	19B801251P101	Metal film: 100 ohms ±5%, 1/10 w.
R720	19B801251P473	Metal film: 47K ohms ±5%, 1/10 w., ±250 PPM/°C (G2 only).
		-------- INTEGRATED CIRCUITS -------
U701	19A705557P2	Digital: 8-Bit Microcomputer; sim to C80C32.
U702	19A703483P302	Digital: Quad 2-Input NAND Gate; sim to 74HC00.
U703	19A705902G1	EPROM: CMOS 32K x 8; sim to 27C256-25. (Pro-grammed.)
U704	19A705553P1	Digital, CMOS: EEPROM, sim to X1COR X24C16 (G2 only).
U705	19A704970P1	Linear: 5 Volt Regulator with Reset Output; sim to SGS L387.
U706	19A705648P1	Microcomputer: 16-Bit; sim to 77C20.
U707	19A703471P302	Digital: Octal Data Latch; sim to 74HC373.
U708	19A704380P312	Digital: CMOS Octal Tri-State Data Flip-Flop; sim to 74HC374.
		---------- SOCKETS ----------
XU703	19A700156P3	Socket, IC: 28 Pins, Tin Plated.
XU704	19A700156P15	Socket, IC: 8 Pins, Tin Plated.
		---------- CRYSTALS ----------
Y701	19A702511G11	Quartz: 8.192000 MHz.

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

REV. A - LOGIC BOARD 19D902172G1
To prevent personality error due to A+ transients and to improve U704 reset, added R716 and changed C721. Old part number was:

C721 - 19A701530P4, Tantalum: 1 µF ±20%, 35 VDCW.

REV. B - LOGIC BOARD 19D902172G1
To prevent turn-on transient from pulsing horn relay option, added R717.

REV. C - LOGIC BOARD 19D902172G1
To provide MDR compatibility, deleted C705, C712 and C732. Old part numbers were:

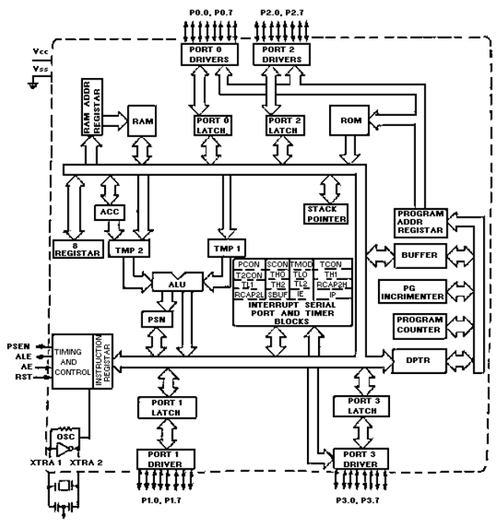
C705 - 19A702061P77, Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.
C712 - 19A702052P5, Ceramic: 1000 pF ±10%, 50 VDCW.
C732 - 19A702061P77, Ceramic: 470 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM.

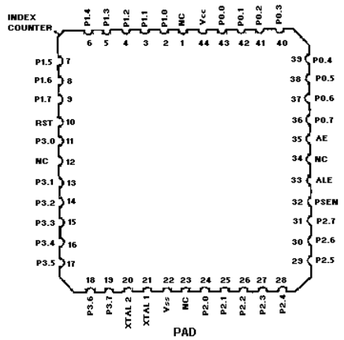
REV. D - LOGIC BOARD 19D902172G1
To provide power control signal for 12V switched power, deleted R707 and added R718 and C733. Old part number was:

R707 - 19B800607P470, Metal film: 47 ohms ±5%, 1/8 w.

U701 MICROCOMPUTER

FUNCTION DIAGRAM



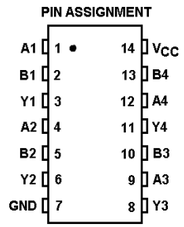


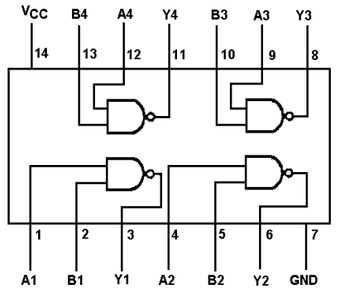
PAD

VSS	CIRCUIT GROUND POTENTIAL.
VCC	+5V POWER SUPPLY.
PORT 0	8 - BIT OC BI-DIRECTIONAL I/O PORT.
PORT 1	8 - BIT QUASI-BIDIRECTIONAL I/O PORT.
PORT 2	8 - BIT QUASI-BIDIRECTIONAL I/O PORT.
PORT 3	8 - BIT QUASI-BIDIRECTIONAL I/O PORT.
3.0	RXD - SERIAL PORT RECEIVER DATA.
3.1	TXD - SERIAL PORT TRANSMITTER DATA.
3.2	INT0 - INTERRUPT 0 INPUT.
3.3	INT 1 - INTERRUPT 1 INPUT.
3.5	T1 - COUNTER 1 INPUT.
3.6	WR - WRITE CONTROL.
3.7	RD - READ CONTROL.
RST	RESET.
ALE	ADDRESS LATCH ENABLE.
PSEN	PROGRAM STORE ENABLE OUTPUT.
EA	INTERNAL/EXTERNAL INSTRUCTION FETCH.
XTAL1	INPUT TO OSCILLATOR AMPLIFIER.
XTAL2	OUTPUT FROM OSCILLATOR AMPLIFIER.

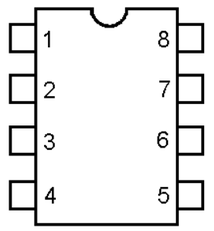
U702 QUAD 2-IN PLUG WAND GATE

PIN ASSIGNMENT





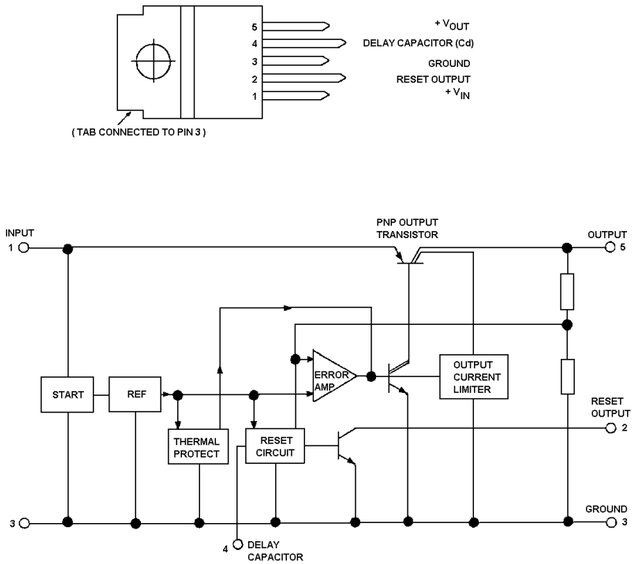
U704 EEPROM



FUNCTIONS

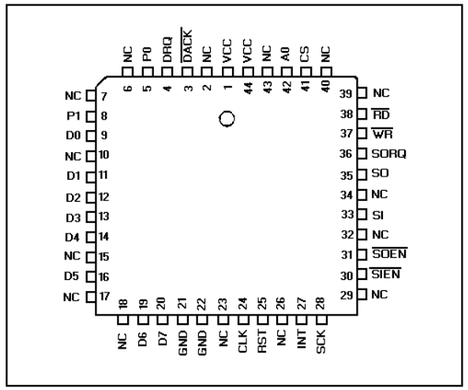
1 TO 3	A0 TO A2 ADDRESS INPUTS
4	VSS
5	SDA SERIAL DATA
6	SCL SERIAL CLOCK
7	TEST INPUT → TO VSS
8	VCC

U705 VOLTAGE REGULATOR



U706 MICROCOMPUTER

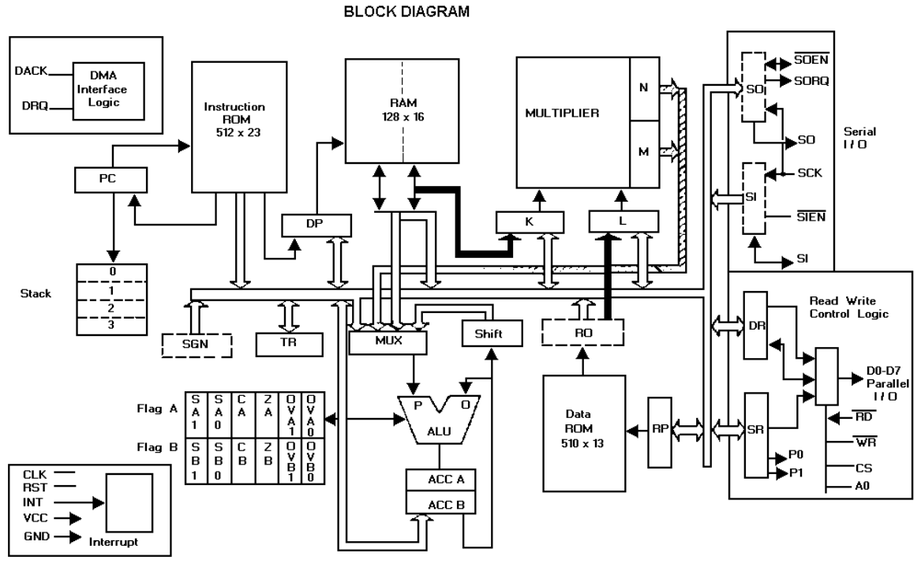
PIN CONFIGURATION



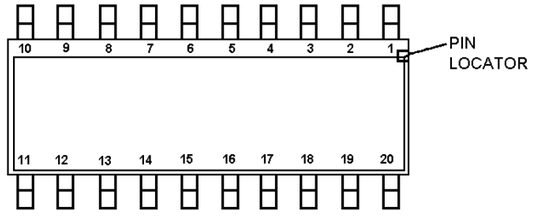
PIN IDENTIFICATION

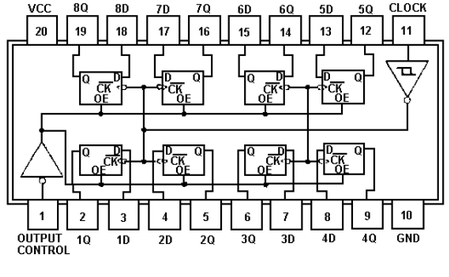
SYMBOL	FUNCTION
A0	Status/data register select input
CLK	Single-phase master clock input
$\overline{CS}$	Chip select input
D0-D7	Three-state I/O data bus
$\overline{DACK}$	DMA request acknowledge input
DRQ	DMA request output
INT	Interrupt input
P0-P1	General-purpose output control lines
$\overline{RD}$	Read control signal input
RST	Reset input
SCK	Serial data I/O clock input
SI	Serial data input
$\overline{SIEN}$	Serial input enable input
SO	Three-state serial data output
$\overline{SOEN}$	Serial output enable input
SORQ	Serial data output request
$\overline{WR}$	Write control signal input
GND	Ground
VCC	+5 V power supply
NC/VPP/VCC	No connection (77C20A_7720A)/ programming voltage (77P20)

BLOCK DIAGRAM



U708 OCTAL 3-STATE D FLIP-FLOP





TRUTH TABLE

OUTPUT CONTROL	CLOCK	DATA	OUTPUT
L	T	H	H
L	T	L	L
L	L	X	Qo
H	X	X	Z

H = HIGH LEVEL, L = LOW LEVEL
X = DON'T CARE
T = TRANSITION FROM LOW-TO-HIGH
Z = HIGH IMPEDANCE STATE
Qo = THE LEVEL OF THE OUTPUT BEFORE STEADY STATE INPUT CONDITIONS WERE ESTABLISHED.