MAINTENANCE MANUAL
DIGITAL SELECTOR MODULE
19D902519G1

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ERICSSON

SPECIFICATIONS

Power Requirements	
Input Voltage	5 Vdc 10%
Current Drain	1200 mA (maximum)
Data I/O	RS-232C
Alarm Output	TTL
Operating Temperature	0 to +60 C (32 to 140 F)
Dimensions	4 X 8 inches
Weight	10 ounces

DESCRIPTION

Digital Selector Module 19D902519G1 is used in the EDACS Simulcast System to automatically select either a 150 baud data or a 9600 baud clock stream. The digital selector module can be configured either as digital selector 1 to select 150 baud data or as digital selector 2 to select the 9600 Hz clock. The position of jumper P2 on the digital selector module determines the mode of operation. Refer to Table 1 below.

If data is not present at the selected input, the selection circuitry will advance to the next source containing a valid data stream. The selected channel or data source is displayed by the 2 digit LED display on the front of the module.

The digital selector module is normally configured as data selector No. 1 and is used only at the Control Point. (Optionally, it is used as data selector No. 2 at the transmit site.) It is physically installed in the universal synchronizer shelf assembly. The digital selector module when configured as digital selector 1 plugs into slot 2 (J2) or when configured as digital selector 2 plugs into slot 12 (J12).

Digital selector 1 is a low speed data selector (150 baud per second) used to select the low speed serial data stream from one of up to twenty-four control GETC's. All working channel control GETC's generate identical low speed data. The low speed data is generated by the GETC logic module in the GETC shelf assembly.

Digital selector 2 is the high speed clock (9600 Hz) selector used to select either an external clock or the master oscillator that generates the internal high speed digital clock. Redundant oscillators are provided on each digital selector module. Oscillator selection is controlled by jumpers P3 and P4.

Clock and control circuitry on the digital selector module provides the scanning mechanism to select a channel or source that contains a valid data stream. The criteria used for scanning is the presence of an active falling edge on the RS-232C input within ten clock cycles. The clock cycle corresponds to 75 Hz for digital selector 1 (150 baud source) and 4800 Hz for digital selector 2 (9600 Hz square wave source). Should the channel or source fail, the digital selector module will automatically advance to the next channel and scan for a valid stream during 10 clock cycle times. This continues until a valid data stream is found.

Momentary switch SW1 provides the manual advance function to force the data selector to the next data source.

A single pole, double throw switch, SW2, enables the test mode of operation. In the test mode a fixed 75 Hz or 4800 Hz is used as the data stream input for test purposes.

Switch, SW3, restricts the channel search to the actual number of operating channels.

The digital selector generates an alarm output when it is not locked onto a channel or source.

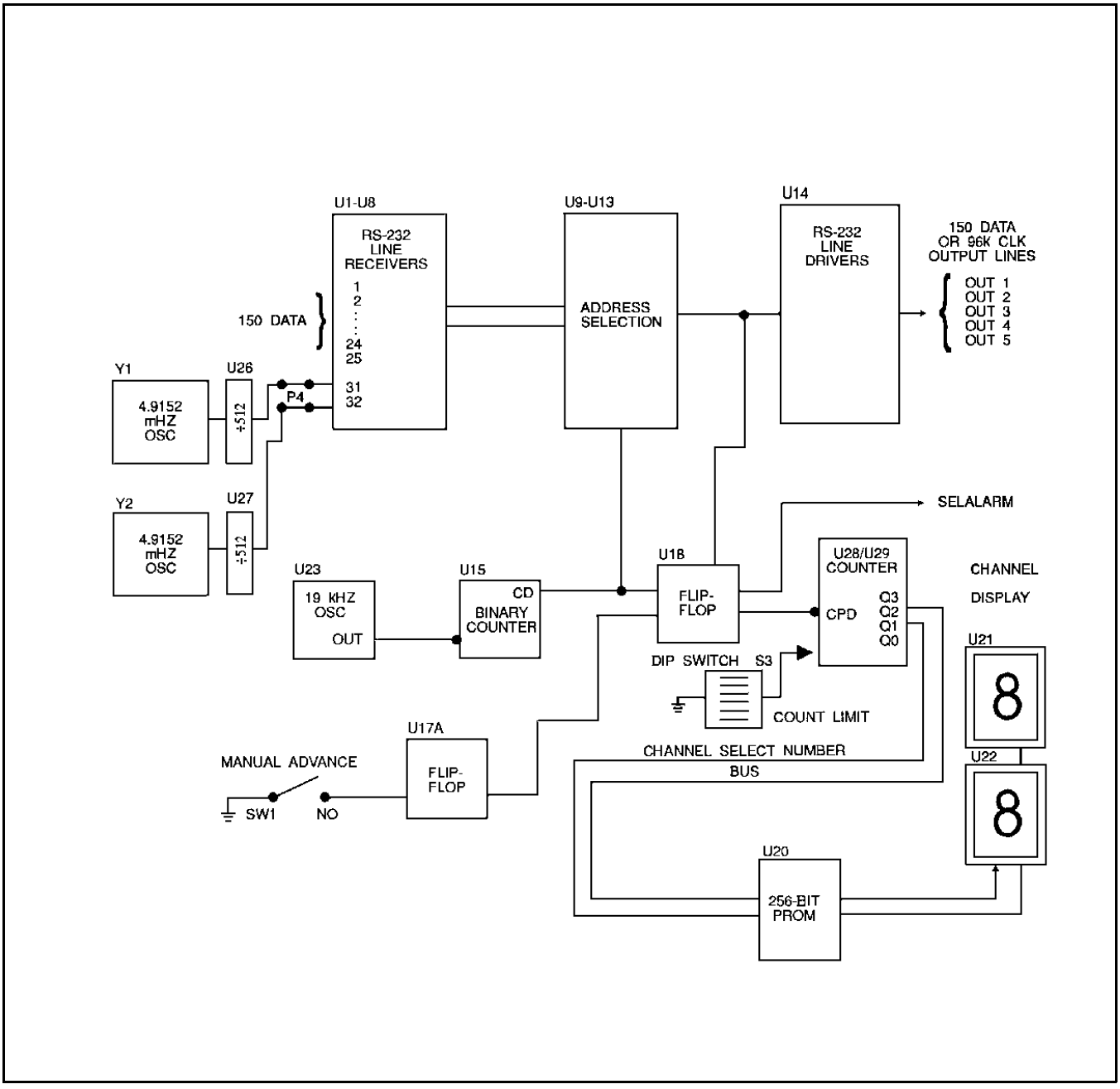
Table 1. Operational Mode Selection

Jumper	Shorting Plug	Position	Operational Mode
J2	P2	1&2	Digital Selector 1 (150) baud selection)
		2&3	Digital Selector 2 (9600 Hz selection)

CIRCUIT AND FUNCTIONAL DESCRIPTION

Digital Selector 1 receives the 150 baud data inputs from one of up to 24 control GETC's via the GETC and the GETC interface card and the cross connect panel. A block diagram of the digital selector module is shown in Figure 1. Digital selector 1 selects data from one of up to 24 control GETC's and forwards it to the FSK modem in the synchronizer shelf. The FSK modem encodes the low speed data stream using a frequency shift keyed signal. The criteria used to select the 150 baud data stream is the existence of a falling edge on the sampled low speed data signal during a 133 msec time period (10 clock cycle times). If no falling edge is detected, the next station in the sequence is scanned for a low speed data falling edge during the 133 msec sample period. This process continues until a valid data stream is found. At this point, the low speed data is sampled for 133 msec on the locked-on station. If the data disappears for 133 msec, scanning is resumed at the next station.

Figure 1. Digital Selector Module Block Diagram



All working channel control GETC's generate identical low speed data. The low speed data encodes group information to allow mobile users to quickly respond to high priority calls. The transmit sites receive the low speed data from the control point and transmit it from the EDACS stations.

Digital selector 2 selects one of the two internal clock sources. The selected 9600 Hz clock is used to synchronize the system. The GETC interface module for each EDACS station uses a phase lock loop oscillator to generate a synchronous 11.0592 MHz operating clock from the selected 9600 Hz reference clock. The 11.0592 MHz synchronous clock from the GETC interface module is sent to the GETC logic circuitry to provide the timing clock for all data signalling and station control. The criteria used to select the 9600 Hz clock is the existence of a falling edge on the sampled reference clock signal during a 2.1 msec time period (10 clock cycle times). If no falling edge is detected, the next channel bank card in the sequence is scanned for a falling edge of the reference clock within the 2.1 msec sample period. This process continues until a valid channel bank card is found. At this point, the reference clock is sampled for 2.1 msec on the locked-on channel bank card. If the clock disappears for 2.1 msec, scanning is resumed.

Momentary switch, SW1, on the digital selector module permits a manual advance to the next valid source, 150 baud data or 9600 Hz clock. This switch bypasses a portion of the scanning circuitry and allows a forced increment in the channel number. The digital selection is thereby advanced until a valid lock is established.

Toggle switch, SW2, places the channel selection function in the test mode. This allows the user to manually step through the 32 positions of the data selector. An LED is provided on the front of the module to indicate test mode operation.

Two LED displays are used to indicate the number of the valid (locked on) channel. A PROM is used for table look up when generating the LED matrix display lines from the binary address of the locked on channel. The display on digital selector 1 will range from 1 to the number of channels in the system. The display on digital selector 2 will be either 31 or 32 depending on which 9600 Hz reference clock is selected.

A 19.2 kHz oscillator (U23) is used to provide the timing for the scanning circuitry on the digital selector module.

RS-232C drivers (U14) are used to buffer the selected channel (data or clock) delivered to the FSK modem (from digital selector 1) or to the GETC interface module (from digital selector 2).

RS-232C receivers (U1 - U8) are used to buffer the input to the digital selector module. The source is the GETC interface low speed data to digital selector 1 or the clock to digital selector 2.

Flip flop U25 generates an alarm output (TTL high level) whenever the digital selector module is not locked on a valid channel.

The digital selector contains the following hardware components:

- Five 8:1 digital mux IC's (U9 - U13) to multiplex one of 32 sources to be scanned.
- One RS-232C driver (U14) to buffer the selected channel, 150 data or 9600 Hz clock.
- Eight RS-232C receivers (U1 - U8) to buffer incoming channel information.
- One 555 timer (U23) to generate the 19.2 kHz oscillator.
- One binary counter (U15) to create the sample period for the scanning interval.
- One decade counter (U16) to derive the sample period width.
- One updown counter (U28- U30) to count the present channel number.
- Two flip flops (U17) for manual advance override and next channel increment.
- One PROM (U20) for channel number table lookup to drive the led displays.
- Two LED matrix displays (U21 - U22) to display the channel number.
- One flip flop (U25) to generate the alarm output for no valid channel.

CONNECTORS AND SYSTEM INTERFACE

A single connector, P1, is used to mate the digital selector module to the sync unit assembly. The digital selector plugs into slot 2 (J2) for 150 baud selection or slot 12 (J12) for 9600 Hz selection of the sync unit assembly. A description of the various signals, data, and clocks used are summarized in Table 2.

DIGITAL SELECTOR MODULE AND CROSS CONNECT PANEL SIGNAL FLOW

IN1 Through IN32

IN1 through IN32 are RS-232C compatible inputs derived from the GETC low speed data (digital selector 1) or from the 9600 Hz clock (digital selector 2). Digital selector 1 receives the low speed data from the GETC logic modules (through the GETC interface card and the cross connect panel) for up to twenty-four control point GETC's. Digital

selector 2 receives the 9600 Hz clock from two reference oscillators located on the digital selector module.

OUT1 Through OUT5

OUT1 through OUT5 are identical RS-232C outputs from the digital selector module. These outputs are derived from valid channel data (150 baud data for digital selector 1) or clock (9600 Hz clock for digital selector 2) and are sent to the FSK modem from digital selector 1 or to up to 24 GETC interface modules from digital selector 2 to establish synchronous operation.

Table 2. Connector P1 Definition

CONNECTOR PIN	SIGNAL NAME	INPUT/ OUTPUT	LEVEL DIGITAL DC-VOLT AC-VRMS
P1-A1	+5	I/O	+5V
P1-C1	+5	I/O	+5V
P1-A2	GND	I/O	0V
P1-C2	GND	I/O	0V
P1-A3	IN1	I	RS-232C
P1-C3	IN2	I	RS-232C
P1-A4	IN3	I	RS-232C
P1-C4	IN4	I	RS-232C
P1-A5	IN5	I	RS-232C
P1-C5	IN6	I	RS-232C
P1-A6	IN7	I	RS-232C
P1-C6	IN8	I	RS-232C
P1-A7	IN9	I	RS-232C
P1-C7	IN10	I	RS-232C
P1-A8	IN11	I	RS-232C
P1-C8	IN12	I	RS-232C
P1-A9	IN13	I	RS-232C
P1-C9	IN14	I	RS-232C
P1-A10	IN15	I	RS-232C
P1-C10	IN16	I	RS-232C
P1-A11	IN17	I	RS-232C
P1-C11	IN18	I	RS-232C
P1-A12	IN19	I	RS-232C
P1-C12	IN20	I	RS-232C
P1-A13	IN21	I	RS-232C
P1-C13	IN22	I	RS-232C
P1-A14	IN23	I	RS-232C
P1-C14	IN24	I	RS-232C
P1-A15	IN25	I	RS-232C
P1-C15	IN26	I	RS-232C
P1-A16	IN27	I	RS-232C
P1-C16	IN28	I	RS-232C
P1-A17	IN29	I	RS-232C
P1-C17	IN30	I	RS-232C
P1-A18	IN31	I	RS-232C
P1-C18	IN32	I	RS-232C
P1-A24	OUT1	O	RS-232C
P1-C24	OUT2	O	RS-232C
P1-A25	OUT3	O	RS-232C
P1-C25	OUT4	O	RS-232C
P1-A26	OUT5	O	RS-232C
P1-A30	SELALARM	O	TTL
P1-A31	GND	I/O	0V
P1-C31	GND	I/O	0V
P1-A32	+5	I/O	+5V
P1-C32	+5	I/O	+5V

SELALARM

SELALARM is a TTL output from the digital selector module and is sent to the subsystem alarm module of the sync unit. This signal indicates the loss of a locked channel i.e., the digital selector is scanning.

SWITCH OPERATION

Switch SW1 provides manual advance to the next valid channel. It forces the digital selector module to lock onto an alternate valid channel. The normal position of this switch is manual advance disable.

Switch SW2 enables the test mode and is used to manually step through all 32 positions of the scan circuitry.

Switch SW3 restricts operation to the total number of channels searched. It consists of a bank of six dip switches that are set for the total number of operating channels in the system. See Figure 2.

POWER DISTRIBUTION AND FILTERING

The +5 Vdc power source (P1-A1) required for operation of the digital selector module is supplied by the simulcast power supply and is present at P1-A1 (Refer to Schematic Diagram). The +5 Vdc power input supplies power to the 8:1 digital multiplexers, RS-232C drivers and receivers, 19.2 kHz oscillator, scanning circuitry, PROM, and LED matrix displays.

Power bypass capacitors C3 - C28 filter out any noise transients or spikes to prevent them from affecting module performance.

DIGITAL MULTIPLEXER

The digital multiplexers consist of U9, U10, U11, U12, and U13. These devices are used to scan up to 32 sources. The data is derived from IN1 through IN32 and buffered through the RS-232C receivers, U1 through U8, before arriving at multiplexers, U9 through U12.

The 8:1 multiplexers, U9 through U12 derive their steering, address or select inputs, from the three least significant bits of channel address counter U28 - U30. The 32 sources enter multiplexers, U9 through U12. Data mux U13 selects one of the four 8:1 multiplexers or a fixed 75 Hz from clock divider, U15.

The select control for U13 is derived from the most significant two bits of the channel address and the test mode switch position. If test mode is enabled, LED D1 is on and a logic high is present at the C input to U13. This steers the 75 Hz to the SELOUT line. If the test mode is disabled, the two channel address lines, SEL16 and SEL8, select the 4 digital multiplexers.

The 4 digital multiplexers use select lines, SEL4, SEL2, and SEL1 from channel address counter U28 - U30 to select one of 8 inputs per device.

DIGITAL SELECT OSCILLATOR

The digital select oscillator consists of a free running 19.2 kHz clock generated by 555 timer U23. Resistors and capacitors determine the nominal free running frequency.

The 19.2 kHz output (U23-3) is input to dual stage binary counter, U15. The two sections of U15 are coupled such that the falling edge of the first output (U15-8) is input to the second stage at U15-1 to form an 8 bit ripple counter.

Selected taps from U15 are used to generate the nominal 4800 Hz and 75 Hz clocks for the sampling circuitry.

The 75 Hz clock is used by digital selector 1 to sample the 150 baud data from the GETC interface card.

The 4800 Hz clock is used by digital selector 2 to sample the 9600 Hz clock.

Jumper J2 and shorting plug P2 configure the digital selector module for 9600 Hz clock sampling (positions 2 and 3) or 150 data sampling (positions 1 and 2). The appropriate clock, 4800 Hz or 75 Hz is sent to the decade counter U16 to set up the sample period.

DIGITAL SELECT SAMPLER AND CHANNEL SELECTOR

The digital sampler consists of decade counter U16, data sampling FF U18, and the NOR gates of U24. U16 generates a 10 cycle sampling period, U18 captures a rising edge of SELOUT within the sample period and enables continued counting of the channel counter (U28-U30) if a valid channel is not found. The NOR gates of U24 perform the required gating for sampling.

The clock input to sample period decade counter U16 is generated from the data select oscillator and a counter (U15 and U23). It is selected by jumper J2. The clock input is 4800 Hz for 9600 Hz clock selection and 75 Hz for 150 baud low speed data selection.

Decade counter U16 is a free running counter that counts from 0 to 9 and rolls back to 0. During the count from 7 to 8, the SELOUT line is checked for a rising edge during the sample period. If a rising edge occurs, U18 pin 5 will be logic low which is passed through U24 to the input of data sampling FF U18-12. The count (from 7 to 8) on decade counter U16 samples the state of U18-12. If a low is present

(SELOUT had a rising edge), the output at U18-8 will be a logic high (or remain a logic high). If SELOUT is determined to have no rising edges during the sample period, U18-8 will go low, thereby generating a clock edge to the channel address binary counter, U28-U30, and decrementing the count to the next channel for subsequent sampling.

Channel number selection is determined by 8-bit ripple counter U28 - U30. The count of the 8-bit ripple counter is sent to the digital multiplexers to select one of 32 possible sources for the data select input. Dip switch SW3 restricts channel search to a subset of channels equal to the total number of channels in the system. Dip switch SW3 consists of a bank of six dip switches that allow binary selection for up to 32 channels. Dip switch position versus total number of channels is shown in Figure 2. An "X" indicates an open switch.

Figure 2. Channels Versus SW3 Setting

Channels	SW3					
	6	5	4	3	2	1
1	-	-	-	-	-	X
2	-	-	-	-	X	-
3	-	-	-	-	X	X
4	-	-	-	X	-	-
5	-	-	-	X	-	X
6	-	-	-	X	X	-
7	-	-	-	X	X	X
8	-	-	X	-	-	-
9	-	-	X	-	-	X
10	-	-	X	-	X	-
11	-	-	X	-	X	X
12	-	-	X	X	-	-
13	-	-	X	X	-	X
14	-	-	X	X	X	-
15	-	-	X	X	X	X
16	-	X	-	-	-	-
17	-	X	-	-	-	X
18	-	X	-	-	X	-
19	-	X	-	-	X	X
20	-	X	-	X	-	-
21	-	X	-	X	-	X
22	-	X	-	X	X	-
23	-	X	-	X	X	X
24	-	X	X	-	-	-
25	-	X	X	-	-	X
26	-	X	X	-	X	-
27	-	X	X	-	X	X
28	-	X	X	X	-	-
29	-	X	X	X	-	X
30	-	X	X	X	X	-
31	-	X	X	X	X	X
32	X	-	-	-	-	-

A voltage, indicating the position of the manual advance switch, is used to trigger and reset FF U17. The output of U17 is coupled to NOR gate U24C and provides a manual channel decrement by forcing the input of FF U18-12 to a logic high. The manual advance switch resets FF U17-6. Upon release of the momentary switch, a rising edge is generated on U17-11. This sets U17-9 high and executes the manual advance function. U17-9 is subsequently reset via the channel decrement pulse from U18-8, thereby allowing only one channel advance per switch toggle.

Figures 3, 4 and 5 show the timing diagram for a valid lock on channel, no valid channel, and manual advance from a lock on channel, respectively.

Figure 3. Timing Diagram For A Valid Locked On Channel Without Manual Advance

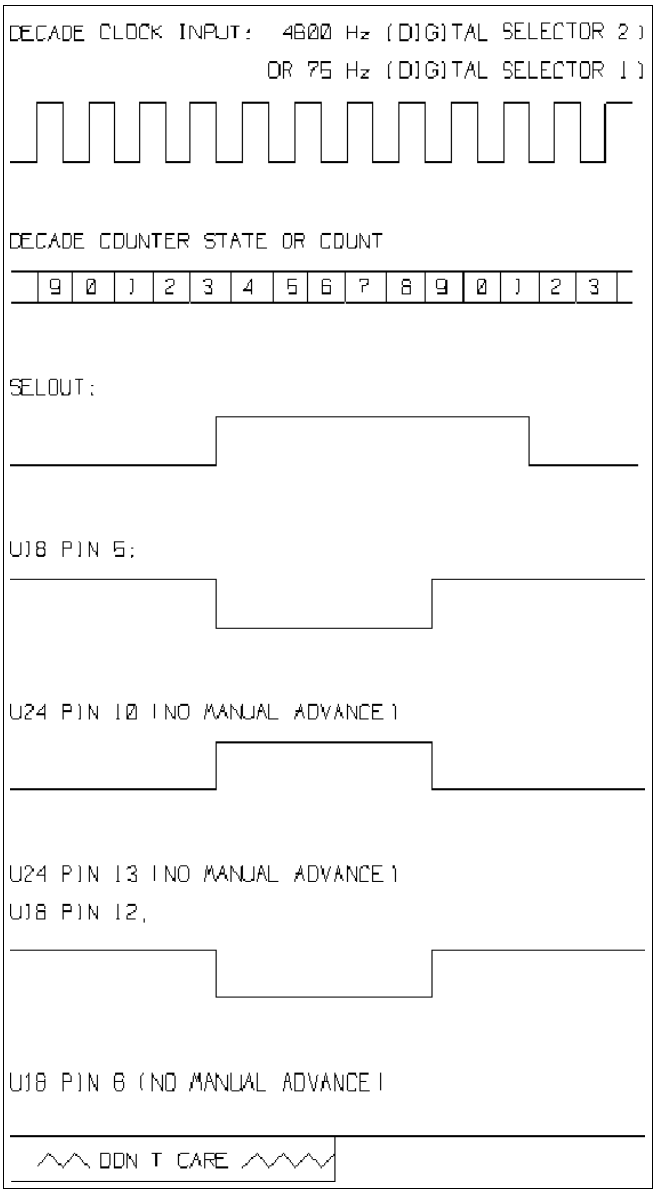


Figure 4. Timing Diagram For A Non-Valid Channel Without Manual Advance

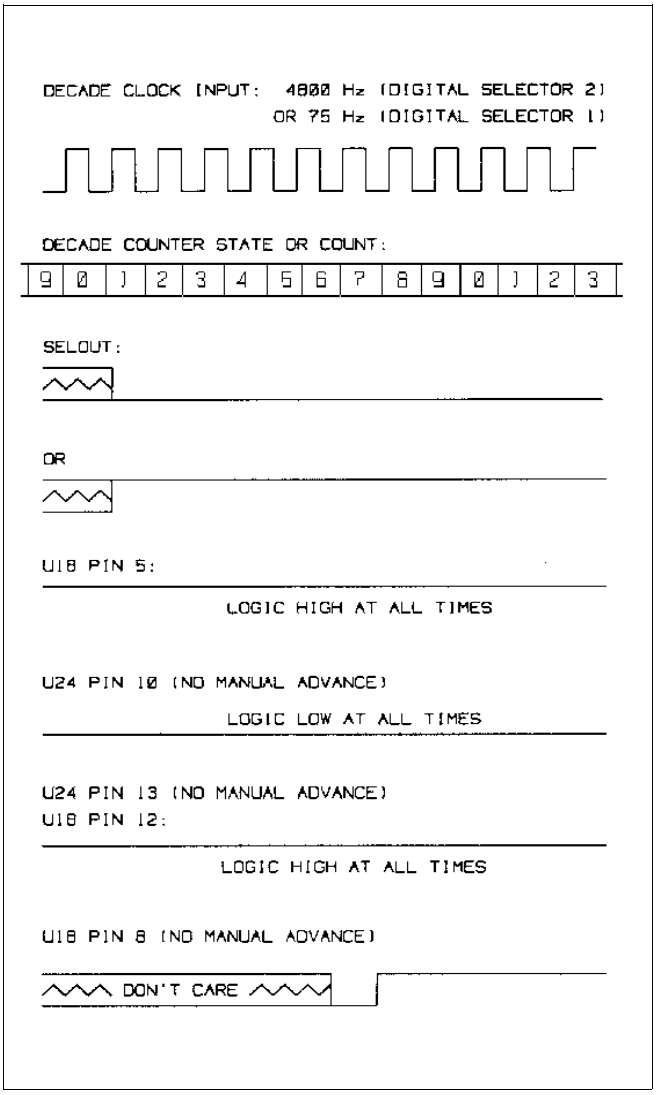
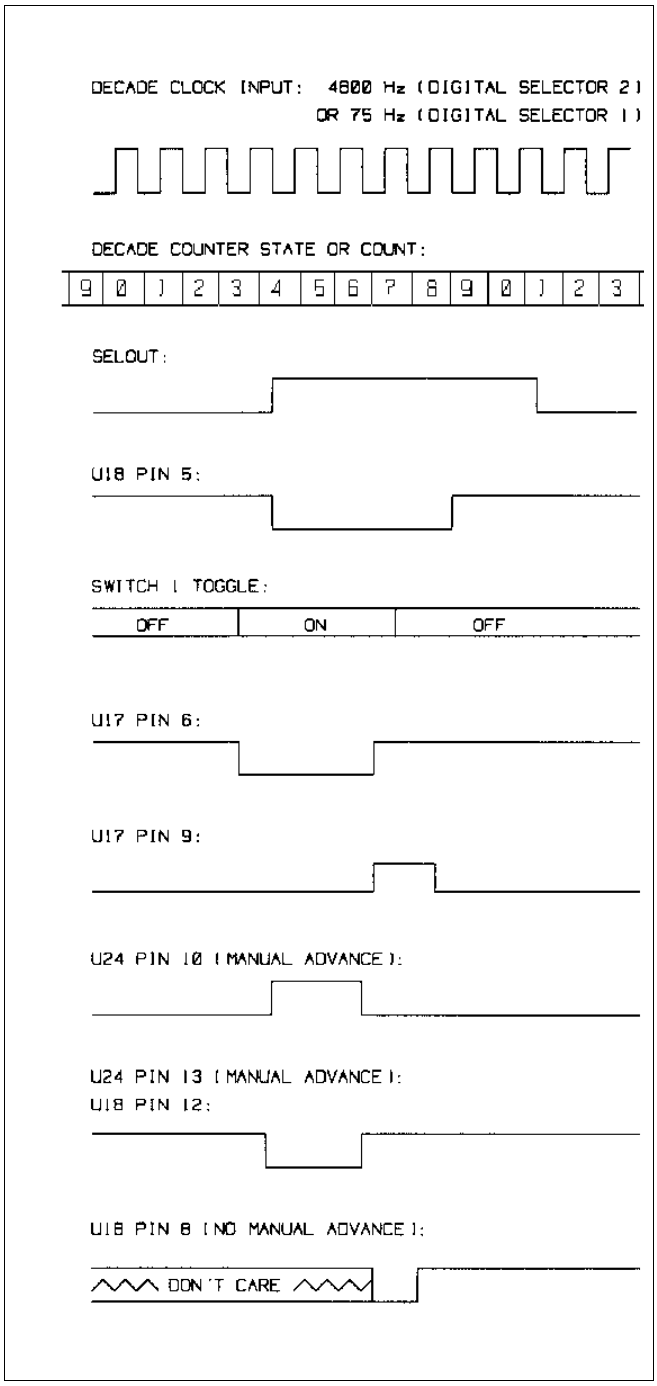


Figure 5. Timing Diagram For A Valid Locked On Channel With Manual Advance



PULSE FILL OPTION

The pulse fill option is provided to facilitate operation of the resynchronization circuitry in some special applications. The pulse fill option, consisting of C69, R14, and D2 and associated circuitry, is not used in standard simulcast systems. It is enabled via jumpers P4 and P5.

Table 3. Pulse Fill Jumper Configuration

JUMPER	NORMAL	PULSE FILL
P5	2-3, 4-5	1-2, 3-4
P4		3-4

TEST, DISPLAY, AND ALARM FUNCTIONS

The 75 Hz clock is the clocking input to the decade counter when configured as a digital selector No. 1. It is also the SELOUT line when the test enable switch is set to the test position. The decade counter period, therefore, will always have transitions of the 75 Hz clock within its sample period. The channel selector will lock onto the present channel (unless the manual advance switch is thrown to manually force the channel selection to the next decrement).

The 4800 Hz clock is the clocking input to the decade counter when configured as digital selector No. 2. It is also the SELOUT line when the test enable switch is set to the test position. The decade counter period will not have a single transition of the 75 Hz clock with 10 clock periods of the 4800 Hz clock input to the counter. The digital selector 2 configuration will therefore continually decrement the channel selection and never find a valid channel.

The channel number selection is performed by binary counter U28 - U30. The binary count is sent to the digital multiplexers to select one of 32 possible sources for the data select input. Dip switch SW3 allows search to be restricted to a subset of channels (1 dip switch setting) so that LSD search will not linger on unavailable channels. The channel number is also sent to look up PROM U20.

The PROM is used to generate the logic signals to the channel displays, U21 and U22. U21 is the most significant channel display and U22 is the least significant channel display. The PROM has a simple lookup such that the binary channel number from 0 to 31 (decimal) is encoded to the displays as 1 to 32, respectively. The PROM U20, also generates a blanking output to U21 to blank the display if the binary count input is less than 9 (or less than 10 at the PROM output).

The digital selector module also generates an alarm output indicating whether the digital selector module is presently scanning for the next valid channel. This function is performed by FF U25. The operation of U25 is similar to FF U18 which generates the clock input to the channel binary counter, U28-U30.

Both U25 and U18 have the same clock input. The D input to U25 and U18 are identical when the manual advance is not used. U25 does not register an alarm condition based on the manual advance switch override, rather it only generates an alarm based on the absence of a rising edge on SELOUT within the sample period. The alarm output is a minimum of one sample period long and can change state only at the end of each sample period.

CRYSTAL CONTROLLED OSCILLATORS

Two crystal controlled oscillators (Y1 - Y2) operating at 4.9152 MHz provide the reference frequency for generating the two 9600 Hz reference clocks. The output of the oscillators are divided by 512 by counters U26 & U27 to provide the 9600 Hz reference clocks.

Jumpers J3, 4, 6 and 7 are used to connect the oscillator outputs to IN31 and 1N32 inputs when the module is used as digital selector 2. Jumpers J6 and J7 provide the interconnect for the source clock and are normally connected for 9600 Hz operation: P6-3 to P3-3 and P7-3 to P4-3. Thus 9600 Hz is always present at jumpers P3 and P4. Operation with either internal or external clock is available via jumper connections P3 and P4. Refer to Table 4 for the appropriate jumper configuration.

A 4800 Hz clock is also provided by U26 and U27 and may be selected by repositioning jumper P6 or P7 to connect 1-2.

Table 4z. 9600 Hz Reference Clock Selection

JUMPER	INTERNAL	EXTERNAL
P3	2-3	1-2
P4	2-3	1-2
P6	2-3	9600 Hz source
P7	2-3	9600 Hz source
P6	1-2	4800 Hz source
P7	1-2	4800 Hz source

MAINTENANCE

The digital selector module must be configured to operate as digital selector 1 or digital selector 2 as required by the particular system application. Refer to Table 1 for proper jumper configuration.

Switches SW1, SW2, and SW3 must be properly configured for the system application and normal operation. SW1 is a momentary switch that performs the manual advance function. SW2 is a toggle switch that enables the test mode of operation. SW3 must be set to restrict the channel search to the total number of operational channels in the system. The normal positions of these switches are shown in Table 5

There are no circuit adjustments on the digital selector module.

Table 5. Switch Functions

Switch	Position	Definition
SW1	down	Manual advance disabled
SW2	up	Test mode disabled
SW3		Refer to Figure 5

TEST AND SERVICE

The following test equipment is necessary to test the digital selector module as part of the simulcast system.

1. Extender Card
2. Tektronix R5223 Digital Storage Scope or equivalent
3. Triplett Model 630-PL Type 5 or equivalent
4. Test Cables as required
5. HP 8116 Pulse/Function Generator or equivalent.

The following steps are necessary to test the digital selector as part of the simulcast system.

1. Configure jumpers J2 - J4 for the desired mode of operation (150 baud data or 9600 Hz clock selection).

2. Install the Digital Selector Module as part of the simulcast system (slot 3 for 150 baud data selection or slot 15 for 9600 Hz clock selection).

3. Verify the presence of +5 volt power (+5).

4. Digital Selector 1 (150 baud data selection)

   Verify 150 baud data on IN1 through IN32 as per site configuration.

   Verify 150 baud data on SELOUT.

   Verify 150 baud data on OUT1 through OUT5.

   Verify the operation of the manual advance switch to search for other channels of valid low speed data.

   Verify the operation of the test enable switch to lock onto the present channel, followed by the manual advance switch to increment to the next channel irrespective of whether it contains valid low speed data.

   Digital Selector 2 (9600 Hz selection)

   Verify 9600 Hz clock on IN31 and IN32.

   Verify 9600 Hz clock on SELOUT.

   Verify 9600 Hz clock on OUT1 through OUT5.

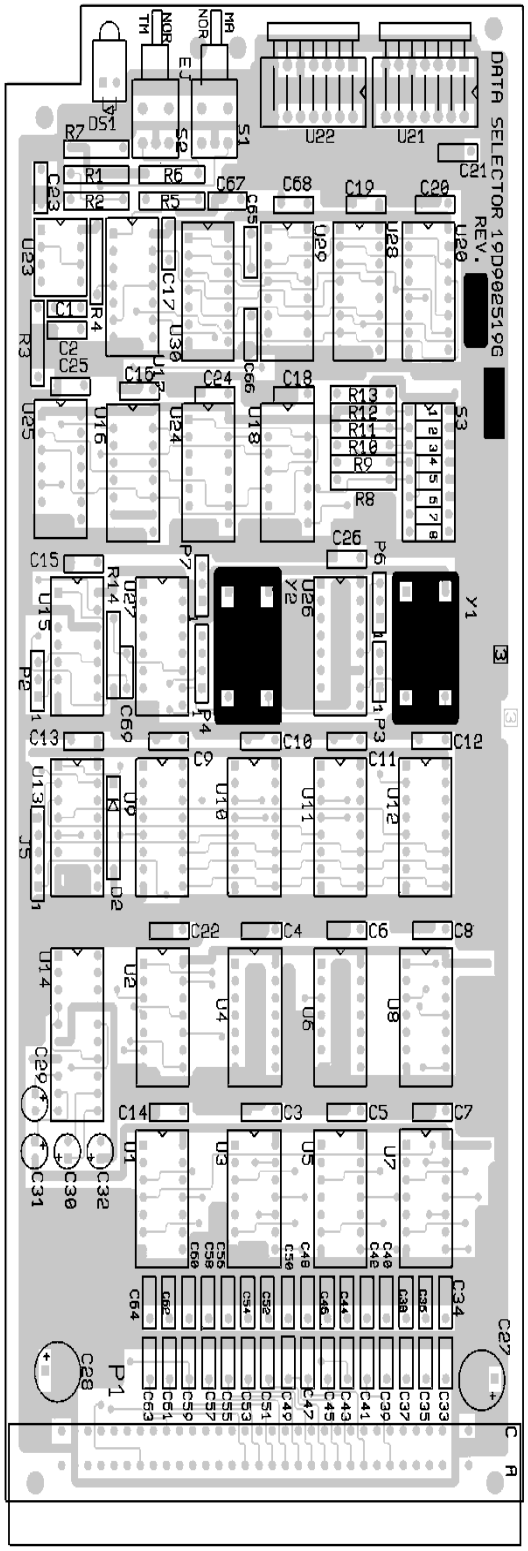
   Verify the operation of the manual advance switch to search for other channels of valid 9600 Hz clocking.

   Verify the operation of the manual advance switch to search for other channels of valid low speed data.

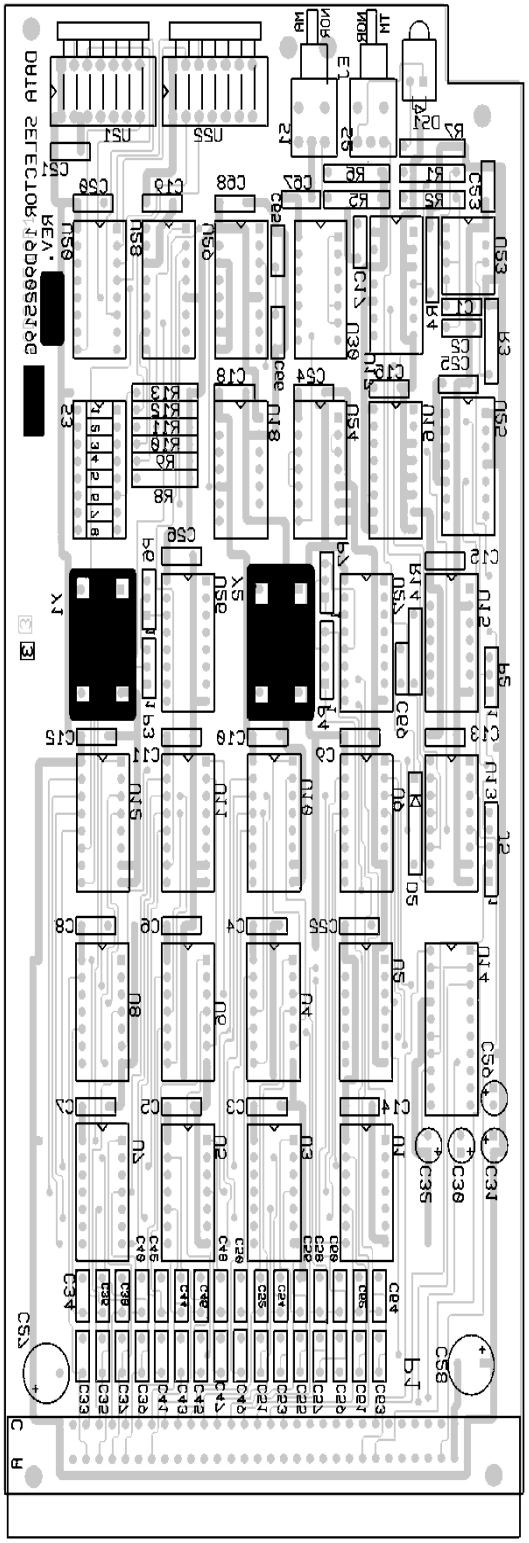
   Verify the operation of the test enable switch to lock onto the present channel, followed by the manual advance switch to increment to the next channel irrespective of whether it contains valid low speed data.

5. Reconfigure the module back to normal system operation and install back into the proper slot of the Sync Unit Assembly.

Component Side

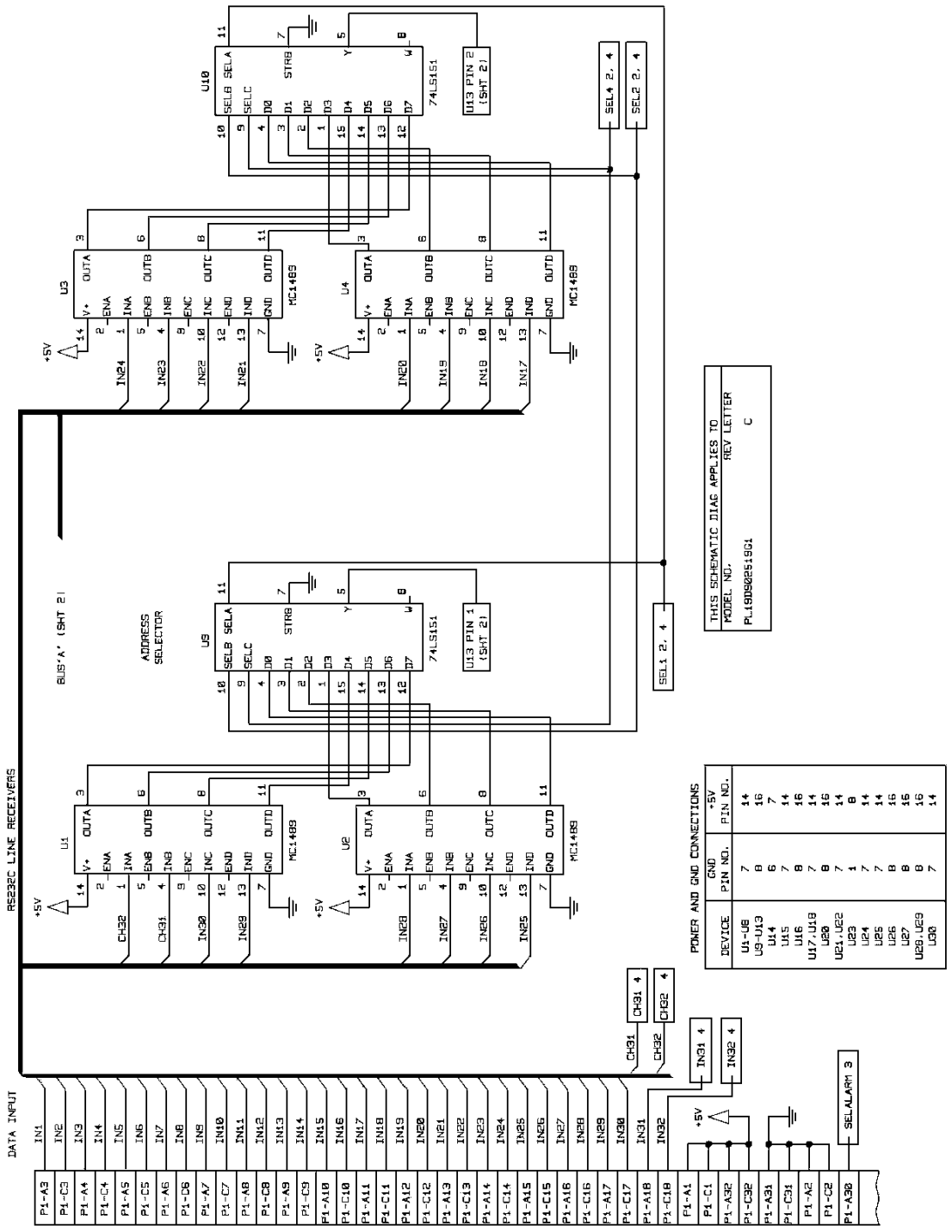


Solder Side



DIGITAL SELECTOR MODULE
19D902519G1

(19D902518, Rev. 4)



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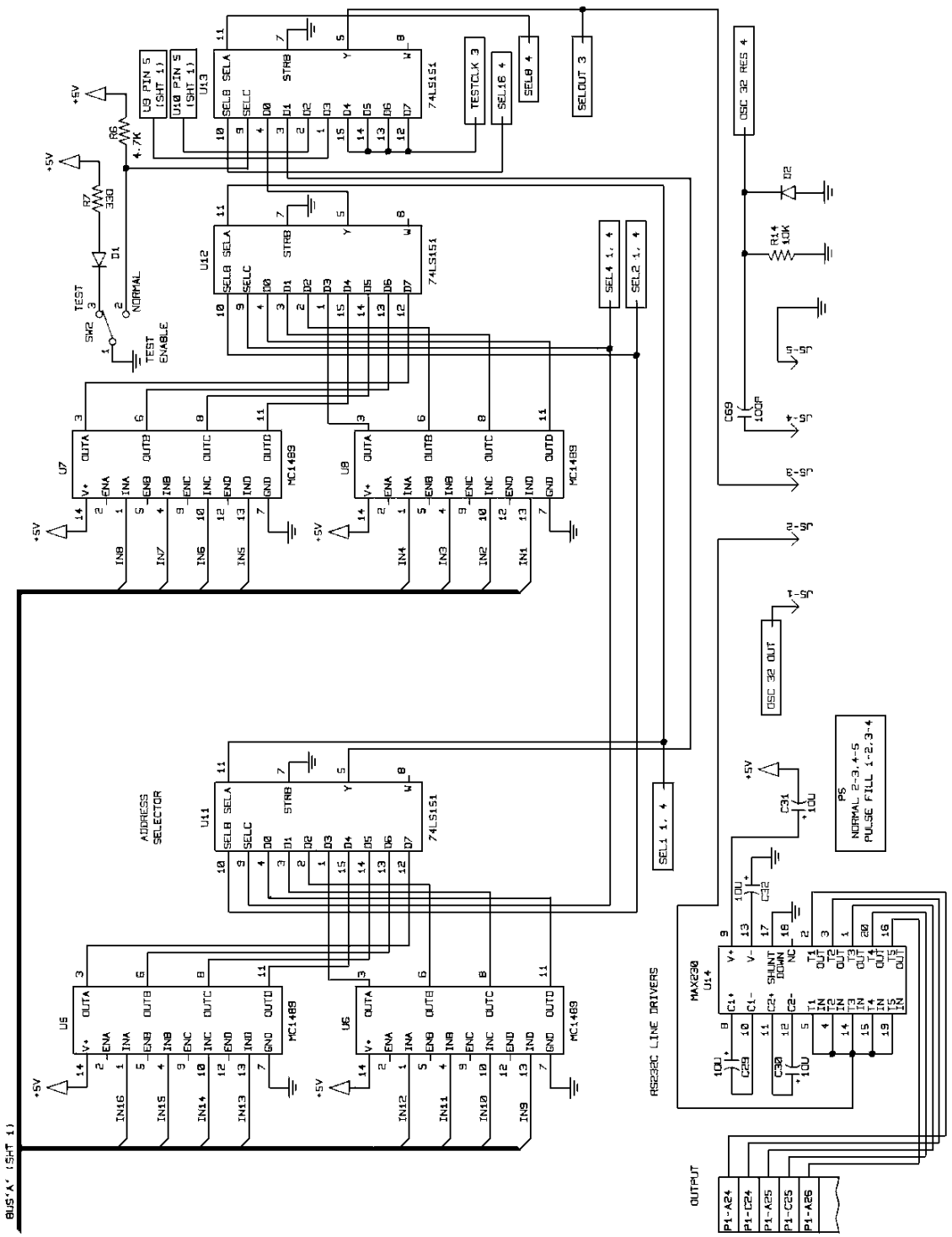

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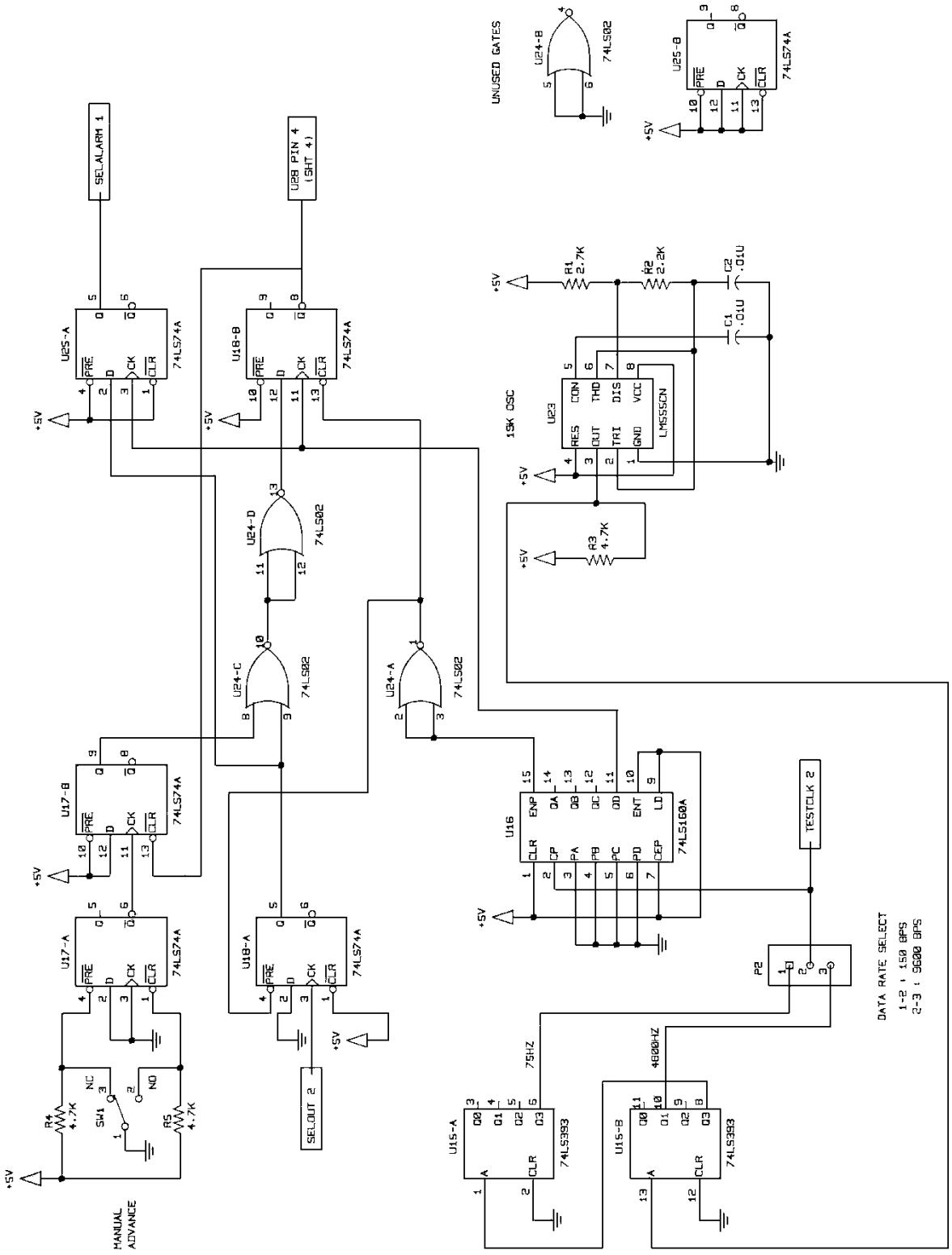

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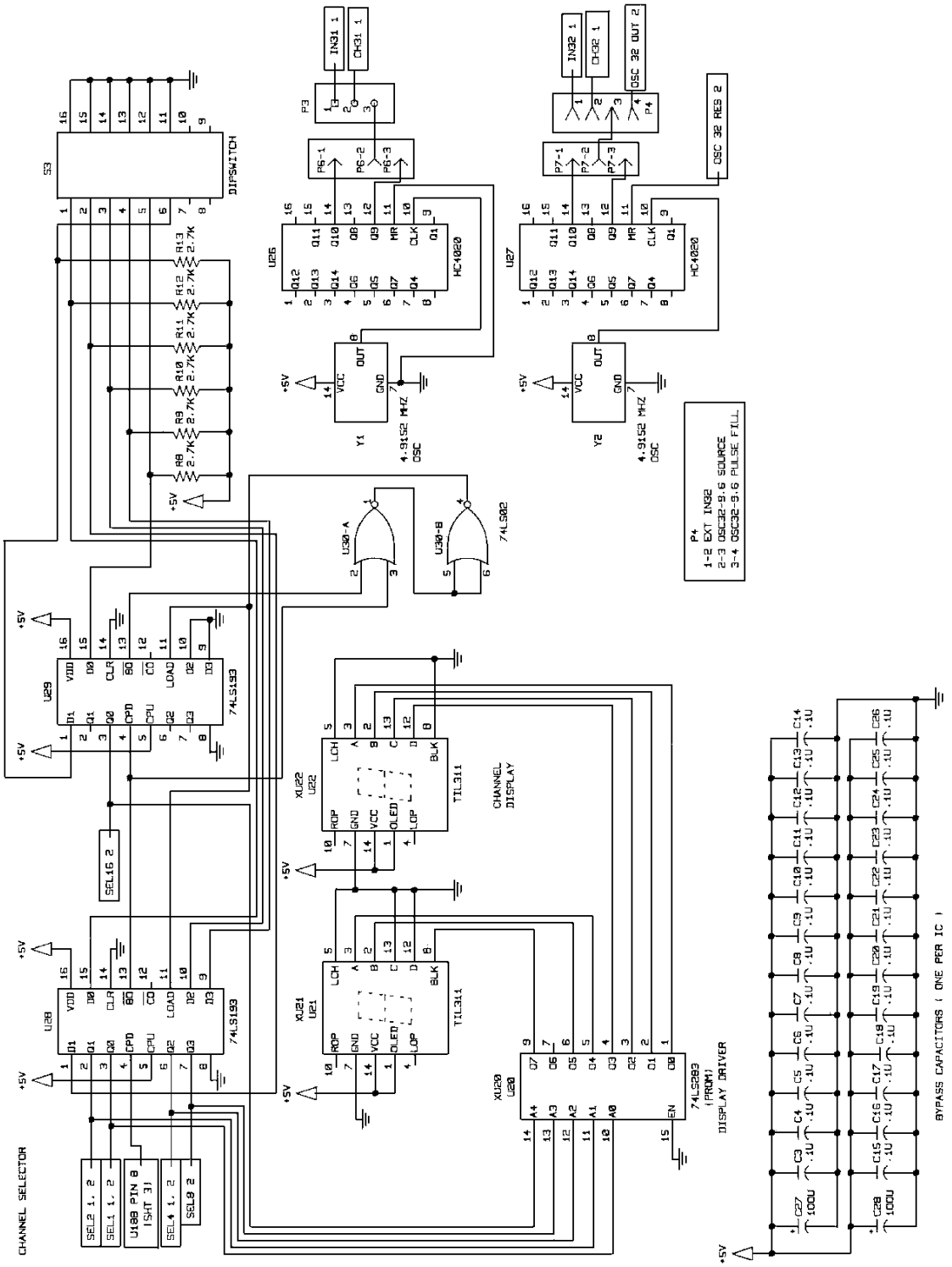
19D902519G1
(19C851934, Sh. 3, Rev. 5)



DIGITAL SELECTOR MODULE
19D902519G1

(19C851934, Sh. 4, Rev. 5)

DIGITAL SELECTOR MODULE 19D902519G1

SYMBOL	PART NUMBER	DESCRIPTION
		- - - CAPACITORS - - - - - -
C1,C2	T644ACP310K	Polyester: 0.01 F.
C3-C26	T644ACP410K	Polyester: 0.1 F.
C27,C28	19A703314P1	Electrolytic: 100 F, 10VDC.
C29-C32	19A701534P7	Tantalum: 10 F, 16VDCW.
C67,C68	T644ACP410K	Polyester: 0.1 F.
C69	19A700233P1	Ceramic: 1000 pF, 5%, 50 VDCW.
		- - - - - - DIODES- - - - - - - - -
DS1		Opto electric; sim to DIALIGHT 550-5106.
D2	19A115250P1	Diode, silicon.
		- - - - - - - JACKS - - - - - - - - -
J2,J3	19A704852P2	Printed wire connector.
J4	19A704852P3	Printed wire connector.
J5	19A704852P4	Printed wire connector.
J6,J7	19A704852P2	Printed wire connector.
		-- - - - - - - - PLUGS - - - - - - - - -
P1	19B801587P1	Connector, two part.
P2-P7	19A702104P2	Connector.
		-- - -- - - -RESISTORS - - - -- -- - - -
R1	H212CRP227C	Carbon film: 2.7K ohms 5%, 1/4 w.
R2	H212CRP222C	Carbon film: 2.2K ohms 5%, 1/4 w.
R3-R6	H212CRP247C	Carbon film: 4.7K ohms 5%, 1/4 w.
R7	H212CRP133C	Carbon film: 2.2K ohms 5%, 1/4 w.
R8-R13	H212CRP227C	Carbon film: 2.7K ohms 5%, 1/4 w.
R14	H212CRP310C	Carbon film: 10K ohms 5%, 1/4 w.
		- -- - - - -SWITCHES - - - - - - -
S1		Momentary: sim to AT1F-RA-MON.
S2		Single pole-double throw; sim to AT1DGRA1-SPDT.
S3	19B800010P2	Push switch.
		- - - INTEGRATED CIRCUITS - - - - -
U1-U8	19A116704P2	Linear, digital; sim to MC1489AN.
U9-U13	19A700037P361	Digital, address selector; sim to 74LSD151.
U14		RS-232 Line driver; sim to Maxim MAX230CPP.
U15	19A700037P421	Digital counter; sim to 74LS393N.
U16	19A700037P367	Digital synchronous 4-bit counter; sim to 74LS160AN.
U17,U18	19A700037P335	Digital flip-flop; sim to 74LS74AN.
U20	19J706247P2	Digital PROM display driver.
U21,U22		Digital, display; sim to Tll311.
U23	19A701865P1	Digital timer; sim to NE555P.
U24	19A700037P303	Digital quad 2-input NOR gate; sim to 74LS 02N.
U25	19A700037P335	Digital flip-flop; sim to 74LS74AN.
U26,U27	19A7039897P16	Digital counter; sim to 74HC4020N.
U28,U29	19A700037P381	Digital 4-bit up/down counter; sim to 74LS193.
U30	19A700037P303	Digital quad 2-input NOR gate; sim to 74LS02N.

SYMBOL	PART NUMBER	DESCRIPTION
		- - - - - - -SOCKETS -- - - - - - - -
XU20	19A700156P9	Socket.
XU21-XU22		Socket, 19-pin; sim to Aries-14-822-90C
Y1,Y2		Crystal CTS Knight; sim to MXO-55GA-2C-4.9152MHz.
		- - - - MISCELLANEOUS - - - - - - - -
		Card handle; sim to VERO 21-0243G PULL.

PRODUCTION CHANGES

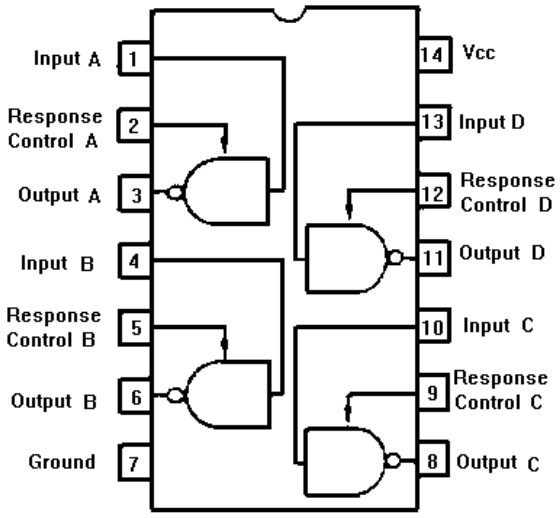
Changes in the equipment to improve or to simplify circuits are identified by a "Revision Letter" which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the description of parts affected by these revisions.

REV. A - DATA SELECTOR MODULE 19D902519G1. Incorporated in initial shipment.

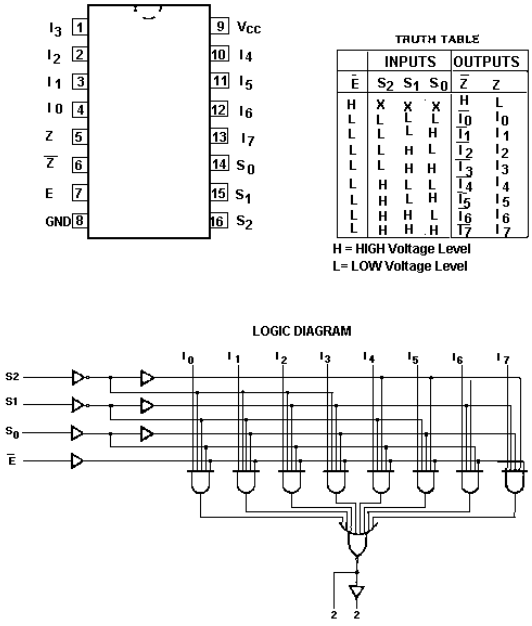
REV. B - To improve operation. Added ground to SW3-11, added pulse fill capability and 4800 Hz clock option. Added C69, D2, R14, J4-J7, AND P5-P7.

Refer to Parts List for parts description.

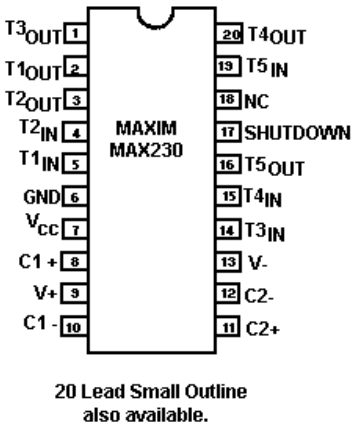
REV. C - To improve Power-Up operation. Deleted capacitors C33 through C66.



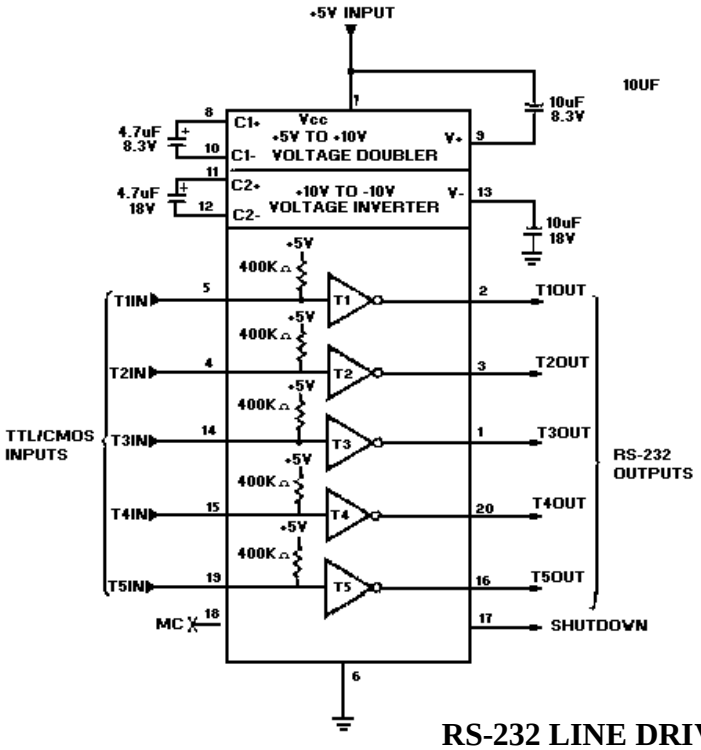
RS-232C LINE RECEIVERS U1-U8
MC1489AN



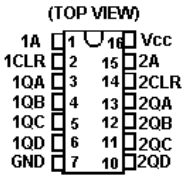
ADDRESS SELECTORS U9-U13
74LS151N



20 Lead Small Outline
also available.

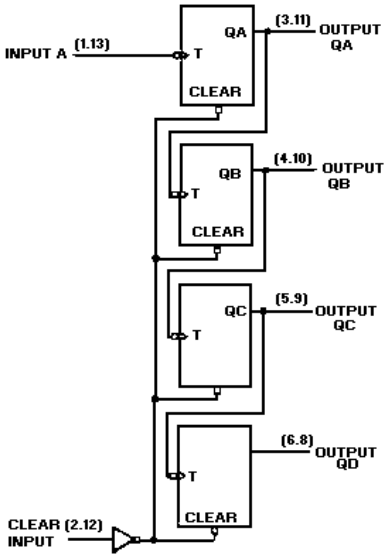


RS-232 LINE DRIVERS U14
MAX230CPP

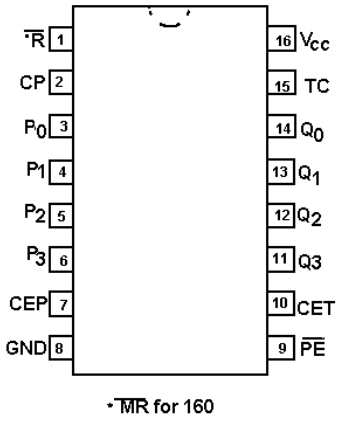


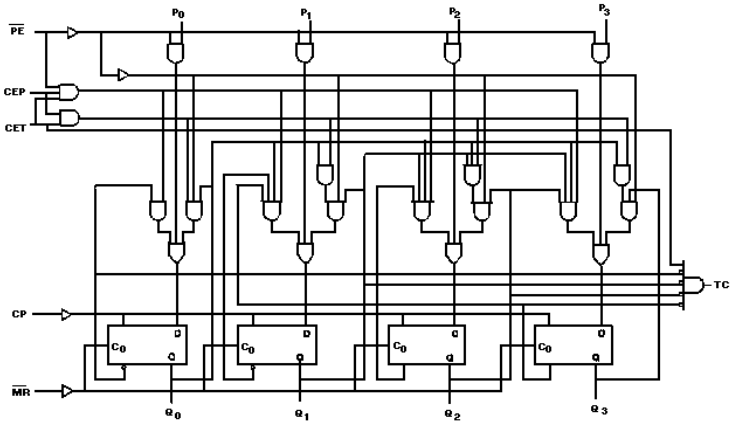
COUNT SEQUENCE
(EACH COUNTER)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H



COUNTERS U15, U19
SN74LS393N

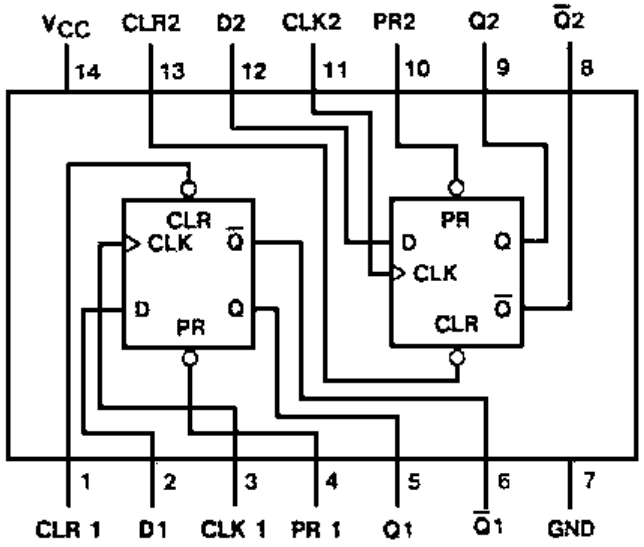




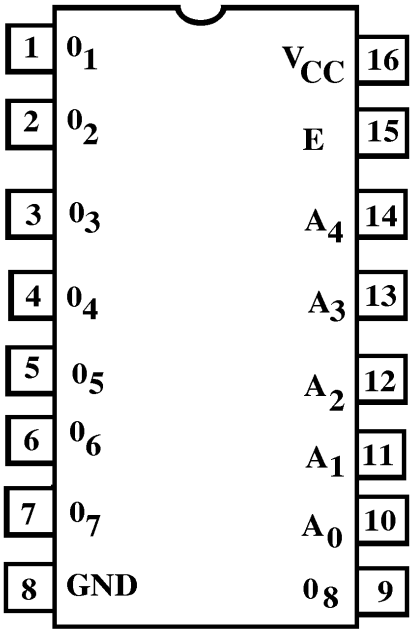
DECADE COUNTER U16
74L9160AN

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

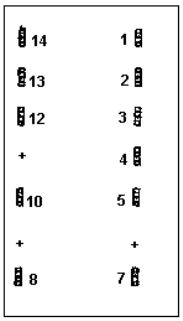
Notes: Q0 = the level of Q before the indicated input conditions were established.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



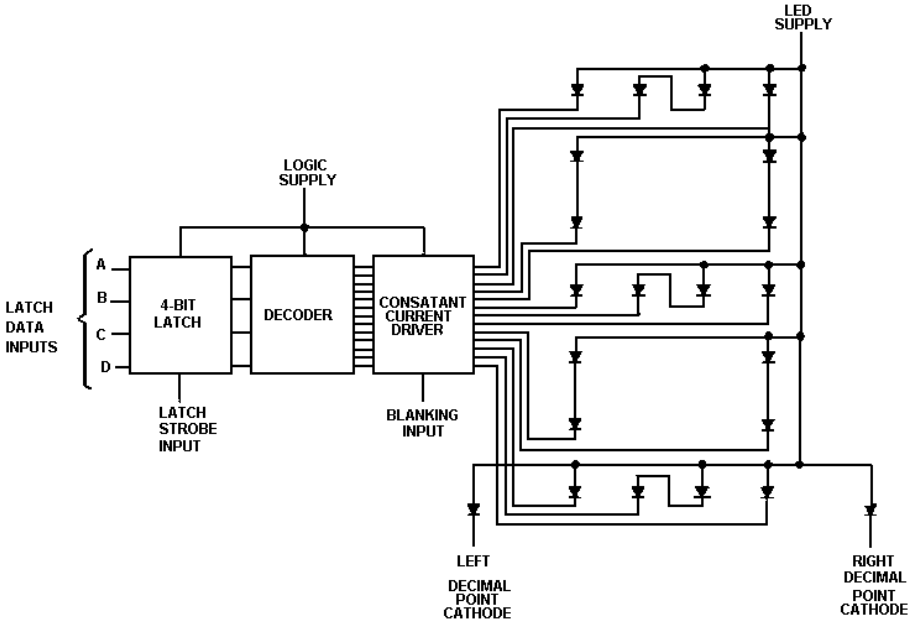
FLIP-FLOPS U17, U18 AND U25
SN74LS74AN



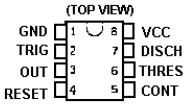
DISPLAY DRIVER 32 X 8 PROM U20
DM74LS288N



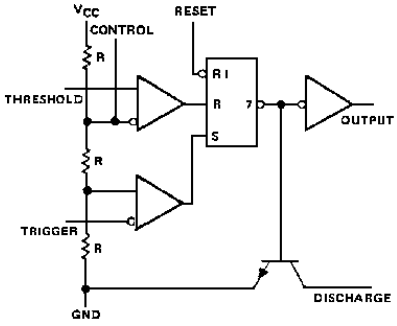
PIN 1 LED SUPPLY VOLTAGE
PIN 2 LATCH DATA INPUT B
PIN 3 LATCH DATA INPUT A
PIN 4 LEFT DECIMAL POINT CATHODE
PIN 5 LATCH SROBE INPUT
PIN 6 OMITTED
PIN 7 COMMON GROUND
PIN 8 BLANKING INPUT
PIN 9 OMITTED
PIN 10 RIGHT DECIMAL POINT CATHODE
PIN 11 OMITTED
PIN 12 LATCH DATA INPUT D
PIN 13 LATCH DATA INPUT C
PIN 14 LOGIC SUPPLY VOLTAGE, V_{CC}



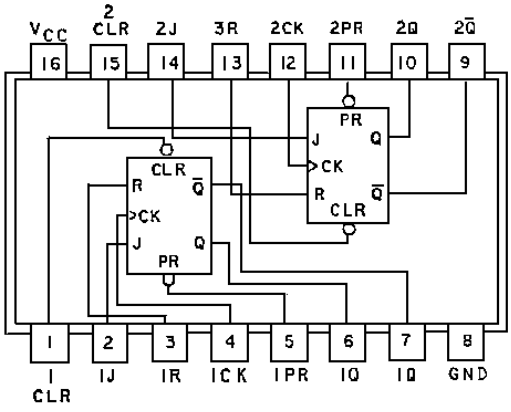
LED DISPLAY U21 AND U22
T1L311



functional block diagram

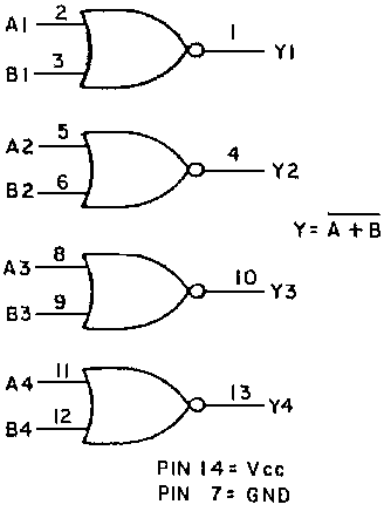


TIMER U23
ME55SN



COUNTERS U28, U29
74LS193

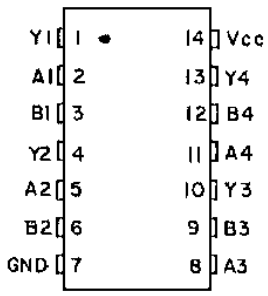
LOGIC DIAGRAM



$Y = \overline{A + B}$

PIN 14 = Vcc
PIN 7 = GND

PIN ASSIGNMENT

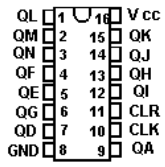


FUNCTION DIAGRAM

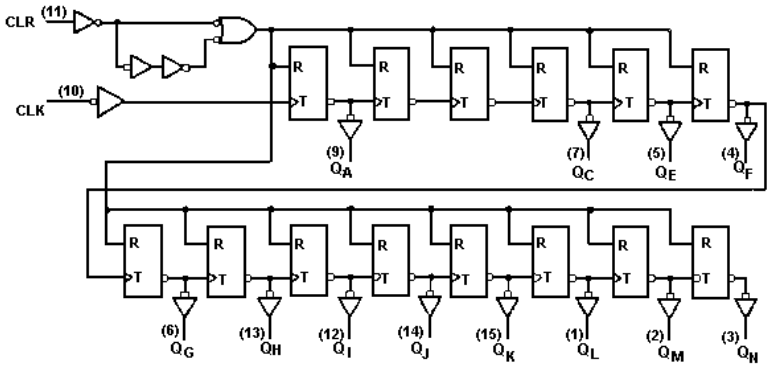
INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

NOR GATE U24, U30
SN74LS02N

(TOP VIEW)



logic diagram (positive logic)



COUNTER U26 AND U27
SN74HC4020N

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