MAINTENANCE MANUAL
ANALOG DELAY MODULE
19D902526G1

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SPECIFICATIONS

- Tables 1 through 4 depict the specifications of the Analog Delay Module.
- Table 1 outlines the general specifications.
- Table 2 outlines the power drain specifications.
- Tables 3 through 5 outline the connector interface.
- Table 6 outlines the Dip switch definition.
- Tables 1 through 6 depict the specifications as it relates to the actual operation as part of the EDACS™ Simulcast System.

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SPECIFICATIONS
(Continued)

Table 1 - General Specifications

ITEM	SPECIFICATION
POWER SUPPLY	+5 VOLTS ± 5%
TEMPERATURE	0 TO +60 DEGREES C
DIMENSION	VME STYLE - 6U , 220 MM
DIGITAL/DATA TYPE	TTL
ANALOG/AUDIO TYPE	VOICE/DATA GRADE AUDIO
DELAY	32 ms (max)

Table 2 - Power Specification

VOLTAGE	CONNECTOR POINT	• TOLERANCE ± %	CURRENT DRAIN TYPICAL mA	CURRENT DRAIN MAXIMUM mA	CURRENT DRAIN STANDBY mA
GND	P1-A2 P1-C2 P1-A31 P1-C31 P2-A2 P2-C2 P2-A31 P2-C31	NA	NA	NA	NA
+5	P1-A1 P1-C1 P1-A32 P1-C32 P2-A1 P2-C1 P2-A32 P2-C32	5	1200	2000	NA

SPECIFICATIONS
(Continued)

Table 3 - Connector P1 Definition

CONNECTOR PIN	SIGNAL NAME	INPUT/ OUTPUT	ANALOG/ DIGITAL	LEVEL DIGITAL DC-VOLT AC-VRMS
P1A1	+5	I	D	5 V
P1C1	+5	I	D	5 V
P1A2	GND	I/O	D	0 V
P1C2	GND	I/O	D	0 V
P1A3	OUT1+	O	A	-10 DBM
P1C3	OUT1-	O	A	-10 DBM
P1A5	OUT2+	O	A	-10 DBM
P1C5	OUT2-	O	A	-10 DBM
P1A7	OUT3+	O	A	-10 DBM
P1C7	OUT3-	O	A	-10 DBM
P1A9	OUT4+	O	A	-10 DBM
P1C9	OUT4-	O	A	-10 DBM
P1A11	OUT5+	O	A	-10 DBM
P1C11	OUT5-	O	A	-10 DBM
P1A13	OUT6+	O	A	-10 DBM
P1C13	OUT6-	O	A	-10 DBM
P1A15	OUT7+	O	A	-10 DBM
P1C15	OUT7-	O	A	-10 DBM
P1A17	OUT8+	O	A	-10 DBM
P1C17	OUT8-	O	A	-10 DBM
P1A19	OUT9+	O	A	-10 DBM
P1C19	OUT9-	O	A	-10 DBM
P1A21	OUT10+	O	A	-10 DBM
P1C21	OUT10-	O	A	-10 DBM
P1A24	OUT11+	O	A	-10 DBM
P1C24	OUT11-	O	A	-10 DBM
P1A26	OUT12+	O	A	-10 DBM
P1C26	OUT12-	O	A	-10 DBM
P1A28	OUT13+	O	A	-10 DBM
P1C28	OUT13-	O	A	-10 DBM
P1A31	GND	I/O	D	0 V
P1C31	GND	I/O	D	0 V
P1A32	+5	I	D	5 V
P1C32	+5	I	D	5 V

Continued

SPECIFICATIONS
(Continued)

Table 4 - Connector P2 Definition

CONNECTOR PIN	SIGNAL NAME	INPUT/ OUTPUT	ANALOG/ DIGITAL	LEVEL DIGITAL DC-VOLT AC-VRMS
P2A1	+5	I	D	5 V
P2C1	+5	I	D	5 V
P2A2	GND	I/O	D	0 V
P2C2	GND	I/O	D	0 V
P2A3	IN1+	I	A	-10 DBM
P2C3	IN1-	I	A	-10 DBM
P2A5	IN2+	I	A	-10 DBM
P2C5	IN2-	I	A	-10 DBM
P2A7	IN3+	I	A	-10 DBM
P2C7	IN3-	I	A	-10 DBM
P2A9	IN4+	I	A	-10 DBM
P2C9	IN4-	I	A	-10 DBM
P2A11	IN5+	I	A	-10 DBM
P2C11	IN5-	I	A	-10 DBM
P2A13	IN6+	I	A	-10 DBM
P2C13	IN6-	I	A	-10 DBM
P2A15	IN7+	I	A	-10 DBM
P2C15	IN7-	I	A	-10 DBM
P2A17	IN8+	I	A	-10 DBM
P2C17	IN8-	I	A	-10 DBM
P2A19	IN9+	I	A	-10 DBM
P2C19	IN9-	I	A	-10 DBM
P2A21	IN10+	I	A	-10 DBM
P2C21	IN10-	I	A	-10 DBM
P2A23	BSEL	I	A	TTL
P2A24	IN11+	I	A	-10 DBM
P2C24	IN11-	I	A	-10 DBM
P2A26	IN12+	I	A	-10 DBM
P2C26	IN12-	I	A	-10 DBM
P2A28	IN13+	I	A	-10 DBM
P2C28	IN13-	I	A	-10 DBM
P2A31	GND	I/O	D	0 V
P2C31	GND	I/O	D	0 V
P2A32	+5	I	D	5 V
P2C32	+5	I	D	5 V

Continued

SPECIFICATIONS
(Continued)

Table 5 Connector P3 Definition

CONNECTOR PIN	SIGNAL NAME	INPUT/ OUTPUT	ANALOG/ DIGITAL	LEVEL DIGITAL DC-VOLT AC-VRMS
1	A0	I	D	TTL
2	A1	I	D	TTL
3	A2	I	D	TTL
4	A3	I	D	TTL
5	A4	I	D	TTL
6	A5	I	D	TTL
7	A6	I	D	TTL
8	A7	I	D	TTL
9	A8	I	D	TTL
10	A9	I	D	TTL
11	A10	I	D	TTL
12	A11	I	D	TTL
13	A12	I	D	TTL
14	A13	I	D	TTL
15	A14	I	D	TTL
17	GND	I/O	D	0 V
18	+5	O	D	5 V
20	BSEL	I	D	TTL

SPECIFICATIONS
Continued

Table 6 - Dip Switch Definition

DIP SWITCH	BINARY CODE
S1 - 8	BIT 0 OF A (PRIMARY) DELAY A LSB
S1 - 7	BIT 1 OF A (PRIMARY) DELAY
S1 - 6	BIT 2 OF A (PRIMARY) DELAY
S1 - 5	BIT 3 OF A (PRIMARY) DELAY
S1 - 4	BIT 4 OF A (PRIMARY) DELAY
S1 - 3	BIT 5 OF A (PRIMARY) DELAY
S1 - 2	BIT 6 OF A (PRIMARY) DELAY
S1 - 1	BIT 7 OF A (PRIMARY) DELAY
S2 - 8	BIT 8 OF A (PRIMARY) DELAY
S2 - 7	BIT 9 OF A (PRIMARY) DELAY
S2 - 6	BIT 10 OF A (PRIMARY) DELAY
S2 - 5	BIT 11 OF A (PRIMARY) DELAY
S2 - 4	BIT 12 OF A (PRIMARY) DELAY
S2 - 3	BIT 13 OF A (PRIMARY) DELAY
S2 - 2	BIT 14 OF A (PRIMARY) DELAY A MSB
S2 - 1	BSEL CONTROL (0=A DELAY, 1=B DELAY)
S3 - 8	BIT 0 OF B (SECONDARY) DELAY B LSB
S3 - 7	BIT 1 OF B (SECONDARY) DELAY
S3 - 6	BIT 2 OF B (SECONDARY) DELAY
S3 - 5	BIT 3 OF B (SECONDARY) DELAY
S3 - 4	BIT 4 OF B (SECONDARY) DELAY
S3 - 3	BIT 5 OF B (SECONDARY) DELAY
S3 - 2	BIT 6 OF B (SECONDARY) DELAY
S3 - 1	BIT 7 OF B (SECONDARY) DELAY
S4 - 8	BIT 8 OF B (SECONDARY) DELAY
S4 - 7	BIT 9 OF B (SECONDARY) DELAY
S4 - 6	BIT 10 OF B (SECONDARY) DELAY
S4 - 5	BIT 11 OF B (SECONDARY) DELAY
S4 - 4	BIT 12 OF B (SECONDARY) DELAY
S4 - 3	BIT 13 OF B (SECONDARY) DELAY
S4 - 2	BIT 14 OF B (SECONDARY) DELAY
S4 - 1	BIT 15 OF B (SECONDARY) DELAY B MSB

DESCRIPTION

The Delay Unit assembly houses the Digital Delay backplane on the left side of the card cage and the Audio Delay backplane on the right side of the card cage. The card cage is a 6 rack units (Ru) (10.5 inches) high and will accommodate 20 delay modules. The Analog Delay Module are installed in the Analog Delay Backplane of the Delay Unit Assembly. Up to 10 Analog Delay Modules can be installed in the Audio Delay backplane. Ten Analog Delay Modules will support a 10 site, 25 channel system.

The Delay Unit assembly is used only at the control point. The Analog Delay Module performs the bulk audio delay to one particular transmit site. The number of Analog Delay Modules in the Delay Unit assembly is equal to the number of transmit sites in the system, for systems having 12 channels or less and twice that number for systems having greater than 12 channels.

The Analog Delay Module provides the delay of all voice and 150 baud data to the transmit sites in order to ensure equal time of arrival of the audio signals in the simulcast overlap region.

The Analog Delay Module performs the bulk delay on 13 signals. The 13 audio inputs are delayed by the same offset (time) and sent through the multiplexer to the transmit site.

The audio to be delayed is derived from the 25 audio outputs from the audio equalizer subsystem and the audio bridge located in the audio processing shelf #2 (slot 1) for the 150 baud low speed data from Data Selector 1.

The selection of the amount of audio delay is set by a bank of dip switches. Two Dip switches set up the amount of the primary audio delay and two Dip switches set up the secondary path audio delay. The second delay is used only if a ring connection is made between transmit sites.

The audio delay is performed in increments of 1 microsecond with a maximum delay of 32 milliseconds.

The audio delay is performed via the analog to digital conversion of the audio, subsequent time delay of the digital data stream via a RAM based FIFO buffer, and followed by the digital to analog conversion back to audio.

CIRCUIT AND FUNCTIONAL DESCRIPTION

The Analog Delay Module performs the delay of the voice and the 150 baud data used in the simulcast system. Each module performs the audio delay on 12 voice signals and the 150 baud FSK signal (low speed data) or 13 voice signals.

The audio delay is performed using digital techniques. The audio is sampled and converted to a digital serial stream via a **CODEC** (U23 - U35). The digital serial stream of 8 bits per sample is stored in 8 successive addresses in a RAM (U18 - U21). The contents of the RAM are read back out with an address offset from the address used to store the data in the RAM. This address offset is the mechanism by which the delay audio is generated. The read address recovers the delay 8 bit sample, where it is sent back to the **CODEC** to be transformed back into audio.

The RAM is addressed via a set of two addresses formed from a free running counter (U5 - U8) along with a fixed offset as set up by the **A** (primary) offset (S1, S2) or **B** (secondary) offset (S3, S4). The RAM is configured as a FIFO buffer with the free running counter and the offset adder serving as the FIFO ram controller.

Four quad 2:1 multiplexers, U1 - U4, can select the **A** (primary) offset, the **B** (secondary) offset, or zero (min offset). The **A** or **B** offsets are selected via the **BSEL** control line. The **BSEL** control is generated from a setting on the Dip switch, from the alarm/control system, or from an optional external control input. The choice of zero address is made via the timing and control logic on the Analog Delay Module during periods of storing the sampled data from the **CODECS**.

Four 4-bit binary counters (U5 - U8) are used to generate the free running counter. The free running counter is driven by a 1 MHz clock (output of U22).

Four 4-bit adders (U9 - U12) comprise the address generator to the RAM. The adder inputs are the free running counter and the offset address multiplexer. The timing for the **CODECS** are also generated from the outputs of the adders.

The timing and control section of the Analog Delay Module consists of a 10 MHz TTL oscillator (M1), a registered **PAL** (**P**rogrammable **A**rray **L**ogic) device (U22), two dual D-type flip flops (U14, U15), and a **NOR** gate (U13). The NOR gate and flip-flops are used to generate the transmit and receive frame sync pulses to the **CODECS**. The **PAL** device uses the TTL oscillator and the frame sync pulses from the flip flops to generate the master and bit clocks to the **CODECS**, along with the read, write, and enable controls to the RAM's.

Four RAM's (U18 - U21) are used to store the serial data stream from the 13 audio sources (12 voice channels, FSK signalling).

Two tri-state buffers (U16, U17) are used to present the sampled data to the RAM's to be stored.

Thirteen **CODECS** are used, one to sample each of the audio signals.

Twenty six transformers are used to couple the incoming (from the audio equalizer subsystem) audio and the outgoing (to the multiplexer/channel bank) audio from the **CODECS**.

A DC to DC converter (M2) is used on the Analog Delay Module to generate the -5 volt power required by the **CODECS**.

An optional connector (P3) is used on the Analog Delay Module to provide an input from an external device to control the address selection.

A general block diagram of the Analog Delay Module is shown in Figure 1.

The **CODECS** require that the negative 5 volts be applied to the circuits before the positive voltage is applied. This function is performed by U36A and relay K1. All codes have an IN4148 diode from -5 volts to ground to ensure that the -5 volts supply line never goes positive.

CONNECTORS AND SYSTEM INTERFACE

There are 3 connectors on the Analog Delay Module, P1, P2, and P3. Connectors P1 and P2 are used to mate the Analog Delay Module to the Audio Delay backplane of the Delay Unit assembly. Connector P3 is used for an optional external internal interface to allow remote control of the delay offset address.

A description of the various signals on the connectors is summarized in Tables 3 - 5.

ANALOG DELAY MODULE AND CROSS CONNECT PANEL SIGNAL FLOW

The audio equalizer subsystem obtains the voted voice from the analog voter and performs the gain and group delay equalization on the voice band audio. The bulk delay is performed via the Analog Delay Module. The FSK signalling is the audio band representation of the low speed data from the Data Selector Module/ Audio Bridge. Up to 13 signals are bulk delayed by one Analog Delay Module for one transmit site.

IN1+ - IN13+

IN1+ through **IN13+** are the signals (tip) from the audio equalizer subsystem along with the FSK low speed signalling from the audio bridge located in Audio Pro-cessing shelf #2.

IN1- - IN13-

IN1- through **IN13-** are the signals (ring) from the audio equalizer subsystem along with the FSK low speed signalling.

OUT1+ - OUT13+

OUT1+ through **OUT13+** are the signals (ring) from the Analog Delay Module to the multiplexer.

OUT1- - OUT13-

OUT1- through **OUT13-** are the signals (tip) from the Analog Delay Module to the multiplexer.

BSEL

BSEL is the offset select control line which selects either the **A** (primary) path or the **B** (secondary) path.

DIP SWITCH DEFINITION

The Dip switch (S1-S4) definition and configuration is summarized in Table 6.

Switches S1 and S2 select the **A** (primary) path delay while switches S3 and S4 select the **B** (secondary) path delay. Switch S2 (position 1) also allows the capability to manually select the **B** (secondary) path.

The Dip switches allow a delay to be established as set up by 15 bits of the **A** delay switches or 16 bits of the **B** delay switches.

The switches have a binary weighting to perform the delay. The least significant bit (**A0** or **B0**) is capable of a delay equal to the clock period of the free running counter. The possible delays range from the minimum as set by all switches closed (zero address offset) to maximum as set by all switches open (maximum address offset).

The minimum address offset is set by the binary address given as:

minimum address offset =
000 0000 0000 0000 (A path)
0000 0000 0000 0000 (B path)

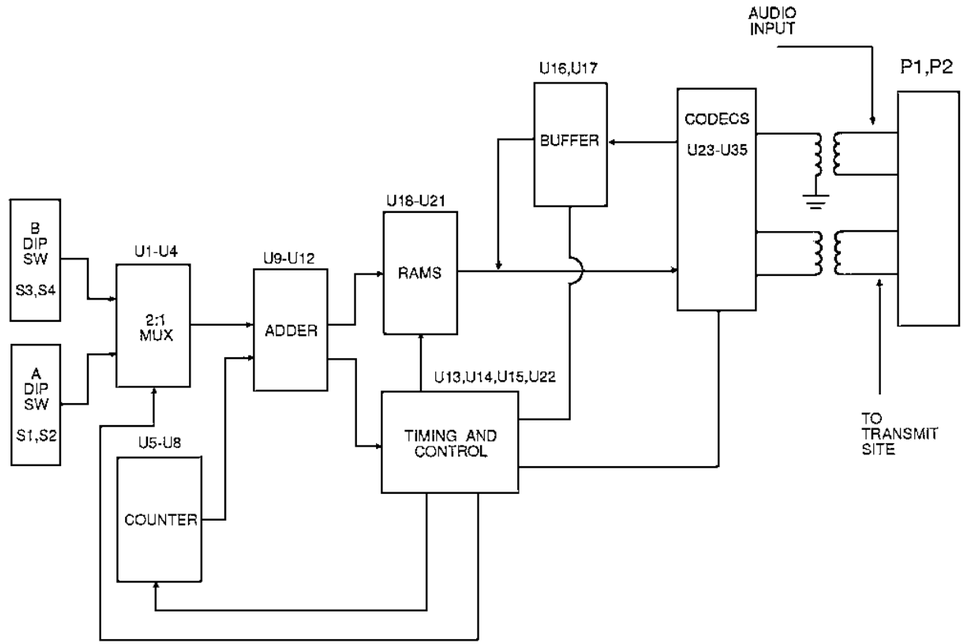


Figure 1 - Analog Delay Module Block Diagram

The maximum address offset is set up the binary address given as:

maximum address offset =
111 1111 1111 1111 (A path)
1111 1111 1111 1111 (B path)

The offset delay is determined from the address offset, the clock period, and the delay time through the **CODEC**.

The clock period is 1 µSEC. The **CODEC** delay time consists of sampling the input, converting to a digital serial stream, and finally converting the serial data stream back to audio signal. The **CODEC** sampling and conversion time is determined by the timing and control chain. This time is given by:

T(CODEC) = 128 µSEC (receive sample) + 128 µSEC (transmit sample)

Since this time is constant from **CODEC** to **CODEC**, it merely represent an inherent fixed delay.

The minimum offset delay is given by: minimum offset delay = 256 µSEC

The maximum offset delay is given by:

Maximum offset delay =
256 µSEC + 1 µSEC (32768) (A path)
256 µSEC + 1 µSEC (65536) (B path)

A closed form equation for the offset delay is given by:

$$\text{OFFSET DELAY} = [256 + 2^{(\text{address})}]_{\text{units in µSEC}}$$

Note that the binary address is the exponent of the base, 2.

A closed form equation for the address required to achieve a specified delay is given by:

$$\text{ADDRESS} = \text{LOG}_2\,[\text{OFFSET DELAY} - 256]$$
$$= 3.32 * \text{LOG}_{10}\,[\text{OFFSET DELAY} - 256]$$

— Offset Delay given in µSEC

POWER DISTRIBUTION AND FILTERING

The +5 volt power supply used by the Analog Delay Module is obtained from the simulcast power supplies. The +5 volt power is used to energize the digital logic devices, the RAM's, the TTL oscillator, and the **CODECS**. The positive 5 volts is switched to the **CODEC** through relay K1. This ensures that the negative 5 volts is present when the positive voltage is applied. This prevents the **CODEC** from going into a latched condition. All **CODEC** also have a diode from the negative 5 volts to ground to ensure that the V_{BB} input to the **CODEC** never goes positive.

The +5 volt power is also used by the DC to DC converter, M2, to generate the onboard -5 volt power to the **CODECS**. There are filter and bypass capacitors on the Analog Delay Module to filter any power noise transients or spikes from affecting circuit operation and module performance. Capacitors C27 through C48 are 0.1 µF in value and are used as bypass filters near the digital logic devices and the a RAM's. Capacitor C49 is a 100 µF component and provides the bulk filter on the +5 volt power. Capacitors C1 through C26 are 0.1 µF in value and are placed at the supply inputs to the CODECS on the +5 volt and -5 volt power lines.

TIMING AND CONTROL CHAIN

The timing and control chain of the Analog Delay Module provides the clocking to the **CODECS** and the read/write pulses to the RAM's. The timing and control chain consists of NOR gate, (U13), flip-flops, (U14, U15), PAL device (U22), and the TTL oscillator, (M1).

The TTL oscillator, M1, provides the basic clock from which all other clocks and pulses are derived. It operates at 10 MHz and is input to the PAL device, (U22).

The **PAL** device is a registered programmable and/or array with 8 D-type outputs. The inputs to the **PAL** device are the transmit frame sync clock (**FSX**) and the receive frame sync clock (**FSR**). The frame sync clocks are generated from the address decoding of the RAM address. The **FSX** clock is generated from the free running coun-ter and the offset address (**A** or **B** offset), while the **FSR** clock is generated from the free running counter only. The write address (which is generated during the **FSX** pulse) is higher than the read address (which is gen-erated during the **FSR** pulse) by the amount as programmed via the offset Dip switches. The sampled serial data stream from the **CODEC** therefore is stored at the a logically higher address and is read back some time later when the read address has incremented up to the higher addresses.

The frame sync clocks are derived from the NAND gate and flip-flops. The **NAND** gate utilizes four lines from the adders to generate a multiplexed frame clock for the transmit and receive sections of the **CODECS**. The frame sync clocks are demultiplexed via flip-flops, (U14, U15). To generate the **FSX** and **FSR** clocks to the **CODECS** and the **PAL** device. The frame sync clocks are pulses of a high time of 8 **CODE**C data bit times (1 usec per bit time or 8 usec total) and a frame clock period of 128 **CODEC** data bit times (1 µsec per bit time or 128 µsec total).

Figure 2 depicts the timing diagrams for the timing and control chain.

AUDIO SAMPLING AND GENERATION

The audio receive, analog to digital conversion, digital to analog conversion and audio transmit functions are performed by the **CODECS**. The major functions of the **CODECS** also include bandpass filtering of the audio signals prior to encoding and after encoding, encoding and decoding of the audio, and encoding and decoding of the clock and signalling. The **CODECS** are clocked in the variable data rate mode. This mode allows for a flexible data frequency to be set up equal to the pre-scribed 1 µsec maximum delay time increment in the simulcast system.

The clocks to the **CODEC** include the master clock (2 MHz) on pin 9 of each **CODEC**, the receive and transmit data clocks (1 MHz) on pins 5 and 12 of each **CODEC**, the transmit frame sync clock (7.8 KHz) on pin 10 of each **CODEC** and the receive frame sync clock (7.8 KHz) on pin 7 of each **CODEC**.

The frame sync clocks are high for 8 µsec and low for 120 µsec. The master clock is a 50 percent duty cycle clock. The transmit and receive data clocks are a 50 percent duty cycle clock.

The transmit section of the **CODEC** consists of the transmit filter and the transmit encoder. The input audio enters the **CODECS** through input transformers. The transformers couple the audio to the **CODECS**. A 600 ohm resistor provides the terminating load to the transformer secondary. Two resistors are used to provide unity gain to the input of the **CODECS** on pins 14 and 15.

The transmit input section provides gain adjustment in the passband by an operational amplifier, which has a common mode range of 2.17 volts. The gain of the amplifier is set for 0 dB via the two resistors on pins 15 and 14 of the **CODEC**. A low pass anti-aliasing section is include in the **CODEC** to provide 35 dB of attenuation at the sampling frequency (7.8 KHz). The transmit passband provides flatness and stopband attenuation. The transmit encoder samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor. The encoder then performs an analog to digital conversion. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame when **FSX** is high.

The receive section of the **CODEC** consists of the receive decoder, the receive filter and the output power amplifiers. The pulse code modulated word (8 bits) is serially fetched on the first eight data clock bits of the frame when FSR is high. A digital to analog conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. The sample is then transferred to the receive filter. The receive filter provides flatness and stopband rejection as well as providing the required compensation for the sampling (**sin x/x**) distortion. A balanced output amplifier is provided in order to allow the differential outputs to drive a transformer directly. The differential outputs from the **CODECS** are transformer coupled to the multiplexer.

FIFO RAM ADDRESS GENERATION

The address to the RAMs (U18 - U21) is generated at the output of the adders. The address is time multiplexed to generate the read address and the write address to the rams. The read address is the free running counter value and is used to read an eight bit continuous sample from the RAMs to be input to the **CODECS**. The eight bit continuous sample is read coincident with the activation of **FSR**.

The write address is the sum of the free running counter value plus the address offset and is used to write an eight bit continuous sample from the **CODECS** to the RAMs. The eight bit continuous sample is written coincident with the activation of **FSX**. At any one point in time, the write address is equal to the read address plus the fixed offset address (delay offset). The read address (generated from the free running counter) will eventually be positioned to read the present data stored but at a later point in time (when the read address or free running counter has incremented enough).

MAINTENANCE

The Analog Delay Module has dip switches that must be configured for the audio delay on both the **A** (primary) and **B** (secondary) paths. The offset delay desired in terms of the address was given in closed form. The **BSEL** control line on dip switch S2-1 must be set for the desired mode of operation given below:

S2-1 BSEL SWITCH SETTING

OPEN : SELECT B PATH DELAY, OR ENABLE ALARM AND CONTROL UNIT OVERRIDE, OR ENABLE REMOTE CONTROL OVERRIDE

CLOSED : SELECT A PATH DELAY ALWAYS

No other adjustments are necessary in order to place the Analog Delay Module into operation.

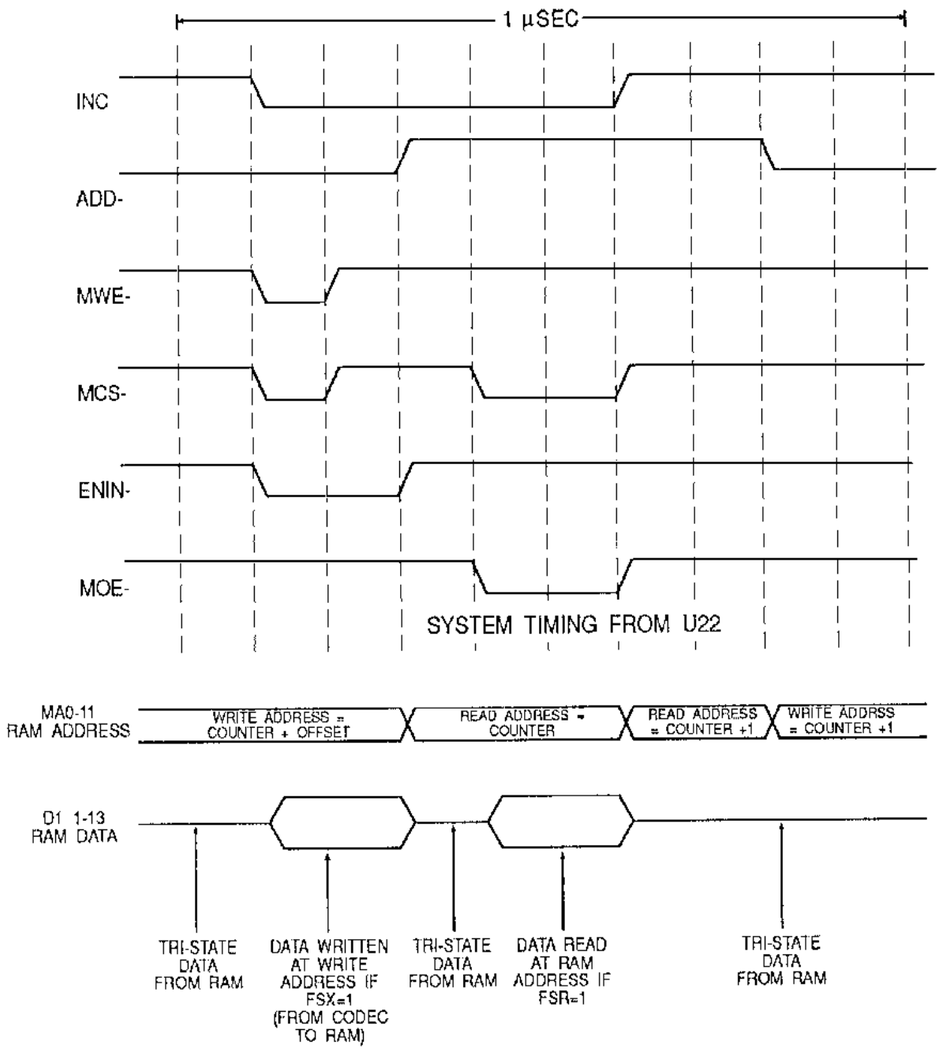


Figure 2 - Timing And Control Chain Timing Diagrams

TEST AND SERVICE

The equipment required to test the Analog Delay Module:

1. Extender Card
2. Tektronix 2430A/1R Digital Storage Scope or equivalent
3. Triplett Model 630-PL Type 5 or equivalent
4. Test Cables as required
5. HP 8116A/001 Pulse/Function Generator or equivalent

To test the Analog Delay Module:

1. Configure the Dip switches for the desired **A** (primary) and **B** (secondary) path delays. Also configure the **BSEL** Dip switch for the desired mode of operation.
2. Install the Analog Delay Module as part of the operational simulcast system.
3. Verify the presence of +5 volt power (+5) and -5 volt power (-5).
4. Verify the generation of the 10 MHz clock. Verify the generation of the master clock, 2 MHz, on pin 9 of **CODECS**.

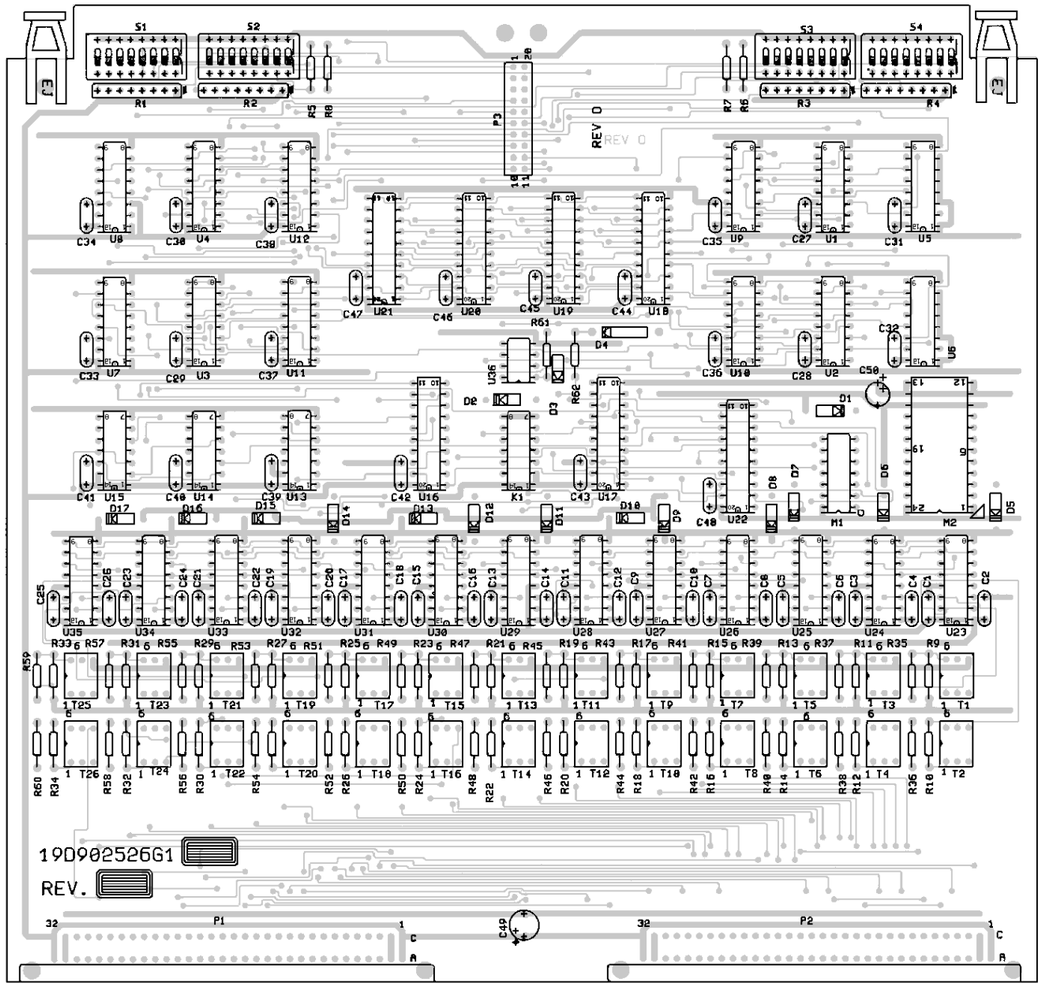
   Verify the generation of the data clocks, 1 MHz, on pins 5, 12 of **CODECS**.

   Verify the generation of the **FSR** clock, 7.8 kHz and 6.25 % duty cycle (high).

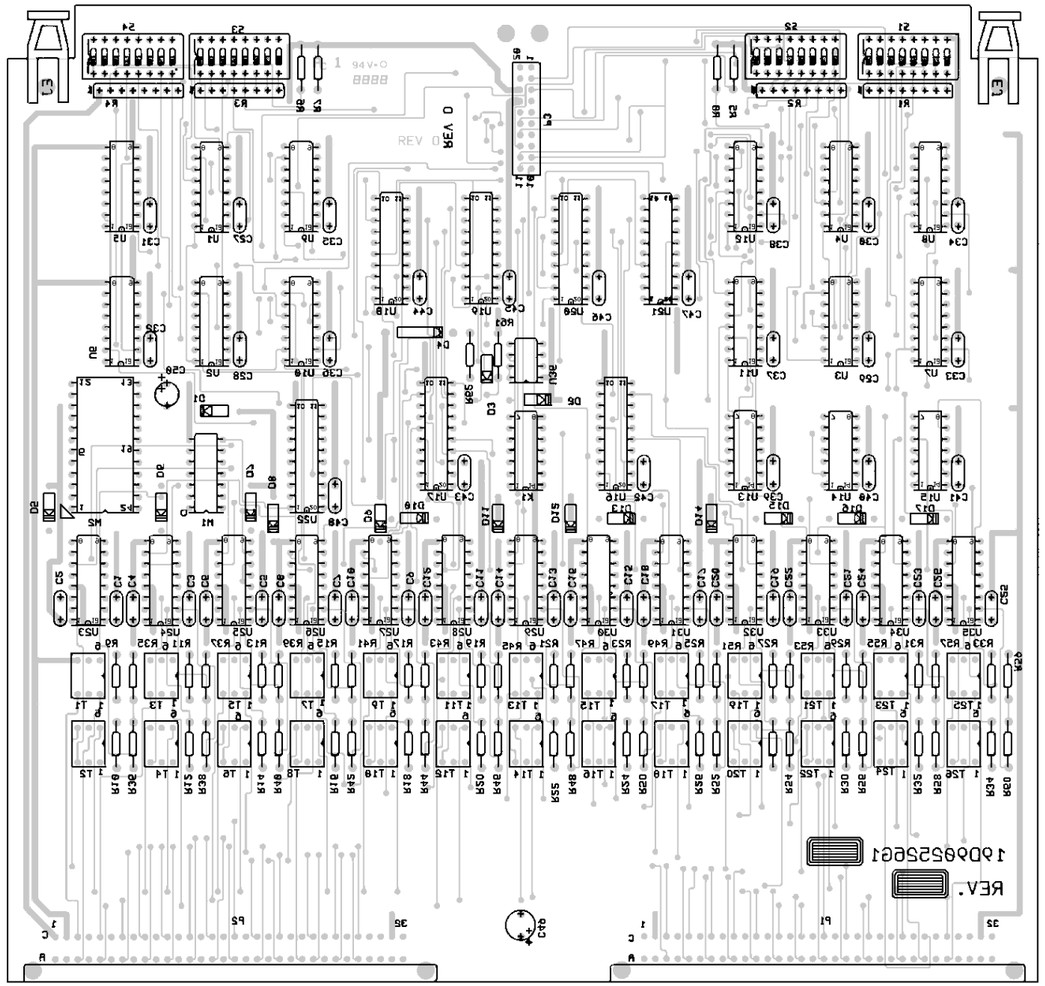
   Verify the generation of the FSX clock, 7.8 kHz and 6.25 % duty cycle (high).

   Input an audio signal (100 Hz test tone at -10 dBm) to the audio signal under test. Verify that the primary address offset delays the audio input to the audio output. Verify each bit of the address offset Dip switch selection. Verify each audio input channel for delay operation. Verify the secondary address offset delay selection via the Dip switches.

COMPONENT SIDE

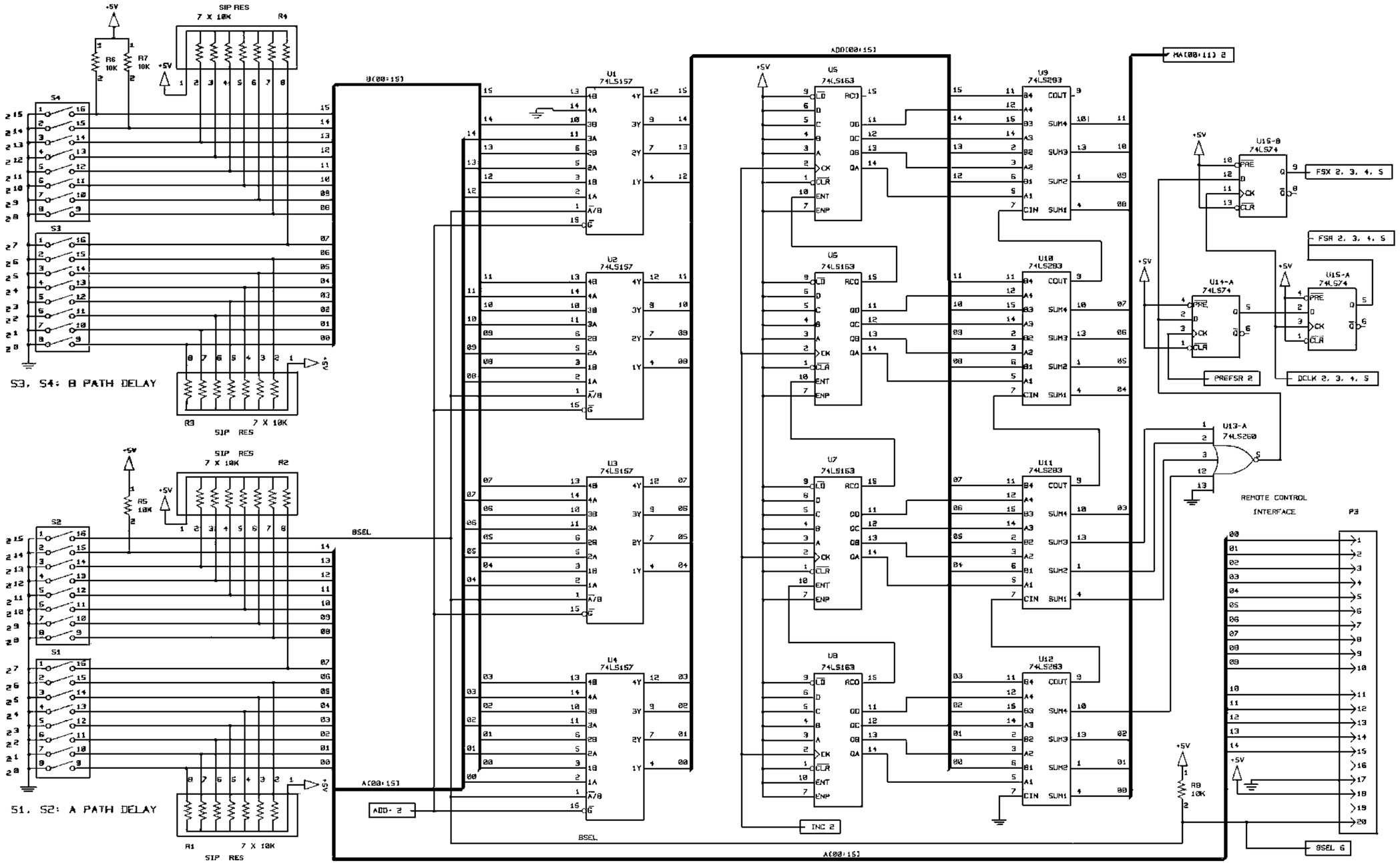


SOLDER SIDE

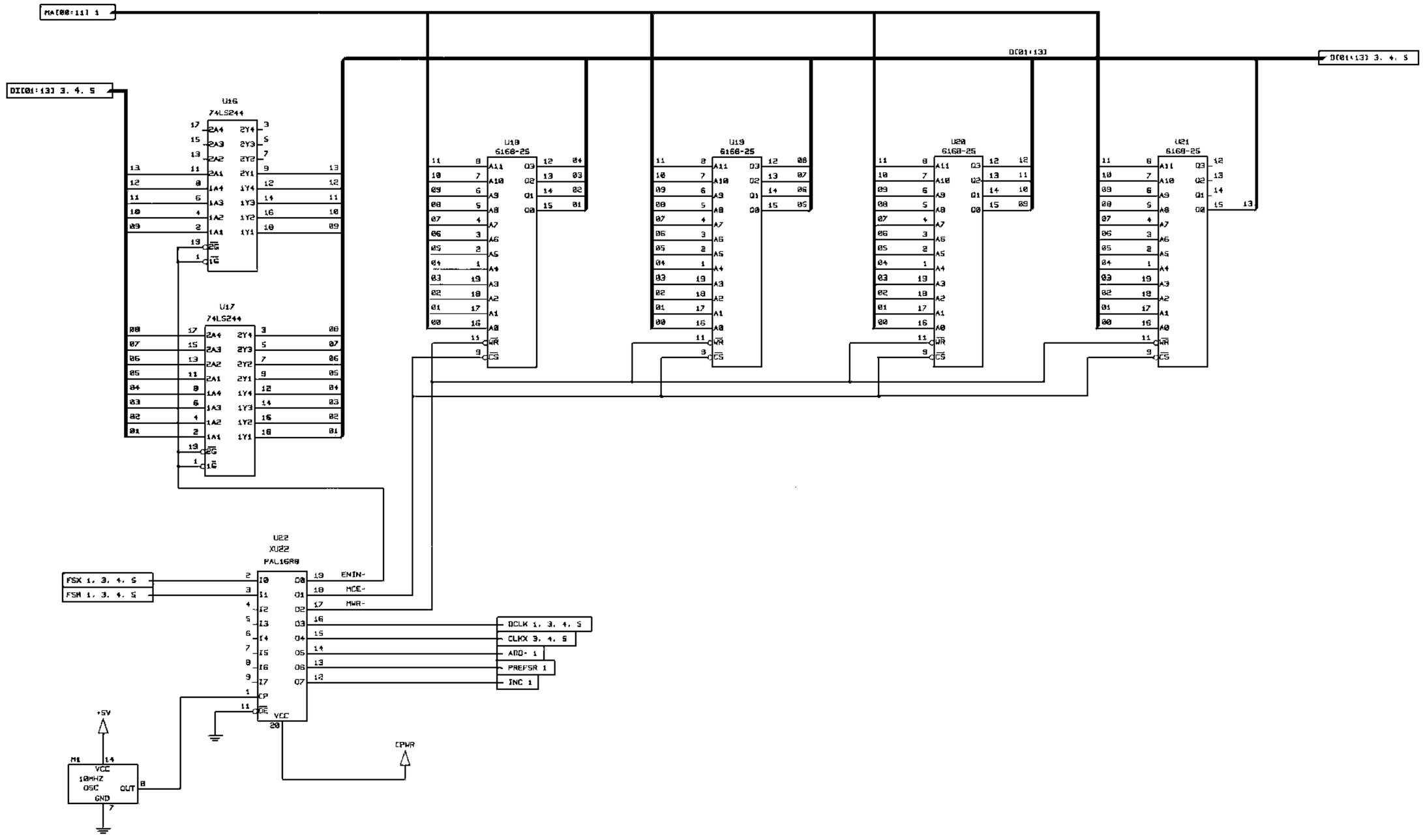


ANALOG DELAY MODULE
19D902526G1

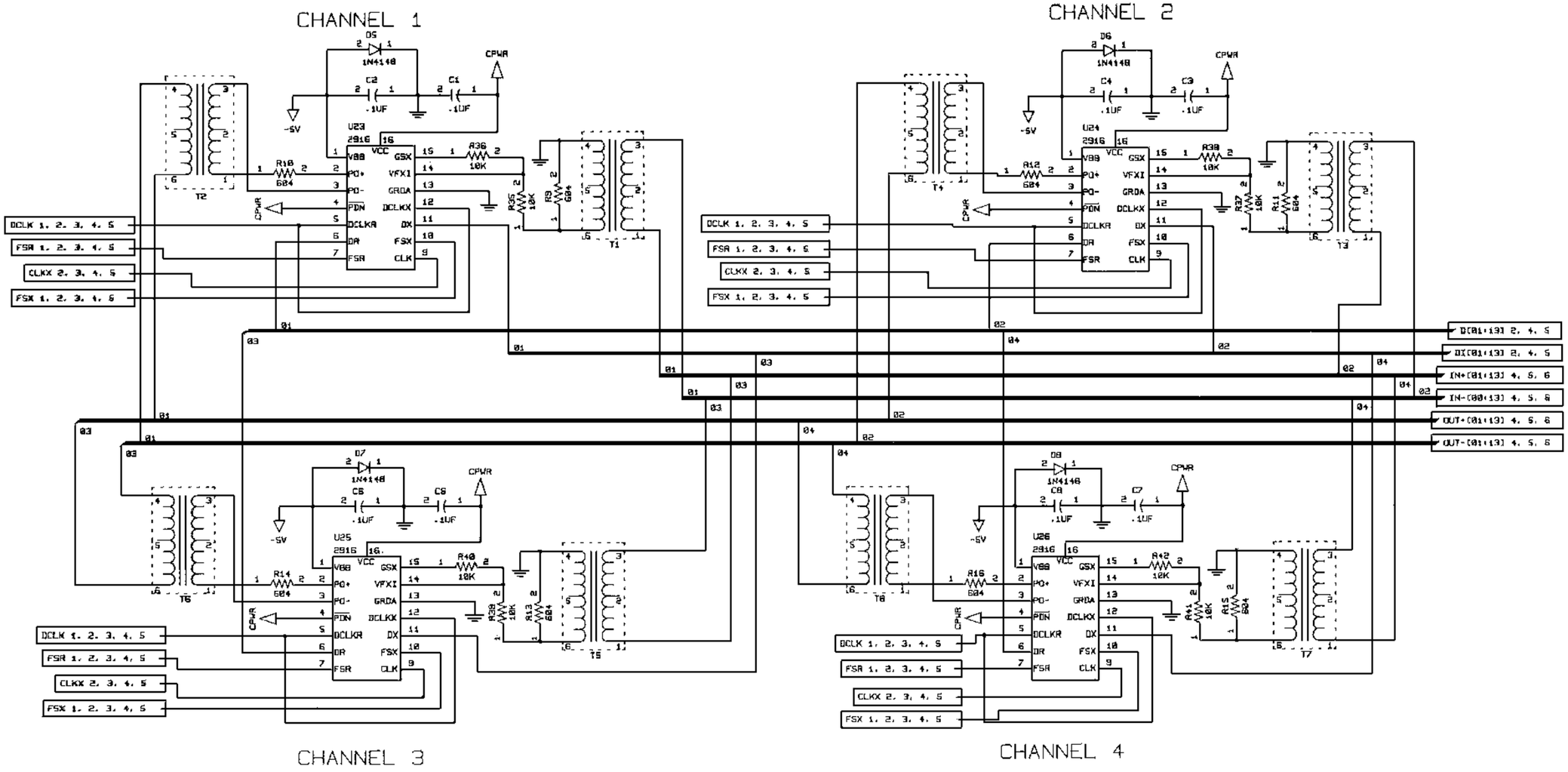
(19D902526, Sh. 1, Rev. 0)
(ADS D008, Component Side, Rev. 0)
(ADS D008, Solder Side, Rev. 0)



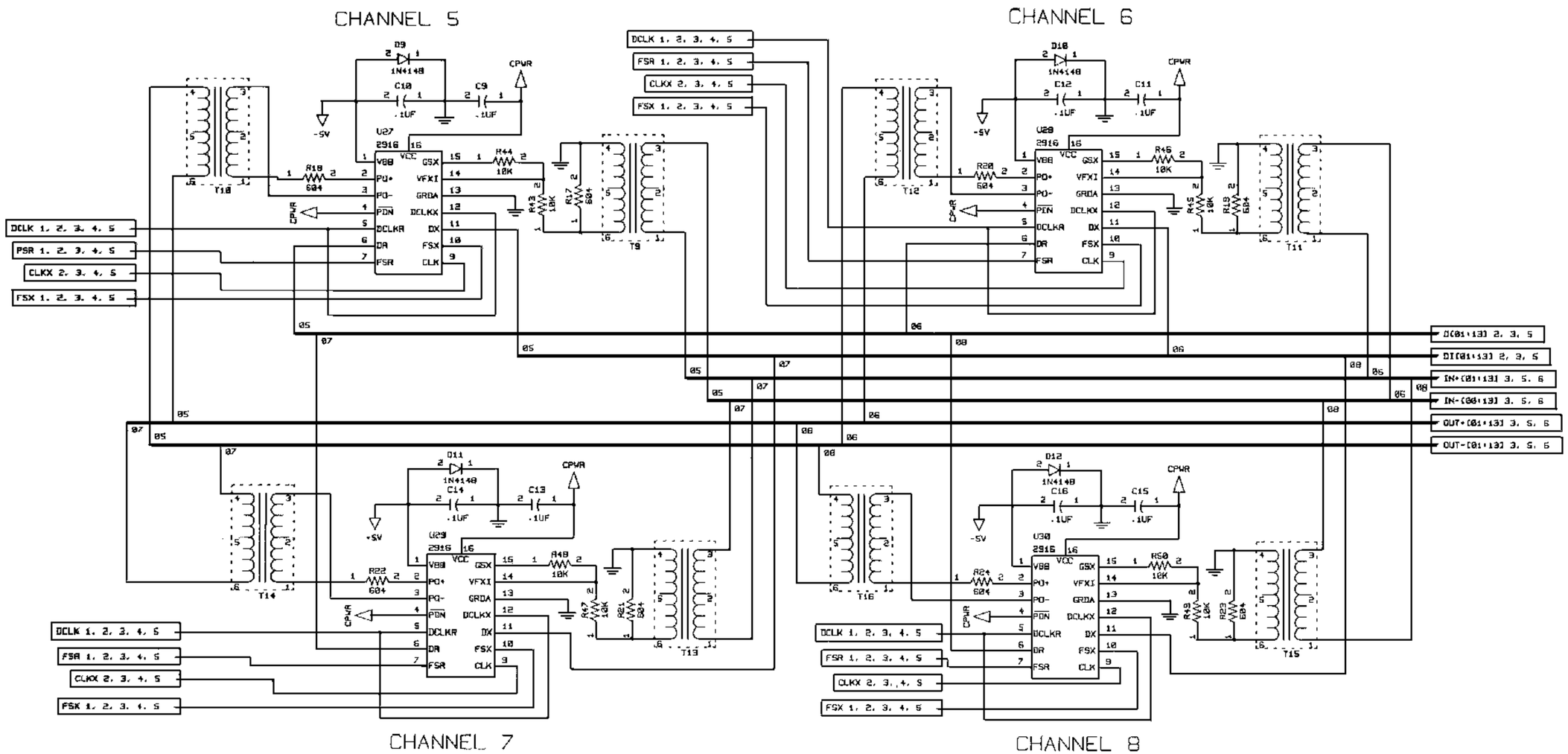
(19C851929, Sh. 1, Rev. 1)



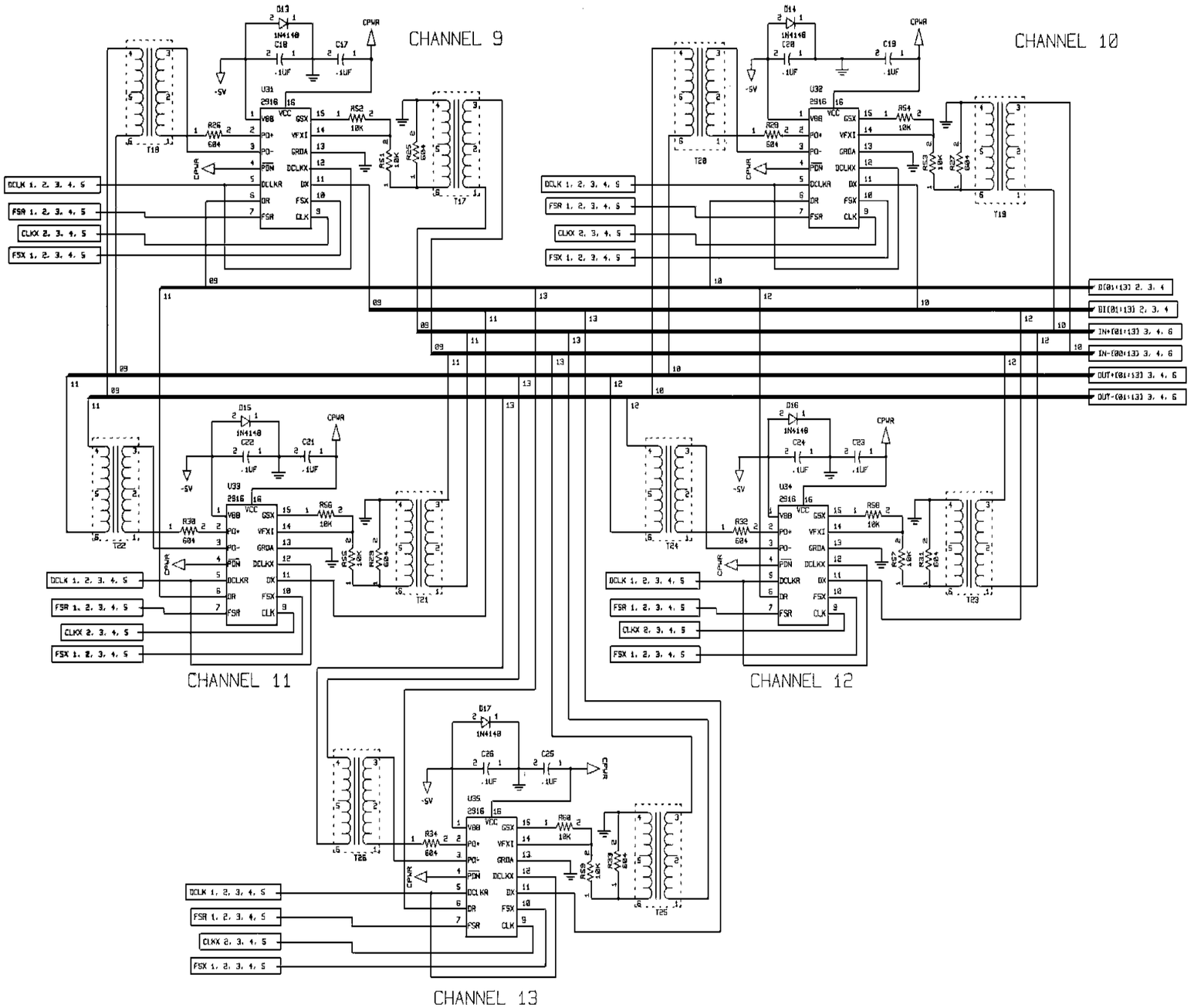
(19C851929, Sh. 2, Rev. 1)



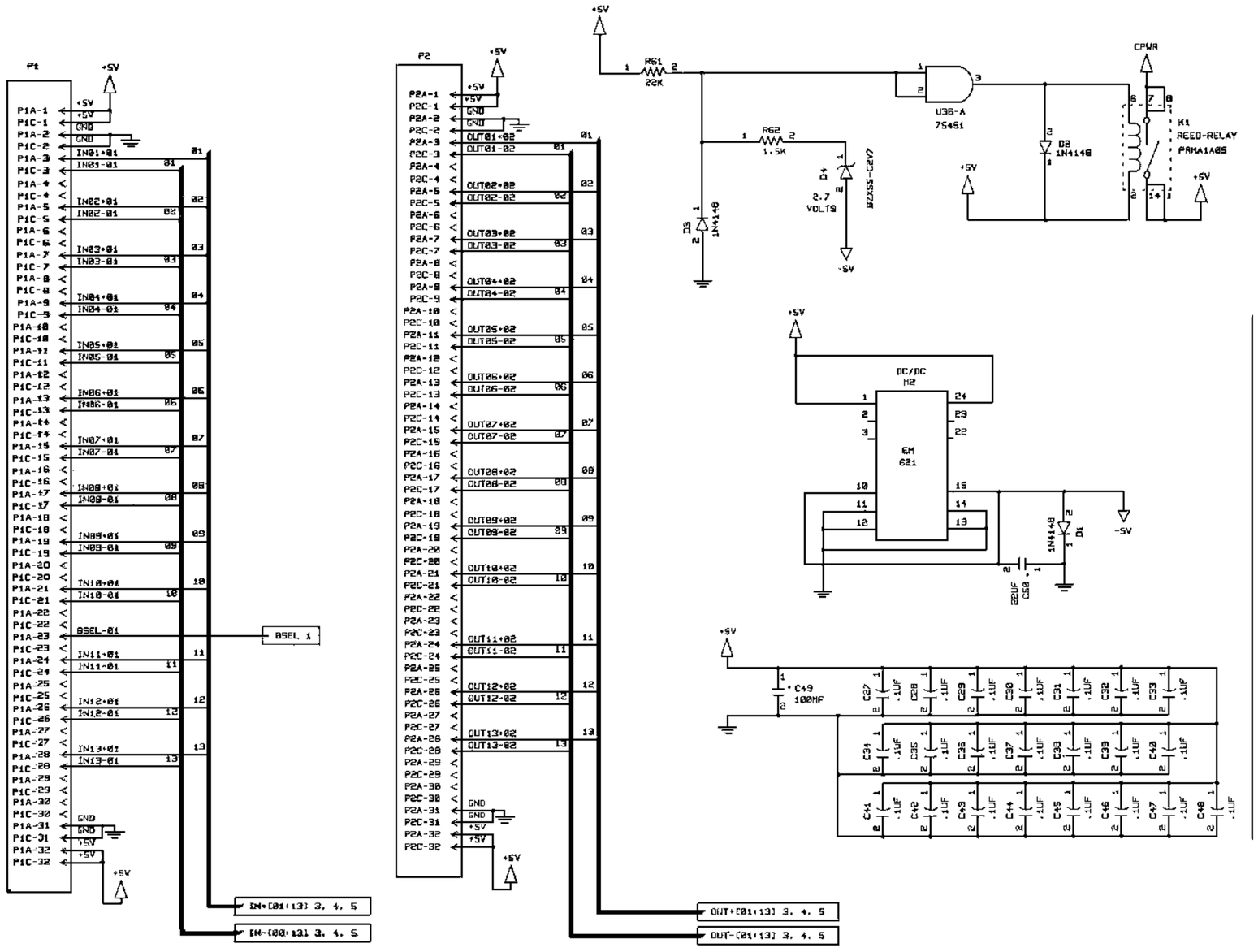
(19C851929, Sh. 3, Rev. 1)



(19C851929, Sh. 4, Rev. 1)

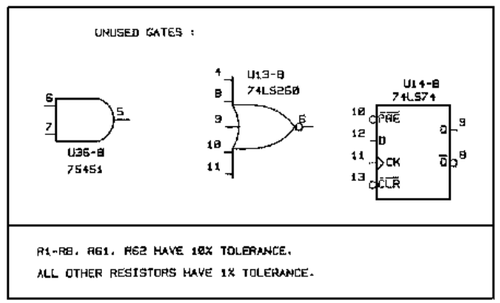


(19C851929, Sh. 5, Rev. 1)



NOTES AND TABLES :

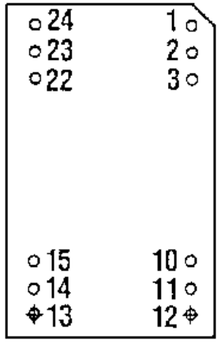
POWER & GROUND TABLE			
DEVICE	+5V	GND	CPWR
U1 - U12	16	8	-
U13 - U15	14	7	-
U16 - U21	20	10	-
U22	-	10	20
U23 - U35	-	8	16
U36	8	4	-



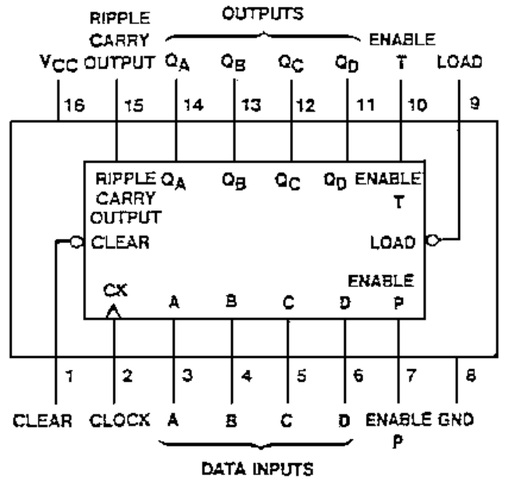
(19C851929, Sh. 6, Rev. 1)

DC TO DC CONVERTER M2
EM621

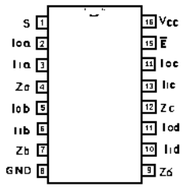
PIN NO.	SINGLE OUTPUT MODULE
1	+V Input
2	Do Not Connect
3	Do Not Connect
9	
10	−V Output
11	+V Output
12	−V Input
13	−V Input
14	+V Output
15	−V Output
22	Do Not Connect
23	Do Not Connect
24	+V Input

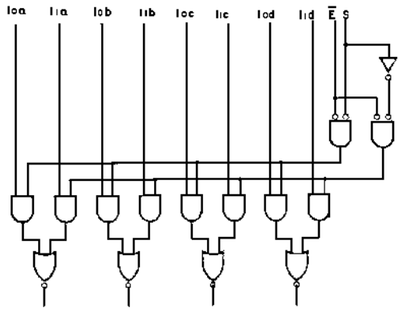


COUNTERS U5-U8
74LS163

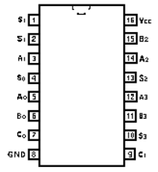


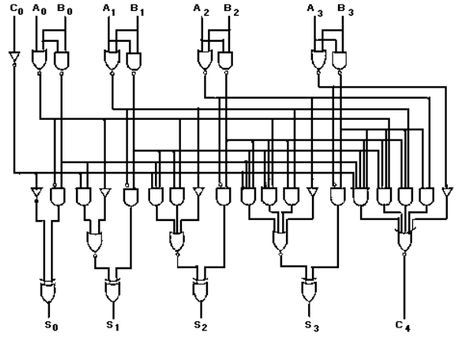
MULTIPLEXERS U1-U4
74LS157





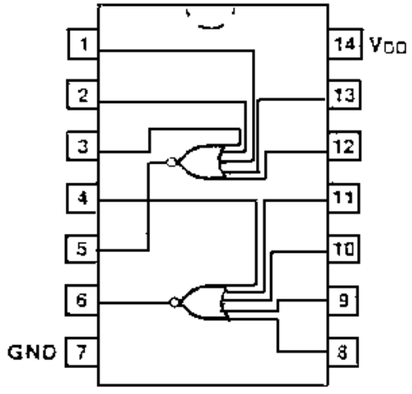
FOUR BIT ADDERS U9-U12
74LS283





NOR GATE U13
72LS260

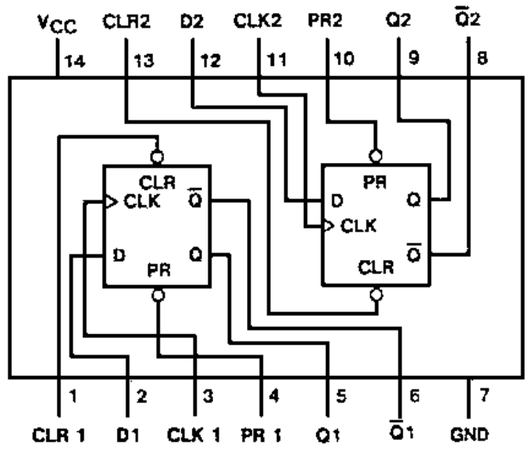
DUAL 5-INPUT NOR GATE



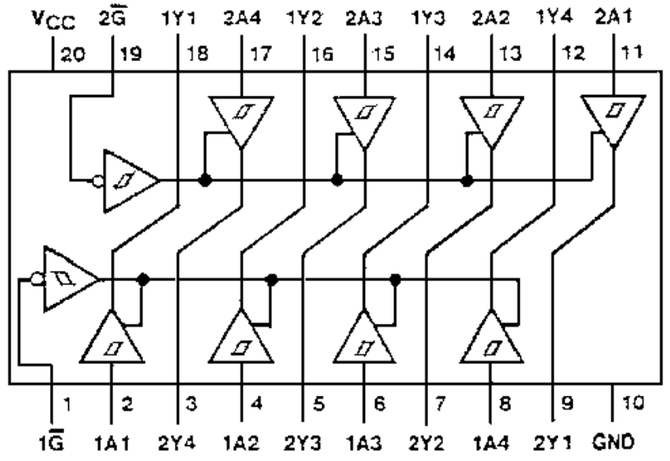
D-TYPE FLIP-FLOPS U14 AND U15
74LS74

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

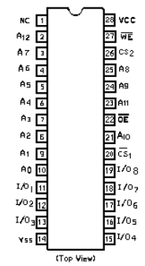
Notes: Q0 = the level of Q before the indicated input conditions were established.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



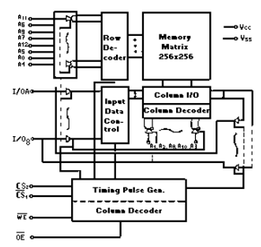
TRI-STATE BUFFERS U16 AND U17
74LS244



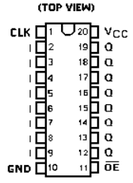
RAM U18-U21
HM6264

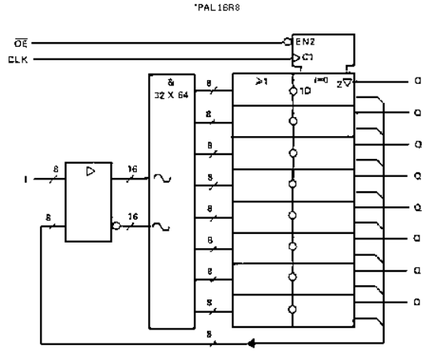


■ BLOCK DIAGRAM

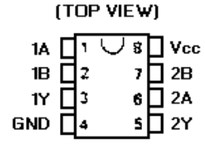


PROGRAMMABLE ARRAY LOGIC U22
PAL16R8A-4





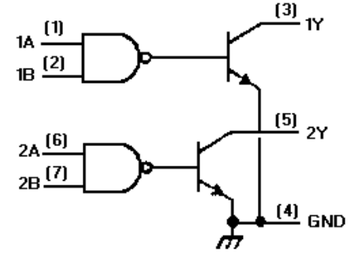
AND GATE U36
75451



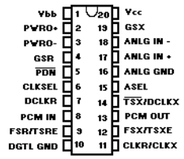
FUNCTION TABLE
(EACH DRIVER)

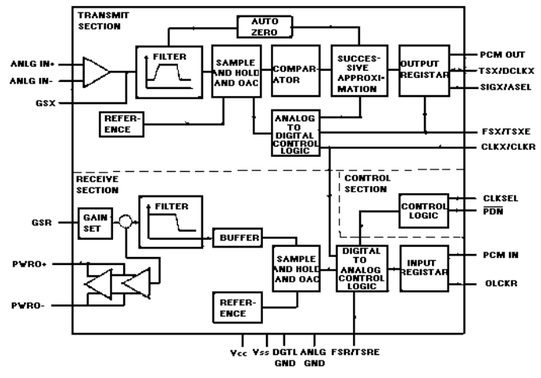
A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

logic diagram (positive logic)



CODEC U23-U35
TCM29C16





SYMBOL	PART NUMBER	DESCRIPTION
		— — — — CAPACITORS — — —
C1 thru C48	T644ACP410K	Polyester: .1 µF.
C49	19A703314P1	Electrolytic: 100 µF, 10 VDCW.
C50	19A703314P5	Electrolytic: 22 µF, 25 VDCW.
		— — — — — DIODES — — — —
D1 thru D3	19A70028P1	Diode.
D4	19A70025P2	Silicon.
		— — — — — — RELAY — — — —
K1	19B209716P1	Relay, reed.
		— — — — — MODULES — — —
M1	CTS MXO-55GA	Module: 10 MHz.
M2	EM621	Module.
		— — — — — — PLUGS — — — —
P1 and P2		DIN, 64 Pins.
P3		HEADER, 20 Pins.
		— — — — — RESISTORS — — —
R1 thru R4	4308R-101-103	Resistor.
R5 thru R8	H212CRP310C	Carbon film: 10K ohms, .2 w.
R9 thru R34	19A701250P176	Metal film: 604 ohms ±1%, 1/4 w.
R36 thru R60	19A701250P301	Metal film: 10 ohms ±1%, 1/4 w.
R61	H212CRP322C	Carbon film: 22K ohms, .2 w.
R62	H212CRP2178	Carbon film: 1.8K ohms, .2 w.
		— — — — — SWITCHES — — —
S1 thru S4	GRAYHILL 8832T	Switch.
		— — — — TRANSITORS — — —
T1 thru T26	PM34-M	Transistor.

SYMBOL	PART NUMBER	DESCRIPTION
		— — INTEGRATED CIRCUITS —
U1 thru U4	74LS157	Integrated Circuit.
U5 thru U8	74LS173	Integrated Circuit.
U9 thru U12	74LS283	Integrated Circuit.
U13	72LS260	Integrated Circuit.
U14 thru U15	74LS74	Integrated Circuit.
U16 thru U17	74LS244	Integrated Circuit.
U18 thru U21	HM6264	Integrated Circuit, 4K X 4.
U22	PAL16R8A-4	Integrated Circuit.
U23 thru U35	TCM29C16	Integrated Circuit.
U36	75451	Integrated Circuit.
		— — — — SOCKETS — — — —
XU22	19A700156P13	Socket.
		— — — MISCELLANEOUS — —
	VERO 21-0243G	Card Handle.

* COMPONENTS, ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES