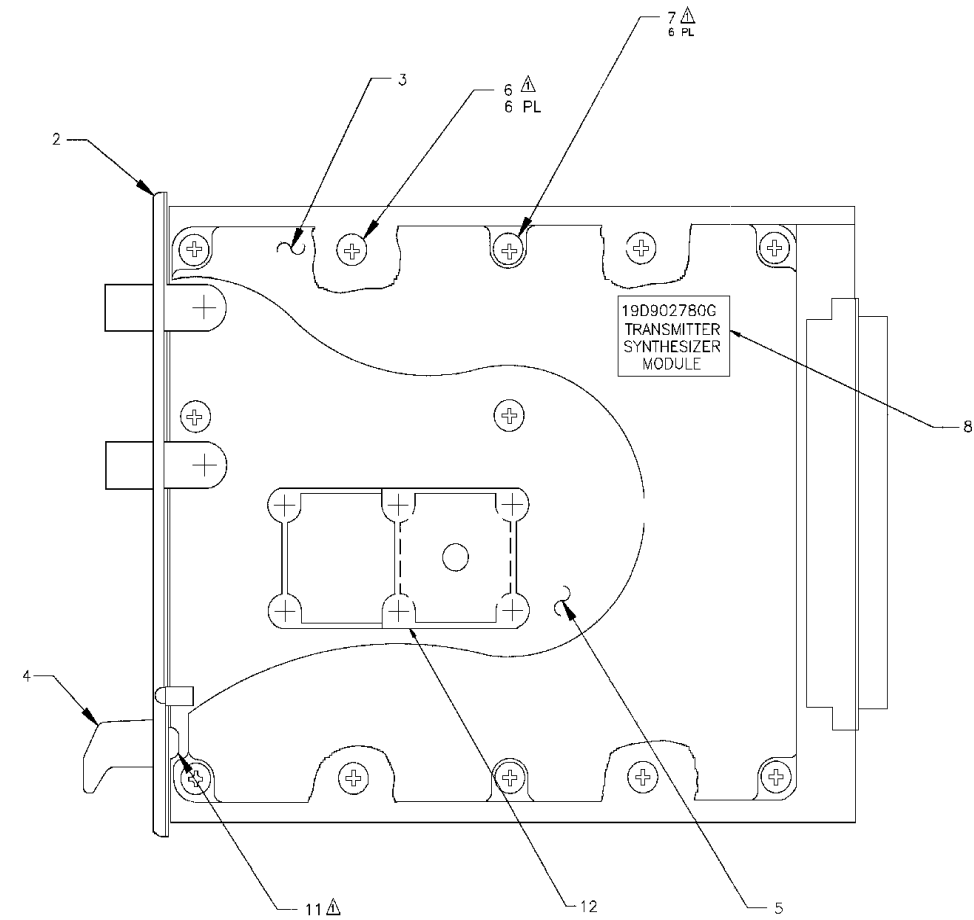
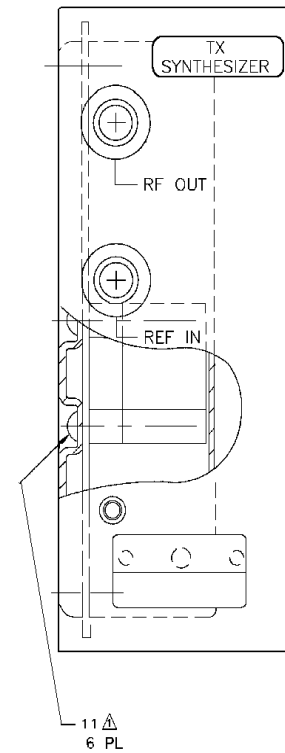


**MAINTENANCE MANUAL  
FOR  
UHF TRANSMITTER SYNTHESIZER MODULE  
19D902780G3, G6 - G10**

**ASSEMBLY DIAGRAM**

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NOTES:

- ⚠ TORQUE SCREWS, ITEMS 6 AND 7, TO 10.0 ± 1.3 INCH POUNDS.
- TORQUE SCREWS, ITEM 11 TO 20 ± 1.3 INCH POUNDS

**UHF TRANSMITTER  
SYNTHESIZER MODULE  
19D902780G3, G6 - G10**

(19D902780, Sh. 1, Rev. 4)

TABLE 1 - GENERAL SPECIFICATIONS

ITEM	SPECIFICATION
FREQUENCY RANGE	450-470 MHz (G3) 425-450 MHz (G7) 403-430 MHz (G6) 380-400 MHz (G8) 470-494 MHz (G9) 490-512 MHz (G10)
CHANNEL SPACING	6.25 kHz
RF POWER OUT (50 Ohm load)	10 to 13 dBm (10 to 20 mW)
RF HARMONICS	< -30 dBc
NON-HARMONIC SPURS	
1 to 200 MHz	< -90 dBc
200 MHz to 1 GHz	< -60 dBc
CARRIER ATTACK TIME	<25 mSec
REFERENCE INPUT	
input level	0 dBm $\pm$ 1.5dB
input impedance	50 Ohm
frequency	5 to 17.925 MHz (must be integer divisible by channel spacing)
MODULATION SENSITIVITY	5 kHz peak dev/1 Vrms, Adjustable
AF INPUT IMPEDANCE	600 Ohm
AF RESPONSE	
10 Hz	$\pm$ 1.5 dB
1000 Hz 0 dB reference	
3 kHz	$\pm$ 1.5 dB
10 Hz SQUARE WAVE MODULATION	
Sq wave droop	<10%
HUM & NOISE	-55 dB
POWER REQUIREMENTS	13.8 Vdc @ 275 mA -12.0 Vdc @ 10 mA

## DESCRIPTION

The principle function of the Transmitter Synthesizer Module is to provide the RF excitation for input to the MASTR III station power amplifier. The output of the synthesizer is a frequency modulated signal at the desired frequency. The module contains the following functional blocks:

- A voltage controlled oscillator.
- Frequency Doubler (Multiplier).
- A chain of integrated circuit RF Amplifiers.
- A reference buffer amplifier.
- Dual modulus prescaler and synthesizer integrated circuits.
- Loop amplifiers and passive loop filter.
- An audio amplifier and a pre-modulation integrator.

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- IC voltage regulators for +5 and -5 Vdc. A discrete component regulator for +8 Vdc, and an Operational Amplifier regulator for +4 Vdc.
- Logic circuitry: address decoder, input signal gates, and a lock indicator circuit.

## CIRCUIT ANALYSIS

### VOLTAGE CONTROLLED OSCILLATOR

Transistor Q1 and associated circuitry comprise a low noise Voltage Controlled Oscillator (VCO). Inductor L1 and associated capacitors form the oscillator resonant circuit (tank). The noise characteristic of this oscillator is dependent on the Q of this resonant circuit. The components used in the tank are specified to have especially high Q. Diode D1 aids in setting the bias point for low noise operation. (Any field replacement of oscillator parts should use identical parts).

Variable Capacitor C10 sets the fixed capacitance in the tank, and therefore sets the frequency range over which the oscillator can be voltage tuned.

The oscillator frequency is voltage tuned by the signal applied through R5 and L5 to the two varicap diodes D2 and D3. Additionally, audio modulation is applied as an AF voltage to the two varicap diodes. This RF voltage varies the oscillator frequency at an audio rate (i.e., it frequency modulates the oscillator). Low frequency audio is applied along with the varicap control voltage through R5 and L5 while high frequency audio (MOD) is applied via C16.

Resistors R6 through R9 provide a two volt negative bias on the varicap diodes.

Transistors Q101 and Q102 and associated circuitry form the oscillator enable switch. This switch allows the station control circuitry to turn the VCO ON or OFF via the ANT\_REL line. Setting the ANT\_REL line to a logic low causes Q102 to conduct. The five (5) volt output at Q102 collector (OSCON) enables the fault indicator gates, U705-3 and U705-4, and turns on Q101. Q101 starts to conduct, providing a ground path for Q1. This turns ON the VCO.

### FREQUENCY DOUBLER

Transistors Q801 and Q802 form a buffer stage to drive transistor multiplier Q803. The buffer isolates VCO Q1 from loading effects which could degrade oscillator loaded Q and hence noise performance. Transistor multiplier Q803 is tuned to pass the second harmonic of the VCO output and serves as a frequency doubler. Tank elements L802, C812-C814 and L803 form a resonant circuit and matching network to drive resistive splitter R201-R204.

### RF AMPLIFIERS

The RF chain begins with resistive splitter R201-R204 and R216-R218. The output of the splitter at R203 is attenuated by 10 dB and provides impedance matching helical filter FL201, which is tuned to pass the fundamental while rejecting harmonics by approximately 40 dB. The output of FL201 is fed thru resistive pad R205-R207 to MMIC Amplifier U201 which operates in compression. U201 drives output amplifier U202 into compression. The output amplifier is followed by a bandpass filter (C208-C210, L203-L205) and resistive attenuators (R210-R215). The final output at the front panel BNC Connector (J2) is nominally 11.5 dBm, and drives the station Power Amp.

The other output of the resistive splitter at R218 is attenuated by 20 dB and drives buffer amp U203 into compression. U203 drives the synthesizer prescaler providing a feedback signal for the synthesizer phase locked loop.

### REFERENCE BUFFER AMPLIFIER

Transistor Q401 and associated components comprise a buffer amplifier for the reference oscillator signal. (The reference oscillator signal is produced by the receiver synthesizer module of a MASTR III station.) The 0 dBm reference oscillator signal is fed through the front panel BNC connector J1. Resistor R405 provides a 50 ohm load to the reference oscillator. The output of the Reference Buffer Amplifier is fed directly to the synthesizer integrated circuit. The output level at TP9 is approximately 3 volts peak to peak.

## PRESCALER AND SYNTHESIZER

Integrated circuit U402 is the heart of the synthesizer. It contains the necessary frequency dividers and control circuitry to synthesize output frequencies by the technique of dual modulus prescaling. U402 also contains an analog sample and hold phase detector and a lock detector circuit.

Within the synthesizer (U402) are three programmable dividers which are loaded serially using the CLOCK, DATA, and ENABLE inputs (pins 11, 12, and 13 respectively). A serial data stream (DATA) on pin 12 is shifted into internal shift registers by low to high transitions on the clock input (CLOCK) at pin 11. A logic high (ENABLE) on pin 13 then transfers the program information from the shift registers to the divider latches.

The reference signal is applied to U402 pin 2 and divided by the "R" divider. This divides the reference signal down to a divided reference frequency ( $F_r$ ). The typical reference frequency is 12.8 MHz and the typical divided reference frequency is 6.25 kHz providing for synthesizer steps of 6.25 kHz for use with both 12.5 kHz and 25 kHz channel spacing. Other channel spacings are possible by providing proper programming.

The "A" and "N" dividers process the loop feedback signal provided by the VCO (by way of the dual modulus prescaler U401). The output of the "N" divider is a divided version of the VCO output frequency ( $F_v$ ).

Synthesizer U402 also contains logic circuitry to control the dual modulus prescaler U401. If the locked synthesizer output frequency is 450 MHz. The prescaler output nominally will be equal to 3.515625 MHz (450 MHz/128). This frequency is further divided down to  $F_v$  by the "N" divider in U402.  $F_v$  is then compared with  $F_r$  in the phase detector section.

The phase detector output voltage is proportional to the phase difference between  $F_v$  and  $F_r$ . This phase detector output serves as the loop error signal. This error signal voltage tunes the VCO to whatever frequency is required to keep  $F_v$  and  $F_r$  locked (in phase).

## LOOP BUFFER AMPLIFIERS AND LOOP FILTER

The error signal provided by the phase detector output is buffered by operational amplifiers (op-amp) U501A and U501B. The audio modulation signal from U601B is also applied to the input of U501B. The output of U501B is the sum of the audio modulation and the buffered error signal.

The output of the second buffer (U501B) is applied to a loop filter consisting of R506, R507, R508, C505 and C506. This filter controls the bandwidth and stability of the synthesizer loop. The UHF transmitter synthesizer has a loop bandwidth of only several Hertz. This is very narrow, resulting in an excessively long loop acquisition time. To speed acquisition, switches U502A and U502C bypass the filter circuit whenever an ENABLE pulse is received by the Input Gates.

## AUDIO FREQUENCY AMPLIFIER

The transmitter synthesizer audio input line is fed to U601A. U601A is configured as a unity gain op-amp. Resistor R601 sets the 600 ohm input impedance of this amplifier. (NOTE: Data for digital modulation is fed to the synthesizer through the audio input line).

The amplifier output is split into two components and fed to two variable resistors VR601 and VR602. VR601 sets the level in the low frequency audio path and VR602 sets the level in the high frequency audio path. (There is no clear break between the low and high frequency ranges. All voice frequencies are within the high frequency range. The low frequency range contains low frequency data components).

The wiper of VR601 (low frequency path) connects to the input of U601B, the pre-modulation integrator. U601B performs the function of a low-pass filter and integrator. The integrator output is summed with the PLL control voltage at the input of loop buffer amplifier U501B. This integrated audio signal phase modulates the VCO. The combination of pre-integration and phase modulation is equivalent to frequency modulation.

The wiper of VR602 (high frequency path) is connected to the modulation input of the VCO through C16.

## VOLTAGE REGULATORS

U301 and U303 are monolithic voltage regulators (+5 Vdc and -5 Vdc respectively). These two voltages are used by synthesizer circuitry. The +5 V regulator output is also used as a voltage reference for the +8 Vdc discrete regulator circuit.

U302A, Q302 and associated circuitry comprise the +8 volt regulator. Most module circuitry is powered from the +8 volt line. The regulator is optimized for especially low noise performance. This is critical because the low noise VCO is powered by the +8 volt line.

The +8 Vdc line also feeds the +4 Vdc regulator, U302B and associated resistors. The +4 Vdc regulator provides a bias voltage for several op-amps in the module.

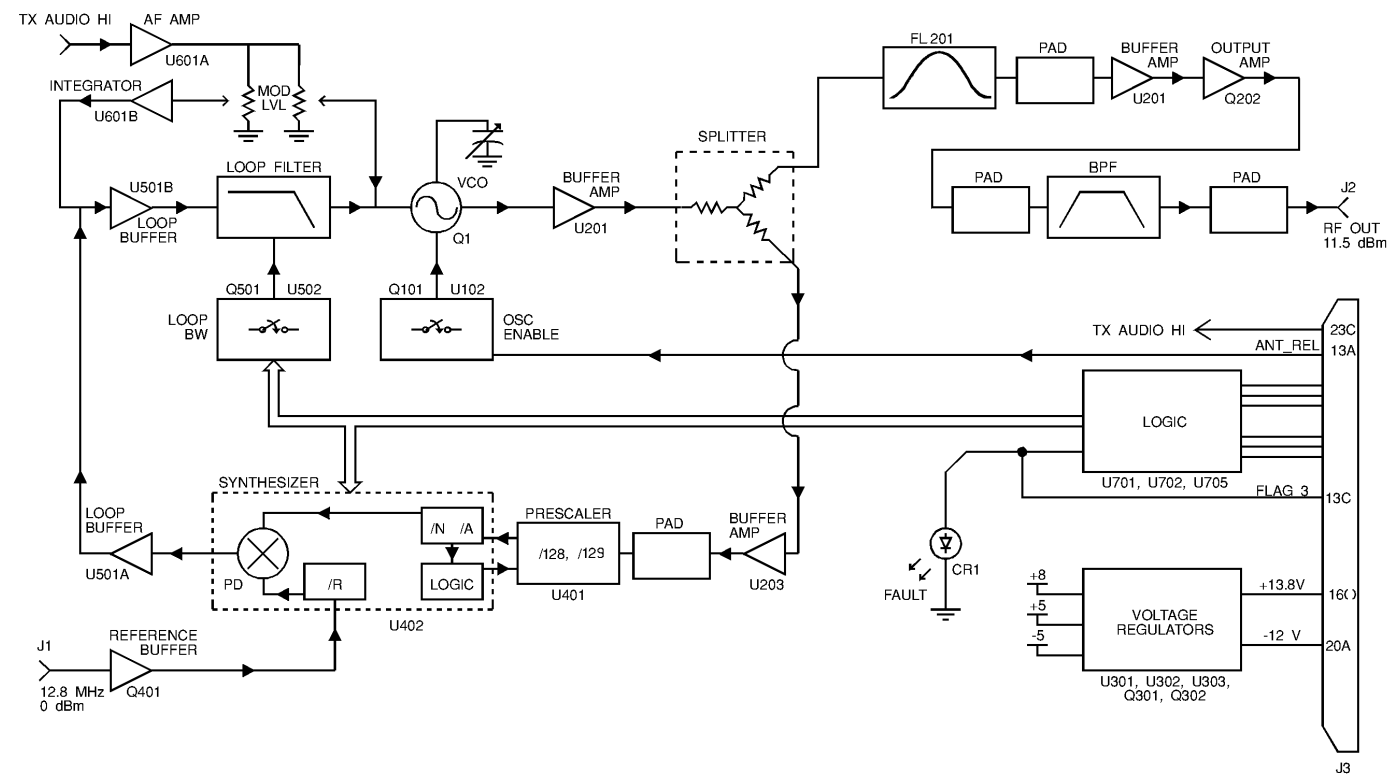


Figure 1 - Block Diagram

## LOGIC CIRCUITS

Logic circuitry (other than that inside the synthesizer IC - U402) consists of the following:

- An address decoder
- Input gates and level shifters
- Lock Indicator circuitry

The address decoder, U702, enables the Input Gates when the A0, A1, and A2 input lines receive the proper logic code (110 for the transmitter synthesizer). After receiving the proper code, Y3 (U702-12) sends a logic low signal to U701C. U701C acts as an inverter and uses the logic high output to turn on Input Gates U701A, U701B, and U701D. The Input Gates allow the clock, data and enable information to pass on to the synthesizer via the level shifters. The Level Shifter Transistors Q701, Q702 and Q703 convert the 5 volt gate logic level to the 8 volt logic level required by the synthesizer U402.

The Fault Indicator circuitry indicates when the synthesizer is in an out-of-lock condition. The fault detector latches, U705A and U705B are reset by the enable pulse during initial loading of data into the synthesizer. If at any time afterwards the lock detector signal (LD) goes low, the high output of U705B will cause the output of gates U705C and U705D to go low. The low output from U705C causes Q704 to conduct turning on the front panel LED (CR701). The output of U705D (FLAG) is connected to J3-13C for external monitoring of the Synthesizer Module. A logic low on the FLAG line indicates an out-of-lock condition.

## MAINTENANCE

### RECOMMENDED TEST EQUIPMENT

The following test equipment is required to test the synthesizer Module:

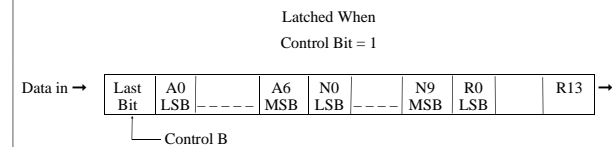
1. RF signal source for 12.8 MHz, 0 dBm reference (included with item 10)
2. AF Generator or Function Generator
3. Modulation Analyzer; HP 8901A, or equivalent, or a UHF receiver
4. Oscilloscope; 20 MHz
5. DC Meter; 10 meg ohm (for troubleshooting)
6. Power Supply; 13.8 Vdc @ 350 mA  
12.0 Vdc @ 25 mA
7. Spectrum Analyzer; 0-1 GHz
8. Frequency Counter; 10 MHz - 500 MHz
9. Personal Computer (IBM PC compatible) to load frequency data
10. Service Parts Kit, (TQ-0650), (includes software for loading frequency data)

## SERVICE NOTES

The following service information applies when aligning, testing, or troubleshooting the TX Synthesizer:

- Standard Modulating Signal = 1 kHz sinusoidal voltage, 0.6 Vrms at the module input terminals (600 ohm R<sub>in</sub>).
- Logic Levels:  
Logic 1 = high = 4.5 to 5.5 Vdc  
Logic 0 = Low = 0 to 0.5 Vdc
- Transmitter Synthesizer Address = A0 A1 A2 = 110
- Synthesizer data input stream is as follows:  
14-bit "R" divider most significant bit (MSB) = R13 through "R" divider least significant bit (LSB) = R0  
10-bit "N" divider MSB = N9 through "N" divider LSB = N0  
7-bit "A" divider MSB = A6 through "A" divider LSB = A0  
Single high Control bit (last bit)  
Latched When Control Bit = 1

### DATA ENTRY FORMAT



For the transmitter synthesizer, 5 kHz channel spacing  
R = 2560  
N = integer part of (frequency in kHz)/(320)  
A = (frequency in kHz)/(5) - 64\*N  
All numbers must be converted to binary.

- ANT\_REL line must be logic low (0V) in order to lock synthesizer.
- Synthesizer lock is indicated by the extinguishing of the front panel LED indicator and a logic high on the fault flag line (J3 pin 13C).
- Always verify synthesizer lock after each new data loading.

## TEST PROCEDURE

(Steps 5, 6, and 7 can be done using a modulation analyzer or UHF receiver with 750 μs de-emphasis switchable in or out.

1. Lock synthesizer at 470.0 (G3), 430 (G6), 450 (G7), 400 (G8), 494 (G9) or 512 (G10) MHz using software provided in the service parts kit.  
Verify lock (flag = high).  
Verify front panel LED is off.
2. Measure output frequency.  
Verify frequency = 470.0000 (G3), 425.000 (G6) or 450.000 (G7) MHz, 400.000 (G8), 494.000 (G9) or 512.000 (G10) ±200 Hz.
3. Measure harmonic content.  
Verify 2nd harmonic is < -30 dBc.
4. Measure RF power output into 50 ohm load.  
Verify 10 to 13 dBm (10 to 20 mW).
5. Measure AF distortion with standard modulating signal input.  
Verify <2.5%.
6. Measure Hum and Noise relative to 0.44 kHz average deviation, (de-emphasis on).  
Verify < -55dB
7. Measure AF response at 300 Hz, 1 kHz (ref) and 3 kHz, (de-emphasis off).  
Verify within ±1.5 dB with respect to 1 kHz reference.
8. Verify lock at different frequencies.
  - a. Lock synthesizer at 380 (G8), 450 (G3), 403 (G6), 425 (G7), 470 (G9) or 492 (G10) MHz. Verify LED is off.
  - b. Lock synthesizer at 385 (G8), 455 (G3), 408.5 (G6), 430 (G7), 476 (G9) or 497 (G10) MHz. Verify LED is off.
  - c. Lock synthesizer at 395 (G8), 465 (G3), 419.5 (G6), 445 (G7), 488 (G9) or 507 (G10) MHz. Verify LED is off.
  - d. Lock synthesizer at 400 (G8), 470 (G3), 425 (G6), 450 (G7), 494 (G9) or 512 (G10) MHz. Verify LED is off.

## ALIGNMENT PROCEDURE

1. Apply +13.8 Vdc and -12 Vdc. Verify the current drain on the 13.8 volt supply is, <300mA and the current drain on the -12 volt supply is <20 mA.
2. Lock the synthesizer at 380 (G8), 450 (G3), 403 (G6), 425 (G7), 470 (G9) or 492 (G10) MHz. Adjust trimmer C10 until Vtest (23A) reads 2.5 (G3, G8), 2.0 (G6, G7, G9) or 3.0 (G10) V ±0.05V.
3. Lock synthesizer at 460.0 (G3), 390.0 (G8), 414 (G6) or 437.5 (G7), 482 (G9) or 502 (G10) MHz for the following three adjustments.
  - Set VR602 for 4.5 kHz peak deviation with a standard modulating signal applied to the audio input.
  - Set VR601 for 4.5 kHz peak deviation with 1.0 Vrms, 10 Hz sine wave audio applied to module AF input.
  - Apply a 10 Hz 1.4 Vpk square wave to module AF input. Adjust VR601 slightly for the flattest demodulated square wave using a modulation analyzer or receiver (no de-emphasis) and an oscilloscope. The maximum net variation in voltage over 1/2 cycle is 5%.

### NOTE

This adjustment is critical for EDACS application and must be reset at customer frequency.

## TROUBLESHOOTING

A troubleshooting guide is provided showing typical measurements at the various test points.

TROUBLESHOOTING GUIDE

SYMPTOM	CHECK (CORRECT READINGS SHOWN)	INCORRECT READING INDICATES DEFECTIVE COMPONENT
SYNTHESIZER FAILS TO LOCK	Check DC voltages +5 V @ U301 Pin 1 +8 V @ Q301 collector -5 V @ U303 Pin 1	U301 or associated components U302, Q301, Q302 or associated components U303 or associated components
	Check 12.8 MHz reference signal 3V P-P, 12.8 MHz @ U402 Pin 2	No reference signal to front panel BNC or Q401
	Check oscillator signal  11.5 ±1.5 dBm 435 to 485 MHz at front panel BNC	Proceed to "Low/No RF output" below
Low/No RF Output	Check prescaler output  IV P-P, 3.5 MHz @ U401 Pin 4	U202, U401
	Check CLOCK, DATA, ENABLE  While loading frequency data into synthesizer Check 8V logic signals @ Pins 11, 12, 13 of U402	Wrong address or U701, U702, Q701, Q702, Q703
	Check Phase detector output  6.25 kHz random signal @ U501 Pin 7	U402, U501
No Modulation	Check AF amplifier  Apply IV, 1 kHz signal to TX/Audio/Hi  Check IV signal @ U601 Pin 1	U601

UHF TRANSMITTER SYNTHESIZER MODULE  
19D902780G3, G6 - G10  
ISSUE 6

SYMBOL	PART NO.	DESCRIPTION
TRANSMITTER SYNTHESIZER BOARD 19D902779G3, G6 - G10		
----- MISCELLANEOUS -----		
2	19D902508P4	Chassis.
3	19D902509P2	Cover.
4	19D902555P1	Handle.
6	19A702381P506	Screw, thread forming: TORX, No. M3.5-.6 x 6.
7	19A702381P513	Screw, thread forming: TORX, No. M3.5 - 0.6 X 13
11	19A702381P508	Screw, thd. form: No. 3.5-0.6 x 8.
12	19D902824P1	Casting.
----- CAPACITORS -----		
C1	19A702236P25	Ceramic: 10 pF + or -.5 pF, 50 VDCW, temp coef + or -30 PPM/C.
C2	19A702236P32	Ceramic: 18 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM
C3	19A702236P28	Ceramic: 12 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM.
C4	19A702236P1	Ceramic: 0.5 pF + or - pF, temp coef 0 + or - PPM/C. (Used in G8).
C4	19A702236P8	Ceramic: 1.5 pF + or -.25 pF, 50 VDCW. (Used in G3, G6, G7)
*C4 and *C5	19A702236P17	Ceramic: 4.7 pF + or -.05%, 50 VDCW, temp coef 0 + or -60 PPM. (Used in G9 & G10).
C5	19A702236P13	Ceramic: 3.3 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM. (Used in G3).
C5	19A702236P17	Ceramic: 4.7 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM. (Used in G6 & G8).
C5	19A702236P15	Ceramic: 3.9 pF + or -.25 pF, 50 VDCW, temp + or -30 PPM/C. (Used in G7).
C6	19A702236P28	Ceramic: 12 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM. (Used in G8 & G3).
C6	19A702236P30	Ceramic: 15 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C. (Used in G6 & G7).
*C6	19A702236P28	Ceramic: 12 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C. (Used in G9 & G10).
C7	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
C8	19A702052P14	Ceramic: 0.01 uF + or -.10%, 50 VDCW.
C9	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C10	19A134227P5	Variable: 1.5 to 14 pF, 100 VDCW.
C11	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C12	19A702052P14	Ceramic: 0.01 uF + or -.10%, 50 VDCW.
C13 and C14	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
*C15	19A700004P6	Metallized polyester: 4.7 uF + or -.10%, 63 VDCW.
*C16	19A702052P106	Ceramic: 1500 pF + or -.5%, 50 VDCW.
C17	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
C18 and C19	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C101	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
C102	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C103	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
C201	19A702061P61	Ceramic: 100 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM.

\*COMPONENTS, ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

SYMBOL	PART NO.	DESCRIPTION
C202	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
C203	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C204 and C205	19A702061P61	Ceramic: 100 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM.
C206	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
C207	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C208	19A702236P28	Ceramic: 12 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM.
C209	19A702236P10	Ceramic: 2.2 pF + or -.25 pF, 50 VDCW, temp + or -30 PPM/C. (Used in G3, G6, G7, G8).
C209	19A702236P8	Ceramic: 1.5 pF + or -.025 pF, 50 VDCW, temp + or -30 PPM/C. (Used in G9 & G10).
C210	19A702236P28	Ceramic: 12 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM.
C211 and C212	19A702061P61	Ceramic: 100 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM.
C213	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C214	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
C215	19A702061P61	Ceramic: 100 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM.
C301	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
C302	19A702052P14	Ceramic: 0.01 uF + or -.10%, 50 VDCW.
C303 and C304	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C305	19A705205P7	Tantalum: 10 uF, 25 VDCW; sim to Sprague 293D.
C306	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C307	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C308 and C309	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
C310	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C311	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C312	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
C313	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C401	19A702052P14	Ceramic: 0.01 uF + or -.10%, 50 VDCW.
C402	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
C403 thru C405	19A702052P14	Ceramic: 0.01 uF + or -.10%, 50 VDCW.
C406	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
C407	19A702052P14	Ceramic: 0.01 uF + or -.10%, 50 VDCW.
C408	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
C409	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C410	19A702052P26	Ceramic: 0.1uF + or -.10%, 50 VDCW
C411	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C412	19A702052P14	Ceramic: 0.01 uF + or -.10%, 50 VDCW.
C413	19A702052P108	Ceramic: 0.01 uF + or -.10%, 50 VDCW.
C414	19A702061P69	Ceramic: 220 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.
C501	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C502	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C503	19A702052P33	Ceramic: 0.1 uF + or -.10%, 50 VDCW.
C504	19A702061P99	Ceramic: 1000 pF + or -.5%, 50 VDCW, temp coef 0 + or -30 PPM/C.

PARTS LIST

LBI-38671

Table with columns: SYMBOL, PART NO., DESCRIPTION. Lists various electronic components such as capacitors, inductors, and connectors.

Table with columns: SYMBOL, PART NO., DESCRIPTION. Lists various electronic components including coils, resistors, and transistors.

Table with columns: SYMBOL, PART NO., DESCRIPTION. Lists various electronic components, primarily metal film resistors.

Table with columns: SYMBOL, PART NO., DESCRIPTION. Lists various electronic components including diodes, integrated circuits, and voltage regulators.

**PRODUCTION CHANGES**

Changes in the equipment to improve or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by these revisions.

**REV. A - TRANSMITTER SYNTHESIZER BOARD 19D902779G3.6.7**

To correct loading problem on synth IC which could cause failure to lock on channel.  
R707 was 47k ohms (19B800607P473).

**REV. B - TRANSMITTER SYNTHESIZER BOARD 19D902779G3. G6-G7**

**REV. A - TRANSMITTER SYNTHESIZER BOARD 19D902779G8**

To make new band splits compatible with helical filters. New PWB.  
C15 was 0.1  $\mu$ F (19A700004P2).  
C16 was 330 pF (19A702061P73).

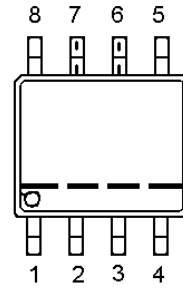
**REV. A - TRANSMITTER SYNTHESIZER BOARD 19D902779G9**

**REV. B - TRANSMITTER SYNTHESIZER BOARD 19D902779G8**

**REV. C - TRANSMITTER SYNTHESIZER BOARD 19D902779G3. G6. G7**

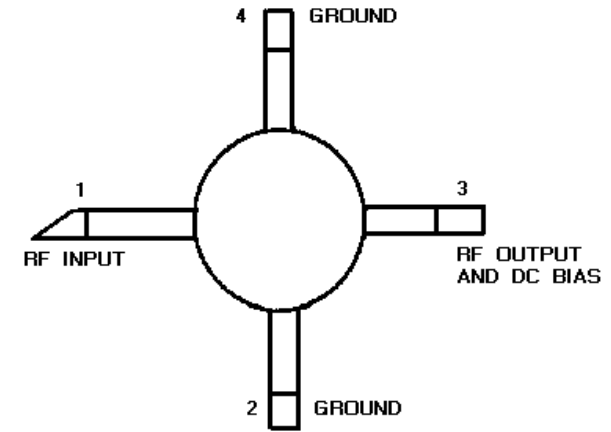
To meet hum & noise performance.  
R101 was 47K ohm (19B800607P473).  
C16 was 1500 pF (19A702061P89).  
R9 was 680 ohm (19B800607P681) for G9.  
R211 was 15 ohm (19B800607P150) for G9.  
R214 was 15 ohm (19B800607P150) for G9.  
R507 was 27K ohm (19B800607P150) for G9.  
C5 was 3.9 pF (19A702236P15) for G9.  
C6 was 18 pF (19A702236P32) for G9.  
PWB was R1 return to R0.

**U201 and U203  
19A705927P11  
Silicon Bipolar MMIC**



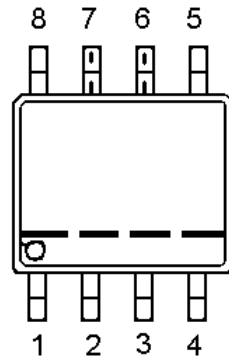
PIN	FUNCTION
1	Vout
2	GROUND
3	GROUND
4	N.C.
5	N.C.
6	GROUND
7	GROUND
8	Vin

**U202  
344A3907P1  
Silicon Bipolar MMIC**

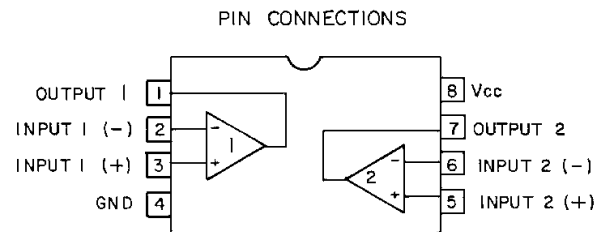


**U302 & U601  
19A116297P7  
Dual Wide Band Op-Amp**

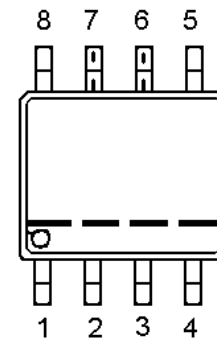
**U301  
19A704971P9  
+5V Regulator**



PIN	FUNCTION
1	Vout
2	GROUND
3	GROUND
4	N.C.
5	N.C.
6	GROUND
7	GROUND
8	Vin

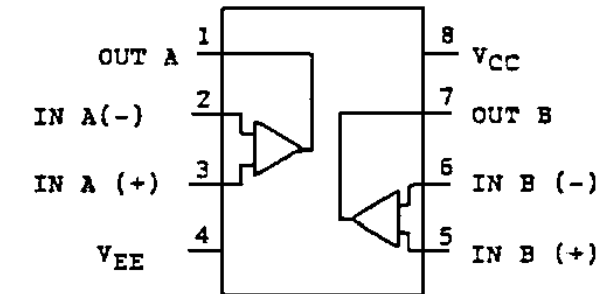


**U303  
19A704971P7  
-5V regulator**



PIN	FUNCTION
1	Vout
2	GROUND
3	GROUND
4	N.C.
5	N.C.
6	GROUND
7	GROUND
8	Vin

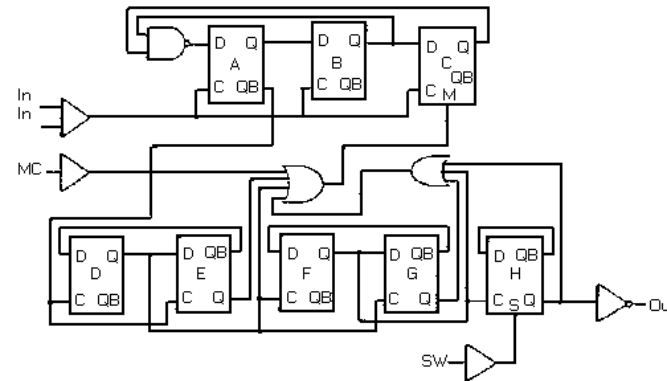
**U501  
344A3070P1  
Operational Amplifier**



**U401**  
**19A149944P201**  
**Dual Modulus Prescaler**

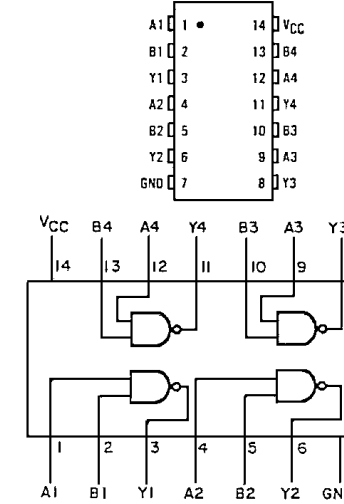
FUNCTION TABLE		
SW	MC	DIVIDE RATIO
H	H	64
H	L	65
L	H	128
L	L	129

SW: H = Vcc L = OPEN  
MC: H = 2.0V TO Vcc  
L = GND TO 0.8V

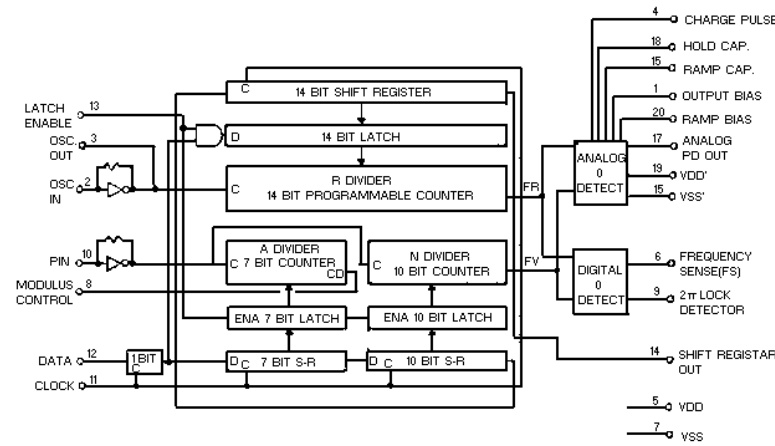
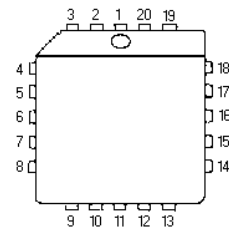


**U701 & U705**  
**19A703483P302**  
**Quad 2-Input NAND Gate**

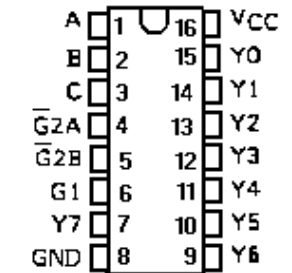
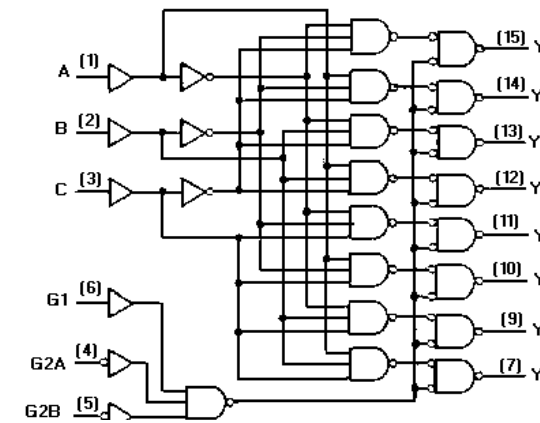
PIN ASSIGNMENT



**U402**  
**19B800902P5**  
**Synthesizer**

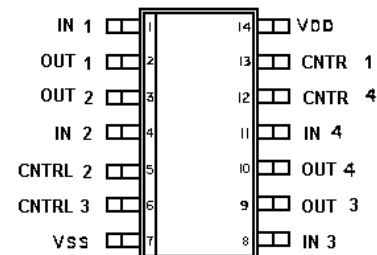


**U702**  
**19A703471P120**  
**Address Decoder**

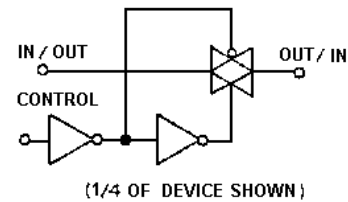


**U502**  
**19A702705P4**  
**Quad Analog Switch**

PIN CONFIGURATION



LOGIC DIAGRAM



CONTROL	SWITCH
0	OFF
1	ON

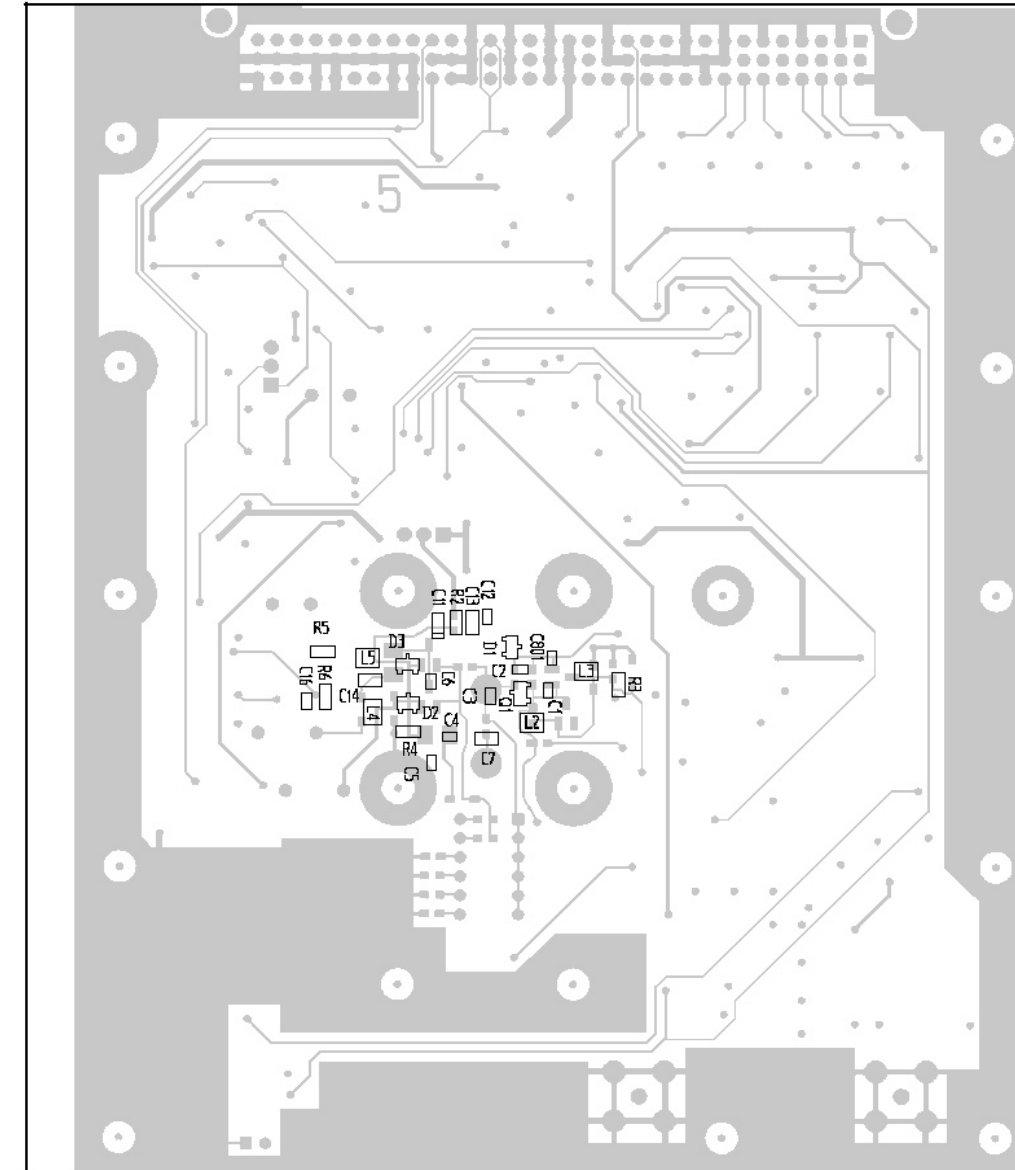
FUNCTION TABLE

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
x	H	x	x	x	x	H	H	H	H	H	H	H	H
x	x	l	x	x	x	H	H	H	H	H	H	H	H
L	x	x	x	x	x	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	L	H	H	H
H	L	L	L	H	L	H	H	H	H	H	L	H	H
H	L	L	L	H	H	L	H	H	H	H	H	L	H
H	L	L	L	H	H	H	H	H	H	H	H	H	L



COMPONENT SIDE

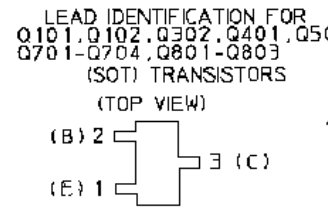
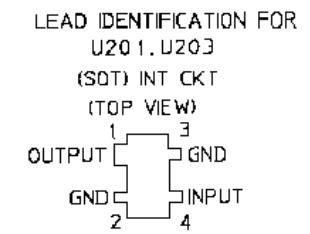
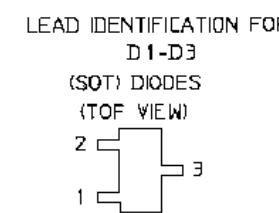
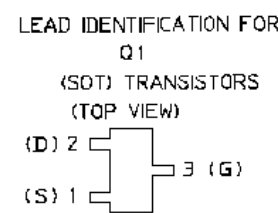
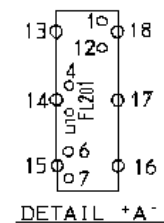
SOLDER SIDE



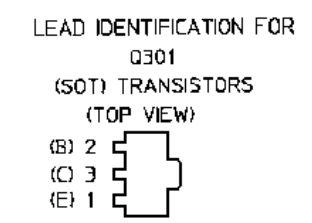
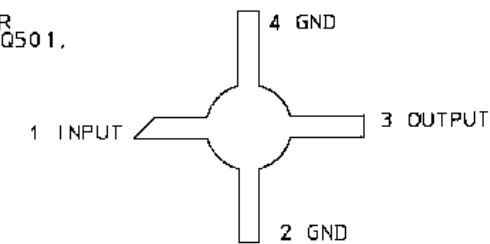
(19D902779, Sh. 2, Rev. 2)  
(19D903361, Layer 1 & 4, Rev. 0)



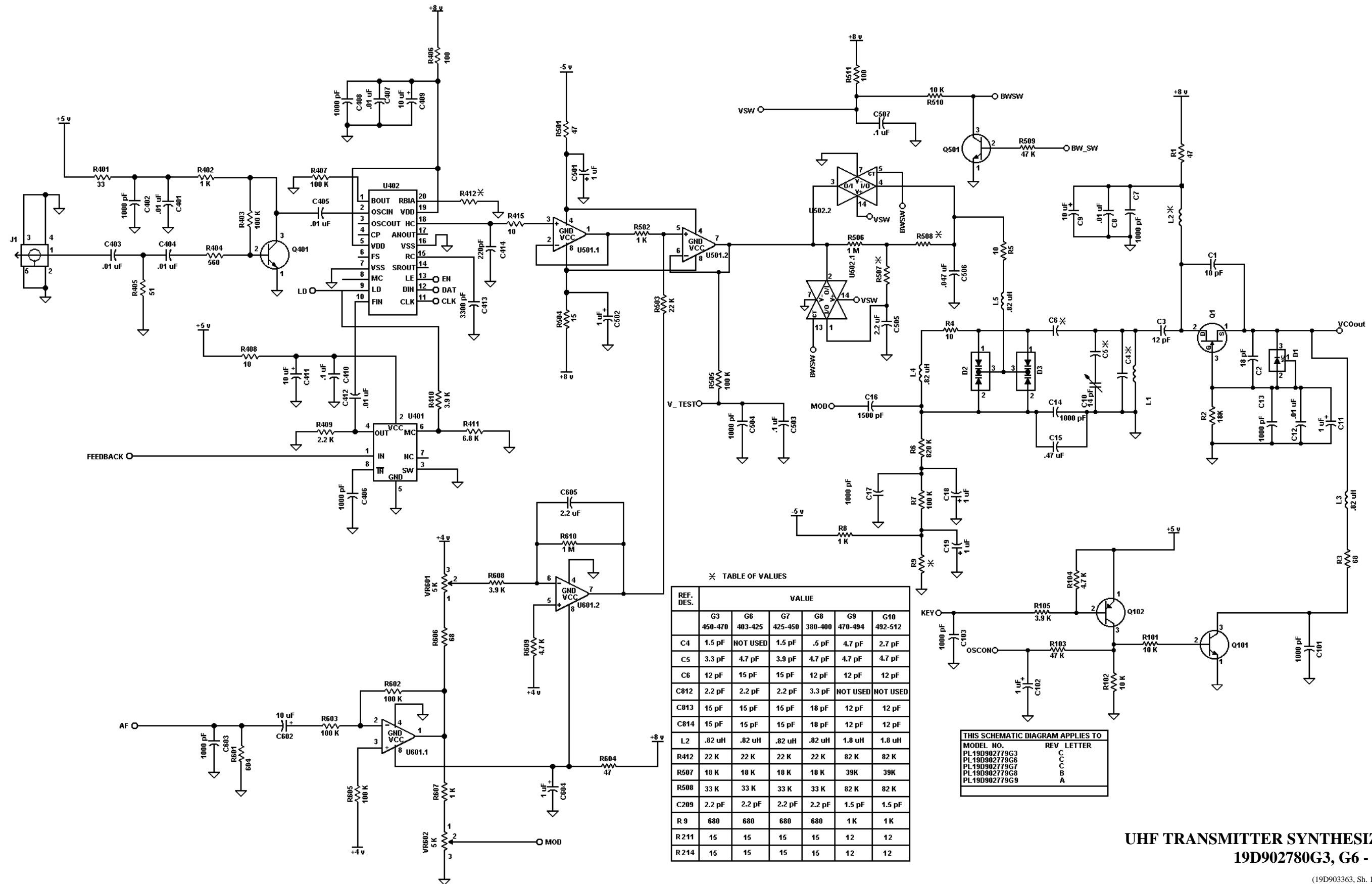
**CAUTION**  
OBSERVE PRECAUTIONS  
FOR HANDLING  
ELECTROSTATIC  
SENSITIVE  
DEVICES



LEAD IDENTIFICATION FOR U202 (SOT) INT CKT (TOP VIEW)

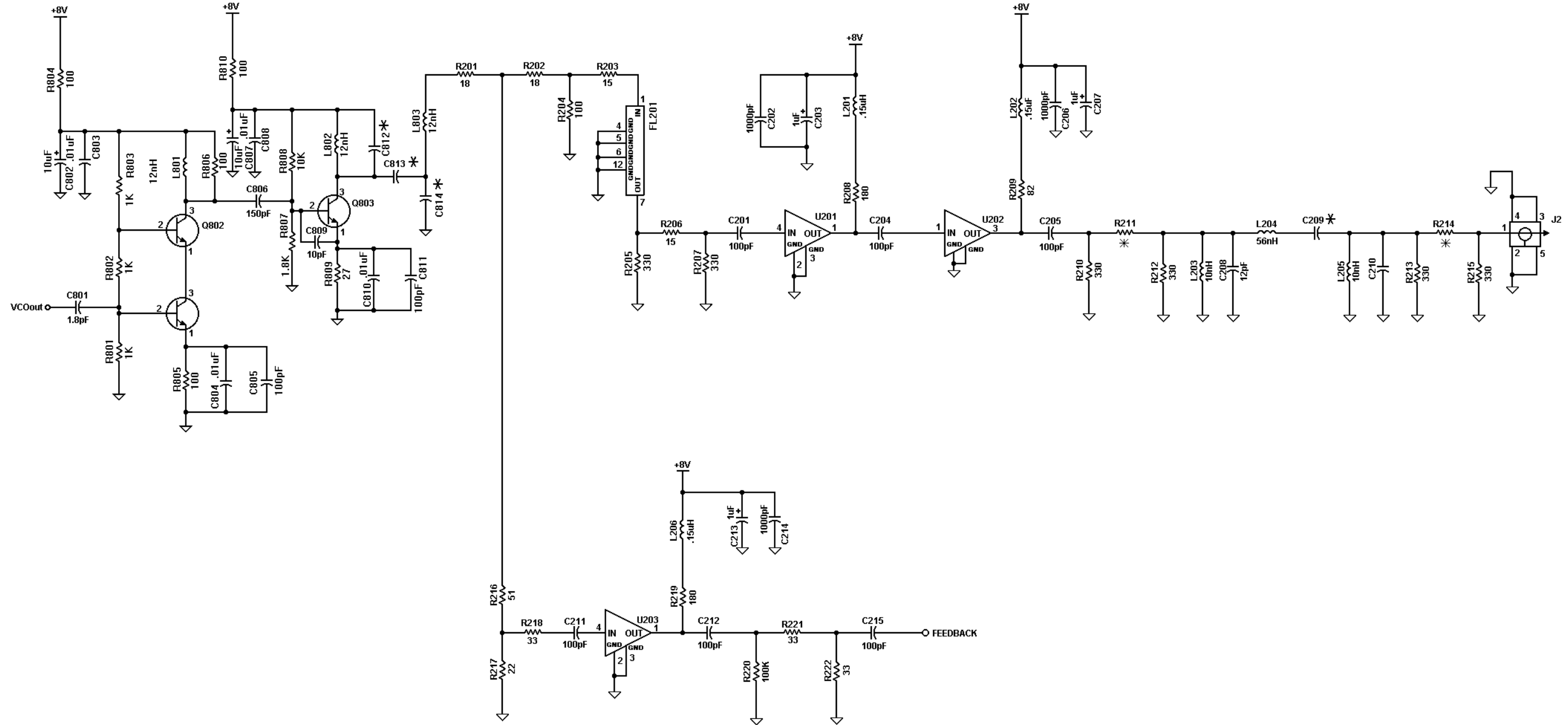


**UHF TRANSMITTER  
SYNTHESIZER BOARD  
19D902779G3, G6 - G10**



**UHF TRANSMITTER SYNTHESIZER  
19D902780G3, G6 - G10**

(19D903363, Sh. 1, Rev. 6)

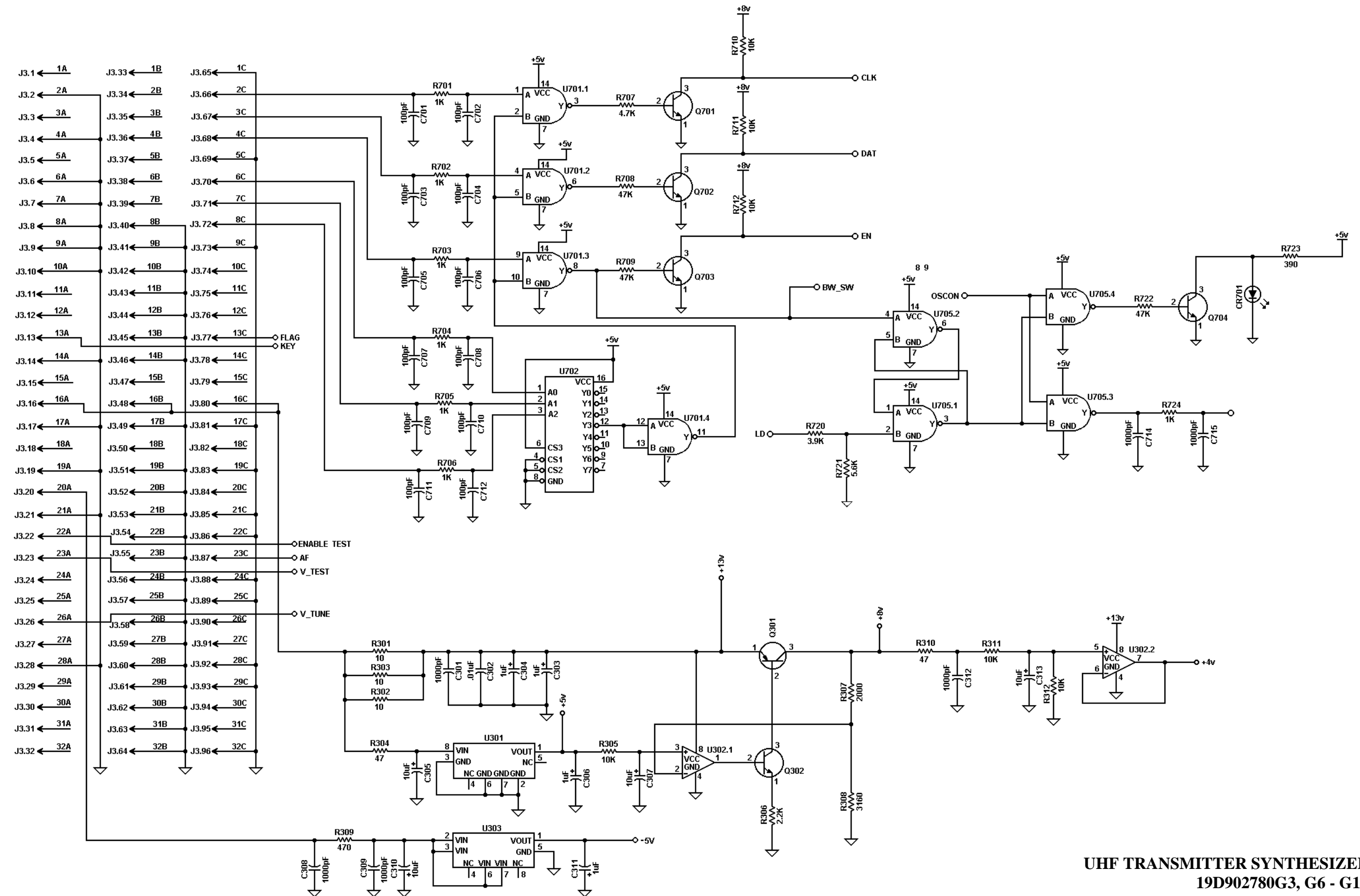


**UHF TRANSMITTER SYNTHESIZER  
19D902780G3, G6 - G10**

(19D903363, Sh. 2, Rev. 4)

SCHMATIC DIAGRAM

LBI-38671



UHF TRANSMITTER SYNTHESIZER  
19D902780G3, G6 - G10

(19D903363, Sh. 3, Rev. 2)