MAINTENANCE MANUAL
INTEGRATED MULTISITE & CONSOLE CONTROLLER
CONVENTIONAL BASE STATION INTERFACE
(Conventional Interface Board 19D903324P1)

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Continued

ERICSSON

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SPECIFICATIONS*

Temperature	-30°C to + 60°C
Height	200 mm typical
Width	330 mm typical
Weight	1.0 kg typical
Power	+5 Volts dc @ 1.75 Amps maximum +15 Volts dc @ 0.3 Amps maximum -15 Volts dc @ 0.3 Amps maximum
Relay Output Contacts	2 Amps maximum @ 120 Volts 30 VA maximum switching power
Optioisolator Inputs	5.0 mA nominal current 1.6 mA minimum, 10 mA maximum
Serial Port Baud Rate	9600 Baud (RTS and CTS required) RS232C, 8 Data, No Parity, 1 Stop
Audio Levels (Input and Output)	+11 to -19 dBm
Audio Distortion	Less than 3%
Audio Hum And Noise	Less than 50 dB
Audio Gain	0 dB
Audio Response	±2 dB 300-3kHz referenced to 1kHz
Line Termination Impedance (conventional)	600 Ohm (or bridged if 4-wire)
VOX Trip Adjust Range	-3.5 to -35 dBm
2175 Hz Hold Tone Levels Output	-20 to -45 dBm
DC Control Currents	0, -2.5, ±6, ±11 mA into 11k Ohm Load Maximum (3k Ohm Matching And 8k Ohm line Z)

*These specifications are intended primarily for the use of the service technician. Refer to the appropriate Specification Sheet for the complete specifications.

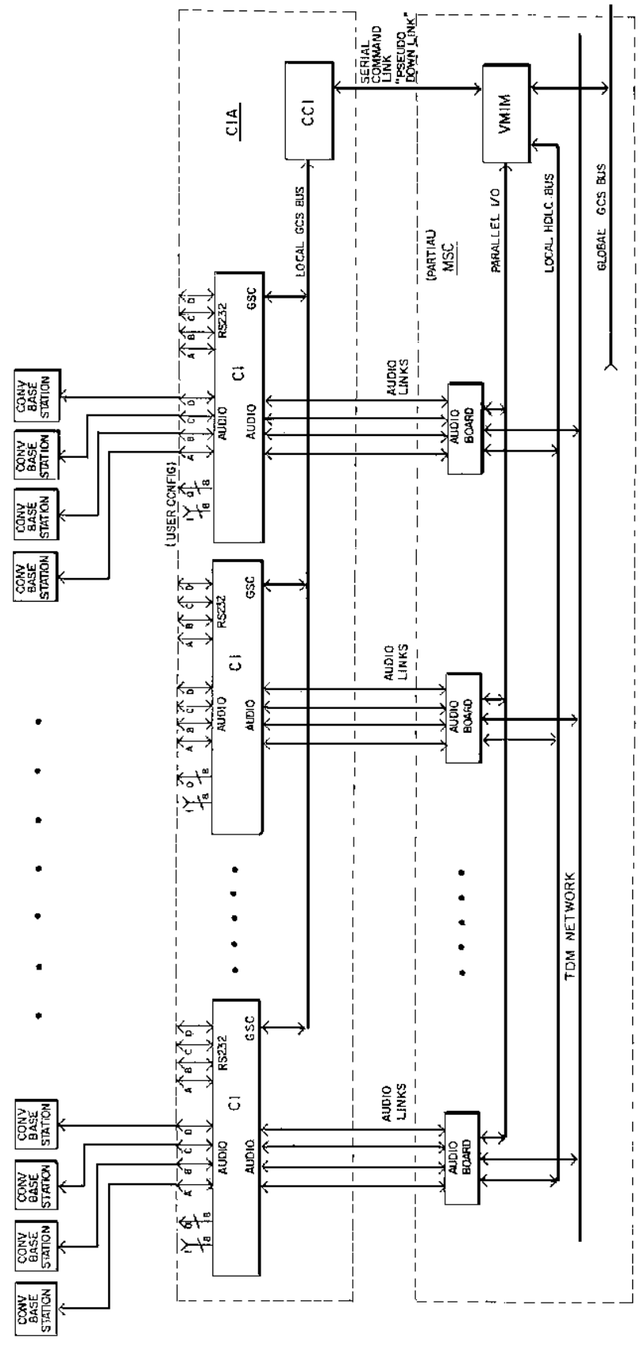


Figure 1 - Conventional Base Station Interface Block Diagram

DESCRIPTION

GENERAL

The Conventional Base Station Interface is part of **Integrated Multiside & Console Controller** digital audio switch. The Conventional Base Station Interface is designed to interface conventional systems controlled by standard tone, DC or E&M signaling to the core **IMC** audio switch. The conventional interface is supported on both the CEC and IMC versions of the IMC.

The Conventional Base Station Interface consists of a **C**onventional **I**nterface **A**daptor **(CIA)** rack, as many as eight (8) **C**onventional **I**nterface **(CI)** circuit boards and a single **C**onventional **C**ontroller **I**nterface board **(CCI)**. The number of CI boards present in the CIA is determined by the number of conventional stations to be interfaced. Each CI card is capable of interfacing to four (4) conventional stations.

The CIA consists of the standard IMC card cage and backplane assembly (refer to Maintenance Manual LBI-38663) and accommodates the CI boards and the CCI module. The CCI module is a standard IMC Controller module (refer to Maintenance Manual LBI- 38667).

When the Conventional Base Station Interface is used, the IMC is equipped with a con**V**entional **M**ultisite **I**nterface **M**odule **(VMIM)** (refer to Figure 1). Figure 1 is a detailed Block Diagram showing a single node of a Conventional Interface Adaptor (CIA) and a Con**V**entional **M**ultiSite **I**nterface **M**odule **(VMIM)**. The VMIM module is a standard IMC controller module. Each VMIM can couple thirty two (32) conventional stations to the trunked system using up to eight (8) audio boards.

SYSTEM

The IMC and the Conventional Base Station Interface (CIA) in conjunction with each other, are capable of establishing audio pathways between conventional base stations, dispatch consoles and between conventional stations and digitally trunked radio sites if calls are patched/simulselected at the console. The VMIM of the IMC is indirectly coupled, through the CIA, to several audio lines carrying non-trunked conventional audio between the base station and the IMC. The VMIM is capable of receiving and sending conventional calls to and from the base station.

Within the IMC, the VMIM connects to internal **T**ime **D**ivision **M**ultiplexed **(TDM)** audio buses and the control buses. These TDM slotted buses are the digitized audio pathways within the coordinator. The TDM buses connect each of the coordinator nodes and establishes digital audio links between the various sites and dispatcher consoles within the radio network. Also, within the coordinator there are control buses that **c**arry digital control messages between nodes within the coordinator. These messages are used to establish, control and "tear-down" audio pathways and to perform overhead administrative tasks within the coordinator. The VMIM coordinator node interacts with all of the other nodes within the coordinator.

The CIA interfaces directly to the conventional channel lines and the VMIM. The CIA does not directly connect to the TDM or command buses within the coordinator. The CIA has a serial command link and audio lines connecting it to the VMIM. The CIA acts on, or translates the digital control messages from the VMIM into control tones or DC currents for the base station. The CIA also detects voice signals on conventional channels from the base station. The CIA makes the conventional base station appear to be a relatively standard trunked site to the VMIM. The CIA forms a serial command link between the VMIM and a pseudo-downlink to the VMIM.

CONVENTIONAL CONTROLLER INTERFACE BOARD

The CCI Board is programmed to mimic the downlink trunking card of a trunked site controller. The CCI generates many of the same digital messages that are generated by a trunked downlink trunking card and sends these messages through a serial link to the controller card of the VMIM. The CCI also communicates with the CI boards in the CIA through a **G**lobal **S**erial **C**hannel **(GSC)** message bus. The CI boards, for example, send messages to the CCI when an audio signal is detected on a conventional channel. The CCI generates an appropriate digital channel request that is sent to the VMIM. Similarly, upon receiving a digital message from the VMIM, the CCI sends a message on the CIA message bus, instructing one of the CI boards to generate a tone or a DC current level for a particular channel. In this way, the CCI is able to translate control information between a digital multisite switch and a conventional base station.

CONVENTIONAL INTERFACE BOARD

The **C**onventional **I**nterface **(CI)** boards are located in the Conventional Interface Adaptor **(CIA)**. These boards connect through land lines, or other linkage, to the channels of a conventional base station. Each CI board provides four distinct audio source/destination pairs. In the IMC, a VMIM audio module includes four audio links serving one to four conventional channels through the CI board in the CIA. The IMC audio modules act as source gateways **("entrance/exit ramps")** which convert audio signals incoming from the base station into digitized audio signals (PCM) and places the digitized audio signals onto the audio TDM network. These same audio modules act as audio destinations by taking selected signals from the TDM network, converting them from digital into analog form and providing the resulting analog signals to the appropriate CIA CI board. The CI board, in turn, provides the audio signals along with control information to the conventional channel for transmission by the base station.

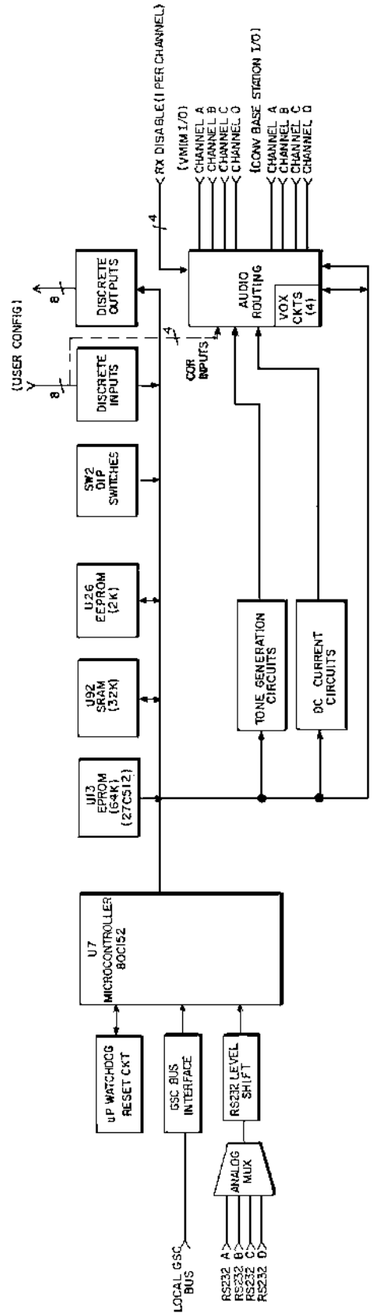


Figure 2 - Conventional Interface Board Block Diagram

Figure 2 is a detailed block diagram of the Conventional Interface (CI) board. Each CI board has a microcontroller to support the audio processing and routing circuitry. The microcontroller is supported by several external memories, including an EPROM, a Static RAM (SRAM) and an EEPROM. These memories hold the operating programs for the microcontroller, provide scratch pad memory and hold other data used by the microcontroller. An internal address and message bus connects the microcontroller to the external memories. This bus also connects the microcontroller to DIP switches that are used to set the personality of the CI board and to discrete inputs and outputs for an I/O user configuration interface to the base station. The I/O port may be used to support E&M signaling.

The CI microcontroller communicates with the CCI over the CIA local GSC bus. Similarly, the CI microcontroller can communicate with the optional peripheral equipment over a series of serial links that are multiplexed into the microcontroller.

The microcontroller operates the tone generation circuits and DC current circuits that provide control commands for the conventional base station. As previously stated, the conventional base station is generally controlled by tones added to the audio signal, or by DC currents applied through the channel lines to the base station. At start-up, the microcontroller receives information identifying whether the base station is controlled by tones or DC currents, has 2/4-wire channel links and has E&M signaling. The tone or DC current controls are combined with the audio signals to conventional base stations. The **V**oice **O**perated **(VOX)** circuit detects audio on a conventional channel causing the CI to send a message to the CCI through the GSC bus which sends a signal (equivalent to the signal in trunked systems) to the VMIM, by way of the pseudo-downlink, indicating that the channel has been keyed or unkeyed.

CIRCUIT ANALYSIS (Conventional Interface Board)

Conventional Interface Board 19D903324G1 consists of four (4) identical audio processing circuits and a control circuit. For the sake of simplicity, only one audio processing circuit will be analyzed. Each audio processing circuit consists of a programmable DC current source, a tone generation circuit, audio interface and voice operated circuits (VOX). The audio interface circuits consists of amplifiers for audio inputs and audio outputs. Figure 3 is a detailed diagram of a single circuit for processing a single channel through the CI board of the CIA.

VOLTAGE REGULATION

External voltage input levels to the Conventional Interface Board are +5 Vdc, +15 Vdc and -15 Vdc. These levels are filtered and regulated to produce +5 Vdc (Vcc), +12 Vdc, -12 Vdc and -5 Vdc respectively (Refer to the Schematic Diagram, Sheet 5).

+5 Vdc (Vcc) Filtering

The external +5 Vdc connects to the Vcc filter circuit through 2 amp fuse F17 connected between fuse connectors XF1 and XF2. The external +5 Vdc can be metered at TP31. Filtering is provided by 100 H inductor L3, 220 F capacitor C23 and 0.1 F capacitor C25.Leaded diode D35 removes any negative transients. LED CR1 illuminates when Vcc is present.

The filtered Vcc output is taken from the point labeled **Vcc** on the Schematic Diagram. The Vcc can be read, using a voltmeter, between **TP26** (Vcc) and **TP30** (GND).

+12 Vdc Regulation

The external +15 Vdc connects to the +12 Vdc regulation circuits through 0.5 amp fuse F18 connected between fuse holders XF3 and XF4. The external +15 Vdc can be metered at TP33. Filtering, ahead of voltage regulator U64, is provided by 0.1 F capacitor C28 and 100 F capacitor C33. Additional filtering, after U64, is provided by 100 F capacitor C24 and 0.1 F capacitor C26. Leaded diode D5 removes any negative transients. LED CR2 illuminates when +12 Vdc is present.

The regulated +12 Vdc is taken at the point labeled **+12V** on the Schematic Diagram. The +12 Vdc can be read, using a voltmeter between **TP27** (+12 Vdc) and **TP30** (GND).

-12 Vdc Regulation

The external -15 Vdc connects to the -12 Vdc regulation circuits through 0.5 amp fuse F19 connected between fuse connectors XF5 and XF6. The external -15 Vdc can be metered at TP32. Filtering, ahead of voltage regulator U62, is provided by 100 F capacitor C32. Additional filtering, after U62, is provided by 0.1 F capacitor C27 and 100 F capacitor C31. Leaded Diode D48 provides protection from positive transients. LED CR3 illuminates when -12 Vdc is present.

The regulated -12 Vdc is taken at the point labeled **-12V** on the Schematic Diagram. The -12 Vdc can be read, using a voltmeter between **TP28** (-12 Vdc) and **TP30** (GND).

-5 Vdc Regulation

The regulated -12 Vdc is applied to the input of voltage regulator U63. Input filtering is provided by 0.1 F capacitor C29. Additional output filtering is provided by 0.1 F capacitor C30 and 100 F capacitor C34. Leaded diode D34 provides protection from positive transients. LED CR4 illuminates when -5 Vdc is present.

The regulated -5 Vdc is taken at the point labeled **-5V** on the Schematic Diagram. The -5 Vdc can be read, using a voltmeter between **TP29** (-5 Vdc) and **TP30** (GND).

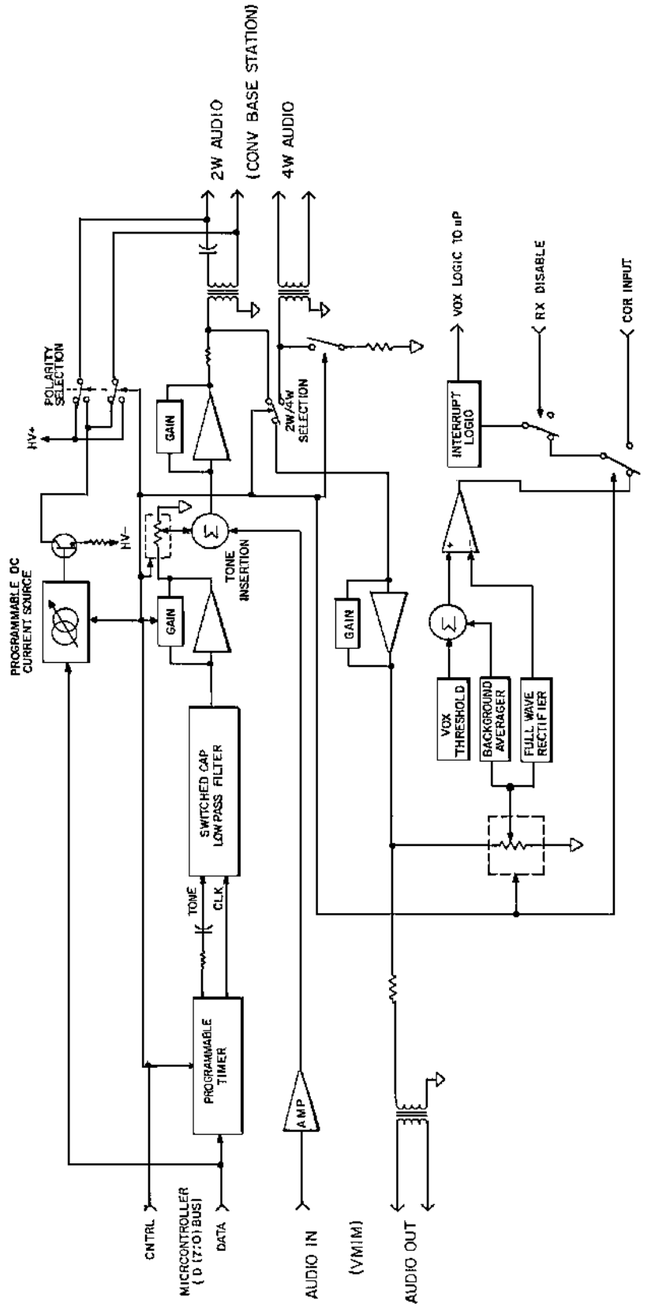


Figure 3 -Single Circuit For Processing A Single Channel Through The CI Board Of The CIA

DECOUPLING

Decoupling on the Conventional Interface Board is provided by 0.01 F capacitors (C35 through C82, C128, C131, C133 and C186 through C202) connected between all voltage inputs of integrated circuits (U1 through U109) and ground (GND). Refer to the Schematic Diagram, Sheet 5.

CONTROL

(Schematic Diagram, Sheet 1)

Microcontroller

Microcontroller U7 is the heart of the CI board. It communicates with the CCI over the CIA GSC bus. It operates tone generation and DC current circuits. At start up, U7 determines if the base station is controlled by tone or DC currents, has 2 or 4-wire channel links and if the station has E&M signaling. It also sets signal levels for tone generation and VOX circuits and controls audio routing circuits.

Clock

Microcontroller U7 provides an internal clock oscillator circuit. Crystal Y1 (14.745 MHz) connects across U7, Pin 31 **(XTAL2)** and Pin 32 **(XTAL1)**. The clock output (14.745 MHz) goes to the input of wave shaping inverter circuit U103B (74HC04D). The output of U103B then goes to the input of another inverter circuit U103D (74HC04D). The output of U103D goes to the CLK input of flip-flop circuit U25A (74HC74) witch divides the clock by two (2). The **CLKOUT** signal **(7.3728 MHz)** goes to tone generation circuits U28, U35 and U36 (refer to **TONE GENERATION**).

Address Latch

The low order memory address byte A(7:0) is latched from the D(7:0) address/data bus by address latch U12 (74HC573). Microcontroller U7 provides a **L**atch **EN (LEN)** signal from U7, Pin 55 **(ALE)** to U12, Pin 11 **(LEN)** which activates the latch. The low order address byte A(7:0) and the high order address byte A(15:8) combine to form a 16 bit address bus A(15:0). Address bus A(15:0) connects to the address inputs of all memory circuits U13, U26 and U92.

Address Decoder/Chip Select Generator

Address decoder U27 (74HC154) and **NAND** gate U11A (74HC00) segment the 64k byte I/O address space of U7 by decoding address lines A11 through A15 and generating chip select signals. These chip select signals are used to select different circuits throughout the CI board. **NAND** gate U11A monitors the **\PSEN** signal from U7, Pin 54 and memory address line **A15** to enable U27. The select signals generated include **/IO_EN**, **/PERSNL**, **/F_CLK**, **/CH_LOAD**, **/EEPOT**, **/DCCH1_2**, **/DCCH3_4**, **/TONE1_3**, **/TONE4_6** and **/EEP_CS**.

NOTE

The "/" indicate the **"barred"** or **"Not"** condition. The barred condition states that the action is true when the circuit condition is low (logical 0).

DIP Switches

The address/data bus (D(7:0)) also connects the microcontroller to configuration DIP switches SW2 through non-inverting bus transceiver U18 (74HC245). Transceiver U18 is enabled by **/RD** and **/PERSNL** signals on inputs to **OR** gate U19C, Pins 10 and 9 respectively. The **/RD** signal is generated by U7 and the **/PERSNL** signal is generated by address decoder/chip select generator U27. When enabled, transceiver U18 places the state of the dip switches **(SW2)** onto the address/data bus D(7:0), allowing the microcontroller to read the state of the switches. DIP Switches SW2 are used to set the personality of the CI board (See the **SET UP** section for the definition of DIP switches).

Memory

External memories are provided to support the operation of the microcontroller. They include 64k UVEPROM (UltraViolet Erasable PROM) U13 (27C512), 32k SRAM (Static RAM) U92 (HM62256P) and 2k EEPROM U26 (28C16). These memories contain the operating program for the microcontroller, provide scratch memory and hold non-volatile data used by the microcontroller respectively. An address bus (A(15:0) and an address/data bus (D(7:0)) connects the microcontroller to the external memories. EEPROM U26 is enabled through **OR** gate U19B (74HC32D). **OR** gate U19B monitors the **/WR** signal from U7, Pin 24 and the **WR_P** signal generated by supervisory circuit U8.

Watchdog Timer

Supervisory circuit U8 (MAX691CWE) provides a watchdog timer that times out and automatically resets the microcontroller when it is not updated by the processor. Under normal operation the microprocessor toggles the **!WD_TRIG** output on U7, Pin 7. It is inverted by inverter U2F (74HC04D) and the **!WD_DIS** signal from DIP switch SW2 is inverted by inverter U2E. Inverters U2E and U2F and **NOR** gate U98D (74HC02D) form an **AND** function. Microcontroller U7 generates a short low going pulse periodically on Pin 7 **(/WD_TRIG)**. If the watchdog is enabled by a high on **\WD_DIS** (generated by dip switch SW2) then the low going pulse causes U98D, Pin 13 to go low turning transistors Q1 and Q22 off. When Q22 is off the **WDI** signal into U8, Pin 11 floats. This disables the watchdog timer temporarily, which resets the timeout timer. When Q1 is off LED CR9 is off. However, the low going pulses at U98D, Pin 13 are so short that CR9 appears to be on all the time.

When the watchdog timer is disabled, by DIP switch SW2, **/WD_DIS** goes low causing U98D, Pin 13 to stay low all the time. This causes Q1 and Q22 to stay off which turns off LED CR9 and disables the watchdog timer permanently by causing the **WDI** input on U8, Pin 11 to stay in a floating state.

When the watchdog is enabled by SW2 and it fails to get reset by Q22, it times out after approximately 1.6 seconds and generates a low going reset pulse on U8, Pin 15. This low reset pulse resets the microcontroller causing it to reinitialize and turn transistor Q27 off. Transistor Q27 turning off causes LED CR10 to turn off indicating it is not in the normal **RUN** mode. The input to transistors Q1 and Q22 can be metered at test point TP24. The collector of Q22 **(WDI)** can be metered at test point TP25.

Manual Reset

The microcontroller can be manually reset by pressing manual reset switch SW1. When SW1 is pressed the **/uPrst** line goes low to discharge capacitor C1 and reset U7. The /uPrst line connects to the base of transistor Q27 through resistor R312. When the /uPrst line goes low, Q27 stops conducting and **RUN/!RESET** LED CR10 turns **OFF** to indicate the RESET condition. Capacitor C1 then recharges through resistor R72. When C1 is recharged, the microcontroller comes out of reset, transistor Q27 conducts and **RUN/!RESET** LED CR10 turns **ON** to indicate the **RUN** condition.

Serial Ports

There are four RS-232 serial ports to the CI board brought in through modular, 6-position jacks J3 - J6. The **C**lear-**T**o-**S**end **(CTS)** inputs from each port (**CTS1**, **CTS2**, **CTS3** and **CTS4**) are monitored by RS-232 DTL line receivers U57A through U57D (MC1489D). Line receiver U57D monitors CTS1, U57C monitors CTS2, etc. The output of these line receivers **(/CTS1**, **/CTS2**, **/CTS3** and **/CTS4)** connect to inputs of 4-input **AND** gate U10B (74HC21D). When any one of the outputs of the four line receivers is low, the **AND** gate provides an interrupt signal **(/INT1)** to U7, Pin 18. This interrupt signal informs the microcontroller that a channel is active. The **/CTS1**, **/CTS2**, **/CTS3** and **/CTS4** signals connect to U7, Pins 67 (6.0), 66 (6.1), 52 (6.2), 57 (6.3) respectively. The microcontroller checks these pins to determine which serial port(s) is active.

All four serial ports are serviced by a single internal **UART** within U7. To achieve this, the RX#, TX# and RTS# signals are switched onto the microcontroller pins so that the microcontroller only communicates on one serial port at a time. The microcontroller monitors the CTS lines to determine which serial port to select.

All transmit channels, TX1 through TX4, from J1 through J4, connect to analog multiplexer U14 (DG509A), Pins 13, 12, 11 and 10 respectively. All **R**equest-**T**o-**S**end **(RTS)** lines, RTS1 through RTS4, from J1 through J4, connect to U14, Pins 4, 5, 6 and 7 respectively. When a **/RTS (/TXD)** signal is generated by U7, Pin 51 (Pin 15) it connects to RS-232 transceiver U73 (MAX232C), Pin 10 (Pin 11). The RS-232 output on U73, Pin 7 (Pin 14) **(RTSSER) (TXDSER)** connects to analog switch U14, Pin 8 (Pin 9). The **SER_SEL0** and the **SER_SEL1** signals from U7 select the active channel on which the transmission will occur:

SER_SEL0	SER_SEL1	CHANNEL
0	0	1
0	1	2
1	0	3
1	1	4

All receive channels RX1 through RX4, from J1 through J4, connect to analog multiplexer U15, Pins 4 through 7 (DG509AO) respectively. RS-232 receive data on the active channel, selected by the **SER_SEL0** and **SER_SEL1** inputs from U7, is routed to the **RXDSER** output. This output connects to the input of RS-232 transceiver U73, Pin 13. Transceiver U73 converts the signal from RS-232 levels to TTL levels. The output of U73 on Pin 12 **(RXD)** connects to U7, Pin 14 which goes to the receive section of the microcontroller internal **UART**.

GSC Bus Interface

The microcontroller communicates with the CCI over a bidirectional CIA local GSC bus. Interfacing to the GSC bus is provided by the **GSC TRANSCEIVER** circuit (see Schematic Diagram, Sheet 1). The CI board supports redundant GSC buses (**GSC_HI_1** and **GSC_HI_2**) for fault tolerance. The **GSC_HI_1** line (J2, Pin 6A) connects to Pin 20 of 4-Channel Transceiver U1 (DS3897M). The GSC_HI_2 (J1, Pin 29A) connects to U1, Pin 18. GSC_HI_1 can be metered at test point TP22. GSC_HI_2 can be metered at test point TP23.

Receive:

Since the microcontroller has only one GSC port, data can only be received from one GSC line at a time. The receive output from U1, Pin 2 (R1) connects to 3-Input **NAND** Gate U3A, Pin 2 (74HC10D). The receive output from U1, Pin 4 (R2) connects to 3-Input **NAND** Gate U3B, Pin 3 (74HC10D). When the **/BUS1 EN** signal from U7, Pin 50 line is high, **BUS1 EN** through Inverter U2B (74HC04D) is low. With this low input on U3A, Pin 1, the output of U3A, Pin 12 remains high. Any received data passes through U3B. When the **/BUS1 EN** is low any received data will pass through U3A. The outputs of U3A and U3B connect to 2-Input NAN Gate U11C, Pins 9 and 10 respectively (74HC00). The output on U11C, Pin 8 connects to Inverter U103E, Pin 11 (74HC04D). The received data output on U103E, Pin 10 connects to U7, Pin 4. This received data can be metered at test point TP21.

Transmit:

The transmit data signal **GTXD** from U7, Pin 5 connects to the input of Inverter U103C, Pin 5 (74HC04D). The output of U103C, Pin 6 connects to U1, Pins 1 (D1) and 3 (D2). When the transmit enable signal **/DEN** is generated by U7, Pin 6 and applied to U1, Pin 10 **(/TE)** then transmit data is transmitted on both GSC lines **(GSC_HI_1 and GSC_HI_2)**.

EEPOT Gain Set

The tone level and VOX threshold level for each audio channel is set by U7 through EEPOT's connected in the audio circuits (refer to Schematic Diagram, Sheets 6-9). These pots are selected by the **EEPOT SELECT** circuit which consists of inverting flip-flop circuit U20 (74HC573) and **NOR** gate U21A (74C02D). The EEPOT selection information provided by U7 is read from the D(7:0) data/message bus by U20 when address decoder U27 generates a **/EEPOT** signal applied to U21A, Pin 2 and a **/WR** signal is applied to U21A, Pin 3 by microcontroller U7. The EEPOT select signal can be **TX1-POT** through **TX4_POT** or **RX1_POT** through **RX4_POT**. The selected pot can then be increased or decreased by **/POT_INC** or **POT_U/D** signals from U7, Pins 19 and 23 respectively.

DC TO DC CONVERSION

The external +5 Vdc input to the Conventional Interface Board also connects through 2 amp fuse F20, connected between fuse holders XF7 and XF8, to the positive input terminals (Pin 1, +Vin) of dc to dc converters U65 through U68 (PS3220P2). Filtering for this line is provided by 100 µH inductor L2 and 220 F capacitor C177. With +5 Vdc on the input of one of these circuits, the output is 150 Vdc. U65 generates the CHN1_HV and CH1_LV. U66 generates the CHN2_HV and CHN2_LV. U67 generates the CHN3_HV and CHN3_LV. U68 generates the CHN4_HV and CHN4_LV. Filtering for these lines is provided by 0.33 F capacitors C173 through C176 respectively. These outputs (150 Vdc) provide a high voltage potential used by the constant dc current generators (Refer to Schematic Diagram, Sheet 3).

CONSTANT DC CURRENT GENERATOR

The DC Current Generator circuit is a programmable DC current source that applies a selected current level through a transistor circuit and polarity selector switch and through a channel line to the conventional base station . These selectable current levels are 2.5 mA, 6 mA, 11 mA or 0 mA. These current levels are commonly used for control and operation of conventional remote repeater stations. Microcontroller U7 in the control circuit provides control commands through the D(7:0) bus to set the amount of current from the DC current source and to set the polarity switching relay so that the current is applied with the appropriate polarity to the channel line.

There are four (4) identical Constant DC Current Generator circuits on each conventional interface board. Each circuit corresponds to a conventional base station. These circuits are controlled by 3-state, inverting, flip-Flops U33 and U44 (74HC564DQ). Flip-flop U33 controls the circuits for conventional base station channels 1 and 2. Flip-Flop U44 controls the circuits for conventional base station channels 3 and 4. The selection of U33 or U44 is accomplished through **NOR** gates U21C and U21D (74HC02D). When the **/WR** and the **/DCCH1-2** inputs to U21C go low, U33 is selected to control the current generator circuit for channels 1 and 2.

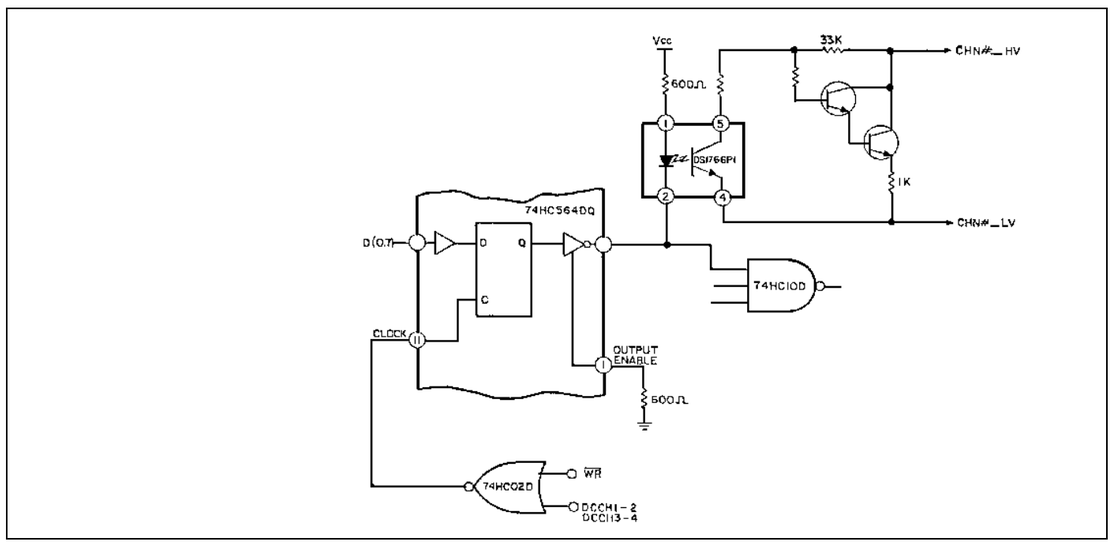


Figure 4 - Constant DC Current Generation

When the **/WR** and the **/DCCH3-4** inputs to U21D go low, U44 is selected to control the current generator circuit for channels 3 and 4.

When an input (D0-D7) to U33/U44 is low (logical 0) and the clock input goes high, the output goes high, or when the input is high (logical 1) and the clock goes high, the output goes low. The output connects to the cathode of an opto coupler (e.g. U40 (DS1766P1), Pin 2 (refer to Figure 4). With this input to U40 going low the internal LED turns on and the transistor conducts. The amount of conduction is determined by the resistor in the collector circuit (R98). This resistor determines the selected current level (2.5 mA) by determining the bias on the base of transistors Q23 and Q2. The emitter of the opto coupler transistor connects to the CHN1-LV. The voltage connected to the collector circuit of the transistor is derived from the CHN1-HV generated by the DC to DC converter U65 (150 Vdc). The conduction of the internal transistor of the opto coupler controls the conduction of transistors Q23 and Q2. In this case resistor R98 in the collector of U40 causes 2.5 mA to flow through Q2, through polarity selector relay K1 and through the channel line **CHN1 (+)** or **CHN1 (-)**.

Each opto coupler is selected by an output of flip-flop U33/U44 going low. The collector resistors of each opto coupler in a generator circuit are in parallel. Opto Coupler U40 is selected by U33 for 2.5 mA . Opto Coupler U41 is selected for 6 mA and U42 is selected **for** 11 mA. **None** of the first three opto couplers are selected for 0 mA. This makes the inputs to 3-input **NAND** gate U32A (74HC10D) high (logical 1) and the output low to select opto Coupler U43. Opto Coupler U43 has no collector resistor and pulls the bias voltage to Q23 low enough to stop any conduction of current.

Overvoltage protection is provided for the base circuit of transistors Q23 and Q2 by zener diode VR1. Zener diode VR2 regulates HV to approximately 20 Vdc which is used by U40 and U43. Additional filtering is provided by 10 µF capacitor C178.

The polarity switch K1/K2/K3 or K4 (LM44B00) determines in which side of the channel line the current flows (refer to Figure 5). Normally the CHN#_HV connects to K#, Pin 13, through the switch, to Pin 11 connected to the CH# (+) side of the line. The collectors of the associated transistor circuits connect to Pin 4, through the switch to Pin 6 connected to the CH# (-) side of the line. This condition allows a positive current signal to be sent to the conventional station. When a signal from microcontroller U7 through the D(7:0) bus to U33/U44 causes the transistor connected to K#, Pin 16 to conduct the switch activates. The CH#_HV on Pin 13 connects through the switch to Pin 9 connected to the CH# (-) side of the channel line. The collectors of the associated transistor circuits connect through Pin 4, through Pin 8 to the CHN# (+) side of the channel line. This allows a negative current signal to be sent to the conventional station.

TONE GENERATION

The tone generation circuits consist of programmable interval timers and a switched capacitor low-pass filter (Refer to Schematic Diagram, Sheet 2). The microcontroller U7 sets up the timer, through data bus D(7:0), so that the timer U28/U36 (82C54) generates the appropriate tone to be applied to the audio channel through the low-pass filter U29/U37/U38/U39 (DS3125P1, MF6) which passes the tone. The timer also provides clocking information to the filter for a clock reference which is 100 times the tone frequency. A clock reference is needed by the filter for square wave to sine wave conversion.

AMPLITUDE CONTROL

The amplitude of the tone from the output of the low-pass filter (U29, Pin 3) is applied to the non-attached amplifier stage located within the MF6 filter. Secure-it, Function and Hold Tone level differences are achieved by changing the feedback resistance of the amplifier stage. Analog switches U30 and U31 (4066BM) switch 49.9K ohms in parallel with 1.5 meg ohms for the Secure-it Tone and 178k ohms in parallel with 1.5 meg ohm for the Function Tone. The 1.5 meg ohm is used by itself for Hold Tone. The tone is added to the outgoing audio signal in a summing circuit. The microcontroller sets the level (specified by the Secure-it Tone level) of the Keying Tone by EEPOTS U71, U85, U86 and U88 (X9503S). These pots set the tone level prior to the audio summing stage.

The audio tone going to the conventional base station connects to a line coupling transformer (e.g. T2) through a 600 ohm resistor. Surge protection is provided for the T2 circuit by zener diodes VR9 and VR10. The audio can be monitored at test point TP4. The audio out channel lines are fuse protected by fuses F1 and F2.

The audio coming from the conventional base station connects to the CI board through line coupling transformer T3 when operation is in a 4-wire, full duplex operating mode. Surge protection is provided for the T3 circuit by zener diodes VR11 and VR12. The channel line is fuse protected by fuses F3 and F4. When in the 2-wire operating mode, the audio from the conventional base station comes in through coupling transformer T2.

The CI supports 2-wire (simplex) and 4-wire (full duplex) channel lines to the conventional base station. Microcontroller U7 sends command signals (e.g. **CHN1_SPLX**) using flip-flop U22 to select either the 2-wire or the 4-wire operating mode.

While operating in the 4-wire mode, U7 may be progrmmed to bridge the line. This is accomplished by activating the **LOAD_DIS[1]** signal from flip-flop U23. The **CHN1_SPLX** and **LOAD_DIS[1]** signals connect to SPDT analog switches U9A and U9B (MAX333) respectively. When U9A is activated the system operates in the 2-wire mode. When U9B is activated system operates with the 4-wire input load (600 ohms) **DISABLED**. Analog switch U9B allows the CI board to bridge the line in 4-wire operation by removing the 600 ohm termination making it a high impedance input.

The **CHN#_SPLX** signal is generated through flip-flop circuit U22 (74HC374). Flip-flop U22 is clocked by a **/PERSNL** and a **/WR** signal on the inputs of **NOR** gate U21B (74HC02D) (see Schematic Diagram, sheet 1). The output of U21B connects to the clock input, Pin 11, of U22. When clocked, U22 takes the information from the D(7:0) data bus, as generated by U7 and produces the appropriate **CH#_SPLX** signal. The **/PERSNL** signal is generated through decoder U27 (74HC154D). The /WR signal is generated by U7.

The **COR_SEL#** signal is also generated by U22 the same way the **CH#_SPLX** signal is generated. The **COR_SEL** will be covered later in this text.

The **LOAD_DIS[#]** is selected by U7 through the D(7:0) data bus and latch U23 (74HC573). Latch U23 is enabled by a **/CH_LOAD** and a **/WR** signal on the inputs of **NOR** gate U98B. The output of U98B connects to U23, Pin 11 **LEN**. The **/CH_LOAD** signal is generated by decoder U27.

Audio coming from the VMIM (e.g. **AUDIO_IN_H1/AUDIO_IN_L1**) is buffered through operational amplifier U69A (DS3070P3) and summed with a control tone at operational amplifier U69D, Pin 13 before being sent out over the appropriate conventional channel line with unity gain. Audio coming from the base station is passed directly to the VMIM with unity gain. The audio level from the conventional base station is adjusted through EEPOT U72 and is applied to the input of operational amplifier U70A. The output of U70A is rectified through diodes D6, D7 and D8 then applied to the input of a VOX circuit. The VOX detects audio and signals the microcontroller that audio is present.

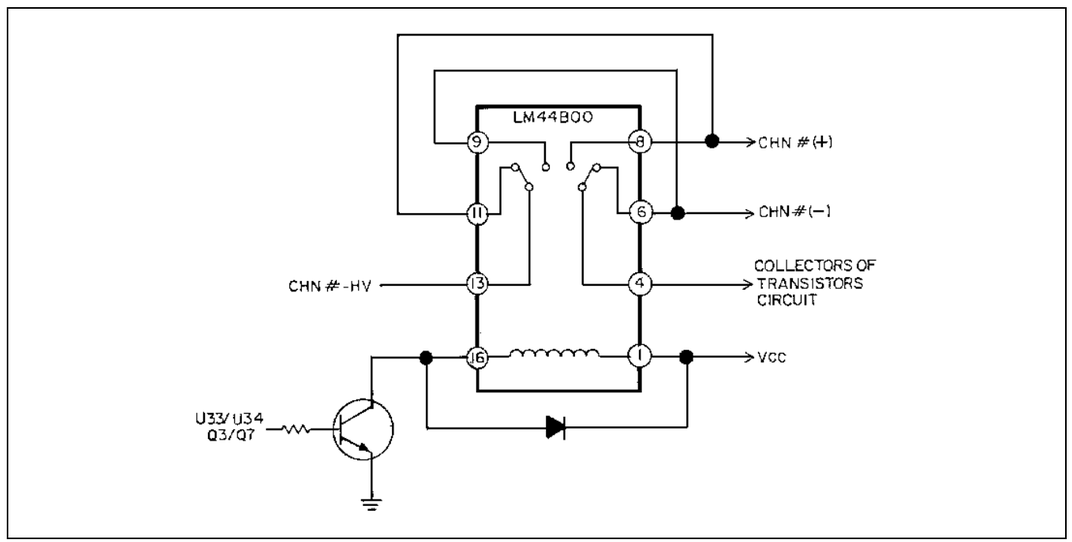


Figure 5 - Polarity Switch

VOX CIRCUIT

The VOX circuit, is a comparator circuit that compares the rectified audio from the diode circuit to the sum of a VOX threshold and the average background noise on the line. This circuit consist of operational amplifiers, e.g. U70B, U70C, U70D (DS3070P3) and comparator U93A (LM339D). If the rectified voice audio exceeds this sum, then the comparator U93A causes an interrupt logic to signal microcontroller U7 that the channel has been keyed. This interrupt signal passes through analog switch U9C (MAX333) to the base of transistor Q18 causing Q18 to conduct and turn LED CR5 on. LED CR5 indicates VOX **"trip"** for the channel. (The analog switch U9C allows use of a **C**arrier **O**perated **R**elay **(COR)** instead of VOX circuitry.) The signal then goes through inverter U75B (74HC14D) to flip-flop U6B and through inverter U75A to flip-flop U6A. The outputs of U6A (Pin 5, **VOX1_U** (Unkey)) and U6B (Pin 9, **VOX1_K** (Key)) go to the inputs of **NOR** gate U34A (refer to Schematic Diagram, Sheet 1). The output of U34A goes to an input of **AND** gate U10A. **AND** gate U10A applies the interrupt **(/INTO (VOX))** to Pin 16 of U7 (P3.2). Microcontroller U7 then reads P5.4/5/6/7 to see which channel generated the interrupt. In this case P5.4 would be low indicating channel 1. Then U7 would read P5.0 **(VOX STATUS)** to see whether channel 1 is indicating a **"KEY"** (P5.0=Low) or an **"UNKEY"** (P5.0=High).

A similar interrupt occurs when the voice audio stops. When the audio stops the rectified audio falls off. When the audio falls off the microcontroller is again interrupted. Microcontroller U7 determines that the channel has been unkeyed using Pins 17, 20, 21, 22, 38, 39, 40 and 49 of U7.

The VOX circuit for channel 1 is cleared by the **\INT1_CLR** signal generated by U7, Pin 8. This signal connects to U6B, Pin 13 **(*CLR)**.

CARRIER OPERATED RELAY

A **C**arrier **O**perated **R**elay **(COR)** may be used to interrupt the microprocessor and key/unkey the transmitter. In the case of channel 1, opto coupler U60D (see Schematic Diagram, Sheet 4) causes the **COR_IN[1]** line to go low as the result of an externally applied DC voltage on the anode and cathode. The **COR_IN[1]** signal is connected to analog switch U9C, Pin 12.

Flip-flop circuit U22 is enabled by a **/PERSNL** and a **/WR** signal on the inputs to **NOR** gate U21B. The **/WR** signal is generated by U7 and the **/PERSNL** signal is generated by U27. From the information on D(7:0), Flip-Flop U22 causes the **COR_SEL[1]** line to go low activating analog switch U9. When in this state, the **COR_IN[1]** signal is used to determine conventional channel activity instead of the VOX circuit. With **COR_IN[1]** low and U9 activated, a low is applied to the input of transistor Q18 through 100k ohm resistor R157. Transistor Q18 and VOX Interrupt indicator CR5 turn **OFF**. A high input on U75B, Pin 3 causes a high on the clock input to flip-flop U6A. This causes the output on U6A, Pin 5 to go high. This high is now on the VOX detection circuit **NOR** gate U34A, the output of which is monitored by **AND** gate U10A to generate the interrupt.

NOTE

If the **COR** option is not selected, the corresponding optocoupler in U60 will be available as a standard input.

RX DISABLE

An external **RX DISABLE** is provided by opto- coupler U94A (IL066-004). The collector of U94A connects to the base of transistor Q18 and the emitter connects to ground. The anode of the internal LED connects through 4.7k ohm resistor R1 to external voltage **Vext**. **Vext** is comes from J1, Pin 28C. When the **RX_DIS1** signal from J1, Pin 24C goes low, the opto coupler turns ON pulling the base of Q18 to ground. This disables the selected receiver by not allowing an interupt to be genrerated for that particular audio channel. LED CR5 will not come on either.

BASIC INPUTS

The user configured Basic Inputs (8) to the CI board is through opto couplers U59A-D and opto coupler U60A-D **(IL066-004)** (refer to Schematic Diagram, Sheet 4). These inputs (**OPT_IN_A1-A8** and **OPT_IN_B1-B8**) come from the backplane connector J2 (Bottom) (refer to Schematic Diagram, Sheet 5) The inputs **OPT_IN_A1** through **OPT_IN_A8** connect directly to the cathode **(K)** of the coupler. The inputs **OPT_IN_B1** through **OPT_IN_B8** connect through a 4.7k ohm resistor to the LED anode **(A)** of the coupler. The emitter of each opto coupler connects to ground. The collector connects to Vcc through a 10k ohm resistor. The collector also connects to an input of buffer line driver U58 (74HC240D). U58 is enabled by **/RD** and **/IO__ EN** signals on the inputs of **OR** gate U19A. When U58 is enabled any signal on the input is imposed on the D(7:0) bus. Opto Couplers 5-8 can be configured for use as COR inputs instead of using VOX.

BASIC OUTPUTS

The user configured Basic Outputs (8) from the CI board are provided through switching relays K5 through K12 (LM44B00). These circuits are controlled by octal, three state, D, flip-flop U61 (74HC374D) and transistor circuits Q10 through Q17. Flip-flop U61 is enabled by a **/WR** and a **/IO_EN** signal on the input to **NOR** gate U98A. The output of U98A connects to the clock input Pin 11, **CLK** of U61. When U61 is clocked, the information on the **D** inputs from the D(7:0) bus will be placed on the **Q** outputs. When a high (logical 1) is on the base of a transistor circuit, the associated switch activates and closes switch contacts between Pin 4 and Pin 8 (e.g. **RLY A1** and **RLY B1**). These **RLY** outputs are located on backplane connectors **J1** and **J2** (refer to Schematic Diagram, Sheet 5).

LED IDENTIFICATION

CR1	+5V
CR2	+12V
CR3	-12V
CR4	-5V
CR5	VOX or COR activated (Channel 1)
CR6	VOX or COR activated (Channel 2)
CR7	VOX or COR activated (Channel 3)
CR8	VOX or COR activated (Channel 4)
CR9	WATCHDOG ENABLE
CR10	RUN/RESET

SET UP

Conventional Interface Board DIP switch SW2 is normally set at system assembly and should not need changing. If, however, there is a need to check the switch positions, DIP switch bit definitions are as follows:

Bit 1 - Site Number (position **0** implies Site 1, conventional channels 1 through 32; position **1** implies Site 2, conventional channels 33 through 64)

Bit 2 - Tone/DC (test purposes only) **NOT USED** in normal operation **ON**=Test Mode, **OFF**=Normal Operation

Bit 3 - Default E&M signaling (test purposes only) Test Mode Indicator **ON** = Test Mode, **OFF**=Normal Operation

Bit 4 - Watch Dog Timer Enable/Disable **ON**=Enabled

Bits 5 - Channel Group (Bit 5 is the **M**ost **S**ignificant **B**it **(MSB)**

Site 1	**Site 2**
0 = invalid	0 = invalid
1 = Chn 1 - 4	1 = Chn 33 - 36
2 = Chn 5 - 8	2 = Chn 37 - 40
3 = Chn 9 - 12	3 = Chn 41 - 44
4 = Chn 13 - 16	4 = Chn 45 - 48
5 = Chn 17 - 20	5 = Chn 49 - 52
6 = Chn 21 - 24	6 = Chn 53 - 56
7 = Chn 25 - 28	7 = Chn 57 - 60
8 = Chn 29 - 32	8 = Chn 61 - 64
> 8 = invalid	> 8 = invalid

NOTES:

1. Position 0 or OFF corresponds to the switch in the downward position and position 1 or ON corresponds to the switch in the upward position.

2. The polarity of the lines carrying audio and DC signals to the conventional station on channel 2 (CHN2_HI and CHN2_L) is reversed for **Initial-revision CI boards**. This will only affect the operation of **DC-controlled stations**. It is most easily corrected by swapping the connections at the punch-block. Future revisions will correct the problem at the CI.

MONITOR MODULE (MOM)

Consult the **MO**nitor **M**odule **(MOM)** users manual to set **EE** Potentiometer settings for **VOX_TRIP** level and Tone Signaling Levels (if tone control) at the MOM PC. The MOM PC is also used to select which function tone frequency or DC control current level should be used by the CI board for each of the various station control functions (e.g. TX frequency, CG MON, VOX/COR selection, 2-wire/4-wire programming, bridging (if 4-wire) etc.). These selections must be made prior to system operation.

SYSTEM MANAGER

If a call is initiated from a conventional channel while the channel is included in a console patch/simulselect, the IMC will request a trunked channel for a caller whose LID corresponds to the channel number defined by bits 1 and 5-8 of DIP switch SW2 on the CI board. This LID will be from 1-64. Therefore, the LID must be defined as a LID in the system manager database or user validation must be disabled in the system.

TEST

Before the Conventional Interface can be tested, the CIA must be set up correctly (refer to the preceding **SET UP** section). To test the Conventional Interface, a module must be defined on the console for the conventional channel (refer to the console operator's manual for instructions). Select the conventional module and make sure the correct transmit and receive frequencies are selected. Transmit from the console and verify that the conventional station keys up and audio is heard on a conventional radio programmed to receive on the station transmit frequency.

Key a conventional radio which is programmed to transmit on the conventional station receiver frequency with proper Channel Guard. Verify that audio is heard on the selected speaker if the corresponding conventional channel module is selected at the console or on the unselected speaker if the conventional channel module is unselected.

Refer to the following **TROUBLESHOOTING** section if the above test is not successful.

QUICK REFERENCE TO TROUBLESHOOTING (Conventional Interface Board)

IMPORTANT TEST POINTS

TP26 - Vcc (+5 Vdc)
TP27 - +12 Vdc
TP28 - -12 Vdc
TP29 - -5 Vdc
TP30 - Ground (GND)

AUDIO TEST POINTS (TP)

	Chn1	Chn2	**Chn3**	**Chn4**
Audio From Trunked Audio Card	TP1	TP10	TP11	TP16
Audio To Conventional Station	TP4	TP7	TP14	TP19
Audio From Conventional Station To Trunked Audio Card.	TP3	TP8	TP13	TP18

TROUBLESHOOTING

1. Check Voltage LED's and **T**est **P**oints **(TP)** (If fail, check fuses).

2. Check to see if **RUN** LED is on (if off check for bent pins on EPROM U13).

CAUTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES

QUICK CHECKS

SYMPTOMS		**CONDITION TO CHECK**
1.	Call indicator (CR5 - CR8) **not** turned **ON** with incoming conventional call.	Check appropriate Test Point for audio from conventional Station. If no audio check cabling (check 2-wire/4-wire programming). Verify COR/VOX programming on MOM PC.
2.	Call indicator (CR5 - CR8) **ON**, but no audio with incoming conventional call	Check TP referred to above.If audio is there, check appropriate **"SITE-IN"** TP on trunked audio card. If **NO**→Check cabling between CI and trunked audio card(s). If **YES**→Check VMIM Slot allocations.
3.	No Tx audio from the MSC II to the convention station.	Check the appropriate **"SITE-OUT"** TP on the trunked audio card: If **NO**→ **Check VMIM DIP switches. Reset audio card.** If **YES**→ Check **"Audio From Trunked Audio Card"** test point (TP1/TP10/TP11 /TP16). If **NO** audio at the appropriate TP→Check CI to audio card cable. If **YES**→ **Check for "Audio To Conventional station"** test point (TP4/TP7/ TP14/TP19). If **NO** audio at the appropriate TP→ Bad CI card. If **YES**→ **Check cable from CI to conventional base station.** Check Tone/DC programming on MOM PC. Check receive and transmit frequency selections. Check tone levels and frequencies if tone controlled. Verify that tone signaling is turned OFF on the VMIM if tone controlled. Verify function Tone/DC control current programming.

Q2,Q5,Q7, & Q9
(TO-220) TRANSISTORS
(TOP VIEW)

LEAD IDENTIFICATION FOR
U62 & U63
(TO-220) INTEGRATED CIRCUITS
(TOP VIEW)

PIN 1 COMMON
PIN 2 OUTPUT
PIN 3 INPUT

LEAD IDENTIFICATION FOR
U64
(TO-220) INTEGRATED CIRCUIT
(TOP VIEW)

PIN 1 INPUT
PIN 2 COMMON
PIN 3 OUTPUT

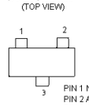
LEAD IDENTIFICATION FOR
Q23,Q24,Q25, & Q26
(TO-92) TRANSISTORS
(TOP VIEW)

LEAD IDENTIFICATION FOR
Q1,Q3,Q4,Q6,Q8,
Q10,Q11,Q12,Q13,Q14,
Q15,Q16,Q17,Q18,Q19,
Q20,Q21,Q22, & Q27
(SOT-23) TRANSISTORS
(TOP VIEW)

LEAD IDENTIFICATION FOR
VR1 THRU VR24
(SOT-23) ZENER DIODES
(TOP VIEW)

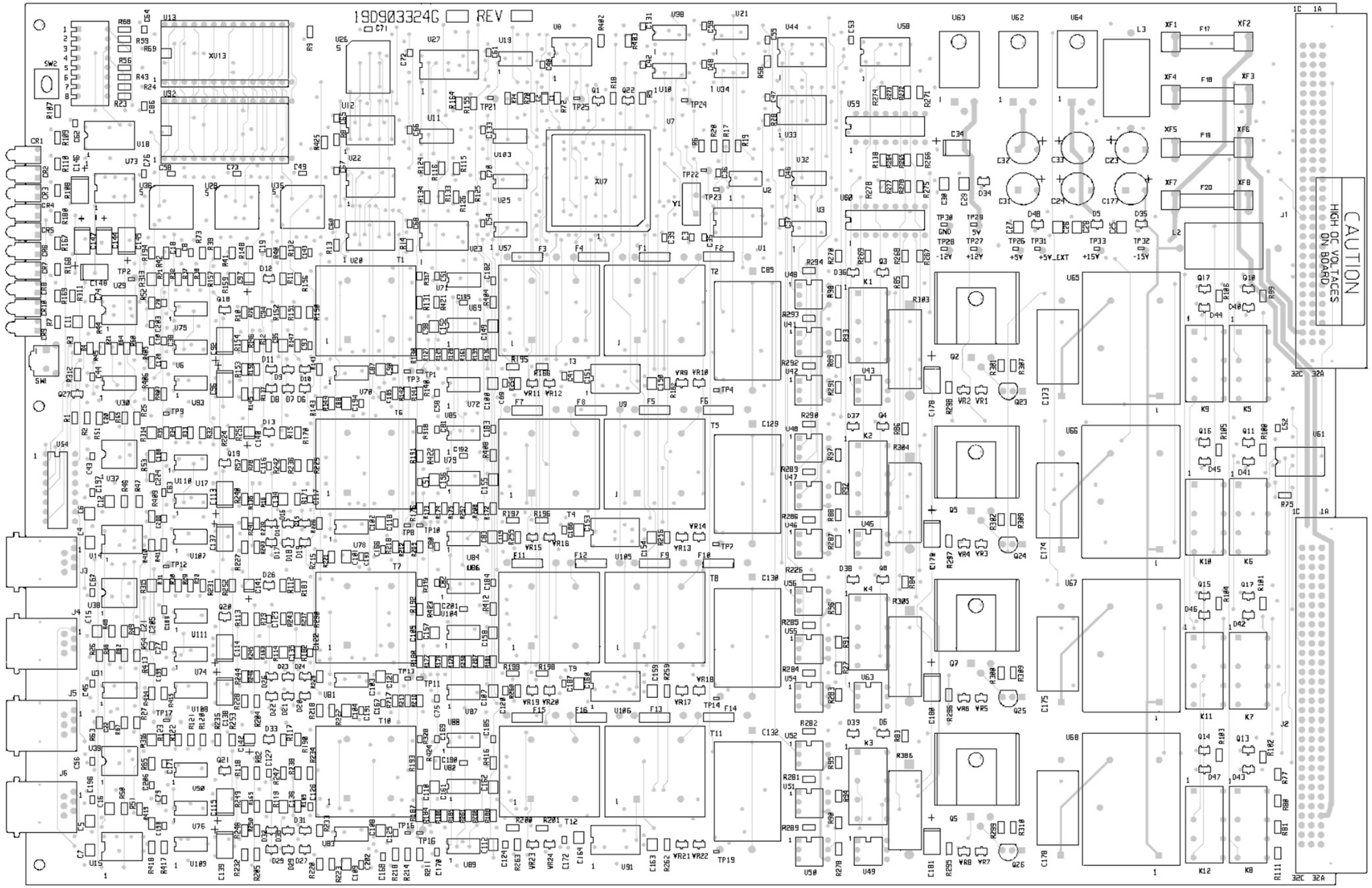
PIN 1 NC
PIN 2 ANODE
PIN 3 CATHODE

LEAD IDENTIFICATION FOR
D5 THRU D48
(SOT-23) DIODES
(TOP VIEW)



PIN 1 NC
PIN 2 ANODE
PIN 3 CATHODE

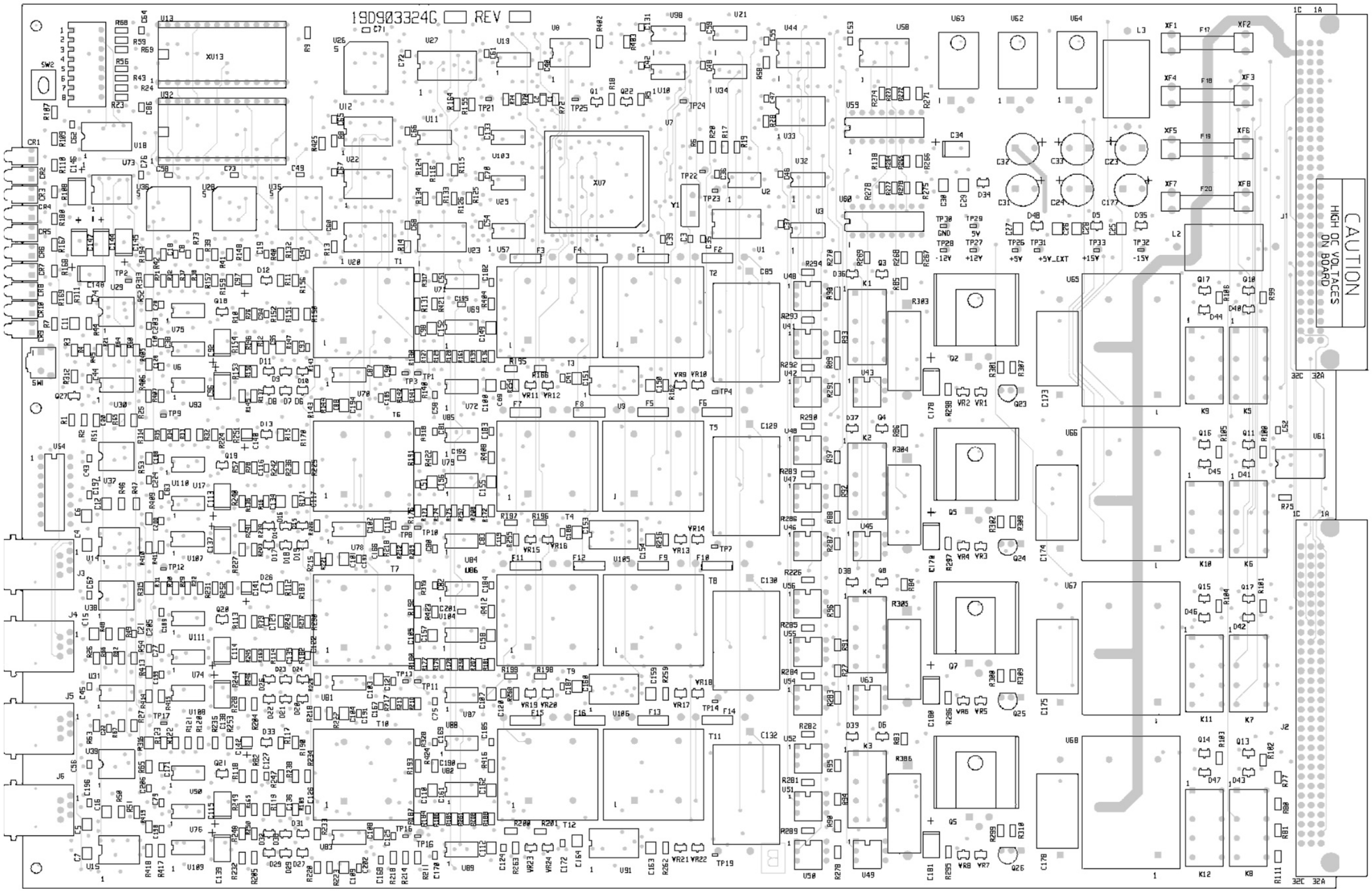
COMPONENT SIDE



E&M CONVENTIONAL
BASE STATION
Station Interface Board
19D903324P1

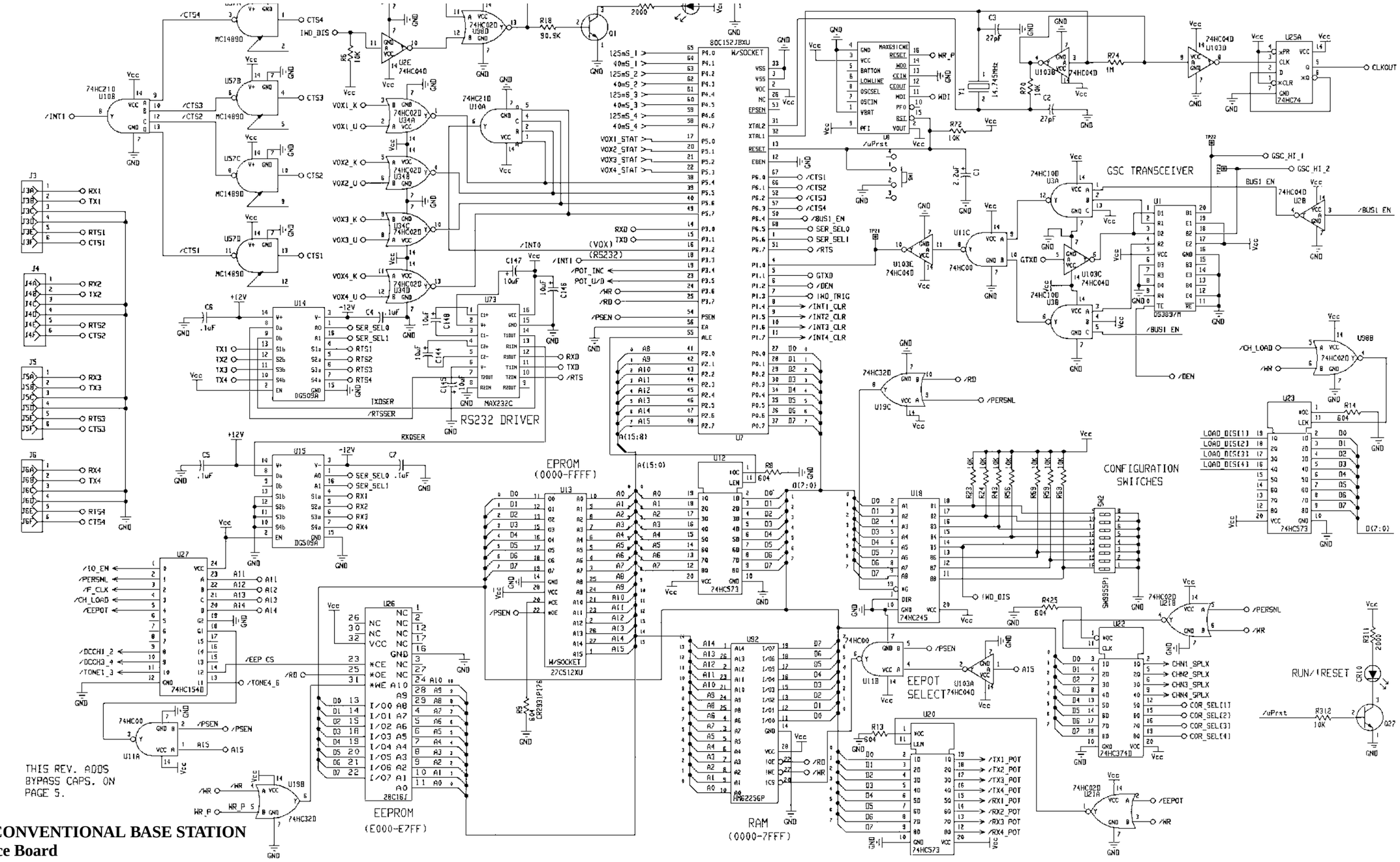
(19D903324, Rev. 1)
(19D903325, Layer 1, Rev. B)
(19D903325, Layer 2, Rev. B)

SOLDER SIDE - PWB PATTERN (VIEWED FROM COMPONENT SIDE)



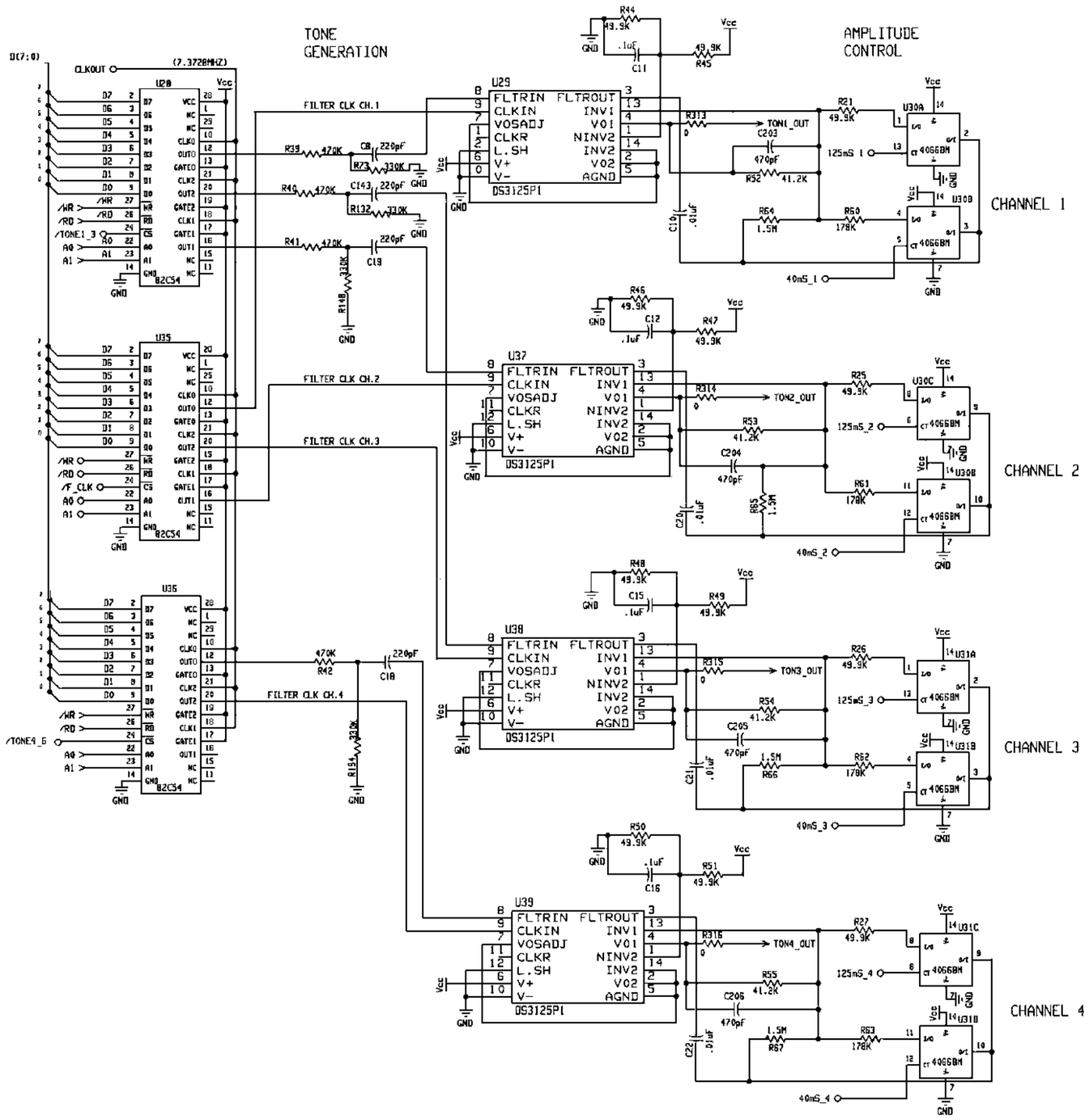
E&M CONVENTIONAL BASE STATION
Interface Board
19D903324P1

(19D903324, Rev. 1, Flipped)
(19D903325, Layer 8, Rev. B)
(19D903325, Layer 7, Rev. B (Flipped)
(19D903325, Layer 6, Rev. B (Flipped)



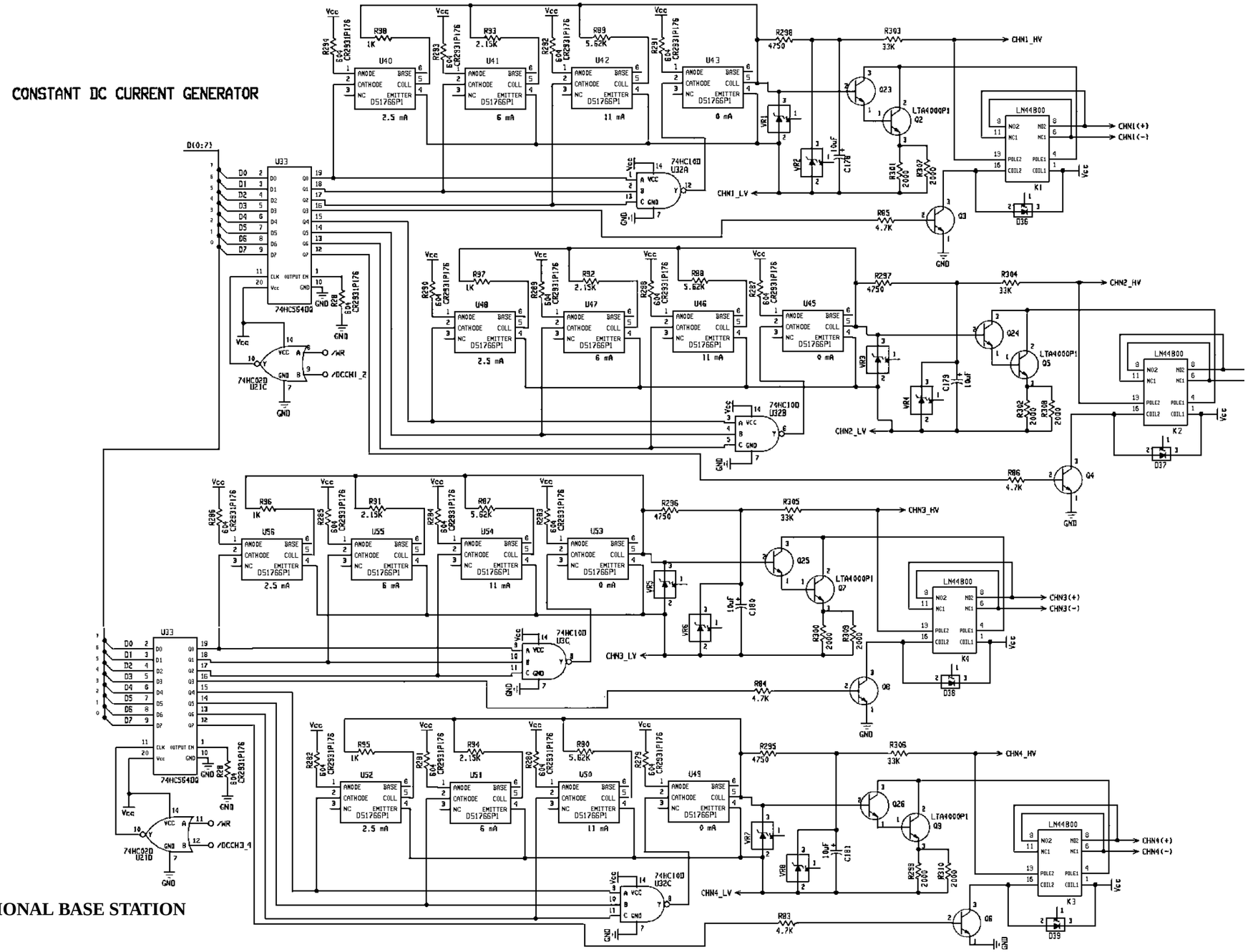
E&M CONVENTIONAL BASE STATION
Interface Board
19D903324P1
Sheet 1 of 9

(19D903326, Sh. 1, Rev. 1)



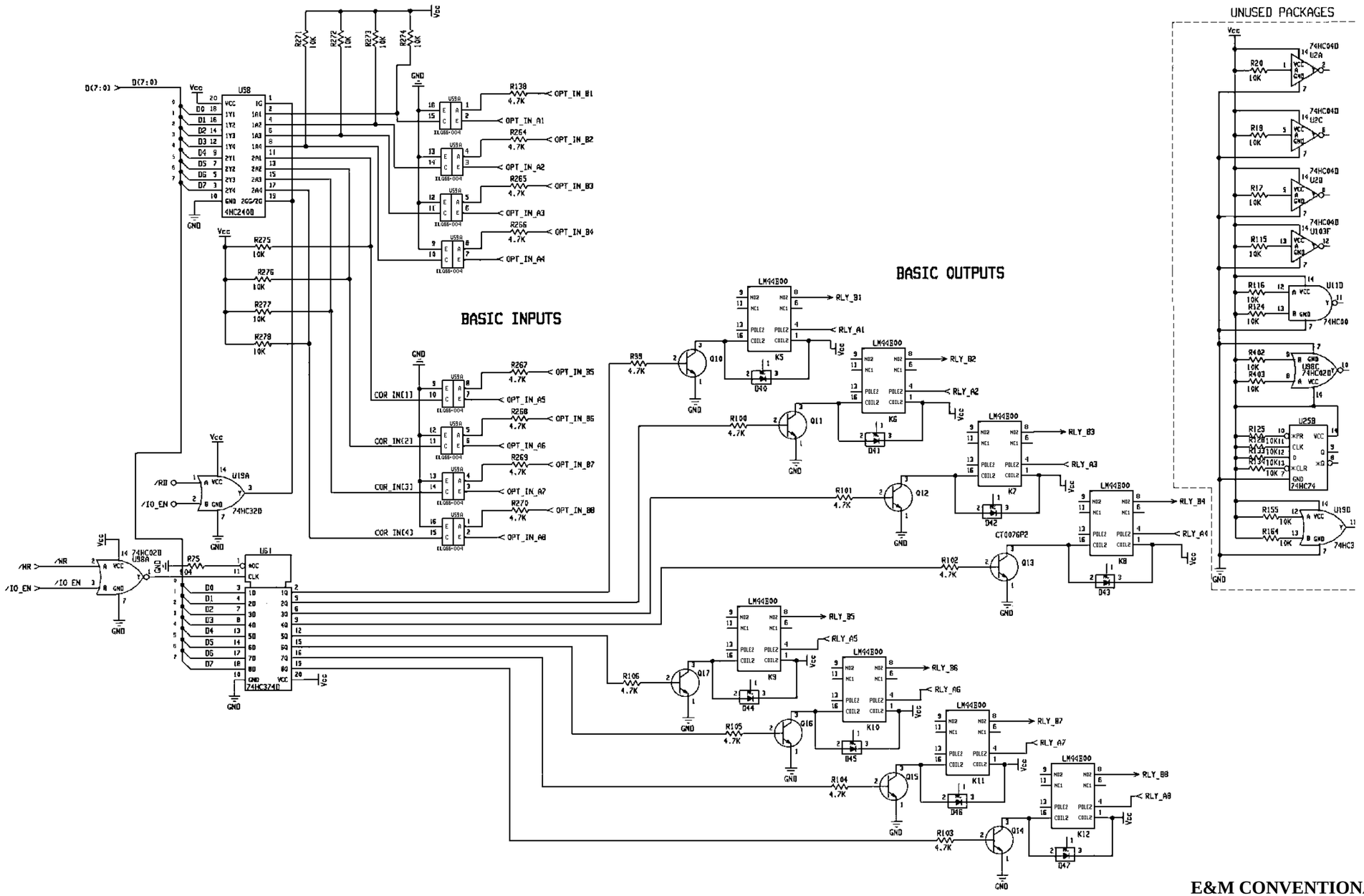
E&M CONVENTIONAL BASE STATION
Interface Board
19D903324P1
Sheet 2 of 9

(19D903326, Sh. 2, Rev. 1)



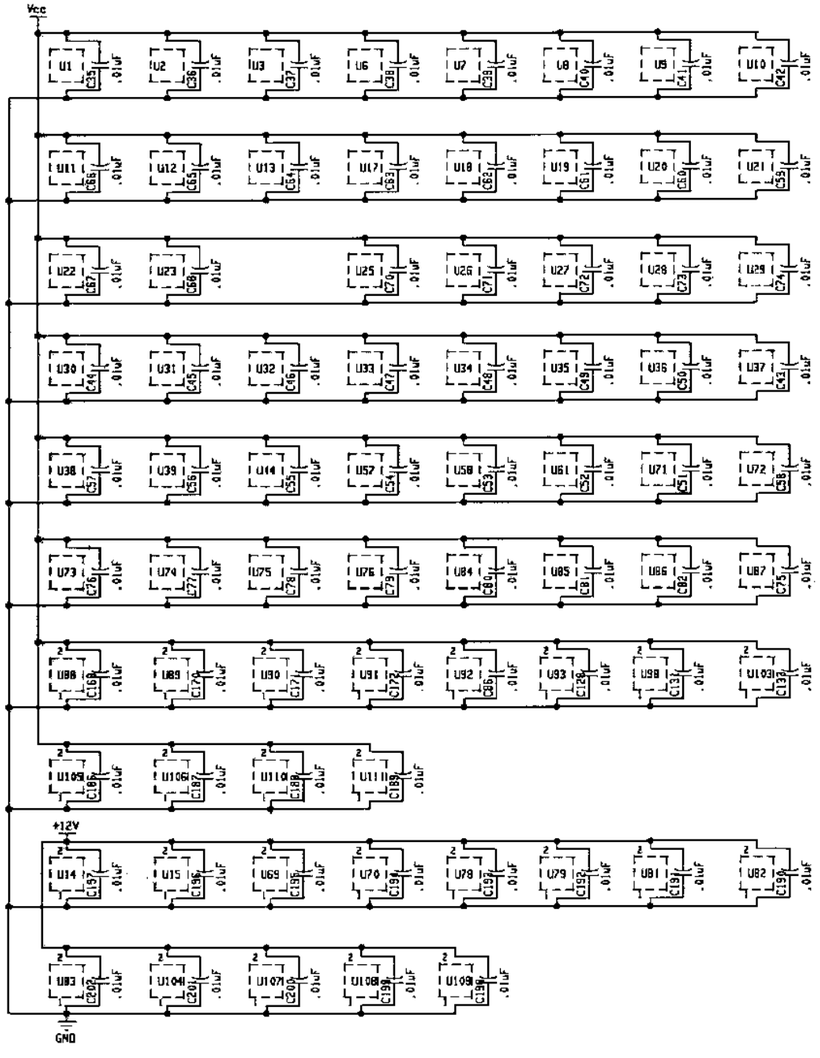
E&M CONVENTIONAL BASE STATION
Interface Board
19D903324P1
Sheet 3 OF 9

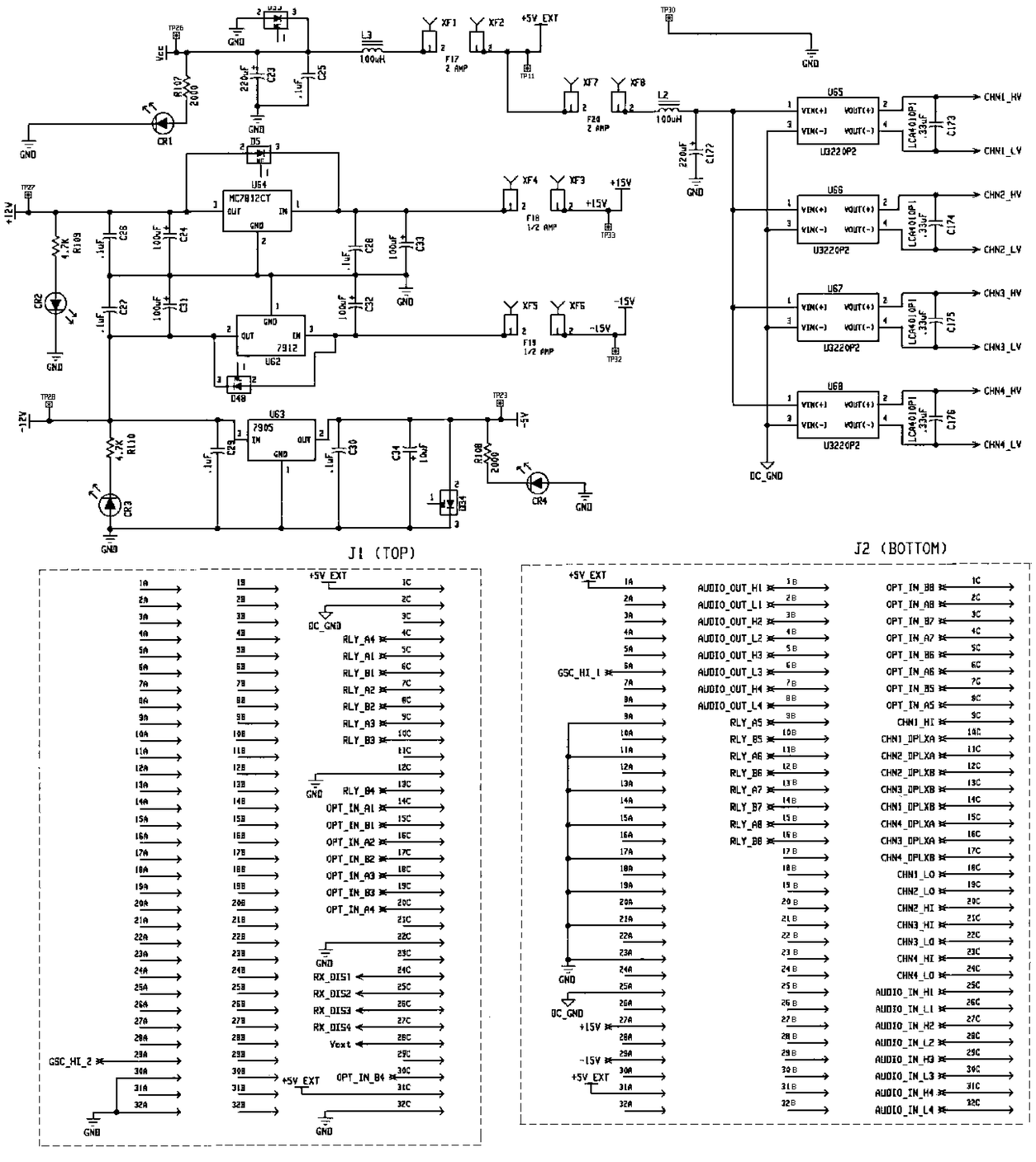
(19D903326, Sh. 3, Rev. 1)



E&M CONVENTIONAL BASE STATION
Interface Board
19D903324P1
Sheet 4 of 9

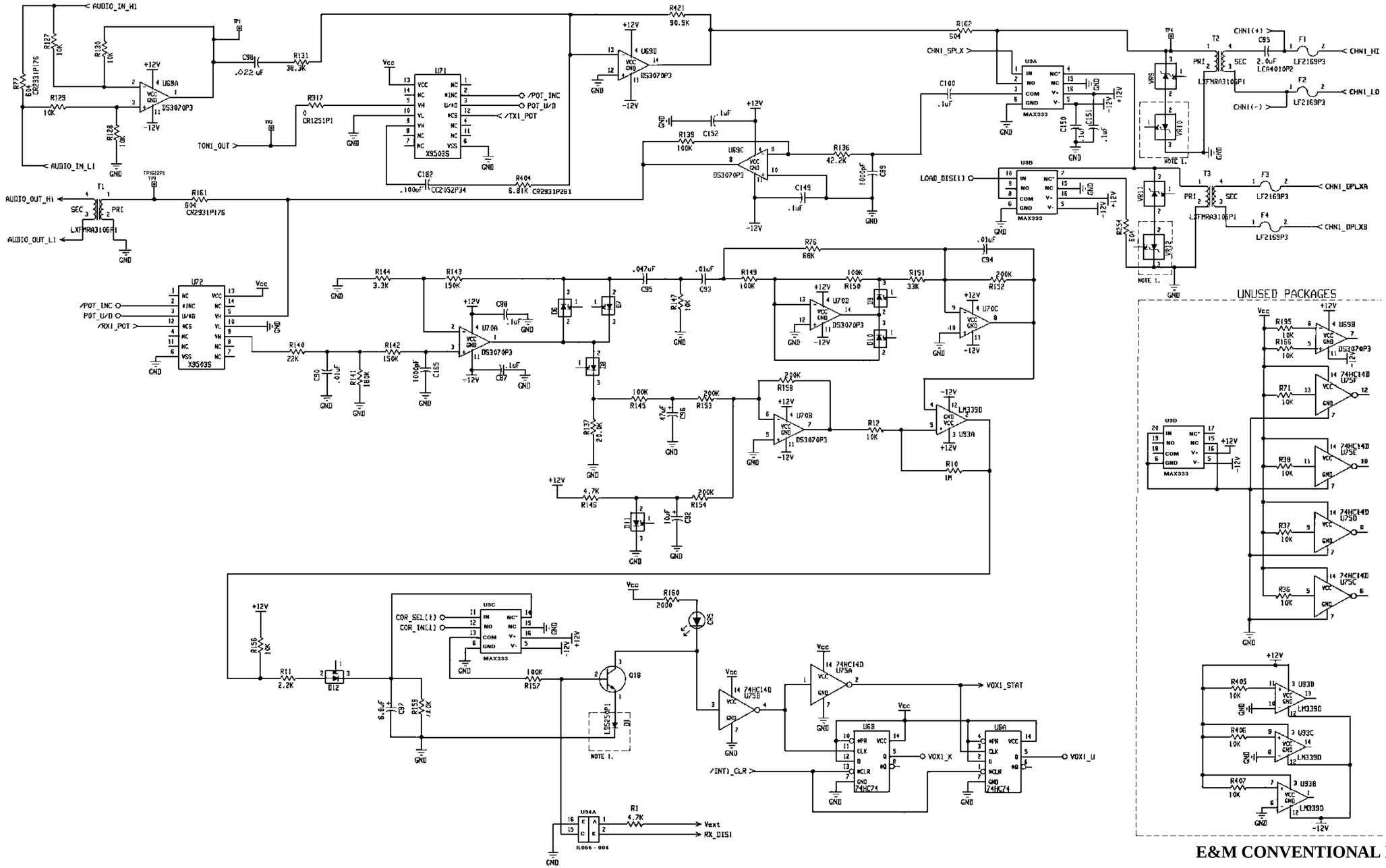
19D903326, Sh. 4, Rev. 1)





E&M CONVENTIONAL BASE STATION
Interface Board
19D903324P1
Sheet 5 of 9

(19D903326, Sh. 5, Rev. 1)



E&M CONVENTIONAL BASE STATION
Interface Board
19D903224P1
Sheet 6 of 9

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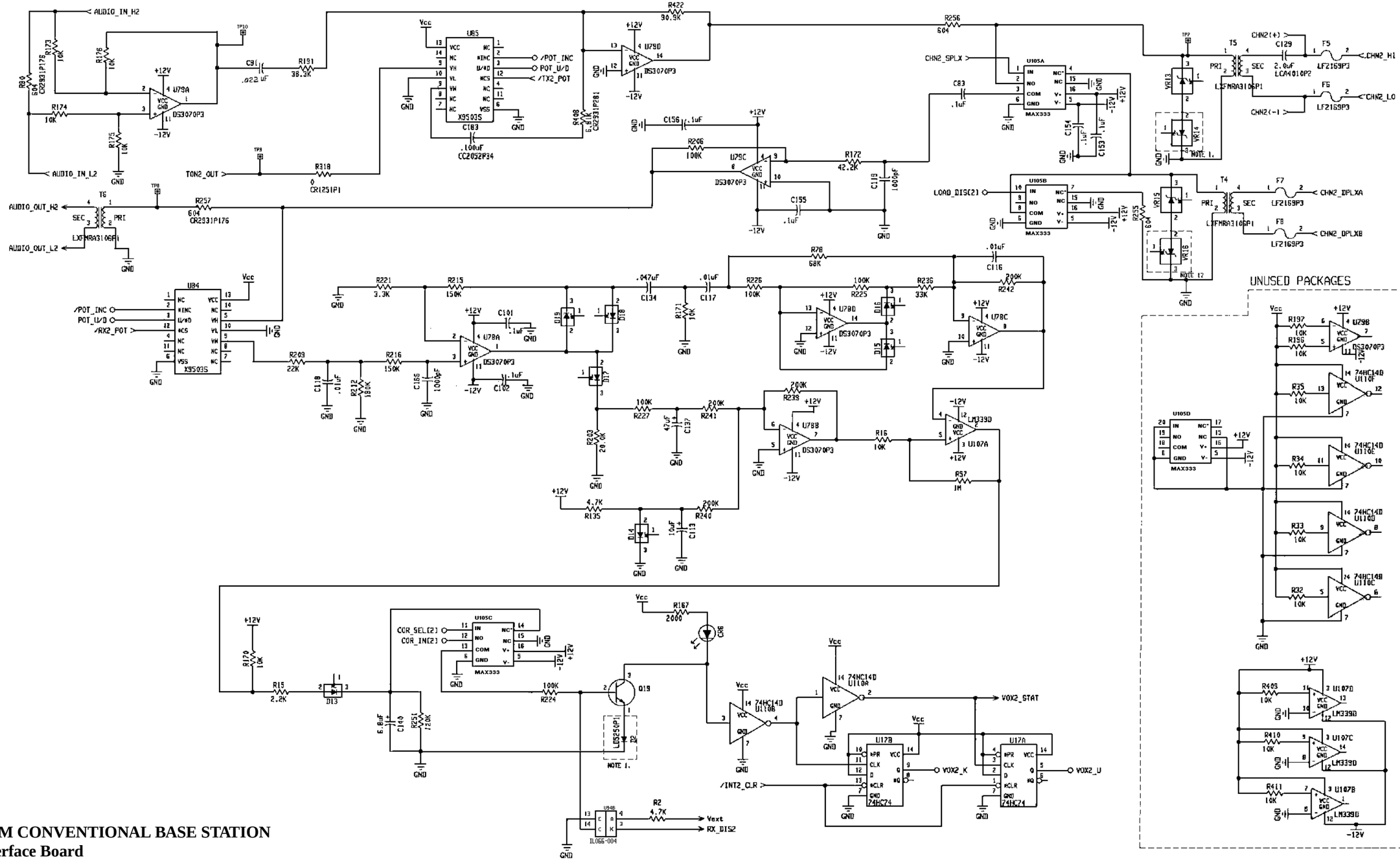
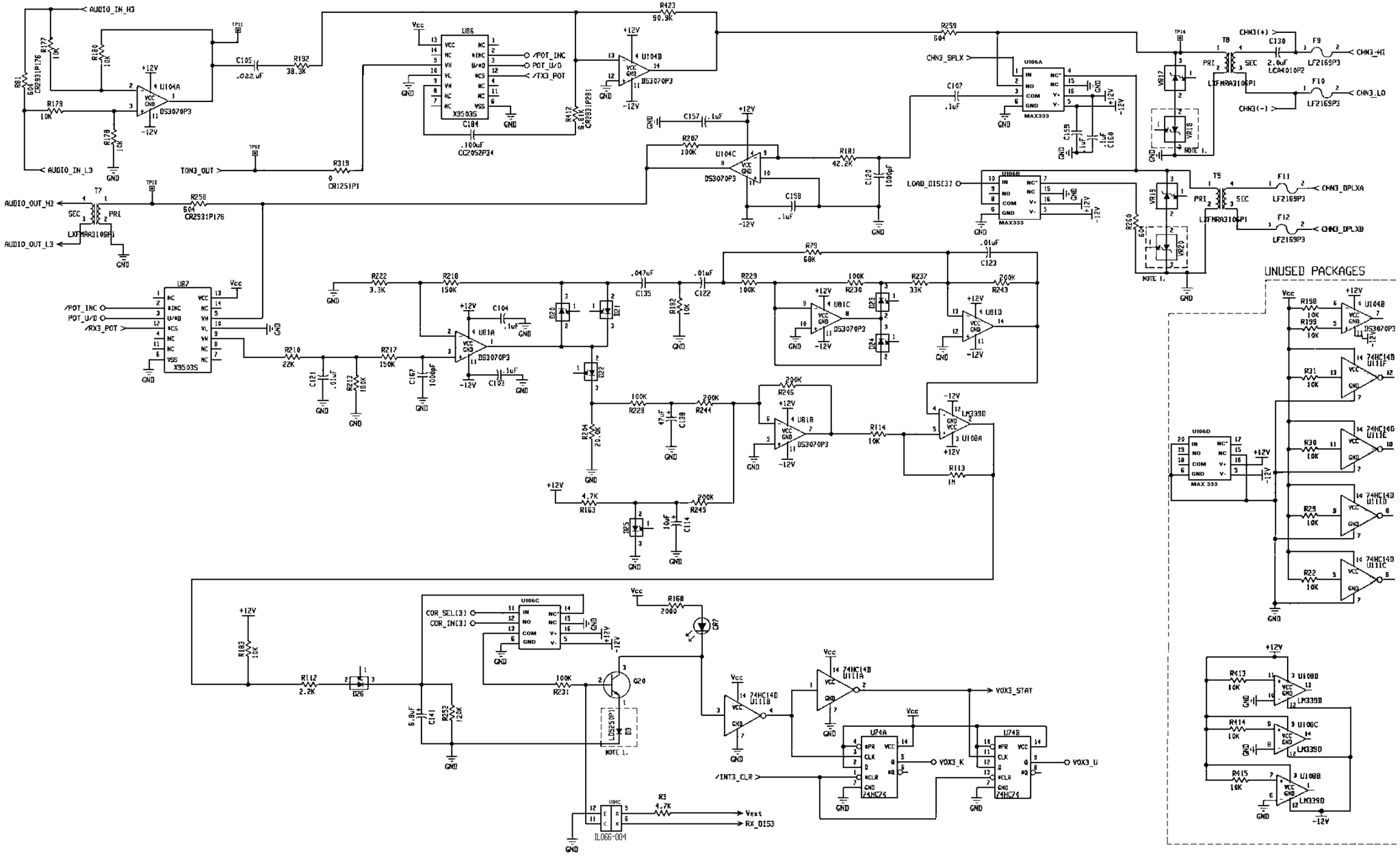


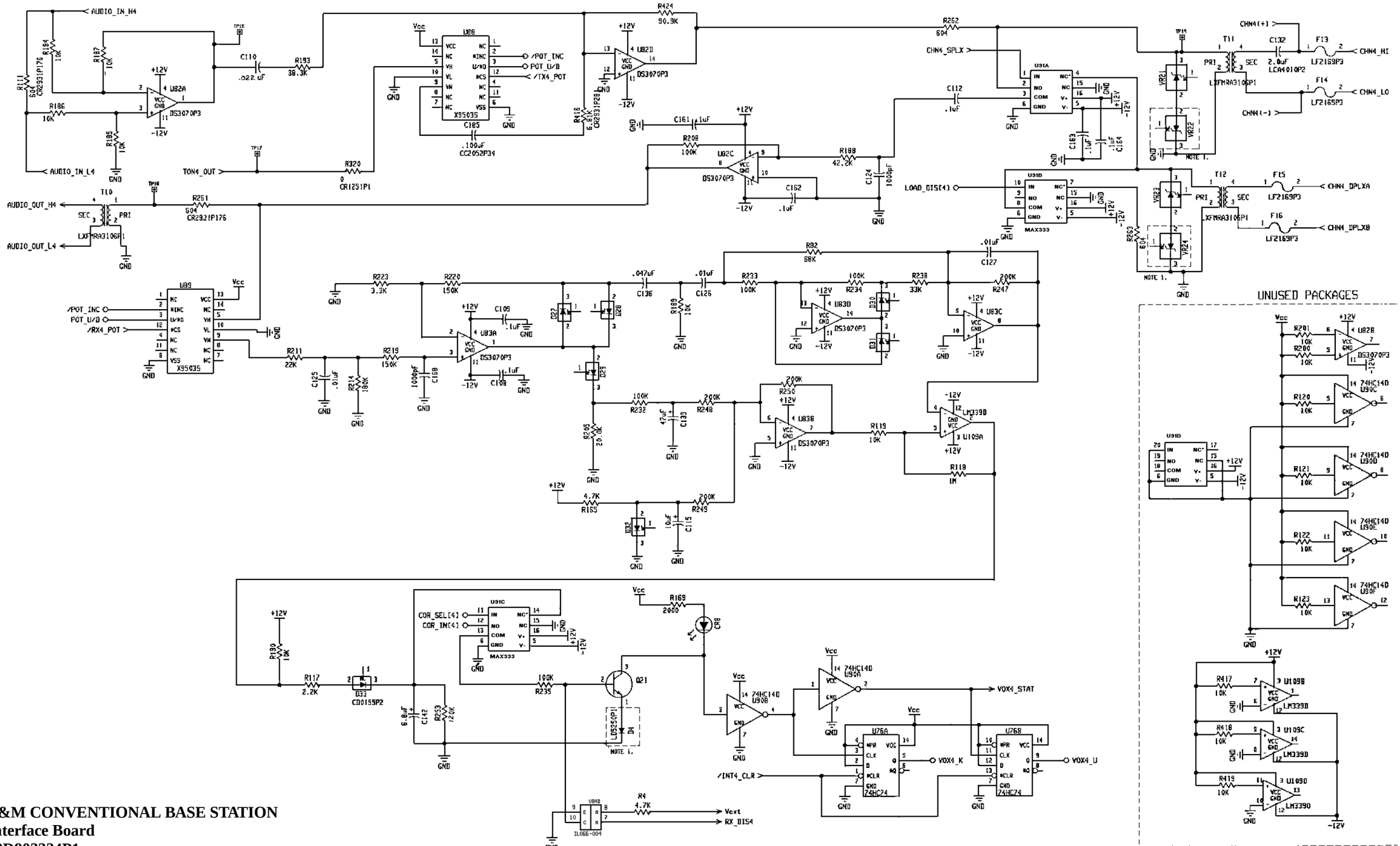
E&M CONVENTIONAL BASE STATION
Interface Board
19D903324P1
Sheet 7 of 9

(19D903326, Sh. 7, Rev 3)



E&M CONVENTIONAL BASE STATION
Interface Board
19D903324P1
Sheet 8 of 9

(19D903326, Sh. 8, Rev. 3)



E&M CONVENTIONAL BASE STATION
Interface Board
19D903324P1
Sheet 9 of 9

(19D903326, Sh. 9, Rev. 3)

CONVENTIONAL INTERFACE BOARD
19D903324P1
Issue 2

SYMBOL	PART NO.	DESCRIPTION
		CONVENTIONAL INTERFACE BOARD 344A3535G1
		- - - - - - - - - CAPACITORS- - - - - - - - -
C1	19A705205P19	Tantalum: 2.2 µF ±20%, 10 VDCW.
C2 and C3	19A702061P33	Ceramic: 27 pF ±5%, 50 VDCW, and temp coef 0 30 PPM/°C.
C4 thru C7	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C8	19A702061P69	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 30 PPM/°C.
C10	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C11 and C12	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C15 and C16	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C18 and C19	19A702061P69	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C20 thru C22	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C23	19A703314P2	Tantalum: 220 µF, -10+50%, 10 VDCW.
C24	19A703314P12	Electrolytic: 100 µF ±14%, 25 VDCW.
C25 thru C30	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C31 thru C33	19A703314P12	Electrolytic: 100 µF ±14%, 25 VDCW.
C34	19A705205P7	Tantalum: 10 µF, 25 VDCW; sim to Sprague 293D.
C35 thru C68	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C70 thru C82	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C83	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C85	344A4010P2	Polyester: 2 µF ±10%, 200 VDCW.
C86	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C87 and C88	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C89	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C90	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C91	19A702052P30	Ceramic: .022µF ±10%, 50 VDCW.
C92	19A705205P7	Tantalum: 10 µF, 25 VDCW; sim to Sprague 293D.
C93 and C94	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C95	19A702052P22	Ceramic: 0.047 µF ±10%, 50 VDCW.
C96	19A705205P111	Tantalum: 47 µF, 10 WVDC; sim to Sprague 293D.
C97	19A705205P5	Tantalum: 6.8 µF, 10 VDCW; sim to Sprague 293D.
C98	19A702052P30	Ceramic: .022 µF ±10%, 50 VDCW.
C100 thru C104	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C105	19A702052P30	Ceramic: .022 µF ±10%, 50 VDCW.
C107 thru C109	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C110	19A702052P30	Ceramic: .022 µF ±10%, 50 VDCW.
C112	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C113 thru C115	19A705205P7	Tantalum: 10 µF, 25 VDCW; sim to Sprague 293D.
C116 thru C118	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C119 and C120	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C121 thru C123	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C124	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C125 thru C128	19A702052P14	Ceramic: 0.01µF ±10%, 50 VDCW.
C129 and C130	344A4010P2	Polyester: 2 µF ±10%, 200 VDCW.
C131	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C132	344A4010P2	Polyester: 2 µF ±10%, 200 VDCW.
C133	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C134 thru C136	19A702052P22	Ceramic: 0.047 µF ±10%, 50 VDCW.
C137 thru C139	19A705205P111	Tantalum: 47 µF, 10 WVDC; sim to Sprague 293D
C140 thru C142	19A705205P5	Tantalum: 6.8 µF, 10 VDCW; sim to Sprague 293D
C143	19A702061P69	Ceramic: 220 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C144 thru C148	19A705205P7	Tantalum: 10 µF, 25 VDCW; sim to Sprague 293D
C149 thru C164	19A702052P26	Ceramic: 0.1 µF ±10%, 50 VDCW.
C165 thru C168	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C169 thru C172	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C173 thru C176	344A4010P1	Polyester: 0.33 µF ±10%, 200 VDCW.
C177	19A703314P2	Tantalum: 220 mF, -10+50%, 10 VDCW.
C178 thru C181	19A705205P7	Tantalum: 10 mF, 25 VDCW; sim to Sprague 293D.
C182 thru C185	19A702052P34	Ceramic: 0.1 µF ±10%, 25 VDCW.
C186 thru C202	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C203 thru C206	19A702052P3	Ceramic: 470 pF ±10%, 50 VDCW.
		- - - - - - - - - - DIODES - - - - - - - - - -
CR1 thru CR10	19A703595P9	LED: Green.
D1 thru D4	19A115250P1	Silicon, fast recovery, 225 mA, 50 PIV.
D5 thru D48	19A700155P2	Silicon, fwd current: 100 mA, 35 VIP.
		- - - - - - - - - - FUSES - - - - - - - - - -
F1 thru F16	19A702169P3	Enclosed Fuse Link: 0.375 amp.
F17	19A134961P20	Fuse: 2 amp @ 250V, slow blow.
F18 and F19	19A134961P10	Cartridge: 1/2 amp @ 250 volts; sim to Littlefuse 213.500.
F20	19A134961P20	Fuse: 2 amp @ 250V, slow blow.
		- - - - - - - - - - JACKS - - - - - - - - - -
J1 and J2	19B801587P4	Connector, DIN: 96 male contacts, right angle mounting; sim to AMP 532505-1.
J3 thru J6	344A3288P3	Modular jack: 6-position; sim to AMP 555163-1.
		- - - - - - - - - - RELAYS - - - - - - - - - -
K1 thru K12	19B235621P1	RELAY: 2 form C, 5VDC operating sim to General Inst. HGZMZ-C05.
		- - - - - - - - - - INDUCTORS - - - - - - - - - -
L2 and L3	19A149806P2	Reactor: 100 µH @ 2.1 amp ±10%.
		- - - - - - - - - - TRANSISTORS - - - - - - - - -
Q1	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile
Q2	344A4000P1	Silicon, NPN: sim to MJF47.
Q3 and Q4	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q5	344A4000P1	Silicon, NPN: sim to MJF47.
Q6	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q7	344A4000P1	Silicon, NPN: sim to MJF47.
Q8	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q9	344A4000P1	Silicon, NPN: sim to MJF47.
Q10 thru Q22	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
*Q23 thru *Q26	RYN1216010/1	Silicon, NPN: High voltage.
Q27	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1 thru R4	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R5	19B800607P332	Metal film: 3.3K ohms ±5%, 1/8 w.
R6	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R7	19A702931P230	Metal film: 2000 ohms ±1%, 200 VDCW, 1/8 w.
R8 and R9	19A702931P176	Metal film: 604 ohms ±1%, 200 VDCW, 1/8 w.
R10	19B800607P105	Metal film: 1M ohms ±5%, 1/8 w.
R11 and R12	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R13 and R14	19A702931P176	Metal film: 604 ohms ±1%, 200 VDCW, 1/8 w.
R15 thru R17	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R18	19A702931P393	Metal film: 90.9K ohms ±1%, 200 VDCW, 1/8 w.
R19 and R20	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R21	19A702931P368	Metal film: 49.9K ohms ±1%, 200 VDCW, 1/8 w.
R22 thru R24	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R25 thru R27	19A702931P368	Metal film: 49.9K ohms ±1%, 200 VDCW, 1/8 w.
R28	19A702931P176	Metal film: 604 ohms ±1%, 200 VDCW, 1/8 w.
R29 thru R38	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R39 thru R42	19B800607P474	Metal film: 470K ohms ±5%, 1/8 w.
R43	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R44 thru R51	19A702931P368	Metal film: 49.9K ohms ±1%, 200 VDCW, 1/8 w.
R52 thru R55	19A702931P360	Metal film: 41.2K ohms ±1%, 200 VDCW, 1/8 w.
R56	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R57	19B800607P105	Metal film: 1M ohms ±5%, 1/8 w.
R58	19A702931P176	Metal film: 604 ohms ±1%, 200 VDCW, 1/8 w.
R59	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R60 thru R63	19A702931P425	Metal film: 178K ohms ±1%, 200 VDCW, 1/8 w.
R64 thru R67	19B800607P155	Metal film: 1.5M ohms ±5%, 1/8 w.
R68 thru R72	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R73	19B800607P334	Metal film: 330K ohms ±5%, 1/8 w.
R74	19B800607P105	Metal film: 1M ohms ±5%, 1/8 w.
R75	19A702931P176	Metal film: 604 ohms ±1%, 200 VDCW, 1/8 w.
R76	19B800607P683	Metal film: 68K ohms ±5%, 1/8 w.
R77	19A702931P176	Metal film: 604 ohms ±1%, 200 VDCW, 1/8 w.
R78 and R79	19B800607P683	Metal film: 68K ohms ±5%, 1/8 w.
R80 and R81	19A702931P176	Metal film: 604 ohms ±1%, 200 VDCW, 1/8 w.
R82	19B800607P683	Metal film: 68K ohms ±5%, 1/8 w.
R83 thru R86	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R87 thru R90	19A702931P273	Metal film: 5620 ohms ±1%, 200 VDCW,1/8 w.
R91 thru R94	19A702931P233	Metal film: 2150 ohms ±1%, 200 VDCW, 1/8 w.
R95 thru R98	19A702931P201	Metal film: 1000 ohms ±1%, 200 VDCW,1/8 w.
R99 thru R106	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R107 and R108	19A702931P230	Metal film: 2000 ohms ±1%, 200 VDCW,1/8 w.
R109 and R110	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R111	19A702931P176	Metal film: 604 ohms ±1%, 200 VDCW, 1/8 w.

* COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

SYMBOL	PART NO.	DESCRIPTION
R112	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R113	19B800607P105	Metal film: 1M ohms ±5%, 1/8 w.
R114 thru R117	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R118	19B800607P105	Metal film: 1M ohms ±5%, 1/8 w.
R119 thru R126	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R127 thru R130	19A702931P301	Metal film: 10K ohms ±1%, 200 VDCW, 1/8 w.
R131	19A702931P357	Metal film: 38.3K ohms ±1%, 200 VDCW, 1/8 w.
R132	19B800607P334	Metal film: 330K ohms ±5%, 1/8 w.
R133 and R134	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R135	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R136	19A702931P361	Metal film: 42.2K ohms ±1%, 200 VDCW, 1/8 w.
R137	19A702931P330	Metal film: 20K ohms ±1%, 200 VDCW, 1/8 w.
R138	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R139	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R140	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R141	19B800607P184	Metal film: 180K ohms ±5%, 1/8 w.
R142 and R143	19B800607P154	Metal film: 150K ohms ±5%, 1/8 w.
R144	19B800607P332	Metal film: 3.3K ohms ±5%, 1/8 w.
R145	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R146	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R147	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R148	19B800607P334	Metal film: 330K ohms ±5%, 1/8 w.
R149 and R150	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R151	19B800607P333	Metal film: 33K ohms ±5%, 1/8 w.
R152 thru R154	19A702931P430	Metal film: 200K ohms ±1%, 200 VDCW, 1/8 w.
R155 and R156	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R157	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R158	19A702931P430	Metal film: 200K ohms ±1%, 200 VDCW, 1/8 w.
R159	19B800607P474	Metal film: 470K ohms ±5%, 1/8 w.
R160	19A702931P230	Metal film: 2000 ohms ±1%, 200 VDCW, 1/8 w.
R161 and R162	19A702931P176	Metal film: 604 ohms ±1%, 200 VDCW, 1/8 w.
R163	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R164	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R165	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R166	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R167 thru R169	19A702931P230	Metal film: 2000 ohms ±1%, 200 VDCW, 1/8 w.
R170 and R171	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R172	19A702931P361	Metal film: 42.2K ohms ±1%, 200 VDCW, 1/8 w.
R173 thru R180	19A702931P301	Metal film: 10K ohms ±1%, 200 VDCW, 1/8 w.
R181	19A702931P361	Metal film: 42.2K ohms ±1%, 200 VDCW, 1/8 w.
R182 and R183	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R184 thru R187	19A702931P301	Metal film: 10K ohms ±1%, 200 VDCW, 1/8 w.
R188	19A702931P361	Metal film: 42.2K ohms ±1%, 200 VDCW, 1/8 w.
R189 and R190	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R191 thru R193	19A702931P357	Metal film: 38.3K ohms ±1%, 200 VDCW, 1/8 w.
R194	19B800607P334	Metal film: 330K ohms ±5%, 1/8 w.
R195 thru R201	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R203 thru R205	19A702931P330	Metal film: 20K ohms ±1%, 200 VDCW, 1/8 w.
R206 thru R208	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R209 thru R211	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R212 thru R214	19B800607P184	Metal film: 180K ohms ±5%, 1/8 w.
R215 thru R220	19B800607P154	Metal film: 150K ohms ±5%, 1/8 w.
R221 thru R223	19B800607P332	Metal film: 3.3K ohms ±5%, 1/8 w.
R224 thru R235	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R236 thru R238	19B800607P333	Metal film: 33K ohms ±5%, 1/8 w.
R239 thru R250	19A702931P430	Metal film: 200K ohms ±1%, 200 VDCW, 1/8 w.
R251 thru R253	19B800607P474	Metal film: 470K ohms ±5%, 1/8 w.
R254 thru R263	19A702931P176	Metal film: 604 ohms ±1%, 200 VDCW, 1/8 w.
R264 thru R270	19B800607P472	Metal film: 4.7K ohms ±5%, 1/8 w.
R271 thru R278	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R279 thru R294	19A702931P176	Metal film: 604 ohms ±1%, 200 VDCW, 1/8 w.
R295 thru R298	19A702931P266	Metal film: 4750 ohms ±1%, 200 VDCW, 1/8 w.
R299 thru R302	19A702931P230	Metal film: 2000 ohms ±1%, 200 VDCW, 1/8 w.
R303 thru R306	19A700111P99	Composition: 33K ohms ±5%, 2 w.
R307 thru R311	19A702931P230	Metal film: 2000 ohms ±1%, 200 VDCW, 1/8 w.
R312	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R313 thru R316	19B800607P1	Metal film: Jumper.
R317 thru R320	19B801251P1	Jumper.
R402 and R403	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R404	19A702931P281	Metal film: 6810 ohms ±5%, 200 VDCW, 1/8 w.
R405 thru R407	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R408	19A702931P281	Metal film: 6810 ohms ±1%, 200 VDCW, 1/8 w.
R409 thru R411	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R412	19A702931P281	Metal film: 6810 ohms ±1%, 200 VDCW, 1/8 w.
R413 thru R415	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R416	19A702931P281	Metal film: 6810 ohms ±1%, 200 VDCW, 1/8 w.
R417 thru R419	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R421 thru R424	19A702931P393	Metal film: 90.9K ohms ±1%, 200 VDCW, 1/8 w.
R425	19A702931P176	Metal film: 604 ohms ±1%, 200 VDCW, 1/8 w.
		---------- SWITCHES ---------
SW1	19A149923P1	Push; sim to ITT SCHADOW KSAIV311.
SW2	19A149955P1	Rocker switch.
		---------- TRANSFORMERS --------
T1 thru T12	344A3106P1	Audio Frequency.
		---------- TEST POINTS ---------
TP1 thru TP4	19A701622P1	Cotter pin.
TP7 thru TP14	19A701622P1	Cotter pin.
TP16 thru TP19	19A701622P1	Cotter pin.
TP21 thru TP33	19A701622P1	Cotter pin.
		-------- INTEGRATED CIRCUITS -------
U1	19A149953P202	TRANSCEIVER; 4-Channel, sim to TISN75ALS057.
U2	19A703483P104	Digital: CMOS Hex Inverter; sim to 74HC04.
U3	19A703483P306	Triple 3-Input NAND Gate; sim to 74HC10.
U6	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U7	19A705982P101	Microcomputer, CMOS 8-Bit.
U8	19A149895P1	Microprocessor, Supervisory Circuit; sim to MAX691C.
U9	344A3113P101	Analog Switch, Quad SPDT, CMOS; sim to MAX333.
U10	19A703483P320	Dual 4-Input Position AND Gates; sim to 74HC21.
U11	19A703483P302	Digital: Quad 2-Input NAND Gate; sim to 74HC00
U12	19A703471P318	Digital: Octal Tri-State Transceiver/Latch; sim to 74HC573.
U14 and U15	344A3171P1	Multiplexer, Monolitic Analog; sim to DG509A.
U17	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U18	19A703471P308	Octal Bus Transceiver w/3-State input; sim to 74HC245.
U19	19A703483P111	Digital: CMOS Quad 2-Input OR Gate; sim to 74HC32.
U20	19A703471P318	Digital: Octal Tri-State Transceiver/Latch; sim to 74HC573.
U21	19A703483P101	Digital: CMOS Quad 2-Input NOR Gate; sim to 74HC02.
U22	19A704380P112	Digital: CMOS Octal Tri-State Data Flip-Flop; sim to 74HC374.
U23	19A703471P318	Digital: Octal Tri-State Transceiver/Latch; sim to 74HC573.
U25	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U26	19A703952P105	EEPROM, 2 K x 8, 5 Volts.
U27	19A703471P326	4 TO 16 Decoder/Demux; sim to 74HC154.
U28	19A149466P301	CH MOS Programmable Timer, sim to 82C54.
U29	344A3125P1	LINEAR, Filter, Switched Capacitor; sim to MF6-100.
U30 and U31	19A702705P1	Digital: Qaud Analog Switch/Multiplexer; sim to 4066BM
U32	19A703483P306	Triple 3-Input NAND Gate; sim to 74HC10.
U33	19A704380P315	Octal 3-State Inverting F-F; sim to 74HC564.
U34	19A703483P101	Digital: CMOS Quad 2-Input NOR Gate; sim to 74HC02.
U35 and U36	19A149466P301	CH MOS Programmable Timer, sim to 82C54.
U37 thru U39	344A3125P1	LINEAR, Filter, Switched Capacitor; sim to MF6-100.
U40 thru U42	19A701766P1	Coupler, optoelectronic.
*U43	RYR353608/1	Optocoupler.
U44	19A704380P315	Octal 3-State Inverting F-F; sim to 74HC564.
*U45	RYR353608/1	Optocoupler.
U46 thru U48	19A701766P1	Coupler, optoelectronic.
*U49	RYR353608/1	Optocoupler.
U50 thru U52	19A701766P1	Coupler, optoelectronic.
*U53	RYR353608/1	Optocoupler.
U54 thru U56	19A701766P1	Coupler, optoelectronic.
U57	19A116704P102	Quad DTL Line Receiver.
U58	19A703471P325	Octal Buffers And Line Drivers w/3-State Outputs; sim to 74HC240.
U59 and U60	344A3071P1	Optocoupler, Photo Darlington.
U61	19A704380P112	Digital: CMOS Octal Tri-State Data Flip-Flop; sim to 74HC374.
U62	19A134718P2	Linear: -12 Volt Regulator; sim to µA7912U.
U63	19A134718P1	Linear: -5 Volt Regulator; sim to µA7905U.
U64	19A134717P2	Linear: 12 Volt Regulator: sim to MC7812CT.
U65 thru U68	344A3220P2	DC-DC Converter, 5Vin, 150Vout; sim to ERG E505-1.515u.
U69 and U70	344A3070P3	LINEAR, JFET Input Operational Amp; sim to TL074.
U71 and U72	19A705180P101	Digital Controlled Potentiometer, 50K ohms.
U73	19A149446P2	Digital: Transmitter/Receiver; sim to MAX232C.
U74	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U75	19A703483P321	Hex Schmitt Trigger Inverter CMOS; sim to 74HC14.
U76	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74
U78 and U79	**344A3070P3**	LINEAR, JFET Input Operational Amp; sim to TL074.
U81 thru U83	344A3070P3	LINEAR, JFET Input Operational Amp; sim to TL074.
U84 thru U89	19A705180P101	Digital Controlled Potentiometer, 50K ohms.
U90	19A703483P321	Hex Schmitt Trigger Inverter CMOS; sim to 74HC14.
U91	344A3113P101	Analog Switch, Quad SPDT, CMOS; sim to MAX333.
U92	19A705981P101	Hex Schmitt Trigger Inverter CMOS; sim to 74HC14.
U93	19A704125P1	Linear: Quad Comparator; sim to LM339D.
U94	344A3071P1	Optocoupler, Photo Darlington.
U98	19A703483P101	Digital: CMOS Quad 2-Input NOR Gate; sim to 74HC02.
U103	19A703483P104	Digital: CMOS Hex Inverter; sim to 74HC04.
U104	344A3070P3	LINEAR, JFET Input Operational Amp; sim to TL074.

SYMBOL	PART NO.	DESCRIPTION
U105 and U106	344A3113P101	Switch, Analog, Quad SPDT, CMOS; sim to MAX333.
U107 thru U109	19A704125P1	Linear: Quad Comparator; sim to LM339D.
U110 and U111	19A703483P321	Hex Schmitt Trigger Inverter CMOS; sim to 74HC14.
		-------- VOLTAGE REGULATORS -------
VR1	19A700083P108	Silicon, Zener: 15 Volt; sim to BZX84-C15.
VR2	19A700083P110	Silicon, Zener: 22 Volt; sim to BZX84-C22.
VR3	19A700083P108	Silicon, Zener: 15 Volt; sim to BZX84-C15.
VR4	19A700083P110	Silicon, Zener: 22 Volt; sim to BZX84-C22.
VR5	19A700083P108	Silicon, Zener: 15 Volt; sim to BZX84-C15.
VR6	19A700083P110	Silicon, Zener: 22 Volt; sim to BZX84-C22.
VR7	19A700083P108	Silicon, Zener: 15 Volt; sim to BZX84-C15.
VR8	19A700083P110	Silicon, Zener: 22 Volt; sim to BZX84-C22.
VR9 thru VR24	19A700083P104	Silicon, Zener: 7 Volt; sim to BZX84-C648.
		---------- FUSE SOCKETS --------
XF1 thru XF8	19A116688P2	CLIP, FUSE: sim to Littlefuse 111501.
		---------- SOCKETS ----------
XU7	344A3339P5	PLCC, SMT: sim to AMP 822070-4.
XU13	19A700156P3	Socket, IC: 28 Pins, Tin Plated.
		---------- CRYSTALS ---------
Y1	19A702511G37	Crystal Unit, Quartz: 14.7456 MHz.

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter" which is stamped after the model number of the unit. the revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

REV. A - CONVENTIONAL INTERFACE BOARD 19D903324P1
Incorporated in initial shipments.

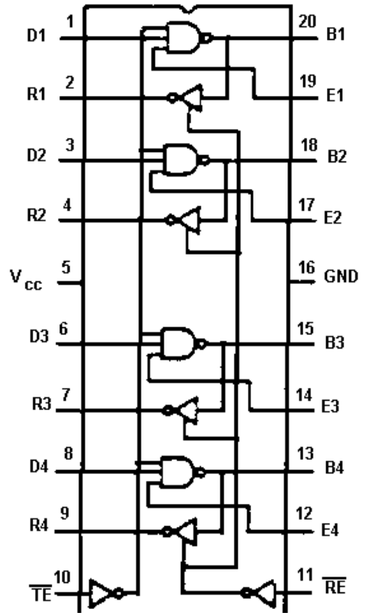
REV. B - CONVENTIONAL INTERFACE BOARD 19D903324P1
Shorten VOX release time.
R159, R251, R252 AND R253 were 470K ohms (19B800607P474).

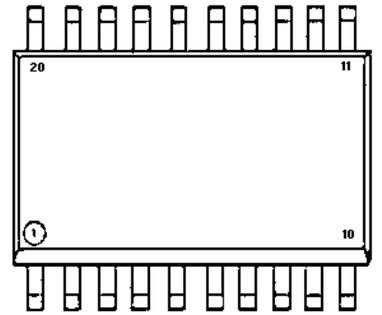
REV. C - CONVENTIONAL INTERFACE BOARD 19D903324P1
Correct low frequency attenuation in audio path from trunked audio board to conventional station.
C91, C98, C105 and C110 were 0.01µF (19A702052P14).

REV. D - CONVENTIONAL INTERFACE BOARD 19D903324P1
Correct error in Parts List.
U13 (19A705551P3) blank PROM removed.

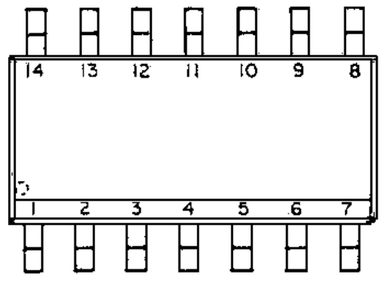
REV. E - CONVENTIONAL INTERFACE BOARD 19D903324P1
Correct failures in constant DC current generator.
U43, U45, U49 and U53 were 19A701766P1.
Q23 thru Q26 were 19A705953P1.

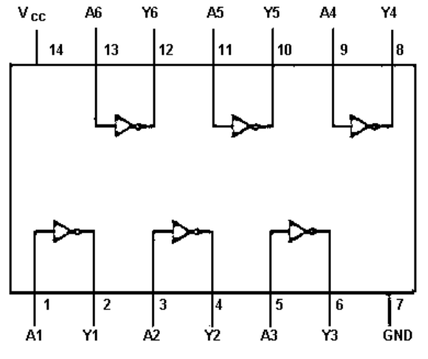
4 Channel Transceiver U1
19A149953P202



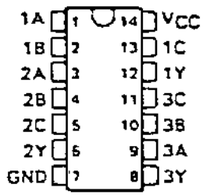


Hex Inverter U2, U4, U103
19A703483P104





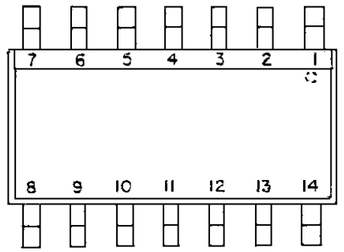
Triple 3-Input NAND Gate U3
19A703483P306



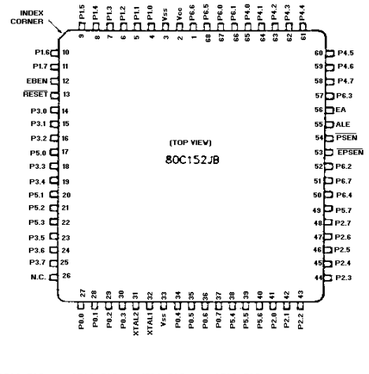
FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

CMOS dual D Flip-Flop W/Set-Reset U6, U17, U25, U74, U76
19A703483P302

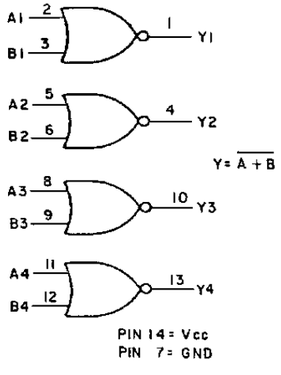


Microcontroller U7
19A705982P101



Quad 2 Input NOR Gate U5, U21, U98
19A703483P101

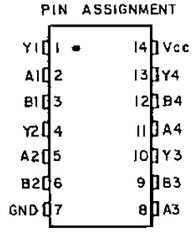
LOGIC DIAGRAM



$Y = \overline{A + B}$

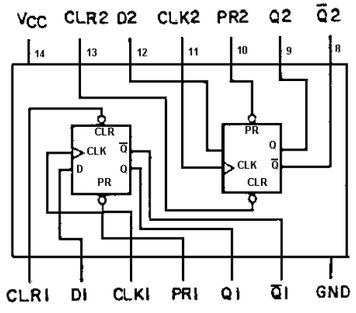
PIN 14 = Vcc
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION DIAGRAM

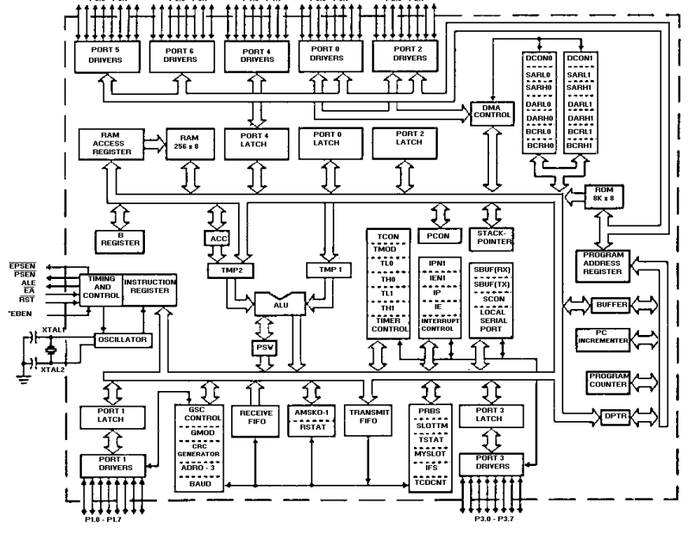
INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L



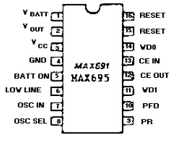
Inputs				Outputs	
PR	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	Q̄0

Note: Q0 = the level of Q before the indicated input conditions were established

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

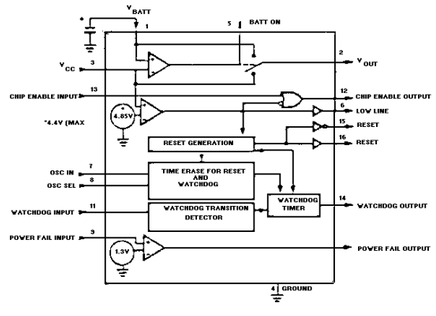


Supervisory Circuit U8



TOP VIEW

BLOCK DIAG.

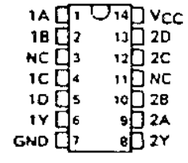


FUNCTION TABLE

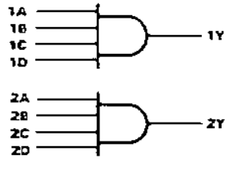
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

Two 4-Input AND Gates U10
19A703483P320

PIN IDENTIFICATION

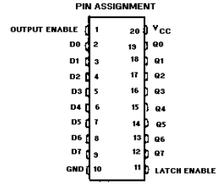


LOGIC DIAGRAM



Octal 3-State Non-Inverting Trans Latch U12
19A703472P318

PIN ASSIGNMENT

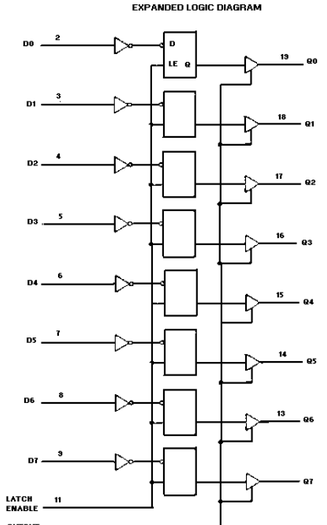


FUNCTION TABLE

INPUTS			OUTPUT
OUTPUT ENABLE	LATCH ENABLE	D	Q
L	H	H	H
L	H	L	L
L	L	X	NO CHARGE
H	X	X	Z

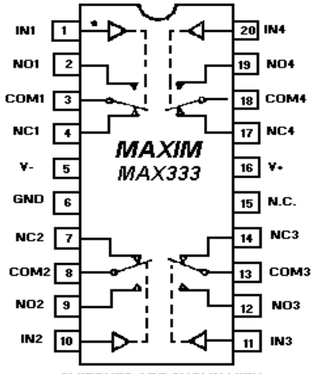
X = don't care
Z = high impedance

EXPANDED LOGIC DIAGRAM

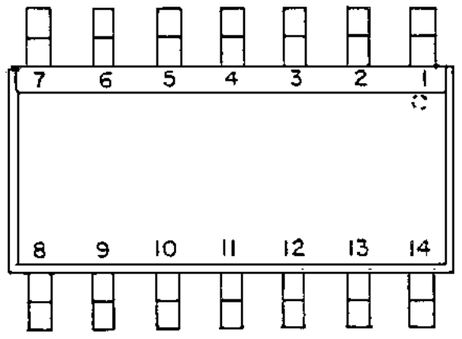


Quad SPST Analog Switch U9, U105, U106

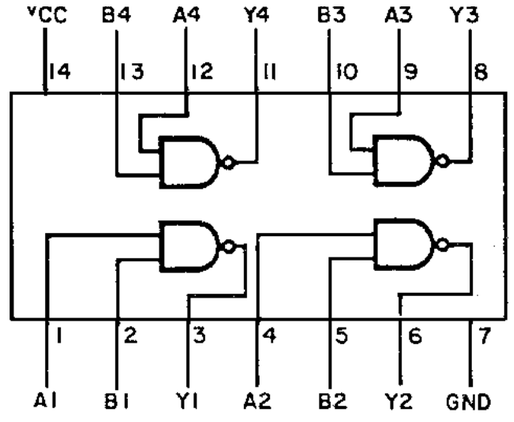
PIN CONFIGURATION



SWITCHES ARE SHOWN WITH LOGICAL 0 INPUT

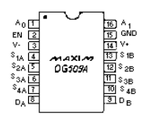


Quad 2-Input NAND Gates U11
19A703483P302

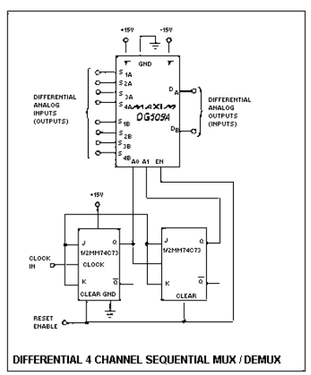


Analog Multiplexer U14, U15
344A3171P1

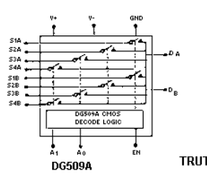
PIN INDENTIFICATION



TYPICAL OPERATING CIRCUIT



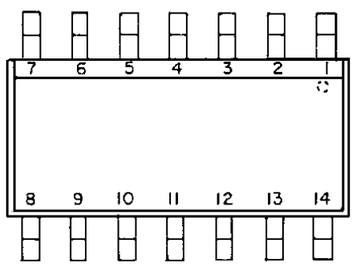
FUNCTIONAL DIAGRAM

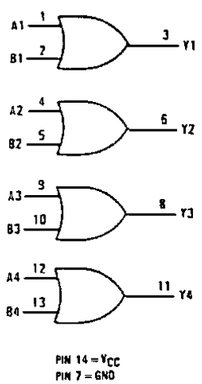


TRUTH TABLE

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

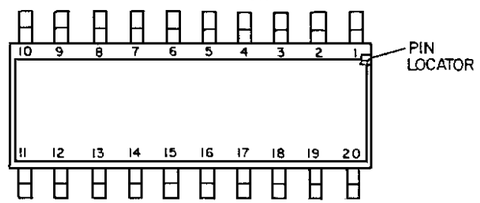
Quad 2-Input OR U19
19A703483P111

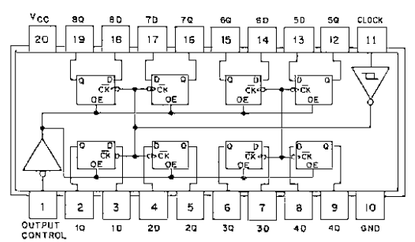




Octal 3-State D Flip-Flop U22, U61
19A704380P112

PIN CONFIGURATION





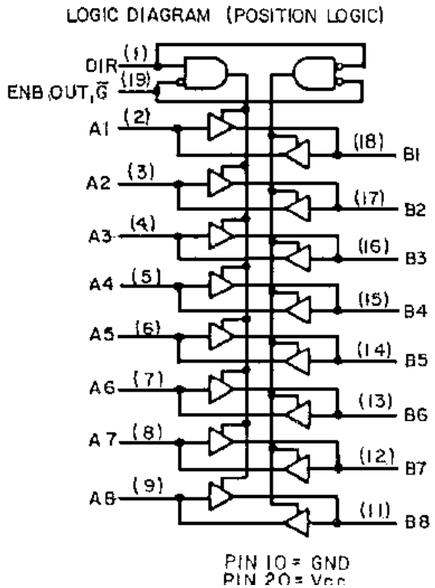
TRUTH TABLE

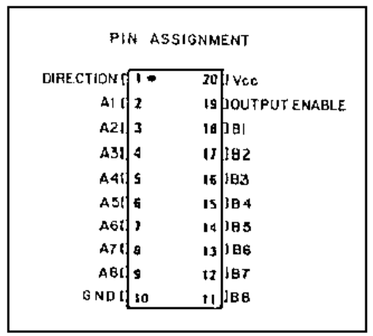
OUTPUT CONTROL	CLOCK	DATA	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = HIGH LEVEL, L = LOW LEVEL
X = DON'T CARE
↑ = TRANSITION FROM LOW-TO-HIGH
Z = HIGH IMPEDANCE STATE
Q_0 = THE LEVEL OF THE OUTPUT BEFORE STEADY STATE INPUT CONDITIONS WERE ESTABLISHED.

Octal 3-State Non-Inverting Bus Transceiver U18
19A703471P308

LOGIC DIAGRAM (POSITION LOGIC)





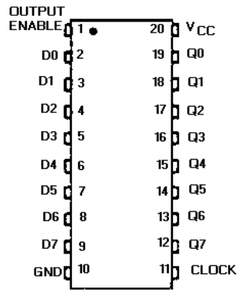
FUNCTION TABLE

CONTROL INPUTS		OPERATION
OUTPUT ENABLE	DIRECTION	
L	L	DATA TRANSMITTED FROM BUS B TO BUS A
L	H	DATA TRANSMITTED FROM BUS A TO BUS B
H	X	BUSES ISOLATOR (HIGH IMPEDANCE STATE)

X = DON'T CARE

CMOS Octal 3-State Inverting Dual Flip-Flop U20
19A704380P315

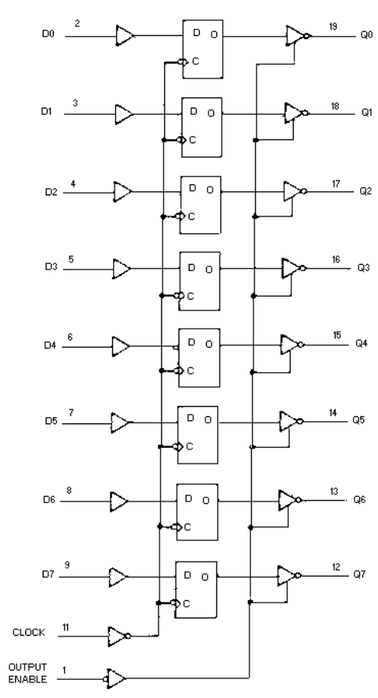
PIN ASSIGNMENT



FUNCTION TABLE

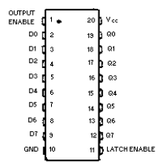
INPUTS			OUTPUT
OUTPUT ENABLE	CLOCK	D	Q
L	↑	H	L
L	↑	L	H
L	L,H,	X	no change
H	X	X	Z

X = don't care
Z = high impedance



Octal 3-State Non-Inverting Buffer U23
19A703471P318

PIN ASSIGNMENT

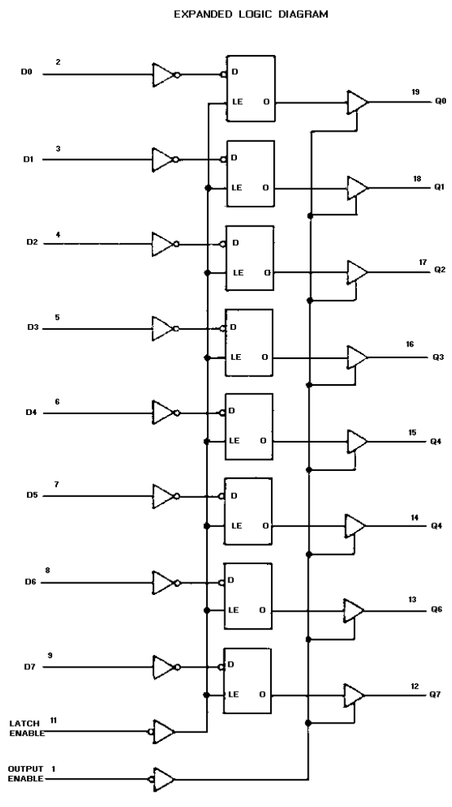


FUNCTION TABLE

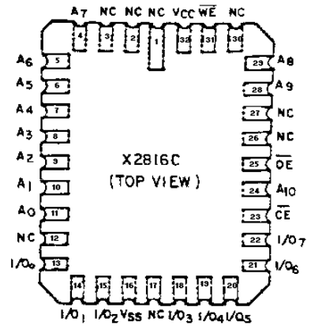
INPUTS			OUTPUT
OUTPUT ENABLE	LATCH ENABLE	D	Q
L	H	H	H
L	H	L	L
L	L	X	NO CHARGE
H	X	X	Z

X = don't care
Z = high impedance

EXPANDED LOGIC DIAGRAM

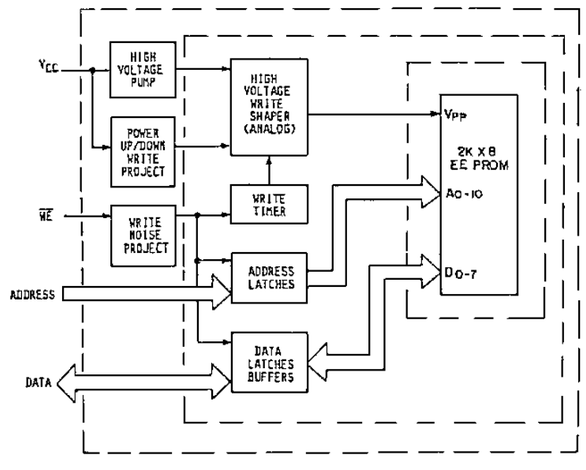


CMOS 2K X 8 EEPROM U26
19A703952P102

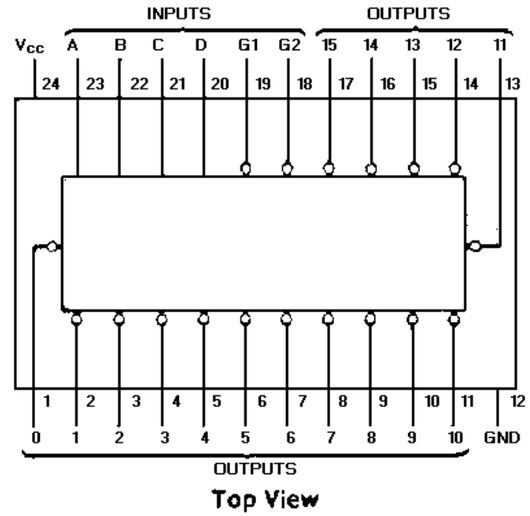


PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
I/O_0-I/O_7	DATA INPUTS/OUTPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
V_{CC}	+5V
V_{SS}	GROUND
NC	NO CONNECT

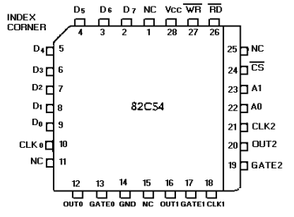


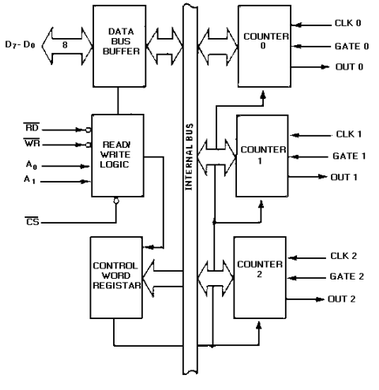
4 To 16 Decoder/Demux U27
19A703471P326



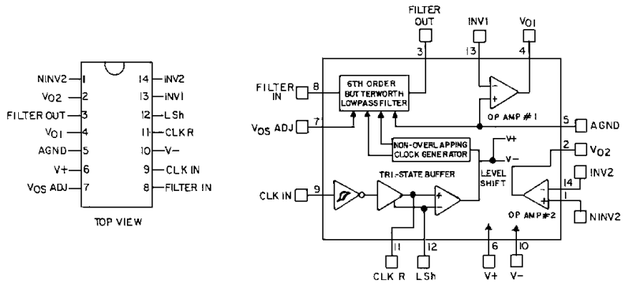
Top View

Programmable Interface Timer U28
19A149466P301

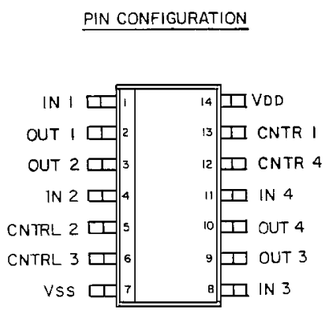


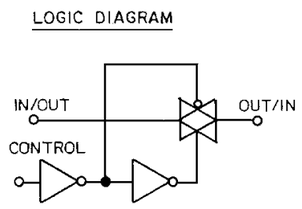


Switch Capacitor Lowpass Filter U29, U37, U38, U39
344A3125P1



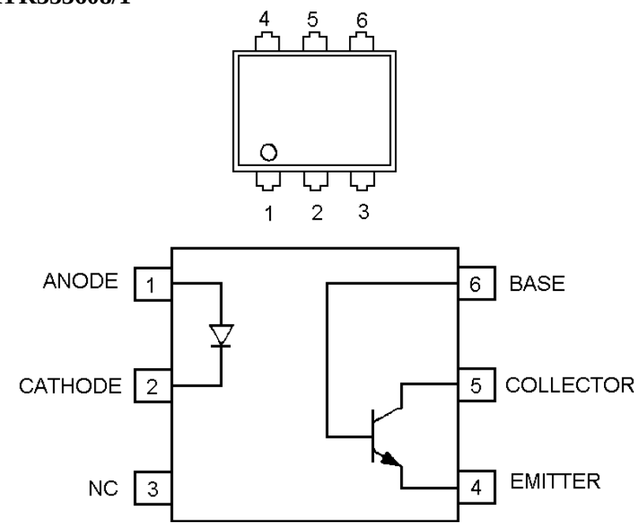
CMOS Bilateral Switch/Multiplexer U30, U31
19A702705P1



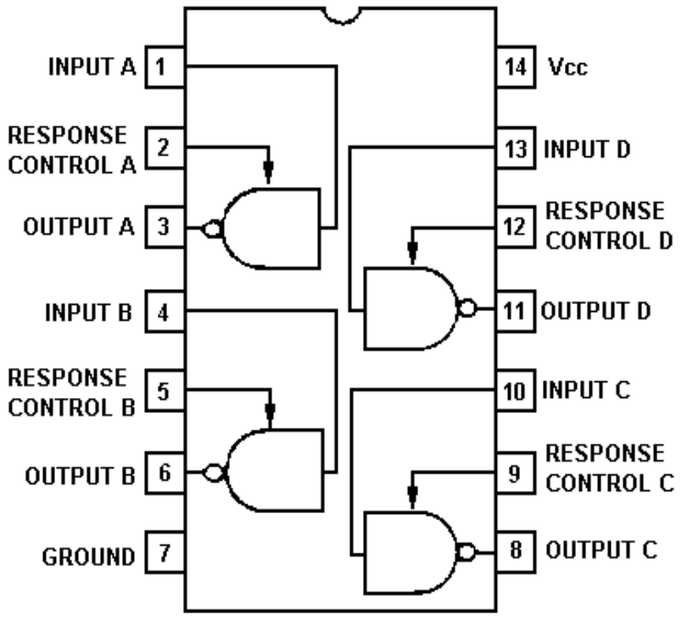


CONTROL	SWITCH
0	OFF
1	ON

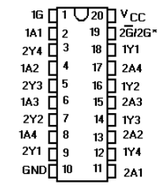
Opto Coupler U40, U41, U42, U46, U47, U48, U50,U51, U52, U54, U55, U56
19A701766P1
U43, U45, U49, U53
RYR353608/1



Quad DTL Line Receiver RS-232C U57
19A116704P2

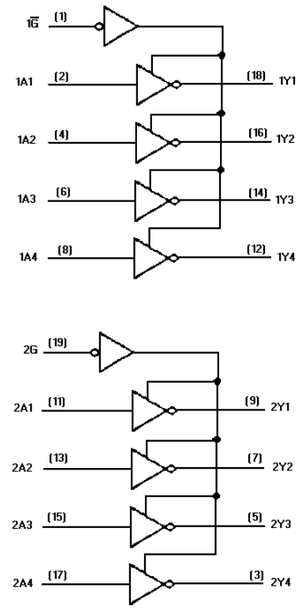


Octal Buffers and Line Drivers U58
19A703471P325



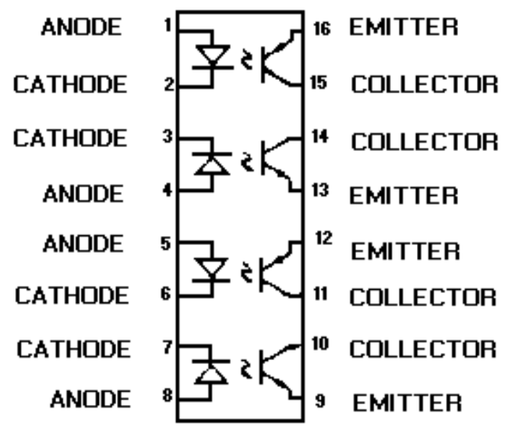
FUNCTION TABLE
(EACH BUFFER)

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	L
L	L	H
H	X	Z



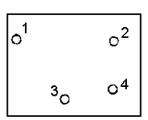
Opto Coupler U59, U60
344A3071P1

TOP VIEW



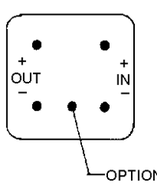
LED CHIPS ON PINS 2, 3, 6, 7
PT CHIPS ON PINS 10, 11, 14, 15

DC - DC Converter U65, U66, U67, U68
344A3220P2



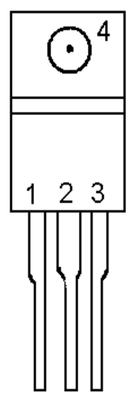
1 Vin (+)
2 Vout (+)
3 Vin (−)
4 Vout (−)

Vin = 5 VDC
Vout = 150 VDC



Vin = 12 VDC
Vout = 150 VDC @ 10mA

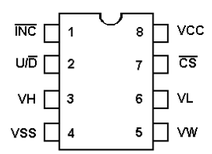
Voltage Regulator U64
19A134717P2



1. INPUT
2. COMMON
3. OUTPUT
4. TAB COMMON

EEPOT U71, U72
19A705180P101

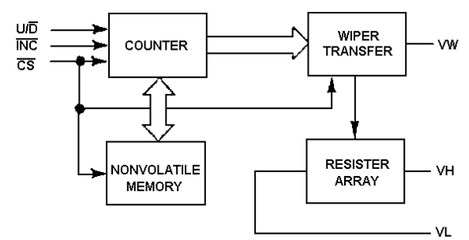
PIN CONFIGURATION



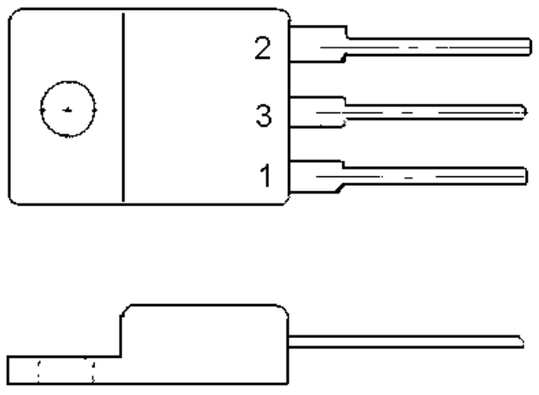
PIN NAME

VH	HIGH TERMINAL OF POT
VW	WIPER TERMINAL OF POT
VL	LOW TERMINAL OF POT
VSS	GROUND
VCC	SYSTEM POWER
U/D	UP / DOWN CONTROL
INC	WIPER MOVEMENT CONTROL
CS	CHIP SELECT

FUNCTIONAL DIAGRAM

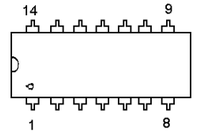


Voltage Regulator U62, U63
19A134718P1

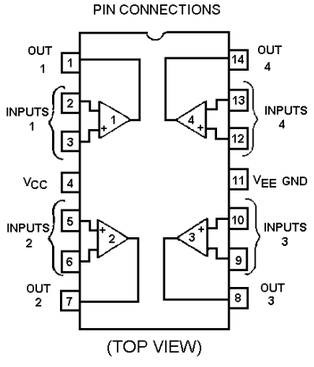


1. COMMON
2. OUTPUT
3. INPUT

Operational Amplifier
U69, U70, U78, U79, U81, U82, U83, U104
344A3070P3

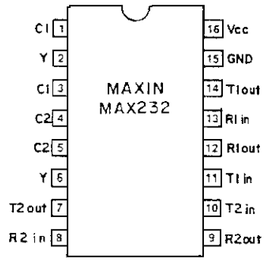


PIN CONNECTIONS

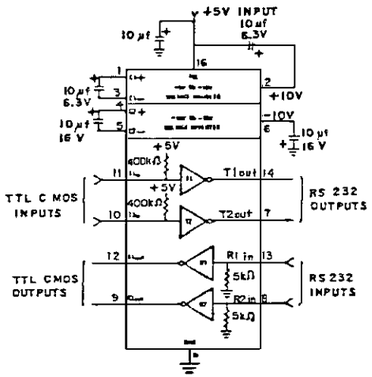


(TOP VIEW)

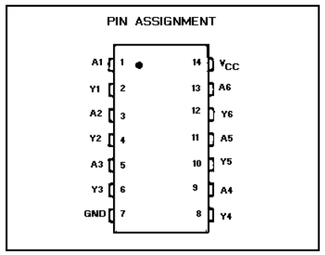
PIN IDENTIFICATION

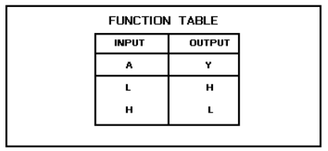


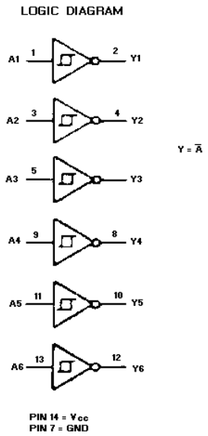
Transmitter/Receiver (RS-232) U73
19A149446P2



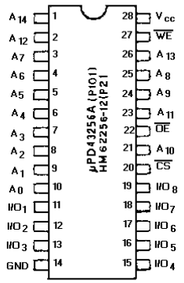
Hex Schmitt Trigger Inverters U75, U90
19A703483P321

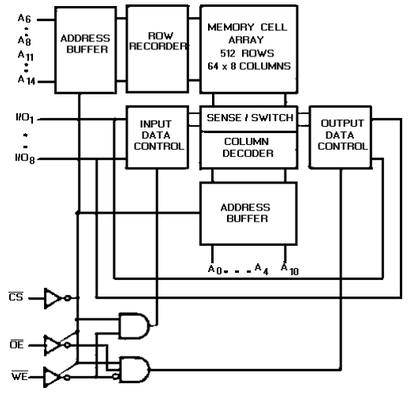




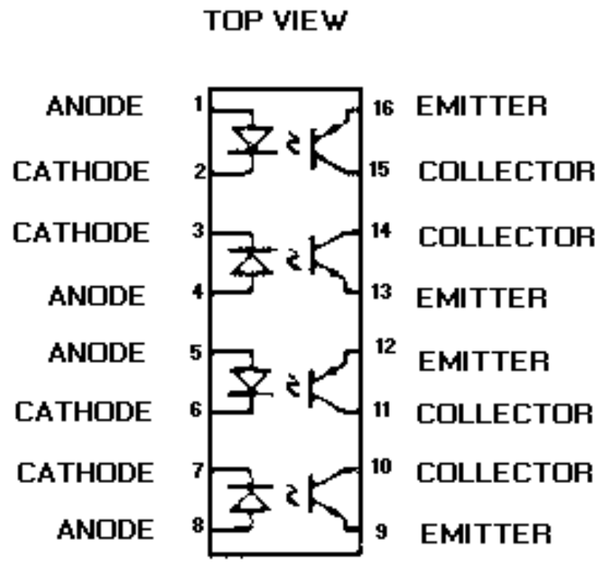


Static RAM U92
19A705981P101



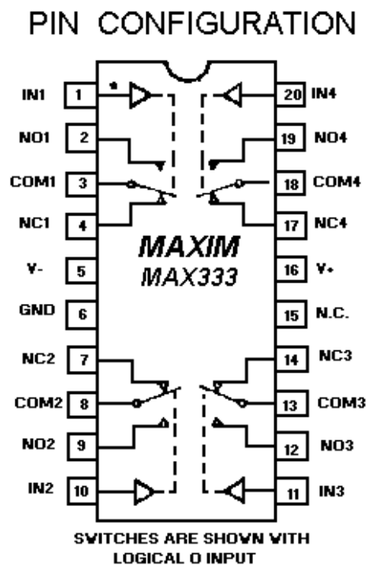


Opto Coupler U94
344A3071P1

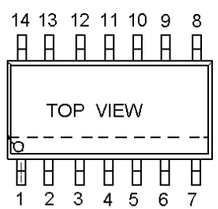


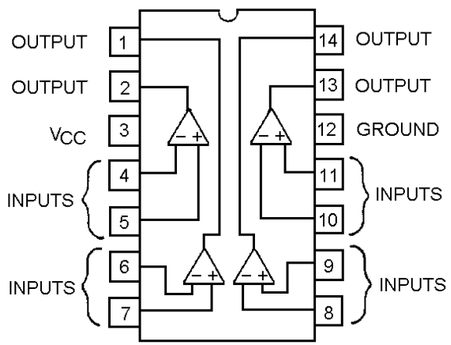
LED CHIPS ON PINS 2, 3, 6, 7
PT CHIPS ON PINS 10, 11, 14, 15

Quad Analog SPDT Switch U91
344A3113P101



Comparator U93, U107, U108, U109
19A704125P1





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