MAINTENANCE MANUAL

TIMING INTERFACE MODULE ROA1172209

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DESCRIPTION

The Timing Interface Module is used in simulcast systems to route the clock reference signals from the multiplexer to the Universal Synchronizer Shelf and then to the digital cross connects at the Control Point or to the transmit cross connects at the Transmit Site. Refer to Figure 1.

The Timing Interface Module will accept up to 30 clock reference inputs from the multiplexer at the Transmit Site, or three reference clock inputs from each of up to 10 sites at the Control Point. The clocks are routed from J4T at the Transmit Site mux cross connect panel to J3 of the Timing Interface Module. As shown on the schematic diagram, these signals are received on pins 1 through 15 and 26 through 40 of J3. The input reference signals are labeled SE21N1 through SE21N30. They are routed through J1 of the Timing Interface Module to P12 of the Universal Sync. Shelf and then to Digital Selector Module #2 in slot 12. One of these signals is selected and returned to the Timing Interface Module on pins 43 through 47 of J1. The selected signal is designated SEL2OUT A through SEL2OUT E and routed to the transmit cross connect connector (J43) at the Transmit Site or to J78 on the Digital Cross Connect at the Control Point.

At the Control Point, reference clocks associated with channels 1, 2, & 6 from each site are fed into the Timing Concentrator Module via jacks J11 through J20. The Timing Concentrator module is capable of receiving up to 30 inputs - 3 from each of 10 sites. These reference clocks are merged and fed from J1 of the Timing Concentrator Module to J3 of the Timing Interface Module. Refer to Figure 2.

At the Transmitter Sites, one clock is associated with each data channel, in groups of 5 for a maximum of 30 reference clocks. These clocks are routed directly to the Timing Interface Module.

PARTS IDENTIFICATION

J1, J2 - RPV403143/50 - Connector, P.W. Header, 50 pin.

J3 - RNT403237/50 - Connector, P.W. Champs, 50 pin.



Figure 1. Timing Interface Module Interconnect, Transmit Site

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Figure 2. Timing Interface Module Interconnect, Control Point



Outline Diagram

Timing Interface Module (ROA1172209)

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X-CONN J4) TX ENTRATOR J2) CP	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	13 210
J3 (TO M1UX) (TO CONCE	$\begin{array}{c} J_{3} > 1 \\ J_{3} > 2 \\ J_{3} > 2 \\ J_{3} > 2 \\ J_{3} > 2 \\ J_{3} > 4 \\ J_{3} > 5 \\ SE21N1 \\ J_{3} > 4 \\ J_{3} > 5 \\ SE21N1 \\ J_{3} > 1 \\ J_{3} > 2 \\ J_{3}$	

3) TX 3)-CP	2 -2 12 6 12 6 12 10 12 12 12 14 12 16 12 16 12 16 12 16 12 -26 12 -28 12 -28 12 -28 12 -28 12 -34 12 -36 12 -36 12 -36 12 -36 12 -36 12 -36 12 -36 12 -36 12 -36 12 -36 12 -36 12 -36 12 -36 12 -36 12 -36 12 -36 12 -36 12 -46
J2(TO J4 (TO J7	1 1 1

J1 <u>-2</u> SE21N2 J1 <u>-4</u> SE21N4	J1 -6 SE21N6 م	J1 - ⁰ S E21N8 SE21N10	J1 12 SE21N12	J1 14 SE21N14	_{J1} — ¹⁶ — SE21N16	_{J1} — ¹⁸ — SE21N18	J1 ²⁰ SE21N20	J1-22 SE21N22	J1 24 SE21N24	J1 26 SE21N26	J1 28 SE21N28	J1 <u>30</u> SE21N30	J1 <u>32</u>	J1 _34	J1 _36	J1 <u>38</u>	J1 <u>40</u>	J1 <u>42</u>	J1 _4SEL2OUTE	_{J1} — <u>48</u> SEL2OUTE 48		
л -1 SE21N1 л 3 SE21N3	J1 - 5 SE21N5	л- <u>-'</u> SE21N7 119SE21N9	<mark>л 11 SE21N11</mark>	J1 <mark>11 13 SE21N13</mark>	_{یا} 15 SE21N15	_{J1} — ^{1/} — SE21N17	_л ¹⁹ SE21N19	J1_21SE21N21	J1 23 SE21N23	J1 <u>25</u> SE21N25	J1 <u>27</u> SE21N27	J1 <u>29</u> SE21N29	л 31	<mark>л 33</mark>	л 35	л <u>37</u>	J1 <u>39</u>	J1 <u>41</u>	J1 43 SEL20UTA	и — <u>*/ </u>	л <u>— — — </u>	

J1 (TO P12)

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