MAINTENANCE MANUAL

AUDIO SYSTEM BOARD
P29/7720037000 (350A1371P20)

TABLE OF CONTENTS

TABLE OF CONTENTS

CIRCUIT ANALYSIS

The Audio System Board is the heart of the Enhanced Audio Enclosure. It accommodates all audio and logical processing circuitry for the Enhanced Audio Enclosure. Primary circuits include:

- **Audio Input Circuits** – These circuits provide amplification, filtering and level-adjustment for all audio signals applied to the Enhanced Audio Enclosure's audio inputs. Input signals include mic audio signals, balanced-line audio signals from the CEC/IMC, balanced-line audio signals from Call Director patch equipment, and audio signals from a pager (or similar device).

- **Audio Switching Matrix Circuits** – The audio switching matrix routes or switches conditioned (amplified, filtered, level-adjusted) input audio signals to the appropriate audio output circuits. This matrix consists of ten (10) "cross-point switch" integrated circuits or "chips" which each have an 8 x 8 switch matrix. All console audio signals are routed through the matrix chips. Input audio signals are applied to the "x" side of the matrix and output signals are sent out from the "y" side. Audio matrix and all other logical circuitry on this board is controlled by the on-board microcontroller circuits.

- **Audio Output Circuits** – Prior to application to the appropriate Enhanced Audio Enclosure output, each audio signal on the output side of the audio matrix (a switched-in signal) is applied to an audio output circuit. Each audio output circuit provides amplification/attenuation, impedance matching and/or level-adjustment in the output path. Output paths include headset earphone audio, low-power speaker audio ("select" and "unselect" audio), balanced-line audio signals to the CEC/IMC, balanced-line audio signals to Call Director patch equipment, and single-ended audio signals to call-check recorders.

- **Digital Potentiometer Circuits** – Digital pots are incorporated throughout the audio input and audio output circuits on the Audio System Board. There are no mechanical pots. All audio levels are 100% adjustable from Personal Computer via the serial data link and the microcontroller circuits on the Audio System Board.

- **Microcontroller Circuits** – Intel 80C32-based microcontroller circuits on the Audio System Board control and process all logical data signals to and from the Audio System Board's I/O logic circuits. These circuits include (non-inclusive listing) the audio switching matrix, several serial ports, digital pots, bi-state logical inputs, and bi-state logical outputs. The microcontroller circuits also read the on-board analog-to-digital converter circuits to provide VU meter data to the PC.

- **PC Serial Port Circuit** – An RS-232 port for control data communication with the Personal Computer (PC).

- **Dispatch Keyboard Serial Port Circuit** – This serial port receives keystroke data from the Dispatch Keyboard. Operating dc power is also delivered to the Dispatch Keyboard via this serial port.

- **Expansion Serial Port Circuit** – An RS-422 serial port which permits control data interfacing to serially-interfaced external equipment. (Reserved for future use.)

- **Bi-State Logic Input Circuits** – These circuits interface bi-state logical sense lines from external equipment connected to the Enhanced Audio Enclosure to the Audio System Board's microcontroller circuits. Examples include mic PTT sense lines, mic connected/not connected sense lines, Call Director off hook, and Call Director jack sense lines. Each circuit includes a pull-up resistor for the external device and low-pass filtering.

- **Bi-State Logic Output Circuits** – These circuits interface the microcontroller circuits to bi-state logical outputs devices such as relay contacts. The Audio System Board has a total of seven (7) on-board relays.

- **Analog-to-Digital Converter Circuit** – The analog-to-digital (A/D) converter circuit's primary function is to provide VU (Volume Unit) data on various Enhanced Audio Enclosure audio output signal levels. The microcontroller reads the A/D converter. It sends the read data to the PC via the serial control data link. VU indications are displayed within communication modules on the PC's monitor. The A/D converter circuit is also utilized during automated test and alignment procedures.

- **Tone Generator Circuits** – Programmable sinewave generator chips on the Audio System Board give it the ability to generate single-tone and DTMF (Dual-Tone Multi-Frequency) tone signals. Currently, these circuits are not used and they are not supported by firmware.

- **Switching Regulator Power Supply Circuits** – Switching regulator circuits on the Audio System Board convert +12 Vdc power from the Enhanced Audio Enclosure's power supply to regulated ±5 Vdc power. This bipolar power supply feeds all analog and digital circuits on the Audio System Board.

With the Enhanced Audio Enclosure's top cover removed, the Audio System Board slides into and out of the case between two (2) plastic printed circuit board guides attached to the left and right inner sides of the case. Two plastic hinge-type locking tabs located near the front corners of the board hold it in place. These tabs also provide quick board insertion and removal during maintenance procedures. The board's approximate dimensions are 14¼ x 8 inches (36.2 x 20.3 cm).

When fully-inserted, two (2) rectangular 96-pin DIN-type connectors on the Audio System Board mate with 96-pin DIN connectors on the I/O Backplane Board. Specifically, DIN connector J22 on the I/O Backplane Board mates with connector J1 on the Audio System Board and DIN connector J21 on the I/O Backplane Board mates with J2 on the Audio System Board.

SWITCHING VOLTAGE REGULATOR CIRCUITS

Twelve-volt dc power from the power supply unit in the Enhanced Audio Enclosure is applied to the Audio System Board at J2 pins 1 and 23. From these pins, the power (+12V) is applied to the inputs of the two (2) switching voltage regulator circuits on the Audio System Board via an L-C low-pass filter network. [Audio System Board schematic diagram sheets 1 and 7.]

The low-pass filter network is formed by inductor L6 and capacitors C80 & C81. This network feeds filtered dc power to the regulator circuits via the +12VA line. LED1 which is visible through the Enhanced Audio Enclosure's front panel, lights when +12V power is present. As indicated in the POWER TABLE on sheet 1 of the Audio System Board schematic diagram, the filter network also feeds quad op-amp IC U28 at pin 4. [Audio System Board schematic diagram sheets 1, 16 and 21.]

Both voltage regulators on the Audio System Board are switching regulators which are used to generate a dual-polarity or bipolar (positive and negative) ±5 Vdc power supply from the single-polarity +12 Vdc input power (+12V). All op-amps and the sinewave generator ICs are powered by this bipolar supply. In addition, the digital logic circuits are powered from the +5V side. As shown in Figure 1, two output filter circuits are employed at the +5 Vdc regulator's output to provide isolation between the +5 Vdc analog and digital power supply lines. Each regulator circuit employs a Linear Technology LT1076 switching regulator IC (or equivalent) packaged in a 5-lead TO-220 case. These regulators feature a 2-amp maximum output capability, current limiting, and low external support component count. [Audio System Board schematic diagram sheet 7.]

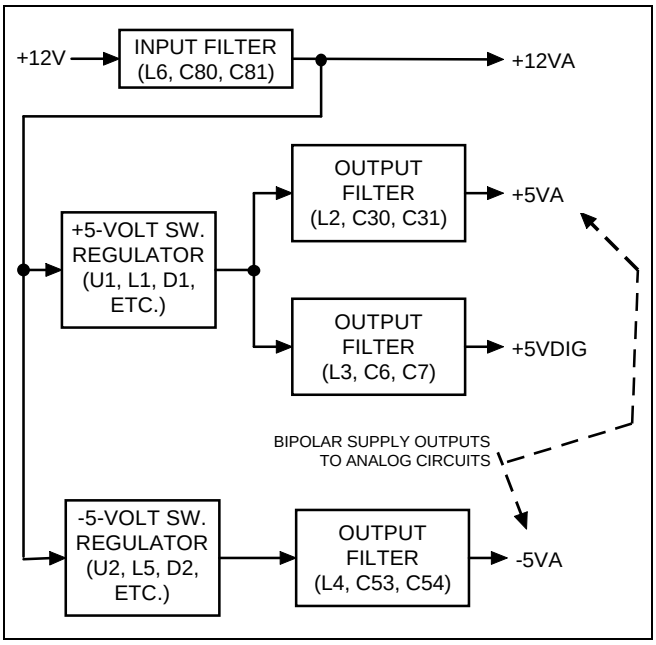


Figure 1 – Audio System Board Power Supplies

+5-Volt Switching Regulator

Integrated circuit U1 and associated components form the +5-volt switching regulator circuit. The +12 Vdc input is located at U1 pin 5. This IC operates in a positive buck converter mode with L1 being the driven inductor and Schottky diode D1 providing a clamp function when U1 turns off. Divider resistors R1, R3 and R4 produce a 2.2 Vdc feedback voltage at U1's feedback input, pin 1. C1, C3 and C5 provide filtering and decoupling functions. [Audio System Board schematic diagram sheet 7.]

The +5 Vdc regulated output from U1 is applied to two separate L-C output filter circuits. L2, C30 and C31 output +5 Vdc filtered supply power for the board's analog circuits (+5VA). This is the positive side of the bipolar power supply. L3, C6 and C7 output +5 Vdc filtered power for the digital circuits (+5VDIG). Digital and analog grounds are isolated starting at these filters. See the POWER TABLE on sheet 1 of the schematic diagram for +5VA and +5VDIG power supply distributions to the integrated circuits.

-5-Volt Switching Regulator

The -5-volt switching regulator is formed by U2 and associated components. This regulator stage converts the positive 12 Vdc input power to -5 Vdc power for use by the op-amps and other analog circuits on the board. As with the +5-volt regulator, 12 Vdc from the power supply (+12V) is applied to pin 5. L5 is the driven inductor and Schottky diode D2 provides clamping when the switching regulator turns off. Divider resistors R5 thru R8 produce a 2.2 Vdc feedback voltage at U2's feedback input. R9 thru R11 and C13 provide frequency compensation. C8 and C9 provide filtering and decoupling at the output and C11 provides decoupling at the regulator's input. [Audio System Board schematic diagram sheet 7.]

The -5 Vdc regulated output power from U2 is applied to an L-C filter network comprised of L4, C53 and C54. This filter circuit outputs the -5 Vdc analog power supply line which is identified as -5VA. This supply line is the negative side of the bipolar power supply. See the POWER TABLE on sheet 1 of the Audio System Board's schematic diagram for -5VA distribution details.

MICROCONTROLLER CIRCUITS

Microcontroller circuits on the Audio System Board perform the following principal functions for the Enhanced Audio Enclosure:

- interfacing to the Personal Computer (PC) via a serial port
- interfacing to the Dispatch Keyboard via a serial port
- microphone PTT sensing for all microphones
- microphone connected/not connected sensing
- cross-point matrix chip switching for the ten (10) on-board cross-point switch chips per PTTs from currently connected microphone(s), messages received from PC, etc.
- frequency control of the two (2) tone generator circuits (currently not used and supported by firmware)
- digital potentiometer setting control
- analog-to-digital (A/D) converter circuit reading
- interfacing to Call Director patch equipment
- output control of the relay outputs
- input control of the digital optocoupler inputs (currently not used and not supported by firmware)

Microcontroller U56

Microcontroller U56 is an Intel® 80C32 (or equivalent) 8-bit microprocessor which provides all processing power for the Audio System Board. Features of this chip utilized in the Enhanced Audio Enclosure include 64K bytes of external program memory storage addressing (ROM), 64K bytes of external data memory storage addressing (RAM; 32K of 64K used), a programmable serial communications port, and 16-bit timers/counters. [Audio System Board schematic diagram sheet 2.]

Specifically, the memory map includes 32K bytes of RAM, 8K bytes of boot ROM (normally only installed for flash applications), and either 64K bytes of one-time programmable ROM (non-flash applications) *or* 56K bytes of flash EEPROM. Firmware is stored in the ROM chip(s). If installed, the boot ROM may either be an 8K or 16K byte chip. Some boards do not use the boot ROM in which case the boot-up code is stored in the one-time programmable ROM.

The 80C32's port usage is detailed in Table 1. These ports provide both memory and I/O interfacing.

Table 1 – 80C32 Microcontroller U56 Port Usage

PORT	USE
0	multiplexed: low address byte output (A0 - A7) and bidirectional data bus (D0 - D7)
1	serial device control (digital pots, EEPROM) and sinewave generator control
2	high address byte output (A8 - A15)
3	single-line I/O control logic lines, serial comm port, interrupts and memory control logic lines

Address Latch U59

As indicated in Table 1, microcontroller U56 incorporates a multiplexed 8-bit wide address and data bus at port 0 (pins 36 – 43). This port transfers both the lower address byte to external memory and 8-bit bidirectional data to and from external memory and I/O devices. Before U56 can read or write data, it must first latch the lower address byte to the Q outputs of octal data latch U59. [Audio System Board schematic diagram sheet 2.]

To latch the lower address byte, U56 first outputs the byte at port 0. It next pulls its ALE (address latch enable) logic line at U56 pin 33 low. The byte remains latched on U59's Q outputs until the external data read or write is completed via port 0, at which time, U56 brings ALE back

to a high state. This sequence repeats upon subsequent memory or I/O reads and writes.

Boot ROM U85 (if installed)

Boot ROM U85 is typically an EPROM chip. If installed, it stores the initialization and other low-level portions of the Audio System Board's operating program such as interrupt jump vectors. The installed chip may be either an 8K x 8-bit (2764 or equivalent) or a 16K x 8-bit (27128 or equivalent) device. U85 is mapped into the 0000 hexadecimal (0 decimal) to 1FFF hexadecimal (8191 decimal) program storage memory range of microcontroller U56 as described in the following paragraph. [Audio System Board schematic diagram sheet 2.]

Fourteen (14) address logic lines (A0 – A13) are applied to U85. With current chip enable decoding logic, address logic line A13 is never used by U85; it is wired to the ROM chip for future memory expansions, if required. Two (2) OR gates (part of U75) generate the BROMCS/ logic line for U85 by "ORing" the three (3) highest address lines (A13 – A15) from the 80C32. BROMCS/ is an active-low boot ROM chip select logic line which enables U85 during boot ROM reads via its active-low chip enable input at pin 23. BROMCS/ is active (low) only when address logic lines A13 thru A15 are all low. This maps the boot ROM into U56's 0000H to 1FFFH (hexadecimal) address space. BROMCS/ is always inactive (high) any time U56 addresses an external memory byte at 2000H or above.

After the address is set during a boot ROM read, microcontroller U56 next pulses its program store enable output (pin 32) low. This enables U85's data bus output buffers via its active-low output enable logic input at U85 pin 25. U56 then reads the boot ROM data byte at the addressed location.

PROM U84

PROM U84 stores the majority of the Audio System Board's operating program (firmware) *or*, in cases where the boot ROM U85 is *not* installed, *all* of the operating program is stored within U84. The installed PROM may either be a one-time programmable ROM chip or, for flash applications, a flash EEPROM. Current firmware does not support flash programming.

In either case, the 64K x 8-bit PROM is mapped into the microcontroller's program storage memory address space from 2000H (8192 decimal) to FFFFH (65,535 decimal). All sixteen (16) address lines are applied to U84 – A0 thru A15. [Audio System Board schematic diagram sheet 2.]

U84 chip selection is accomplished in one of the following methods based upon the installed/not installed status of boot ROM U85:

- If boot ROM U85 is installed, chip selection for U84 is generated by simply inverting the BROMCS/ logic line via an inverter within U73 (pins 1 & 2). In this case, jumper R502 is installed and jumper R503 is *not* installed. The inverted line, FPROMCS/, pulls U85's chip enable input low whenever microcontroller U56 addresses any memory location at 2000H or above.

- In cases where U85 is not installed, jumper R503 is installed and jumper R502 is *not* installed. This pulls U84's active-low chip enable input low at all times.

Microcontroller U56 reads U84 by pulsing its program store enable (PSEN/) logic line low. This microcontroller output is also applied to boot ROM U85 (if installed) and to I/O address decoder U76. [Audio System Board schematic diagram sheets 2 and 6.]

During normal program operations, the EE/RAM* logic line from U56 pin 9 remains low. However, when U84 is flashed programmed, microcontroller U56 pulls EE/RAM* high. EE/RAM* and theactive-low write enable logic line from U56 pin 18 (WR/) are decoded by inverter U73 (pins 3 & 4) and OR gate U75 (pins 8, 9 & 10). The resultant decoded output, FPROMWR*, transitions low when U56 writes a flash byte to U84.

RAM U77

RAM chip U77 provides 32K bytes of volatile static random access memory for the Audio System Board. This chip is mapped into the 0000H (0 decimal) to 7FFFH (32767 decimal) range of microcontroller U56's read/write memory space. Address logic lines A0 thru A14 are applied to U77's address inputs and A15 is tied to its active-low chip select logic line. [Audio System Board schematic diagram sheet 2.]

During normal (non-flash) operations, microcontroller U56 keeps the EE/RAM* logic line at U56 pin 9 low. OR gate U75 (pins 11, 12 & 13) ORs the EE/RAM* logic line with the active-low write enable logic line from U56. The resultant RAMIOWR* logic line is applied to the active-low write enable input of U77 at pin 27. Accordingly, RAMIOWR* pulses low when U56 writes a byte to the RAM.

RAMIOWR* is also used by several memory-mapped I/O chips which are addressed by I/O address decoder U76 and additional OR gates. [Audio System Board schematic diagram sheets 4, 5 and 6.]

During a RAM byte read, U56 pulses its active-low read logic line (pin 19) low. This enables the data bus output buffers within U77 via its output enable logic input line at U77 pin 22. RAMIOWR* remains high during the RAM read.

Counter U74

Integrated circuit U74 is a dual 4-bit binary counter which generates several reference clocks from the microcontroller's 14.7456 MHz clock. U74 pins 4, 5 and 6 output divided-by 4, 8 and 16 clocks respectively. The 3.686 MHz (÷ 4) output is applied to the clock input of serial communications controller U71 and the 1.8432 MHz (÷ 8) output is applied to the clock input of I/O scanner U72. The 921.6 kHz clock (÷ 16) output drives the clock inputs of both sinewave generator chips, U46 & U58. [Audio System Board schematic diagram sheets 2, 3, 5 and 6.]

In addition, the 921.6 kHz clock output is applied to the clock input of the second counter within U74. This second counter's divided-by 16 output at U74 pin 8 is applied back to the microcontroller at U56 pin 16. When required, U56 can read these 57.6 kHz pulses and generate long time delays via software counters. [Audio System Board schematic diagram sheet 2.]

Microcontroller Reset/Watchdog Timer U55

Integrated circuit U55 is a microprocessor supervisory chip that performs power-up reset and "watchdog" timer functions for microcontroller U56. Resets generated by this chip also reset other logic circuitry on the Audio System Board. [Audio System Board schematic diagram sheet 2.]

At power-up, U55 holds its reset output at pin 7 low until approximately 50 milliseconds *after* the +5VDIG power supply line stabilizes. Therefore, via inverter U73 (pins 5 & 6), the RESET logic line is held high for the same time interval. The Audio System Board is in a reset (non-operating) state when RESET is high.

U55 will also reset the microcontroller and other logic circuits on the Audio System Board if the microcontroller fails to periodically pulse U55's watchdog input or if the +5VDIG power supply line falls out of regulation. U55's watchdog input is located at pin 6 and +5VDIG voltage sensing is accomplished via the chip's power pin (U55 pin 2).

If U55 pin 6 remains low or high for more than 1.6 seconds, the watchdog timer will time-out and an active-low reset pulse will appear at U55 pin 7. This produces an active-high reset pulse at the output of inverter U73, the RESET logic line for the entire board. RESET is applied to the microcontroller's reset logic line at U56 pin 10 and to various other logic circuits on the board.

Serial EEPROM U57

Integrated circuit U57 is a serially-accessed EEPROM (Electrically Erasable Programmable Read Only Memory) that provides 128 bytes of non-volatile memory storage for the Audio System Board. In this application, its stores data such as digital pot settings and other initialization values required at board power-up. [Audio System Board schematic diagram sheet 3.]

Microcontroller U56 writes data to and reads data from U57 using the SCLK (serial clock), SDATA (serial data) and EEPROM_CS (EEPROM chip select) logic lines. These lines are located between U56's port 1 and U57's serial I/O pins. SDATA is a bidirectional data logic line and SCLK provides clock pulses for the synchronous serial data transfers. EEPROM_CS basically provides a strobe-type function before and after data activity on SDATA. [Audio System Board schematic diagram sheets 2 and 3.]

SCLK and SDATA are also used to load frequency data into the sinewave generator chips and pot settings into the digital pots. These processes are described in subsequent sections of this manual.

LOGIC INTERFACE CIRCUITS

PTT And Sense Inputs

Eleven (11) identical logic input buffers circuits are located on the Audio System Board. Each circuit interfaces a PTT or sense logic line from the rear panel of the Enhanced Audio Enclosure into the Audio System Board's microcontroller circuits. PTT buffers are shown on sheet 28 of the schematic diagram and sense buffers are shown on sheet 29. A logic input line becomes active when it is pulled low by an external device. For example, DESK_MIC_PTT_IN (J2 pin 42) is pulled low by the switch in the desk mic when the desk mic's PTT button is depressed. Sense logic lines provide connected/not status for the headsets, microphones. In addition, two (2) sense inputs are used for Call Director patch status interfacing.

Enhanced Audio Enclosure PTT and sense inputs originate from the connectors at the rear panel. All are routed through the I/O Backplane Board to Audio System Board connector J2. J2 is a 96-pin rectangular DIN connector that mates with I/O Backplane Board connector J21. The I/O Backplane Board contains no active or passive components, only connectors.

On the Audio System Board, each logic input buffer circuit consists of a pull-up resistor, an R-C low-pass filter network, a surge suppression diode and an Schmitt trigger

inverter. Each low-pass network provides a switch contact debounce function for its input. It also prevents induced charges such as static electricity from falsely triggering the input. Buffer circuit input and output schematic diagram labeling is given in Table 2.

The Schmitt triggers are located within hex inverters U45 (PTT inputs) and U4 (sense inputs). All eleven (11) inverter outputs are applied to the microcontroller's input scanning circuitry described in the following section. [Audio System Board schematic diagram sheet 5.]

Input Scanning

Integrated circuit U72 is an Intel® 8279 (or equivalent) keyboard/display interface chip. In the Enhanced Audio Enclosure, this chip is used only for input scanning functions. It scans a total of nineteen (19) Enhanced Audio Enclosure logic inputs. When a logic change occurs in one, it interrupts microcontroller U56 so the change can be read by U56. At power-up, microcontroller U56 programs U72 to operate in an 8279 "scanned sensor matrix mode". [Audio System Board schematic diagram sheet 5.]

Scanned inputs include the six (6) PTT logic inputs from the mics, the three (3) mic sense (connected/not connected) logic lines, two (2) Call Director sense logic lines (jack sense and on-hook sense), and eight (8) digital input logic lines from on-board optocouplers. PTT and sense inputs originate from the buffer circuits described in the previous section. [Audio System Board schematic diagram sheets 5, 24, 25, 28 and 29.]

No debounce operations are performed by U72. This function is accomplished via the R-C and Schmitt trigger networks on the input lines as previously described.

U72 scans the inputs by sequentially reading three-state octal buffers U43, U70 and U54. This is accomplished using scan logic line outputs SL1 thru SL3 from U72 to sequentially strobe each octal buffer. The scan rate is 102.4 kHz or approximately 10 microseconds between scan logic line toggles. [Audio System Board schematic diagram sheet 5.]

For example, to read the eight digital input logic lines from the optocouplers, U72 pulls its SL1 output low and all other SL outputs high. This enables U43. When enabled, U43's eight output buffers drive U72's eight return logic line row inputs identified as RL0 thru RL7. Since the SL2 and SL3 outputs are high, all U70 and U54 buffer outputs remain in a high-impedance state. Next, U72 stores the logic state of each return logic line in an internal register so it can be read by microcontroller U56 if a change has occurred since the previous read. Approximately 10 microseconds later, scan logic line SL1 transitions high, disabling U43, and SL2 transitions low so U70's PTT and sense input logic lines can be read.

When a change occurs in one or more inputs, U72 pin

Table 2 - PTT And Sense Inputs*

FROM I/O BACKPLANE BOARD	J2 & J21 PIN	INPUT NAME - FROM I/O BACKPLANE BOARD (Active Low)	BUFFERED NAME (Active High)	USE
J7 pin 6	41	SUPR_PTT_IN	SUPR_PTT	Supervisor Headset PTT Input
J6 pin 6	45	OPR_PTT_IN	OPR_PTT	Operator Headset PTT Input
J5 pin 6	42	DESK_MIC_PTT_IN	DESK_MIC_PTT	Desk Mic PTT Input
J4 pin 6	43	B/G_PTT_IN	B/G_PTT	Boom/Gooseneck Mic PTT Input
J2 pin 3	40	PAGER_PTT_IN	PAGER_PTT	Pager PTT (Enable) Input
J14 & J15 pins 4, J5 pin 3	44	MONITOR_PTT_IN	MONITOR_PTT	Monitor Switch/Button
J7 pin 3	74	SUPR_JACK_SENSE_IN	SUPR_JACK_SENSE	Supervisor Headset Jack Box Sense Input
J6 pin 3	76	OPR_JACK_SENSE_IN	OPR_JACK_SENSE	Operator Headset Jack Box Sense Input
J3 pin 3	75	CD_JACK_SENSE_IN	CD_JACK_SENSE	Call Director Handset Jack Sense Input
J3 pin 2	71	CD_HOOK_SENSE_IN	CD_HOOK_SENSE	Call Director Off-Hook Sense Input
J4 pin 3	72	B/G_MIC_SENSE_IN	B/G_MIC_SENSE	Boom/Gooseneck Mic Sense Input

* Refer to Audio System Board schematic diagram sheets 28 and 29.

4 transitions high. This pulls the interrupt logic line to microcontroller U56 identified as KEYINTR* low via inverter U73 (pins 8 & 9). Upon being interrupted via the KEYINTR* pulse, U56 reads U72 to determine which input(s) has changed.

Control inputs from U56 to U72 include the active-low read logic line (RD/), the active-low RAM or I/O write logic line (RAMIOWR*) and a chip select logic line (8279CS*). In addition, U72 is reset at power-up by RESET (high = reset) from microprocessor supervisory chip U55. [Audio System Board schematic diagram sheets 2 and 5.]

RS-232 Dispatch Keyboard Serial Port

Integrated circuit U44 and the associated components perform TTL-to-RS-232 conversions between the microcontroller's TTL-level serial port and the Dispatch Keyboard's RS-232 serial port. This keyboard is sometimes referred to as the "Custom Keyboard". Connector J18, shown within dotted lines on the schematic, is the DB-9 connector located at the rear panel of the Enhanced Audio Enclosure. The keyboard plugs to this connector. J18 is a connector on the I/O Backplane Board. RS-232 serial keyboard data received from the keyboard is present on J18 pin 2. The transmit line to the Dispatch Keyboard (J18 pin 3) is not used with current keyboard hardware. [Audio System Board schematic diagram sheet 5.]

When a key on the keyboard is pressed, RS-232 serial data from the keyboard is applied J18 pin 2. This signal is routed through the I/O Backplane Board and applied to J2 pin 38 on the Audio System Board. Inductor L7 couples the signal, RX_DATA_KEYBOARD_IN, to U44 pin 13 for RS-232-to-TTL conversion. A suppressor within transient voltage suppressor TVS9 provides surge suppression from induced charges such as static electricity. The level-converted data (TTL-level) is sent to microcontroller U56's serial port input at U56 pin 11 via the RX_DATA_KEYBOARD line.

TX_DATA_KEYBOARD at U44 pin 11 is the TTL-level keyboard transmit output serial data from the microcontroller's serial port (U56 pin 13). As previously stated, this output is not used with current keyboard hardware. However, if used in the future, data on this transmit logic line to the keyboard could include keyboard control codes such as keyboard buffer clear codes. U44 converts this TTL-level data to ±10-volt RS-232-level data. The RS-232 output is pin 14. Inductor L8 couples the signal to J2 pin 39, identified as TX_KEYBOARD_DATA_OUT. As shown on the Audio System Board schematic diagram, J2 pin 39 is connected to J18 pin 3 on the I/O Backplane Board. A suppressor within transient voltage suppressor TVS9 provides surge suppression.

Integrated circuit U44 has a built-in +5-volt to ±10-volt charge pump converter; therefore, it only requires power from the +5VDIG supply to generate positive and negative RS-232 voltages. Capacitors C211 thru C213 are the chip's charge-pump capacitors. The ±10-volt supplies are used by the chip's RS-232 TX drivers, only one of which is wired for use.

Keyboard operating power is applied to J2 pin 34 and routed through the I/O Backplane Board to J18 pin 1 at the Enhanced Audio Enclosure's rear panel. Thermistor F1 provides an automatic resettable fuse function. In some cases, this component is not installed and as noted on the schematic, R12 is substituted.

Serial Communications Controller U71

Integrated circuit U71 is an Intel 82530 (or equivalent) Serial Communications Controller (SCC) chip. It provides two (2) additional serial ports for the Enhanced Audio Enclosure. One port – port A – is used for RS-232 serial interfacing to the PC (Personal Computer). The other – port B – provides an RS-422 serial port for expansion capability. U71 is addressed by microcontroller U56 as a part of U56's memory mapped I/O. [Audio System Board schematic diagram sheet 6.]

Drivers/receivers U68 for port A and U69 for port B convert U71's transmit and receive data TTL-level signals to RS-232 and RS422 level signals respectively. These drivers/receivers are described in greater detail in the following subsections.

On the microcontroller-side of U71, 8-bit parallel data is transferred to and from U71 via U56's multiplexed address/data bus, AD0 thru AD7. Transferred data includes the data to be converted and transmitted by U71, the data received and converted by U71, and SCC command data. U71 performs parallel-to-serial and serial-to-parallel conversions for the transmit and receive data respectively.

SERCS* from I/O address decoder U76 is the active-low memory-mapped chip select line for SCC U71. It is applied to U71's chip select input at U71 pin 38. This chip select line is mapped to the microcontroller's external memory area between A000H and AFFFH. However, only the A000H thru A003H addresses are used as described in the following paragraph.

Address lines between microcontroller U56 and SCC U71 include only U56's lower two (2) address lines, A0 and A1. Thus, U56 reads from and writes to U71 via memory locations A000H thru A003H. A0 is applied to U71's data/command input at U71 pin 37. When high and the SCC is selected, data is transferred between U56 and U71.

When low and the SCC is selected, commands are transferred between the two chips. Address line A1 is applied to U71's A/B port select input at pin 39. When A1 is high and the SCC is selected, port A communications occur. When A1 is low and the SCC is selected, port B communications occur.

RAMIOWR* from U56 and OR gate U75 (pins 11, 12 & 13) is applied to U71's active-low write enable input at U71 pin 40. This logic line pulses low when U56 writes a byte to a RAM location or to an memory-mapped I/O location such as address A000H. [Audio System Board schematic diagram sheet 2.]

RS-232 Serial Port

On the rear panel of the Enhanced Audio Enclosure, the DB-9 connector labeled "PC" provides RS-232 interconnections for the PC. Normally, serial port COM2 at the PC is used for PC-to-Enhanced Audio Enclosure control data interfacing. The data rate is 9600 baud.

Integrated circuit U68 is a Maxim MAX202 (or equivalent) dual transceiver device. As previously stated, U71's port A is utilized for communications with the PC and driver/receiver (transceiver) U68 performs TTL-to-RS-232 conversions between U71 port A and the PC's serial port. [Audio System Board schematic diagram sheet 6.]

Connector J17, shown within dotted lines on the schematic, is a female DB-9 connector at the Enhanced Audio Enclosure's rear panel (part of I/O Backplane Board). Transmit and receive RS-232 serial data to and from the PC is present on J17 pins 2 and 3 respectively. Interconnections are provided by 96-pin DIN connector J2 on the Audio System Board, mating connector J21 on the I/O Backplane Board, and the I/O Backplane Board's traces.

One driver within U68 is employed for RS-232 communications to the PC. TTL-level serial data signals from U71's port A transmit output at U71 pin 16 are applied to U68 pin 11, the input of the driver. The driver's output at U68 pin 14 is coupled to J2 pin 35 by inductor L12. This signal is identified TX_PC_DATA_OUT and it is routed through the I/O Backplane Board to J17 pin 2 and from here, to the PC's serial COM port receive input.

The other driver within U68 is used as a power-up status line to the PC. POWER_STATUS_OUT from U68 pin 7 is applied to the COM port's clear-to-send pin. It is pulled to approximately -9 volts by the driver when the Enhanced Audio Enclosure is powered-up. This signal is routed through the I/O Backplane Board to J17 pin 8.

Only one receiver within U68 is used. Receive serial data from the PC's serial COM port is routed into the Enhanced Audio Enclosure via J17 pin 3 at the rear panel. From this point the serial data is applied to J2 pin 13 on the Audio System Board. Inductor L11 couples this signal into the receiver at U68 pin 13. The receiver then converts the RS-232-level signals to TTL-level signals and applies them to U71's port A receive input at pin 14.

Three (3) suppressors within transient voltage suppressor TVS11 provide surge suppression on the serial and power-up status lines.

Integrated circuit U68 has a built-in +5-volt to ±10-volt charge pump converter; therefore, it only requires power from the +5VDIG supply to generate positive and negative RS-232 voltages. Capacitors C287 thru C290 are the chip's charge-pump capacitors. The ±10-volt supplies are used by the chip's two RS-232 TX drivers.

RS-422 Serial Port

Future serial I/O expansion capability is provided by the RS-422 full-duplex serial port at the back of the Enhanced Audio Enclosure. These connections are present at the female DB-9 connector labeled "I/O". This port meets EIA RS-422-A specifications up to a data rate of 19.2k baud. RS-422 serial links transfer data using balanced differential signals.

Integrated circuit U69 performs TTL-to-RS-422 conversions for SCC U71 port B. This chip is an Maxim MAX490 (or equivalent) device. Transmit and receive TTL-level serial data from U71 pins 29 and 31 is applied to the driver and receiver within U69 at pins 3 and 2 respectively. Differential lines on the external side of U69 are applied to the 96-pin connector J2 via inductors L13 thru L16. These differential lines are interconnected to J16 (part of I/O Backplane Board) at the Enhanced Audio Enclosure's rear panel.

Four (4) suppressors within transient voltage suppressor TVS12 provide surge suppression on the RS-422 differential serial data lines.

AUDIO INPUT CIRCUITS

All audio signals applied to a C3 Maestro console system are routed into the console system by connectors and terminal blocks at the rear panel of the Enhanced Audio Enclosure. These connectors and terminal blocks are parts of the I/O Backplane Board. The I/O Backplane Board routes the signals to the input circuitry on the Audio System Board. Audio inputs include signals such as mic audio, line input audio from the CEC/IMC, and tones from a paging encoder.

After conditioning by the respective audio input circuits described in the following subsections, the audio signals are applied to the audio switching matrix formed by

the cross-point switch chips. Before application to the audio matrix, each signal is adjusted for a nominal level of 436 millivolts rms (1.23 Vp-p) via one or more digital pots within the particular input audio circuit. Most audio input circuits on the Audio System Board have a dynamic range of approximately 12 dB.

Supervisor Headset Mic

Input At the rear panel of the Enhanced Audio Enclosure, the cable from the supervisor's headset jack box mates with the female DB-9 connector labeled "SUPER H/S". This is connector J7 on the I/O Backplane Board. Mic audio from the headset is applied to J7 pin 9 and the I/O Backplane Board routes this signal, SUPR_HEADSET_MIC_IN, to the Audio System Board's supervisor mic input at connector J1 pin 76. On the Audio System Board, this line is also identified as SUPR_HEADSET_MIC_IN. Connector J1 on the Audio System Board is a 96-pin DIN connector which mates with J22 on the I/O Backplane Board. [Audio System Board schematic diagram sheet 10. Also see I/O Backplane Board schematic diagram sheets 2 and 5 in LBI-39102.]

Mic DC Bias & Surge Protection

SUPR_HEADSET_MIC_IN is biased-up by the +12VA supply and resistor R163 on the Audio System Board. This relatively low-impedance dc bias is required for the mic and earphone amp circuits within the headset. When a headset is connected, the bias drops to approximately 3.0 Vdc. Static discharge surge protection is provided by one suppressor within transient voltage suppressor TVS3. As shown in the schematic, this suppressor is basically two 12-volt zener diodes connected back-to-back. [Audio System Board schematic diagram sheet 10.]

Ground reference for the supervisor's mic audio is provided by J1 pin 44. This connection is identified as SUPR_HEADSET_MIC_IN_GND on both the Audio System Board and the I/O Backplane Board schematic diagrams.

Input Buffer

The moderate-level SUPER_HEADSET_MIC_IN mic audio signal (approximately 200 mVp-p) is ac-coupled by C28 into an inverting buffer circuit formed by op-amp U10 (pins 8, 9 & 10) and associated components. This buffer stage does not provide any voltage gain for the mic audio signal but simply impedance buffering and high-frequency roll-off. C74 in the feedback loop sets the -3 dB roll-off point to approximately 7.2 kHz. U10's non-inverting input (+) is grounded and thus the output signal on pin 8 rides on a zero-volt dc potential in reference to analog ground. This is possible since all op-amps on the Audio System Board are powered by the bipolar (dual-polarity) power supply generated by the switching regulator circuits.

Input Level Control

Buffered mic audio from U10 pin 8 is applied to the high-side (H1) of a digital pot within U16 (pins 3, 4 & 5). During alignment procedures performed at the Personal Computer (PC), this digital potentiometer (pot 4) provides input level-adjustment for the supervisor mic audio prior to application to the succeeding automatic level control (ALC) circuit. When commanded from the PC, microcontroller U56 loads wiper position data into U16. See the section entitled "**DIGITAL POT CIRCUITS**" for circuit analysis details describing how the digital pots are adjusted. The attenuated signal on U16's wiper at pin 5 is applied to the succeeding ALC circuit.

Automatic Level Control (ALC)

One-half of U29 (pins 9 – 16), a dual transconductance op-amp, and the associated components form the supervisor headset mic ALC circuit. This high-performance ALC stage also provides pre-limiting functions for the supervisor mic audio. ALC can be enabled or disabled by changing the DIP switch at U29 pin 15 (S1 position 4). Normally, ALC is always enabled by selecting the "ON" or CLOSED" position. See LBI-39101 for additional information.

Buffer & Fast-Limiter

The buffered, level-controlled and pre-limited output from U29 pin 12 is applied to op-amp voltage follower U41. The output of this stage at U41 pin 1 is applied to a fast-limiter stage.

Op-amp U64 (pins 1, 2 & 3) and associated components form a fast-limiter circuit for the supervisor headset mic audio signal. At the output, U64 pin 1, the maximum signal swing will not exceed approximately 5.9 Vp-p (2.1 Vrms). This signal is then scaled by divider network R369 and R370 and applied to high-pass and low-pass filter circuits which jointly, form a bandpass circuit for voice audio frequencies.

High & Low-Pass Filters

The supervisor headset mic audio high-pass filter circuit is formed by U64 (pins 5, 6 & 7) and the associated components. This filter greatly attenuates any low-frequency signals such as 60 Hz hum which may exists in the mic audio signal.

The high-pass filter's output is fed to a low-pass filter formed by U63 (pins 1, 2 & 3) and the associated components. This filter greatly attenuates audio signals

above 3 kHz which may be present in the mic audio signal such as high-frequency hiss.

Output Level Control

The low-pass filter's output at U63 pin 1 is ac-coupled into the high-side of a digital pot within U65 (at U65 pin 12). This digitally-controlled potentiometer (pot 7) allows the supervisor's headset mic level to be set from the PC. This pot's setting should ***not*** be changed from the factory setting. See the section entitled "**DIGITAL POT CIRCUITS**" for additional details.

Output Buffer/Filter & Audio Matrix Inputs

The signal on the wiper of the digital pot is ac-coupled into a buffer/filter circuit formed by U63 (pins 5, 6 & 7) and associated components. The output of this stage, identified as SUPR_MIC (U63 pin 7), is applied to cross-point switch chips U82, U81 and U80 for distribution (pins 23, 23 & 6 respectively). At nominal voice levels into the supervisor's headset mic, the signal on SUPR_MIC is approximately 1.0 Vp-p. [Audio System Board schematic diagram sheets 10, 14, 15 and 19.]

In most instances, SUPR_MIC is routed only to the Line 1 output via U82. (Supervisor mic audio is recorded by sending the Line 1 output audio to the recorder.) However, during local Call Director telephone operations (non-CD patch operations), SUPR_MIC is routed via U80 to the Call Director output line so it can be applied to the phone line connected to the Call Director. See the section entitled "**AUDIO OUTPUT CIRCUITS**", subsection "**Line Outputs**", for details on the Line output circuits. [Audio System Board schematic diagram sheets 14 and 19.]

Sidetone

SUPR_MIC audio is also applied to the supervisor sidetone level adjustment circuit consisting of one-half of digital potentiometer U60 and the associated components. This digital potentiometer (pot 9) provides adjustment for the supervisor's sidetone via PC control. The attenuated mic signal on the digital pot's wiper (U60 pin 13) is buffered by op-amp U47 (pins 12, 13 & 14) and applied to the audio matrix via the SUPR_SIDETONE line from U47 pin 14.

Specifically, SUPR_SIDETONE audio is applied to cross-point switch chip U40 at pin 22. The sidetone signal is switched to the supervisor's headset earphones by U40 under microcontroller U56 control. SUPR_SIDETONE may also be switched to the operator's headset earphones. In both instances, other signals such as select audio (SELECT_AUDIO) is summed with SUPR_SIDETONE before application to a headset via U40 and the supervisor headset earphone output circuit. [Audio System Board schematic diagram sheets 10 and 20.]

See the section entitled "**AUDIO OUTPUT CIRCUITS**" for details on the supervisor and operator headset earphone output circuits.

Keying

The supervisor's headset can be keyed from a footswitch via the "SUPR_F/S" connector (I/O Backplane Board connector J15) at the rear panel, or the PTT input provided at the "SUPR H/S" connector (J7), also at the rear panel. It *cannot* be keyed from the Dispatch Keyboard. Footswitch and headset connectors on the rear panel have a common PTT line identified as SUPR_PTT_IN. SUPR_PTT_IN is applied to the Audio System Board at J2 pin 41. Microcontroller U56 reads SUPR_PTT_IN using the logic interface circuitry described in the sections entitled "**PTT And Sense Input**" and "**Input Scanning**". [Audio System Board schematic diagram sheets 5 and 28.]

Operator Headset Mic

Basically, the first four (4) stages of the operator's headset mic input circuit are identical to the first four stages of the supervisor's circuit. Therefore, these stages will not be discussed in full detail.

At the rear panel of the Enhanced Audio Enclosure, the cable from the operator's headset jack box mates with the female DB-9 connector labeled "OPER H/S". This is connector J6 on the I/O Backplane Board. Mic audio from the headset is applied to J6 pin 9 and the I/O Backplane Board routes this signal, OPR_HEADSET_MIC_IN, to the Audio System Board's operator mic input at J1 pin 83. This input is also identified as OPR_HEADSET_MIC_IN. J1 is a 96-pin DIN connector on the Audio System Board which mates with J22 on the I/O Backplane Board. [Audio System Board schematic diagram sheet 9. Also see I/O Backplane Board schematic diagram sheets 2 and 5 in LBI-39102.]

Selection

Buffered and level-controlled operator headset mic audio from the output of the first four stages at U41 pin 7 (OPR_HEADSET_MIC) is applied to the audio matrix at U80 pin 8. As shown in the schematic diagram, three (3) switches within U80 are used to select between the operator, desk or boom/gooseneck mic signals. The selected signal at the output of the matrix chip, OPR_MIC_SELECT (U80 pin 14), is routed to the input of non-supervisory mic audio post-conditioning circuit. [Audio System Board schematic diagram sheets 9, 11 and 19.]

See the following section entitled "**Non-Supervisory Mic Audio Selection And Post-Conditioning**" for circuit analysis details on the post-conditioning mic audio circuits.

Keying

The operator's headset can be keyed from any of several places including the Dispatch Keyboard, a footswitch, or the OPR_PTT_IN input. The OPR_PTT_IN input is located at "OPER H/S" connector J6 pin 6 on the Enhanced Audio Enclosure's rear panel. Microcontroller U56 reads OPR_PTT_IN (J2 pin 45 on the Audio System Board) via the associated I/O Backplane Board interconnections and the logic interface circuitry on the Audio System Board. Logic interface circuitry is described in detail in the sections entitled "**PTT And Sense Input**" and "**Input Scanning**". J2 is a 96-pin DIN connector on the Audio System Board which mates with J21 on the I/O Backplane Board. [Audio System Board schematic diagram sheets 5 and 28. Also see I/O Backplane Board schematic diagram sheets 3 and 5 in LBI-39102.]

Desk Mic

With the exception of the dc mic bias circuitry and slight input level differences, the first four stages of the desk mic input circuit is basically identical to the supervisor circuit previously described. Therefore, these stages will not be discussed in full detail.

At the rear panel of the Enhanced Audio Enclosure, the desk mic connects to the female DB-9 connector labeled "DESK MIC", connector J5 on the I/O Backplane Board. Audio from the mic is applied to J5 pin 9 and the I/O Backplane Board routes this signal, DESK_MIC_IN, to the Audio System Board's desk mic input at J1 pin 82. The Audio System Board desk mic input is also identified as DESK_MIC_IN. J1 is a 96-pin DIN connector on the Audio System Board which mates with J22 on the I/O Backplane Board. [Audio System Board schematic diagram sheet 9.]

Mic DC Bias & Surge Protection

A well-filtered dc bias for the desk microphone is provided by the network formed by R40, R60, R61 and C64. With a microphone connected (1000-ohm load), dc bias on DESK_MIC_IN is approximately 4 Vdc.

Selection

Buffered and level-controlled desk mic audio from the output of the first four (4) stages at U41 pin 14 (DESK_MIC) is applied to the audio matrix at U80 pin 21. As shown in the schematic diagram, three (3) switches within U80 are used to select between the operator, desk, or boom/gooseneck mic signals. The selected signal at the output of the matrix chip (U80 pin 14) is routed to the non-supervisory mic audio post conditioning circuit. Desk mic audio is only selected if no headset and/or no boom/gooseneck mic is connected; it has the lowest priority. [Audio System Board schematic diagram sheets 9, 11 and 19.]

Keying

The desk mic can be keyed from the Dispatch Keyboard, footswitch, or the DESK_PTT_IN input at "DESK MIC" connector J5 pin 6. Microcontroller U56 reads DESK_MIC_PTT_IN at J2 pin 42 via the associated I/O Backplane Board interconnections and the logic interface circuitry. This logic interface circuitry is described in detail in the sections entitled "**PTT And Sense Input**" and "**Input Scanning**". J2 is a 96-pin DIN connector on the Audio System Board which mates with J21 on the I/O Backplane Board. [Audio System Board schematic diagram sheets 5 and 28.]

Boom/Gooseneck Mic

With the exception of the lack of any mic dc bias circuitry and increased signal gain in the first amplifier stage, the first four (4) stages of the boom/gooseneck mic input circuit is nearly identical to the supervisor circuit previously described. Therefore, these stages will not be discussed in full detail.

At the rear panel of the Enhanced Audio Enclosure, a boom or gooseneck microphone connects to the female DB-9 connector labeled "B/G MIC", connector J4 on the I/O Backplane Board. Audio from the mic is applied to J4 pin 9 and the I/O Backplane Board routes this signal, B/G_MIC_IN, to the Audio System Board's boom/gooseneck mic input at J1 pin 85. On the Audio System Board, this input is also identified as B/G_MIC_IN. [Audio System Board schematic diagram sheet 9.]

All boom or gooseneck microphones used with the C3 Maestro console employ dynamic magnetic cartridge-type voice coils and no internal amplifiers; therefore, no dc bias is required on the mic audio input line. Typically, these mics have output levels less than 10 millivolts peak-to-peak at average voice sound levels.

Input Buffer/Amp

Since audio from the boom/gooseneck mic is much lower than the headset and desk mics, the gain of the first amplifier on the Audio System Board stage is much larger. Op-amp U10 (pins 1, 2 & 3) and the associated components provide approximately 22 dB of gain. Capacitor C50 sets the -3 dB high-frequency roll-off point to approximately 7.2 kHz. This stabilizes the circuit by preventing oscillations.

Selection

Buffered and level-controlled boom/gooseneck mic audio (B/G_MIC) from U41 pin 8 is applied to the audio matrix at U80 pin 9. As shown in the schematic diagram, three (3) switches within U80 are used to select between the operator, desk or boom/gooseneck mic signals. The selected signal at the output of the matrix chip (U80 pin 14) is routed to the non-supervisory mic audio post conditioning circuit. Boom/gooseneck mic audio is only selected if no headset (supervisor or operator) is connected to the Enhanced Audio Enclosure. [Audio System Board schematic diagram sheets 9, 11 and 19.]

Keying

The boom/gooseneck mic can be keyed from the Dispatch Keyboard, footswitch, or the B/G_PTT_IN input at "B/G MIC" connector J4 pin 6 on the I/O Backplane Board. Microcontroller U56 reads B/G_PTT_IN at J2 pin 43 via the associated I/O Backplane Board interconnections and its logic interface circuitry. This logic interface circuitry is described in detail in the sections entitled "**PTT And Sense Input**" and "**Input Scanning**". J2 on the Audio System Board mates with J21 on the I/O Backplane Board. [Audio System Board schematic diagram sheets 5 and 28. Also see I/O Backplane Board schematic diagram sheets 2 and 4.]

NOTE

All boom/gooseneck mic connectors (male DB-9) must have pins 2 and 3 jumpered together so B/G_MIC_SENSE_IN will be activated (grounded) when the mic is connected to J4 (female DB-9).

Non-Supervisory Mic Audio Selection And Post-Conditioning

Selection

If *no* headset is connected to the Enhanced Audio Enclosure's supervisor headset connector, I/O Backplane Board J7 pin 3 and Audio System Board J2 pin 74 (SUPR_JACK_SENSE_IN) are inactive or high. In this case, the Audio System Board selects a non-supervisory mic audio signal (OPR_HEADSET_MIC, DESK_MIC or B/G_MIC). This selection is based upon the boom/gooseneck mic sense input at Audio System Board J2 pin 72 (I/O Backplane Board J4 pin 3) and the operator headset sense input at J2 pin 76 (I/O Backplane Board J6 pin 3).

As previously described, the selected mic audio is connected to OPR_MIC_SELECT using switches within cross-point switch U80. Of these three non-supervisory mic inputs, the operator headset audio has the highest priority and the desk mic audio has the lowest. In other words, mic audio from the desk mic is never selected if a headset or a boom/gooseneck mic is connected. In addition, mic audio from the desk and boom/gooseneck mics are never used if a headset is connected. The microcontroller's operating firmware sets this mic priority. [Audio System Board schematic diagram sheets 9, 11, 19 and 29. Also see I/O Backplane Board schematic diagram sheets 3 and 5.]

Post-Conditioning

The selected (switched-in) non-supervisory OPR_MIC_SELECT signal from U80 pin 14 is applied to post-conditioning circuits which are nearly identical to the supervisor post-conditioning mic audio circuits previously described. Therefore, these circuits will not be discussed in full detail. The circuitry includes a fast-limiter, high and low-pass filters which together provide voice-audio bandpass filtering, a digital pot level adjustment circuit, a mic buffer/filter, a sidetone digital pot level adjustment circuit, and a sidetone buffer/amp circuit. [Audio System Board schematic diagram sheets 11 and 19.]

The circuit's output, OPR_MIC at U63 pin 8, is applied to cross-point switch chips U82, U81 and U80 for distribution as needed. In most instances, the selected non-supervisory mic audio signal is routed only to the Line 1 output via U82. However, during local Call Director telephone operations (non-CD patch operations), OPR_MIC is routed via U80 to the Call Director output line so it can be applied to the phone line connected to the Call Director. [Audio System Board schematic diagram sheets 11, 14, 15 and 19.]

OPR_MIC is also applied to the non-supervisory sidetone level adjustment circuit consisting of digital potentiometer U60 (wiper = pin 5) and an op-amp buffer stage. This digital pot can be set via <Alt> <Vol ↑ > (increase sidetone) and <Alt> <Vol ↓ > (decrease sidetone) keystrokes at the Dispatch Keyboard program. The C3 Maestro's application program also allows digital pot adjustment via a note card. See the section entitled "**DIGITAL POT CIRCUITS**" in this manual for additional circuit analysis details. See LBI-39101 for specific details on adjusting a digital pot via a note card. [Audio System Board schematic diagram sheet 11.]

The attenuated and buffered sidetone signal, OPR_SIDETONE, is applied to the cross-point switch chip U40 at pin 7. This sidetone signal is switched into a summing network and applied to the operator's headset earphones. It may also be summed with other signals and

applied to the supervisor's headset earphones. [Audio System Board schematic diagram sheet 20.]

Line Inputs

Four 600-ohm 4-wire balanced line interfaces are provided at the Enhanced Audio Enclosure's rear panel for interfacing to the CEC/IMC Digital Audio Switch. All four inputs are basically identical; therefore, only the Line 1 input circuit will be discussed in detail. [Audio System Board schematic diagram sheets 12 and 13.]

At the Enhanced Audio Enclosure, all 4-wire balanced line audio connections to and from the CEC/IMC are made at I/O Backplane Board connector J1. This female DB-25 connector is labeled "LINES 1-4" on the rear panel. All balanced line audio signals on J1 are routed to 96-pin DIN connector J22. J22 mates with Audio System Board connector J1.

Line Coupling & Surge Protection

Audio on the Line 1 input pair is coupled into the Audio System Board via 600-ohm coupling transformer T11. The balanced inputs are identified LINE_1_IN+ and LINE_1_IN- at 96-pin DIN connector J1 pins 96 and 95 respectively. The I/O Backplane Board's DB-25 connector at the rear panel of the Enhanced Audio Enclosure also uses this same labeling (J1 pin 1 = LINE_1_IN+ and J1 pin 2 = LINE_1_IN-). [Audio System Board schematic diagram sheet 12. Also see I/O Backplane Board schematic diagram sheets 1 and 5.]

On the Audio System Board, resistor R497 loads T11's secondary for an approximate line input impedance of 600 ohms. Surge protection on the transformer's secondary or non-line side is provided by one suppressor within transient voltage suppressor TVS13.

Level Control & Buffer/Amp

C336 ac-couples the signal on the secondary of T11 to one of the digital pots within U90. This digital pot provides computer-controlled level adjustment for the Line 1 audio input via the PC during alignment procedures. See the section entitled "**DIGITAL POT CIRCUITS**" for circuit analysis details describing how the digital pots are adjusted.

Op-amp U89 (pins 12, 13 & 14) and associated components form a non-inverting buffer/amplifier stage that provides a voltage gain of two (2). Capacitor C325 sets the -3 dB roll-off point at 7.2 kHz. This stage amplifies the signal from the wiper of the digital pot (U90 pin 13). The amplified signal is applied to the succeeding high-pass filter stage via capacitor C324.

High-Pass Filter/Buffer & Audio Matrix Input

Capacitor C324 ac-couples Line 1 audio from U89 pin 14 to the input of a high-pass filter circuit formed by U89 (pins 5, 6 & 7) and associated components. This active filter circuit passes all voice audio frequencies and greatly attenuates any frequency below 300 Hz which may be present on the Line 1 input (60 Hz hum, for example). The output of this filter, LINE_1_IN at TP38, is applied to matrix chip U49 at pin 6. Using a cross-point switch within U49, microcontroller U56 can switch Line 1 input audio to the SELECT_AUDIO line as required. With a -5 dBm signal (436 mV rms into 600 ohms) on the Line 1 balanced input, the LINE_1_IN signal at TP38 is set via the digital pot to 436 millivolts rms (1.23 Vp-p).

Call Director

The C3 Maestro console system can be connected to Call Director (CD) for CD patch telephone operations. This feature allows the dispatcher to "patch" a telephone line to a specific unit, talk group, conventional channel or radio patch in the CEC/IMC network. When not being used for CD patch telephone communications, the dispatcher may also use the Call Director for local telephone operations.

NOTE

A *Call Director patch* should not be confused with a *radio patch* in which a collection of radio talk groups are interconnected for common communications as one group.

Audio interfacing to a CD is performed by a 4-wire 600-ohm balanced line interface. On the Audio System Board, the input pair interface is very similar to the Line 1 input circuitry described in the previous section. Audio on this pair is from the CD (originating from the telephone's "mic") and it is heard by a radio in a patch operation or by the dispatcher in a local CD telephone operation.

Line Coupling & Surge Protection

Audio from the Call Director is applied to connector J3 on the I/O Backplane Board. This female DB-9 connector at the Enhanced Audio Enclosure's rear panel is labeled "CALL DIR". I/O Backplane Board interconnections route the balanced line input signal from J3 to 600-ohm coupling transformer T2 on the Audio System Board. On the Audio System Board, these balanced line audio inputs are identified as CALL_DIRECTOR_IN+ and CALL_DIRECTOR_IN- at Audio System Board connector J1 pins 55 and 87 respectively. J1 is the 96-pin DIN connector on the Audio System Board that mates with J22 on the I/O Backplane Board. A typical CD balanced line

audio input signal is -20 dBm. [Audio System Board schematic diagram sheet 8.]

Resistor R171 loads T2's secondary for a 600-ohm line input impedance. Surge protection is provided by one suppressor within transient voltage suppressor TVS6.

Level Control & Output Buffer/Amp

Capacitor C119 ac-couples the signal on the secondary side of T2 to one of the digital pots within U19. This digital pot provides computer-controlled level adjustment for the CD input audio. See the section entitled "**DIGITAL POT CIRCUITS**" for circuit analysis details describing how the digital pots are adjusted.

Op-amp U18 (pins 12, 13 & 14) and associated components form a non-inverting buffer/amplifier stage with an approximate voltage gain of twenty-one (21) or 26 dB. C118 in the op-amp's feedback loop sets high-frequency roll-off to -3 dB at 7.2 kHz. With a -20 dBm CALL_DIRECTOR_IN+/- line input signal, the CD signal at TP15 (U18 pin 14) is set via the digital pot to 436 millivolts rms (1.23 Vp-p) into the matrix.

Audio Matrix Inputs

Buffered and level-adjusted CD input audio from U18 pin 14, identified as CD, is applied to cross-point switch chips U81, U49, U39, U48, U80 and U40 for distribution as required. For example, during a CD radio patch, a switch within U81 turns on to route the CD input audio (originating from telephone's "mic") to the CEC/IMC via CIM Line 4. [Audio System Board schematic diagram sheets 15 thru 20.]

If the unselect/telephone recorder output is used for sending *Call Director audio to a recorder*, CD input audio applied to U80 pin 20 is switched on and off via the switch within U80. Switched CD audio on the output side of the audio matrix, CD_SWITCHED, is applied to the unselect/telephone recorder output circuit (output is USEL/TELE_RECORDER_OUT at J2 pin 86). However, if this output circuit is used for sending *unselect audio* to a recorder, CD_SWITCHED is not used and line 2, 3 and 4 input audio is switched in via U48 pins 21, 9 and 20 respectively. [Audio System Board schematic diagram sheets 18 and 19.]

Pager

Audio from a paging encoder (or similar device) is applied to terminal block J2 at the rear panel of Enhanced Audio Enclosure. This terminal block is labeled "PAGING". It provides connections for both pager audio (usually tones) and a pager PTT (enable) input. Pager audio is applied to J2 terminals 1 and 2. On both the Audio System Board and the I/O Backplane Board, the balanced line audio input is identified PAGER_IN+ and PAGER_IN-.

The pager PTT input is routed to the Audio System Board via the I/O Backplane Board and then interfaced to microcontroller U56. See the section entitled '**PTT And Sense Input**" for specific details. Pager audio is only switched in when the paging encoder activates the pager PTT input.

Line Coupling & Surge Protection

Balanced audio from J2 terminals 1 and 2 is routed through the I/O Backplane Board and applied to 600-ohm coupling transformer T3 on the Audio System Board. PAGER_IN+ is located at J1 pin 28 and PAGER_IN- is located at J1 pin 60. Typical pager audio input level is -5 dBm. [Audio System Board schematic diagram sheet 8.]

Resistor R198 loads T3's secondary for a line input impedance of 600 ohms. Surge protection is provided by a suppressor within transient voltage suppressor TVS6.

Level Control & Output Buffer/Amp

Capacitor C140 ac-couples the signal on the secondary or non-line side of T3 to one of the digital pots within U21 (pot 28). See the section entitled **DIGITAL POT CIRCUITS**" for circuit analysis details describing how the digital pots are adjusted. The attenuated pager signal on the wiper of the pot (U21 pin 5) is applied to the buffer/amp stage formed by op-amp U18 (pins 8, 9 & 10) and associated components. This stage has an approximate voltage gain of four (4) or 12 dB. C116 in the feedback loop sets the high-frequency roll-off to approximately -3 dB at 7.2 kHz. The output at U18 pin 8 or TP14 is identified PAGER.

Audio Matrix Inputs

PAGER audio signals are applied to cross-point switch chips U82, U81 and U49 pins 7, 7 and 23 respectively. U82 and U81 switch the pager's signals to the line outputs. U49 switches the signals to the SELECT_AUDIO line so it can be routed to the select audio output devices. These devices include the select speaker, headsets and the select recorder output. [Audio System Board schematic diagram sheets 14, 15, 16 & 20.]

DIGITAL POT CIRCUITS

To provide computer-controlled level settings from the Personal Computer (PC), the audio input and output circuits incorporate 256-position digitally-controlled potentiometers. These digital pots allow all audio levels associated with the Enhanced Audio Enclosure to be

adjusted via the PC. Adjustments include dispatch operator-adjustable audio levels such as headset sidetone volumes and system-level adjustments such as line input and output levels to and from the CEC/IMC Digital Audio Switch.

With the exception of the headsets' sidetone volume adjustments, none of the digital pots provide volume adjustments for the speaker or headset earphone audio signals. Speaker and headset volume adjustments are accomplished at the respective speaker or headset by mechanical potentiometers or as described in the following note.

NOTE

Communication module volume changes at the C3 Maestro effect CEC/IMC CIM line output levels, not the digital pots within the Enhanced Audio Enclosure.

Fifteen (15) dual potentiometer chips are located on the Audio System Board for a total of thirty (30) individual pots; there are *no* mechanical potentiometers – *all* audio level adjustments are made via software control. Basically, commands from the PC instruct microcontroller U56 to load new settings into a digital pot. See Table 3.

As shown in Table 3, for example, both pots within U16 are in separate circuits. One is located in the operator headset mic input preamp/pre-adjustment circuit (wiper is pin 13; pot 3) and the other is in the supervisor headset mic input preamp/pre-adjustment circuit (wiper is pin 5; pot 4). [Audio System Board schematic diagram sheets 9 and 10.]

All of the digital pots initially power-up with the wiper in a 50% or centered position. Microcontroller 56 then immediately loads each pot in accordance with its respective setting stored in a "working" area of serial EEPROM chip U57. This EEPROM also contains an unchangeable "default" digital pot storage area. When shipped from the factory, the working area matches the default area.

The operator sidetone digital pot (U60 pins 3, 4 & 5) can be set via <Alt> <Vol ↑ > and <Alt> Vol ↓ > key stokes from the console's Dispatch Keyboard. [Audio System Board schematic diagram sheets 10 and 11.]

In addition, this pot and all other digital pots on the Audio System Board may be set using the console's application program via a note card. Refer to LBI-39101 for details.

NOTE

DO NOT ADJUST any digital pot from the factory setting unless a full understanding of the consequences is known.

When a digital pot adjustment occurs, commands are sent from the PC to microcontroller U56 via the RS-232 serial communication link between the PC and the Enhanced Audio Enclosure. Next, U56 processes these commands and serially loads the new setting into the appropriate digital pot using the serial data (SDATA) line, the serial clock (SCLK) line, and a chip select logic line. As shown in Table 3, the fifteen (15) chip select logic lines, one for each dual pot chip, are identified as DIG_POT_SEL_1/2 thru DIG_POT_SEL_29/30. The serial data stream length sent out from U56 via SDATA during a digital pot adjustment is 17 bits long.

For example, to load both pots within U16 with new settings, DIG_POT_SEL_3/4 transitions high to enable the chip. Next, seventeen bits which represent the two pots' new settings are clocked into U16 using SDATA and SCLK. Finally, DIG_POT_SEL_3/4 returns low which latches the new pots settings and disables U16 from subsequent SDATA and SCLK activity. [Audio System Board schematic diagram sheets 9 and 10.]

The DIG_POT_SEL_xx logic lines are generated by microcontroller U56 by latching data bytes into octal data flip-flops U87 and U88. DIG_POT_SEL_1/2 thru DIG_POT_SEL 15/16 are latched outputs from U88 and DIG_POT_SEL_17/18 thru DIG_POT_SEL 29/30 are latched outputs from U87. [Audio System Board schematic diagram sheet 4.]

Table 3 – Digital Potentiometers

SCH. DGRM. SHEET	IC	WIPER PIN	DIGITAL POT SELECT LOGIC LINE NAME	DIGITAL POT NUMBER *	CIRCUIT LOCATED IN / ADJUSTS
1	U21	13	DIG_POT_SEL_27/28	27	N/A (pot not used)
8	U19	13	DIG_POT_SEL_1/2	1	Call Director Input
8	U21	5	DIG_POT_SEL_27/28	28	Pager Input
9	U16	13	DIG_POT_SEL_3/4	3	Operator Headset Mic Input (pre-adjustment)
9	U17	5	DIG_POT_SEL_5/6	6	Desk Mic Input (pre-adjustment)
9	U17	13	DIG_POT_SEL_5/6	5	Boom/Gooseneck Mic Input (pre-adjustment)
10	U16	5	DIG_POT_SEL_3/4	4	Supervisor Headset Mic Input (pre-adjustment)
10	U65	13	DIG_POT_SEL_7/8	7	Supervisor Headset Mic Input (post-adjustment)
10	U60	13	DIG_POT_SEL_9/10	9	Supervisor Sidetone
11	U65	5	DIG_POT_SEL_7/8	8	Operator (selected) Mic Input (post-adjustment)
11	U60	5	DIG_POT_SEL_9/10	10	Operator (Non-Super.) Sidetone
12	U90	13	DIG_POT_SEL_11/12	11	Line 1 Input
12	U90	5	DIG_POT_SEL_11/12	12	Line 2 Input
13	U67	13	DIG_POT_SEL_17/18	17	Line 3 Input
13	U67	5	DIG_POT_SEL_17/18	18	Line 4 Input
14	U51	5	DIG_POT_SEL_15/16	16	Line 2 Output
14	U51	13	DIG_POT_SEL_15/16	15	Line 1 Output
15	U32	5	DIG_POT_SEL_13/14	14	Line 4 Output
15	U32	13	DIG_POT_SEL_13/14	13	Line 3 Output
16	U14	13	DIG_POT_SEL_29/30	29	Select Speaker Output
16	U27	13	DIG_POT_SEL_21/22	21	Select Recorder Output
16	U12	13	DIG_POT_SEL_19/20	19	Select Audio Output
17	U13	13	DIG_POT_SEL_23/24	23	Unselect Speaker 2 Output
17	U14	5	DIG_POT_SEL_29/30	30	Unselect Speaker 1 Output
18	U27	5	DIG_POT_SEL_21/22	22	Unselect 4/Telephone Recorder Output
18	U13	5	DIG_POT_SEL_23/24	24	Unselect Speaker 3 Output
19	U19	5	DIG_POT_SEL_1/2	2	Call Director Output
20	U9	13	DIG_POT_SEL_25/26	25	Supervisor Headset Earphone Output
20	U9	5	DIG_POT_SEL_25/26	26	Operator Headset Earphone Output
30	U12	5	DIG_POT_SEL_19/20	20	Auxiliary Input (used for CD patch)

* Refer to LBI-39101 for typical digital pot settings.

Microcontroller U56 latches the DIG_POT_SEL_xx logic levels into U87 and U88 via its address/data bus (AD0 – AD7) and a decoded chip select logic line for each octal latch chip. The decoded chip select logic line (U87 or U88 pin 11) is a logical "OR" of the active-low POTSyy_zz from 3-to-8 line decoder U76 ($\overline{\text{POTS16\_31}}$ for U87 and $\overline{\text{POTS0\_15}}$ for U88) and the active-low RAMIOWR*. As shown on the schematic diagram $\overline{\text{POTS16\_31}}$ is mapped to the B000H memory area. Therefore, to latch new data to the Q outputs of U87 and thus change one of the DIG_POT_SEL_xx logic outputs from U87 (DIG_POT_SEL_17/18 thru DIG_POT_SEL_29/30), microcontroller U56 simply writes the data byte to I/O location B000H. The written byte has only one bit high and it activates the $\overline{\text{POTS16\_31}}$ logic line. U56 changes the DIG_POT_SEL_1/2 thru DIG_POT_SEL_15/16 logic outputs from U88 in a similar fashion by writing a data byte to memory location C000H. This write activates the active-low $\overline{\text{POTS0\_15}}$ logic line. [Audio System Board schematic diagram sheets 4 and 6.]

TONE GENERATION CIRCUITS

Sinewave Generators U46 And U58

Two (2) identical programmable sinewave generator chips on the Audio System Board, U46 and U58, give it the ability to generate single-tone and DTMF (Dual-Tone Multi-Frequency) tone signals. With current firmware and PC software, this circuitry is not utilized.

Both chips are directly controlled by microcontroller U56. On-chip circuitry includes serial interface circuits (a shift register and a latch), a sine look-up table, an 8-bit digital-to-analog converter, a smoothing filter circuit and an op-amp buffer output stage. [Audio System Board schematic diagram sheet 3.]

A 921.6 kHz reference clock from U74 pin 6 is applied to the clock inputs at pin 16 of each sinewave generator chip. U46 and U58 are powered from the bipolar ±5-volt supply lines. Pin 11 on each chip is the sinewave output pin. [Audio System Board schematic diagram sheets 2 and 3.]

Frequency data from microcontroller U56 is serially loaded into U46 and U58 via the SCLK, SDATA and the respective chip select logic line – SINGEN_CS1 for U46 and SINGEN_CS2 for U58. All of these logic lines originate from port 1 of U56. To change one of the sinewave generator's output frequency, U56 first clocks an appropriate 16-bit word into the generator's input shift register via the SCLK and SDATA logic lines. Next, U56 pulses (low-high-low) the respective chip select logic line (SINGEN_CS1 or SINGEN_CS2) to latch the word into the chip's internal 16-bit latch. Upon latching, the generator immediately begins generating the newly loaded tone frequency. To turn a generator's output off, U56 loads a 0000H 16-bit word (all zeros).

Summer/Buffer Op-Amp Stage

Each sinewave generator outputs a 5 Vp-p (±2.5 V) tone at its pin 11. The signals are then summed into a summer/buffer stage formed by op-amp U47 (pins 1, 2 & 3) and then amplified by U47 (pins 5, 6 & 7) and the associated components. The resulting TONE output from U47 pin 7 is applied to the audio switching matrix so it may be switched into and summed with a line output, a speaker output, or the Call Director output.

Cross-point switch chips which route TONE to an audio output circuit include U82 (Line 1 & 2 output), U81 (Line 3 & 4 output), U49 (select audio) and U80 (Call Director output). [Audio System Board schematic diagram sheets 14, 15, 16 and 19.]

TEST_TONE from U47 pin 1 may be used during automated test procedures by selectively switching it to the input of any one of several audio circuits via cross-point switch chips U79 and U62 within the audio switching matrix. During these test, the output of the circuit under test is monitored by the VU meter circuitry to provide a pass/fail status indication to Personal Computer. [Audio System Board schematic diagram sheets 3 and 21.]

AUDIO MATRIX CONTROL CIRCUITS

All audio routing within the Enhanced Audio Enclosure's audio switching matrix is accomplished by ten (10) cross-point switch chips. These ten chips form the audio switching matrix. They are directly controlled by microcontroller U56. Specific chip numbers are listed in Table 4. Each cross-point switch chip has an 8 x 8 switch matrix for a total of 64 switches per chip and 640 switches in the complete matrix. Audio signal inputs are applied to the chips' X pins and all matrix outputs originate from the chips' Y pins. Microcontroller U56 can individually address and control (switch on or switch off) each switch as required. [Audio System Board schematic diagram sheets 14 thru 21.]

Not all of the 240 switches within the audio matrix are used. On the schematic diagram, switches which may be turned on during normal console operations are indicated by a small dot (•) on the appropriate X-Y cross-point (┼) matrix location. Switches which are never turned on contain no dot on the cross-point.

Power-Up Initialization

When the Audio System Board is powered-up, all cross-point switches within the cross-point switch chips are initially cleared (switched open or off). This is accomplished via the hardware RESET pulse from microprocessor supervisory chip U55. Typically, this reset period lasts between 60 and 100 milliseconds after power-up. RESET is applied to the reset input of each cross-point chip (pin 10). [Audio System Board schematic diagram sheets 2 and 14 – 21.]

To ensure correct audio routing after the hardware power-up/reset, *all* cross-point switches are first sent "turn off" commands from microcontroller U56. Next, the switches that must be closed are sent "turn on" commands For example, if U56 senses the supervisor headset is plugged in, it turns on the necessary switch within U82 to route the supervisor's mic audio signal to the Line 1 output. [Audio System Board schematic diagram sheet 14.]

Since each of the ten (10) cross-point switch chips has an 8 x 8 matrix array, at power-up, U56 must send out 640 "turn off" commands followed by several "turn on" commands. Switch turn-on/off control logic is described in the following section.

Control Logic Lines

Control logic lines for the cross-point switch chips include six (6) address logic lines and a data logic line. In addition, each chip also has a strobe logic line that performs chip selection.

Cross-Point Address And Data

Each switch within a cross-point switch chip has a unique address location that microcontroller U56 can address via the six (6) cross-point address logic lines. These logic lines are identified as XPT_A0 thru XPT_A5. An X switch coordinate is addressed by XPT_A0, XPT_A1 and XPT_A2 and a Y coordinate is addressed by the XPT_A3, XPT_A4 and XPT_A5. Address decoders within a cross-point switch decode these 3-bit X by 3-bit Y address inputs into 8 by 8 matrix addresses. [Audio System Board schematic diagram sheets 14 – 21.]

During a matrix switch change, data logic line XPT_AD0 controls on/off switch selection. This line is applied to the switch data input (pin 4) of *all* of the cross-point switch chips. U56 sets XPT_AD0 high to turn a switch on and low to turn a switch off.

Both the cross-point address logic lines and cross-point data logic line are generated by microcontroller U56 using octal buffer U86. U56 consecutively sends the required 7-bit patterns to U86 via the active-low $\overline{\text{XPT\_ENABLE}}$ line from I/O address decoder U76, its six least significant address lines (A0 thru A5), and its least significant bidirectional data line (AD0). [Audio System Board schematic diagram sheet 6.]

Table 4 – Cross-Point Switch Chips' Chip Selects

OUTPUT FROM U78 PIN NUMBER	CHIP SELECT LOGIC LINE NAME	SELECTS CROSS-POINT SWITCH CHIP
9	XPT_STROBE01	U82
10	XPT_STROBE02	U81
8	XPT_STROBE03	U49
7	XPT_STROBE04	U39
6	XPT_STROBE05	U48
5	XPT_STROBE06	U80
4	XPT_STROBE07	U40
18	XPT_STROBE08	U61
17	XPT_STROBE09	U79
20	XPT_STROBE10	U62

Strobe

After U56 sets a given XPT_A0 thru XPT_A5 address and the XPT_AD0 data logic line via U86's outputs, it toggles a switch within one of the cross-point switch chips. This is accomplished by pulsing the appropriate XPT_STROBExx logic line at pin 2 of the required cross-point switch chip. These cross-point strobe pulses are generated by U56 using 4-to-16 decoder/latch U78. The addressed switch toggles to the position defined by XPT_AD0 (high = switch on or low = switch off) when the cross-point strobe line pulses. [Audio System Board schematic diagram sheet 4.]

AUDIO OUTPUT CIRCUITS

All audio output signals from a C3 Maestro console system are sent out from the console by connectors and a terminal block at the Enhanced Audio Enclosure's rear panel. Interconnections between the Audio System Board's audio output circuits and the connectors and the terminal block at the rear panel are provided by the I/O Backplane Board. Audio outputs include signals such as headset earphone audio, speaker audio, balanced line audio to the CEC/IMC, and audio to a recorder. Recorder audio is applied to the 4-position terminal block and all other audio is applied to pins of the D-subminiature (DB) style connectors.

Supervisor Headset Earphone

Audio Matrix Switching

Using cross-point switch chips U40 and U49 in the audio matrix, microcontroller U56 selects the correct audio from an input circuit and sends it to the supervisor's headset earphones. Before it reaches a headset, audio is routed through the audio matrix twice – first through U49 and then through U40. Specifically, U49 can switch any of six (6) inputs to the SELECT_AUDIO line and then U40 is used to switch SELECT_AUDIO at U40 pin 6 to the supervisor's headset earphone (headphone) output circuit. [Audio System Board schematic diagram sheets 8, 16 & 20.]

Sidetone signals are only routed through the audio matrix once – operator sidetone (OPR_SIDETONE) via U40 pins 7 and supervisor sidetone (SUPR_SIDETONE) via U40 pin 22. In addition, audio from the Call Director's balanced line input circuit (originating from the telephone's "mic") can be switched to the supervisor's headset via U40 pin 23. [Audio System Board schematic diagram sheet 20.]

Summing And Limiter

The summing resistors on U40 pins 11 thru 14 sum the switched in audio signals from U40 and apply the summed signal to the input of a fast-limiter stage formed by op-amp U15 (pins 8, 9 & 10) and the associated components. Audio on the output of this stage at U15 pin 8 is clipped at approximately 5.9 Vp-p.

Low-Pass Filter

The audio is next applied to a active low-pass filter circuit formed by op-amp U15 (pins 5, 6 & 7) and the associated components. This stage greatly attenuates any high-frequency "hiss" which may have passed through the limiter stage.

Level Control

Next, the audio signal is ac-coupled via C88 to a digital pot within U9 (pins 11, 12 & 13). Under PC control, this digital pot (pot 25) sets the supervisor's earphone output level. See the section entitled "**DIGITAL POT CIRCUITS**" for circuit analysis details describing how the digital pots are adjusted. The attenuated signal on the digital pot's wiper, U9 pin 13, is applied to the input of the output buffer/amp stage.

Output Buffer/Amp

The signal on digital pot's wiper is ac-coupled to the supervisor headset earphone buffer/amp stage formed by U8 (pins 5, 6 and 7) and the associated components. This low-noise buffer/amp stage drives the earphones in the supervisor's headset via the SUPR_HEADPHONE_OUT line at J1 pin 68. R34 tailors the output impedance. No ac coupling capacitor is required since the op-amp's output is biased at a 0 Vdc potential. Connector J1 is one of the two 96-pin DIN connectors on the Audio System Board. It mates with J22 on the I/O Backplane Board.

SUPR_HEADPHONE_OUT is routed through the I/O Backplane Board to the female DB-9 connector on the I/O Backplane Board (J7 pin 7). This connector is labeled "SUPER H/S" on the rear panel. The cable from the supervisor's headset jack box mates with J7.

Operator Headset Earphone

Basically, the operator headset earphone output circuit is identical to the supervisor headset earphone output circuit described in the previous section. Therefore, this circuit will not be discussed in full detail. [Audio System Board schematic diagram sheet 20.]

On the Audio System Board, the signal from the operator headset earphone output circuit is applied to J1 pin 72. This signal is routed through the I/O Backplane Board to female DB-9 connector J6 at the rear panel. It is applied to J6 pin 7. This connector is labeled "OPER H/S". The cable from the operator's headset jack box mates with J6.

Operator headset volume adjustments are accomplished from the PC using a digital pot within U9 (pins 3, 4 & 5) on the Audio System Board. See the section entitled "**DIGITAL POT CIRCUITS**" for circuit analysis details describing how the digital pots are adjusted.

Line Outputs

All four (4) 600-ohm balanced line outputs from the Audio System Board are routed through the I/O Backplane Board and applied to connector J1 at the rear panel. This female DB-25 connector is labeled "LINES 1-4".

On the Audio System Board, the four line output circuits are basically identical, with the exception of component designators. Therefore, only the Line 1 output will be discussed in full detail. [Audio System Board schematic diagram sheets 14, 15, 22 and 23.]

Audio Matrix Switching

Cross-point switch chip U82 in the audio matrix switches audio to the Line 1 and Line 2 output circuits (LINE_1_OUT and LINE_2_OUT) and U81 switches audio to the Line 3 and Line 4 output circuits (LINE_3_OUT and LINE_4_OUT). Both U82 and U81 are controlled by microcontroller U56 as described in the section entitled "**AUDIO MATRIX CONTROL CIRCUITS**". [Audio System Board schematic diagram sheets 14 and 15.]

Summing and Amplification

For Line 1, summing resistors at U82 pins 15 thru 18 on the output side of the audio matrix sum one or more audio signals from the input circuits. This occurs when switches within U82 turn on. The summed signal is applied to a buffer/amp stage formed by op-amp U50 (pins 8, 9 & 10) and the associated components. This stage has a voltage gain of approximately two (2) or 6 dB at low frequencies. The capacitor in the op-amp's feedback loop provides a high-frequency roll-off of -3 dB at 7.2 kHz.

Level Adjustment and Buffer/Amp

Audio from op-amp U50 pin 8 is ac-coupled to a digital pot within U51 (pins 11, 12 & 13). This digital pot provides level adjustment for the Line 1 output. See the section entitled "**DIGITAL POT CIRCUITS**" for circuit analysis details describing how the digital pots are adjusted. C246 couples the attenuated signal on the pot's wiper, U51 pin 13, into a buffer/amp stage made from U50 (pins 12, 13 & 14) and the associated resistors. The signal on U50 pin 14 is ac-coupled to the line driver circuit via LINE_1_OUT [Audio System Board schematic diagram sheet 14.]

Line Drivers And Coupling

Dual low-noise op-amp U53 and the associated components form a differential line driver circuit which drives the non-line side of transformer T7. This is the Line 1 output 600-ohm coupling transformer. The upper op-amp (U53 pins 1, 2 & 3) operates as a inverting amplifier and itdrives one side of T7's winding. Its input signal is LINE_1_OUT from U50 pin 14. The lower op-amp (U53 pins 5, 6 & 7) drives the opposite side of the transformer's winding exactly 180 degrees out-of-phase. The output of the first op-amp (U53 pin 1) drives this stage. Both op-amps are wired for unity gain. Two suppressors within transient voltage suppressors TVS10 provide surge protection. [Audio System Board schematic diagram sheet 22.]

On the line or secondary side of T7, the balanced pair is identified as LINE_1_OUT+ and LINE_1_OUT- at J1 pins 32 and 64 respectively. This pair is routed through the I/O Backplane Board and applied to pins 14 and 15 of the female DB-25 connector labeled "LINES 1-4". This balanced line audio is applied to the Line 1 input of the Console Interface Module (CIM) within the CEC/IMC Digital Audio Switch.

Select Audio

Audio signals on the SELECT_AUDIO line are applied to the select speaker or a headset. In addition, these signals are also applied to the select recorder. In most cases, the signal source is the Line 1 input pair since the dispatcher will typically listen to audio from the console's currently selected entity (unit, group, etc.). This audio is transmitted to the console from the CIM via the CIM's channel/line 1. Other sources for SELECT_AUDIO include pager input audio during a page PTT, tones from the Audio System Board's tone generator circuits, Call Director balance line input audio, auxiliary audio and Line 1 output audio. The Line 1 output signal (LINE_1_OUT) is only switched in during certain test procedures. [Audio System Board schematic diagram sheet 16.]

Audio Matrix Switching and Summing

Cross-point switch chip U49 switches the audio sources (six possible) to the select audio output circuit. The resistors on the output of the audio matrix at U49 pins 13 thru 18 sum the switched-in signal(s) and apply the resultant summed signal to the following op-amp stage.

Amplification and Level Adjustment

The summed signal is applied to the input of a op-amp stage formed by U28 (pins 1, 2 & 3) and the associated components. Audio from the U28 pin 1 is ac-coupled to one digital pot within U12. This pot provides level adjustment for the SELECT_AUDIO line during alignment procedures. SELECT_AUDIO is set for 436 millivolt rms when an equal signal is present on one switched-in audio matrix input – for example LINE_1_IN audio at TP38 or U49 pin 6.

Output Buffer

The attenuated signal from the digital pot's wiper (U12 pin 13) is ac-coupled to a buffer circuit formed by op-amp U5 (pins 5, 6 & 7) and the associated resistors. The buffered signal at U5 pin 7 is applied to three (3) other audio matrix inputs via the capacitor C237 and the SELECT_AUDIO line. It is also summed into the input of the select recorder's audio output circuit via R125. [Audio System Board schematic diagram sheets 16, 20 and 21.]

Speakers

Speaker Assemblies used with the Enhanced Audio Enclosure employ internal speaker power amplifier circuits which amplify the low-power speaker audio signals from the Enhanced Audio Enclosure's Audio System Board. Each Speaker Assembly requires dc power from the Enhanced Audio Enclosure. Table 5 lists the possible audio sources for each speaker. See LBI-39104 for detailed information on the Speaker Assemblies.

Volume control for each speaker is accomplished via a mechanical pot at the Speaker Assembly, not a digital pot on the Audio System Board.

Select Speaker Output Buffer

The select speaker audio output circuit drives the speaker power amplifier circuit in the Speaker Assembly employed as the select speaker. This speaker is connected to the male DB-9 connector at the Enhanced Audio Enclosure's rear panel labeled "SEL SPKR".

When select audio must be applied to this speaker, microcontroller U56 switches SELECT_AUDIO at U49 pin 9 to the input of the select speaker output buffer circuit. The switched audio matrix output at U49 pin 11 is applied to the circuit's input at op-amp U7 pin 9. This stage provides a voltage gain of approximately 1.5 or 3.5 dB at low frequencies. A -3 dB roll-off is set by the capacitor in the op-amp's feedback loop. [Audio System Board schematic diagram sheet 16.]

Audio from U7 pin 8 is ac-coupled into a digital pot within U14 (pins 11, 12 & 13). This pot (pot 29) allows the select speaker's audio output level to be set during alignment procedures. The stage formed by op-amp U7 (pins 1, 2 & 3) and the associated components buffers the signal on the wiper of the digital pot (U14 pin 13) and it drives the SELECT_SPEAKER_OUT line. This audio is applied to the Speaker Assembly via the I/O Backplane Board interconnections and the connector labeled "SEL SPKR" at the rear panel (I/O Backplane Board connector J8). With a SELECT_AUDIO level of 436 millivolt rms, the digital pot is adjusted for an equal SELECT_SPEAKER_OUT output audio level. Surge protection for SELECT_SPEAKER_OUT is provided by a suppressor within transient voltage suppressor TVS2.

Unselect Speaker Output Buffer

The Audio System Board has a total of three (3) unselect speaker audio outputs. Like the select speaker audio output buffer circuit, each unselect speaker output buffer circuit drives the speaker's power amplifier circuit in its respective Speaker Assembly. All three circuits are basically identical and therefore only the unselect speaker 1 output circuit will be described. [Audio System Board schematic diagram sheets 17 and 18.]

Up to four (4) audio signals from four different audio matrix inputs can be summed by the resistors at cross-point switch chip U39 pins 15 thru 18. The summed signal is applied the inverting input of op-amp U7 at pin 13.

Op-amp U7 (pins 12, 13 & 14) amplifies the summed signal. High-frequency roll-off is provided by the capacitor in the feedback loop. The amplified signal is then ac-coupled to a digital pot within U14.

The digital pot within U14 (pins 3, 4 & 5) is used to set the output level of the unselect speaker 1 audio signal. This setting is accomplished during alignment procedures. The attenuated signal on the wiper (U14 pin 5) is applied to a non-inverting buffer stage formed by U7 (pins 5, 6 & 7) and the associated components. R25 and C21 couple the output signal at U7 pin 7 to the USELECT_SPEAKER_1_OUT line. This audio is applied to the Speaker Assembly via the I/O Backplane Board interconnections and the connector labeled "UNSEL SPKR1" at the rear panel (I/O Backplane Board connector J9). With a switched-in LINE_2_IN level of 436 millivolts rms, the digital pot is adjusted for an equal USELECT_SPEAKER_1_OUT level. Surge protection is provided by a suppressor within transient voltage suppressor TVS2.

Recorder Outputs

Recorder outputs are available on I/O Backplane Board terminal block J13 at the rear panel. This terminal block is labeled "RECORDER".

Two recorder outputs are provided by the Audio System Board – one for select audio and one for unselect audio. Normally, only audio on the SELECT_AUDIO line

Table 5 – Speaker Audio Sources

	LINE 1 IN	LINE 1 OUT	LINE 2 IN	LINE 2 OUT	LINE 3 IN	LINE 3 OUT	LINE 4 IN	LINE 4 OUT	CD IN	PAGER IN	AUX IN	TONE
SELECT	X	*							X	X	X	X
UNSELECT 1			X	*					X		X	
UNSELECT 2					X	*			X		X	
UNSELECT 3							X	*	X		X	

X = Possible audio connection.
* = Possible audio connection; typically only used during test purposes.

is sent out on the select recorder output. The unselect recorder output can send out Line 1 output audio and Line 2 thru 4 input audio. Both recorder outputs are basically identical; therefore, only the select output circuit will be described. [Audio System Board schematic diagram sheets 16 and 18.]

Resistors R124 and R125 provide a summing function for the SELECT_AUDIO and Line 1 output audio. The summed signal is applied to the inverting input of op-amp U5 (pins 8, 9 & 10). High-frequency roll-off is provided by the capacitor in the op-amp's feedback loop. [Audio System Board schematic diagram sheet 16.]

To allow recording of Call Director-related audio, operator mic audio may be switched in via the OPR_MIC_SWITCHED line from U80. Also, CD input audio from the Call Director (originating from the telephone's "mic") may be switched in via the CD_IN_SWITCHED line from U80. [Audio System Board schematic diagram sheets 16 & 19.]

Audio from U5 pin 8 is ac-coupled to one digital pot within U27. This pot (pot 21) provides level adjustment for the SELECT_RECORDER_OUT line during alignment procedures. It is set for 436 millivolt rms when an equal switched-in signal is applied to the audio matrix. [Audio System Board schematic diagram sheet 16.]

The attenuated signal from the digital pot's wiper (U27 pin 13) is ac-coupled to a buffer/amp circuit formed by op-amp U11 (pins 1, 2 & 3) and the associated components. The buffered signal at U11 pin 1 is coupled to the SELECT_RECORDER_OUTPUT line via R94, C56 and C33. SELECT_RECORDER_OUTPUT is routed through the I/O Backplane Board and applied to J13 terminal 3.

Call Director

As previously described in the Call Director audio input section, the C3 Maestro console system can be connected to a Call Director (CD) for CD radio patch telephone operations. When not being used for CD patch telephone communications, the dispatcher may also use the Call Director for local telephone (non-CD patch) operations.

Audio interfacing to a CD is performed by a 4-wire 600-ohm balanced line interface. On the Audio System Board, the CD output circuitry is very similar to the Line 1 output circuitry previously described. Audio on this pair is applied to the CD and it is heard by the land-line telephone user.

Audio Matrix Switching

Cross-point switch chip U80 in the audio matrix switches audio to the Call Director output circuit (CALL_DIRECTOR_OUT) as controlled by microprocessor U56. See the section entitled "**AUDIO MATRIX CONTROL CIRCUITS**" for specific details. [Audio System Board schematic diagram sheet 19.]

Summing And Amplification

The summing resistors at U80 pins 15 thru 18 on the output side of the audio matrix sum one or more audio signals from the audio input circuits. This occurs when switches within U80 turn on. Normally, only one signal is switched-in for summing. For example, during a CD radio patch operation, LINE_4_IN audio from the CEC/IMC at U80 pin 7 is switched in and, during local CD telephone operations, SUPR_MIC or OPR_MIC is switched in. The summed signal is applied to a buffer/amp stage formed by op-amp U18 (pins 5, 6 & 7) and the associated components. This stage has a voltage gain of approximately two (2) or 6 dB at low frequencies. The capacitor in the op-amp's feedback loop provides a high-frequency roll-off of approximately -3 dB at 7.2 kHz.

Level Adjustment and Output Buffer

Audio from op-amp U18 pin 7 is ac-coupled to a digital pot within U19 (pins 3, 4 & 5). This digital pot provides level adjustment for the CD output audio during alignment procedures performed at the PC. See the section entitled "**DIGITAL POT CIRCUITS**" for additional details. C96 couples the attenuated signal on the pot's wiper, U19 pin 5, into a buffer op-amp stage made from U18 (pins 1, 2 & 3) and the associated resistors. The signal on U18 pin 1 is coupled to the line driver circuit via the CALL_DIRECTOR_OUT line.

Line Drivers And Coupling

Dual low-noise op-amp U20 and the associated components form a differential line driver circuit which drives the non-line side of transformer T1. This is the CD output 600-ohm coupling transformer which sends audio to the Call Director. The upper op-amp (U20 pins 1, 2 & 3) operates as a inverting amplifier and it drives one side of T1's winding. Its input signal is CALL_DIRECTOR_OUT from U18 pin 1. The lower op-amp (U20 pins 5, 6 & 7) drives the opposite side of the transformer's winding exactly 180 degrees out-of-phase. The output of the first op-amp (U20 pin 1) drives this stage. Both op-amps are wired for unity gain. Two suppressors within transient voltage suppressors TVS6 provide surge protection. [Audio System Board schematic diagram sheet 30.]

On the line or secondary side of T1, the balanced pair is identified CALL_DIRECTOR_OUT+ and CALL_DIRECTOR_OUT- at J1 pins 22 and 54 respectively. This pair is routed through the I/O Backplane Board and applied to pins 7 and 8 of the DB-9 connector

labeled "CALL DIR". At the CEC/IMC, this audio is applied to the Line 4 input of the Console Interface Module (CIM).

A/D CONVERTER CIRCUIT

The Audio System Board is equipped with an analog-to-digital (A/D) converter circuit. During normal dispatch console operations this circuit is used to provide VU (Volume Unit) meter data to the PC so the C3 Maestro application program can display a VU indication. Various audio signal levels are switched-in and applied to the A/D converter's input as required. For example, when the dispatcher is transmitting, Line 1 output audio is applied to the circuit and converted to a digital value. This digital value is sent to the PC via the serial control data link between the Enhanced Audio Enclosure and the PC.

During automated test procedures, a test tone may be applied to the input of a particular audio circuit and the circuit's output can be monitored by the PC using the A/D converter circuit. Thus, a pass/fail indication can be displayed on the PC.

The A/D converter circuit basically consist of two op-amps within quad op-amp U28 and a 12-bit A/D converter chip, U38. The op-amps from a detector circuit which converts ac audio signal levels into proportional dc voltages. U38 monitors the proportional dc voltages and performs the actual analog-to-digital conversions. Microcontroller U56 reads the converted values. [Audio System Board schematic diagram sheets 6 and 21.]

Detector

The input of the detector circuit is located at op-amp U28 pin 10. Under U56 control, cross-point switch chips U61 and U62 are utilized to switch audio signals to this input through C160. Only one signal is switched in at a time. U28 (pins 8, 9 & 10) and the associated components rectify and integrate the audio signal, thus charging integrating capacitor C150. The second op-amp (U28 pins 12, 13 & 14) is wired as a voltage follower. It buffers the proportional dc voltage across C150 to generate the VU_METER dc voltage. VU_METER is applied to the input of the A/D converter chip. [Audio System Board schematic diagram sheet 21.]

A/D Converter

Integrated circuit U38 is a 12-bit analog-to-digital converter. VU_METER, the proportional dc voltage from the detector circuit, is applied to U38's analog input at pin 13.

Features of U38 include successive approximation conversions circuitry, an internal voltage reference, clock, and parallel interface circuitry. This 12-bit chip is interfaced to the 8-bit microcontroller via multiplexing; two microcontroller reads are necessary to read the 12-bit converted value. [Audio System Board schematic diagram sheet 6.]

Microcontroller U56's multiplexed address/data bus (AD0 thru AD7) is wired to U38's data output lines. Inside U38, these lines employ 3-state buffers which remain in a high-impedance state when the chip is not selected. When selected by U56, U38 outputs a digital value to the address/data bus (AD0 thru AD7). As shown on the schematic diagram, U38 is addressed in U56's memory mapped I/O space from 9000H to 9003H. U56 reads U38 approximately every 100 milliseconds.

RELAY OUTPUT CIRCUITS

Contacts

Seven (7) microprocessor-controlled relays on the Audio System Board provide relay contact-type outputs at the rear panel of the Enhanced Audio Enclosure. [Audio System Board schematic diagram sheets 26 and 27.]

Six of the seven relays, K1 thru K6, provide Form-C (single-pole double-throw) contacts for interfacing to external equipment. All of these contacts are available on terminal block J19 on the I/O Backplane Board. On the rear panel, this connector is labeled "RELAYS" and the first ("1") and last ("18") terminal numbers are indicated. See Table 6, LBI-39101 or LBI-39102 for specific J19 terminal details.

The seventh relay, K7, provides a Form-A (single-pole single-throw) relay contact connection for Call Director on-hook/off-hook status control. At the Enhanced Audio Enclosure's rear panel, these connections are located at the DB-9 connector labeled "CALL DIR" – connector J3 on the I/O Backplane Board. See Table 6, LBI-39101 or LBI-39102 for specific J3 pin-out details. This relay provides a momentary contact closure for automatically placing the CD on-hook without operator intervention. This "on-hook" relay is energized when the console disconnects the CD from the CEC/IMC due to operator manual operation or site time-out. Since most CDs do not have an on-hook input, use of this relay is optional.

Specified contact rating for all relays is 0.75 amps at 26 Vdc. Open contact isolation is specified to 500 Vrms (60 Hz). Isolation between any relay terminal and the Enhanced Audio Enclosure's ground is also specified to 500 Vrms (60 Hz).

Control

Seven TTL-level outputs from eight-bit addressable latch U42 control the seven NPN transistors which drive the relays' coils. These control logic lines are identified as RELAY_1 thru RELAY_7. A relay is energized (turned on) when its respective control logic line is high. [Audio System Board schematic diagram sheet 4.]

Microcontroller U56 writes relay on/off data to latch U42. U42's logic inputs include address logic lines A0 thru A2, address/data logic line AD0, and a decoded chip select logic line. The address logic lines are used to select which latch within U42 is written to. AD0 sets the relay on/off

Table 6 – Relay Outputs

CONSOLE ACTIVATION METHOD	AUDIO SYSTEM BOARD				I/O BACKPLANE BOARD
	RELAY	CONTACT TYPE (FORM)	SIGNAL NAME *	CONNECTOR J2 PIN NUMBER	CONNECTOR J19** PIN NUMBER
console PTT	K4	C	RELAY_1_NO	33	1
			RELAY_1_C	46	2
			RELAY_1_NC	5	3
Dispatch Keyboard <Alt><F10> (momentary action)	K5	C	RELAY_2_NO	77	4
			RELAY_2_C	70	5
			RELAY_2_NC	78	6
Dispatch Keyboard <Alt><F9> (toggle action)	K2	C	RELAY_3_NO	65	7
			RELAY_3_C	66	8
			RELAY_3_NC	3	9
(currently not supported by firmware)	K3	C	RELAY_4_NO	67	10
			RELAY_4_C	68	11
			RELAY_4_NC	69	12
(currently not supported by firmware)	K1	C	RELAY_5_NO	79	13
			RELAY_5_C	7	14
			RELAY_5_NC	81	15
(currently not supported by firmware)	K6	C	RELAY_6_NO	80	16
			RELAY_6_C	6	17
			RELAY_6_NC	47	18
Call Director on hook	K7	A	ON_HOOK_ COMMON	49	6**
			ON_HOOK_NO	48	1**

* "_NO" = normally-open contact; "_C" = common contact; "_NC" = normally-closed contact.
** Call Director on hook relay contacts are located at J3 on the I/O Backplane Board, not J19.

condition – low = relay off (coil not energized) and high = relay on (coil energized). When a relay is off, its normally-closed contacts are closed.

The decoded chip select logic line at U42 pin 14 ($\overline{\text{RELAY\_CS}}$) is a logical "OR" of the active-low RELAY_CS logic line from 3-to-8 line decoder U76 and the active-low RAMIOWR* line from microprocessor U56 via OR gate U75. As shown on the schematic diagram RELAY_CS is mapped to the E000H memory area. Therefore, to switch a relay, the microcontroller simply writes a data byte to an I/O location between E000H and E006H with the least-significant bit (AD0) of the written byte low to turn the relay off or high to turn the relay on. [Audio System Board schematic diagram sheets 2, 4 and 6.]

All relay coils are powered from the RELAY_V+ line which originates from either the +12V *or* the +5DIG supply lines depending upon coil voltages of the installed relays. Each relay has an NPN drive transistor that buffers its RELAY_x control line (RELAY_1 thru RELAY_7) from U42. To energize a relay's coil, the respective RELAY_x line is brought high by the microcontroller as described in the previous paragraph. This saturates the respective NPN transistor and energizes the relay's coil. The reversed-baised diode across each relay's coil suppresses reverse voltage (back-EMF) surges that appear across the coil at turn-off. [Audio System Board schematic diagram sheets 4, 26 and 27.]

As previously described, U42 is an 8-bit addressable latch that outputs the RELAY_1 thru RELAY_7 drive signals. For example, to turn relay K4 on, microcontroller U56 latches U42's Q0 output (RELAY_1) at pin 4 high. This turns transistor Q4 on which energizes K4. When K4 is energized, its normally-open (RELAY_1_NO) contact is connected to its common (RELAY_1_C) contact. See Table 6 for additional information.

TESTING

All Audio System Board tests presented in this section are accomplished with the board installed in the Enhanced Audio Enclosure. These procedures are primarily written to check basic audio signal path operation and signal level alignment of the audio circuits on the Audio System Board. In most cases, the related interconnections on the I/O Backplane Board are also tested.

RECOMMENDED TEST EQUIPMENT

The following list represents test equipment recommended for Audio System Board testing. Other test equipment may be substituted provided it is electrically equivalent or superior in accuracy and operational range to that which is listed.

- Personal Computer with C3 Maestro application software installed and configured in accordance with LBI-39101 and/or SRN-1000-xx
- Hewlett Packard 204C Audio Signal Generator (600-ohm output impedance) **or**
  Hewlett Packard 8111A Pulse/Function Generator (50-ohm output impedance)
- Fluke 87 True-RMS Handheld Digital Multimeter
- Tektronix 2205 Portable 20 MHz Analog Oscilloscope
- male DB-9 breakout/test point extender
- female DB-9 breakout/test point extender
- female DB-25 breakout/test point extender
- test leads, cables, etc.
- 600-ohm load resistors
- 47 µF (50-Volt minimum) non-polarized capacitor **or** two 100 µF (25-Volt minimum) polarized capacitors connected in series (+ to + or - to -) to form a non-polarized unit

WARNING

Hazardous voltages are present within the Enhanced Audio Enclosure when ac power is applied to the unit. Refer to the assembly diagram within LBI-39100 for specific areas.

INITIAL SET-UP

Cable Disconnections & Disassembly

- ❑ **DISCONNECT AC POWER from the Enhanced Audio Enclosure.**
- ❑ With the exception of the serial cable to/from the PC, disconnection of all other cables and wiring from the back of the Enhanced Audio Enclosure is recommended.
- ❑ Remove the Enhanced Audio Enclosure's top cover and front panel assembly in accordance with the disassembly procedure presented in LBI-39100.
- ❑ Verify the DIN connectors on the Audio System Board are fully mated with the DIN connectors on

the I/O Backplane Board. Full mating should occur when the ejector tabs on the front corners of the board are engaged in the sides of the unit and completely depressed. In some cases, it may be necessary to compress the Audio System Board to the I/O Backplane Board by grasping the Audio System Board and the rear panel and sqeezing the two together.

Power Supply Tests

- ❑ Apply ac power to the Enhanced Audio Enclosure and turn the power switch on the rear panel on. Verify the indicator light (typically green) within the switch is lit. If not, **remove ac power** and check both fuses in the ac power receptacle (IEC-320 type) on the rear panel. If necessary, refer to the parts list in LBI-39100 for fuse part number, voltage and current information.
- ❑ Verify the LED on the front of the Audio System Board is lit. This indicates the presence of +12 Vdc power on the Audio System Board. If it is not lit, there is most likely a blown fuse or problem with the switching power supply mounted to the bottom of the Enhanced Audio Enclosure's case. The power supply is a non-serviceable unit and it should be replaced if defective. The following steps should determine defective/non-defective status of a fuse or the power supply:
  1. **REMOVE AC POWER from the Enhanced Audio Enclosure.**
  2. Temporarily remove the Audio System Board.
  3. Reapply ac power.
  4. With the multimeter, **carefully** verify ac power is present at the power supply's ac input connector. Refer to the interconnection diagram within LBI-39100 as necessary.
  5. With the multimeter, **carefully** verify 12 Vdc power (±0.1 Vdc) is present at the I/O Backplane Board connector, J23 pin 1 (-) and pin 2 (+). If not, **remove ac power** and check the fuse located on the power supply's board. Some units may not be equipped with this on-board fuse.
  6. If the power supply's fuse and ac input are good and no dc power exists on its output, it should be considered defective and replaced. Refer to LBI-39100 for part number information.
- ❑ **REMOVE AC POWER from the Enhanced Audio Enclosure** and reinstall the Audio System Board.
- ❑ Reapply ac power.
- ❑ On the Audio System Board, verify +12 Vdc (±0.3 Vdc) is present on both leads of inductor L6. This inductor is one of the three large axial-lead inductors near DIN connector J2. Refer to the outline diagram in this manual for specfic location. Use TP7 (digital ground) as a ground reference. This test point is located near the three inductors. [Audio System Board schematic diagram sheet 1.]
- ❑ Verify +5 Vdc (±0.25 Vdc) is present on both leads of inductor L2. This inductor is one of the three large axial-lead inductors near DIN connector J2. Use TP7 (digital ground) as a ground reference. [Audio System Board schematic diagram sheet 7.]
- ❑ Verify +5 Vdc (±0.25 Vdc) is present on both leads of inductor L3. This inductor is one of the three large axial-lead inductors near DIN connector J2. Use TP23 (analog ground) as a ground reference. This test point is located near the center of the board. [Audio System Board schematic diagram sheet 7.]
- ❑ Verify -5 Vdc (±0.25 Vdc) is present on both leads of inductor L4. This inductor is one of the three large axial-lead inductors near DIN connector J2. TP23 (analog ground) should be used as a ground reference. [Audio System Board schematic diagram sheet 7.]

Establish Serial Link With PC And Dispatch Keyboard

- ❑ Interconnect the C3 Maestro's Personal Computer to the Enhanced Audio Enclosure in accordance with LBI-39101.
- ❑ Interconnect the Dispatch Keyboard to the Enhanced Audio Enclosure in accordance with LBI-39101.
- ❑ Power-up console system in accordance with the procedure in LBI-39101.
- ❑ Start the C3 Maestro application program in accordance with the procedure in LBI-39101.
- ❑ Verify the Enhanced Audio Enclosure is communicating with the PC over the RS-232 serial control data link. If this link is not operating the C3 Maestro's monitor will indicate an "Audio

subsystem link down on COMx" (normally, "x" = 2) message in the lower portion of the screen. Upon restoration of the serial link, an "Audio comm link error condition cleared " message is displayed.

- ❑ Verify the Dispatch Keyboard is operating by programming a communication module. Refer to the training/operator's manual as necessary.

AUDIO INPUT CIRCUITS

Supervisor Headset Mic Input

- ❑ At the female DB-9 connector labeled "SUPR H/S" on the rear panel, apply a 1 kHz tone to pin 9 through a 47 µF ac-coupling capacitor. This is connector J7 on the I/O Backplane Board. Use pin 5 as a signal ground. Initially set the signal generator for a 100 mVrms output level. Maintain minimum test lead length and use shielded test leads to prevent hum (i.e. 60 Hz) from being induced.
- ❑ Using TP23 on the Audio System Board as a ground reference, adjust the signal generator's output level for 100 mVrms at TP8 on the Audio System Board. [Audio System Board schematic diagram sheet 10.]
- ❑ Monitor the output of the supervisor headset mic input circuit at TP36. Verify the 1 kHz tone is 436 mVrms ±10%. With the scope, verify the 1 kHz tone at this test point is not distorted or clipping and it measures approximately 1.2 Vp-p.
- ❑ Verify the 1 kHz sidetone signal at TP25 is approximately 45 mVrms. With the scope, verify the signal at this test point is not distorted or clipping and it measures approximately 125 mVp-p. These signal levels will differ if the setting of digital pot 9 has changed from the factory setting given in LBI-39101.

NOTE

For typical digital pot settings and adjustment details, refer to LBI-39101. Digital pots applicable to the supervisor headset mic are pots 4, 7 and 9. DO NOT ADJUST any digital pot from the factory setting unless a full understanding of the consequences is known.

- ❑ Simulate an supervisor headset connection and PTT by, at the DB-9 connector, shorting pins 3 (sense) and 6 (PTT) to pin 4 (ground). Observe the VU meter on the monitor is indicating red. **If the C3 Maestro is connected to an operating CEC/IMC Digital Audio Switch, the 1 kHz tone will be broadcast on the selected entity (unit, group, conventional channel, etc.) assuming no Enhanced Audio Enclosure audio problems exists.**
- ❑ Remove all connections from the "SUPR H/S" connector.

Operator Headset Mic Input

- ❑ At the female DB-9 connector labeled "OPER H/S" on the rear panel, apply a 1 kHz tone to pin 9 through a 47 µF ac-coupling capacitor. This is connector J6 on the I/O Backplane Board. Use pin 5 as a signal ground. Maintain minimum test lead length and use shielded test leads.
- ❑ Using TP23 on the Audio System Board as a ground reference, adjust the signal generator's output level for 100 mVrms at TP4. [Audio System Board schematic diagram sheet 9.]
- ❑ Simulate an operator headset connection and PTT by, at the DB-9 connector, shorting pins 3 (sense) and 6 (PTT) to pin 4 (ground). Observe the VU meter on the monitor is indicating red. **If the C3 Maestro is connected to an operating CEC/IMC Digital Audio Switch, the 1 kHz tone will be broadcast on the selected entity (unit, group, conventional channel, etc.) assuming no Enhanced Audio Enclosure audio problems exists.**
- ❑ Monitor the output of the operator mic input circuit at TP34. Verify the 1 kHz tone is 436 mVrms ±10%. With the scope, verify the 1 kHz tone at this test point is not distorted or clipping and it measures approximately 1.2 Vp-p. [Audio System Board schematic diagram sheet 11.]
- ❑ Verify the sidetone signal at TP29 is approximately 45 mVrms. With the scope, verify the signal at this test point is not distorted or clipping and it measures approximately 125 mVp-p. These signal levels will differ if the setting of digital pot 10 has changed from the factory setting given in LBI-39101.

NOTE

For typical digital pot settings and adjustment details, refer to LBI-39101. Digital pots applicable to the operator headset mic are pots 3, 8 and 10. DO NOT ADJUST any digital pot from the factory setting unless a full understanding of the consequences is known.

- ❑ Remove all connections from the "OPER H/S" connector.

Desk Mic Input

- ❑ At the female DB-9 connector labeled "DESK MIC" on the rear panel, apply a 1 kHz tone to pin 9 through a 47 µF ac-coupling capacitor. This is connector J5 on the I/O Backplane Board. Use pin 5 as a signal ground. Maintain minimum test lead length and use shielded test leads.
- ❑ Using TP23 on the Audio System Board as a ground reference, adjust the signal generator's output level for 71 mVrms at TP5. [Audio System Board schematic diagram sheet 9.]
- ❑ Simulate a desk mic PTT by, at the DB-9 connector, shorting pin 6 (PTT) to pin 4 (ground). No other mics (headsets, boom or gooseneck) should be connected to the Enhanced Audio Enclosure. Observe the VU meter on the monitor is indicating red. **If the C3 Maestro is connected to an operating CEC/IMC Digital Audio Switch, the 1 kHz tone will be broadcast on the selected entity (unit, group, conventional channel, etc.) assuming no Enhanced Audio Enclosure audio problems exists.**
- ❑ Monitor the output of the operator mic input circuit at TP34. Verify the 1 kHz tone is 436 mVrms ±10%. With the scope, verify the 1 kHz tone at this test point is not distorted or clipping and it measures approximately 1.2 Vp-p. [Audio System Board schematic diagram sheet 11.]

NOTE

For typical digital pot settings and adjustment details, refer to LBI-39101. Digital pots applicable to the desk mic are pots 6, 8 and 10. DO NOT ADJUST any digital pot from the factory setting unless a full understanding of the consequences is known.

- ❑ Remove all connections from the "DESK MIC" connector.

Boom/Gooseneck Mic Input

- ❑ At the female DB-9 connector labeled "B/G MIC" on the rear panel, apply a 1 kHz tone to pin 9. This is connector J4 on the I/O Backplane Board. Initially set the signal generator's output level to 10 mVrms or lower. A 10:1 (or greater) resistive attenuator network may be necessary if the audio signal generator being used will not output low signal levels such as this and/or it has a poor signal-to-noise ratio. If an attenuator network is used, impedance matching is not necessary. Use pin 5 as a signal ground. Maintain minimum test lead length and use shielded test leads to prevent hum (i.e. 60 Hz) from being induced in this high-gain mic input.
- ❑ Using TP23 on the Audio System Board as a ground reference, adjust the signal generator's output level for 5 mVrms at TP6. [Audio System Board schematic diagram sheet 9.]
- ❑ Simulate a boom/gooseneck mic connection and PTT by, at the DB-9 connector, shorting pins 3 (sense) and 6 (PTT) to pin 4 (ground). No headsets should be connected to the Enhanced Audio Enclosure at this time. Observe the VU meter on the monitor is indicating red. **If the C3 Maestro is connected to an operating CEC/IMC Digital Audio Switch, the 1 kHz tone will be broadcast on the selected entity (unit, group, conventional channel, etc.) assuming no Enhanced Audio Enclosure audio problems exists.**
- ❑ Monitor the output of the operator mic input circuit at TP34. Verify the 1 kHz tone is 436 mVrms ±10%. With the scope, verify the 1 kHz tone at this test point is not distorted or clipping and it measures approximately 1.2 Vp-p. [Audio System Board schematic diagram sheet 11.]

NOTE

For typical digital pot settings and adjustment details, refer to LBI-39101. Digital pots applicable to the boom/gooseneck mic are pots 5, 8 and 10. DO NOT ADJUST any digital pot from the factory setting unless a full understanding of the consequences is known.

- ❑ Remove all connections from the "B/G MIC" connector.

Line Inputs

NOTE

For typical digital pot settings and adjustment details, refer to LBI-39101. Applicable pots are 11 (Line 1), 12 (Line 2), 17 (Line 3) and 18 (Line 4). DO NOT ADJUST any digital pot from the factory setting unless a full understanding of the consequences is known.

Line 1 Input

- ❑ At the female DB-25 connector labeled "LINES 1-4" on the rear panel, apply a 436 mVrms (-5 dBm @ 600 ohms) 1 kHz tone between pins 1 and 2 (balanced input). This is connector J1 on the I/O Backplane Board.
- ❑ Verify the 436 mVrms 1 kHz tone is present between TP56 and TP57 on the Audio System Board. [Audio System Board schematic diagram sheet 12.]
- ❑ Using TP23 as a ground reference, monitor the output of the Line 1 input circuit at TP38. Verify the 1 kHz tone is 436 mVrms ±10%. With the scope, verify the 1 kHz tone at this test point is not distorted or clipping and it measures approximately 1.2 Vp-p.

Line 2 Input

- ❑ At the "LINES 1-4" female DB-25 connector, apply a 436 mVrms 1 kHz tone between pins 4 and 5.
- ❑ Verify the 436 mVrms 1 kHz tone is present between TP54 and TP55. [Audio System Board schematic diagram sheet 12.]
- ❑ Using TP23 as a ground reference, monitor the output of the Line 2 input circuit at TP39. Verify the 1 kHz tone is 436 mVrms ±10%. With the scope, verify the 1 kHz tone at this test point is not distorted or clipping and it measures approximately 1.2 Vp-p.

Line 3 Input

- ❑ At the "LINES 1-4" female DB-25 connector, apply a 436 mVrms 1 kHz tone between pins 7 and 8.
- ❑ Verify the 436 mVrms 1 kHz tone is present between TP52 and TP53. [Audio System Board schematic diagram sheet 13.]
- ❑ Using TP23 as a ground reference, monitor the output of the Line 3 input circuit at TP35. Verify the 1 kHz tone is 436 mVrms ±10%. With the scope, verify the 1 kHz tone at this test point is not distorted or clipping and it measures approximately 1.2 Vp-p.

Line 4 Input

- ❑ At the "LINES 1-4" female DB-25 connector, apply a 436 mVrms 1 kHz tone between pins 10 and 11.
- ❑ Verify the 436 mVrms 1 kHz tone is present between TP50 and TP51. [Audio System Board schematic diagram sheet 13.]
- ❑ Using TP23 as a ground reference, monitor the output of the Line 4 input circuit at TP37. Verify the 1 kHz tone is 436 mVrms ±10%. With the scope, verify the 1 kHz tone at this test point is not distorted or clipping and it measures approximately 1.2 Vp-p.

Call Director Input

- ❑ At the female DB-9 connector on the rear panel labeled "CALL DIR", apply a 78 mVrms (-20 dBm @ 600 ohms) 1 kHz tone between pins 5 and 9 (balanced input). This is connector J3 on the I/O Backplane Board.
- ❑ On the Audio System Board, verify the 78 mVrms 1 kHz tone is present between TP12 and TP13. [Audio System Board schematic diagram sheet 8.]
- ❑ Using TP23 as a ground reference, monitor the output of the Call Director input circuit at TP15. Verify the 1 kHz tone is 436 mVrms ±10%. With the scope, verify tone is not distorted or clipping and it measures approximately 1.2 Vp-p.

NOTE

For typical digital pot settings and adjustment details, refer to LBI-39101. The digital pot applicable to the Call Director input is pot 1. DO NOT ADJUST any digital pot from the factory setting unless a full understanding of the consequences is known.

Pager Input

- ❑ At the 4-position terminal block on the rear panel labeled "PAGING", apply a 436 mVrms (-5 dBm @ 600 ohms) 1 kHz tone between terminals 1 and

2 (balanced input). This is connector J2 on the I/O Backplane Board.

- ❑ On the Audio System Board, verify the 436 mVrms 1 kHz tone is present between TP40 and TP41. [Audio System Board schematic diagram sheet 8.]
- ❑ Using TP23 as a ground reference, monitor the output of the pager input circuit at TP14. Verify the 1 kHz tone is 436 mVrms ±10%. With the scope, verify the tone is not distorted or clipping and it measures approximately 1.2 Vp-p.

NOTE

For typical digital pot settings and adjustment details, refer to LBI-39101. The digital pot applicable to the pager input is pot 28. DO NOT ADJUST any digital pot from the factory setting unless a full understanding of the consequences is known.

AUDIO OUTPUT CIRCUITS

Supervisor Headset Earphone Output

- ❑ Apply 1 kHz tone to the Line 1 input in accordance with the test procedure entitled "**Line Inputs**", subsection "**Line 1 Input**" (page 31). At TP38 on the Audio System Board, verify the 1 kHz tone is present at a 436 mVrms level. Use TP23 as a ground reference.
- ❑ At the female DB-9 connector labeled "SUPR H/S" on the rear panel, simulate a supervisor headset connection by shorting pin 3 (sense) to pin 4 (ground). This is connector J7 on the I/O Backplane Board. The C3 Maestro's monitor should indicate "HSET" in the "**STATUS**" area of the screen.
- ❑ Verify the 1 kHz tone is present at TP32 on the Audio System Board at a level of 436 mVrms ±10%. Use TP23 as a ground reference. This is the select audio signal on the Audio System Board. [Audio System Board schematic diagram sheet 16.]
- ❑ Using TP23 as a ground reference, monitor the level of the 1 kHz tone at TP30. This is the output of the supervisor headset earphone output circuit. Signal level should be 100 mVrms ±10% with no load on the output. An equal signal should appear across pins 7 (out) and 8 (ground) at the DB-9. With the scope, verify the 1 kHz tone is not distorted or clipping and it measures approximately 280 mVp-p. Levels will differ if the setting of digital pot 25 has changed from the factory setting given in LBI-39101. [Audio System Board schematic diagram sheet 20.]
- ❑ If the following operator headset earphone test will be performed, maintain the 1 kHz tone injection into the Line 1 input.

NOTE

For typical digital pot settings and adjustment details, refer to LBI-39101. The digital pot applicable to the supervisor headset earphone output is pot 25. DO NOT ADJUST any digital pot from the factory setting unless a full understanding of the consequences is known.

Operator Headset Earphone Output

- ❑ Apply 1 kHz tone to the Line 1 input in accordance with the test procedure entitled "**Line Inputs**", subsection "**Line 1 Input**" (page 31). At TP38 on the Audio System Board, verify the 1 kHz tone is present at a 436 mVrms level. Use TP23 as a ground reference.
- ❑ At the female DB-9 connector labeled "OPER H/S" on the rear panel, simulate a operator headset connection by shorting pin 3 (sense) to pin 4 (ground). This is connector J6 on the I/O Backplane Board. The C3 Maestro's monitor should indicate "HSET" in the "**STATUS**" area of the screen.
- ❑ Verify the 1 kHz tone is present at TP32 on the Audio System Board at a level of 436 mVrms ±10%. Use TP23 as a ground reference. This is the select audio signal on the Audio System Board. [Audio System Board schematic diagram sheet 16.]
- ❑ Using TP23 as a ground reference, monitor the level of the 1 kHz tone at TP18. This is the output of the operator headset earphone output circuit. Signal level should be 100 mVrms ±10% with no load on the output. An equal signal should appear across pins 7 (out) and 8 (ground) at the DB-9. With the scope, verify the 1 kHz tone is not distorted or clipping and it measures approximately 280 mVp-p. Levels will differ if the setting of digital pot 26 has changed from the factory setting given in LBI-39101. [Audio System Board schematic diagram sheet 20.]

❑ If the following select speaker output test will be performed, maintain the 1 kHz tone injection into the Line 1 input.

NOTE

For typical digital pot settings and adjustment details, refer to LBI-39101. The digital pot applicable to the operator headset earphone output is pot 26. DO NOT ADJUST any digital pot from the factory setting unless a full understanding of the consequences is known.

Select Speaker Output

❑ Apply 1 kHz tone to the Line 1 input in accordance with the test procedure entitled "**Line Inputs**", subsection "**Line 1 Input**" (page 31). At TP38 on the Audio System Board, verify the 1 kHz tone is present at a 436 mVrms level. Use TP23 as a ground reference.

❑ Disconnect all headsets from the Enhanced Audio Enclosure. With no headsets connected, Line 1 input audio is switched to the select audio line on the Audio System Board and this signal is then applied to the select speaker output circuit.

❑ Verify the 1 kHz tone is present at TP32 on the Audio System Board at a level of 436 mVrms ±10%. Use TP23 as a ground reference. This is the select audio signal on the Audio System Board. [Audio System Board schematic diagram sheet 16.]

❑ Using TP23 as a ground reference, monitor the level of the 1 kHz tone at TP19. This is the output of the select speaker output circuit. Signal level should be 436 mVrms ±10% with no load on the speaker output or approximately 360 mVrms with a speaker connected. An equal signal should appear across pins 1 and 2 of the "SEL SPKR" DB-9 connector on the rear panel. This is connector J8 on the I/O Backplane Board. With the scope, verify the 1 kHz tone is not distorted or clipping and it measures approximately 1.2 Vp-p with no select speaker load.

NOTE

For typical digital pot settings and adjustment details, refer to LBI-39101. The digital pot applicable to the select speaker output is pot 29. DO NOT ADJUST any digital pot from the factory setting unless a full understanding of the consequences is known.

Unselect Speaker Outputs

Unselect Speaker 1

❑ Apply 1 kHz tone to the Line 2 input in accordance with the test procedure entitled "**Line Inputs**", subsection "**Line 2 Input**" (page 31). At TP39 on the Audio System Board, verify the 1 kHz tone is present at a 436 mVrms level. Use TP23 as a ground reference.

❑ Monitor TP20 on the Audio System Board for the 1 kHz tone at a level of 436 mVrms ±10% with no load on the speaker output or approximately 360 mVrms with a speaker connected. This is the output of the unselect speaker 1 output circuit. An equal signal should appear across pins 1 and 2 of the "UNSEL SPKR1" male DB-9 connector on the rear panel. This is connector J9 on the I/O Backplane Board. With the scope, verify the 1 kHz tone is not distorted or clipping and it measures approximately 1.2 Vp-p with no unselect speaker load. [Audio System Board schematic diagram sheet 17.]

Unselect Speaker 2

❑ Apply 1 kHz tone to the Line 3 input in accordance with the test procedure entitled "**Line Inputs**", subsection "**Line 3 Input**" (page 31). At TP35 on the Audio System Board, verify the 1 kHz tone is present at a 436 mVrms level. Use TP23 as a ground reference.

❑ Monitor TP22 on the Audio System Board for the 1 kHz tone at a level of 436 mVrms ±10% with no load installed or approximately 360 mVrms with a speaker connected. This is the output of the unselect speaker 2 output circuit. An equal signal should appear across pins 1 and 2 of the "UNSEL SPKR2" male DB-9 connector on the rear panel. This is connector J10 on the I/O Backplane Board. With the scope, verify the 1 kHz tone is not distorted or clipping and it measures approximately 1.2 Vp-p with no unselect speaker load. [Audio System Board schematic diagram sheet 17.]

Unselect Speaker 3

❑ Apply 1 kHz tone to the Line 4 input in accordance with the test procedure entitled "**Line Inputs**", subsection "**Line 4 Input**" (page 31). At TP37 on the Audio System Board, verify the 1 kHz tone is present at a 436 mVrms level. Use TP23 as a ground reference.

- ❑ Monitor U6 pin 7 for the 1 kHz tone at a level of 436 mVrms ±10% with no load installed or approximately 360 mVrms with a speaker connected. This is the output of the unselect speaker 3 output circuit. An equal signal should appear across pins 1 and 2 of the "UNSEL SPKR3" male DB-9 connector on the rear panel. This is connector J11 on the I/O Backplane Board. With the scope, verify the 1 kHz tone is not distorted or clipping and it measures approximately 1.2 Vp-p with no unselect speaker load. [Audio System Board schematic diagram sheet 18.]

NOTE

For typical digital pot settings and adjustment details, refer to LBI-39101. Applicable digital pots are 30 (unselect 1), 23 (unselect 2) and 24 (unselect 3). DO NOT ADJUST any digital pot from the factory setting unless a full understanding of the consequences is known.

Line Outputs

Line 1 Output

- ❑ Apply 1 kHz tone to the operator headset mic input circuit in accordance with the test procedure entitled "**Operator Headset Mic Input**" (page 29). Simulate an operator connection and PTT as described in the test procedure section. At TP34 on the Audio System Board, verify the 1 kHz tone is present at a 436 mVrms level. Use TP23 as a ground reference. Observe the VU meter on the monitor is indicating red. **If the C3 Maestro is connected to an operating CEC/IMC Digital Audio Switch, the 1 kHz tone will be broadcast on the selected entity (unit, group, conventional channel, etc.) assuming no Enhanced Audio Enclosure audio problems exists.**
- ❑ At the "LINES 1-4" female DB-25 connector on the rear panel, load the Line 1 output by installing a 600-ohm resistor between pins 14 and 15. This DB-25 connector is J1 on the I/O Backplane Board.
- ❑ Monitor the 1 kHz tone level between TP48 and TP49 on the Audio System Board. A signal level of 436 mVrms ±10% should exist. An equal signal should exist across the 600-ohm load resistor. With the scope, verify the signal is not distorted or clipping and it measures approximately 1.2 Vp-p. [Audio System Board schematic diagram sheet 22.]
- ❑ If the following Line 4 output test will be performed, maintain the 1 kHz tone injection into the operator mic input.

Line 4 Output

- ❑ Apply 1 kHz tone to the operator headset mic input circuit in accordance with the test procedure entitled "**Operator Headset Mic Input**" (page 29).
- ❑ Simulate an operator headset connection by shorting pin 3 (sense) to pin 4 (ground) at the "OPR MIC" DB-9 connector. A PTT is not necessary. Using TP23 on the Audio System Board as a ground reference, verify the 1 kHz tone is present at TP34 at level of 436 mVrms ±10%.
- ❑ At the "LINES 1-4" female DB-25 connector on the rear panel, load the Line 4 output by installing a 600-ohm resistor between pins 23 and 24. This DB-25 connector is J1 on the I/O Backplane Board.
- ❑ From the Dispatch Keyboard's numeric keypad, enter <Alt>], 2041 and then press <Enter>. This turns a switch on inside the audio matrix which routes operator headset mic audio to the Line 4 output circuit.
- ❑ Monitor the 1 kHz tone level between TP42 and TP43 on the Audio System Board. A signal level of 436 mVrms ±10% should exist. An equal signal should exist across the 600-ohm load resistor. With the scope, verify the signal is not distorted or clipping and it measures approximately 1.2 Vp-p. [Audio System Board schematic diagram sheet 23.]
- ❑ From the Dispatch Keyboard's numeric keypad, enter <Alt>], 2040 and then press <Enter>. This turns the switch off.

NOTE

For typical digital pot settings and adjustment details, refer to LBI-39101. Applicable digital pots are 15 (Line 1 output) and 14 (Line 4 output). DO NOT ADJUST any digital pot from the factory setting unless a full understanding of the consequences is known.

Recorder Outputs

Select Recorder

- ❑ Apply 1 kHz tone to the Line 1 input in accordance with the test procedure entitled "**Line Inputs**", subsection "**Line 1 Input**" (page 31). At TP38 on the Audio System Board, verify the 1 kHz tone is present at a 436 mVrms level. Use TP23 as a ground reference.
- ❑ Verify the 1 kHz tone is present at TP32 on the Audio System Board at a level of 436 mVrms ±10%. Use TP23 as a ground reference. This is the select audio signal on the Audio System Board. [Audio System Board schematic diagram sheet 16.]
- ❑ At the 4-position terminal block on the rear panel labeled "RECORDER", load the select recorder output by installing a 600-ohm resistor between terminals 3 and 4. This terminal block is J13 on the I/O Backplane Board.
- ❑ Using TP23 as a ground reference, monitor the level of the 1 kHz tone at TP21. This is the output of the select recorder output circuit. Signal level should be 436 mVrms ±10%. An equal signal should appear across the 600-ohm resistor at terminals 3 (out) and 4 (ground) of the terminal block. With the scope, verify the 1 kHz tone is not distorted or clipping and it measures approximately 1.2 Vp-p.

Unselect/Telephone Recorder

- ❑ Apply 1 kHz tone to the Line 2 input in accordance with the test procedure entitled "**Line Inputs**", subsection "**Line 2 Input**" (page 31). At TP39 on the Audio System Board, verify the 1 kHz tone is present at a 436 mVrms level. Use TP23 as a ground reference.
- ❑ At the 4-position terminal block on the rear panel labeled "RECORDER", load the unselect/telephone recorder output by installing a 600-ohm resistor between terminals 1 (out) and 2 (ground). This terminal block is J13 on the I/O Backplane Board.
- ❑ Monitor the level of the 1 kHz tone across the 600-ohm load resistor. Signal level should be 436 mVrms ±10%. With the scope, verify the tone is not distorted or clipping and it measures approximately 1.2 Vp-p.

NOTE

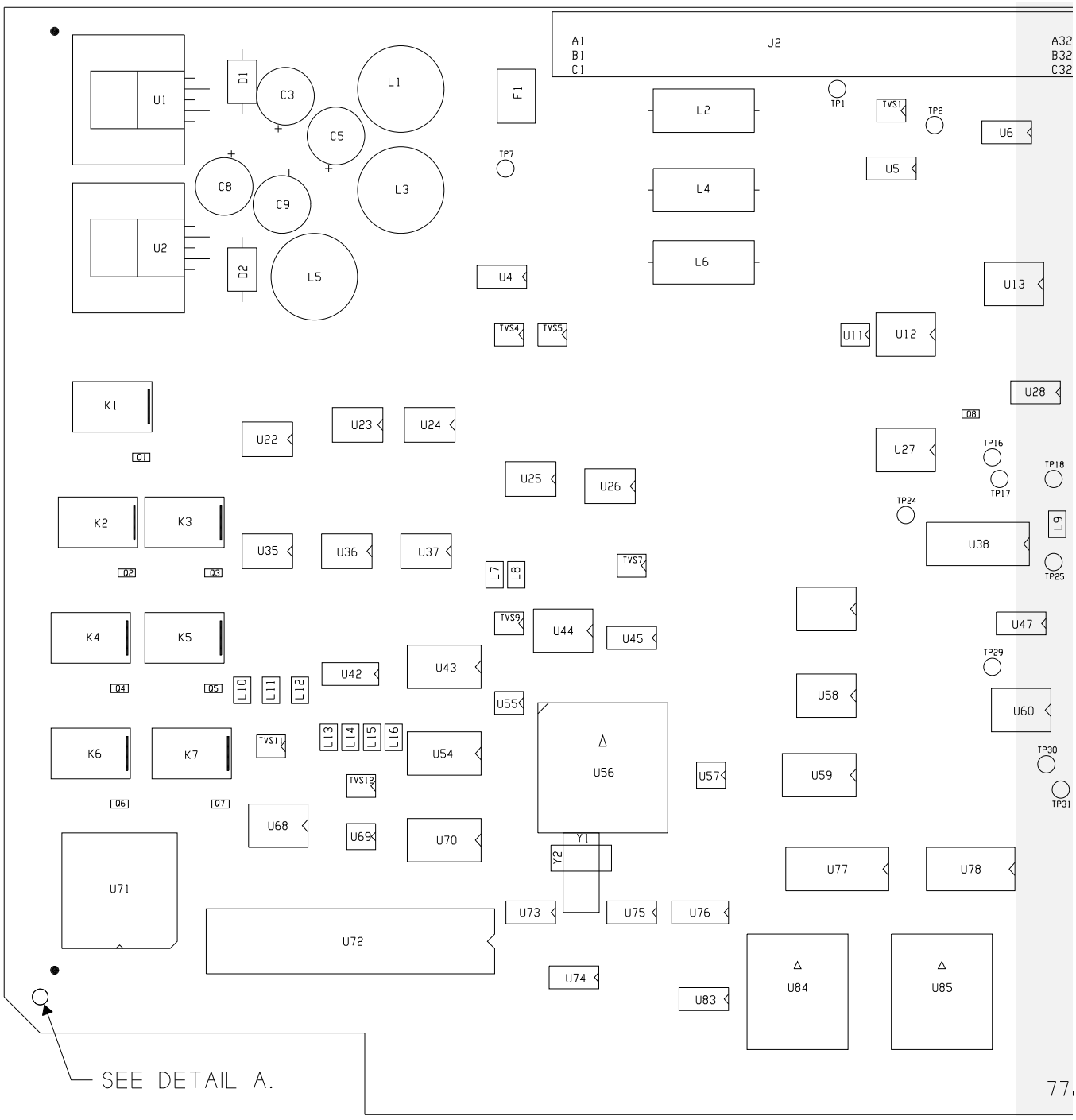
For typical digital pot settings and adjustment details, refer to LBI-39101. Applicable digital pots are 21 (select recorder) and 22 (unselect/telephone recorder). DO NOT ADJUST any digital pot from the factory setting unless a full understanding of the consequences is known.

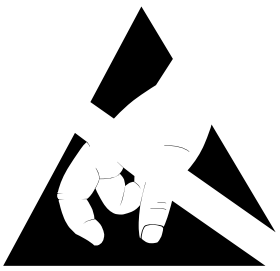
Call Director Output

- ❑ Apply 1 kHz tone to the Line 4 input in accordance with the test procedure entitled "**Line Inputs**", subsection "**Line 4 Input**" (page 31). At TP37 on the Audio System Board, verify the 1 kHz tone is present at a 436 mVrms level. Use TP23 as a ground reference.
- ❑ At the "CALL DIR" female DB-9 connector on the rear panel, load the Call Director line output by installing a 600-ohm resistor between pins 7 and 8 (balanced output). This DB-9 connector is J3 on the I/O Backplane Board.
- ❑ From the Dispatch Keyboard's numeric keypad, enter <Alt>], 6221 and then press <Enter>. This turns a switch on inside the audio matrix which routes Line 4 input audio to the Call Director line output circuit. [Audio System Board schematic diagram sheet 19.]
- ❑ Monitor the 1 kHz tone level between TP10 and TP11 on the Audio System Board. A signal level of 436 mVrms ±10% should exist. An equal signal should exist across the 600-ohm load resistor. With the scope, verify the signal is not distorted or clipping and it measures approximately 1.2 Vp-p. [Audio System Board schematic diagram sheet 30.]

NOTE

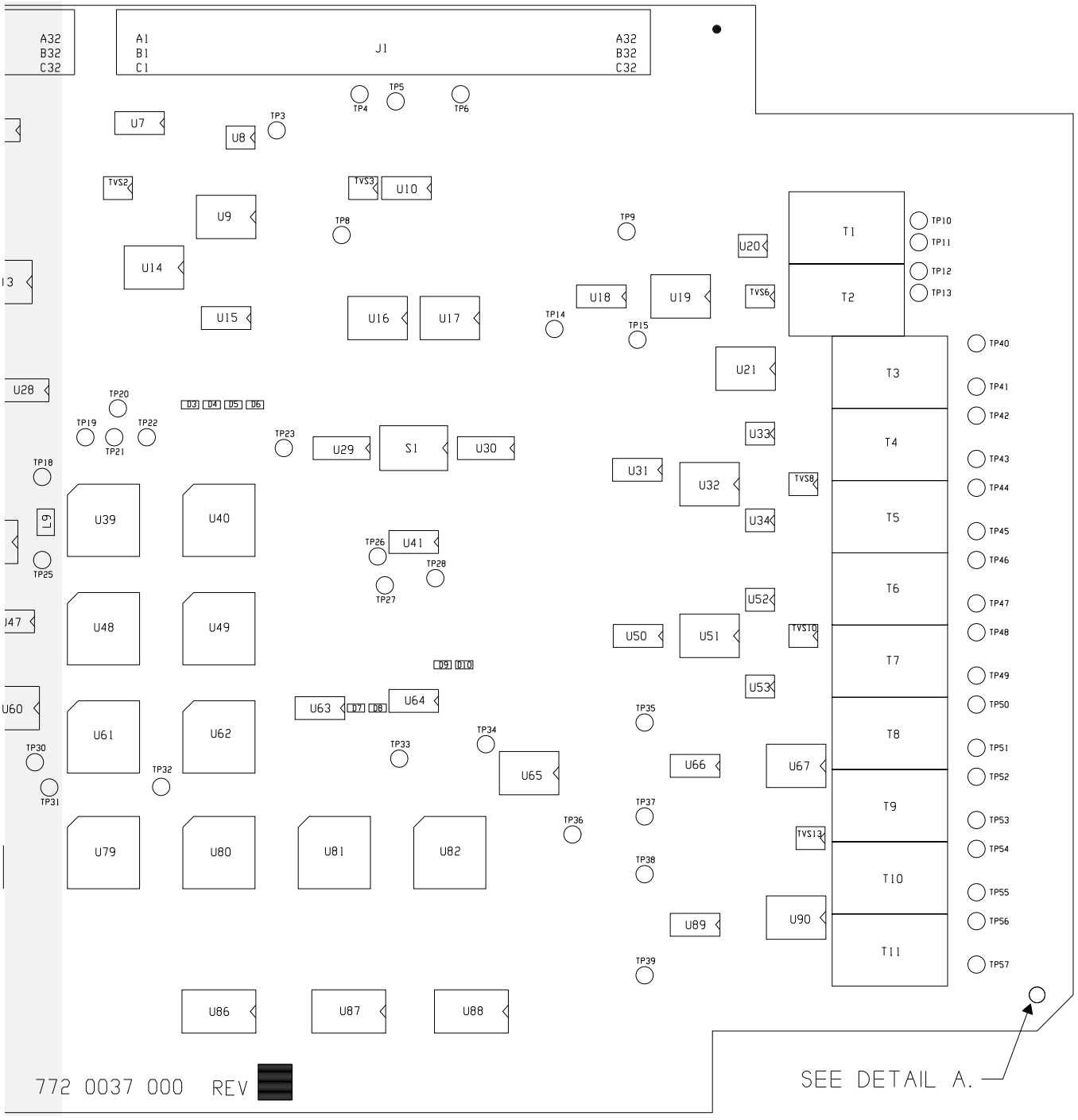
For typical digital pot settings and adjustment details, refer to LBI-39101. Digital pot 2 adjusts the Call Director output audio level.

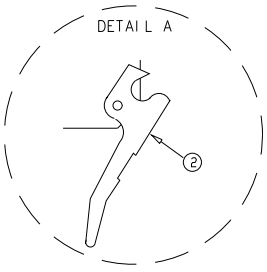




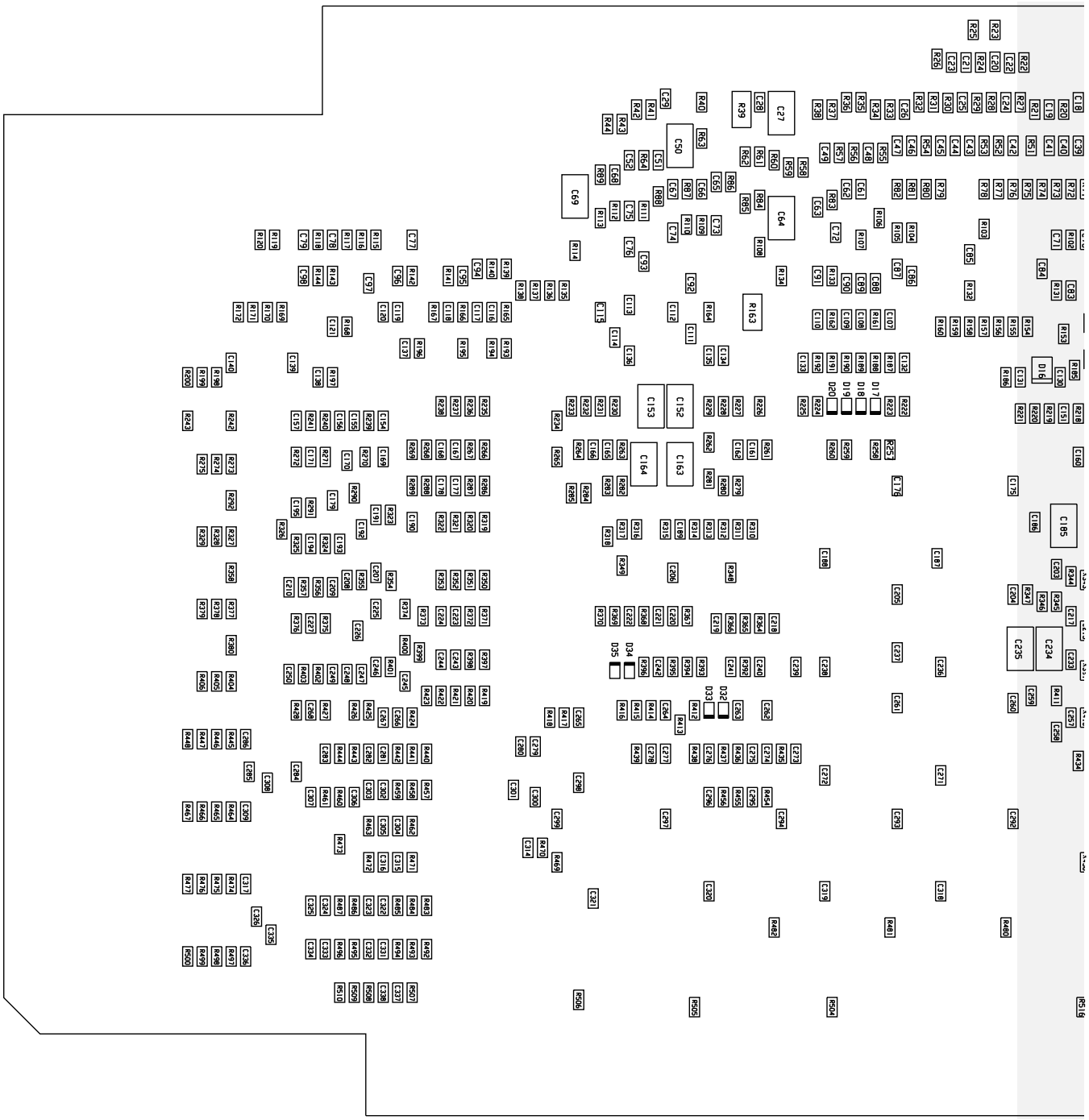
CAUTION

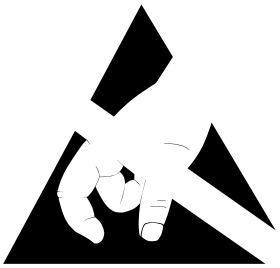
OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES





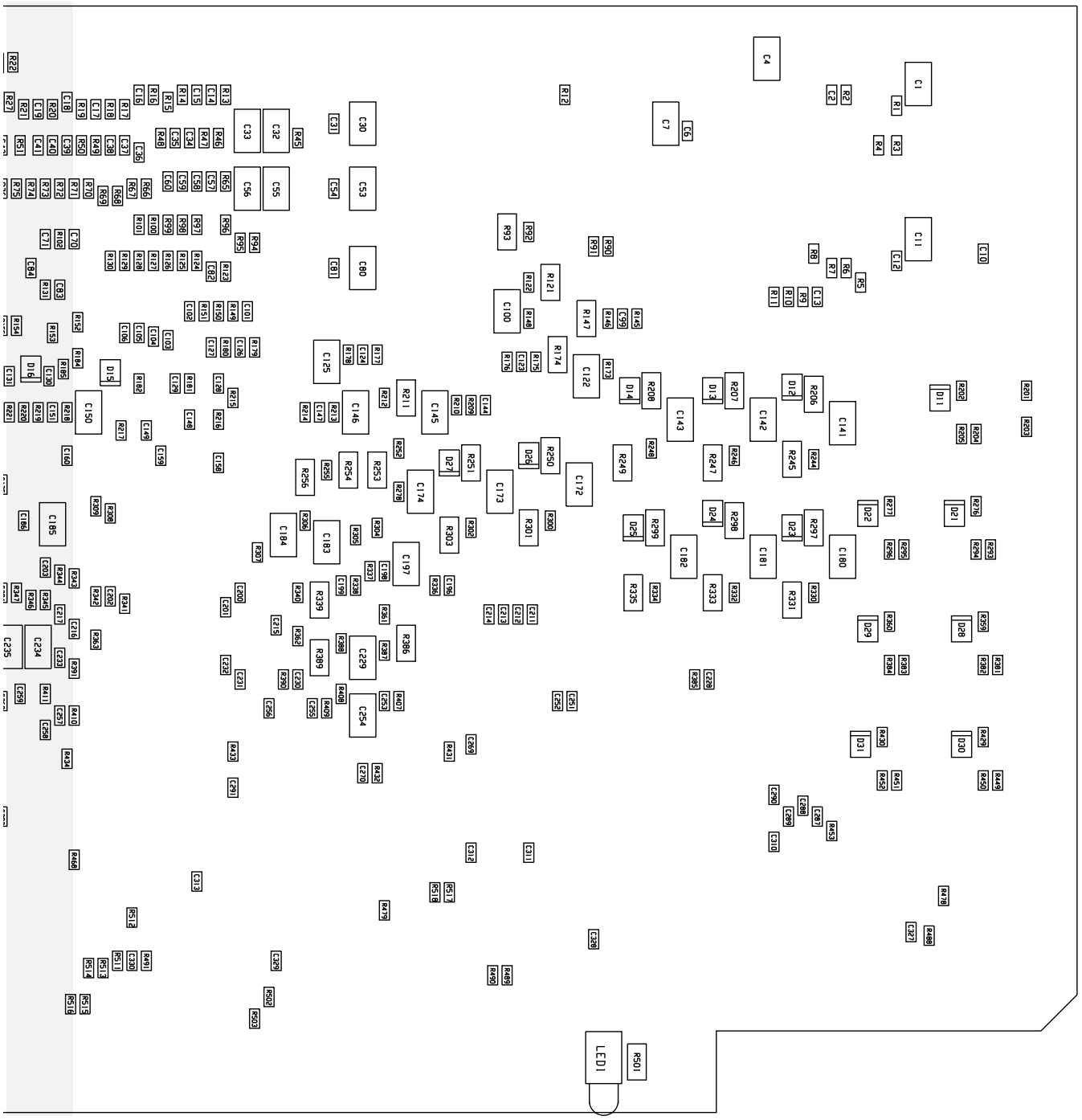
AUDIO SYSTEM BOARD
P29/7720037000
Component (Upper) Side
(772-0037-XXX-HD, Sh. 1, Rev. A)





CAUTION

OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES



AUDIO SYSTEM BOARD
P29/7720037000
Chip Component (Lower) Side
(772-0037-XXX-HD, Sh. 1, Rev. A)

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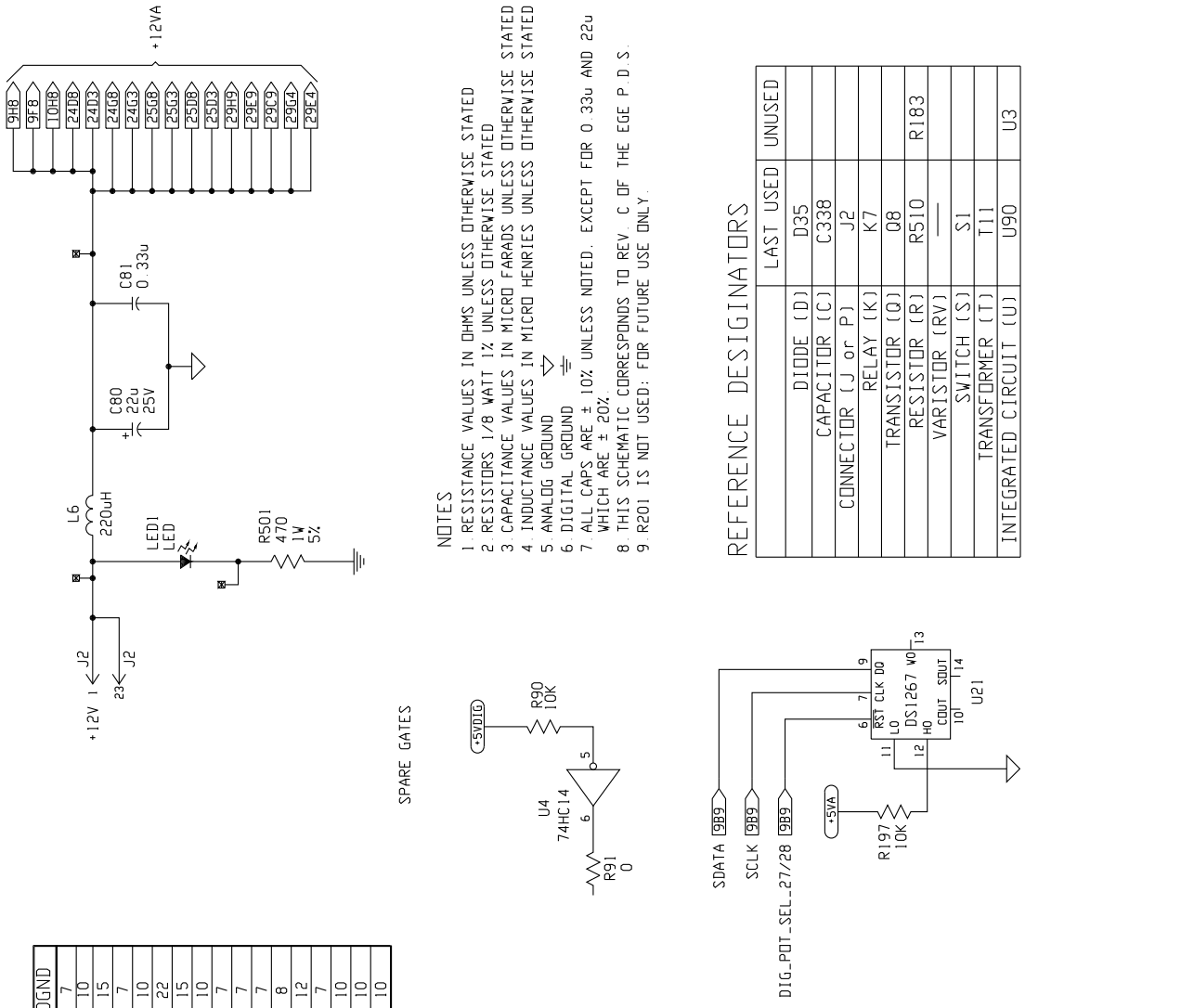


POWER TABLE

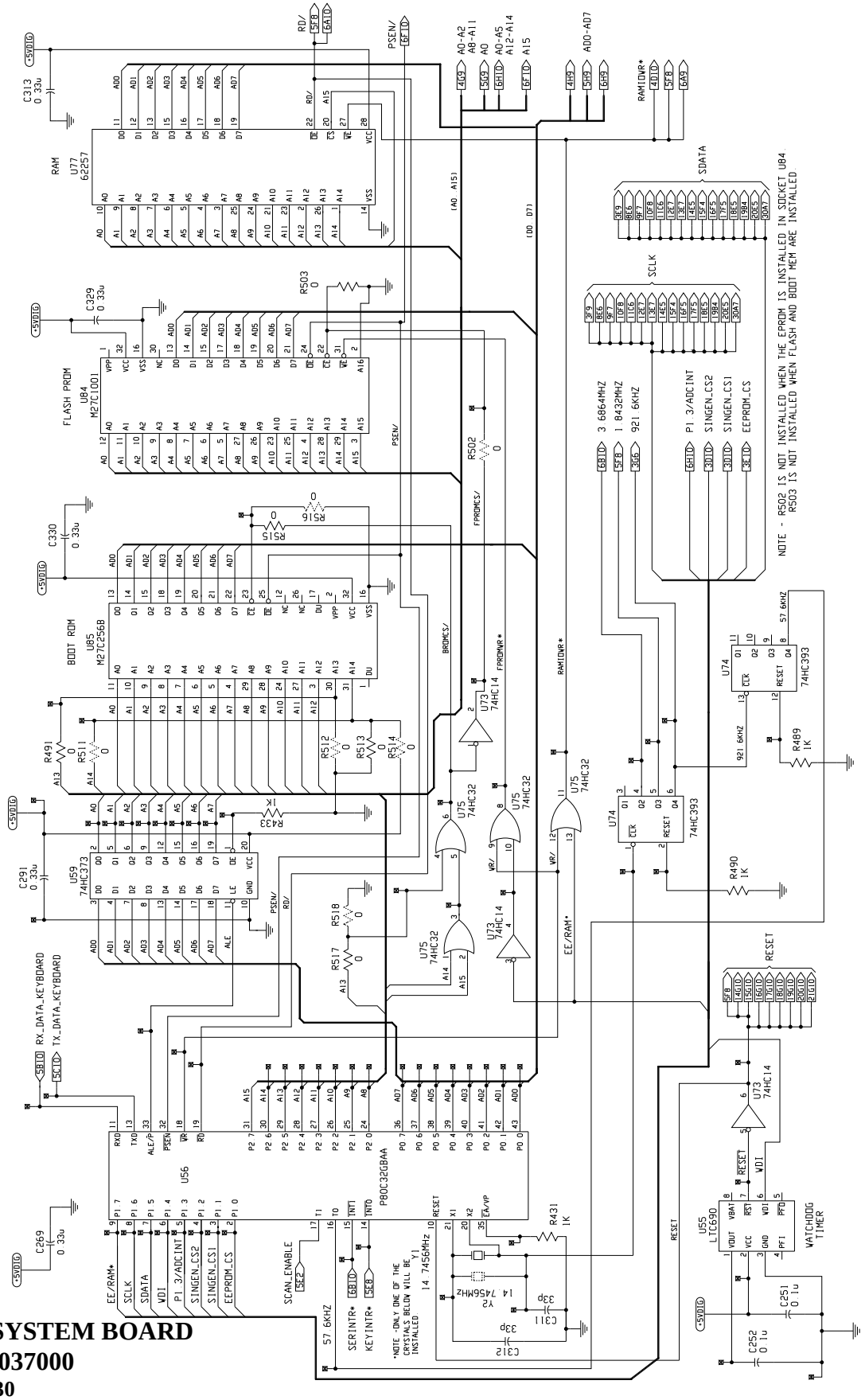
REF	+5VA	-5VA	AGND	+12VA	REF	+5VDIG	DGND
U5	4	11			U4	14	7
U6	4	11			U43	20	10
U7	4	11			U44	16	15
U8	8	4			U45	14	7
U9	16	1	8		U54	20	10
U10	4	11			U56	44	22
U11	8	4			U68	16	15
U12	16	1	8		U70	20	10
U13	16	1	8		U73	14	7
U14	16	1	8		U74	14	7
U15	4	11			U75	14	7
U16	16	1	8		U76	16	8
U17	16	1	8		U78	24	12
U18	4	11			U83	14	7
U19	16	1	8		U86	20	10
U20	8	4			U87	20	10
U21	16	1	8		U88	20	10
U27	16	1	8	4			
U28		11					
U29	11	6					
U30	11	6					
U31	4	11					
U32	16	1	8				
U33	8	4					
U34	8	4					
U41	4	11					
U47	4	11					
U50	4	11					
U51	16	1	8				
U52	8	4					
U53	8	4					
U60	16	1	8				
U63	4	11					
U64	4	11					
U65	16	1	8				
U66	4	11					
U67	16	1	8				
U89	4	11					
U90	16	1	8				

AUDIO SYSTEM BOARD
P29/7720037000

Sheet 1 of 30

Notes, IC Power Distribution Table, Etc.

(772-0037-XXX-EC, Sh. 1 , Rev. A)

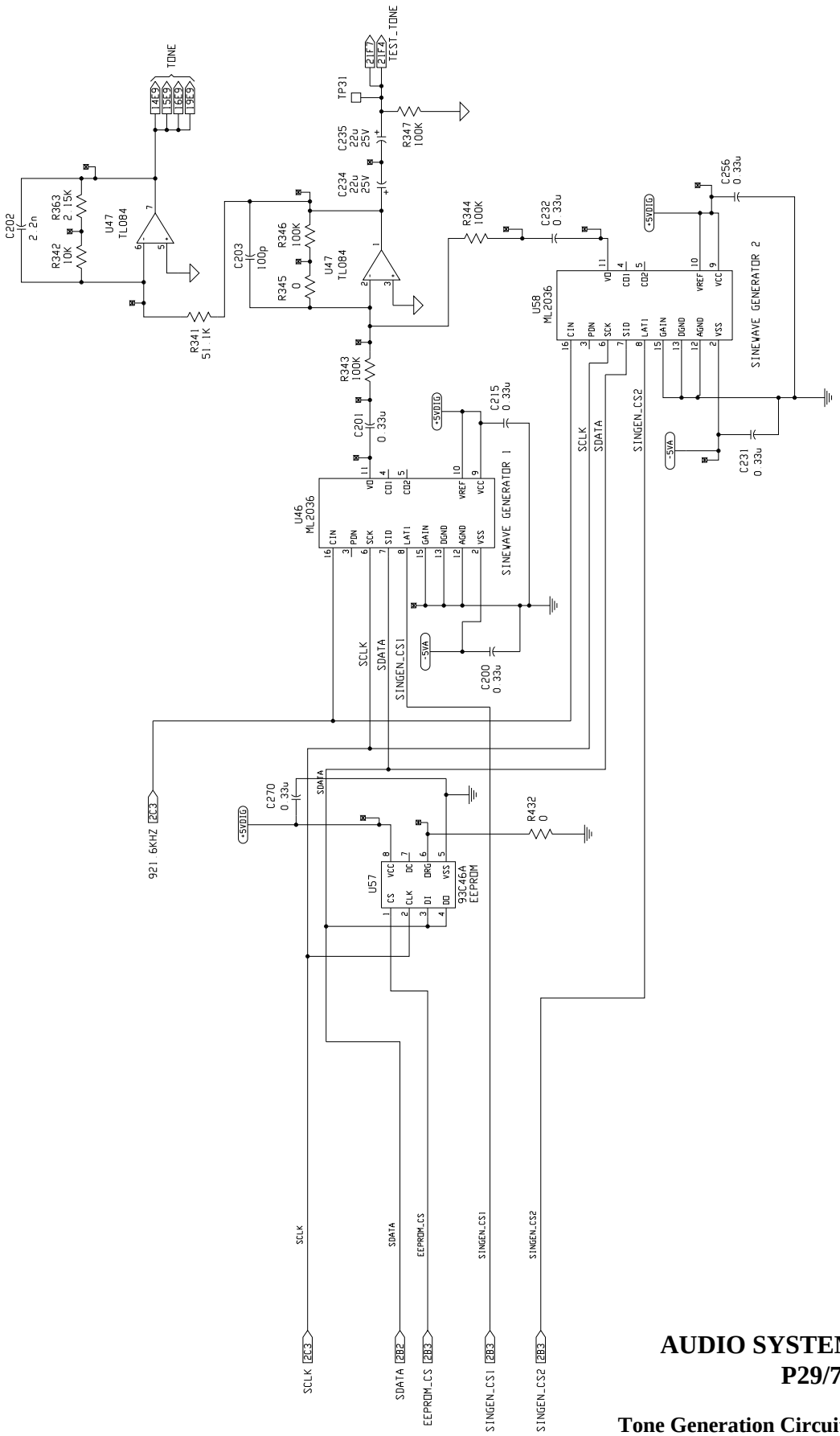


AUDIO SYSTEM BOARD
P29/7720037000

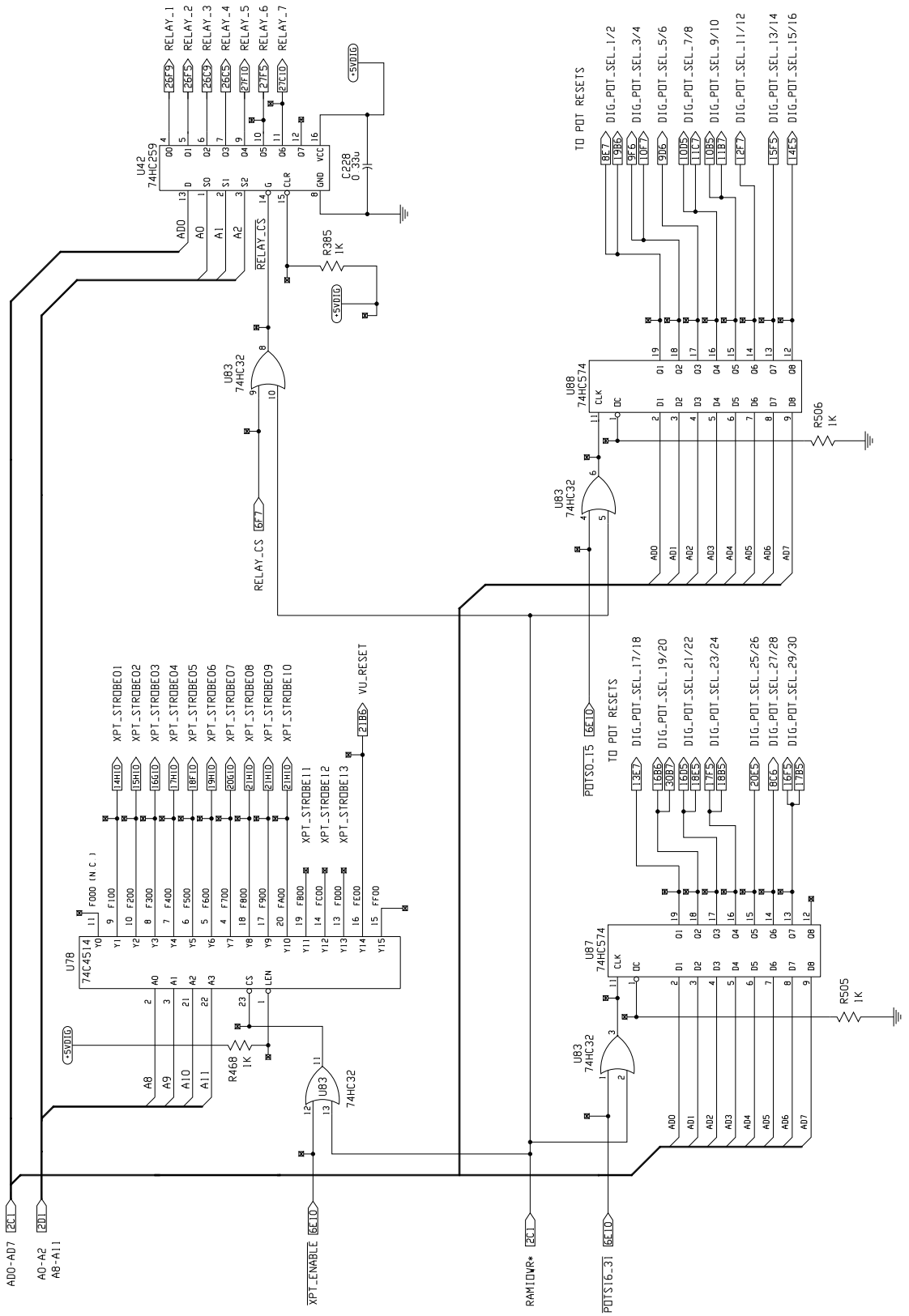
Sheet 2 of 30

Microcontroller Circuits

(772-0037-XXX-EC, Sh. 2 , Rev. A)



AUDIO SYSTEM BOARD
P29/7720037000
Sheet 3 of 30
Tone Generation Circuits (Not Used)
(772-0037-XXX-EC, Sh. 3 , Rev. A)

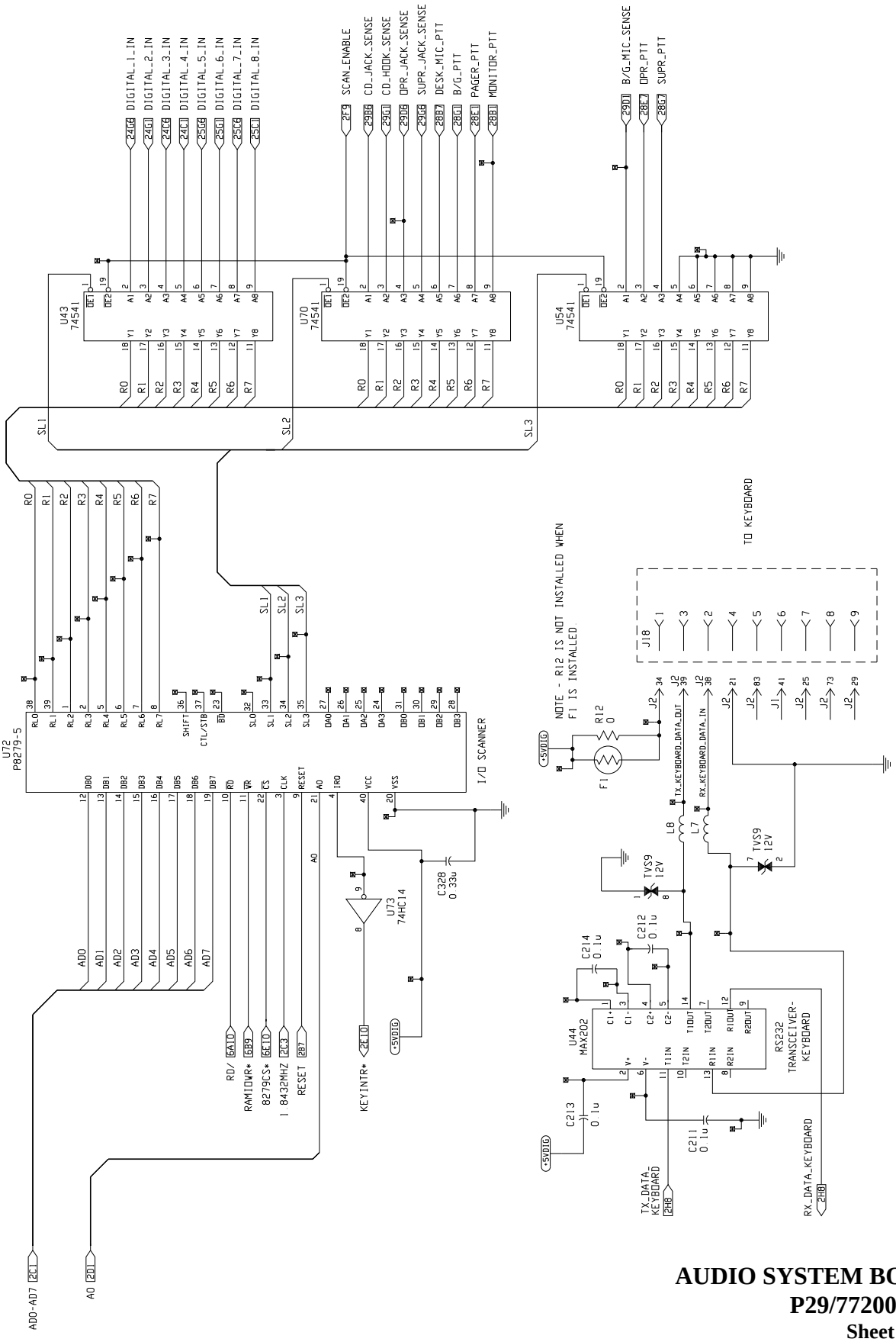


AUDIO SYSTEM BOARD
P29/7720037000

Sheet 4 of 30

Cross-Point, Digitial Pot & Relay Logic

(772-0037-XXX-EC, Sh. 4 , Rev. A)

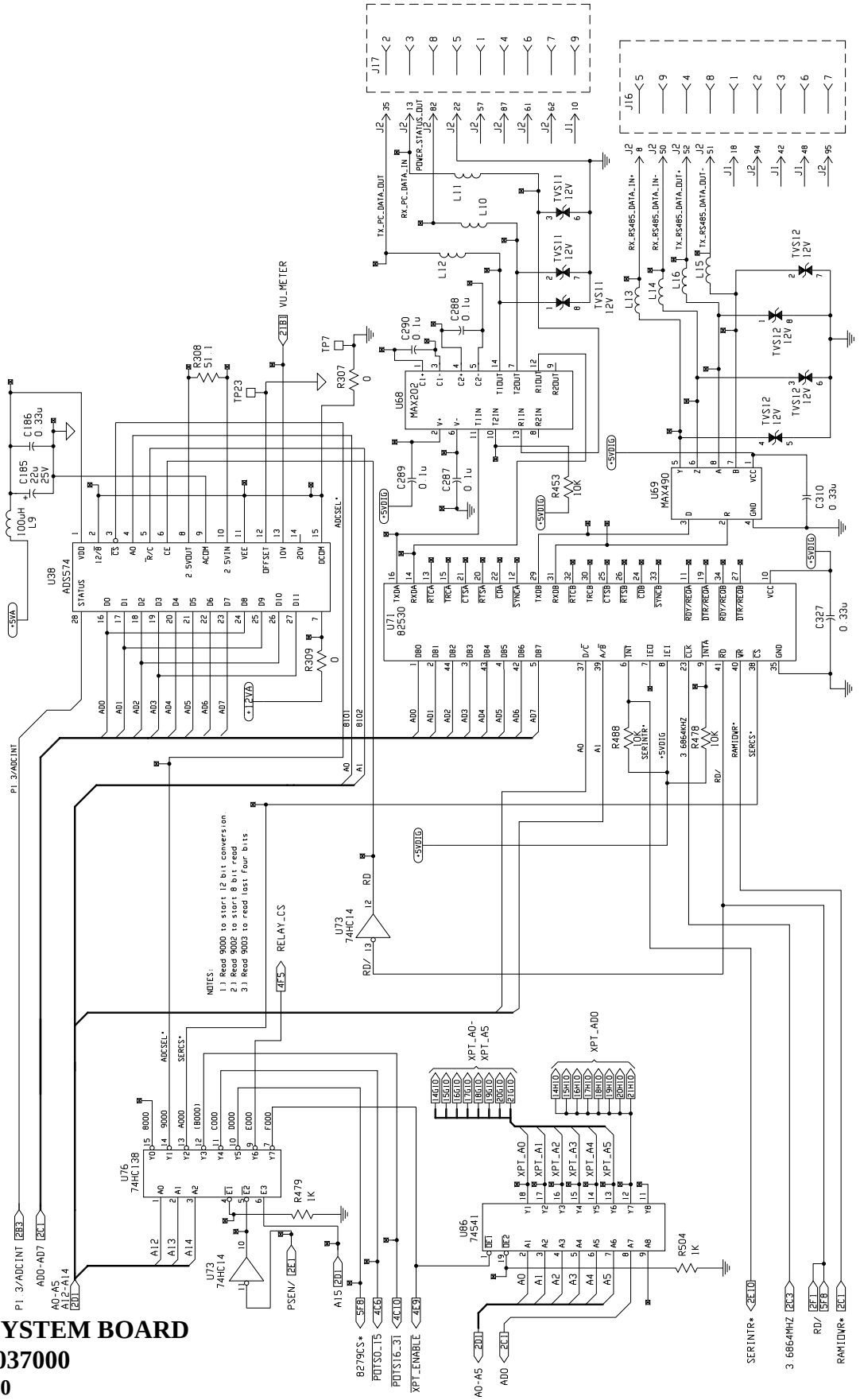


AUDIO SYSTEM BOARD
P29/7720037000

Sheet 5 of 30

PTT & Sense Logic, Keyboard Serial Port

(772-0037-XXX-EC, Sh. 5 , Rev. A)

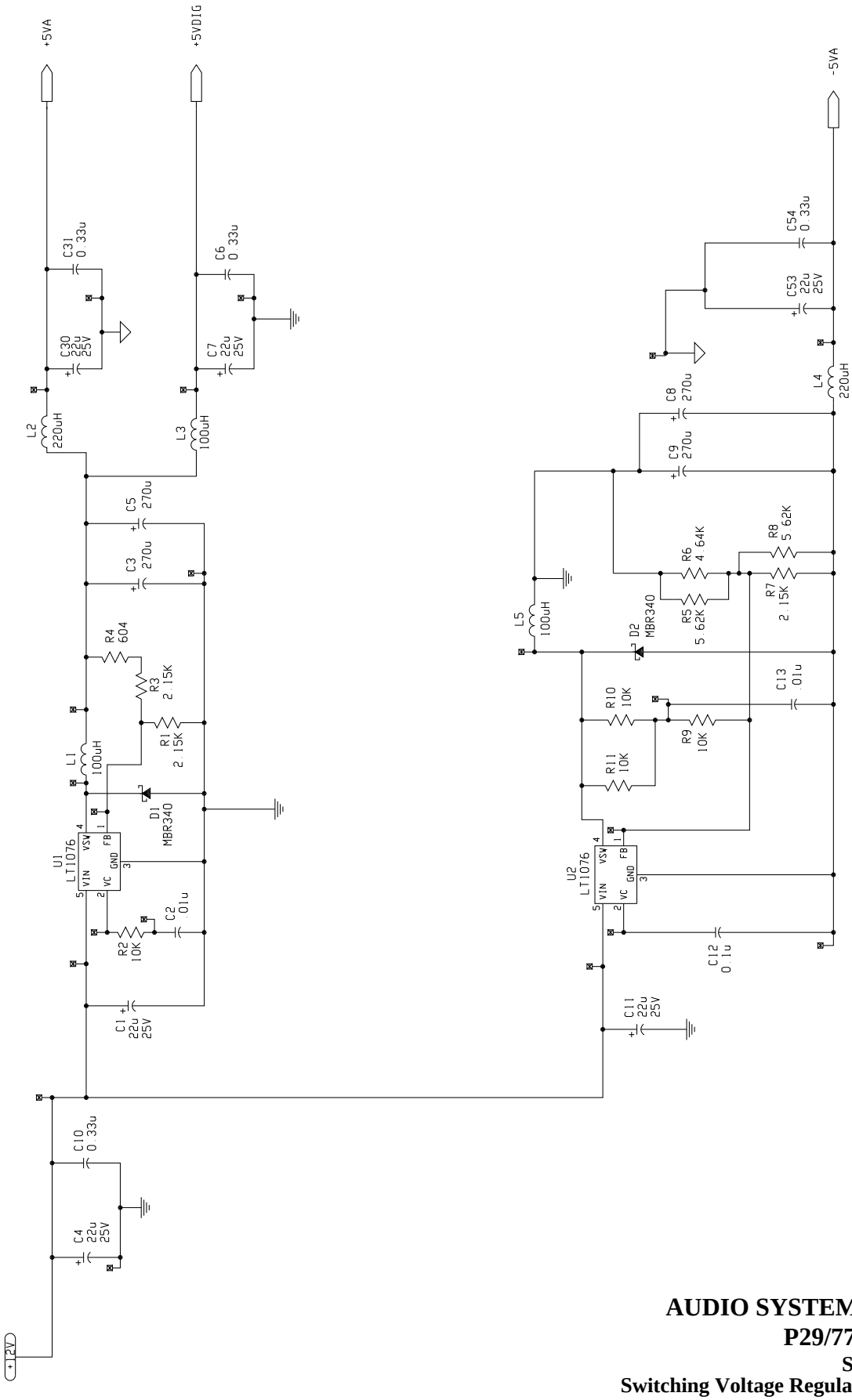


AUDIO SYSTEM BOARD
P29/7720037000

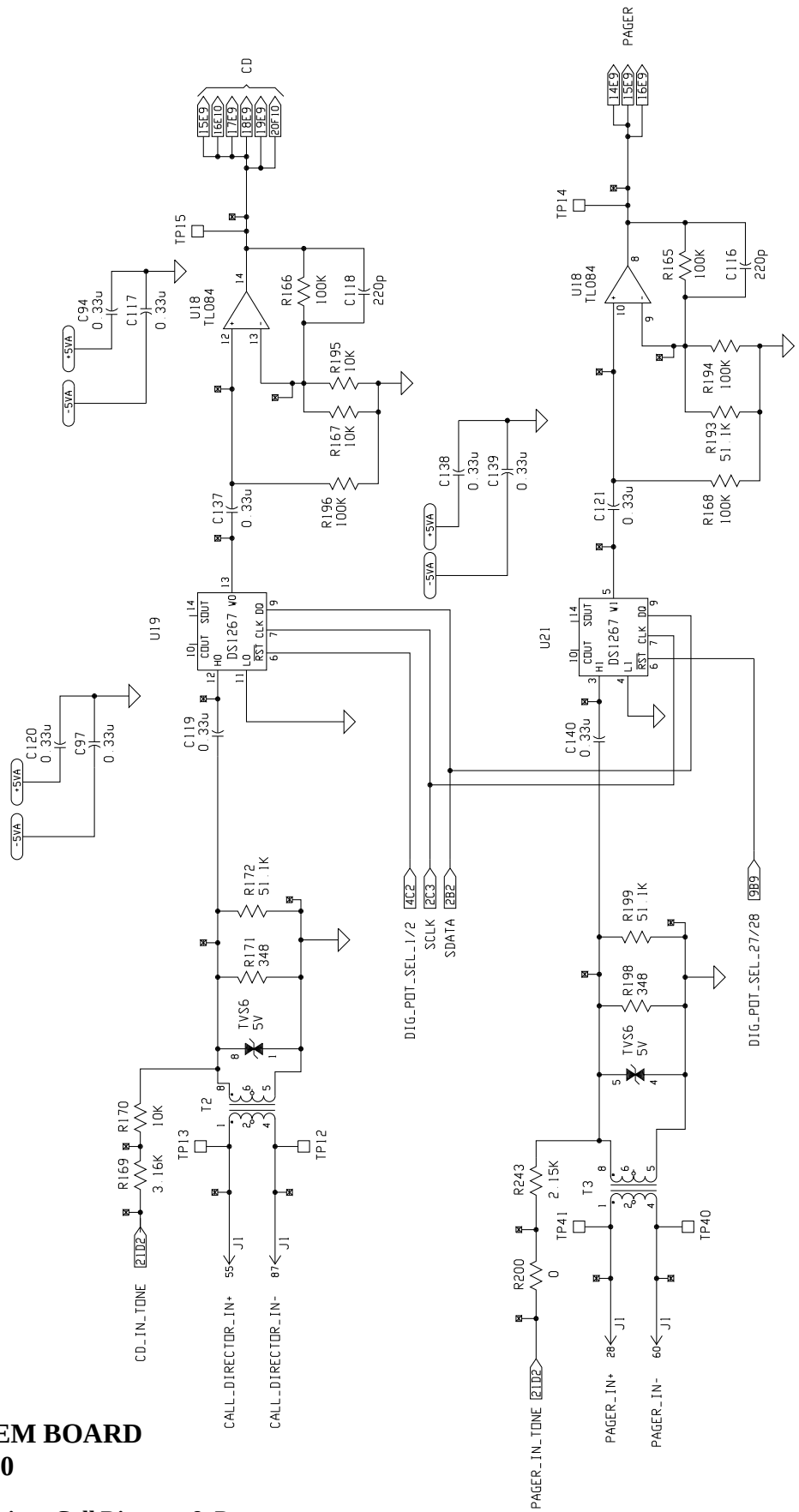
Sheet 6 of 30

PC & Expansion Serial Ports, Address Decoders, A/D Converter

(772-0037-XXX-EC, Sh. 6 , Rev. A)

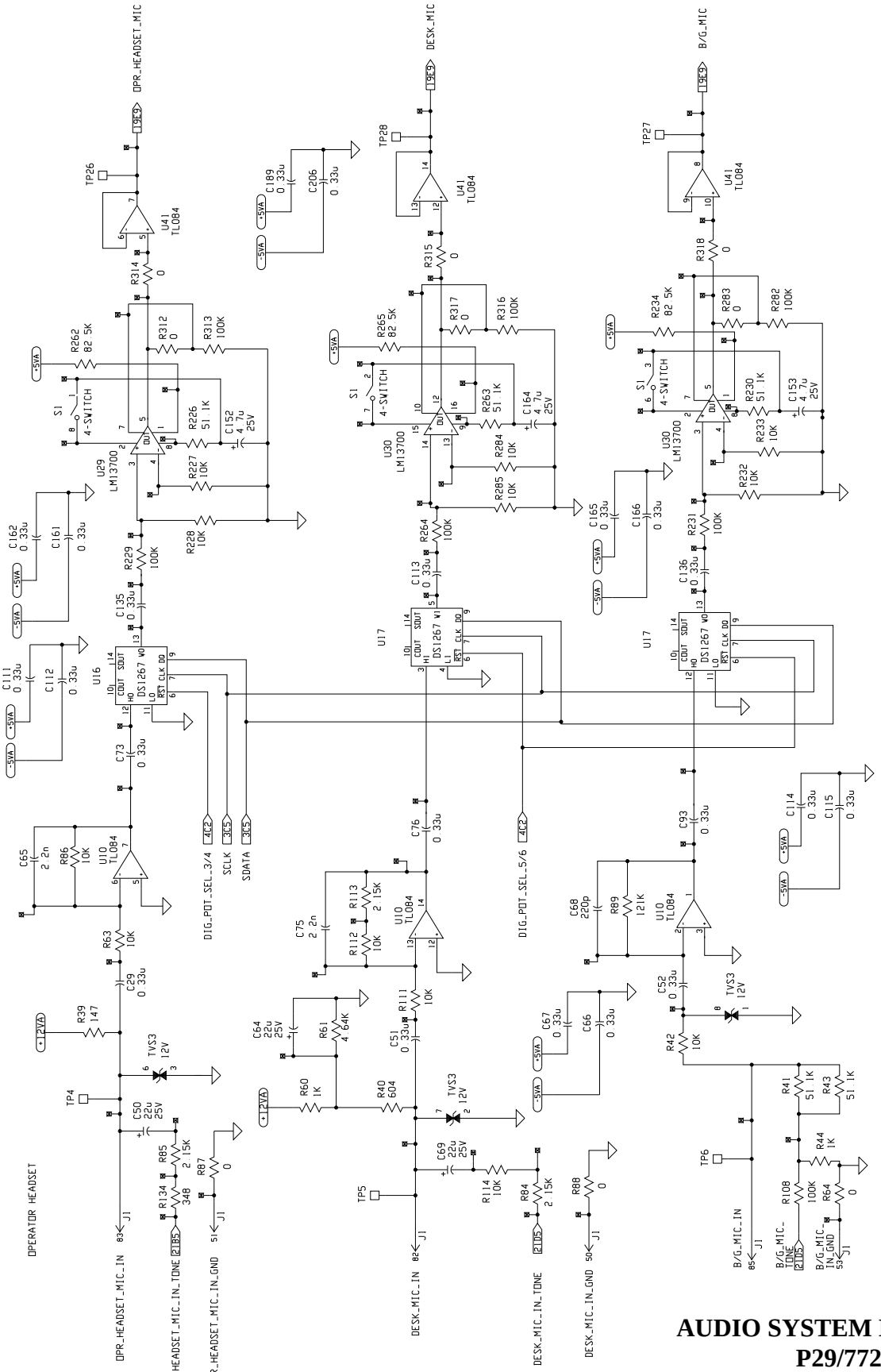


AUDIO SYSTEM BOARD
P29/7720037000
Sheet 7 of 30
Switching Voltage Regulator Circuits
(772-0037-XXX-EC, Sh. 7 , Rev. A)



AUDIO SYSTEM BOARD
P29/7720037000
Sheet 8 of 30
Audio Input Circuits – Call Director & Pager

(772-0037-XXX-EC, Sh. 8 , Rev. A)

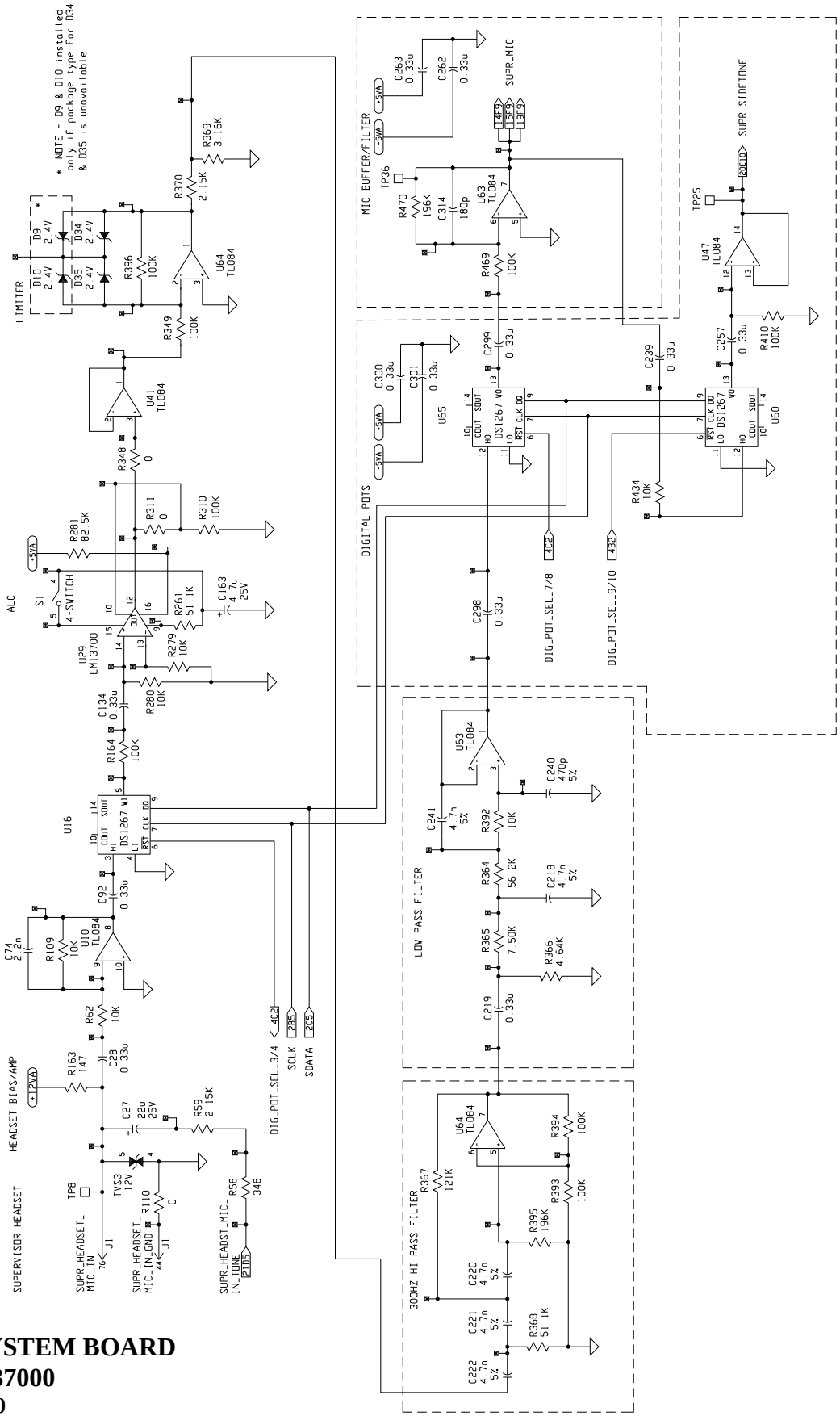


AUDIO SYSTEM BOARD
P29/7720037000

Sheet 9 of 30

Audio Input Circuits – Oper. Headset, Desk & B/G Mics

(772-0037-XXX-EC, Sh. 9 , Rev. A)

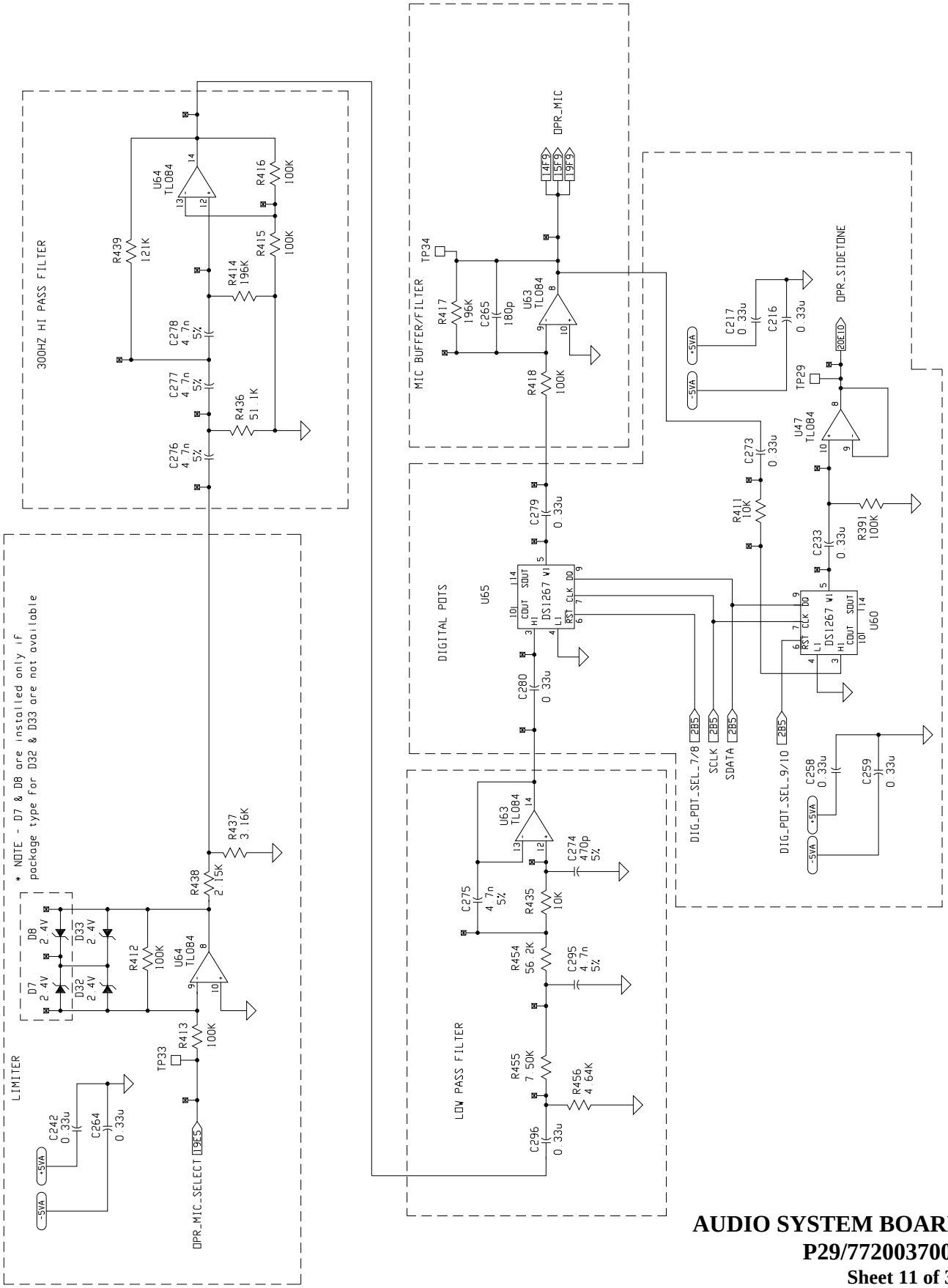


AUDIO SYSTEM BOARD
P29/7720037000

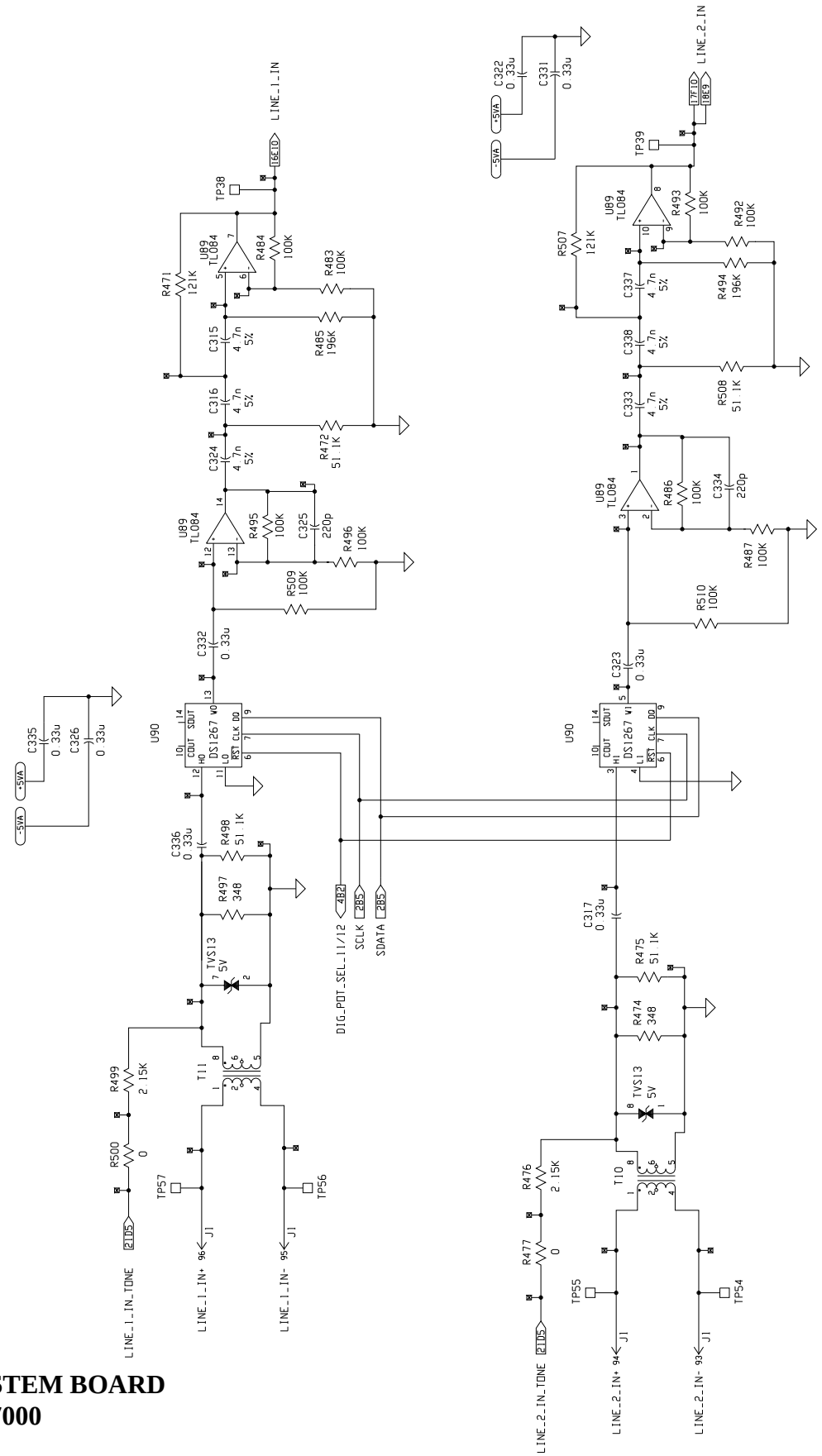
Sheet 10 of 30

Audio Input Circuit – Supervisor Headset Mic

(772-0037-XXX-EC, Sh. 10 , Rev. A)



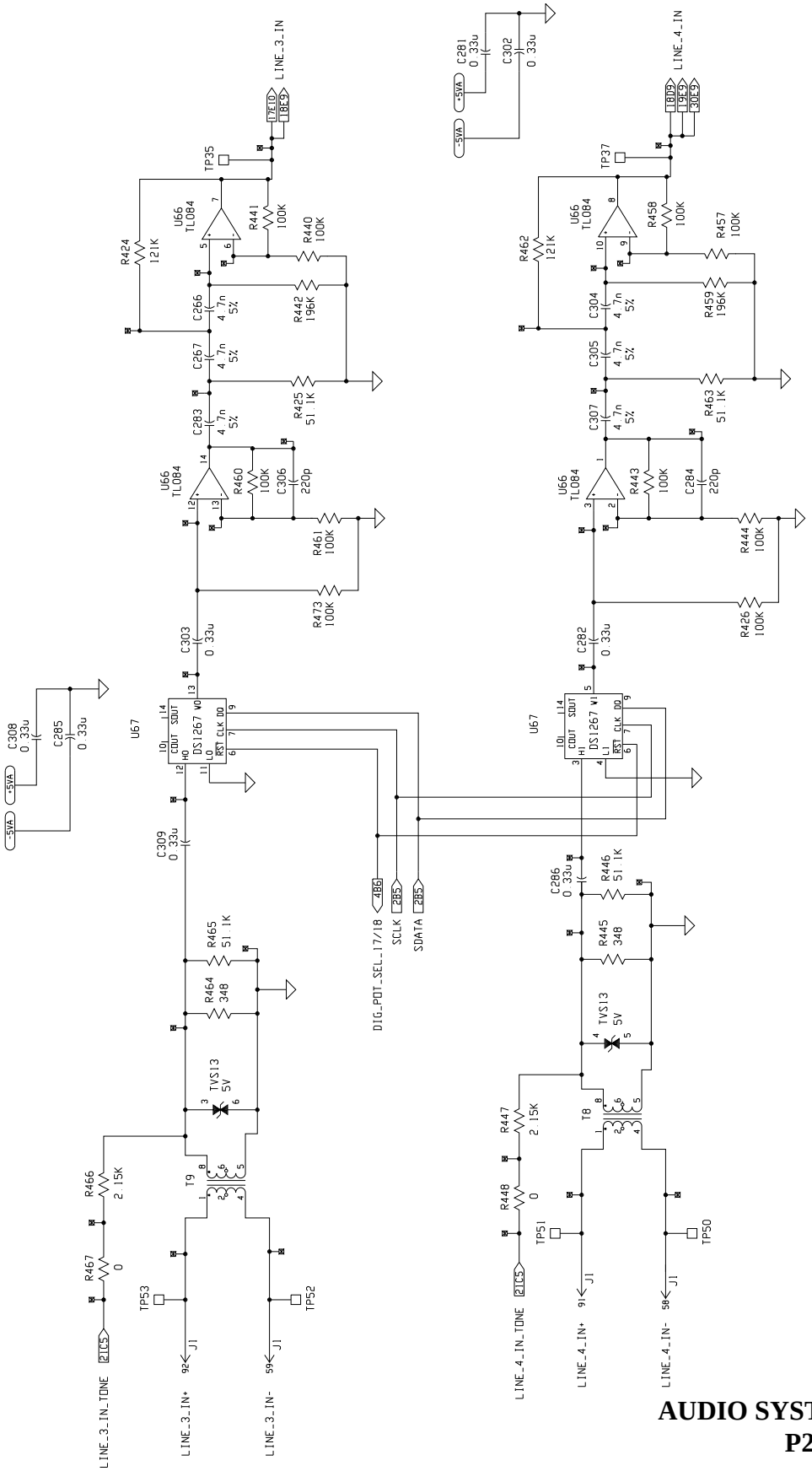
AUDIO SYSTEM BOARD
P29/7720037000
Sheet 11 of 30
Audio Input Circuit – Non-Supervisory Mic Post-Conditioning
(772-0037-XXX-EC, Sh. 11 , Rev. A)



AUDIO SYSTEM BOARD
P29/7720037000

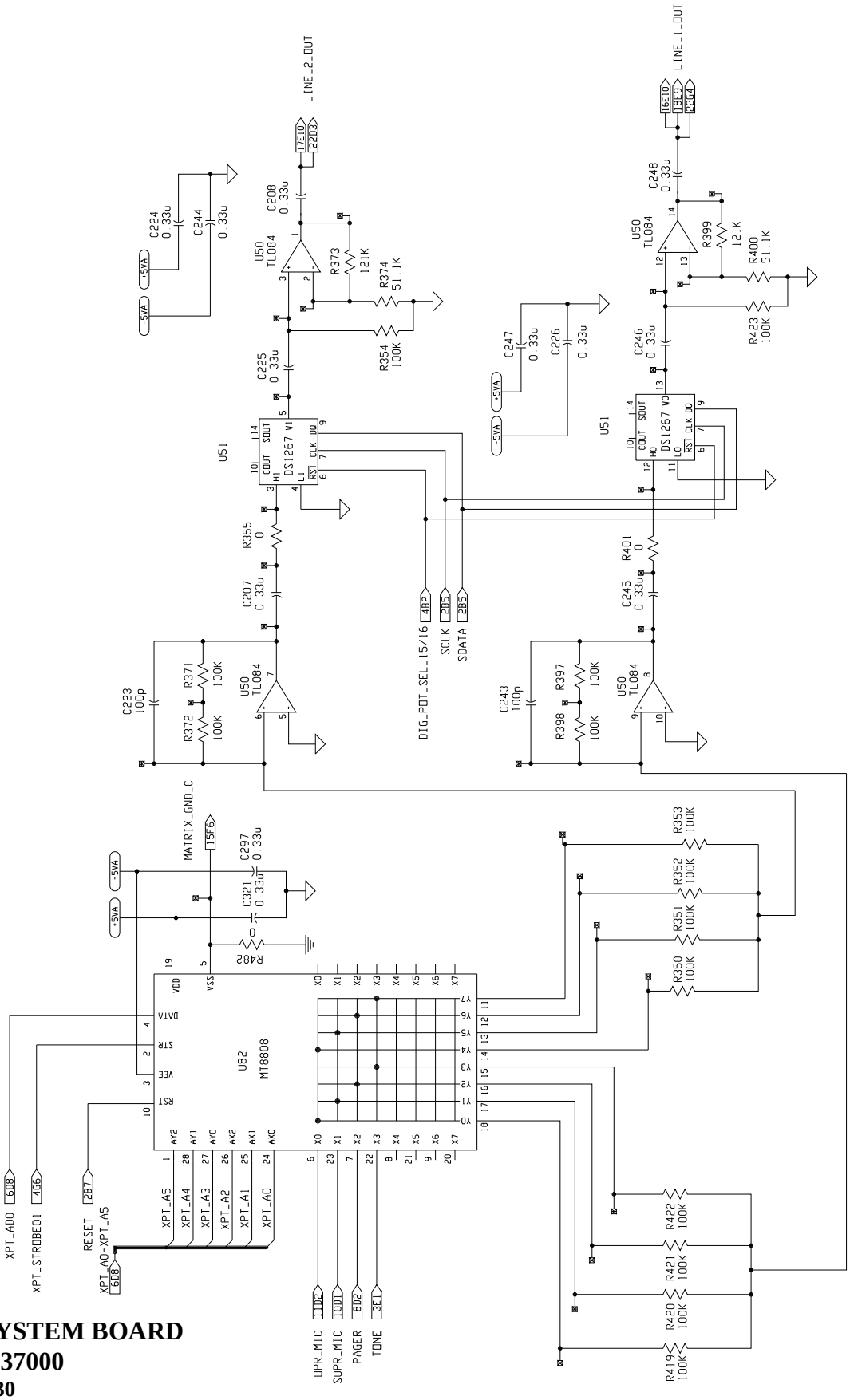
Sheet 12 of 30
Audio Input Circuits – Lines 1 & 2

(772-0037-XXX-EC, Sh. 12 , Rev. A)



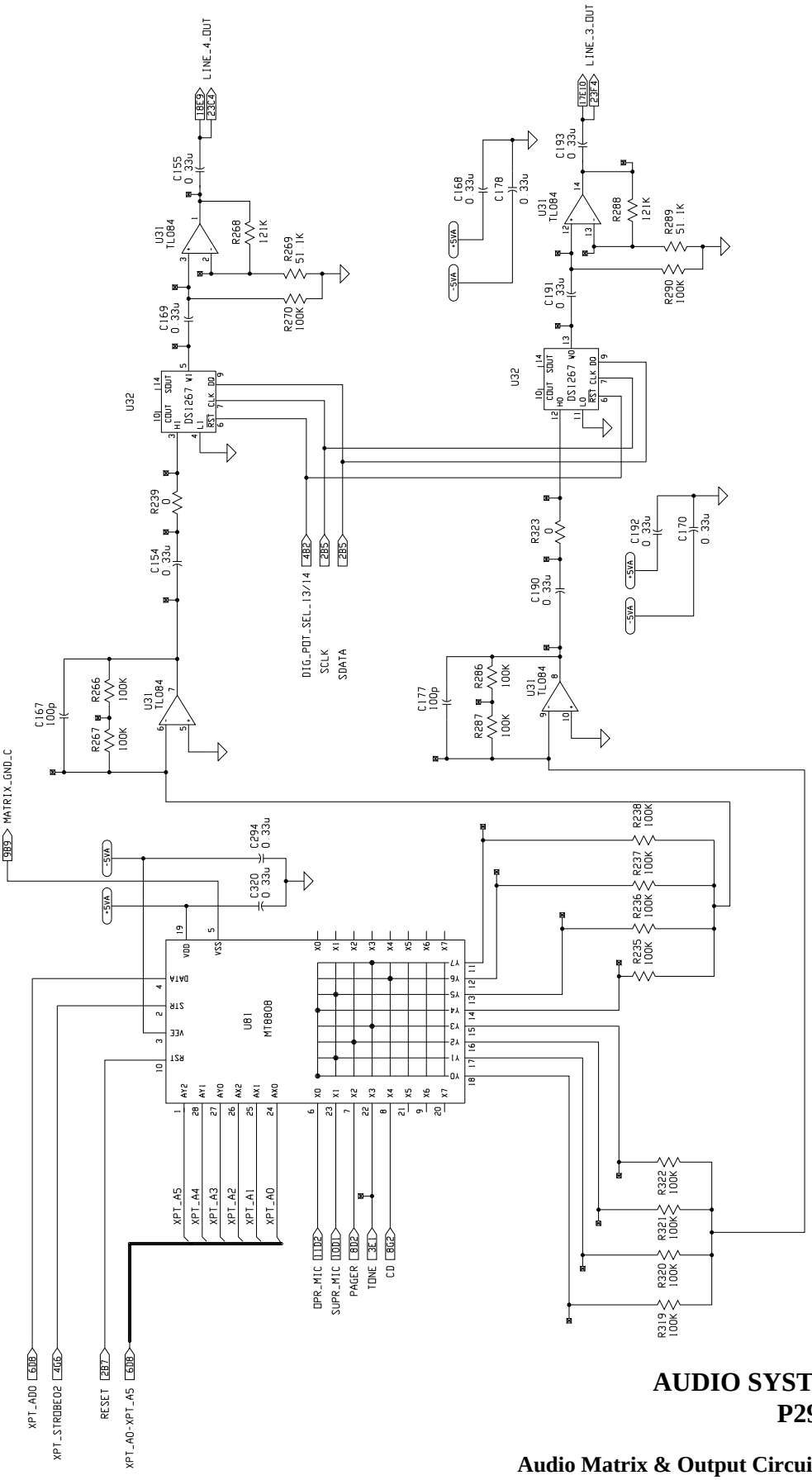
AUDIO SYSTEM BOARD
P29/7720037000
Sheet 13 of 30
Audio Input Circuits – Lines 3 & 4

(772-0037-XXX-EC, Sh. 13 , Rev. A)



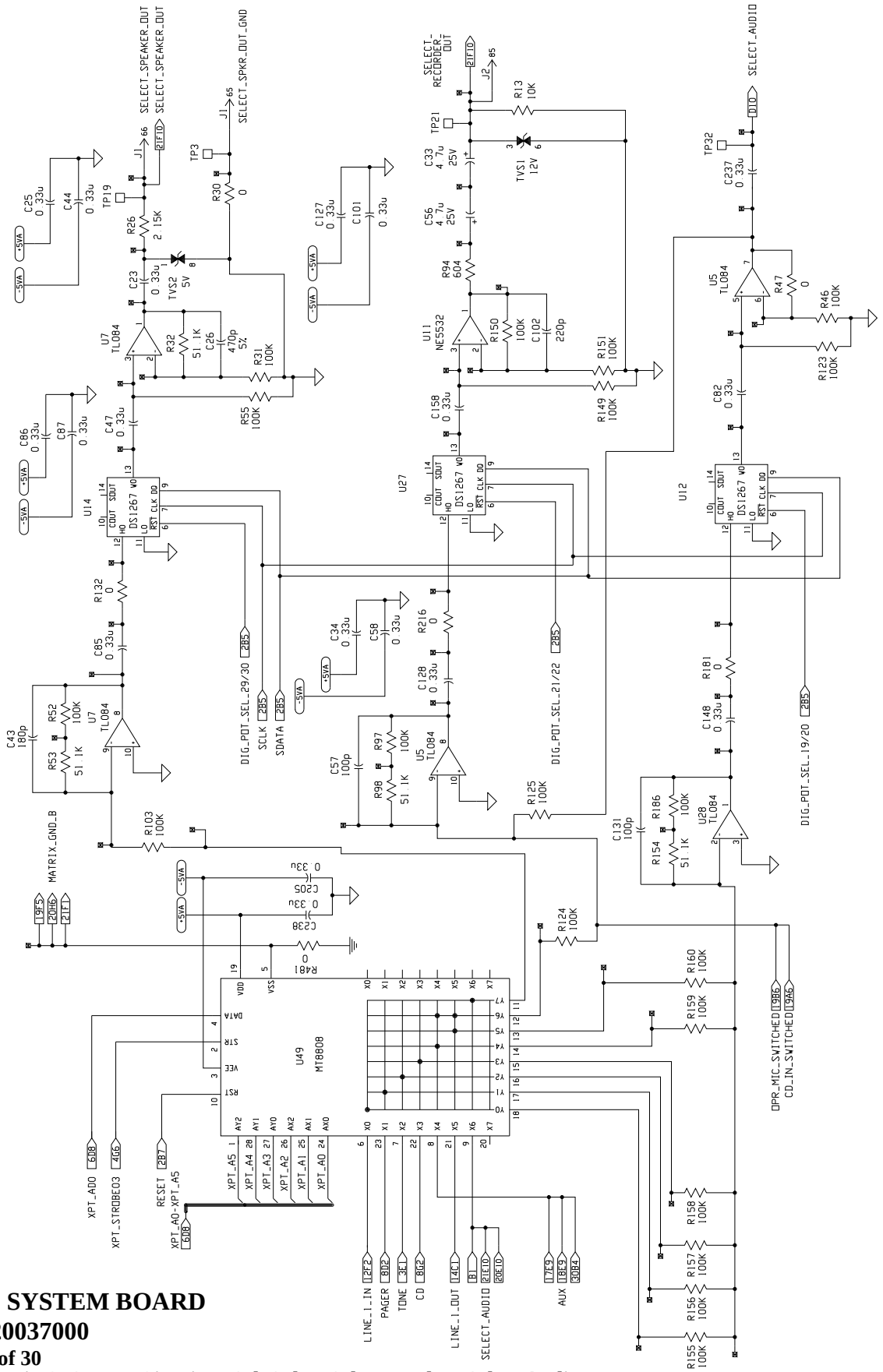
AUDIO SYSTEM BOARD
P29/7720037000
Sheet 14 of 30
Audio Matrix & Output Circuits – Lines 1 & 2

(772-0037-XXX-EC, Sh. 14 , Rev. A)



AUDIO SYSTEM BOARD
P29/7720037000
Sheet 15 of 30
Audio Matrix & Output Circuits – Lines 3 & 4

(772-0037-XXX-EC, Sh. 15 , Rev. A)

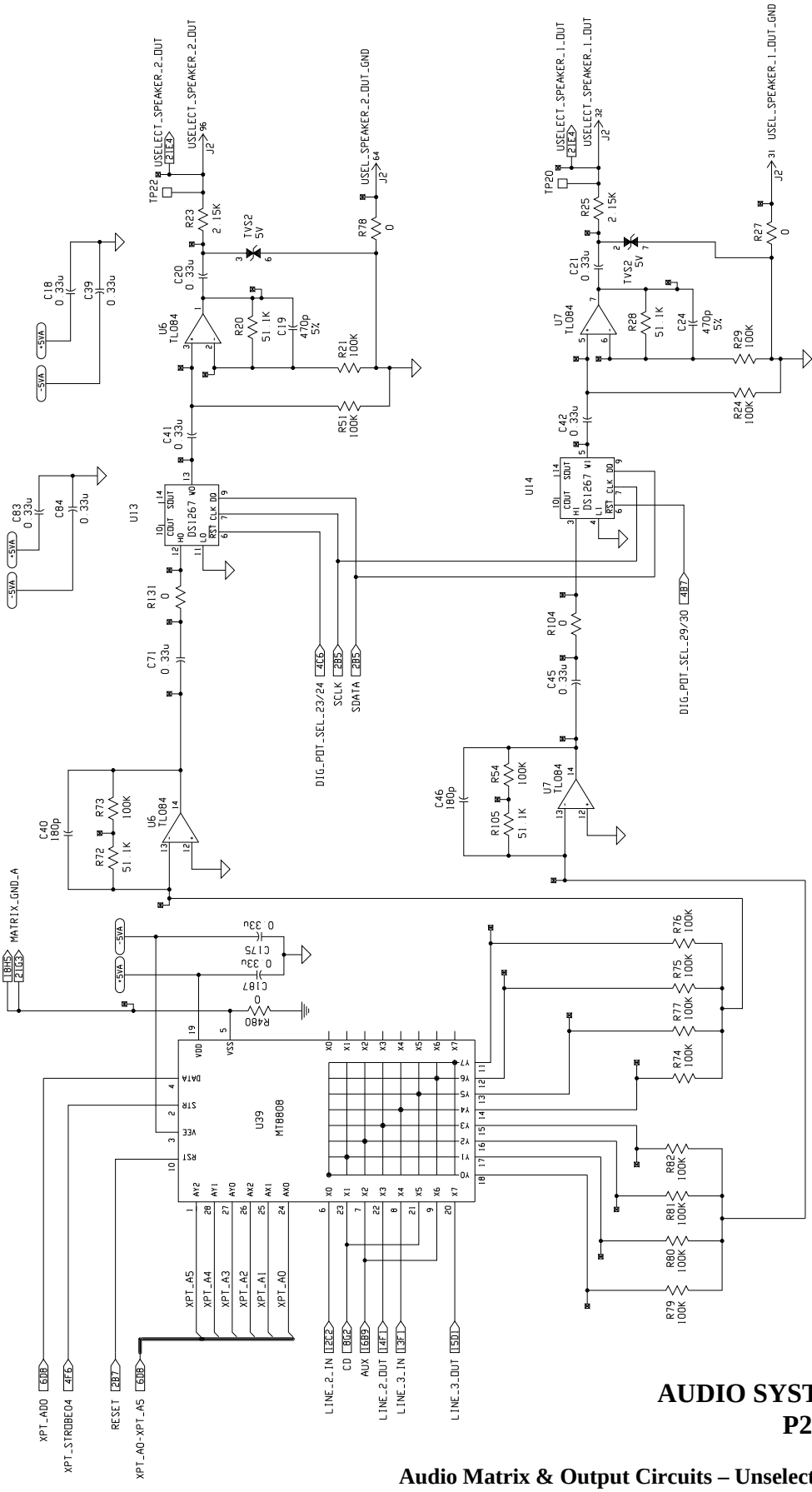


AUDIO SYSTEM BOARD
P29/7720037000

Sheet 16 of 30

Audio Matrix & Output Circuits – Sel. Spkr., Sel. Recorder., Select Audio

(772-0037-XXX-EC, Sh. 16 , Rev. A)

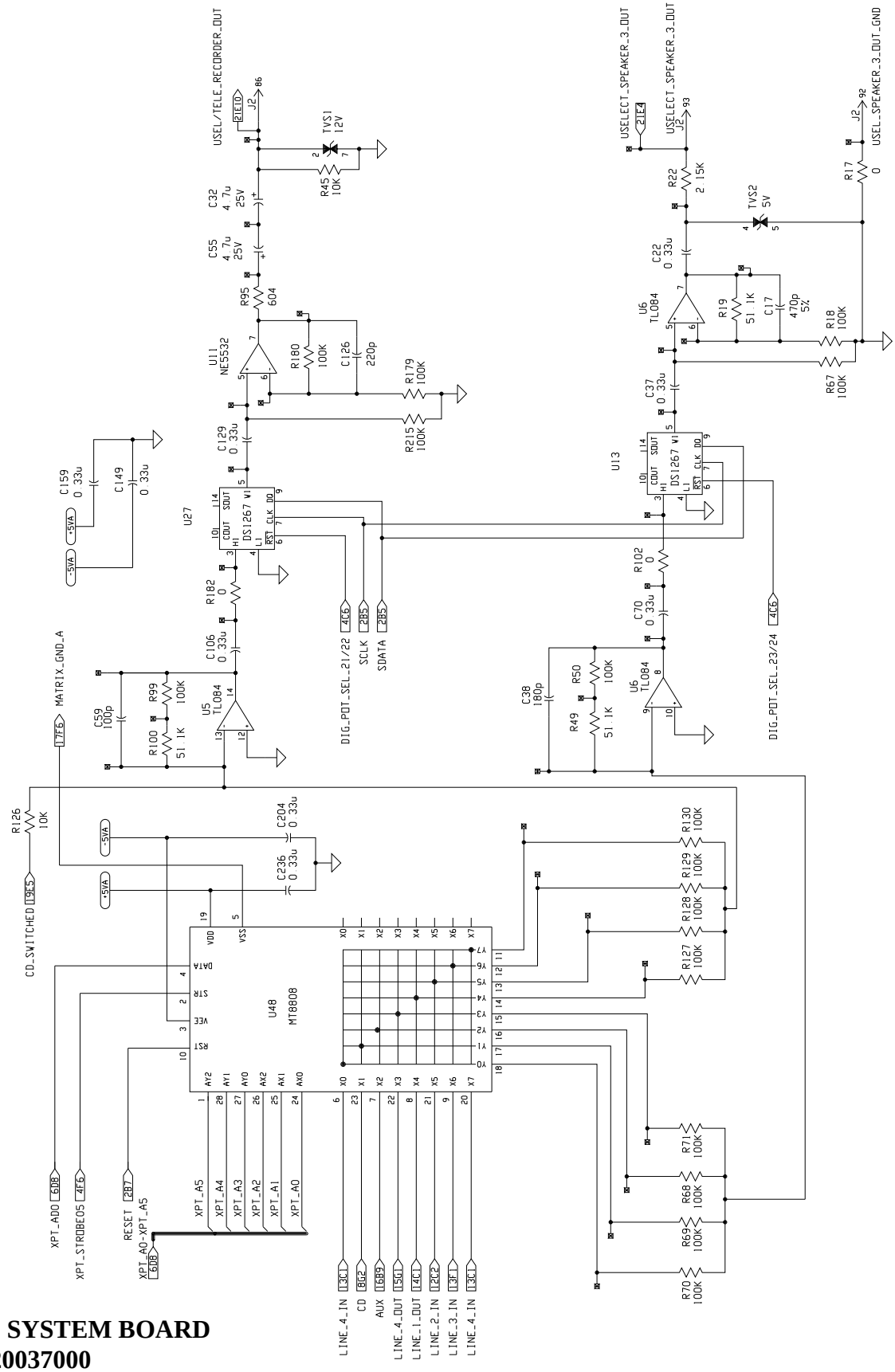


AUDIO SYSTEM BOARD
P29/7720037000

Sheet 17 of 30

Audio Matrix & Output Circuits – Unselect Speakers 1 & 2

(772-0037-XXX-EC, Sh. 17 , Rev. A)

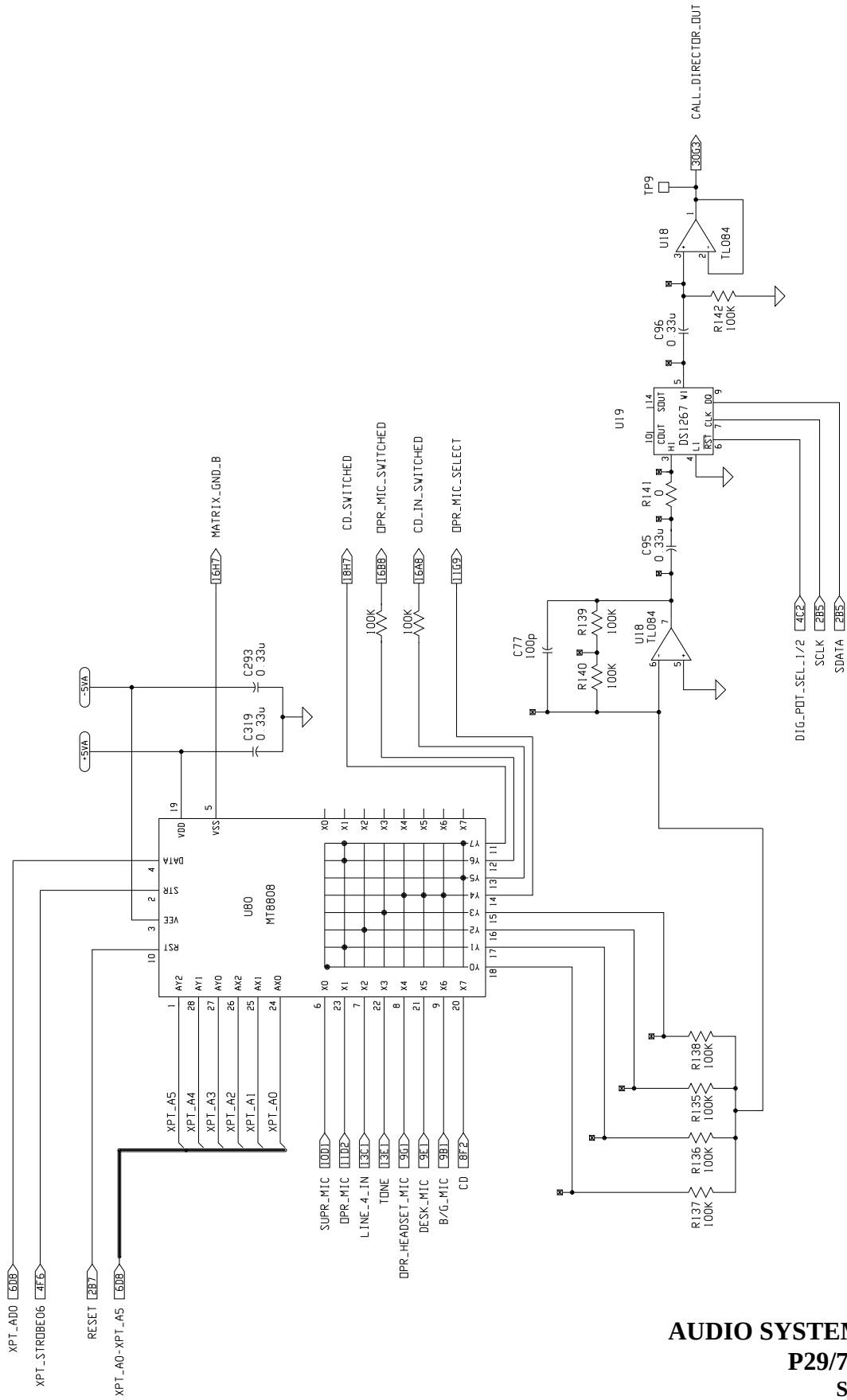


AUDIO SYSTEM BOARD
P29/7720037000

Sheet 18 of 30

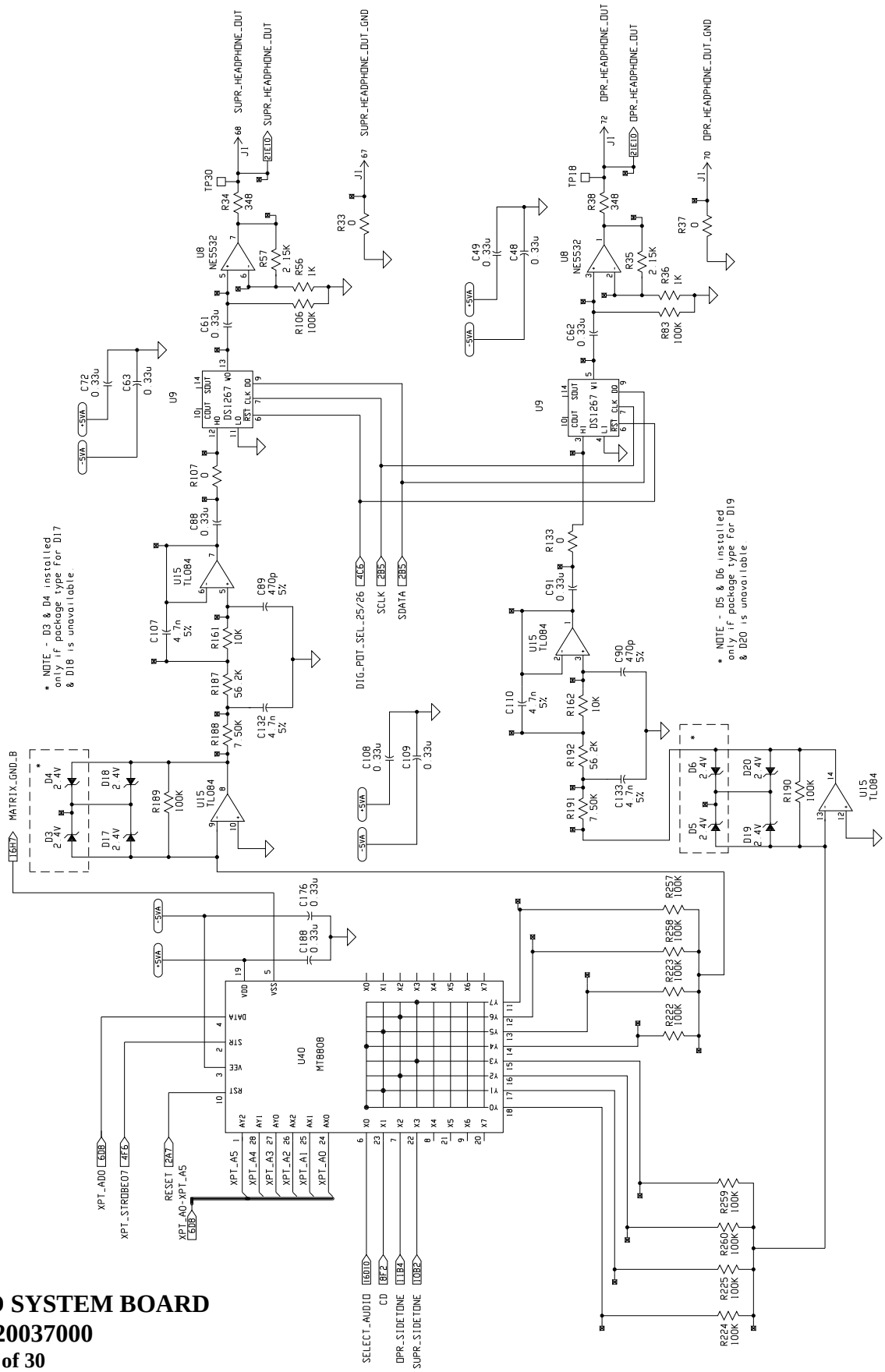
Audio Matrix & Output Circuits – Unselect/Tele. Recorder, Unselect Spkr. 3

(772-0037-XXX-EC, Sh. 18 , Rev. A)



AUDIO SYSTEM BOARD
P29/7720037000
Sheet 19 of 30
Audio Matrix & Output Circuits – Operator Mic Selection & Call Director

(772-0037-XXX-EC, Sh. 19 , Rev. A)

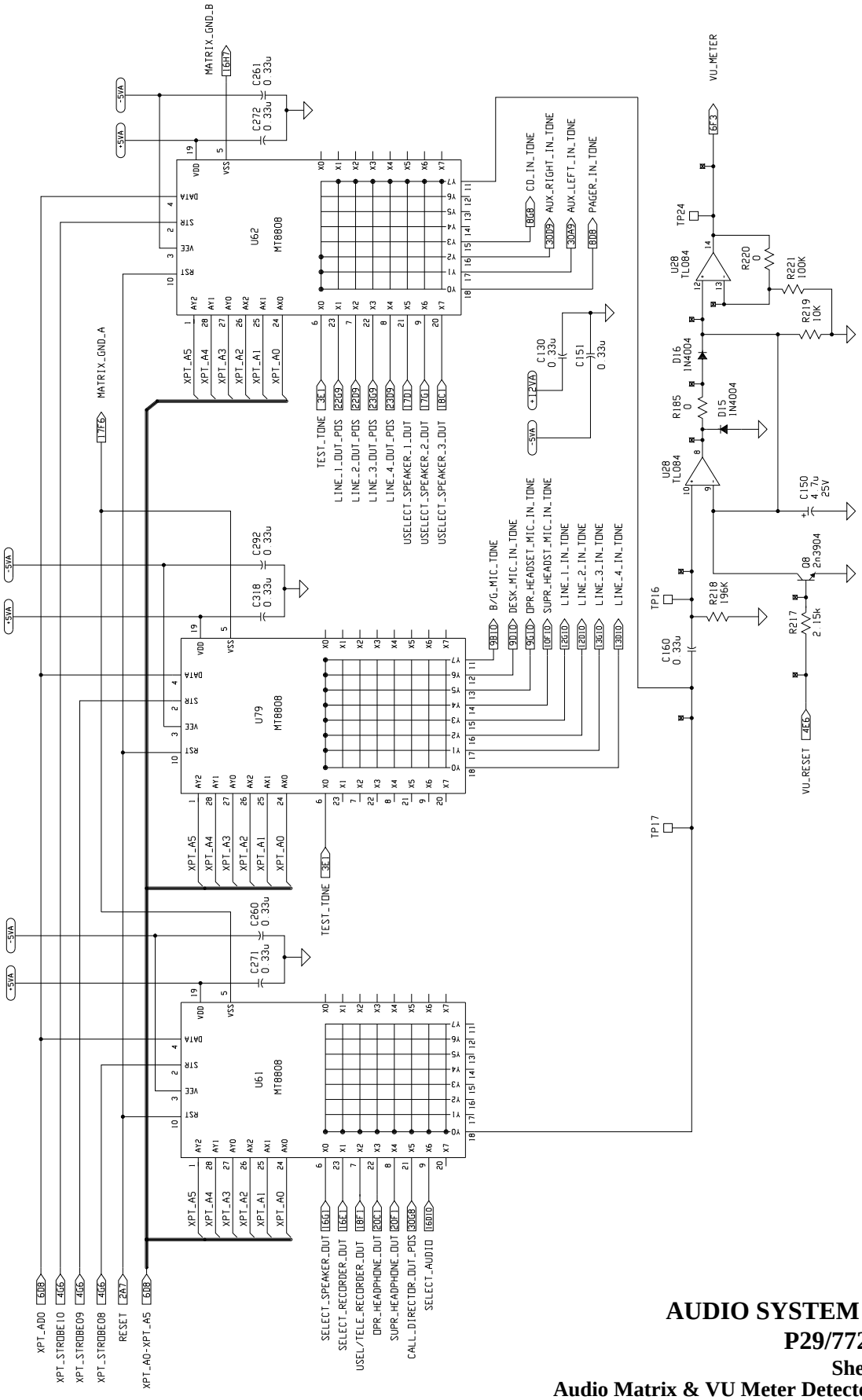


AUDIO SYSTEM BOARD
P29/7720037000

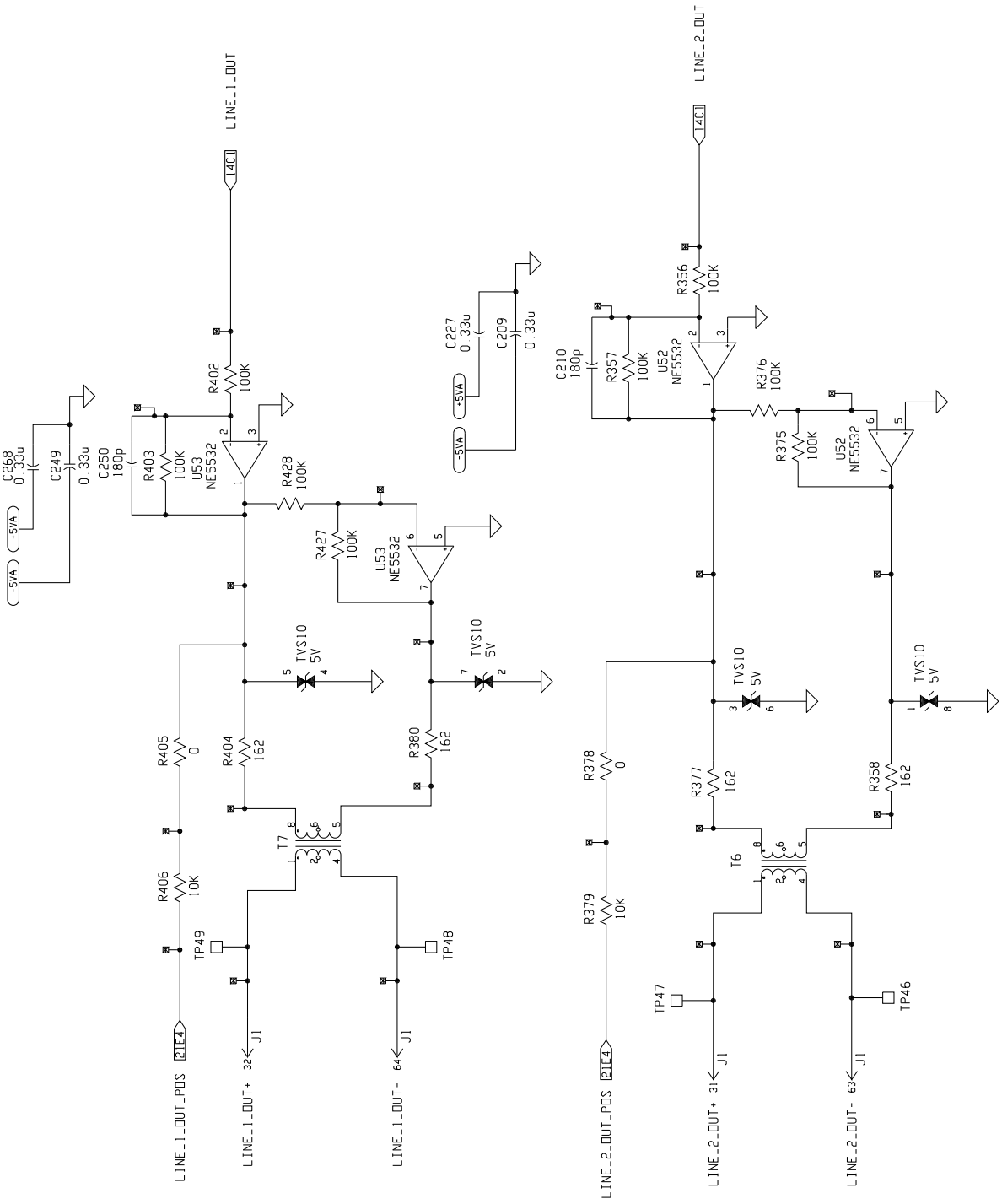
Sheet 20 of 30

Audio Matrix & Output Circuits – Super. & Oper. Headset Earphones

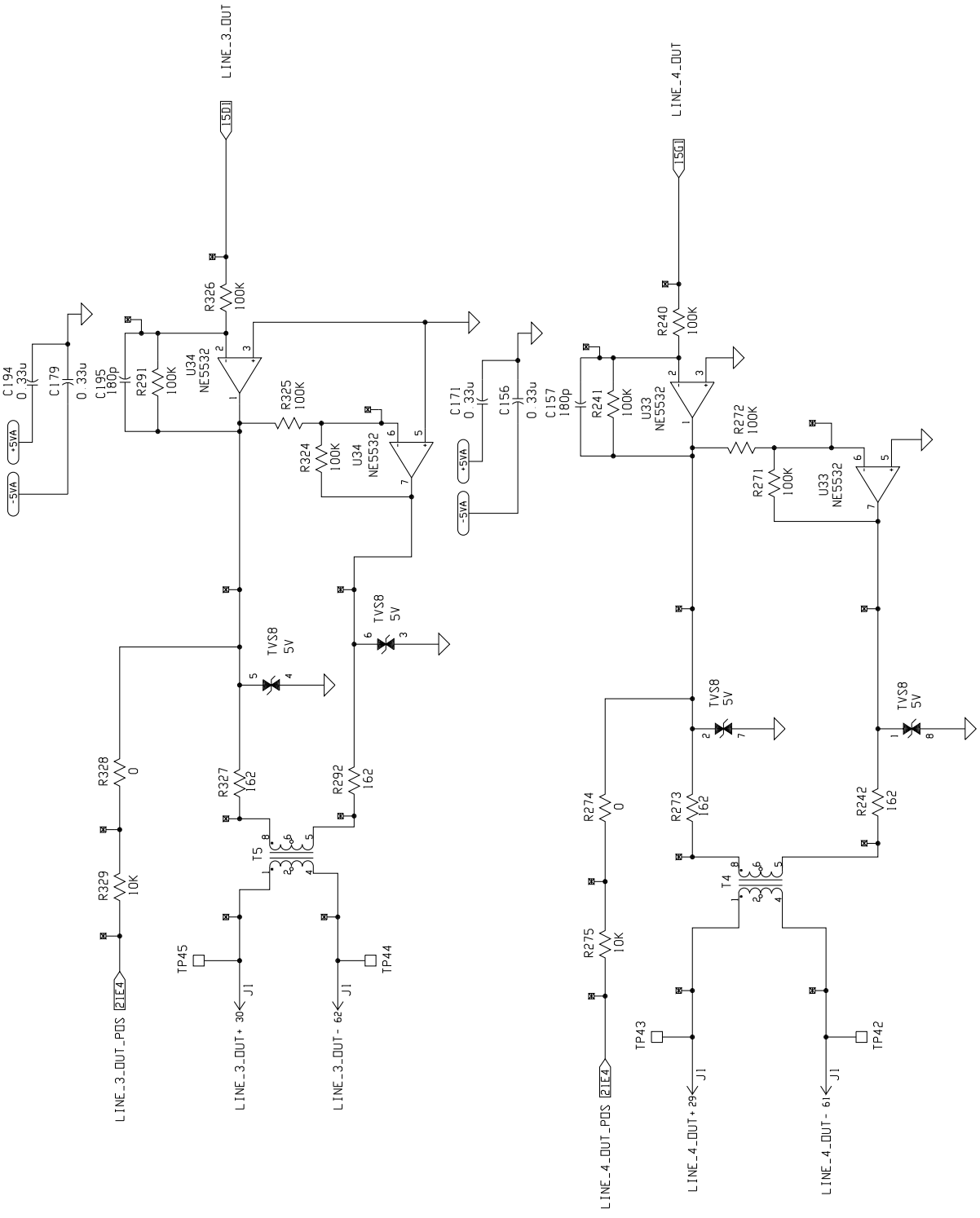
(772-0037-XXX-EC, Sh. 20 , Rev. A)



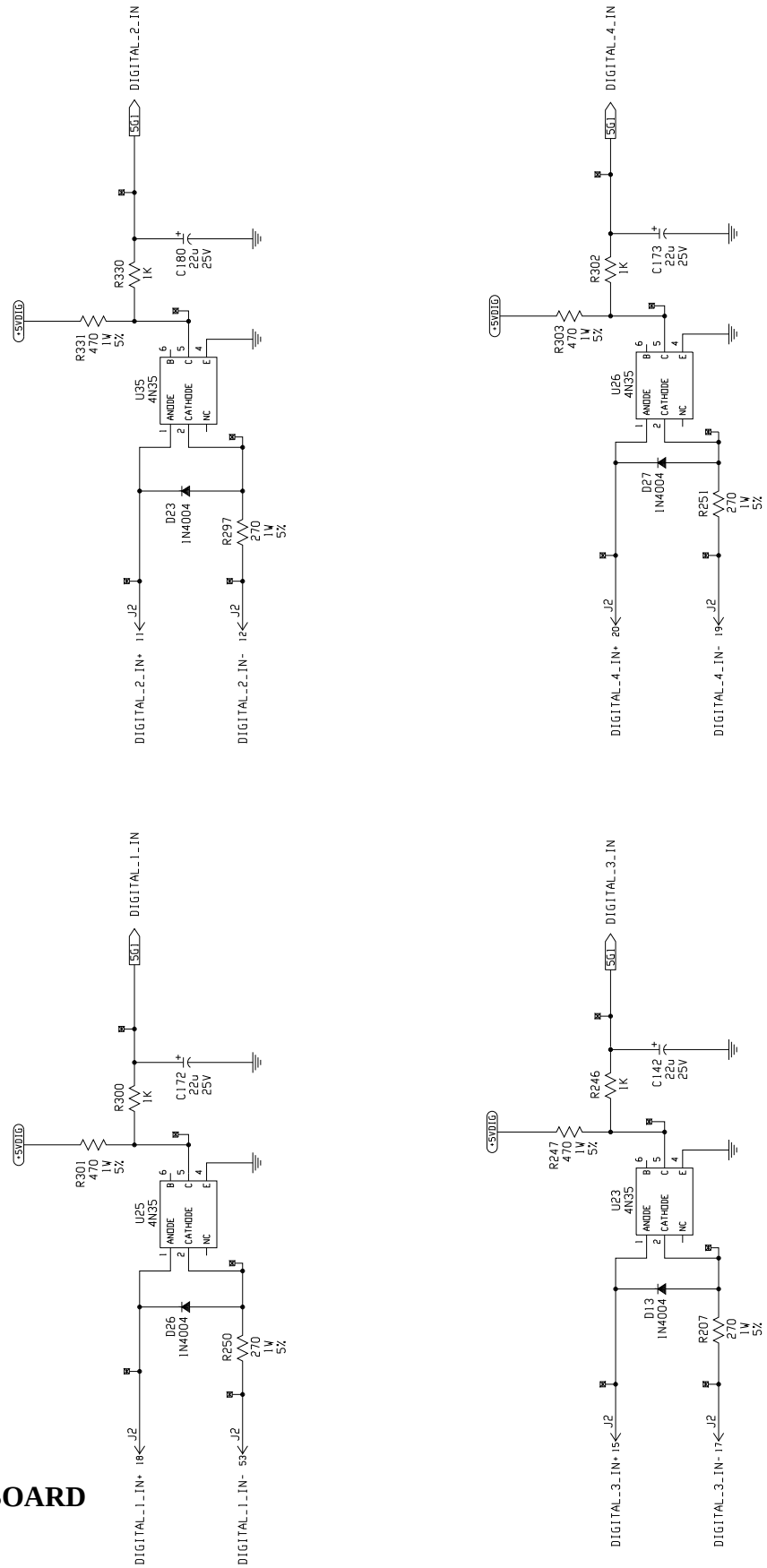
AUDIO SYSTEM BOARD
P29/7720037000
Sheet 21 of 30
Audio Matrix & VU Meter Detector Circuits
(772-0037-XXX-EC, Sh. 21 , Rev. A)



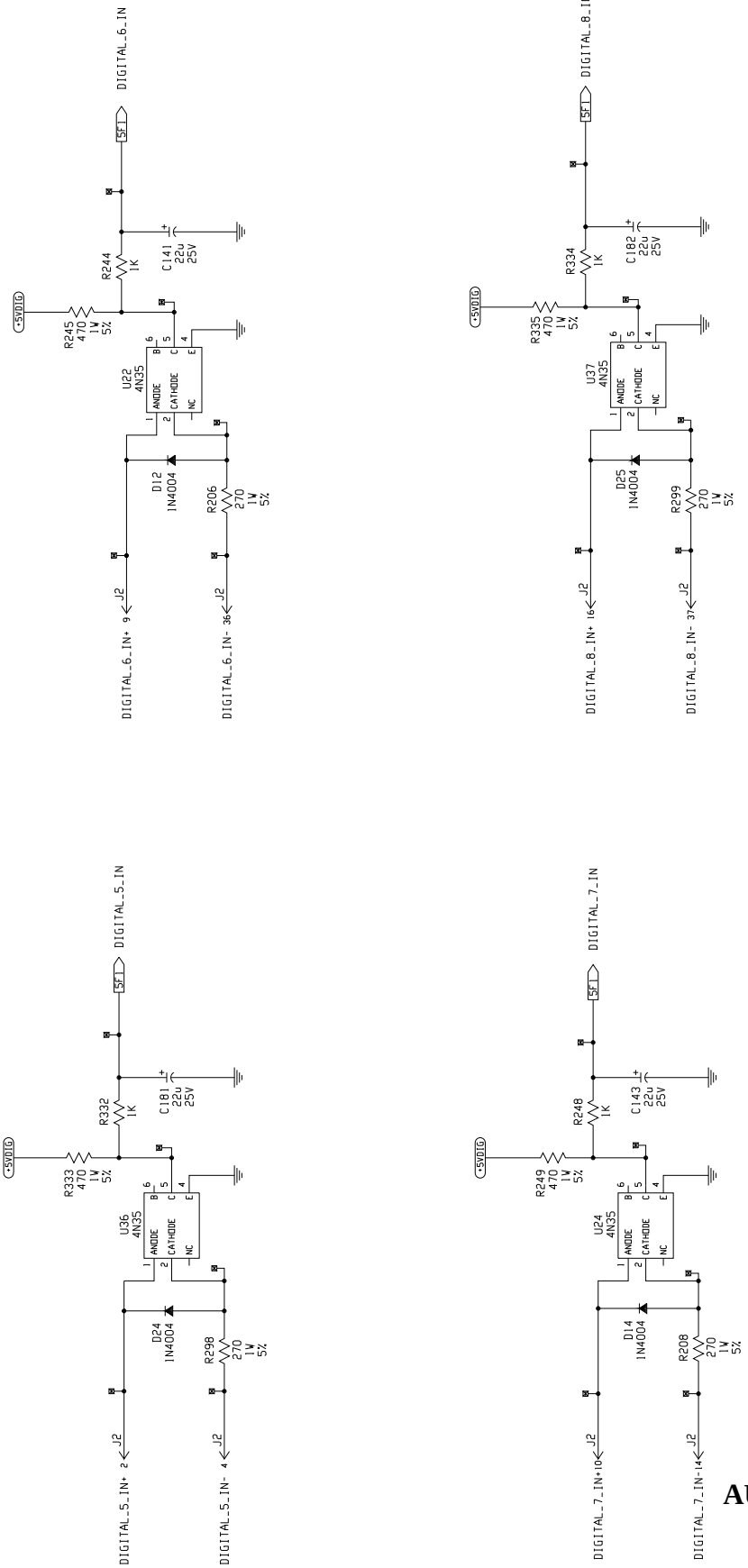
AUDIO SYSTEM BOARD
P29/7720037000
Sheet 22 of 30
Audio Output Circuits – Line 1 & 2 Drivers
(772-0037-XXX-EC, Sh. 22 , Rev. A)



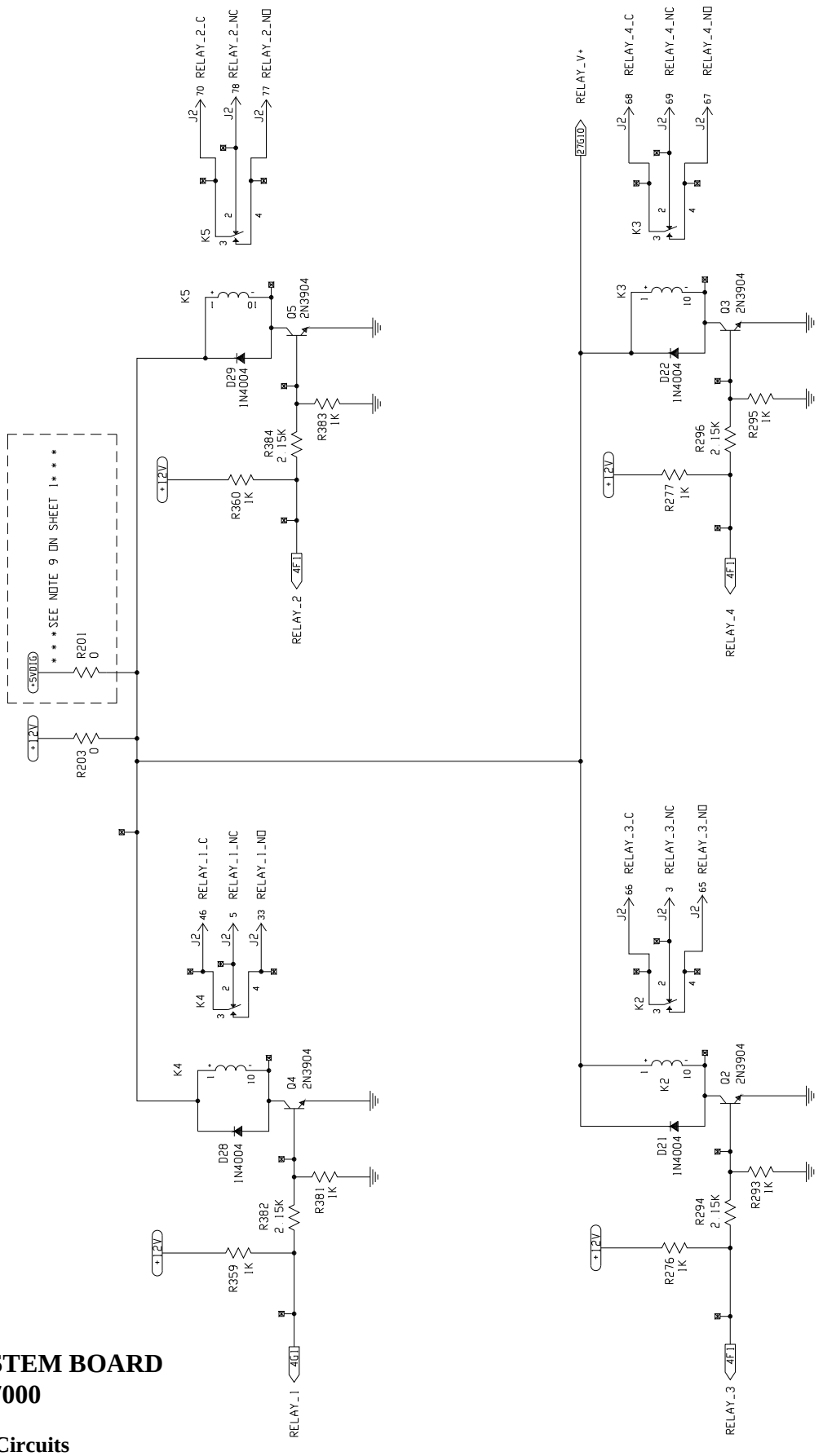
AUDIO SYSTEM BOARD
P29/7720037000
Sheet 23 of 30
Audio Output Circuits – Line 3 & 4 Drivers
(772-0037-XXX-EC, Sh. 23 , Rev. A)



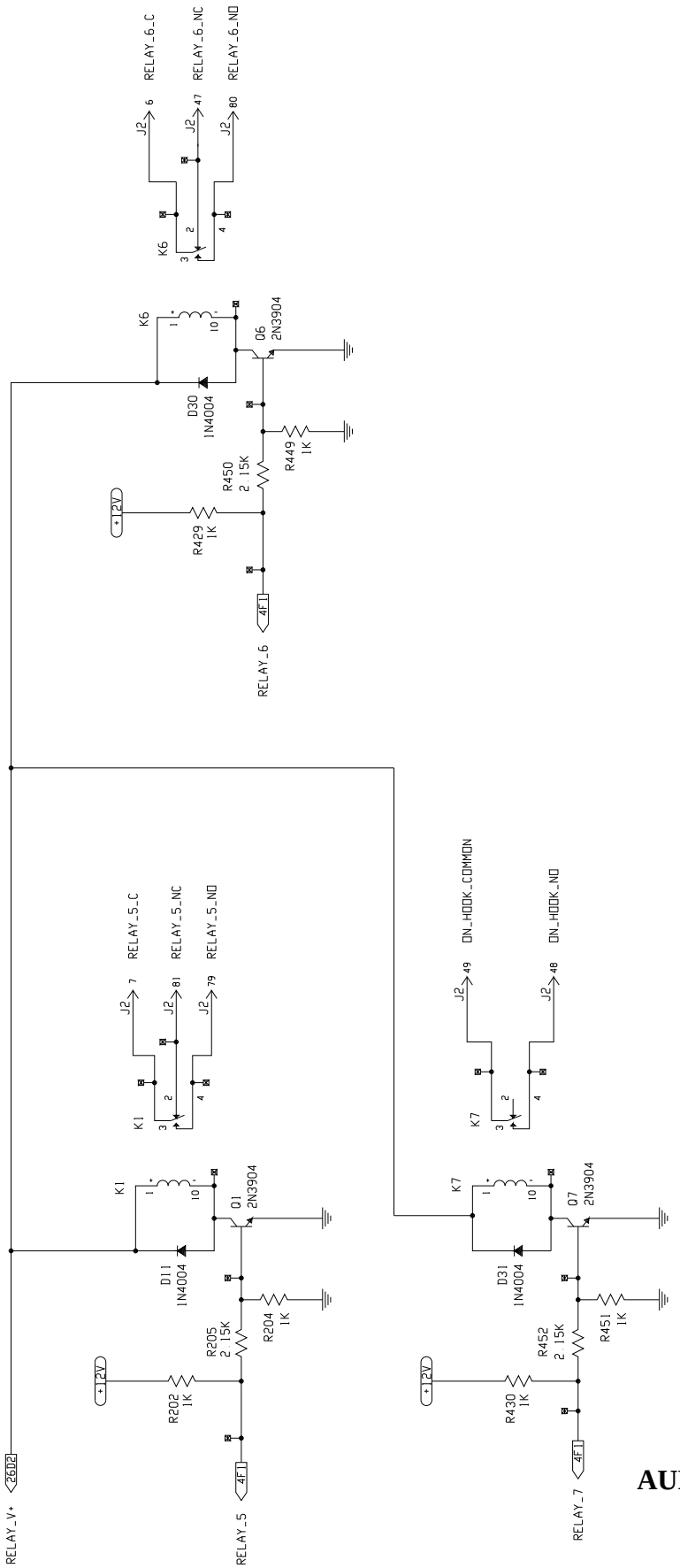
AUDIO SYSTEM BOARD
P29/7720037000
Sheet 24 of 30
Logic Interface Circuits – Digital Inputs
(772-0037-XXX-EC, Sh. 24 , Rev. A)



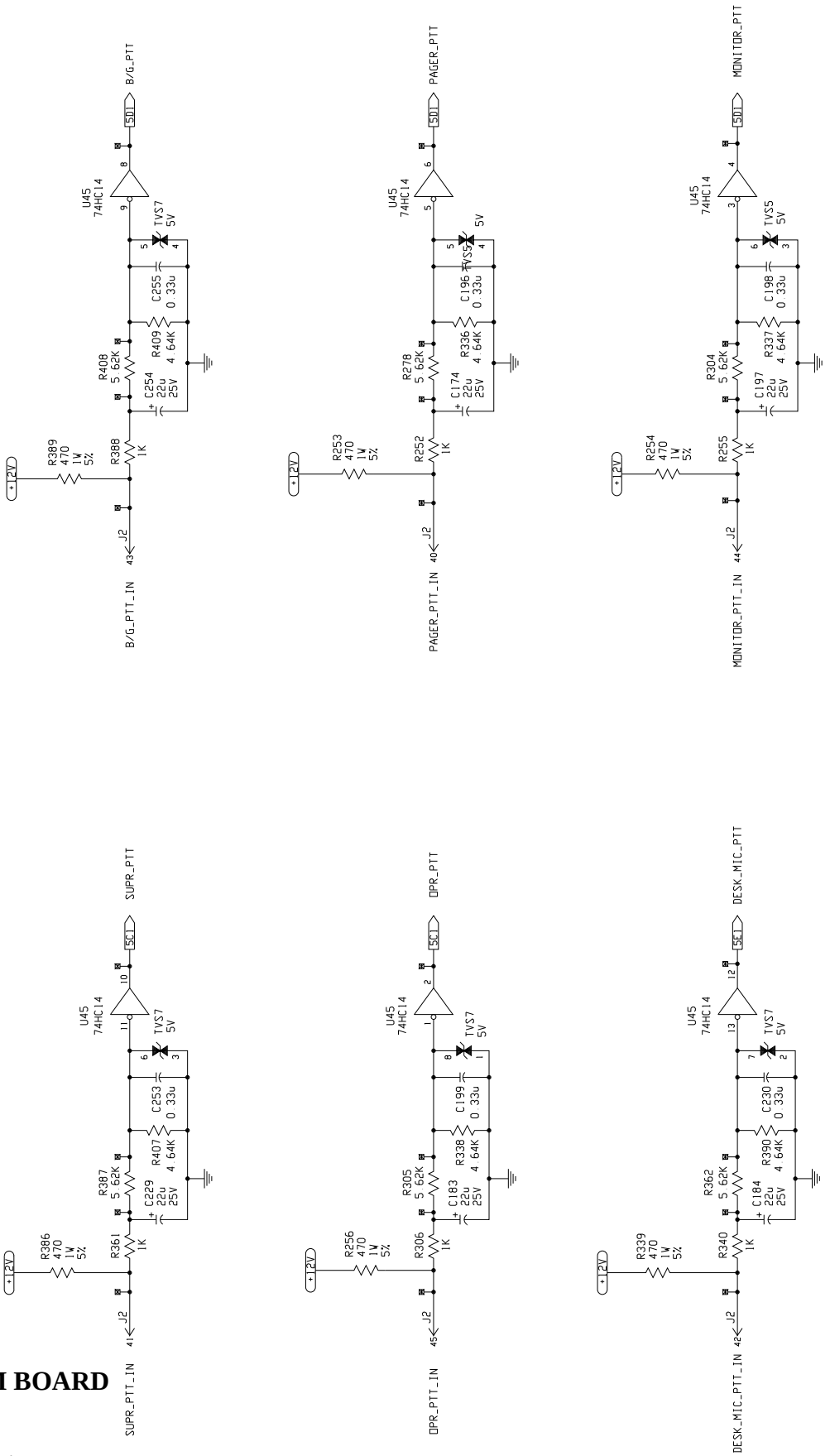
AUDIO SYSTEM BOARD
P29/7720037000
Sheet 25 of 30
Logic Interface Circuits – Digital Inputs
(772-0037-XXX-EC, Sh. 25 , Rev. A)



AUDIO SYSTEM BOARD
P29/7720037000
Sheet 26 of 30
Relay Output Circuits
(772-0037-XXX-EC, Sh. 26 , Rev. A)

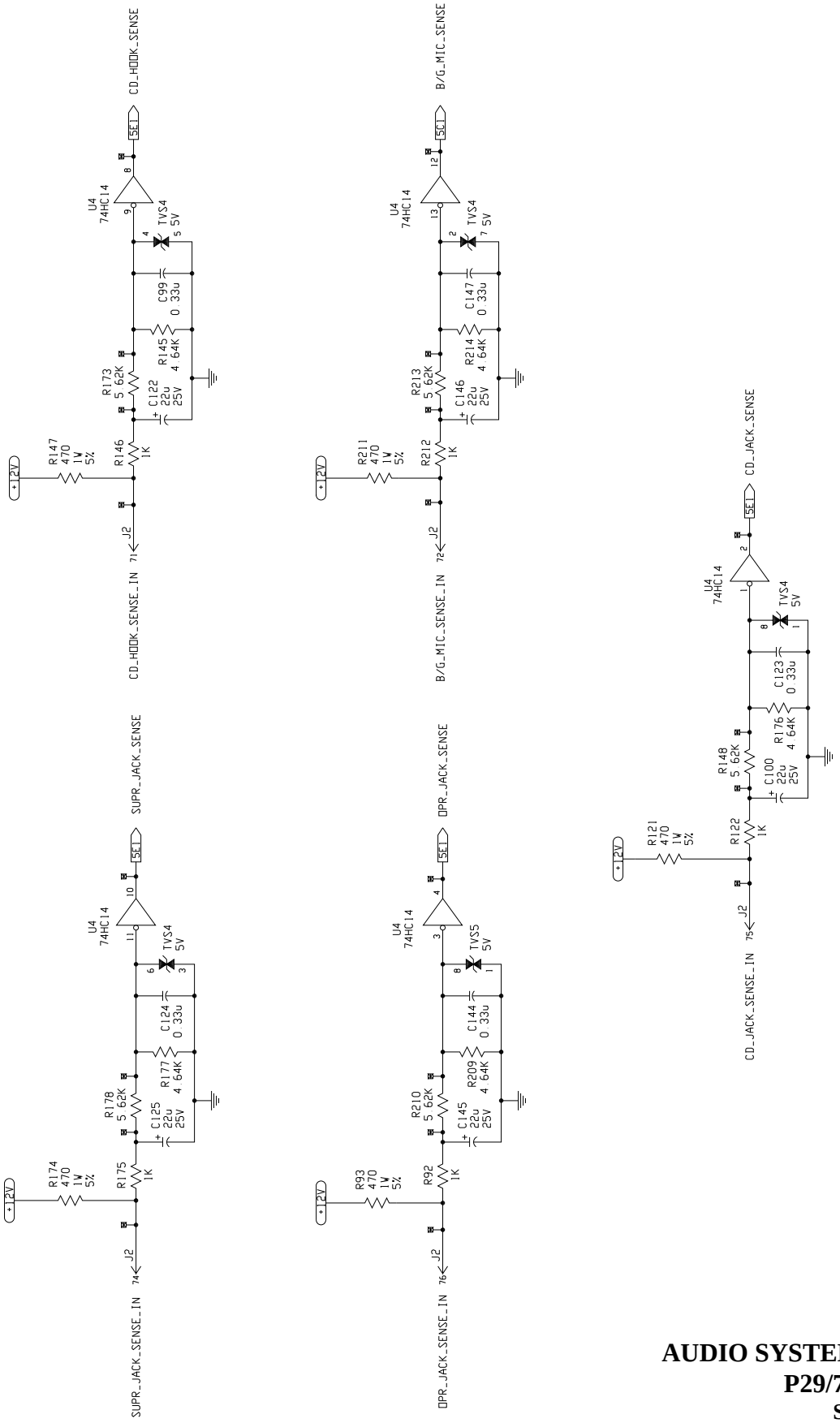


AUDIO SYSTEM BOARD
P29/7720037000
Sheet 27 of 30
Relay Output Circuits
(772-0037-XXX-EC, Sh. 27 , Rev. A)

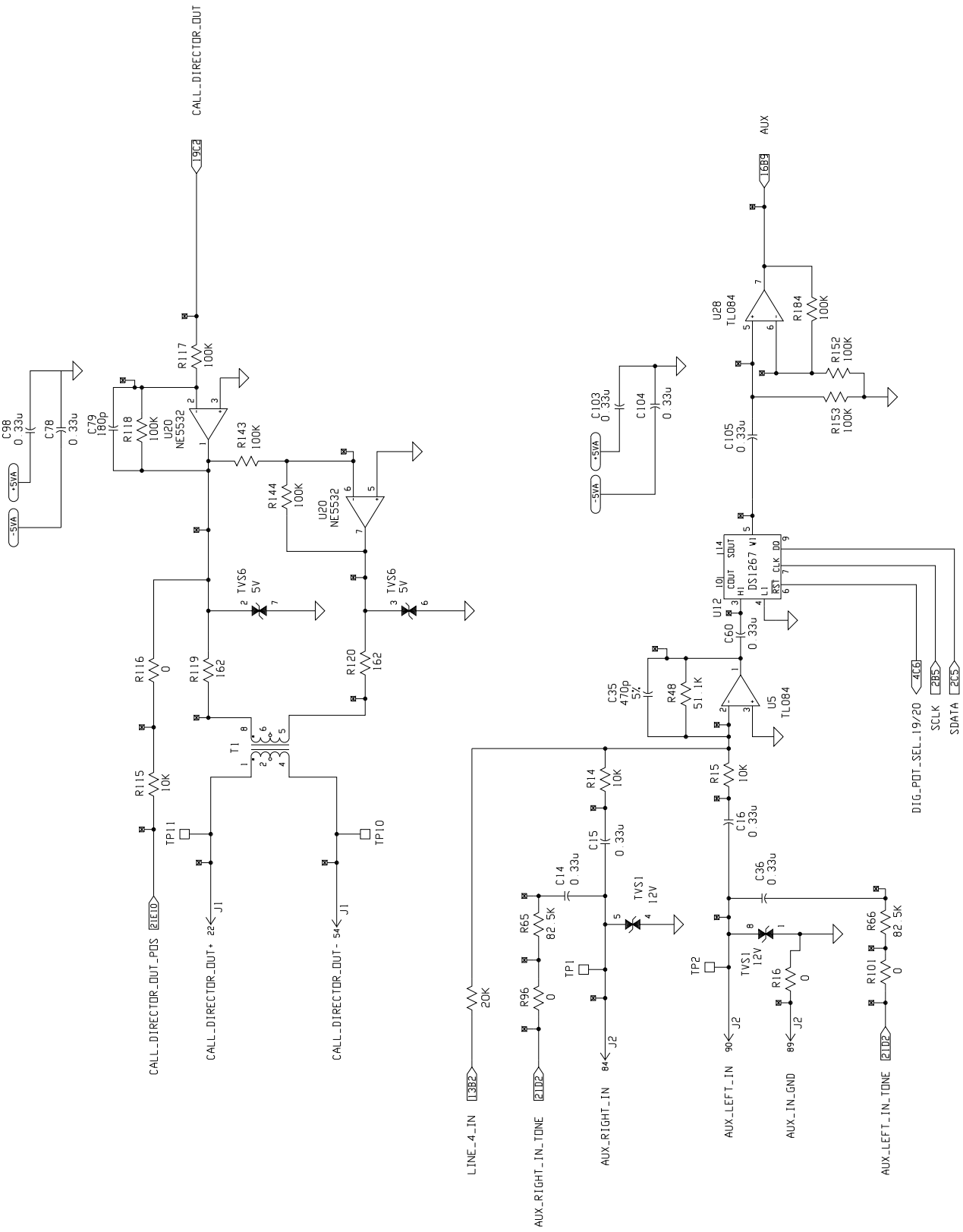


AUDIO SYSTEM BOARD
P29/7720037000
Sheet 28 of 30
Logic Interface Circuits – PTT Inputs

(772-0037-XXX-EC, Sh. 28 , Rev. A)



AUDIO SYSTEM BOARD
P29/7720037000
Sheet 29 of 30
Logic Interface Circuits – Sense Inputs
(772-0037-XXX-EC, Sh. 29 , Rev. A)



AUDIO SYSTEM BOARD
P29/7720037000

Sheet 30 of 30

Audio Circuits – Call Director Output Line Driver & Aux. Input

(772-0037-XXX-EC, Sh. 30 , Rev. A)

AUDIO SYSTEM BOARD
P29/7720037000 (350A1371P20), Rev. A

ISSUE 1

SYMBOL	PART NUMBER	DESCRIPTION
		---------- CAPACITORS ----------
C1	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C2	P29/31A1031J22	Chip, ceramic: 0.01 uF ±5%, 100 V.
C3	P29/3170218000	Electrolytic: 270 uF low ESR, radial leads, 16 V.
C4	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C5	P29/3170218000	Electrolytic: 270 uF low ESR, radial leads, 16 V.
C6	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C7	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C8 and C9	P29/3170218000	Electrolytic: 270 uF low ESR, radial leads, 16 V.
C10	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C11	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C12	P29/31A1041C32	Chip, ceramic: 0.1 uF ±10%, 50 V.
C13	P29/31A1031J22	Chip, ceramic: 0.01 uF ±5%, 100 V.
C14 thru C16	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C17	P29/31A4710J22	Chip, ceramic: 470 pF ±5%, 100 V.
C18	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C19	P29/31A4710J22	Chip, ceramic: 470 pF ±5%, 100 V.
C20 thru C23	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C24	P29/31A4710J22	Chip, ceramic: 470 pF ±5%, 100 V.
C25	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C26	P29/31A4710J22	Chip, ceramic: 470 pF ±5%, 100 V.
C27	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C28 and C29	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C30	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C31	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C32 and C33	P29/31B4750A3B	Chip, tantalum: 4.7 uF ±10%, 35 V.
C34	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C35	P29/31A4710J22	Chip, ceramic: 470 pF ±5%, 100 V.
C36 and C37	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C38	P29/31A1810J32	Chip, ceramic: 180 pF ±10%, 100 V.
C39	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C40	P29/31A1810J32	Chip, ceramic: 180 pF ±10%, 100 V.
C41 and C42	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C43	P29/31A1810J32	Chip, ceramic: 180 pF ±10%, 100 V.
C44 and C45	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C46	P29/31A1810J32	Chip, ceramic: 180 pF ±10%, 100 V.
C47 thru C49	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C50	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C51 and C52	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C53	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C54	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C55 and C56	P29/31B4750A3B	Chip, tantalum: 4.7 uF ±10%, 35 V.
C57	P29/31A1010J32	Chip, ceramic: 100 pF ±10%, 100 V.
C58	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C59	P29/31A1010J32	Chip, ceramic: 100 pF ±10%, 100 V.
C60 thru C63	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C64	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C65	P29/31A2221J32	Chip, ceramic: 2.2 nF ±10%, 100 V.
C66 and C67	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C69	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C70 thru C73	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C74 and C75	P29/31A2221J32	Chip, ceramic: 2.2 nF ±10%, 100 V.
C76	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C77	P29/31A1010J32	Chip, ceramic: 100 pF ±10%, 100 V.
C78	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C79	P29/31A1810J32	Chip, ceramic: 180 pF ±10%, 100 V.
C80	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C81 thru C88	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C89 and C90	P29/31A4710J22	Chip, ceramic: 470 pF ±5%, 100 V.
C91 thru C99	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C100	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C101 thru C106	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C107	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C108 and C109	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C110	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C111 thru C121	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C122	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C123 and C124	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C125	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C127 thru C130	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.

SYMBOL	PART NUMBER	DESCRIPTION
C131	P29/31A1010J32	Chip, ceramic: 100 pF ±10%, 100 V.
C132 and C133	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C134 thru C140	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C141 thru C143	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C144	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C145 and C146	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C147 thru C149	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C150	P29/31B4750A3B	Chip, tantalum: 4.7 uF ±10%, 35 V.
C151	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C152 and C153	P29/31B4750A3B	Chip, tantalum: 4.7 uF ±10%, 35 V.
C154 thru C156	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C157	P29/31A1810J32	Chip, ceramic: 180 pF ±10%, 100 V.
C158 thru C162	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C163 and C164	P29/31B4750A3B	Chip, tantalum: 4.7 uF ±10%, 35 V.
C165 and C166	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C167	P29/31A1010J32	Chip, ceramic: 100 pF ±10%, 100 V.
C168 thru C171	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C172 thru C174	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C175 and C176	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C177	P29/31A1010J32	Chip, ceramic: 100 pF ±10%, 100 V.
C178 and C179	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C180 thru C185	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C186 thru C194	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C195	P29/31A1810J32	Chip, ceramic: 180 pF ±10%, 100 V.
C196	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C197	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C198 thru C201	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C202	P29/31A2221J32	Chip, ceramic: 2.2 nF ±10%, 100 V.
C203	P29/31A1010J32	Chip, ceramic: 100 pF ±10%, 100 V.
C204 thru C209	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.

SYMBOL	PART NUMBER	DESCRIPTION
C210	P29/31A1810J32	Chip, ceramic: 180 pF ±10%, 100 V.
C211 thru C214	P29/31A1041C32	Chip, ceramic: 0.1 uF ±10%, 50 V.
C215 thru C217	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C218	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C219	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C220 thru C222	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C223	P29/31A1010J32	Chip, ceramic: 100 pF ±10%, 100 V.
C224 thru C228	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C229	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C230 thru C233	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C234 and C235	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C236 thru C239	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C240	P29/31A4710J22	Chip, ceramic: 470 pF ±5%, 100 V.
C241	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C242	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C243	P29/31A1010J32	Chip, ceramic: 100 pF ±10%, 100 V.
C244 thru C249	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C250	P29/31A1810J32	Chip, ceramic: 180 pF ±10%, 100 V.
C251 and C252	P29/31A1041C32	Chip, ceramic: 0.1 uF ±10%, 50 V.
C253	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C254	P29/31B226073B	Chip, tantalum: 22 uF ±10%, 20 V.
C255 thru C264	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C265	P29/31A1810J32	Chip, ceramic: 180 pF ±10%, 100 V.
C266 and C267	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C268 thru C273	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C274	P29/31A4710J22	Chip, ceramic: 470 pF ±5%, 100 V.
C275 thru C278	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C279 thru C282	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C283	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C285 and C286	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C287 thru C290	P29/31A1041C32	Chip, ceramic: 0.1 uF ±10%, 50 V.
C291 thru C294	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.

SYMBOL	PART NUMBER	DESCRIPTION
C295	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C296 thru C303	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C304 thru C307	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C308 thru C310	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C311 and C312	P29/31A3300J22	Chip, ceramic: 33 pF ±5%, 100 V.
C313	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C314	P29/31A1810J32	Chip, ceramic: 180 pF ±10%, 100 V.
C315 and C316	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C317 thru C323	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C324	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C326 thru C332	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C333	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C335 and C336	P29/31A3342C42	Chip, ceramic: 0.33 uF ±20%, 50 V.
C337 and C338	P29/31A4721J22	Chip, ceramic: 4.7 nF ±5%, 100 V.
C339 thru C343	P29/31A1810J32	Chip, ceramic: 180 pF ±10%, 100 V.
		---------- DIODES ----------
D1 and D2	P29/3420148002	Schottky: 3-amp.
D11 thru D16	P29/3420147000	Chip, silicon: 1N4004W.
D17 thru D20	P29/3420149000	Chip, Zener: 2.4-Volt, 500 mW.
D21 thru D31	P29/3420147000	Chip, silicon: 1N4004W.
D32 thru D35	P29/3420149000	Chip, Zener: 2.4-Volt, 500 mW.
		---------- FUSE ----------
F1	P29/3130009004	Thermistor: Polyswitch.
		---------- JACKS ----------
J1 and J2	P29/3800707096	Connector: 96-pin DIN, male contacts, right-angle mnt.
		---------- RELAYS ----------
K1 thru K7	P29/3230050000	Surface-mount: DPDT contacts, 12-Volt coil.
		---------- INDUCTORS ----------
L1	P29/3140031000	Coil, toroid: 100 uH.
L2	P29/3140023000	Coil: 220 uH.
L3	P29/3140031000	Coil, toroid: 100 uH.
L4	P29/3140023000	Coil: 220 uH.
L5	P29/3140031000	Coil, toroid: 100 uH.
L6	P29/3140023000	Coil: 220 uH.
L7 and L8	P29/3140034000	Surface-mount: ferrite bead, type 75 material.
L9	P29/3140035101	Chip, coil: 100 uH.
L10 thru L16	P29/3140034000	Surface-mount: ferrite bead, type 75 material.
		---------- LIGHT-EMITTING DIODE ----------
LED1	P29/3430059000	Green: Right-angle mounting.
		---------- TRANSISTORS ----------
Q1 thru Q8	P29/3440082000	Surface-mount, NPN: 2N3904, SOT-23 package.
		---------- RESISTORS ----------
R1	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R2	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R3	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R4	P29/30C6040201	Chip: 604 ohms ±1%, 1/8 W.
R5	P29/30C5621201	Chip: 5.62K ohms ±1%, 1/8 W.
R6	P29/30C4641201	Chip: 4.64K ohms ±1%, 1/8 W.
R7	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R8	P29/30C5621201	Chip: 5.62K ohms ±1%, 1/8 W.
R9 thru R15	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R16 and R17	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R18	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R19 and R20	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R21	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R22 and R23	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R24	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R25 and R26	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R27	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R28	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R29	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R30	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R31	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R32	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R33	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R34	P29/30C3480201	Chip: 348 ohms ±1%, 1/8 W.
R35	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R36	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R37	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R38	P29/30C3480201	Chip: 348 ohms ±1%, 1/8 W.

SYMBOL	PART NUMBER	DESCRIPTION
R39	P29/30F1500522	Chip: 150 ohms ±5%, 1 W.
R40	P29/30C6040201	Chip: 604 ohms ±1%, 1/8 W.
R41	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R42	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R43	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R44	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R45	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R46	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R47	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R48 and R49	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R50 thru R52	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R53	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R54 and R55	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R56	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R57	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R58	P29/30C3480201	Chip: 348 ohms ±1%, 1/8 W.
R59	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R60	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R61	P29/30C4641201	Chip: 4.64K ohms ±1%, 1/8 W.
R62 and R63	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R64	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R65 and R66	P29/30C8252201	Chip: 82.5K ohms ±1%, 1/8 W.
R67 thru R71	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R72	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R73 thru R77	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R78	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R79 thru R83	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R84 and R85	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R86	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R87 and R88	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R89	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R90	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R91	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R92	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R93	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R94 and R95	P29/30C6040201	Chip: 604 ohms ±1%, 1/8 W.
R96	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R97	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.

SYMBOL	PART NUMBER	DESCRIPTION
R98	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R99	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R100	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R101 and R102	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R103	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R104	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R105	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R106	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R107	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R108	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R109	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R110	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R111 and R112	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R113	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R114 and R115	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R116	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R117 and R118	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R119 and R120	P29/30C1620201	Chip: 162 ohms ±1%, 1/8 W.
R121	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R122	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R123 thru R125	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R126	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R127 thru R130	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R131 thru R133	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R134	P29/30C3480201	Chip: 348 ohms ±1%, 1/8 W.
R135 thru R138	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R139	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R140	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R141	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R142 thru R144	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R145	P29/30C4641201	Chip: 4.64K ohms ±1%, 1/8 W.
R146	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R147	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R148	P29/30C5621201	Chip: 5.62K ohms ±1%, 1/8 W.
R149	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R150	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R151 and R153	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R154	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.

SYMBOL	PART NUMBER	DESCRIPTION
R155 thru R160	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R161 and R162	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R163	P29/30F1500522	Chip: 150 ohms ±5%, 1 W.
R164 thru R166	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R167	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R168	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R169	P29/30C3161201	Chip: 3.16K ohms ±1%, 1/8 W.
R170	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R171	P29/30C3480201	Chip: 348 ohms ±1%, 1/8 W.
R172	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R173	P29/30C5621201	Chip: 5.62K ohms ±1%, 1/8 W.
R174	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R175	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R176 and R177	P29/30C4641201	Chip: 4.64K ohms ±1%, 1/8 W.
R178	P29/30C5621201	Chip: 5.62K ohms ±1%, 1/8 W.
R179	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R180	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R181 thru R185	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R186	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R187	P29/30C5622201	Chip: 56.2K ohms ±1%, 1/8 W.
R188	P29/30C7501201	Chip: 7.50K ohms ±1%, 1/8 W.
R189 and R190	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R191	P29/30C7501201	Chip: 7.50K ohms ±1%, 1/8 W.
R192	P29/30C5622201	Chip: 56.2K ohms ±1%, 1/8 W.
R193	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R194	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R195	P29/30C7501201	Chip: 7.50K ohms ±1%, 1/8 W.
R196	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R197	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R198	P29/30C3480201	Chip: 348 ohms ±1%, 1/8 W.
R199	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R200	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R202	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R203	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R204	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R205	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R206 thru R208	P29/30F2700522	Chip: 270 ohms ±5%, 1 W.
R209	P29/30C4641201	Chip: 4.64K ohms ±1%, 1/8 W.
R210	P29/30C5621201	Chip: 5.62K ohms ±1%, 1/8 W.
R211	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R212	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R213	P29/30C5621201	Chip: 5.62K ohms ±1%, 1/8 W.

SYMBOL	PART NUMBER	DESCRIPTION
R214	P29/30C4641201	Chip: 4.64K ohms ±1%, 1/8 W.
R215	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R216	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R217	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R218	P29/30C1963201	Chip: 196K ohms ±1%, 1/8 W.
R219	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R220	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R221 thru R225	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R226	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R227 and R228	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R229	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R230	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R231	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R232 and R233	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R234	P29/30C8252201	Chip: 82.5K ohms ±1%, 1/8 W.
R235 thru R238	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R239	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R240 and R241	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R242	P29/30C1620201	Chip: 162 ohms ±1%, 1/8 W.
R243	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R244	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R245	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R246	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R247	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R248	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R249	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R250 and R251	P29/30F2700522	Chip: 270 ohms ±5%, 1 W.
R252	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R253 and R254	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R255	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R256	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R257 and R260	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R261	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R262	P29/30C8252201	Chip: 82.5K ohms ±1%, 1/8 W.
R263	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R264	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R265	P29/30C8252201	Chip: 82.5K ohms ±1%, 1/8 W.
R266 and R267	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R267	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R268	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.

SYMBOL	PART NUMBER	DESCRIPTION
R269	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R270 and R272	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R273	P29/30C1620201	Chip: 162 ohms ±1%, 1/8 W.
R274	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R275	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R276 and R277	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R278	P29/30C5621201	Chip: 5.62K ohms ±1%, 1/8 W.
R279 and R280	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R281	P29/30C8252201	Chip: 82.5K ohms ±1%, 1/8 W.
R282	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R283	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R284 and R285	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R286 and R287	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R288	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R289	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R290 and R291	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R292	P29/30C1620201	Chip: 162 ohms ±1%, 1/8 W.
R293	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R294	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R295	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R296	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R297 thru R299	P29/30F2700522	Chip: 270 ohms ±5%, 1 W.
R300	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R301	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R302	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R303	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R304 and R305	P29/30C5621201	Chip: 5.62K ohms ±1%, 1/8 W.
R306	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R307	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R308	P29/30C5119201	Chip: 51.1 ohms ±1%, 1/8 W.
R309	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R310	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R311 and R312	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R313	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R314 and R315	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R316	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R317 and R318	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).

SYMBOL	PART NUMBER	DESCRIPTION
R319 thru R322	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R323	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R324 thru R326	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R327	P29/30C1620201	Chip: 162 ohms ±1%, 1/8 W.
R328	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R329	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R330	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R331	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R332	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R333	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R334	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R335	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R336 thru R338	P29/30C4641201	Chip: 4.64K ohms ±1%, 1/8 W.
R339	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R340	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R341	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R342	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R343 and R344	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R345	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R346 thru R347	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R348	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R349 thru R354	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R355	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R356 and R357	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R358	P29/30C1620201	Chip: 162 ohms ±1%, 1/8 W.
R359 thru R361	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R362	P29/30C5621201	Chip: 5.62K ohms ±1%, 1/8 W.
R363	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R364	P29/30C5622201	Chip: 56.2K ohms ±1%, 1/8 W.
R365	P29/30C7501201	Chip: 7.50K ohms ±1%, 1/8 W.
R366	P29/30C4641201	Chip: 4.64K ohms ±1%, 1/8 W.
R367	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R368	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R369	P29/30C3161201	Chip: 3.16K ohms ±1%, 1/8 W.
R370	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R371 and R372	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R373	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R374	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R375 and R376	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.

SYMBOL	PART NUMBER	DESCRIPTION
R377	P29/30C1620201	Chip: 162 ohms ±1%, 1/8 W.
R378	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R379	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R380	P29/30C1620201	Chip: 162 ohms ±1%, 1/8 W.
R381	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R382	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R383	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R384	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R385	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R386	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R387	P29/30C5621201	Chip: 5.62K ohms ±1%, 1/8 W.
R388	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R389	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R390	P29/30C4641201	Chip: 4.64K ohms ±1%, 1/8 W.
R391	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R392	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R393 and R394	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R395	P29/30C1963201	Chip: 196K ohms ±1%, 1/8 W.
R396 thru R398	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R399	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R400	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R401	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R402 and R403	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R404	P29/30C1620201	Chip: 162 ohms ±1%, 1/8 W.
R405	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R406	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R407	P29/30C4641201	Chip: 4.64K ohms ±1%, 1/8 W.
R408	P29/30C5621201	Chip: 5.62K ohms ±1%, 1/8 W.
R409	P29/30C4641201	Chip: 4.64K ohms ±1%, 1/8 W.
R410	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R411	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R412 and R413	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R414	P29/30C1963201	Chip: 196K ohms ±1%, 1/8 W.
R415 and R416	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R417	P29/30C1963201	Chip: 196K ohms ±1%, 1/8 W.
R418 thru R423	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R424	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R425	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R426 thru R428	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R429 thru R431	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R432	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).

SYMBOL	PART NUMBER	DESCRIPTION
R433	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R434 and R435	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R436	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R437	P29/30C3161201	Chip: 3.16K ohms ±1%, 1/8 W.
R438	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R439	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R440 and R441	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R442	P29/30C1963201	Chip: 196K ohms ±1%, 1/8 W.
R443	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R444	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R445	P29/30C3480201	Chip: 348 ohms ±1%, 1/8 W.
R446	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R447	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R448	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R449	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R450	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R451	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R452	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R453	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R454	P29/30C5622201	Chip: 56.2K ohms ±1%, 1/8 W.
R455	P29/30C7501201	Chip: 7.50K ohms ±1%, 1/8 W.
R456	P29/30C4641201	Chip: 4.64K ohms ±1%, 1/8 W.
R457 and R458	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R459	P29/30C1963201	Chip: 196K ohms ±1%, 1/8 W.
R460	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R461	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R462	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R463	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R464	P29/30C3480201	Chip: 348 ohms ±1%, 1/8 W.
R465	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R466	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R467	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R468	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R469	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R470	P29/30C1963201	Chip: 196K ohms ±1%, 1/8 W.
R471	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R472	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R473	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R474	P29/30C3480201	Chip: 348 ohms ±1%, 1/8 W.
R475	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R476	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R477	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R478	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R479	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R480 thru R482	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).

SYMBOL	PART NUMBER	DESCRIPTION
R483 and R484	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R485	P29/30C1963201	Chip: 196K ohms ±1%, 1/8 W.
R486	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R487	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R488	P29/30C1002201	Chip: 10K ohms ±1%, 1/8 W.
R489 and R490	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R491	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R492 and R493	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R494	P29/30C1963201	Chip: 196K ohms ±1%, 1/8 W.
R495	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R496	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R497	P29/30C3480201	Chip: 348 ohms ±1%, 1/8 W.
R498	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R499	P29/30C2151201	Chip: 2.15K ohms ±1%, 1/8 W.
R500	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R501	P29/30F4700522	Chip: 470 ohms ±5%, 1 W.
R503	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R504 thru R506	P29/30C1001201	Chip: 1K ohms ±1%, 1/8 W.
R507	P29/30C1213201	Chip: 121K ohms ±1%, 1/8 W.
R508	P29/30C5112201	Chip: 51.1K ohms ±1%, 1/8 W.
R509 and R510	P29/30C1003201	Chip: 100K ohms ±1%, 1/8 W.
R513 and R515	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
R517	P29/30D0000201	Chip: 0 ohms, 1/8 W. (jumper).
		---------- SWITCH ----------
S1	P29/3670014000	Surface-mount: DIP, 4-position SPST.
		---------- TRANSFORMERS ----------
T1 thru T11	P29/3380074000	Isolation: 600-ohms.
		---------- TEST POINTS ----------
TP1 thru TP57	P29/3780023000	Loop: Insulated (orange).
		--- TRANSIENT VOLT. SUPPRESSERS --
TVS1	P29/3590069000	Surface-mount: 12 V.
TVS2	P29/3590070000	Surface-mount: 5 V.
TVS3	P29/3590069000	Surface-mount: 12 V.
TVS4 thru TVS8	P29/3590070000	Surface-mount: 5 V.
TVS9	P29/3590069000	Surface-mount: 12 V.
TVS10	P29/3590070000	Surface-mount: 5 V.
TVS11 and TVS12	P29/3590069000	Surface-mount: 12 V.
TVS13	P29/3590070000	Surface-mount: 5 V.

SYMBOL	PART NUMBER	DESCRIPTION
		---------- INTEGRATED CIRCUITS ----------
U1 and U2	P29/3590068000	Linear: Switching Regualtor; LT1076CT-5.
U4	P29/3590038000	Digital: Hex Schmitt-Trigger Inverter; 74HCT14.
U5 thru U7	P29/3480100601	Linear: Quad JFET-Input Op-Amp; TL084.
U8	P29/3590099000	Linear: Dual Low-Noise Op-Amp; NE5532.
U9	P29/3480110600	Digital/Linear: Dual Digital Pot, 50K; DS1267S050.
U10	P29/3480100601	Linear: Quad JFET-Input-Amp; TL084.
U11	P29/3590099000	Linear: Dual Low-Noise Op-Amp; NE5532.
U12 thru U14	P29/3480110600	Digital/Linear: Dual Digital Pot, 50K; DS1267S050.
U15	P29/3480100601	Linear: Quad JFET-Input-Amp; TL084.
U16 and U17	P29/3480110600	Digital/Linear: Dual Digital Pot, 50K; DS1267S050.
U18	P29/3480100601	Linear: Quad JFET-Input-Amp; TL084.
U19	P29/3480110600	Digital/Linear: Dual Digital Pot, 50K; DS1267S050.
U20	P29/3590099000	Linear: Dual Low-Noise Op-Amp; NE5532.
U21	P29/3480110600	Digital/Linear: Dual Digital Pot, 50K; DS1267S050.
U22 thru U26	P29/3450028600	Linear: Optocoupler; 4N35.
U27	P29/3480110600	Digital/Linear: Dual Digital Pot, 50K; DS1267S050.
U28	P29/3480100601	Linear: Quad JFET-Input-Amp; TL084.
U29 and U30	P29/3590091000	Linear: Dual Transconductance Op-Amp; LM13700.
U31	P29/3480100601	Linear: Quad JFET-Input-Amp; TL084.
U32	P29/3480110600	Digital/Linear: Dual Digital Pot, 50K; DS1267S050.
U33 and U34	P29/3590099000	Linear: Dual Low-Noise Op-Amp; NE5532.
U35 thru U37	P29/3450028600	Linear: Optocoupler; 4N35.
U38	P29/3590065000	Converter: 12-Bit A/D; ADS574.
U39 and U40	P29/3590063000	Digital: 8 x 8 Analog Switch; MT8808.
U41	P29/3480100601	Linear: Quad JFET-Input-Amp; TL084.
U42	P29/3590097000	Digital: 8-Bit Addressable Latch; 74HC259.
U43	P29/3580129000	Digital: Octal Non-Inverting Buffer; 74HC541.
U44	P29/3480154600	Digital: Dual RS-232 Transceiver; MAX202.
U45	P29/3590038000	Digital: Hex Schmitt-Trigger Inverter; 74HCT14.
U46	P29/3590064000	Linear: Sinewave Generator; ML2036.
U47	P29/3480100601	Linear: Quad JFET-Input-Amp; TL084.
U48 and U49	P29/3590063000	Digital: 8 x 8 Analog Switch; MT8808.

SYMBOL	PART NUMBER	DESCRIPTION
U50	P29/3480100601	Linear: Quad JFET-Input-Amp; TL084.
U51	P29/3480110600	Digital/Linear: Dual Digital Pot, 50K; DS1267S050.
U52 and U53	P29/3590099000	Linear: Dual Low-Noise Op-Amp; NE5532.
U54	P29/3580129000	Digital: Octal Non-Inverting Buffer; 74HC541.
U55	P29/3480109600	Digital: Watchdog Timer; LTC690.
U56	P29/3580121800	Digital: 8-Bit Microcontroller: 80C32.
U57	P29/3590098000	Digital: Serial EEPROM; ST93C46.
U58	P29/3590064000	Linear: Sinewave Generator; ML2036.
U59	P29/3550026000	Digital: Octal Data Flip-Flop; 74HC373.
U60	P29/3480110600	Digital/Linear: Dual Digital Pot, 50K; DS1267S050.
U61 and U62	P29/3590063000	Digital: 8 x 8 Analog Switch; MT8808.
U63 and U64	P29/3480100601	Linear: Quad JFET-Input-Amp; TL084.
U65	P29/3480110600	Digital/Linear: Dual Digital Pot, 50K; DS1267S050.
U66	P29/3480100601	Linear: Quad JFET-Input-Amp; TL084.
U67	P29/3480110600	Digital/Linear: Dual Digital Pot, 50K; DS1267S050.
U68	P29/3480154600	Digital: Dual RS-232 Transceiver; MAX202.
U69	P29/3590095000	Digital: RS-485 Transceiver; MAX490.
U70	P29/3580129000	Digital: Octal Non-Inverting Buffer; 74HC541.
U71	P29/3590100000	Digital: Serial Communications Controlller; 82530.
U72	P29/3590066000	Digital: Keyboard/Display Interface; P8279.
U73	P29/3590038000	Digital: Hex Schmitt-Trigger Inverter; 74HCT14.
U74	P29/3550035600	Digital: Dual 4-Bit Binary Counter; 74HC393.
U75	P29/3550022600	Digital: Quad 2-Input OR Gate; MC74HC32.
U76	P29/3550014600	Digital: 3-to-8 Line Decoder; MC74HC138.
U77	P29/3580119600	Digital: 32K x 8-Bit Static RAM; TC55257BFL-10L.
U78	P29/3590096000	Digital: 4-to-8 Line Decoder; 74HC4514.
U79 thru U82	P29/3590063000	Digital: 8 x 8 Analog Switch; MT8808.
U83	P29/3550022600	Digital: Quad 2-Input OR Gate; MC74HC32.
U84	P29/3590109001	Digital: EPROM (Programmed).
U86	P29/3580129000	Digital: Octal Non-Inverting Buffer; 74HC541.
U87 and U88	P29/3550015600	Digital: Octal Data Flip-Flop; 74HC574.
U89	P29/3480100601	Linear: Quad JFET-Input-Amp; TL084.
U90	P29/3480110600	Digital/Linear: Dual Digital Pot, 50K; DS1267S050.
		---------- IC SOCKETS ----------
XU56	P29/3740078044	Surface-mount, IC: PLCC 44-pin.
XU84 and XU85	P29/3740078032	Surface-mount, IC: PLCC 32-pin.
		---------- CRYSTAL ----------
Y1	P29/3300036000	Surface-mount: 14.7456 MHz.
		---------- MISCELLANEOUS ----------
	P29/6110113000	Latch: card ejector tab. (Qty. = 2)
	P29/6120058000	Heatsink: TO-220, push-on. (Qty. = 2. Used with U1 and U2.)

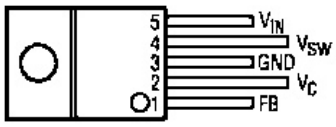
PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter" which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

Rev. A **AUDIO SYSTEM BOARD P29/7720037000**
Initial production release.

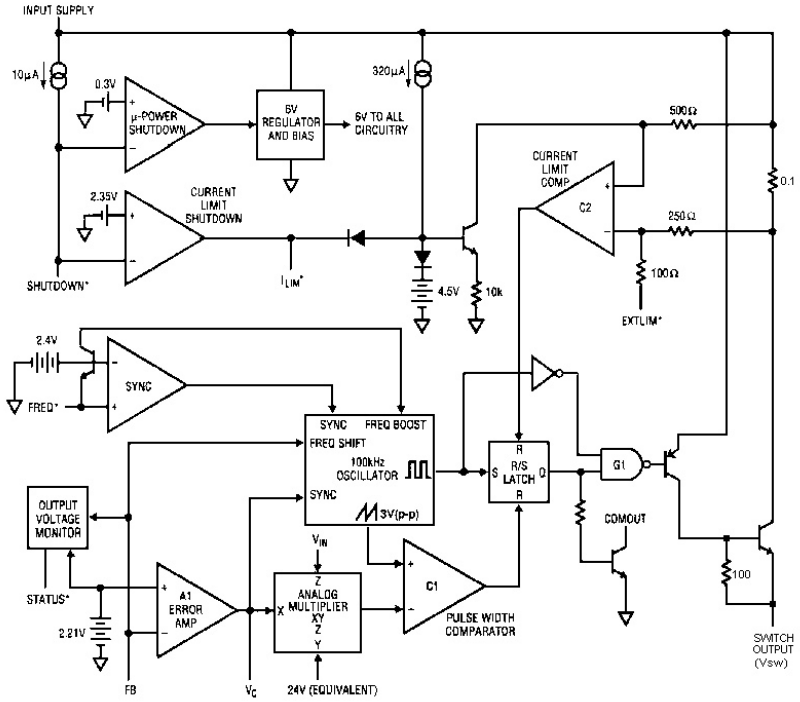
U1 & U2
SWITCHING REGULATOR
P29/3590068000 (LT1076)

PIN-OUT

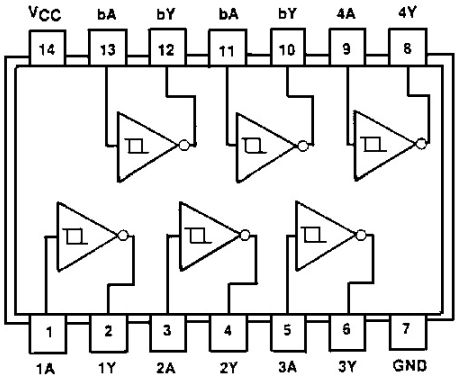


(5-LEAD TO-220 PACKAGE; FRONT VIEW)

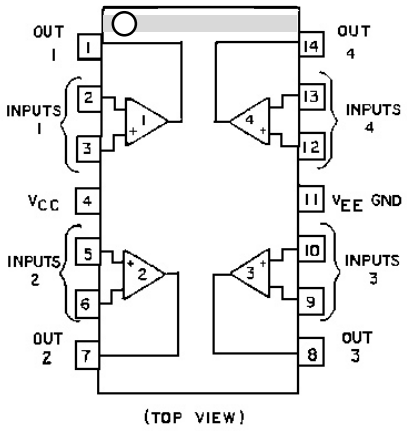
BLOCK DIAGRAM



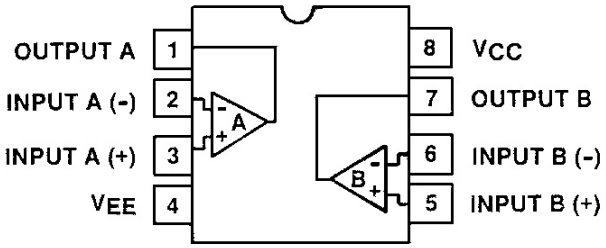
U4, U45 & U73
HEX SCHMITT-TRIGGER INVERTER
P29/3590038000 (74HCT14)



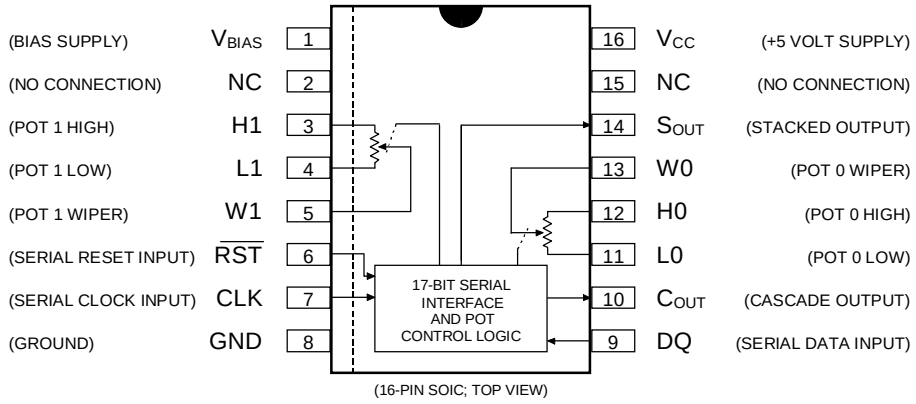
U5 – U7, U10, U15, U18, U28, U31, U41, U47, U50, U63, U64, U66 & U89
QUAD JFET-INPUT OP-AMP
P29/3480100601 (TL084)



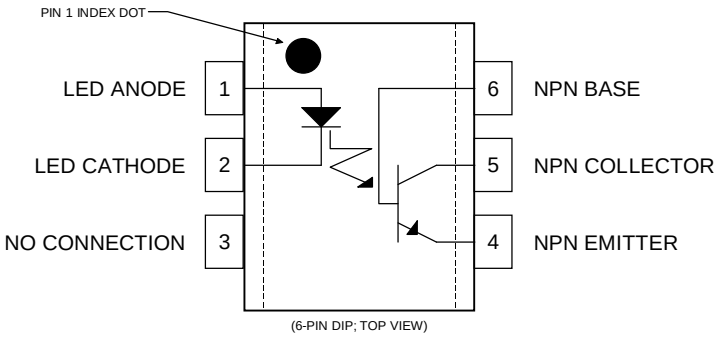
U8, U11, U20, U33, U34, U52 & U53
DUAL LOW-NOISE OP-AMP
P29/3590099000 (NE5532)



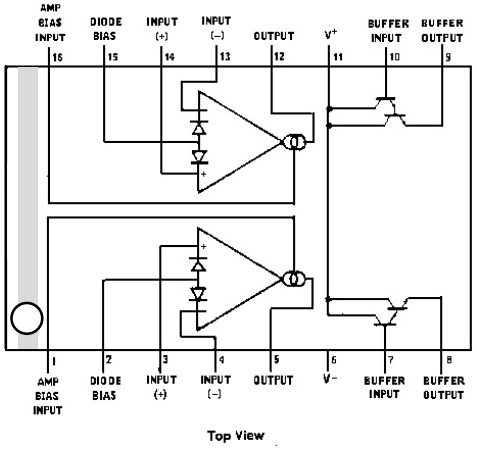
U9, U12 – U14, U16, U17, U19, U21, U27, U32, U51, U60, U65, U67, U90
DUAL DIGITAL POTENTIOMETER
P29/3480110600 (DS1267)



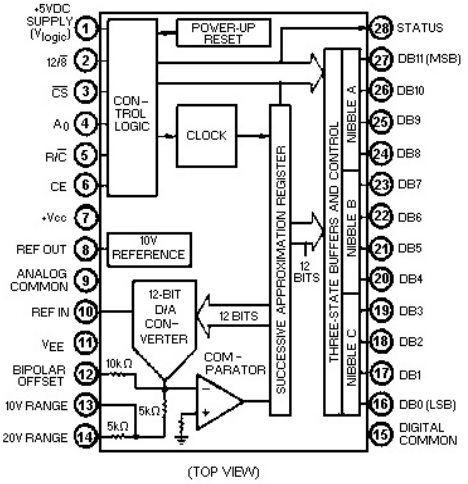
U22 – U26 & U35 – U37
OPTOCOUPLER
P29/3450028600 (4N35)



U29 & U30
DUAL TRANSCONDUCTANCE OP AMP
P29/3590091000 (LM13700)

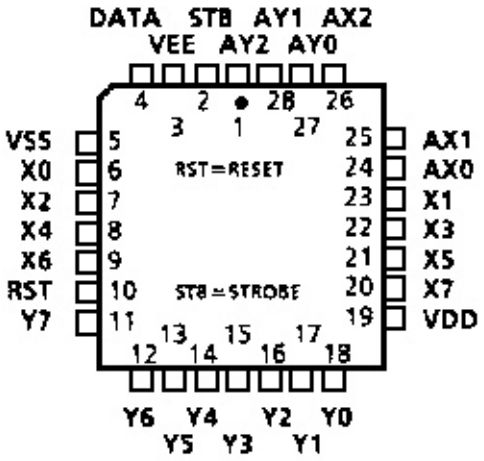


U38
12-BIT A/D CONVERTER
P29/3590065000 (ADS574)



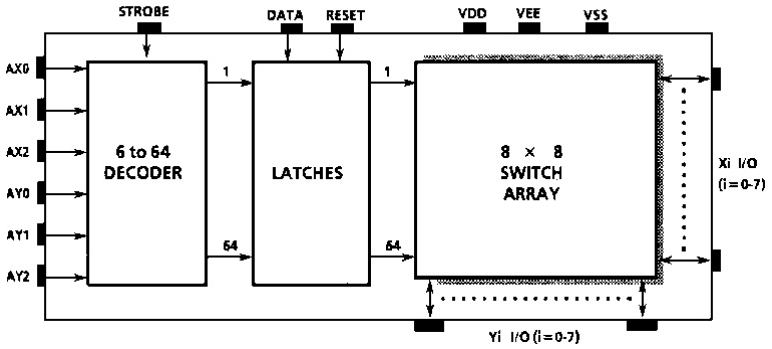
U39, U40, U48, U49, U61, U62, U79 – U82
8 X 8 ANALOG SWITCH
P29/3590063000 (MT8808)

PIN-OUT

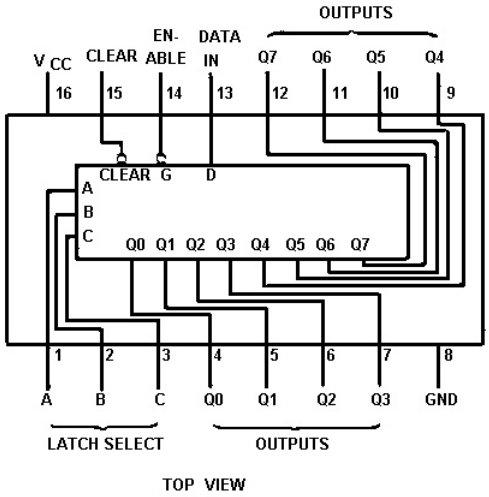


(28-PIN PLCC PACKAGE; TOP VIEW)

BLOCK DIAGRAM



U42
8-BIT ADDRESSABLE LATCH
P29/3590097000 (74HC259)



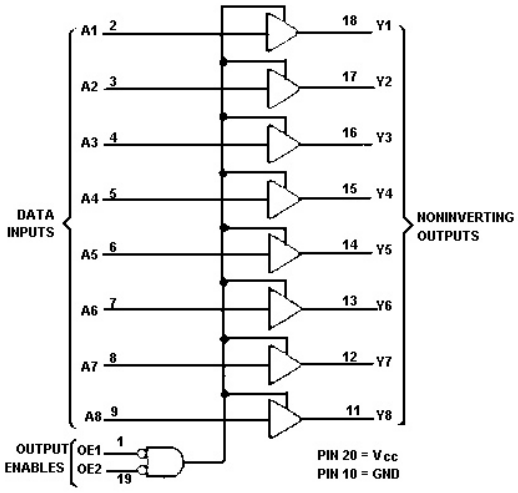
TOP VIEW

TRUTH TABLE

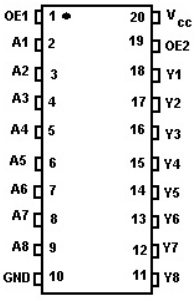
Inputs Clear	Inputs $\overline{G}$	Outputs of Addressed Latch	Each Other Output	Function
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Decoder
L	H	L	L	Clear

U43, U54, U70, U86
OCTAL TRI-STATE NON-INVERTING BUFFER
P29/3580129000 (74HC541)

LOGIC DIAGRAM



PIN ASSIGNMENT



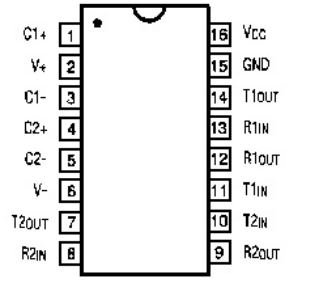
FUNCTION TABLE

Inputs			Ouput
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

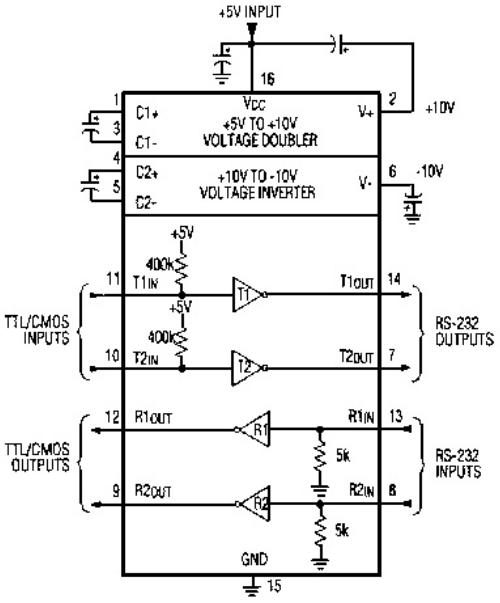
Z = high impedance
X = don't care

U44 & U68
DUAL RS-232 TRANSCEIVER WITH CHARGE-PUMP
P29/3480154600 (MAX202)

PIN-OUT

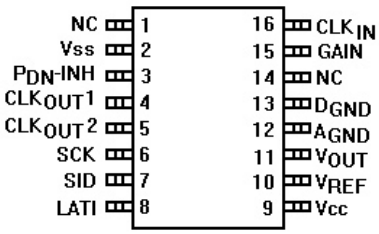


(16-PIN DIP/SOWIDE SO PACKAGE; TOP VIEW)



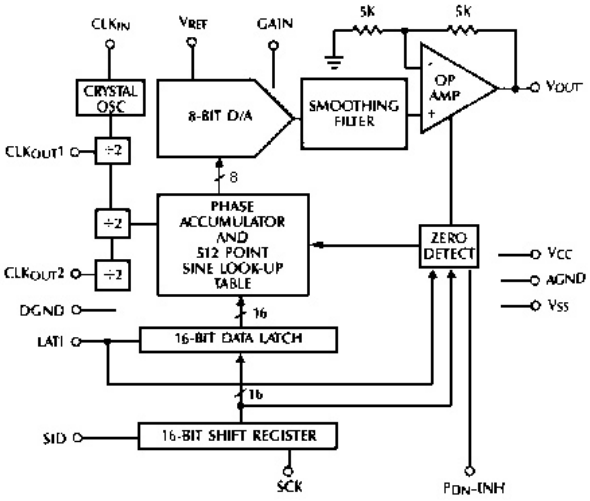
U46 & U58
PROGRAMMABLE SINEWAVE GENERATOR
P29/3590064000 (ML2036)

PIN-OUT



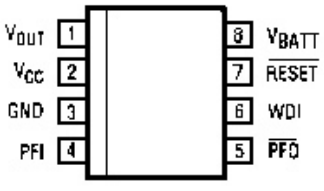
(16-PIN SO PACKAGE; TOP VIEW)

BLOCK DIAGRAM



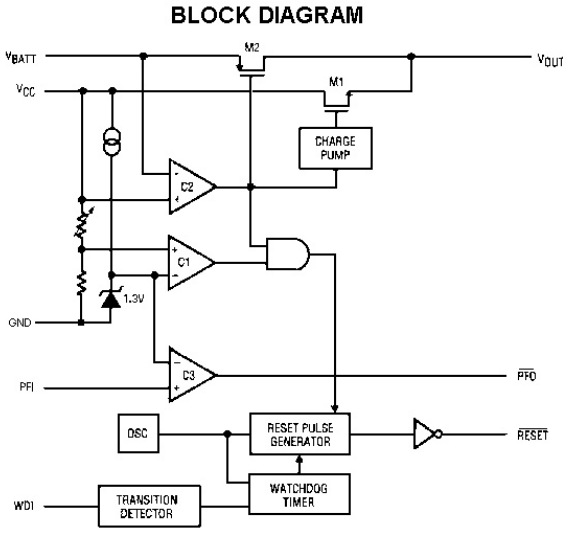
U55
MICROPROCESSOR SUPERVISORY / WATCHDOG TIMER
P29/3480109600 (LTC690)

PIN-OUT

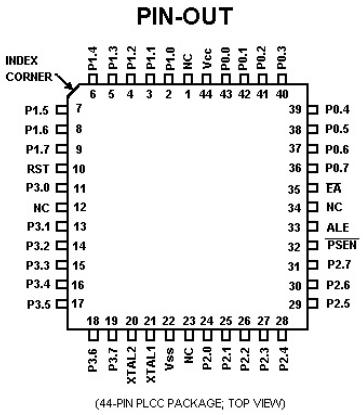


(8-PIN SO PACKAGE; TOP VIEW)

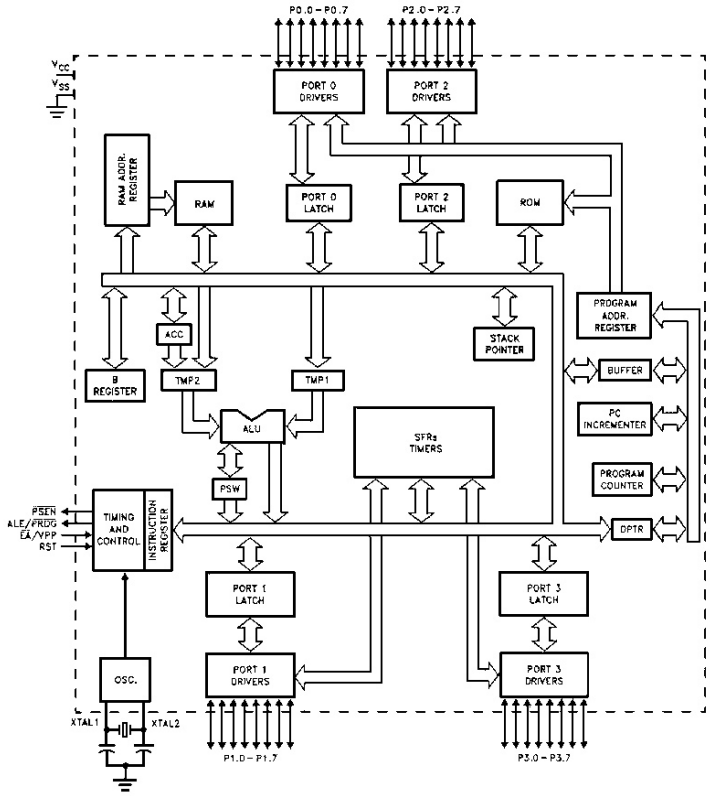
BLOCK DIAGRAM



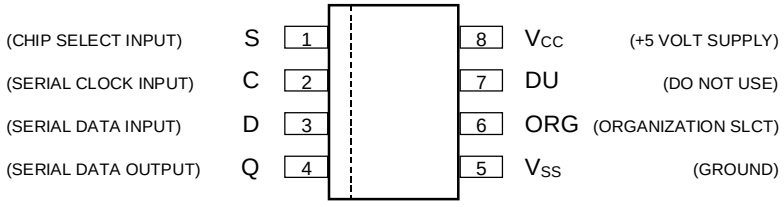
U56
8-BIT MICROCONTROLLER
P29/3580121800 (80C32)



(44-PIN PLCC PACKAGE; TOP VIEW)



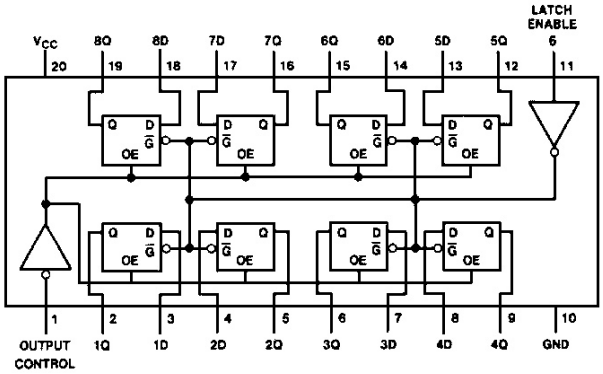
U57
SERIAL EEPROM
P29/3590098000 (ST93C46)



(8-PIN SOIC; TOP VIEW)

U59
OCTAL DATA FLIP-FLOP
P29/3550026000 (74HC373)

PIN-OUT

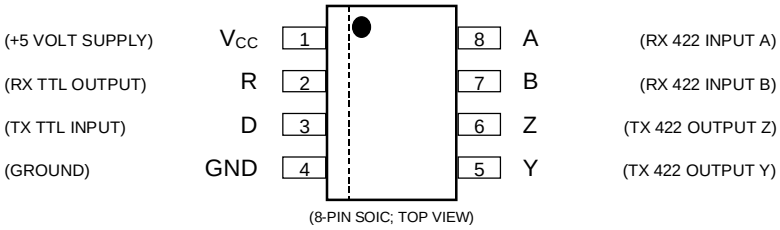


TRUTH TABLE

Output Control	Latch Enable	Data	373 Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level
Q_0 = level of output before steady-state input conditions were established
Z = high impedance

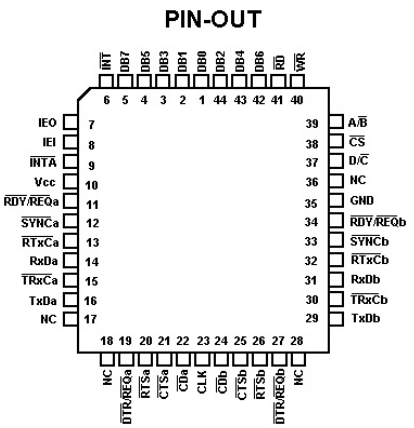
U69
RS-422/485 TRANSCEIVER
P29/3590095000 (MAX490)



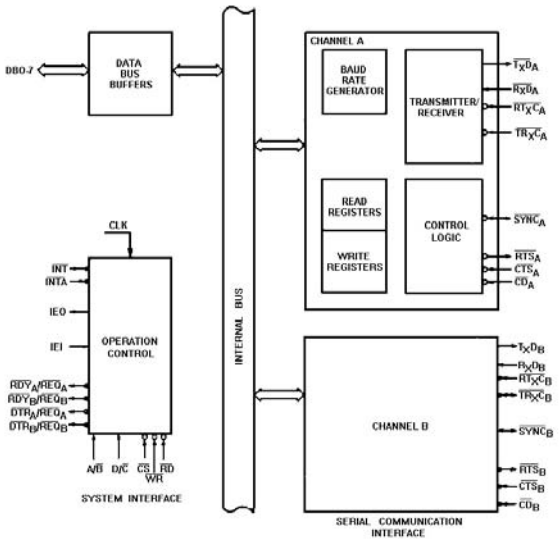
(8-PIN SOIC; TOP VIEW)

U71
SERIAL COMMUNICATIONS CONTROLLER
P29/3590100000 (82530)

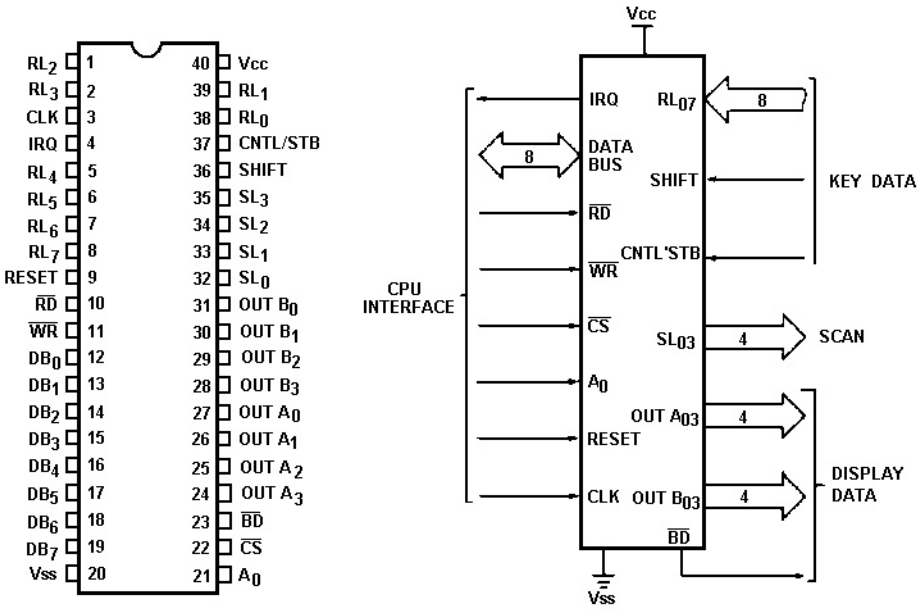
PIN-OUT



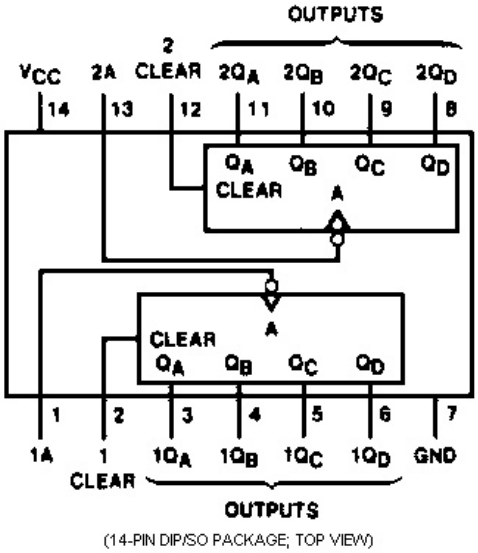
BLOCK DIAGRAM



U72
KEYBOARD/DISPLAY INTERFACE
P29/3590066000 (8279)



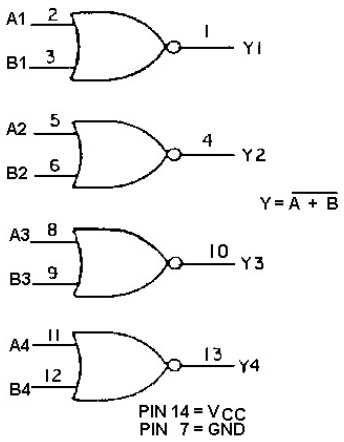
U74
DUAL 4-BIT BINARY COUNTER
P29/3550035600 (74HC393)



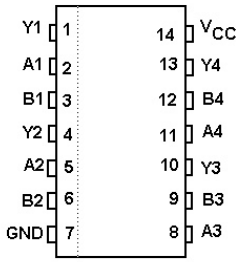
(14-PIN DIP/SO PACKAGE; TOP VIEW)

U75 & U83
QUAD 2-INPUT OR GATE
P29/3550022600 (74HC32)

LOGIC DIAGRAM



$Y = \overline{A + B}$

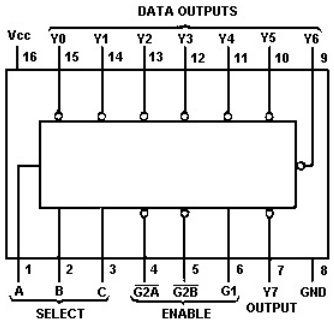


14-PIN SOIC; TOP VIEW

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

U76
3-TO-8 LINE DECODER
P29/3550014600 (74HC138)

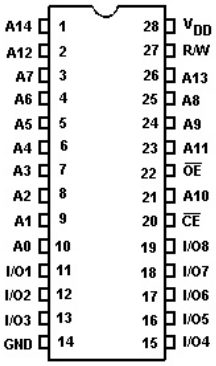


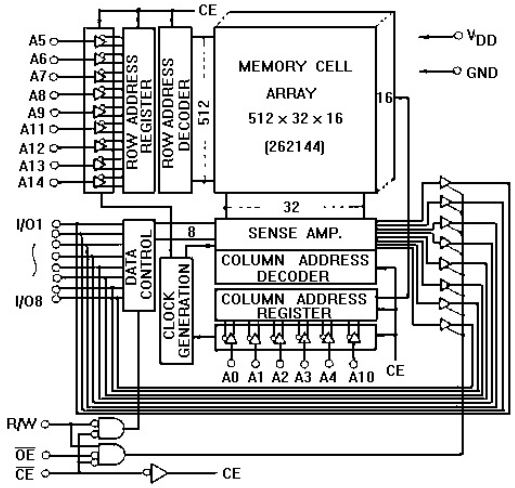
(16-PIN DIP/SO PACKAGE; TOP VIEW)

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

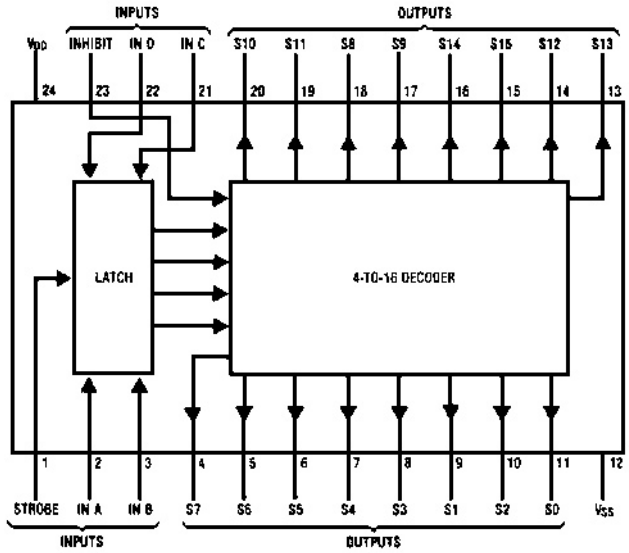
*$\overline{G2} = \overline{G2A} + \overline{G2B}$ H = high level L = low level X = don't care

U77
32K X 8-BIT STATIC RAM
P29/3580119600 (TC55257)



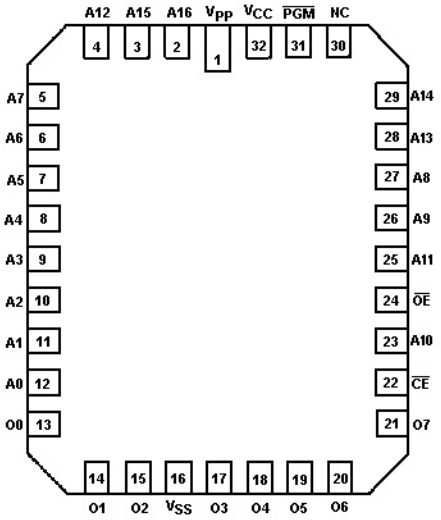


U78
4-TO-8 LINE DECODER
P29/3590096000 (74HC4514)

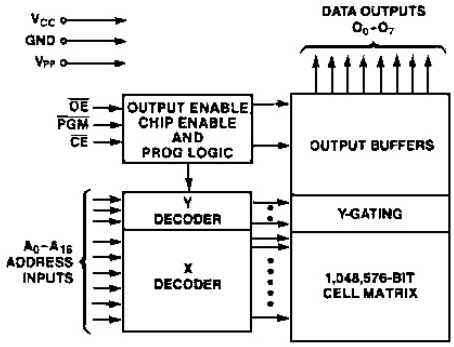


LE	Inhibit	Data Inputs D	C	B	A	Selected Output High
H	L	L	L	L	L	S0
H	L	L	L	L	H	S1
H	L	L	L	H	L	S2
H	L	L	L	H	H	S3
H	L	L	H	L	L	S4
H	L	L	H	L	H	S5
H	L	L	H	H	L	S6
H	L	L	H	H	H	S7
H	L	H	L	L	L	S8
H	L	H	L	L	H	S9
H	L	H	L	H	L	S10
H	L	H	L	H	H	S11
H	L	H	H	L	L	S12
H	L	H	H	L	H	S13
H	L	H	H	H	L	S14
H	L	H	H	H	H	S15
X	H	X	X	X	X	All Outputs = 0
L	L	X	X	X	X	Latched Data

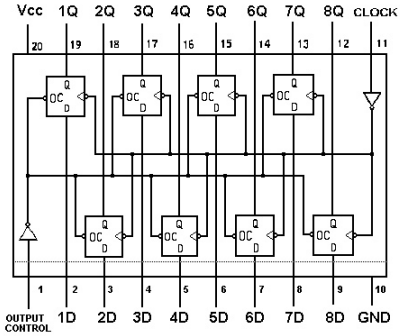
U84
128K X 8-BIT EPROM
P29/3590109001 (27C010/27C1001)



(32-PIN PLCC PACKAGE; TOP VIEW)



U87 & U88
OCTAL DATA FLIP-FLOP
P29/3550015600 (74HC574)



TOP VIEW

TRUTH TABLE

Ouput Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level
Q_0 = level of output before steady-state input conditions were established.
Z = high impedance
X = Don't care
↑ = transition from low-to-high

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