MAINTENANCE MANUAL

CLOCK BOARD
19D903305P1 REV. E

TABLE OF CONTENTS

ERICSSON

SPECIFICATIONS

CLOCK OUTPUTS (A & B)

TDM Bus Network Clocks	
Bit Clock	2.048 MHz (also E1 line-rate clock in E1 mode)
Slot Sync Clock	256 kHz (can be disabled via DIP switch setting)
Frame Sync Clock	8 kHz
Tone Signalling Clock	2174 Hz (can be disabled via DIP switch setting)
T1 Clock	1.544 MHz (not present if slaved synced to an external E1 clocking source via RS-422/RS-232 input)
E1 (CEPT) Clock	2.048 MHz (bit clock)
Stability (All Clock Outputs)	±50 ppm at 25° Celsius (77° Fahrenheit)
Interface Type (All Clock Outputs)	IEEE-896 Futurebus-compatible clocking signals to CEC/IMC Backplane

EXTERNAL CLOCK SYNC INPUTS

Slave Sync Reference Clock Input (Pri. & Sec.)	8 kHz (±2 Hz) IEEE-896 Futurebus-compatible clocking signals from CEC/IMC Backplane supplied by T1/E1 Interface Card(s) installed within CEC/IMC
T1/E1 Line-Rate RS-422/RS-232 Clock Input	
General	1.544 MHz (T1) or 2.048 MHz (E1) RS-422 or RS-232 compatible clocking signals from CEC/IMC Backplane supplied by external equipment
Input Impedance	DIP switch-selectable for low (approximately 100 ohms) or high impedance

SLAVE SYNC ALARM OUTPUT

General	Active-low alarm output generated when either external slave sync reference clock input from CEC/IMC Backplane fails
Interface Type	IEEE-896 Futurebus compatible logic signal to CEC/IMC Backplane

GENERAL

Board Physical Characteristics	Compatible with existing 6-rack unit CEC/IMC boards/cards (VME-like backplane) with two 96-pin DIN connectors
Operating Temperature	0 – 70° Celsius (32° – 158° Fahrenheit)
Power Supply Requirement	5.0 Vdc, 750 mA maximum
Fusing	
Redundancy Protection	Each clock circuit (A and B) independently fused
Fuse Rating & Type (each fuse)	1.0-amp/250-volt fast acting, 2AG cartridge-style
Front Panel Status Indicators (Each Clock Circuit)	Power applied, Futurebus drivers on/off, primary external slave sync present, secondary external slave sync present
Front Panel Toggle Switches (Each Clock Circuit)	Enable/disable Futurebus drivers which drive clock lines on CEC/IMC Backplane

DESCRIPTION

Clock Board 19D903305P1 (revision E) is utilized within the EDACS® CEC/IMC Digital Audio Switch and the EDACS® StarGate Controller Digital Audio Switch. It provides redundant clocking signals for Time Division Multiplexed (TDM) network signal synchronization across the CEC/IMC Backplane. Audio Boards and T1/E1 Interface Cards utilize these clock signals – sometimes referred to as the "system clocks" – for TDM bus synchronization. Specifically, the TDM bus network requires a 2.048 MHz "bit clock", an 8 kHz "frame sync" clock for every 256 bit clock pulses and a 256 kHz "slot sync" clock for every 8 bit clock pulses. In some cases a 256 kHz slot sync clock on the CEC/IMC Backplane is not required; therefore, these Clock Board redundant outputs are sometimes disabled.

When the CEC/IMC operates in an E1 mode, the redundant 2.048 MHz bit clock outputs from the Clock Board are also utilized for E1 line-rate clocking. The Clock Board can also generate redundant 1.544 MHz clock outputs for T1 line-rate clocking. These T1/E1 line-rate clocks are used by T1/E1 Interface Cards installed within the CEC/IMC/StarGate Controller Digital Audio Switch, and in some cases, by other equipment connected to the Digital Audio Switch via T1/E1 links.

NOTE

Unless otherwise noted, from this point forward, the EDACS® CEC/IMC Digital Audio Switch and the EDACS® StarGate Controller Digital Audio Switch products will be commonly referred to as the "CEC/IMC".

Clock outputs from the Clock Board are routed to the Audio Boards and T1/E1 Interface Cards within the CEC/IMC via CEC/IMC Backplane interconnections. These clock pulse signals, listed in Table 1, are applied to the Backplane at Futurebus levels. The Clock Board also applies a 2174 Hz clock to the CEC/IMC Backplane. This 2174 Hz clock, also at Futurebus levels, is utilized by Audio Board-equipped MIMs for EDACS trunked site tone signalling.

Redundancy is provided by the A clock circuit and the B clock circuit. During any given instant, only the outputs from one circuit are utilized by the CEC/IMC and the other circuit's outputs remains for back-up purposes only. For example, if the CEC/IMC is operating from the B clocks, only the B clock circuit's outputs are utilized. Clock A/B selection is dictated by the MOM Controller Board and redundant clock switching is enabled/disabled via the CEC/IMC Manager. See the Circuit Analysis section in this manual for additional details.

Several different system/network-wide clock synchronization options exists for T1/E1 link applications. The exact option used is dependent upon specific CEC/IMC and node T1/E1 requirements. The term "node" here refers to any external equipment interconnected to the CEC/IMC via a T1/E1 link provided by a T1/E1 Interface Card. Examples include EDACS trunked sites equipped with muxes, other CECs/IMCs equipped with T1/E1 Interface Cards, and StarGate Controllers equipped with T1/E1 Interface Cards. The synchronization options are described briefly in the following text:

- **Master** – The *CEC/IMC is the master source* of network clock synchronization and all other nodes are slaved (synchronized) to it. The Clock Board generates master clocking for the CEC/IMC and all nodes connected to it. In essence, all T1/E1 link-connected nodes in the entire CEC/IMC network are synced to the (active) Clock Board.
- **Slaved To T1/E1 Line** – The *CEC/IMC is synchronized to one T1/E1 line* from an external node. Clocks generated on the Clock Board are synchronized to one T1/E1 line from a node. The Clock Board uses an 8 kHz slave sync line on the CEC/IMC Backplane as its reference source for clock synchronization. This 8 kHz slave sync line is driven by a T1/E1 Interface Card – the card which the T1/E1 line is connected to. For redundancy, two (2) 8 kHz slave sync lines exist. These slave sync lines may be driven by a single or two separate T1/E1 Interface Cards per CEC/IMC Manager configuration.
- **Slaved To External 1.544 MHz Clock** – The *CEC/IMC is synchronized to one external 1.544 MHz reference clock source*, typically from co-located equipment. The external reference clock is applied to the Clock Board via RS-422 or RS-232 interconnections.
- **Slaved To External 2.048 MHz Clock** – The *CEC/IMC is synchronized to one external 2.048 MHz reference clock source*, typically from co-located equipment. The external reference clock is applied to the Clock Board via RS-422 or RS-232 interconnections.

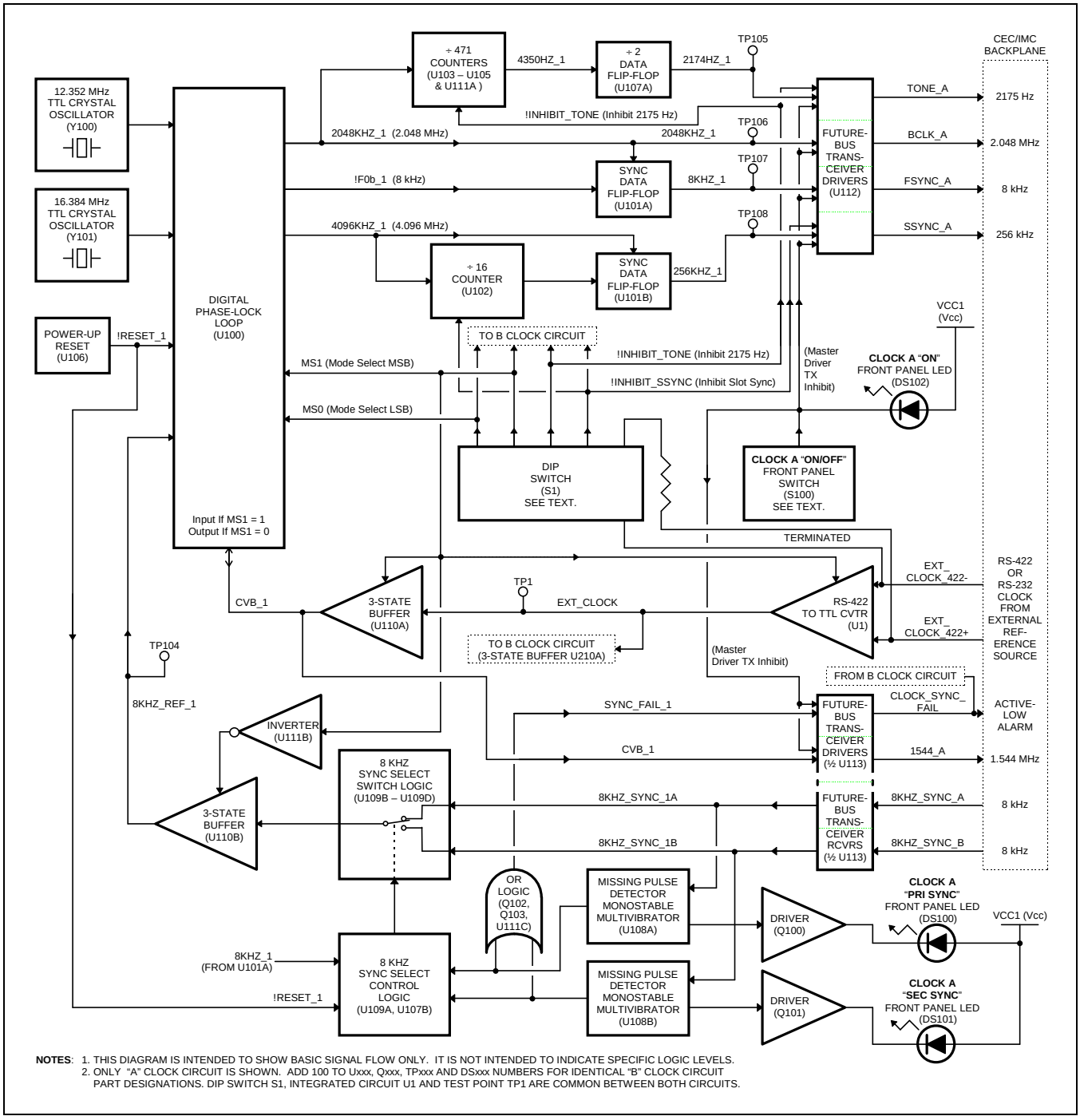
NOTE

Refer to the T1/E1 Interface Card's maintenance manual, LBI-39107 (Network Synchronization Design section), for additional details on the various CEC/IMC-wide and network-wide clock sync configuration options. Also see the "**CONFIGURATION**" section in this manual (begins on page 14).

CIRCUIT ANALYSIS

Figure 1 is a block diagram of the Clock Board. To avoid unnecessary duplication, it only details the A clock circuit. Refer to this figure and the schematic diagram (3 sheets) at the end of this book while reviewing the following circuit analysis.

As indicated in Figure 1, components within the A clock circuit are assigned 100-series designations and components within the B clock circuit are assigned 200-series designations. For example, U105 is located in the A clock circuit [schematic diagram sheet 1] and U205 is located in the B clock circuit [schematic diagram sheet 2]. All paired components with a designation difference of *exactly* one-hundred (100) are identical components which perform identical functions in the redundant A and B clock circuits. For example, U102 in the A clock circuit is a 74HC161 decoder in the A slot sync (256 kHz) counter



NOTES: 1. THIS DIAGRAM IS INTENDED TO SHOW BASIC SIGNAL FLOW ONLY. IT IS NOT INTENDED TO INDICATE SPECIFIC LOGIC LEVELS.
2. ONLY "A" CLOCK CIRCUIT IS SHOWN. ADD 100 TO Uxxx, Qxxx, TPxxx AND DSxxx NUMBERS FOR IDENTICAL "B" CLOCK CIRCUIT PART DESIGNATIONS. DIP SWITCH S1, INTEGRATED CIRCUIT U1 AND TEST POINT TP1 ARE COMMON BETWEEN BOTH CIRCUITS.

Figure 1 – Clock Board Block Diagram

circuit and U202 is a 74HC161 decoder in the B slot sync counter circuit.

Similarly, signal line names in the A clock circuit carry an "_1" (underscore one) suffix and signal line names in the B clock circuit carry an "_2" suffix. For example, 2048KHZ_1 is the bit clock (2.048 MHz) output from U100 in the A clock circuit and 2048KHZ_2 is the bit clock output from U200 in the B clock circuit.

CLOCK OUTPUTS

Basic timing of the Clock Board's clock outputs, respective signal names and test points are shown in Figure 2. This figure indicates waveforms present at the test points, not on the Futurebus lines. Futurebus line waveforms are inverted from the test point waveforms. Futurebus line names are indicated in the figure for reference only. Also, the 2174 Hz tone clock output is not shown since its rise/fall timing is not critical. The clock output signal names are also summarized in Table 1.

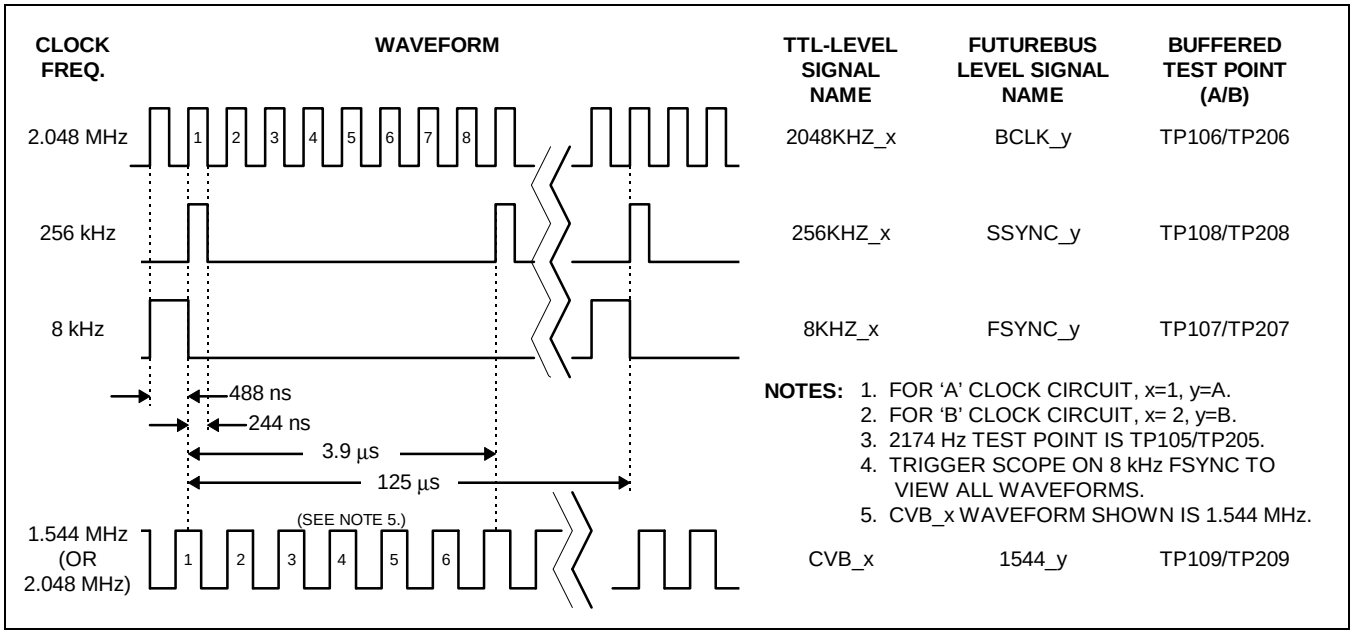


Figure 2 – Clock Output Waveforms At Test Points

Table 1 – Clock Outputs

CLOCK FREQ.	ON-BOARD SIGNAL (TTL Levels)		SIGNAL APPLIED TO BACKPLANE (Futurebus Levels)		COMMENT
	A Clock Circuit	B Clock Circuit	A Clock Circuit	B Clock Circuit	
2.048 MHz	2048KHZ_1	2048KHZ_2	BCLK_A	BCLK_B	"bit clock" for TDM network clocking; also used by T1/E1 Interface Cards operating in E1 mode for E1 line-rate clocking
1.544 MHz *	CVB_1	CVB_2	1544_A	1544_B	1.544 MHz clock for T1 line clocking *
256 kHz **	256KHZ_1	256KHZ_2	SSYNC_A	SSYNC_B	"slot sync" clock for TDM network clocking **
8 kHz	8KHZ_1	8KHZ_2	FSYNC_A	FSYNC_B	"frame sync" clock for TDM network clocking
2174 Hz **	2174HZ_1	2174HZ_2	TONE_A	TONE_B	2174 Hz clock for tone signalling **

* If the Clock Board is externally synced at an E1 line rate (2.048 MHz), the 1544_x clock outputs (2 total) are 2.048 MHz.

** The SSYNC_x and TONE_x clock outputs (4 total) can be disabled via DIP switch settings. SSYNC_x is only used by Audio Board 19D903302P1.

CLOCK GENERATION AND SYNCHRONIZATION

NOTE

A review of the **DESCRIPTION** section within this manual and Network Synchronization Design information in the T1/E1 Interface Card's maintenance manual (LBI-39107) may be beneficial at this time.

Two (2) crystal oscillators and a specialized dual Digital Phase-Locked Loop (DPLL) integrated circuit in each clock circuit are the heart of the circuit's clock generation and synchronization electronics. Refer to Figure 1, Figure 2 and the schematic diagram while reviewing the following circuit analysis.

Crystal Oscillators

Crystal oscillators Y100/Y200 and Y101/Y201 generate 12.352 MHz and 16.384 MHz reference clocks respectively. Y100 and Y101 are located in the A clock circuit and Y200 and Y201 are located in the B clock circuit. To meet T1 and E1 clocking requirement specifications, each oscillator's frequency stability is within ±50 ppm (at 25° Celsius) of its specified operating frequency [schematic diagram sheets 1 and 2].

Pin 8 at each oscillator is a TTL-level compatible clock output with an approximate 50% duty cycle. Each output waveform is applied to a clock reference input pin at the dual DPLL chip. Specifically, the 12.352 MHz clock from Y100/Y200 pin 8 is applied to U100/U200 input pin 3 and the 16.384 MHz clock from Y101/Y201 pin 8 is applied to U100/U200 input pin 10. The DPLL chip uses these reference clocks during all operating modes, with external sync provided in some modes.

Five-volt dc (5 Vdc) operating power is applied to the oscillators at pin 14 of each device. Each oscillator draws approximately 80 milliamps from the 5 Vdc supply. The A circuit's +5 Vdc source line is VCC1 and the B circuit's +5 Vdc source is VCC2. Refer to the section entitled "**POWER SUPPLIES**" (page 12) for additional power supply line details.

Digital Phase-Locked Loop U100/U200

Digital Phase-Locked Loop (DPLL) U100/U200 is the heart of the Clock Board. It is a Mitel MT8941 dual DPLL chip (or equivalent) specifically designed for T1/E1 clocking applications. Operating in one of four (4) DIP switch-configurable modes, it generates phase-locked TTL-level clock pulse signals for the Clock Board [schematic diagram sheets 1 and 2].

Depending upon mode setting, these clocks are locked either to the board's on-board crystal oscillators ("master/free-run" mode), to an 8 kHz slave sync reference clock from a T1/E1 Interface Card installed within the CEC/IMC, or to a 1.544/2.048 MHz line-rate reference clock source external of the CEC/IMC. In the case of the 8 kHz slave sync reference clock from a T1/E1 Interface Card, the T1/E1 Interface Card extracts an 8 kHz reference clock from the connected T1/E1 line and it then routes this clock to the Clock Board via the CEC/IMC Backplane. In the case of the 1.544/2.048 MHz line-rate reference clock from an external source, RS-422/RS-232 line-rate clocking signals are applied to the Clock Board via CEC/IMC Backplane interconnections.

On the Clock Board, the DPLL chip in each clock circuit always provides an 8 kHz clock from its $\overline{\text{F0b}}$ output at U100/U200 pin 8, a 2.048 MHz clock from its C2O output at U100/U200 pin 17, and a 4.096 MHz clock from its C4O output at U100/U200 pin 13. Respectively, these output pins drive the !F0b_x, 2048KHZ_x, and 4096KHZ_x clock lines (where x = 1 in the A clock circuit and x = 2 in the B clock circuit). As described later, the 8 kHz and 2.048 MHz TTL-level outputs indirectly or directly feed the Futurebus transceiver drivers which in-turn drive the CEC/IMC Backplane "bit clock" and "frame sync" clock lines. Also in each clock circuit (A and B), the 4.096 MHz TTL-level clock output is divided-down with a counter circuit to generate the 256 kHz "slot sync" clock. This 256 kHz TTL-level clock then drives its respective Futurebus transceiver driver. In addition, the 2.048 MHz clock output is also divided-down to generate the 2175 Hz tone clock. In each clock circuit, this TTL-level output also drives a Futurebus driver.

Another pin on the DPLL chip, CVb at U100/U200 pin 24, is a bi-directional pin – it is either an input or an output depending upon mode setting. In two (2) modes, it is a 1.544 MHz clock output. In the other two modes it is either a 1.544 or a 2.048 MHz reference clock input. See the following mode-related sections for additional details. This pin connects to the CVB_x clock line.

The DPLL chip generates low-going 8 kHz !F0b clock pulses on the falling-edges of the 4.096 MHz clock. In the A clock circuit this line is labeled !F0b_1 and in the B clock circuit, it is labeled !FOb_2. It is low for only one 4.096 MHz period or 244 nanoseconds. Using the 2.048 MHz clock output from the DPLL chip, data flip-flop U101A/U201A re-clocks, extends and inverts !F0b_x (x = 1 or 2) to produce the 8 kHz frame sync TTL-level 8KHZ_x clock. This 488 nanosecond-wide high-going clock pulse from the flip-flop's $\overline{\text{Q}}$ output at U101A/U201A pin 6, the 8KHZ_x line, feeds the Futurebus transceiver driver which in-turn drives the respective Futurebus-level clock line (frame sync) on the CEC/IMC Backplane. The flip-flop's Q

output (!8KHZ_x at U101A/U201A pin 5) is not utilized on the Clock Board.

Mode Set Logic Inputs

Mode set inputs MS0 through MS3 at U100/U200 pins 2, 6, 9 and 20 respectively set the DPLL chip's operating mode [schematic diagram sheets 1 and 2]. Since the MS2 and MS3 inputs are always pulled high (logic 1) via the respective pull-up resistors, only the state of MS0 and MS1 determine the DPLL chip's operating mode. These two least-significant bit mode set lines are directly controlled by two positions of DIP switch S1 [schematic diagram sheet 3]. One of the four (4) possible operating modes is selected in accordance with the setting of DIP switch positions 1 and 2. See Table 6 for details. Mode changes occur immediately upon a change of a DIP switch position – no reset or power down-up cycle is necessary.

Master/Free Run Mode

The master/free run mode is the most commonly used DPLL operating mode and, in most cases, it is also the factory-set mode per DIP switch configuration. This DPLL mode corresponds to the "**Master**" system synchronization option described in the "**DESCRIPTION**" section of this manual (page 3). It is active when mode set line MS0 is high (logic 1) and mode set line MS1 is low (logic 0).

In this mode the DPLL chip produces clock signals which are *not* synchronized with (*not* phase-locked to) any clocks external of the Clock Board. All clock outputs are simply locked to the on-board crystal oscillators. These outputs include, as previously described, the 2.048 MHz clock, the 8 kHz clock and the 4.096 MHz clock.

Also in this mode, the CVb bi-directional DPLL pin is set for output operation to provide a 1.544 MHz clock for T1 applications; 3-state buffer U110A/U210A is disabled (output pin remains in a high-impedance state) since its control input pin (pin 1) is held low via MS1.

The DPLL chip's TTL-level clock outputs are directly or indirectly applied to the Futurebus transceiver drivers' inputs as previously described in brief and as described in detail later.

Slaved To External 8 kHz Reference Mode

This DPLL chip operating mode is active when both mode set lines – MS0 and MS1 – are low (logic 0) per DIP switch configuration. It corresponds to the "**Slaved To T1/E1 Line**" synchronization option described in the "**DESCRIPTION**" section of this manual (page 3).

In this mode the DPLL chip synchronizes all of its clock outputs to an 8 kHz reference clock applied to the chip's C8Kb input at U100/U200 pin 12. The 8KHZ_REF_x line at pin 12 is driven by the 8 kHz slave sync clock selection circuitry. This circuitry is described in detail in the section entitled "**8 KHZ SLAVE SYNC CLOCK SELECTION**" (page 10). In short, a T1/E1 Interface Card in the CEC/IMC exacts this 8 kHz reference signal from its T1/E1 line and routes it to the Clock Board's 8 kHz slave sync clock selection circuitry via the CEC/IMC Backplane.

As previously described, the DPLL chip's TTL-level clock outputs are directly or indirectly applied to the Futurebus transceiver drivers' inputs.

Inside the DPLL chip, synchronization is performed by generating "speed-up" and "slow-down" logic signals for internal oscillators which are otherwise phase-locked to on-board crystal oscillators (Y100/Y200 and Y101/Y201). The 8KHZ_REF_x clock must be within ±2 Hz of 8 kHz before the DPLL chip will sync to it. To improve jitter performance, the DPLL chip has a no-correction window within which any phase variation of 8KHZ_REF_x will not cause a phase shift of the its clock outputs. As a result, although 8KHZ_REF_x and the system clocks will be frequency-locked, a definite phase relationship between 8KHZ_REF_x and the DPLL chip's clock outputs cannot be guaranteed.

If, when operating in this mode the 8KHZ_REF_x is not present, DPLL chip's outputs remain locked only to the on-board crystal oscillators. Typically, this occurs when the Clock Board has no external 8 kHz slave sync reference; as a result, the Clock Board "free runs" until the slave sync clock reference returns.

Like the previously described mode, the DPLL chip's CVb bi-directional pin is set for output operation to provide the 1.544 MHz clock for T1 applications. Similarly, 3-state buffer U110A/U210A is also disabled.

Slaved To External 1.544 MHz Reference Clock Mode

This mode, normally employed only in T1 applications, is active when mode set line MS0 is low (logic 0) and MS1 is high (logic 1) per DIP switch configuration. It corresponds to the "**Slaved To External 1.544 MHz Clock**" system synchronization option described in the "**DESCRIPTION**" section of this manual (page 3). Essentially, an external RS-422/RS-232-level 1.544 MHz reference clock applied to the Clock Board via the CEC/IMC Backplane is the clock synchronization source.

With MS1 high, the DPLL chip's CVb pin at U100/U200 pin 24 is set as a clock input pin. Also, 3-state buffer U110A/U210A is enabled since its control input pin (pin 1) is high. Since U110A/U210A is enabled, it routes the 1.544 MHz reference clock from RS-422-to-TTL-level converter/receiver chip U1 to pin 24 of the DPLL chip (the CVb bi-directional pin). See the section entitled "**EXTERNAL RS-422/RS-232 LINE-RATE REFERENCE CLOCK INPUT**" (page 12) for a complete description of U1.

In this mode the DPLL chip internally divides the 1.544 MHz clock at pin 24 by 193 to produce an internal 8 kHz sync clock signal. From this point, DPLL chip output clock synchronization, lock range requirements, and what occurs if the sync clock signal is lost is identical to the previously described mode.

Slaved To External 2.048 MHz Reference Clock Mode

This mode, normally employed only in E1 applications, is active when both mode set lines – MS0 and MS1 – are high (logic 1) per DIP switch configuration. It corresponds to the "**Slaved To External 2.048 MHz Clock**" system synchronization option described in the "**DESCRIPTION**" section of this manual (page 3). Essentially, an external RS-422/RS-232-level 2.048 MHz reference clock applied to the Clock Board via the CEC/IMC Backplane is the clock synchronization source.

Like the previously described mode, with MS1 high, the DPLL chip's CVb pin at U100/U200 pin 24 is set as a clock input pin and 3-state buffer U110A/U210A is enabled. Since U110A/U210A is enabled, it routes the 2.048 MHz reference clock from RS-422-to-TTL-level converter/receiver chip U1 to pin 24 of the DPLL chip (the CVb bi-directional pin). See the section entitled "**EXTERNAL RS-422/RS-232 LINE-RATE REFERENCE CLOCK INPUT**" (page 12) for a complete description of U1.

In this mode the DPLL chip internally divides the 2.048 MHz clock at pin 24 by 256 to produce an internal 8 kHz sync clock signal. From this point, DPLL chip output clock synchronization, lock range requirements, and what occurs if the sync clock signal is lost is identical to that as previously described.

As previously described, the DPLL chip's TTL-level clock outputs are directly or indirectly applied to the Futurebus transceiver drivers' inputs.

256 kHz Slot Sync Counter Circuit

The 256 kHz slot sync counter circuit consists of 4-bit binary presettable synchronous counter U102/U202 and data flip-flop U101B/U201B. Basically, this circuit divides the 4.096 MHz clock output from the DPLL chip (4096KHZ_x) by sixteen (16) to produce the 256 kHz slot sync clock signal, 256KHZ_x (where x = 1 in the A clock circuit and x = 2 in the B clock circuit). As a result, one slot sync clock pulse is generated for every eight (8) 2.048 MHz bit clock pulses, a requirement for TDM bus network clocking. As shown in Figure 2, the width of the slot sync clock pulse is 244 nanoseconds – one-half of bit clock's period.

NOTE

The 256 kHz slot sync clock produced by this circuit is only used by Audio Boards 19D903302P1. Therefore, if none of these Audio Boards exist in the CEC/IMC, this Clock Board output may be DIP switch-disabled as described in the configuration section of this manual.

Counter chip U102/U202 performs the actual dividing function and the flip-flop ensures 256KHZ_x clock pulses are rising-edge triggered with 2048KHZ_x (bit clock), also a requirement for TDM bus network clocking. See Figure 2. Actually, the flip-flop is clocked by the 4096KHZ_x clock output from the DPLL chip; inside the DPLL chip the 2.048 MHz clock is itself rising edge-triggered by the 4.096 MHz clock.

The 4.096 MHz clock from DPLL chip U100/U200 pin 13 (C4O) is applied to the counter's clock input at U102/U202 pin 2 and the flip-flop's clock input at U101B/U201B pin 11 via the 4096KHZ_x line. The counter is initially loaded via its preset input pins (3 thru 6) to Eh (hexadecimal). This number is loaded into U102's/U202's internal counters at a rising 4096KHZ_x pulse when !F0b_x (the 8 kHz clock pulse from DPLL chip) is low. The counter then counts from 0Eh back to 0Eh (wraps from Fh to Oh) and it then pulses its ripple-carry output pin 15 upon reaching 0Eh again. This pulse drives the data flip-flop's data input at U101B/U201B pin 11. The 256KHZ_x pulse is then generated at the next rising edge of 4096KHZ_x. 256KHZ_x (TTL-level) is applied to the input of the Futurebus transceiver driver at U112/U212 pin 8 via an RC filter network.

As previously noted, the 256 kHz slot sync clock output may be DIP switch-disabled. The clock is actually disabled/inhibited in two (2) places – at the Futurebus transceiver driver and in the counting circuit. Disabling both circuits insures the greatest possible noise improvement and power consumption efficiency when the slot sync clock is not required. !INHIBIT_SSYNC from DIP switch S1 position 4 is the active-low disable/inhibit line.

In the 256 kHz slot sync counter circuit !INHIBIT_SSYNC is applied to counter U102's/U202's reset pin 1. When low (DIP switch S1 position 4 = "ON" or "CLOSED"), the counter's ripple-carry output at U102/U202 pin 15 remains low. Therefore, 256KHZ_x at the flip-flop's output remains low and the respective Futurebus transceiver driver remains off (SSYNC_x remains high). Simultaneously, the driver is also disabled (output remains high) per the low state on the !INHIBIT_SSYNC line since this line controls the driver's active-high individual enable input pin at U112/U212 pin 12.

2174 Hz Tone Counter Circuit

In each clock circuit, the 2174 Hz tone counter circuit consists of three (3) 4-bit binary presettable synchronous counters U103/U203 thru U105/U205, data flip-flop U107A/U207A, and inverter U111A/U211A. It divides the 2.048 MHz clock output from the DPLL chip (2048KHZ_x) by 942 to produce the 2174 Hz tone clock signal, 2174HZ_x (where x = 1 in the A clock circuit and x = 2 in the B clock circuit). The duty-cycle of 2174HZ_x is 50%.

The three 4-bit counters are preset to 629H (hexidecimal). Each counter is clocked from the 2048KHZ_x clock line at its respective clock input pin (pin 2). U103's/U203's ripple-carry output feeds the count-enable input of U104/U204 and U104's/U204's ripple carry-output feeds the count-enable input of U105/U205. The counter circuit actually counts to 800H from 629H; the result is, as indicated on the schematic diagram, 471 counts at 2048 kHz = 4350 Hz. The counter circuit's output (4350HZ_x) is taken from the Q3 output of U105/U205 at pin 11. This output feeds data flip-flop U107A/U207A which is wired for ÷ 2 toggling to ensure the final output signal, 2174HZ_x, is a 50% duty-cycle signal and at the correct frequency.

Inverter U111A/U211A resets all three counters per their preset inputs upon completion of a 471 count cycle (when Q3 transitions high) so the count cycle can start again. Specifically, the low duty-cycle 4350HZ_x clock output from U105/U205 pin 11 is inverted by U111A/U211A to drive the active-low count load inputs of each counter.

Like the 256 kHz slot sync clock output, the 2174 Hz tone clock output may be DIP switch-disabled. Similarly, it is disabled/inhibited in two (2) places – at the respective Futurebus transceiver driver and in the counting circuit. !INHIBIT_TONE from DIP switch S1 position 3 is the active-low disable/inhibit line.

!INHIBIT_TONE is applied to the reset input pins of all three counters. When low (DIP switch S1 position 4 = "ON" or "CLOSED"), the counters' ripple-carry outputs (pin 15 at each) and Q outputs remain low. Therefore, flip-flop U107A does not toggle so 2174HZ_x remains in a steady state. In addition, since !INHIBIT_TONE is also applied to the respective Futurebus transceiver driver's active-high (individual) enable input at U112/U212 pin 19, the respective Futurebus transceiver driver remains off when DIP switch S1 position 4 is "ON" or "CLOSED".

FUTUREBUS TRANSCEIVERS

All TDM bus and clock lines on the CEC/IMC Backplane utilize IEEE-896 Futurebus-compatible logic lines. This interface defines a logic high state at (or near) +2 volts and a logic low state at (or near) +1 volt. On the Clock Board, two (2) DS-3897 (or equivalent) Futurebus transceiver integrated circuits in each clock circuit are used for Backplane Futurebus line interfacing. These chips are quad devices – each has four (4) driver/receiver pairs.

On the Futurebus (CEC/IMC Backplane) side, drivers within the Futurebus transceiver chips have open-collector outputs. Individual pull-up resistors on the CEC/IMC Terminator Boards pull each respective Futurebus line to an approximate +2-volt level when the line is high (driver off).

The primary purpose of the Futurebus transceivers is to perform TTL-to-Futurebus level conversions between the TTL-level chips on the Clock Board and the Futurebus lines on the CEC/IMC Backplane. Unlike most other non-clock related Futurebus transceivers on other boards/cards within the CEC/IMC, the Futurebus transceivers on the Clock Board *do not* switch between transmit (drive) and receive modes; each individual transceiver in a transceiver chip uses either its driver *or* its receiver, never both. Driver operation is described in the following sub-section entitled "**Clock Outputs To Backplane**" and receiver operation is described in the subsequent sub-section entitled "**Clock Inputs From Backplane**". On the TTL-level side of the Futurebus transceivers, each clock signal is filtered by an RC network.

Clock Outputs To Backplane

All four (4) transceiver drivers within U112/U212 and one (1) driver within U113/U213 drive clock lines on the CEC/IMC Backplane. The five (5) paired receivers are not utilized. See Table 1 for TTL-level and Futurebus-level clock signal names on both sides these drivers. Each driver not only converts from TTL levels to Futurebus levels but it also inverts the voltage-to-logic state relationship. For example, when a driver's input (TTL side) is in the high state – near 5 volts – its output side (Futurebus side) is low – near 1 volt (driver on). This assumes the transceiver is transmit enabled and the driver is not individually inhibited.

Futurebus transceiver drivers must be transmit enabled before each driver can drive (pull low) its respective Futurebus line on the CEC/IMC Backplane. As previously described, two (2) of the five (5) drivers – the 256 kHz and 2174 Hz clock drivers within U112/U212 – also utilize independent inhibit lines for independent driver enable/disable control from the Clock Board's DIP switch.

Transmit driver enabling/disabling is accomplished by toggle switches S100 and S200 mounted on the board's front panel. Each toggle switch is labeled simply "ON" and "OFF". When in the "ON" position, each transceiver's transmit enable input pin is pulled low – the active state – to enable all drivers within it. When enabled, assuming its inhibit line is not low, a driver pulls its respective Futurebus line on the CEC/IMC Backplane low when its TTL input is high. When in the "OFF" position, each transceiver's transmit enable input pin is pulled high – the inactive state.

In this state, a driver's output always remains in a high-impedance condition so it cannot effect signals on the CEC/IMC Backplane.

See the "**CONFIGURATION**" section in this manual, subsection "**TOGGLE SWITCHES S100/S200**" (page 15) for additional details.

8 kHz Slave Sync Clock Alarm Output

One Futurebus transceiver driver in each clock circuit is utilized to output an alarm-type steady-state logic signal onto the CEC/IMC Backplane when either external 8 kHz slave sync clock input from the Backplane is lost. The 8 kHz slave sync clock lines on the Backplane originate from one or more T1/E1 Interface Cards installed in the CEC/IMC. The T1/E1 Interface Card(s) extracts the sync clock signals from its connected T1/E1 line(s). See LBI-39107 for additional details on the T1/E1 Interface Card.

This Futurebus-level output, CLOCK_SYNC_FAIL from pin 20 of U113/U213, is the only non-clocking Futurebus-level signal into or out of the Clock Board. CLOCK_SYNC_FAIL transitions low (the active state) when an 8 kHz slave sync clock input failure occurs. It is routed to the CEC/IMC Backplane via 96-pin DIN connector J2 pin 26A. J2 is the bottom DIN connector. Currently, this line is not utilized by any CEC/IMC board/card.

Both driver's outputs – one in A clock circuit and one in B clock circuit – are tied together to provide a NOR-gate function. This is possible since the drivers have open-collector outputs and each driver inverts the voltage level between its TTL side and its Futurebus side. TTL-level driver inputs include SYNC_FAIL_1 at U113 pin 1 in the A clock circuit and SYNC_FAIL_2 at U213 pin 1 in the B clock circuit. With the NOR-gate function, either the A driver within U113 *or* the B driver within U213 can pull CLOCK_SYNC_FAIL to the low (active) state when its respective SYNC_FAIL_x input transitions to the high (active) state. For details on the 8 kHz slave sync clock line detection circuitry which precedes this Futurebus driver circuitry, see the section entitled "**8 KHZ SLAVE SYNC CLOCK SELECTION**", subsection "**Detection And Status Indicator Circuits**" (page 11).

Like the clock line Futurebus transceiver drivers, the two CLOCK_SYNC_FAIL drivers are master enabled/disabled by the two switches on the Clock Board's front panel. Using the transceivers' active-low transmit enable inputs, S100 enables/disables the driver within U113 and S200 enables/disables the driver within U213.

Clock Inputs From Backplane

As previously described, when configured via the CEC/IMC Manager, the two 8 kHz slave sync clock lines on the CEC/IMC Backplane are driven by one or two T1/E1 Interface Cards in the CEC/IMC. These reference sync clock inputs are only utilized when the board operates in the "**Slaved to T1/E1 Line**" system synchronization mode. See the **DESCRIPTION** (page 3) and **CONFIGURATION** (page 14) sections for additional details.

At the Clock Board's 96-pin DIN connectors these lines are labeled 8KHZ_SYNC_A and 8KHZ_SYNC_B [schematic diagram sheet 3]. Unlike label representation, each line *is not directly related* to a specific clock circuit – either A or B; 8KHZ_SYNC_A is simply a primary sync line for the A clock circuit with 8KHZ_SYNC_B providing backup redundancy. Inversely, in the B clock circuit, 8KHZ_SYNC_B is the primary sync line and 8KHZ_SYNC_A provides backup redundancy.

A total of four (4) Futurebus receivers within U113 and U213 are utilized to convert the Futurebus-level 8 kHz sync clock inputs, 8KHZ_SYNC_A and 8KHZ_SYNC_B, to TTL-level clocks. In the A clock circuit 8KHZ_SYNC_A is applied to a receiver's input at U113 pin 15 and 8KHZ_SYNC_B is applied to a receiver's input at U113 pin 13. Likewise, in the B clock circuit 8KHZ_SYNC_A is applied to a receiver's input at U213 pin 15 and 8KHZ_SYNC_B is applied to a receiver's input at U213 pin 13. All four receivers' paired drivers are disabled per the low states on the driver inhibit inputs at U113/U213 pins 12 and 14. The receivers are always enabled per the low state on U113/U213 pin 11. [schematic diagram sheets 1 and 2].

TTL-level converted clock lines are labeled 8KHZ_SYNC_1A and 8KHZ_SYNC_1B in the A clock circuit and 8KHZ_SYNC_2A and 8KHZ_SYNC_2B in the B clock circuit. An RC network at the output of each receiver low-pass filters each TTL-level clock line before it is routed the respective 8 kHz slave sync clock selection circuitry. Respectively, the filtered clock signals may be monitored at test points TP101, TP102, TP201 and TP202.

8 KHZ SLAVE SYNC CLOCK SELECTION

As previously described, when configured via the CEC/IMC Manager, the two 8 kHz slave sync clock lines on the CEC/IMC Backplane are driven by one or two T1/E1 Interface Cards in the CEC/IMC. These reference sync clock inputs are only utilized when the board operates in the **"Slaved to T1/E1 Line"** system synchronization mode. Two lines – primary and secondary – are provided for redundancy reasons only.

The 8 kHz slave sync clock primary/secondary selection circuitry consists of detection and selection circuits. In each clock circuit, the detection circuit monitors both primary and secondary 8 kHz slave sync reference clocks from the CEC/IMC Backplane. It then controls the selection circuit

accordingly. In addition, it also drives the LED sync status indicators on the front panel; see Table 3 for details.

The selection circuit, per outputs from the detection circuit, always selects the primary 8 kHz slave sync clock if it is present. If neither primary or secondary sync clock is present the selection circuit defaults back to the primary sync clock input. Primary/secondary redundancy mapping for both clock circuits is shown in Table 2. As shown in the table, the primary and secondary sources are inverted between the two clock circuits. This design maximizes clock synchronization fault-tolerance.

Table 2 – 8 kHz Slave Sync Clock Primary/Secondary Redundancy Mapping

8 kHz SLAVE SYNC CLOCK	A CLOCK CIRCUIT INPUT	B CLOCK CIRCUIT INPUT
Primary	8KHZ_SYNC_A (8KHZ_SYNC_1A)	8KHZ_SYNC_B (8KHZ_SYNC_2B)
Secondary	8KHZ_SYNC_B (8KHZ_SYNC_1B)	8KHZ_SYNC_A (8KHZ_SYNC_2A)

* TTL-level clocks shown in parentheses. Other clocks are Futurebus-level clocks.

As indicated in Table 2, 8KHZ_SYNC_1A (primary) and 8KHZ_SYNC_1B (secondary) are the redundant 8 kHz slave sync TTL-level clock lines in the A clock circuit. These two clocks from Futurebus receiver U113 are applied to U108 in the detection circuitry. Similarly, 8KHZ_SYNC_2A (secondary) and 8KHZ_SYNC_2B (primary) are the redundant 8 kHz slave sync TTL-level clock lines in the B clock circuit. These two clocks from Futurebus receiver U213 are applied to U208.

Detection And Status Indicator Circuits

A dual retriggerable monostable multivibrater (one-shot) IC in each clock circuit, U108/U208, is the circuit's main 8 kHz slave sync clocks detection component. Each monostable's on-time is set to approximately 220 µs by its RC network on its timing pin and it is triggered by the 8 kHz slave sync clock from the respective Futurebus transceiver. Therefore, each monostable's Q output remains in a high state as long as the respective 8 kHz slave sync clock (125 µs period) is present.

When high, each monostable's Q output saturates (turns on) the connected drive transistor which in turn, lights the respective LED status indicator on the front panel. U108A/U208A is the primary sync detection monostable and U108B/U208B detects secondary sync.

A 2-input OR gate is formed by transistors Q102/Q202, Q103/Q203, inverter U111C/U211C and associated resistors. In each clock circuit, a monostable's $\overline{Q}$ (active-low) output drives an input of the OR gate circuit. Therefore, if either monostable (primary or secondary sync detect) times-out because of a loss of an 8 kHz slave sync clock, the OR gate circuit's output transitions to the high state. This output is the SYNC_FAIL_x line (TP100/TP200). It is applied to the input of Futurebus transceiver driver which drives the CLOCK_SYNC_FAIL line on the CEC/IMC Backplane. See the previous section entitled "**8 kHz Slave Sync Clock Alarm Output**" (page 10) for additional details on this Futurebus-level output to the CEC/IMC Backplane.

Selection Circuit

NAND gate U109A/U209A is the first component in the selection circuit. It NANDs the $\overline{Q}$ (active-low) output from the primary sync detection monostable with the Q (active-high) output from the secondary detection monostable. As a result, its output pin (pin 3) always remains in a high state if the primary 8 kHz slave sync clock is present (see Table 2) since the $\overline{Q}$ output from U108A/U208A remains low in this condition. U109A/U209A pin 3 will only transition low if the primary sync clock fails *and* secondary sync is present (per a high state on U108B's/U208B's Q output). This NAND gate output feeds the data input of data flip-flop U107B/U207B.

Data flip-flop U107B/U207B syncs any NAND gate output state change with the next rising edge of the 8 kHz clock generated by the DPLL chip. This produces a delay in primary/secondary transitions. The DPLL chip's 8 kHz clock output is applied (via flip-flop U101A/U201A) to the data flip-flop's clock input pin via 8KHZ_x (where x = 1 in the A clock circuit and x = 2 in the B clock circuit).

The Q output of the data flip-flop (U107B/U207B pin 9) remains high as long as the primary 8 kHz slave sync clock is present. This state may be monitored at test point TP103 in the A clock circuit and TP203 in the B clock circuit.

A gating circuit formed by the three (3) subsequent NAND gates switches in (selects) either the primary or the secondary 8 kHz slave sync clock from Futurebus transceiver U113/U213. The switched-in (selected) clock is next applied to the input of 3-state buffer U110B/U210B. This buffer, if enabled, sends the selected 8 kHz slave sync clock to the DPLL chip via the 8KHZ_REF_x line. The buffer is only enabled when mode set line MS1 from the DIP switch is low. This ensures the 8 kHz slave sync reference clock is not applied to the DPLL chip when an external 1.544 or 2.048 MHz line-rate reference clock is utilized.

EXTERNAL RS-422/RS-232 LINE-RATE REFERENCE CLOCK INPUT

In applications where the Clock Board (and thus the entire CEC/IMC) is synchronized or "slaved" to an external 1.544 MHz or 2.048 MHz line-rate reference clock, interconnections from the external reference clocking source to the Clock Board may be either RS-422 or RS-232 interconnections. In these applications, the external RS-422/RS-232-level 1.544/2.048 MHz reference clock is applied to the Clock Board via a 2-wire input connection at one of the board's two respective 24-pin dual-in-line connectors on the CEC/IMC Backplane. As show on the schematic diagram [sheet 3], EXT_CLOCK_422- and EXT_CLOCK_422+ enter the Clock Board via 96-pin DIN connector J2 pins 23C and 24C respectively. J2 is the bottom DIN connector. See Table 7 and Table 8 for specific interconnection details at the 24-pin dual-in-line connector on the CEC/IMC Backplane.

On the Clock Board, integrated circuit U1 is used to convert this RS-422/RS-232-level clock into a TTL-level clock. This receiver IC is common to both the A and B clock circuits. Actually, U1 is a quad line receiver chip but only ¼ of it is utilized. EXT_CLOCK_422- from J2 pin 23C is applied to U1 pin 1 and EXT_CLOCK_422+ from J2 pin 24C is applied to U1 pin 2. Pins 1 and 2 are differential inputs of one receiver within U1. This receiver's output is U1 pin 3.

The TTL-level clock output from U1 pin 3 drives the EXT_CLOCK line. This clock signal is applied to 3-state buffer U110A in the A clock circuit [schematic diagram sheet 1] and 3-state buffer U210A in the B clock circuit [schematic diagram sheet 2]. If necessary, EXT_CLOCK may be monitored at test point TP1 using a high-impedance oscilloscope or frequency counter probe. See the section entitled "**CLOCK GENERATION AND SYNCHRONIZATION**", subsection "**Digital Phase-Locked Loop U100/U200**" (page 6) for details on the clock synchronization circuitry.

DIP switch S1 position 5 provides high/low impedance switching for the external RS-422/RS-232 reference clock input. When S1 position 5 is "ON" or "CLOSED", 100-ohm resistor R1 is placed across the EXT_CLOCK_422- and EXT_CLOCK_422+ inputs from the CEC/IMC Backplane. This is the low-impedance position and it is recommended for most applications since it approximately matches the characteristic impedance of most RS-422 lines. Alternately, if the clocking output from the reference source must drive multiple loads, S1 position 5 can be placed in the "OFF" or "OPEN" position to provide a high-impedance input connection.

FRONT PANEL STATUS INDICATORS

Each clock circuit has four (4) status indicators located on the front panel for a total of eight. All are LED-type (light-emitting diode) indicators. See Table 3.

POWER SUPPLIES

VCC1 And VCC2 Supply Lines

All clock circuits on the Clock Board require 5 Vdc power. For maximum redundancy protection, the A and B clock circuits operate from independently-fused supply lines – VCC1 for the A clock circuit and VCC2 for the B clock circuit. This prevents a severe failure in one supply line such as a shorted decoupling capacitor from affecting the other clock circuit. F100 fuses the A clock circuit supply line and F200 fuses the B clock circuit supply line. Both fuses are socketed [schematic diagram sheets 1 & 2].

Both fuses are fed by the high-current +5 Vdc supply lines on the CEC/IMC Backplane labeled +5EXT on the schematic diagram. As shown on the schematic diagram [sheet 3], +5EXT power enters the Clock Board via many pins on 96-pin DIN connectors J1 and J2.

Many other pins on the two 96-pin DIN connectors provide ground return/reference interconnections between the Clock Board and the CEC/IMC Backplane. These connections are labeled GND on the schematic diagram.

After fusing, each VCC supply passes through a low-pass filter network prior to application to its VCC1/VCC2 line. In the A clock circuit, this network is formed by inductor L100 and capacitors C160 through C162. In the B clock circuit, it is formed by L200 and C260 through C262.

A power indication LED for each clock circuit is powered by its respective VCC1/VCC2 line. Both LEDs, DS103 and DS203, are mounted on the Clock Board's front panel. Each is labeled "PWR". These LEDs should *not* be confused with the other LEDs on the front panel which indicate on/off status of the Futurebus transceiver drivers.

+5V Supply Line

On the Clock Board, one integrated circuit, U1, and DIP switch S1 are common to both the A and B clock circuits. This common circuitry requires 5 Vdc power even if one of the two fuses, an associated dc filter network, or an associated printed circuit board interconnection should fail [schematic diagram sheet 3].

This requirement is fulfilled by a power supply ORing circuit formed by diodes D1 and D2 which deliver dc power to a third supply line labeled +5V. The two diodes also simultaneously isolate the two VCC supplies from each other. D1 feeds the +5V line from the VCC1 supply and D2

Table 3 – Front Panel Status Indicators

LED (A/B Clock Circuits)	FRONT PANEL LABELING	FUNCTION (When On)
DS103/DS203	PWR	Indicates respective clock circuit is powered up (fuse good, VCCx = 5 Vdc, etc.) Does *not* indicate position of the respective front panel toggle switch (S100/S200).
DS102/DS202	ON	Indicates respective clock circuit's Futurebus-level drivers are enabled and driving Futurebus lines* on the CEC/IMC Backplane. Controlled by respective front panel toggle switch (S100/S200).
DS100/DS200	PRI SYNC	Indicates primary 8 kHz slave sync clock input from a T1/E1 Interface Card via the CEC/IMC Backplane is present. Sourcing T1/E1 Interface Card selection is determined via CEC/IMC Manager configuration.
DS101/DS201	SEC SYNC	Indicates secondary 8 kHz slave sync clock input from a T1/E1 Interface Card via the CEC/IMC Backplane is present. Sourcing T1/E1 Interface Card selection is determined via CEC/IMC Manager configuration.

* Futurebus lines on the CEC/IMC Backplane driven by the Clock Board's Futurebus transceiver drivers include the TDM bus clock lines, the 1.544 MHz T1 clock line and the 8 kHz slave sync clock failure alarm line.

feeds the +5V line from the VCC2 supply. Either VCC1 *or* VCC2 alone can power the +5V line. The +5V line feeds U1 at pin 16, several pull-up resistors at U1, and several pull-up resistors at DIP switch S1. Decoupling and filtering are provided by C1 and C3 respectively. R20 provides a minimum load and it ensures these capacitors completely discharge when power is removed. As shown on the schematic diagram, diodes D1 and D2 are actually 3-terminal dual-diodes but only one-half of each device is utilized.

RESET CIRCUIT

The DPLL chip in each clock circuit must be reset just after board power-up in order to guarantee proper operation. U106/U206 is a microprocessor supervisory chip which is used on the Clock Board to perform this function. At power-up, U106/U206 holds the active-low reset line, !RESET_x, low. It continues to hold !RESET_x low for approximately 200 milliseconds *after* the VCCx line rises above the chip's reset threshold voltage of 4.65 Vdc. !RESET_x is applied to the DPLL chip at U100/U200 pin 27. When not active, !RESET_x is pulled high by R132/R232.

!RESET_x is also applied to the active-low preset input of data flip-flop U107B/U207B in the 8 kHz slave sync clock selection circuit. This ensures the flip-flop's Q output is set high at reset, thus avoiding any unnecessary secondary-to-primary 8 kHz slave sync clock toggles soon after power-up.

TEST POINTS

All Clock Board test points are located near the front of board just behind the DIP switch. The A and B clock circuit test points are listed in the following tables.

In addition, two (2) test points on the Clock Board are common to both the A and B clock circuits. TP1 is the EXT_CLOCK signal from RS-422/RS-232 receiver chip U1 and TP2 is the common +5V supply line powered from the VCC1 and VCC2 supplies via D1 and D2 [schematic diagram sheet 3].

As indicated in the following tables, clock output signals are buffered prior to application to test points TP105/TP205 thru TP109/TP209. This prevents any noise picked-up in the long traces necessary to reach the test points or in any connected test leads from degrading clock signals on the CEC/IMC Backplane. However, it should be noted that signals on these test point represent signals on the TTL-level side of the Futurebus transceiver drivers, not on the Futurebus-level (CEC/IMC Backplane) side. Therefore, the presence of a signal on a clock output test point does not necessarily indicate a corresponding inverted signal is present on the CEC/IMC Backplane; a Futurebus transceiver driver could be disabled/inhibited or defective. See Figure 2 for test point waveforms.

Table 4 – "A" Clock Circuit Test Points

TEST POINT		SIGNAL NAME
BUFFERED	UNBUFFERED	
—	TP100	SYNC_FAIL_1
—	TP101	8KHZ_SYNC_1A
—	TP102	8KHZ_SYNC_1B
—	TP103	SELECT_1A
—	TP104	8KHZ_REF_1
TP105	—	2174HZ_1
TP106	—	2048KHZ_1
TP107	—	8KHZ_1
TP108	—	256KHZ_1
TP109	—	CVB_1
—	TP110	GND
—	TP111	VCC1

Table 5 – "B" Clock Circuit Test Points

TEST POINT		SIGNAL NAME
BUFFERED	UNBUFFERED	
—	TP200	SYNC_FAIL_2
—	TP201	8KHZ_SYNC_2A
—	TP202	8KHZ_SYNC_2B
—	TP203	SELECT_2B
—	TP204	8KHZ_REF_2
TP205	—	2174HZ_2
TP206	—	2048KHZ_2
TP207	—	8KHZ_2
TP208	—	256KHZ_2
TP209	—	CVB_2
—	TP210	GND
—	TP211	VCC2

CONFIGURATION

NOTE

A review of the **DESCRIPTION** section within this manual and Network Synchronization Design information in the T1/E1 Interface Card's maintenance manual (LBI-39107) may be beneficial at this time.

DIP SWITCH S1

Two (2) switch positions on DIP switch S1 are utilized to configure the board's basic operating mode per CEC/IMC network system requirements. A third position enables/disables both 2174 Hz tone clock outputs (A and B) and a fourth position enables/disables both 256 kHz slot sync clock outputs. In addition, a fifth position sets the external RS-422/RS-232 clock input termination impedance to either high or low. **Caution should be observed when changing any DIP switch position from the factory setting; a full understanding of the consequences should be known beforehand.**

Normally, the factory-set DIP switch configuration sets the board in a "master" (free run) mode, enables the 2174 Hz tone clock outputs, disables the 256 kHz slot sync clock outputs, and sets the external RS-422/RS-232 clock input termination low (to approximately 100 ohms). See the following text for details.

Basic Operating Mode

The Clock Board has four (4) basic operating modes. This mode selection is accomplished via DIP switch S1 positions 1 and 2. In the "master" mode, the Clock Board's clock outputs are *not* locked to any external reference source. Its outputs are simply locked to the on-board crystal oscillators. The other three (3) modes are used when external 1.544 MHz, 2.048 MHz or 8 kHz synchronization *is* required. See the following table for details. Also refer to LBI-39107 and/or the CEC/IMC Manager's operations guide/on-line help for additional details.

Table 6 – DIP Switch S1 Positions 1 & 2

OPERATING MODE	REQUIRED S1 SETTING*	
	POSITION	
	1 (MS0)	2 (MS1)
all clock outputs slaved to a T1/E1 line (via an 8 kHz slave sync input)	0	0
master (free run)**	1	0
slaved to an external 1.544 MHz source on RS-422/RS-232 input	0	1
slaved to an external 2.048 MHz source on RS-422/RS-232 input	1	1

* 0 = "ON" or "CLOSED"; 1 = "OFF" or "OPEN"
** Factory setting; see text.

2174 Hz Tone And 256 kHz Slot Sync Clocks

Two (2) positions on DIP switch S1 allow enabling/disabling of the Clock Board's 2174 Hz tone clock outputs and 256 kHz slot sync clock outputs to the CEC/IMC Backplane. **Normally, the factory settings should not be changed.** However, the following guidelines may be beneficial for certain CEC/IMC installations:

- The 2174 Hz redundant clock outputs (A and B clock circuits) are used only by CEC/IMC Audio Boards within MIMs to generate 2174 Hz/2175 Hz tone signalling for EDACS trunked site keying. All other Audio Boards within the CEC/IMC also monitor the (selected) 2174 Hz clock (A or B) for clock failure reporting to the MOM Controller Board. Therefore, if no Audio Boards exist in the CEC/IMC (for example – a StarGate Controller which has all T1/E1 Interface Card-equipped NIMs), these Clock Board clock outputs can be disabled to slightly reduce noise emissions from the CEC/IMC Backplane. Disable the outputs by setting DIP switch S1 position 3 "ON" or "CLOSED" (logic 0 state).

- The 256 kHz slot sync clock outputs (A and B clock circuits) are used only by the earlier CEC/IMC Audio Boards, part number 19D903302P1. The later Audio Boards (19D903302P3) have on-board slot sync generation circuitry. Therefore, if no 19D903302P1 Audio Boards exist in the CEC/IMC, the Clock Board's 256 kHz slot sync clock outputs may be disabled to slightly reduce noise emissions from the CEC/IMC Backplane. Disable the outputs by setting DIP switch S1 position 4 "ON" or "CLOSED" (logic 0 state).

TOGGLE SWITCHES S100/S200

As described in this manual's circuit analysis section, the two toggle switches on the Clock Board's front panel provide master enable/disable control of the Futurebus transceiver drivers. These drivers drive the TDM bus clock lines, the 1.544 MHz T1 clock line and the 8 kHz slave sync clock failure alarm line on the CEC/IMC Backplane. S100, the lower toggle switch on the front panel, controls the A clock circuit's drivers and S200, the upper toggle switch, controls the B clock circuit's drivers.

Each toggle switch has an "ON" and an "OFF" position per front panel labeling. Exact on/off switch positioning is dependent upon the number of Clock Boards installed in the CEC/IMC. **At a bare minimum, one toggle switch on one Clock Board must be in the "ON" position.**

One Clock Board Installed In CEC/IMC

If only one Clock Board is installed in the CEC/IMC, in most cases, both S100 and S200 should always remain in their "ON" positions. Redundant clock operation is *not* possible if only one Clock Board is installed and only one of its two toggle switches is on. Redundant clock selection (A or B) is controlled by the MOM Controller Board. This feature must be enabled via the CEC/IMC Manager. Refer to LBI-38938, LBI-39107, and/or the CEC/IMC Manager's operations guide/on-line help for additional details.

Two (Or More) Clock Boards Installed In CEC/IMC

In many cases a CEC/IMC is factory-equipped with two Clock Boards so if a failure occurs in one board the other board can provide full A/B clock redundancy while the failed board is removed for service. **If two or more Clock Boards are installed in the CEC/IMC, equivalent toggle switches on any two Clock Boards (A and A for example) *cannot* be in the "ON" position at the same time.** Severe digital audio distortion, complete inability to route digital audio, and/or no T1/E1 link capability will result.

If two Clock Boards are installed in the CEC/IMC and redundant clock operation is enabled (via CEC/IMC Manager), the toggle switches are normally set in the following manner. Normally, this is the factory setting:

- Clock Board 1 – The A clock toggle switch is turned "OFF" and the B switch is turned "ON".

- Clock Board 2 – The A clock switch is turned "ON" and the B switch is turned "OFF".

It should be noted at this point that, per the Clock Boards' DIP switch configuration (see previous section – page 14) and CEC/IMC Manager configuration, these

clocking sources may or may not be slaved/synchronized to an external reference clock.

With the toggle switches set in this manner, the B clock circuit on Clock Board 1 will be the active/utilized clocking source when the CEC/IMC is initially powered-up. (B is the default clock at initial power-up per MOM Controller Board firmware.) Upon any subsequent B clock failure, the MOM Controller Board will then switch CEC/IMC clock operation to the A clocks; thus, Clock Board 2 clock circuit A will become the active/utilized CEC/IMC clocking source.

At this point, to return to full redundant clock operation, Clock Board 1's B toggle switch must be turned OFF and Clock Board 2's B toggle switch must be turned ON. Now, Clock Board 1 can be removed for service. In the above sequence, the only interruption in CEC/IMC digital audio service occurs at the initial failure of the B clock circuit. Typically, this interruption lasts less than 1 second if the CEC/IMC has no T1/E1 Interface Cards and less than 3 seconds if it does. Refer to LBI-38938, LBI-39107, and/or the CEC/IMC Manager's operations guide/on-line help for additional details.

RS-422/RS-232 WIRING FOR EXTERNAL LINE-RATE SYNCHRONIZATION

If the Clock Board is synced to an external 1.544 MHz or 2.048 MHz reference clock from external equipment, refer to Table 7 and Table 8 for RS-422/RS-232 wiring information. The required 2-wire cable must be field-fabricated. Also see the previous DIP switch configuration information (Table 6).

Table 7 – RS-422/RS-232 External Clock Line-Rate Connections At CEC/IMC Backplane (Connector #s)

CLOCK BOARD INSTALLED IN CEC/IMC CARD CAGE SLOT	INTERCONNECT EXTERNAL RS-422/RS-232 CLOCK TO CEC/IMC BACKPLANE CONNECTOR *
1	PA1-2E1
2	PA101
3	PA102
4	PA103
.	.
.	.
18	PA117
19	PA118
20	PA119
21	PA1-2E2

* Required connector type is a 24-pin dual-row header similiar to AMP 104810-1 with AMP 102920-2 contacts. See Table 8 for pin numbers.

Table 8 – RS-422/RS-232 External Clock Line-Rate Connections At CEC/IMC Backplane (Pin #s)

FOR RS-422 INTERFACING INTERCONNECT		FOR RS-232 INTERFACING INTERCONNECT	
TX+ from clock source to Backplane connector * **pin 1**	**TX–** from clock source to Backplane connector * **pin 3**	**TX** from clock source to Backplane connector * **pin 3**	**Gnd** from clock source to Backplane connector * **pin 1**

* See Table 7 for connector number.

CLOCK BOARD
19D903305P1, Rev. E
ISSUE 1

SYMBOL	PART NUMBER	DESCRIPTION
		---------- CAPACITORS ----------
C1	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C3	19A705205P12	Tantalum: .33 µF, 16 VDCW; sim to Sprague 293D.
C100 thru C114	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C120 and C121	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C150 and C151	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C152 thru C155	19A702061P45	Ceramic: 47 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C157 thru C159	19A702061P45	Ceramic: 47 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C160	19A703314P1	Electrolytic: 100 µF -10+50%, 10 VDCW; sim to Panosonic LS Series.
C161 and C162	344A4010P1	Polyester: 0.33 µF ±10%, 200 VDCW.
C200 thru C214	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C220 and C221	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C250 and C251	19A702052P14	Ceramic: 0.01 µF ±10%, 50 VDCW.
C252 thru C255	19A702061P45	Ceramic: 47 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C257 thru C259	19A702061P45	Ceramic: 47 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C260	19A703314P1	Electrolytic: 100 µF -10+50%, 10 VDCW; sim to Panosonic LS Series.
C261 and C262	344A4010P1	Polyester: 0.33 µF ±10%, 200 VDCW.
		---------- DIODES ----------
D1 and D2	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99.
		---------- INDICATING DEVICES ----------
DS100 thru DS103	19A703595P9	Optoelectric: Green LED; sim to HLMP-1540-010.
DS200 thru DS203	19A703595P9	Optoelectric: Green LED; sim to HLMP-1540-010.
		---------- FUSES ----------
F100 and F200	344A3139P5	Cartridge: 1.0-amp/250-volt, 2AG-style, fast acting; sim to Littelfuse 225001.
		---------- JACKS ----------
J1 and J2	RPV403804/01	Connector, DIN: 96 male contacts w/ 5 extended pins, right-angle mounting.
		---------- INDUCTORS ----------
L100 and L200	19A149806P2	High-current: 100 µH; sim to Dale IHA-102.
		---------- TRANSISTORS ----------
Q100 thru Q103	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q200 thru Q203	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
		---------- RESISTORS ----------
R1	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R2	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R4	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R5 and R6	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R7	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R10 thru R13	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R15 thru R17	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R20	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R100 thru R106	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R107 and R108	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R109 and R110	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R111 and R112	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R113	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R114 thru R120	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R121	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R122	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R123	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R124	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R125 thru R128	19A702931P145	Metal film: 287 ohms ±1%, 1/8 w.
R129	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R130	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R131 and R132	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R133 thru R135	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R150 thru R152	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R159	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R161	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.

SYMBOL	PART NUMBER	DESCRIPTION
R200 thru R206	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R207 and R208	19B800607P223	Metal film: 22K ohms ±5%, 1/8 w.
R209 and R210	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R211 and R212	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R213	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R214 thru R220	19B800607P101	Metal film: 100 ohms ±5%, 1/8 w.
R221	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R222	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R223	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R224	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
R225 thru R228	19A702931P145	Metal film: 287 ohms ±1%, 1/8 w.
R229	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R230	19B800607P104	Metal film: 100K ohms ±5%, 1/8 w.
R231 and R232	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R233 thru R235	19B800607P471	Metal film: 470 ohms ±5%, 1/8 w.
R250 thru R252	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R259	19B800607P103	Metal film: 10K ohms ±5%, 1/8 w.
R261	19B800607P102	Metal film: 1K ohms ±5%, 1/8 w.
		---------- SWITCHES ----------
S1	19A149955P1	DIP, rocker: 8-position; sim to Grayhill 76PSB08S.
S100 and S200	19A705959P3	Toggle, SPDT: right-angle mount; sim to C&K T101-M-H9-A-B-E.
		---------- TEST POINTS ----------
TP1 and TP2	344A3367P1	Metal loop w/orange insulator.
TP100 thru TP111	344A3367P1	Metal loop w/orange insulator.
TP200 thru TP211	344A3367P1	Metal loop w/orange insulator.
		---------- INTEGRATED CIRCUITS ----------
U1	19A149929P201	Digital: Quad RS-422/423 Line Receiver; sim to DS3486.
U100	344A3379P101	Digital: T1/CEPT Dual Digital PLL; sim to MT8941A.
U101	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U102 thru U105	19A703987P306	Digital: Presettable Counter; sim to 74HC161.
U106	RYTUA113001/C	Digital: Micro Supervisor; sim to MAX690A.
U107	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U108	19A704380P321	Digital: Monostable Multivibrator; sim to 74HC123.
U109	19A703483P302	Digital: Quad 2-Input NAND Gate; sim to 74HC00.
U110	19A703471P305	Digital: Quad 3-State Buffer; sim to 74HC126.
U111	19A703483P104	Digital: CMOS Hex Inverter; sim to 74HC04.
U112 and U113	19A149953P202	Digital: 4-Channel Futurebus Transceiver; sim to DS3897.
U114	19A703471P305	Digital: Quad 3-State Buffer; sim to 74HC126.
U200	344A3379P101	Digital: T1/CEPT Dual Digital PLL; sim to MT8941A.
U201	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U202 thru U205	19A703987P306	Digital: Presettable Counter; sim to 74HC161.
U206	RYTUA113001/C	Digital: Micro Supervisor; sim to MAX690A.
U207	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U208	19A704380P321	Digital: Monostable Multivibrator; sim to 74HC123.
U209	19A703483P302	Digital: Quad 2-Input NAND Gate; sim to 74HC00.
U210	19A703471P305	Digital: Quad 3-State Buffer; sim to 74HC126.
U211	19A703483P104	Digital: CMOS Hex Inverter; sim to 74HC04.
U212 and U213	19A149953P202	Digital: 4-Channel Futurebus Transceiver; sim to DS3897.
U214	19A703471P305	Digital: Quad 3-State Buffer; sim to 74HC126.
		----------FUSE SOCKETS----------
XF100 and XF101	19A116688P2	Clip, Fuse: sim to Littelfuse 111501.
XF200 and XF201	19A116688P2	Clip, Fuse: sim to Littelfuse 111501.
		---------- CRYSTALS ----------
Y100 and Y101	RTL201614/1	Oscillator, TTL: 12.352 MHz.
Y200 and Y201	RTL201614/1	Oscillator, TTL: 16.384 MHz.
		---------- MISCELLANEOUS----------
	19C852656P1	Panel, front: aluminum, lettered.
		Handles, extranction, w/brackets: sim to Scanbe 60760-01 or Scanbe 216-611.

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter" which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

Rev. A thru D **CLOCK BOARD 19D903305P1**
(See publication LBI-38668.)

Rev. E **CLOCK BOARD 19D903305P1**
Initial production release.

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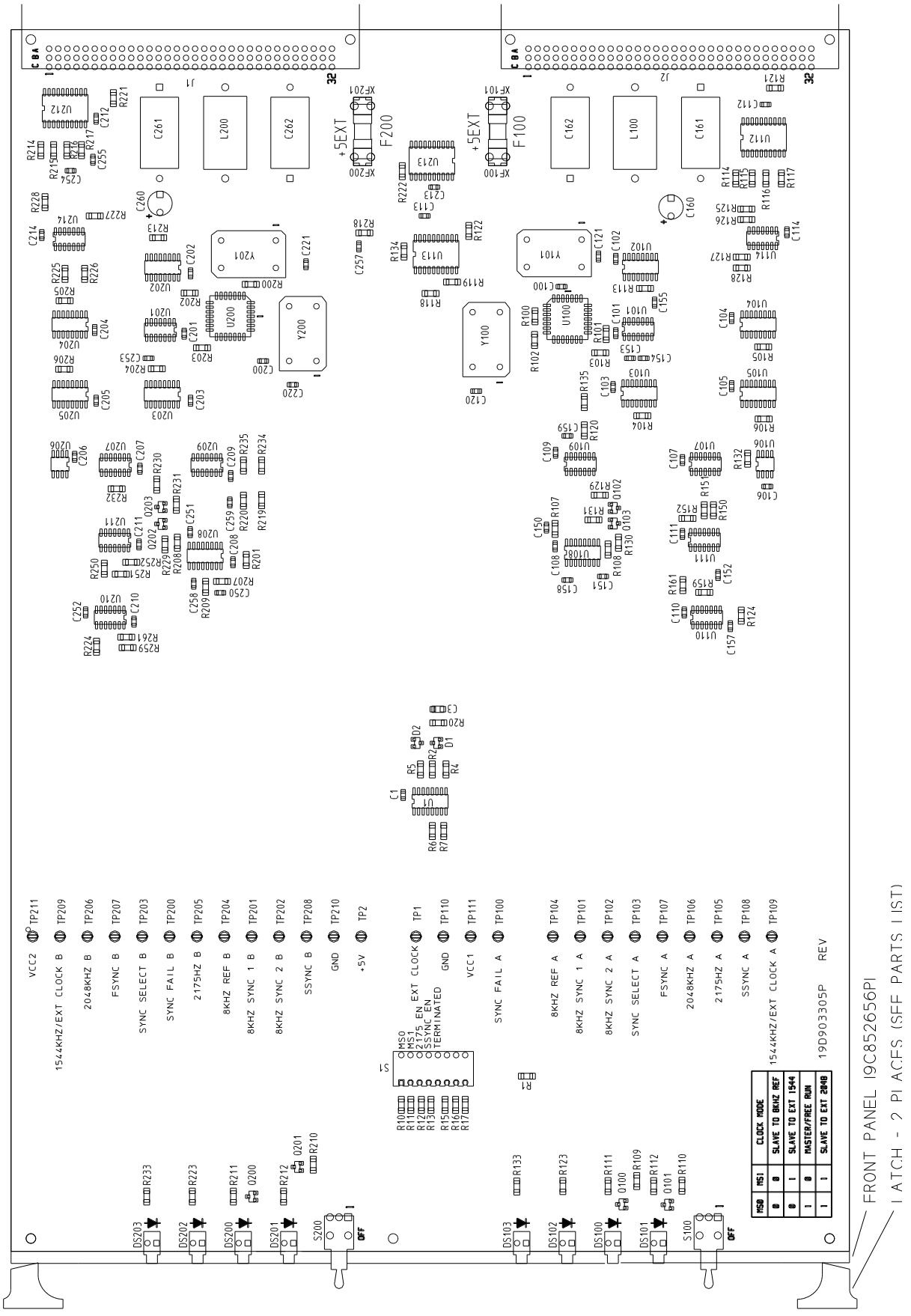
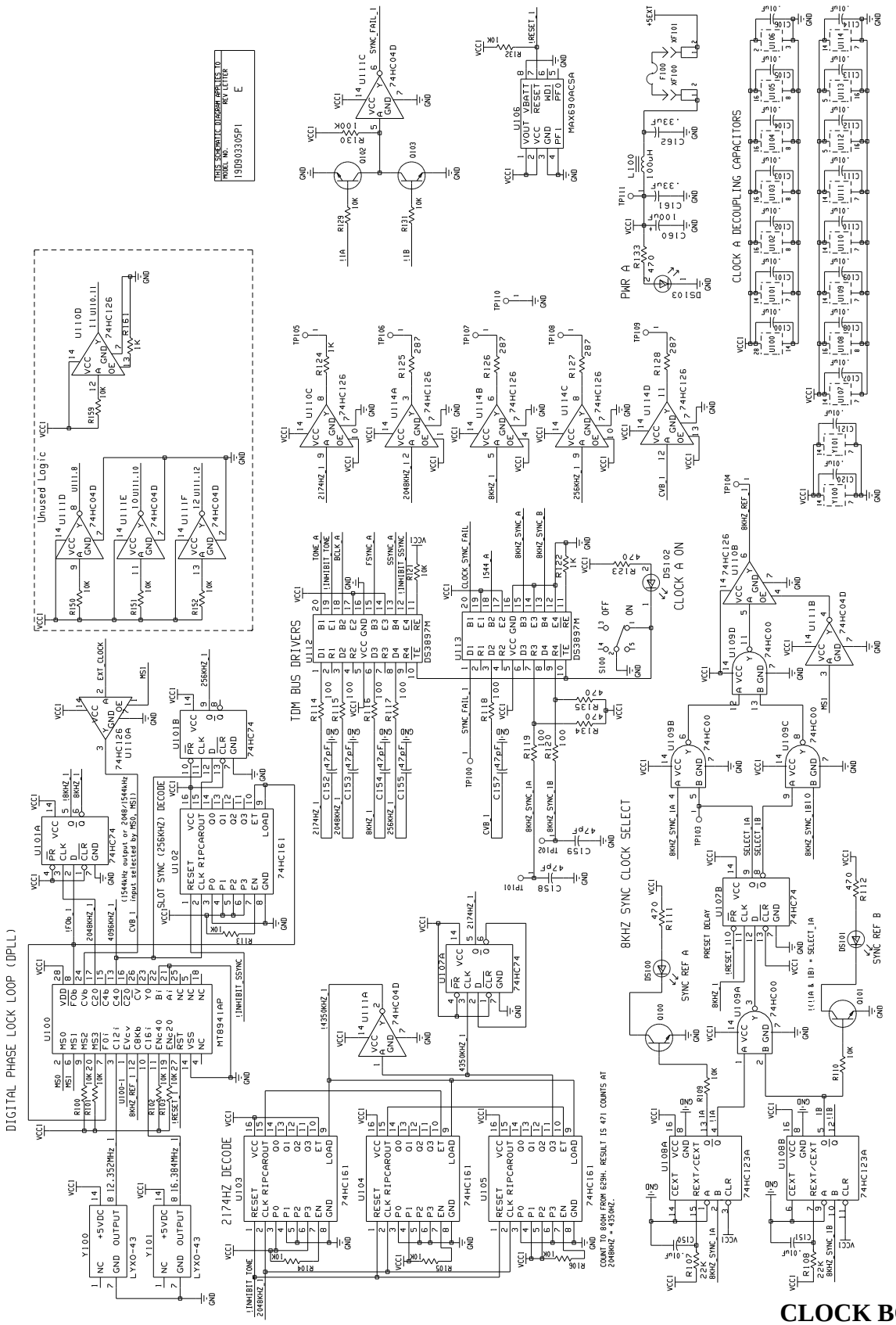


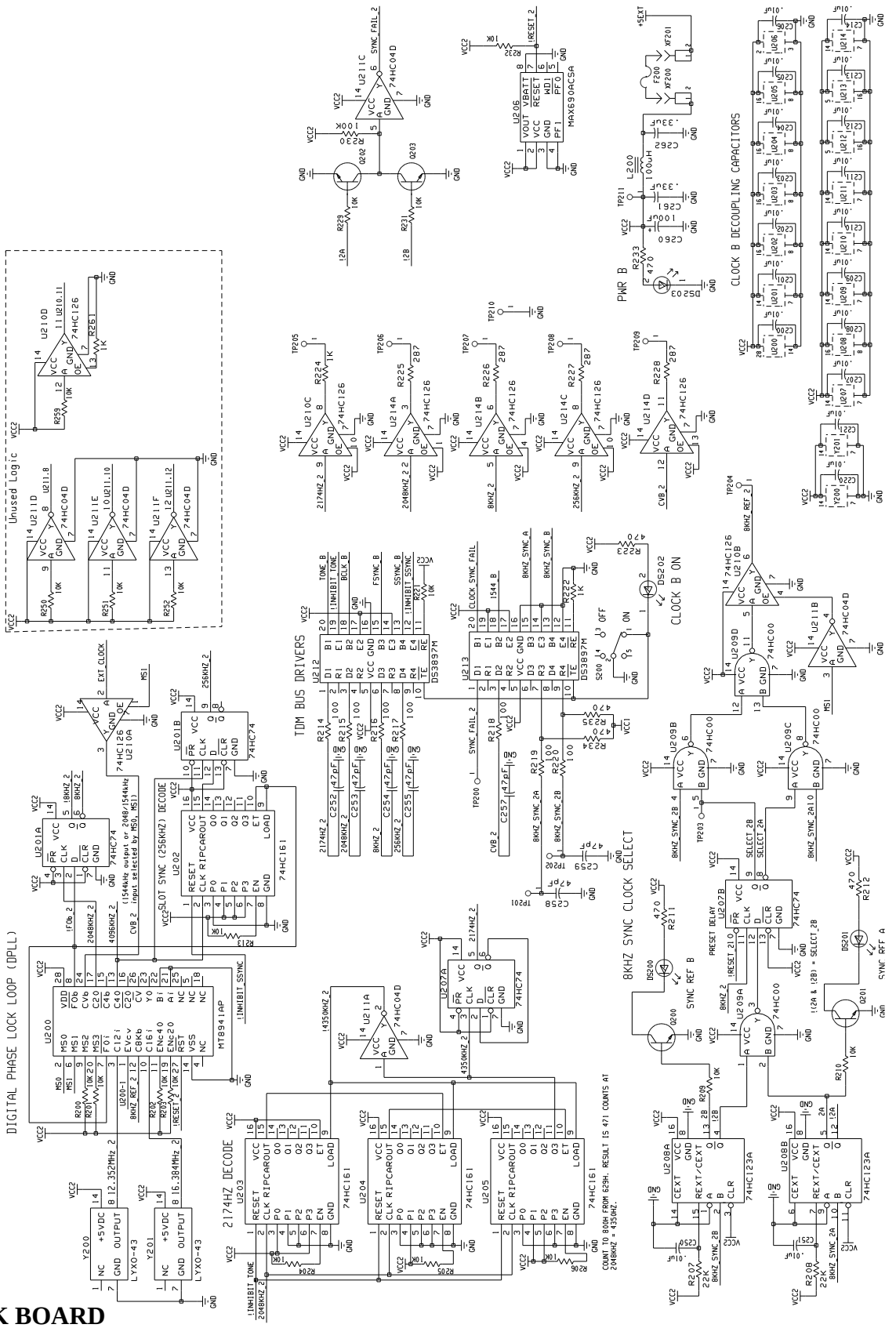
CLOCK BOARD 19D903305P1 REV. E

(19D903305, Rev. 4)



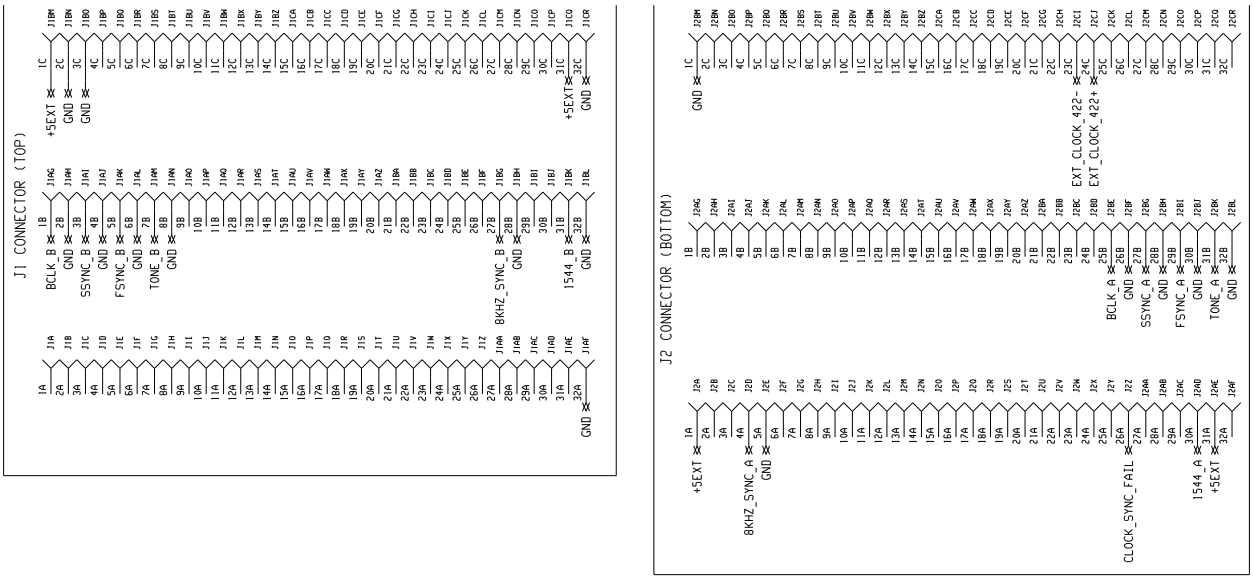
CLOCK BOARD
19D903305P1 REV. E
Sheet 1 of 3 – "A" Clock Circuit

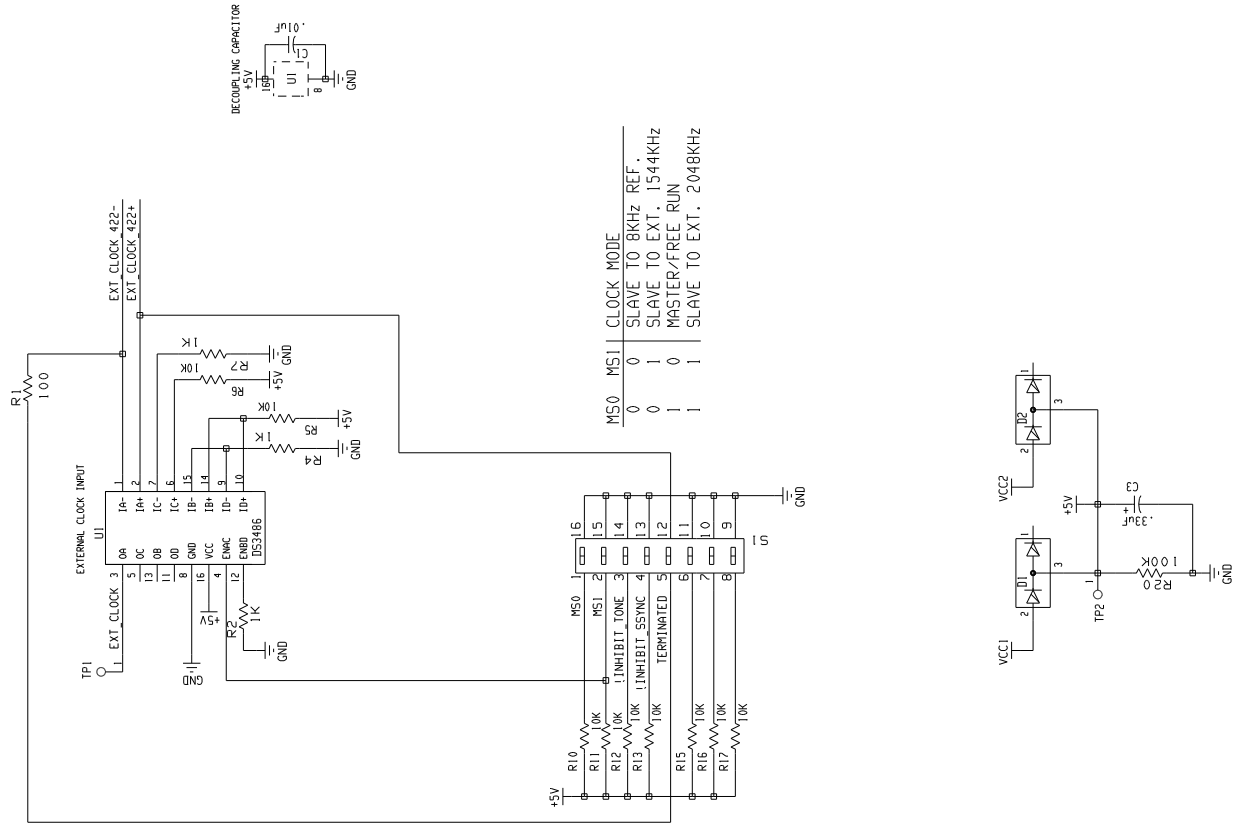
19D903307, Sh. 1, Rev. 5)



CLOCK BOARD
19D903305P1 REV. E
Sheet 2 of 3 – "B" Clock Circuit

(19D903307, Sh. 2, Rev. 5)





CLOCK BOARD
19D903305P1 REV. E
Sheet 3 of 3 – Common Circuits

19D903307, Sh. 3, Rev. 5)

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