

**MAINTENANCE MANUAL
FOR
21.4 MHz RECEIVER IF MODULE
12.5/25 kHz CHANNEL SPACING
19D902783G7**

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DESCRIPTION

The MASTR III Receiver IF Module provides amplification and demodulation of the 21.4 MHz Intermediate Frequency signal. The IF Module also includes the receiver squelch circuitry. However, it does not include de-emphasis or squelch audio gating circuits. Figure 1 is a block diagram showing the functional operation of the IF Module.

The IF Module circuitry contains the following:

- A 50 ohm input impedance IF Amplifier
- A chain of two crystal filters and an integrated circuit IF amplifier
- An integrated circuit containing a crystal oscillator, mixer, limiter, and quadrature detector
- A variable gain AF amplifier
- A squelch circuit
- A fault detector circuit
- An integrated circuit voltage regulator
- An address decoder

TABLE 1 - GENERAL SPECIFICATIONS

ITEM	SPECIFICATION
I.F. frequency	21.4 MHz
Input Impedance	50 ohm
12 dB SINAD	-120 dBm (25 kHz); -119 dBm (12.5 kHz)
Adj. CH SEL	-90 dB (25 kHz); -80 dB (12.5 kHz)
Image	-100 dB
3rd order Intercept Pt	23 dBm (25 kHz); 11 dBm *(12.5 kHz) *@ 50 kHz offset
Variation of Sensitivity with Signal Frequency	2 kHz (25 kHz); 1 kHz (12.5 kHz)
2nd I.F. frequency	455 kHz
2nd L.O. frequency	20.945 MHz
AF output (J2 pin 31C)	1 Vrms adjustable (with standard input signal)
AF output impedance	1k ohm
AF distortion	5% (25 kHz); 5% (12.5 kHz)
<u>AF response</u>	
10 Hz	-3 dB
300 Hz	±1 dB
1000 Hz	0 dB reference
3 kHz	±1 dB
Hum & Noise	-55 dB (25 kHz); -50 dB (12.5 kHz)
RSSI output (J2 pin 20C)	0.7 to 2.7 Vdc prop to log (sig level)
RSSI time constant	5 ms
SQ Threshold Sensitivity	-123 dBm (25 kHz); -122 dBm (12.5 kHz)
SQ Maximum Sensitivity	-110 dBm (25 kHz); -109 dBm (12.5 kHz)
SQ Clipping	3 kHz
SQ Attack	150 ms
SQ Close	250 ms
SQ output (J2 pin 26C)	5V logic (low = squelched)
Fault output (J2 pin IIC)	5V logic (low = fault)
DC Supply	13.8V, 150 mA max.; 12.0V, 18 mA max.

CIRCUIT ANALYSIS

INPUT AMPLIFIER NETWORK

The input amplifier, consisting of Q2 and T1, provides a 50 ohm load for the receiver RF module.

Capacitor C1 provides AC coupling and a DC block on the input line (J1). This DC block protects the module in the event of a failure in a preceding module.

C1 and L9 are series-resonant at 21.4 MHz and provide a low-impedance path from J1 to amplifier Q2. C89 and L8 are parallel-resonant at 21.4 MHz and provide a path to the 50-ohm lead, R105, for mixer products other than 21.4 MHz.

CRYSTAL FILTERS, IF AMPLIFIERS

Y1, Y2, U1, and associated circuitry provide IF filtering and amplification at 21.4 MHz. Filters Y1 and Y2 are both 4-pole bandpass filters with a center frequency of 21.4 MHz and a bandwidth of ±6.5 kHz. Amplifier U1 is an integrated-circuit amplifier. U1 provides 30 dB of gain. The amplifier and filters have terminal impedances of 50 ohms. In-circuit gain measurements can be made using a high impedance probe.

Inductors L3, L5 and associated resistors and capacitors provide power supply decoupling. R3 provides a path to the input of the Fault Detector circuit. This input enables the Fault Detector circuit to monitor the DC voltage of U1.

The RF level detector consists of transistor Q1 along with associated resistors and capacitors. This detector plays no role in the normal operation of the IF Module, but aids in unit testing and module troubleshooting.

OSCILLATOR/MIXER/DETECTOR

Integrated circuit U3 provides several functions including 2nd mixer, if amplifier and limiter, and quadrature detector.

The 20.945 MHz crystal oscillator provides local oscillator injection to the mixer in U3. This mixer converts the 21.4 MHz IF signal to 455 kHz. C20 and C21 are oscillator feedback capacitors and have been chosen to provide the proper capacitance for crystal Y3. The proper oscillator output level is difficult to measure directly without affecting the oscillation.

A preferable measurement is at TP3 which should read about 10 mV pk. (Measured using a 10 megohm 11 pF oscilloscope probe.)

The mixer is internally connected to the crystal oscillator. Pins 1 and 20 of U3 are the mixer input and output respectively. Typical mixer conversion loss is about 2 dB.

In the 12.5 kHz mode, the output of the mixer drives the IF amplifier via analog switch U11-2, filter FL1 and analog switch U11-3. In the 25 kHz mode, the mixer output is routed through analog switch U11-1 and C85 to the IF amplifier. The analog switches are controlled by the signal at point 'A'; high for 25 kHz, low for 12.5 kHz.

The IF amplifier output drives the limiter via the 6-pole ceramic filter FL2.

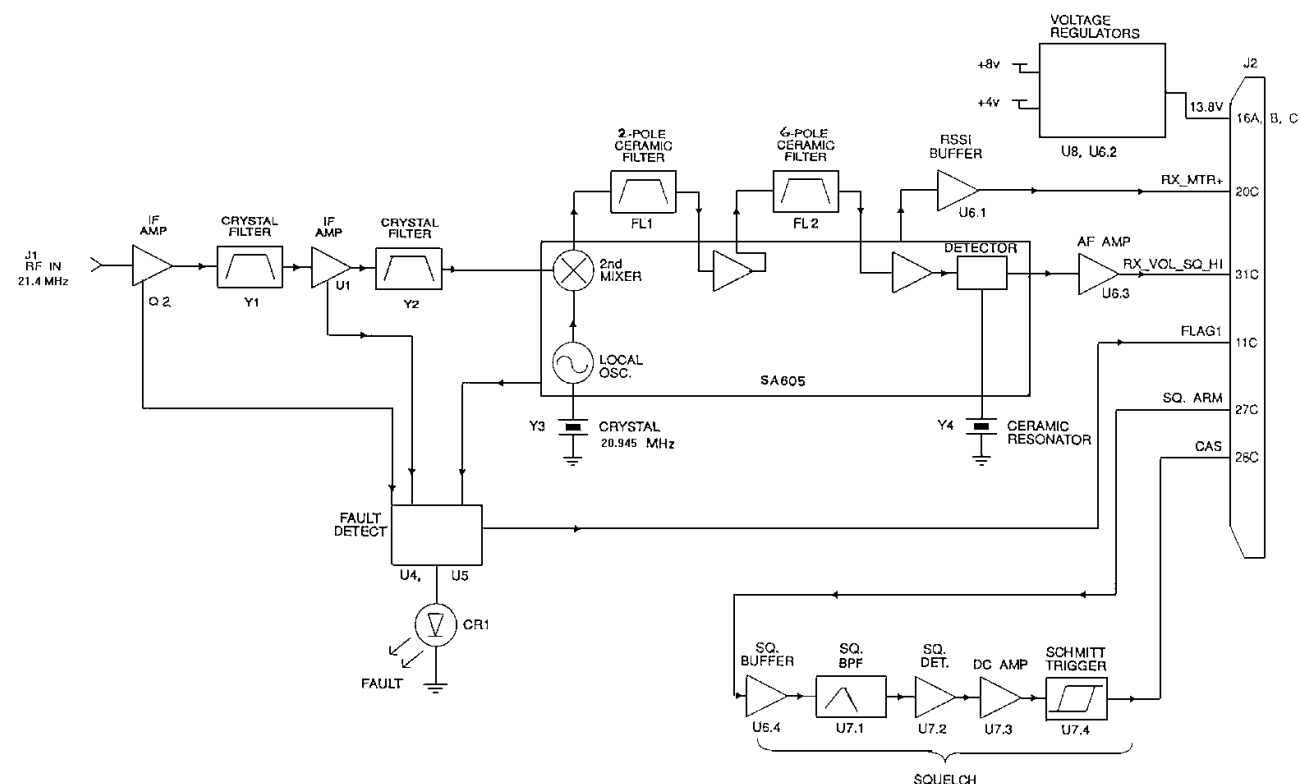
A received-signal-strength indicator (RSSI) is provided at U3 Pin 7. This indicator signal is generated within the limiter circuitry and provides an output current proportional to the logarithm of the input signal strength. This current develops a voltage across R18. The voltage varies from about 1 Vdc for noise input, to about 1.4 Vdc for a 12 dB SINAD signal, to a maximum of about 4.8 Vdc for a high signal level (70 dB stronger than that required for 12 dB SINAD).

The quadrature detector provides a demodulated audio frequency output. The input to the detector is internally connected to the limiter and is not externally available. The output of the detector is U3 pin 9. C28 provides low-pass filtering to remove 455 kHz feedthrough. Ceramic resonator Y4 provides the frequency selective component needed for FM demodulation. Y4 replaces the typical LC resonant circuit found in most quadrature detectors. In contrast to the typical LC network, Y4 requires no adjustment.

The DC supply to U3 is provided through voltage dropping resistor R11 to U3 pin 6. R12 provides a path to the input of the Fault Detection circuit. This enables the Fault Detector to monitor the DC voltage on U3.

AUDIO AMPLIFIER

Operational amplifier U6.3 provides audio frequency amplification. Its gain is set by its associated resistors, including variable resistor VR1. VR1 allows for adjusting the AF output level to 1 Vrms with a standard input signal to the module (1 kHz AF, 3 kHz peak deviation). In the 12.5 kHz mode, the demodulated audio is at a lower level than in the 25 kHz mode. The gain of amplifier U6.3 is, therefore, increased to give the same 1V rms output with a standard input signal to the module of 1.5 kHz deviation. This is done by transistor switch Q6 connecting R1 across R40. U6.2 is used as a voltage regulator to provide 4 Vdc for biasing the operational amplifier.



21.4 MHz IF MODULE - BLOCK DIAGRAM

SQUELCH

Buffer Amplifier

Integrated circuit U6.4 is configured as a unity gain buffer amplifier. It provides a high input impedance to minimize loading of the previous circuits.

Bandpass Filter

The audio frequency bandpass filter consists of U7.1 and its associated circuitry. The purpose of this filter is to reject all voice frequencies and allow only demodulated noise to pass. The functioning of the squelch circuit depends upon the presence or absence of this noise. (When a signal is being received, i.e. the receiver is quiet, the squelch circuit senses the absence of noise and unsquels the radio.)

Noise Detector

U7.2 along with associated components act as a noise detector. The rectified output of U7.2 charges C11/C44 to a nearly constant DC voltage.

DC Amplifier

U7.3 is configured as a basic amplifier with a gain of 3.

Schmitt Trigger

U7.4 is configured as an amplifier with positive feedback. This arrangement provides hysteresis in the output versus input characteristic. This eliminates the possibility of the squelch circuit repeatedly cutting in and out when the input signal is near a threshold. R56 and R57 act as a voltage divider to provide a 5 volt logic level output. (Logic High = unsquels)

FAULT DETECTOR

U4 and U5 are voltage comparators. These are configured into four "window detectors" which sense the presence of voltages within specified ranges (windows).

The four window detector circuits are U4.1 & U4.2, U4.4 & U4.3, U5.1 & U5.2, and U5.4 & U5.3. These monitor DC operating voltages on U6.2, U1, Q2, and U3 respectively. R29 and R30 comprise a voltage divider to provide a 5 volt logic level output. A fault is indicated when the output drops to zero.

Diode D1 and transistor Q3 monitor the output of the 8V regulator. DI is a 8.2 volt breakdown diode. If the regulator output voltage should rise above 8.9 V (8.2 + 0.7 base-emitter drop) Q1 will turn on and a fault will be indicated.

Transistors Q4 and Q5 are drivers for the front panel LED CRI. These are powered from the +13.8 Vdc line before the 8V regulator. Therefore, if the regulator opens, a fault will still be indicated.

VOLTAGE REGULATOR

U8 is a monolithic integrated-circuit voltage regulator providing 8 Vdc. This powers all circuitry in the module with the exception of Q2, the front panel LED and its drivers.

ADDRESS DECODER

The address decoder consists of U2, an 8-stage shift register, and U9, a BCD-to-decimal decoder. When A2, A1 and A0 are '1', '1', '0', respectively and the ENABLE line is high, Q7 on U9 goes high. This enables data input to U2 to propagate through it, controlled by the clock pulses on U2-3. When the ENABLE signal goes low, U9-4 goes low, and the shift-register outputs are latched. Q1 on U2 is then high for the 12.5 kHz mode, and low for the 25 kHz mode.

MAINTENANCE

RECOMMENDED TEST EQUIPMENT

The following test equipment is required to test the IF Module.

1. FM Signal Generator; HP 8640B, HP 8657A, or equivalent
2. AF Generator or Function Generator
3. Audio Analyzer; HP 8903B, HP 339A, or equivalent
4. Oscilloscope
5. Frequency Counter; Racal-Dana 9919 or equivalent
6. DC Meter for troubleshooting
7. Power Supply; 13.8 Vdc @ 150 mA
8. Power Supply; 12 Vdc @ 20 mA

ALIGNMENT PROCEDURE

1. Apply 13.8 Vdc and 12 Vdc supplies to module.
2. Verify 13.8 V DC current consumption is between 90 and 150 mA, and 12 Vdc current is between 12 and 18 mA.
3. Verify fault output is 0 to 0.5 Vdc and front panel LED is off.

4. Apply a standard input signal to the module input. (-60 dBm, 21.4 MHz signal modulated with 1 kHz AF, 3 kHz peak deviation)
5. Monitor TP5 with a high-impedance probe connected to the frequency counter. Adjust L10 for a reading of 455 kHz \pm 100 Hz.
6. Set VRI for 1 Vrms \pm 3% at module output (pin 31C on 96 pin connector J2).

IF amplifier Q2 has a nominal 8 dB gain. U1 has a nominal gain of 30 dB. The mixer has about 2 dB loss with proper LO injection. The proper crystal oscillator level is 10 mV pk measured at TP3.

The following four test points are provided on the PWB for additional test capability:

- TP1: 60 mV pk @ 21.4 MHz with -30 dBm input signal
- TP3: 10 mV pk @ 20.945 MHz independent of input signal
- TP4: 20 mV pk @ 455 kHz with -60 dBm input signal
- TP5: 750 mV pk @ 455 kHz with -60 dbm input signal

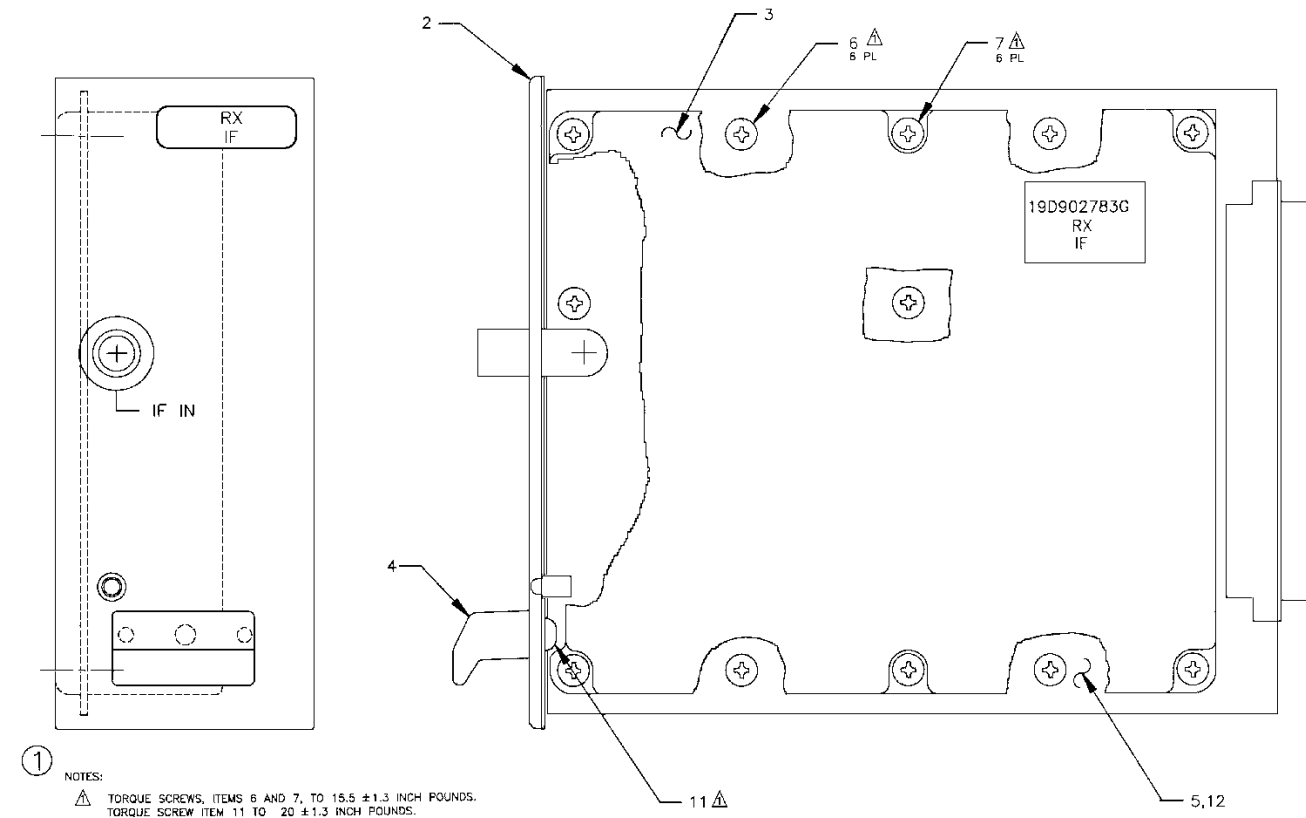
All RF voltages measured with 10 Megohm, 11 pF probe.

TROUBLESHOOTING

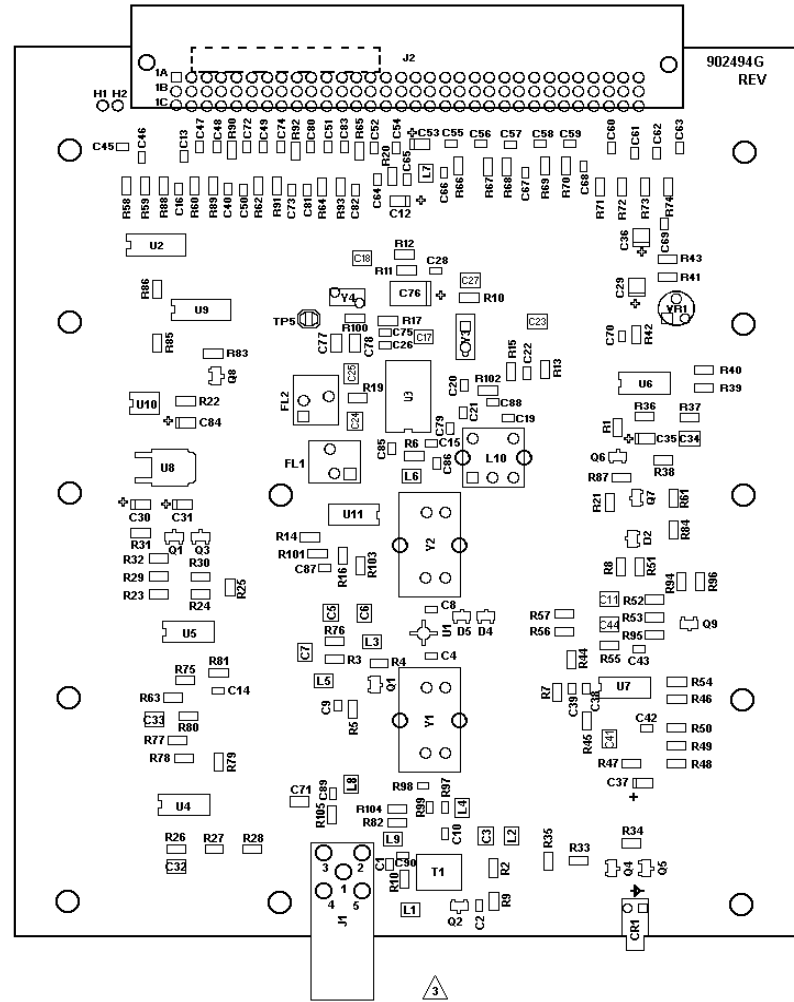
When troubleshooting the module, it is most convenient if the standard test fixture is used. The following conditions are with the module in the 25 kHz mode. This can be set up using a PC with the necessary software connected to the test fixture. Alternatively, a wire link can be soldered between holes H1 and H2 on the PC board.

TROUBLE SHOOTING GUIDE

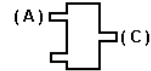
SYMPTOM	CHECK (CORRECT READING SHOWN)	INCORRECT READING INDICATES DEFECTIVE COMPONENT
Fault indicator on	Check DC voltages +8V at U8 Pin 1 +4v at U6 Pin 7 5.5V at U1 output pin 6V at U3 Pin 5	If DC voltages not correct U8 or associated components U6 or associated components U1 or associated components U3 or associated components If DC voltages correct U4, U5, U6, DI, Q3, Q4, Q5
No audio - no noise	With no signal applied to module IF input Check for AF noise @ C29 ; 200mV Check for AF noise @ U6 Pin 14:1 V	U3 or associated components U6 or associated components
Noise only - no demodulated audio	Check crystal oscillator: TP3 10 mVpk 20.945 MHz Apply-30 dBm 21.4 MHz input, check TP1 60 mVpk Apply-60 dBm 21.4 MHz input, check TP4 20 mVpk	U3, Y3 or associated components Q2, Y1, U1 or associated components U3, FL1 or associated components
Poor 12 dB SINAD	Check crystal oscillator: TP3 10 mVpk 20.945 MHz Apply-30 dBm 21.4 MHz input, check TP1 60 mVpk Apply-60 dBm 21.4 MHz input, check TP4 20 mVpk	U3, Y3 or associated components Q6, Y1, U1 or associated components U3, FL1 or associated components
No squelch function	With squelch pot maximum, or with module AUDIO/SQUELCH/HI connected to SQUELCH/ARM input and with no signal to module IF input: Check Presence of 1 Vpk noise at U6 Pin 14 Check presence of 1 Vpk noise U7 at Pin 1 Check DC voltage U7 at Pin 8: 7V Check DC voltage U7 at Pin 14: 0.5V	U6 or associated components U7 or associated components



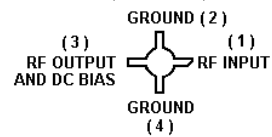
RECEIVER IF MODULE
 19D902783G7
 (19D902783, Sh. 1, Rev. 2)



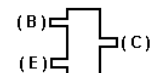
LEAD IDENTIFICATION FOR
D1, D2, D4, D5
(SOT) DIODES
(TOP VIEW)



LEAD IDENTIFICATION FOR
U1
(TOP VIEW)

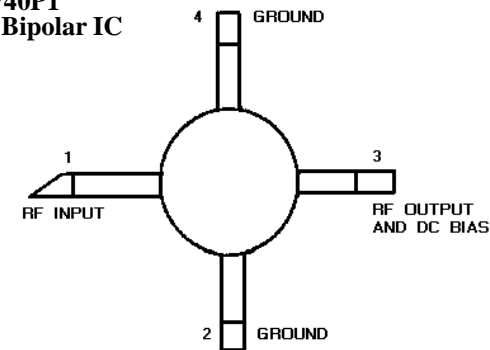


LEAD IDENTIFICATION FOR
Q1-Q9
(SOT) TRANSISTORS
(TOP VIEW)

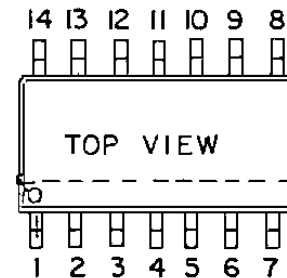
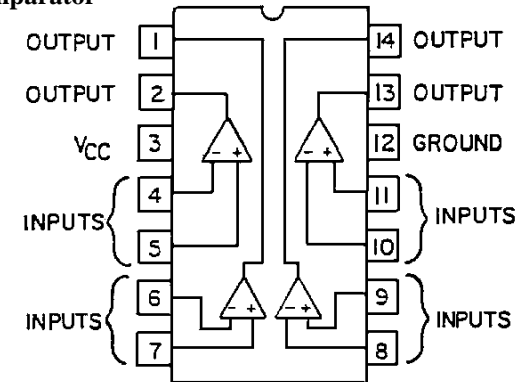


CAUTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

U1
344A3740P1
Silicon Bipolar IC

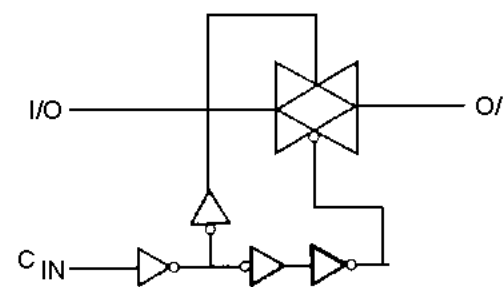


U4 & U5
19A704125P1
Quad Comparator

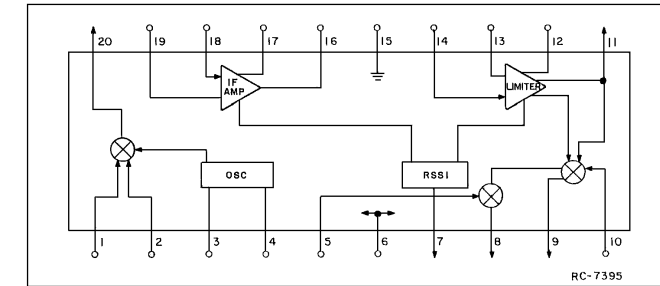


U11
RYT3066018/C
Bilateral Switch

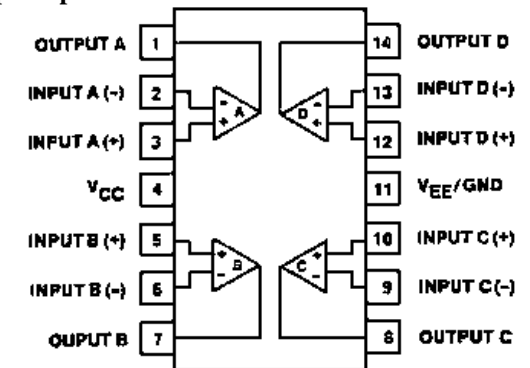
LOGIC DIAGRAM (PER CHANNEL)



U3
19A705535P3
FM Receiver

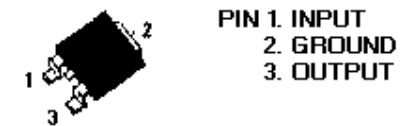


U6 & U7
19A701789P5
Quad Op-Amp

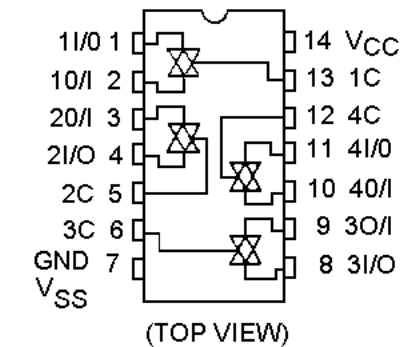


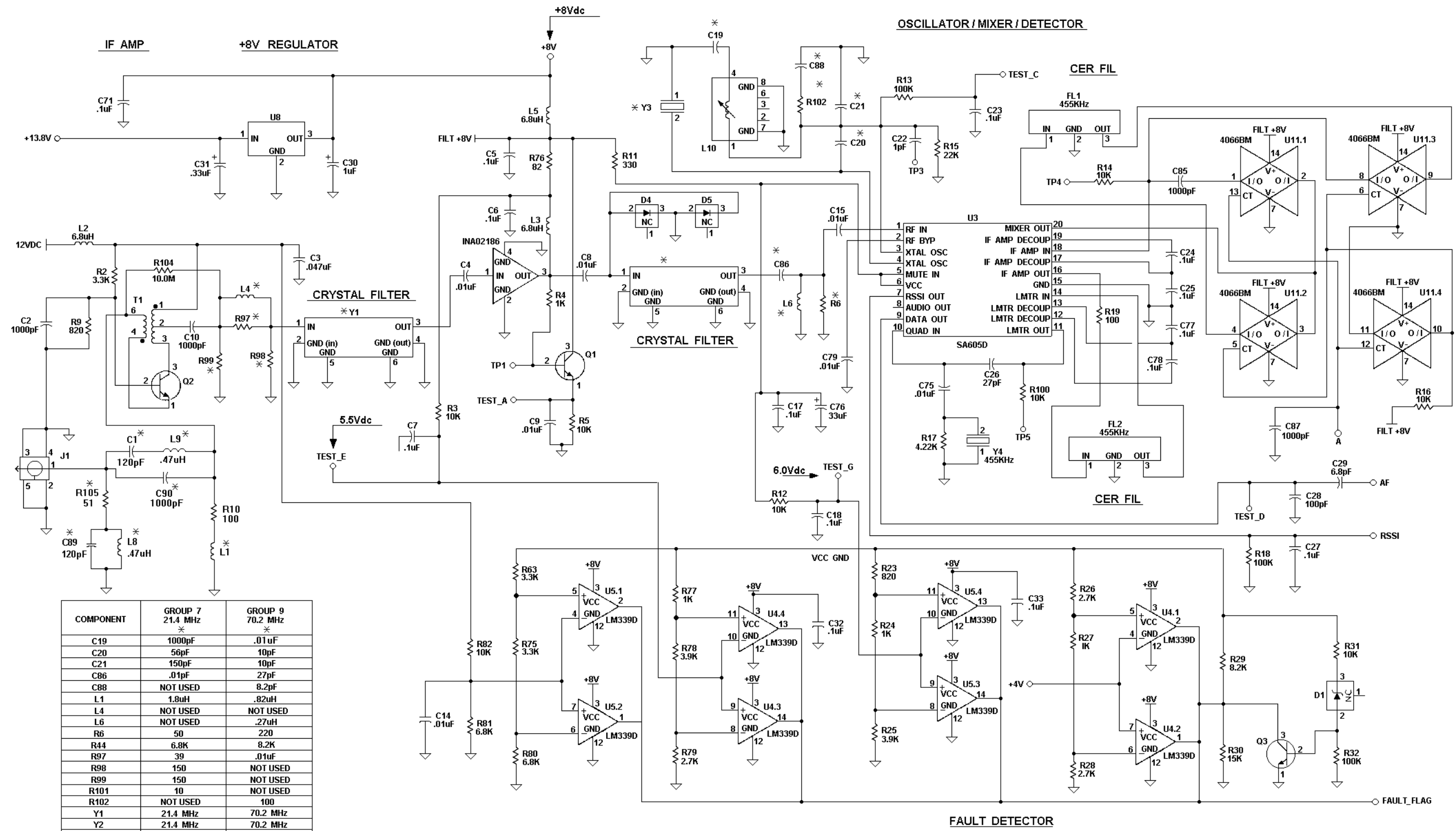
U8
19A704971P10
Voltage Regulator

(Heatsink surface connected to Pin 2)



PIN ASSIGNMENT



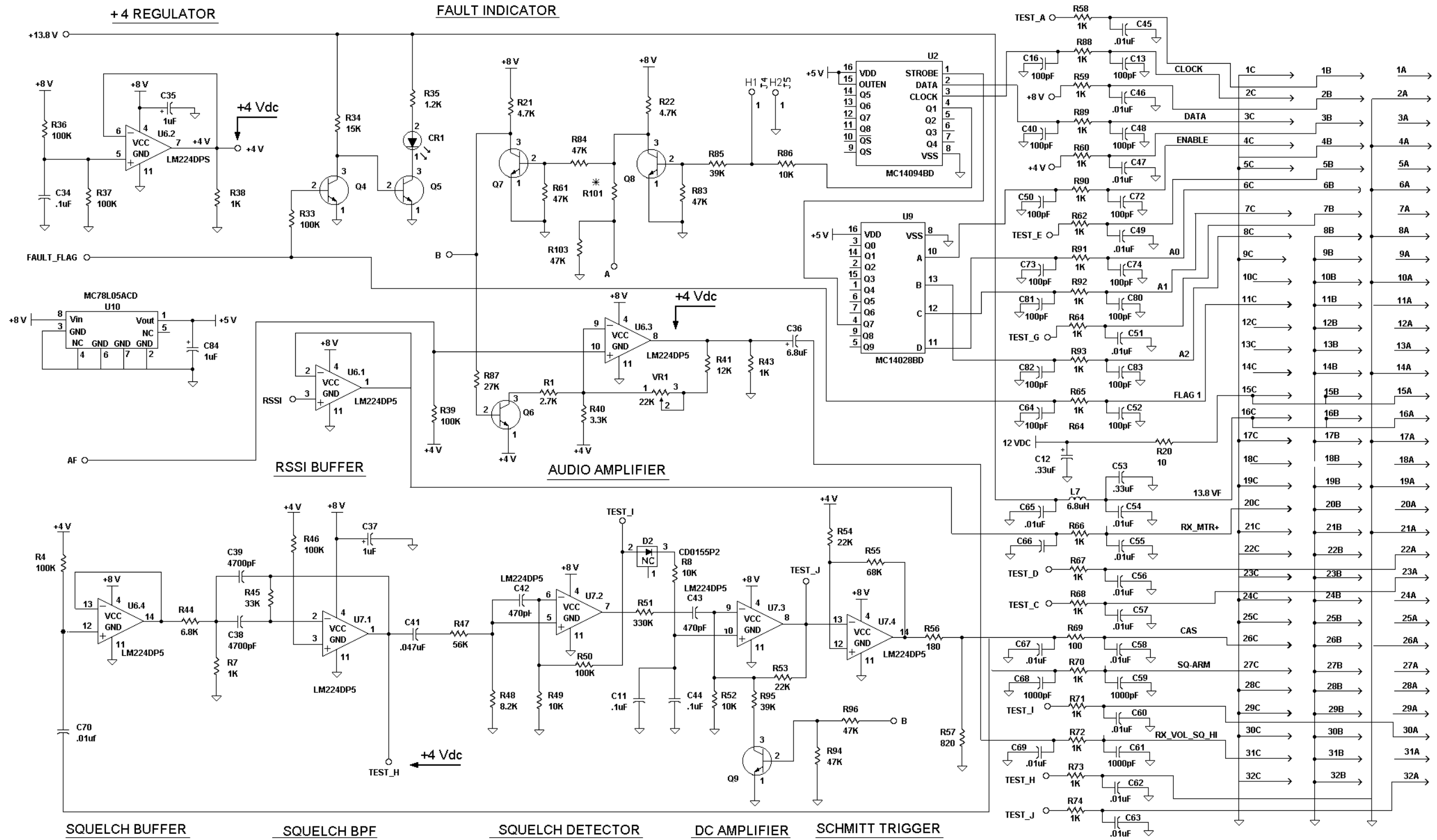


COMPONENT	GROUP 7 21.4 MHz	GROUP 9 70.2 MHz
C19	1000pF	.01 uF
C20	56pF	10pF
C21	150pF	10pF
C86	.01pF	27pF
C88	NOT USED	8.2pF
L1	1.8uH	.82uH
L4	NOT USED	NOT USED
L6	NOT USED	.27uH
R6	50	220
R44	6.8K	8.2K
R97	39	.01uF
R98	150	NOT USED
R99	150	NOT USED
R101	10	NOT USED
R102	NOT USED	100
Y1	21.4 MHz	70.2 MHz
Y2	21.4 MHz	70.2 MHz
Y3	20.945 MHz	69.745 MHz
C90	NOT USED	1000pF
R105	51	NOT USED
C89	120pF	NOT USED
L8	.47uH	NOT USED
C1	120pF	NOT USED
L9	.47uH	NOT USED
R104	NOT USED	NOT USED

THIS SCHEMATIC DIAGRAM APPLIES TO
 -MODEL NO.- REV LETTER
 PL19D902494G7 A
 PL19D902494G9 A

ALL dc measurements +/- 10%

RECEIVER IF MODULE
 19D902494G7
 (188D5586, Sh. 1, Rev. 2)



All dc measurements +/- 10%

