MAINTENANCE MANUAL

TONE INTERFACE MODULE
188D5885G1

TABLE OF CONTENTS

ERISSON

SPECIFICATIONS

Tone Interface Module 188D5885G1 is compatable with Modem data and RS-232 data **EDACS®** Simulcast Systems.

Tables 1 through 4 show the specification of the Tone Interface Module as follows:

- Table 1 outlines the general specifications.
- Table 2 outlines the power drain specifications.
- Table 3 outline the P1 Connector interface.
- Table 4 contains jumper configurations.

Table 1 - General Specifications

ITEM	SPECIFICATION
Input Voltage	+5 Volts ±10%
Operating Temperature	0 to +60° Centigrade
Dimensions	8.0 (L) By 4.0 (W) Inches
Digital/Data Type	RS-232

Table 2 - Power Specifications

VOLTAGE	CONNECTOR POINT	TOLERANCE	CURRENT DRAIN TYPICAL mA	CURRENT DRAIN MAXIMUM mA	CURRENT DRAIN STANDBY mA
+5	J1.1, J1.32, J1.33, J1.64	10%	100	150	N/A

Table 3 - Connector J1 Definition

CONNECTOR PIN (J1)	SIGNAL NAME	INPUT/ OUTPUT	ANALOG/ DIGITAL	LEVEL DIGITAL DC-VOLTS AC-VRMS
1A	5 V	I	-	+5 Vdc
1C	5 V	I	-	+5 Vdc
2A	GND	I	-	0
2C	GND	I	-	0
3A	300 HZ M IN T	I	A	-10 dBm
3C	300 HZ M IN R	I	A	-10 dBm
4A	2400 HZ M IN T	I	A	-10 dBm
4C	2400 HZ M IN R	I	A	-10 dBm
12C	GND	I	-	0
14C	GND	I	-	0
16A	INA+ (Not Used)	I	-	RS-422
16C	INA- (Not Used)	I	-	RS-422
18A	IND+ (Not Used)	I	-	RS-422

Continued

Continued

CONNECTOR PIN (J1)	SIGNAL NAME	INPUT/ OUTPUT	ANALOG/ DIGITAL	LEVEL DIGITAL DC-VOLTS AC-VRMS
18C	IND- (Not Used)	I	-	RS-422
19C	EXT MAJOR ALARM	I	D	0-5 Vdc
20C	GND	I	-	0
21A	300 OUT	O	D	TTL
21C	GND	I	D	0
22A	9600 OUT	I	D	TTL
22C	GND	I	D	0
24C	EXT1 ALARM (Not Used	I	D	0-5 Vdc
26A	INC+ (Not Used)	I	-	RS-422
26C	INC- (Not Used)	I	-	RS-422
28A	INB+ (Not Used)	I	-	RS-422
28C	INB- (Not Used)	I	-	RS-422
30A	TONE ALARM	O	D	0-5 Vdc
31A	GND	I	-	0
31C	GND	I	-	0
32A	5V	I	-	+5 Vdc
32C	5V	I	-	+5 Vdc

Table 4 - Jumper Definition and Configuration

JUMPER	SHORTING PLUG	POSITION	DESCRIPTION
JP1	PP1	1 & 2 No Jumper	LANDLINE EXTERNAL
JP3	PP3	 1 & 2 2 & 3	300 POLARITY NORMAL INVERTED
JP4	PP4	 1 & 2 2 & 3	9600 POLARITY NORMAL INVERTED
JP5	PP5	 1 & 2 2 & 3	300 Hz PLL NORMAL BYPASS

DESCRIPTION

At the Control Point the 300 Hz timing tone and the 2400 Hz frequency reference tone are filtered to produce smooth sine waves for transmission to the transmit sites by the channel multiplexer (mux).

Tone Interface Module 188D5885G1, used at the transmit sites in the Simulcast **EDACS**, provides detection and filtering of the 300 Hz timing tone and the 2400 Hz frequency reference tone between the channel multiplexer (mux) and the Universal Sync Module (Refer to Figure 1). This interface module regenerates the 300 Hz time sync tone, which allows system operation without a Program Channel. This board may be used as a replacement for Tone Interface Module 19D902546G1 found in Modem data and RS-232 type Simulcast EDACS. A jumper option bypasses this regeneration circuit for use in systems using Program Channels. This module generates the 9600 Hz clock from the 2400 Hz sync tone. The Tone Interface Module will also accept main and standby 9600 Hz RS-422 and 300 Hz RS-422 from external sources. If either the 300 Hz or the 2400 Hz tone is missing the Tone Interface Module generates an alarm.

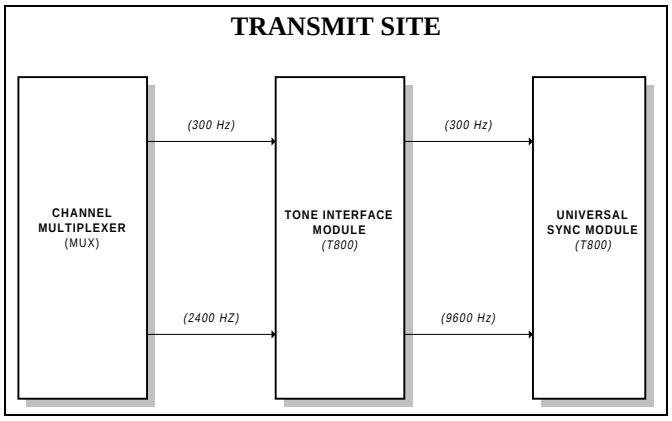


Figure 1 - Tone Interface Module System Connection

CIRCUIT AND FUNCTIONAL ANALYSIS

The Tone Interface Module of the simulcast system is used to perform the filtering and detection of the 300 Hz timing tone and the 2400 Hz tone used for synchronizing the 9600 baud data. The Tone Interface Module is physically located at the transmit site in slot 4 (J4) of the Universal Sync Unit assembly.

CONNECTORS AND SYSTEM INTERFACE

There is one connector on the Tone Interface Module. Connector J1 mates the Tone Interface Module to the Universal Sync Module when the Tone Interface Module is plugged into the Universal Sync Unit assembly, slot 4 (J4). A description of the various signals, data and clocks used between the Tone Interface Module and the Universal Sync Unit is summarized in Table 3.

There are four jumper connections on the Tone Interface Module. Jumper JP1 selects the source of the 300 Hz and 9600 Hz tones. This jumper is installed for landline and removed for external (GPS). Jumper JP3 determines the 300 Hz polarity. Jumper JP4 determines the 9600 Hz clock polarity. Jumper JP5 is used to select 300 Hz tone regeneration or bypasses the regeneration circuit so it can be used with a Program Channel. Table 4 shows the jumper definitions.

300 Hz TIMING TONE

The 300 Hz tone (sine wave) from the channel multiplexer connects to the Tone Interface Module through connector J1, Pins 3A and 3C (Refer to Figure 2 and the Schematic Diagram). This signal is coupled through coupling transformer T1 and a filter circuit consisting of resistors R1, R2 and capacitor C1 to the noninverting positive input of limiter operational amplifier U4.2, Pin 5. Resistor R1 provides the nominal 600 ohm line terminating impedance. The RC network of R2 and C1 provide the high frequency noise roll off to noise components in the received channel multiplexer tone audio. The rollover frequency is located at 1600 Hz.

Operational Amplifier U4.2 operates in an open loop configuration as a hard limiter (comparator) and converts the 300 Hz sine wave to a 300 Hz square wave. The output of U4.2, Pin 7 connects to the positive noninverting input of operational amplifier U4.3, Pin 10. The negative input to U4.3, Pin 9 is biased at 2.7 Vdc. This bias voltage is provided by zener diode VR1. Amplifier U4.3 conducts when the input is greater than 2.7 Vdc. The **300 Hz IN** can be metered at test point TP1. The output of U4.3 connects to the input of Schmitt Trigger U3.6, Pin 13. The output on U3.6, Pin 12 is high when U4.3 conducts, producing a buffered, inverted 300 Hz square wave input to **P**hase-**L**ocked-**L**oop (**PLL**) circuit U8. At this point the 300 Hz square wave, **300 Hz PLL**, is connected to PLL U8, Pin 14 *(SIGin)*. The **300 Hz PLL** is also connected to jumper JP5 so the regeneration circuit can be bypassed if desired (Refer to **Bypass**).

Bypass of Regeneration Circuit

In normal operation, the 300 Hz timing tone is regenerated and a Program Channel is not required. The jumper JP5 is set to jumper JP5.1 & JP5.2, routing the 300 Hz through the regeneration circuitry to data selector U18. If program channel is in use, jumper JP5 is set to JP5.2 & 5.3 bypassing the regeneration circuitry and connects the 300 Hz timing tone directly to Data Selector U18, Pin 2 (*A1).*

Regeneration

The regeneration circuit consists of PLL U8, operational amplifier U11.1, **V**oltage **C**ontrolled **O**scillator (**VCO**) U10 and divide by 8 counters U12 and U16. When a **300 Hz PLL** signal is on U8, Pin 14 *(SIGin),* U8 generates a **VCO** control voltage on Pin 13 *(PC2out).* This output voltage connects to the positive input of operational amplifier U11.1, Pin 3. The output of U11 on Pin 1 connects through a resistor network consisting of resistors R16 through R19 to control the frequency output of U10. Variable resistor R19 and capacitor C26 set the frequency of operation. Voltage controlled oscillator U10 oscillates at 19200 Hz. The output of U10 on Pin 3 *(OUTP)* connects to the clock pulse input of divide by 8 counter U16, Pin 1 *(CP1).* Counter U16 divides the 19200 Hz down to 2400 Hz on Pin 11 *(Q3).* The output on Pin 11 connect to the clock pulse input of divide by 8 counter U12, Pin 1. Counter U12 divides the 2400 Hz down to 300 Hz output on U12, Pin 11 *(Q3).* This 300 Hz output, **300 Hz PLL,** connects to U8, Pin 3 *(COMPin).* PLL U8 compares the signal on Pin 3 with the signal on Pin 14 *(SIGin)* to control the VCO control voltage on Pin 13 *(PC2out).* When the signals on U8, Pin 3 and Pin 14 are the same (*300 Hz)* oscillator U10 is phase locked at 19200 Hz.

The output on U12, Pin 11 also connects to jumper JP5.1 where it is jumpered to the input of data selector U18, Pin 2 *(A1).*

2400 Hz REFERENCE TONE

The 2400 Hz reference tone (sine wave) from the channel multiplexer connects to the Tone Interface Module through connector J1, Pins 4A and 4C. This signal is coupled through coupling transformer T2 and a filter circuit consisting of resistors R3, R4 and capacitor C4 to the noninverting positive input of limiter operational amplifier U14.2, Pin 5. Resistor R3 provides the nominal 600 ohm line terminating impedance. The RC network of R4 and C4 provide the high frequency noise roll off to noise components in the received channel multiplexer tone audio. The rollover frequency is located at 1600 Hz.

Operational Amplifier U14.2 operates in an open loop configuration as a hard limiter (comparator) and converts the 2400 Hz sine wave to a 2400 Hz square wave. The output of U14.2, Pin 7 connects to the positive noninverting input of operational amplifier U14.3, Pin 10. The negative input to U14.3, Pin 9 is biased at 2.7 Vdc. This bias voltage is provided by zener diode VR1. Amplifier U14.3 conducts when the input is greater than 2.7 Vdc. The **2400 Hz IN** can be metered at test point TP2. The output of U14.3 connects to the input of Schmitt Trigger U13.6, Pin 13. The output on U13.6, Pin 12 is high when U14.3 conducts, producing a buffered, inverted 2400 Hz square wave input to PLL circuit U7, Pin 14 *(SIGin).*

9600 Hz CLOCK

PLL U7 generates a VCO control voltage on Pin 13 *(PC2out).* This output voltage connects to the positive input of operational amplifier U15.1, Pin 3. The output of U15 on Pin 1 connects through a resistor network consisting of resistors R20 through R23 to control the frequency output of voltage controlled oscillator U9. Variable resistor R23 and capacitor C31 sets the operating frequency of U9. Voltage controlled oscillator U9 oscillates at 19200 Hz. The output of U9 on Pin 3 *(OUTP)* connects to the clock pulse input of divide by 8 counter U6, Pin 1 *(CP1).* Divide by 8 counter U16 divides the 19200 Hz by 2 to generate a 9600 Hz clock output on Pin 9 *(Q1).* This output connects directly to data selector U18, Pin 14 *(A4*). Counter U16 also divides the 19200 Hz by 8 to a 2400 Hz output on Pin 11 (Q3). This 2400 Hz output, **PLL,** connects to U7, Pin 3 *(COMPin).* PLL U7 compares the signal on Pin 3 with the signal on Pin 14 *(SIGin)* to control the VCO control voltage on Pin 13 *(PC2out).* When the signals on U7, Pin 3 and Pin 14 are the same (*2400 Hz)* oscillator U9 is phase locked at 19200 Hz.

DATA SELECTOR U18

Data selector U18 is intended to select between external sources **300 Hz EXT** and **9600 EXT** as controlled by the **EXT MAJOR ALARM** on J1.51 and U18, Pin 1 *(A/B).* The **EXT MAJOR ALARM** is connected when jumper JP1 is removed. This function is **not** being used at the present time (JP1 should be in place). The 300 Hz on U18, Pin 2 (A1) and the 9600 Hz on U18, Pin 14 (A4) connect straight through to the corresponding outputs on U18, Pins 4 and 12 to the **OUTPUT POLARITY** circuits.

OUTPUT POLARITY

300 Hz

The 300 Hz output U18, Pin 4 connects to the input of Schmitt trigger U3.1, Pin 1. The output of U3.1, Pin 2 can then be connected to a second Schmitt trigger (U3.2) to change the polarity of the signal or connected directly to the 300 Hz timing tone output on 21A. When jumper JP3 is across JP3.1 & JP3.2, the output of U3.1 bypasses U3.2. When JP3 is across JP3.2 & JP3.3, U3.2 is in the circuit (output is inverted).

9600 Hz

The 9600 Hz output U18, Pin 12 connects to the input of Schmitt trigger U13.1, Pin 1. The output of U13.1, on Pin 2, can then be connected to through a second Schmitt trigger (U13.2) to change the polarity of the signal or connected directly to the 9600 Hz clock output on 22A. When jumper JP4 is across JP4.1 & JP4.2, the output of U13.1 bypasses U13.2. When JP4 is across JP4.2 & JP4.3, U13.2 is in the circuit (the output is inverted).

TONE ALARM

When either the 300 Hz timing frequency or the 2400 Hz tone disappears the Tone Interface Module generates an alarm.

The output of U4.2, Pin 7 connects through diode D1 to the positive input of operational amplifier U4.1, Pin 3. This signal is filtered by low pass filter capacitor C6 and resistor R5. The negative input of U4.1, Pin 2 is biased at 2.7 Vdc. When the rectified, low pass filtered 300 Hz tone through D1 drops below 2.7 volts, the output on U4.1, Pin 1 goes high. This high is connected to the input of NAND gate U5.4, Pin 2 *(A)*.

The output of U14.2, Pin 7 connects through diode D2 to the positive input of operational amplifier U14.1, Pin 3. This signal is filtered by low pass filter capacitor C35 and resistor R28. The negative input of U14.1, Pin 2 is biased at 2.7 Vdc. When the rectified, low pass filtered 2400 Hz tone through diode D2 drops below 2.7 volts, the output on U14.1, Pin 1 goes high. This high connects to the input of NAND gate U5.4, Pin 3 *(B)*.

When either the 300 Hz DETECT input on U5.4, Pin 2 or the 2400 Hz DETECT on U5.4, Pin 3 goes low, the output on U5.4, Pin 1 goes high on 30A to create an alarm.

POWER DISTRIBUTION AND FILTERING

The + 5 volt power supply used by the Tone Interface Module is derived from the simulcast power supplies (+5V). The +5 volt power inputs on J1.1, 32, 33 and 64 is used to power all active components on the Tone Interface Module. Power bypass capacitor C23 is used on the Tone Interface Module to filter any power noise transients or spikes from affecting circuit operation performance.

FUTURE CAPABILITY

NOTE

Quad Line Receivers U2, NAND gates U5.2 and U5.3 and Data Selector U17 are not used at this time.

INSTALLATION INSTRUCTIONS

Universal Sync Shelf and Modules

1. When used in Universal Sync backplane 19D902540G1, a jumper must be added between J5-C28 and J5-A30 on the backplane board according to **Modification Instructions** 19B804272 (Refer to Table of Contents).

NOTE

The run cut in the Modification Instructions is only needed if Intraplex Channel Banks are used.

2. Change jumper P7 from 1 - 2 to 2 - 3 on the Master Universal Sync Module

3. Follow maintenance manual LBI-39069, section 4.6 (300 Hz polarity check) and section 4.7 (9600 Hz clock edge reference check) to obtain correct polarity settings for JP3 and JP4. Jumper JP4 is to be changed rather than jumpers on all universal sync cards.

Systems Without Program Channel Units

Tone Interface Module 188D5885G1 is required for Modem data and RS-232 type Simulcast systems that do not employ program channels for the 300 Hz and 2400 Hz tones. The following instructions apply to systems using NEC channel banks and 4-wire E&M cards for distribution of these tones.

1. Install 4W E&M cards (P/N X5260B) in CH 21 and CH 24 slots (Control Point and Tx Sites. Set XMT to 25.5 dB at the Control Point and set RCV ATT to) dB at the Tx sites.
2. On Microwave Cross Connect Panel 188D5114P1, cut the printed circuit runs between J7C-3-4-5-6 and J12-24-49-21-46. On the backside of the printed circuit board these 4 runs drop vertically from J7C. On the front of the printed circuit board these 4 runs feed through the board between J15 and J25. This modification applies to control point and Tx site Cross Connect panels.

NOTE

Once this modification is done, the Cross Connect panel will not work with program channel units.

Tone Interface Module Adjustment

The module will be preset by the factory. If the 300 Hz and /or 9600 Hz tones lose lock the following adjustments are needed.

1. For the 300 Hz tone, adjust R19 for a 1.75 Vdc reading measured at U11, Pin 1.
2. For the 9600 Hz tone, adjust R23 for a 1.75 Vdc reading measured at U15, Pin 1.

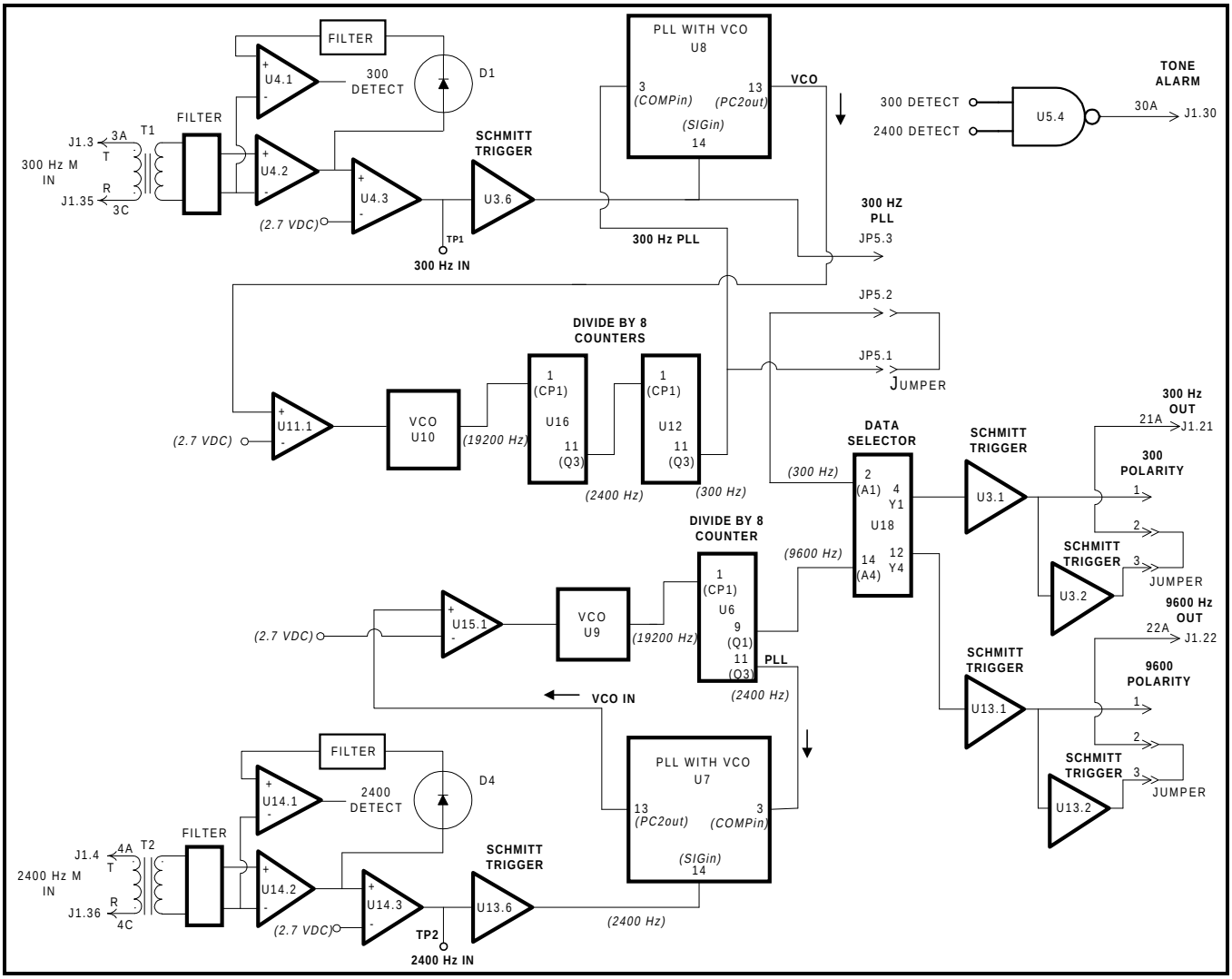


Figure 2 - Block Diagram

Tone Interface Module 188D5885G1

SYMBOL	PART NUMBER	DESCRIPTION
		------CAPACITORS------
C1 thru C5	T644ACP310K	Polyester: 0.01 µF ±10%, 50 VDCW.
C6 and C7	19A701534P3	Tantalum: 0.47µF ±20%, 35 VDCW
C10 thru C12	T644ACP310K	Polyester: 0.01 µF ±10%, 50 VDCW.
C13	19A701534P6	Tantalum: 4.7 µF ±20%, 35 VDCW
C14 and C15	T644ACP310K	Polyester: 0.01 µF ±10%, 50 VDCW.
C16	19A701534P9	Tantalum: 47 µF ±20%, 6.3 VDCW
C17	19A701534P6	Tantalum: 4.7 µF ±20%, 35 VDCW
C18	19A701534P8	Tantalum: 22 µF ±20%, 16 VDCW
C19	19A701534P9	Tantalum: 47 µF ±20%, 6.3 VDCW
C20 thru C22	T644ACP310K	Polyester: 0.01 µF ±10%, 50 VDCW.
C23	19A703314P1	Electrolytic: 100 µF -10 +50%, 10 VDCW; sim to Panasonic LS Series.
C24 and C25	T644ACP310K	Polyester: 0.01 µF ±10%, 50 VDCW.
C26	T644ACP233K	Polyester: 0.0033 µF ±10%, 50 VDCW
C27 thru C30	T644ACP310K	Polyester: 0.01 µF ±10%, 50 VDCW.
C31	T644ACP233K	Polyester: 0.0033 µF ±10%, 50 VDCW
C32 thru C34	19A700233P3	Ceramic: 220 pF ±29%, 50 VDCW.
C35	19A701534P1	Tantalum: 0.1 µF ±20%, 6.3 VDCW
C36 thru C40	T644ACP310K	Polyester: 0.01 µF ±10%, 50 VDCW.
		--------DIODES--------
D1 thru D6	19A700047P3	Schottky Barrier: 100 mW, Sim to HP 5082-2835
		------JACKS------
J1	19B801587P1	
JP1.1 thru JP5.3	19A703248P11	Contact: Electrical
		-------RESISTORS------
R1	19A701250P176	Metal Film: 604 ohms ±1%, 1/2 w.
R2	H212CRP310C	Deposited Carbon: 10k ohms ±5%, 1/4 w.
R3	19A701250P176	Metal Film: 604 ohms ±1%, 1/2 w.
R4	H212CRP310C	Deposited Carbon: 10k ohms ±5%, 1/4 w.
R5	H212CRP347C	Deposited Carbon: 47k ohms ±5%, 1/4 w.
R6	H212CRP247C	Deposited Carbon: 4.7k ohms ±5%, 1/4 w.
R7	H212CRP347C	Deposited Carbon: 47k ohms ±5%, 1/4 w.
R9	H212CRP347C	Deposited Carbon: 4.7k ohms ±5%, 1/4 w.
R10	H212CRP211C	Deposited Carbon: 1k ohms ±5%, 1/4 w.
R11	H212CRP310C	Deposited Carbon: 10k ohms ±5%, 1/4 w.
R12	19A701250P176	Metal Film: 604 ohms ±1%, 1/2 w.
R13	H212CRP410C	Deposited Carbon: 10k ohms ±5%, 1/4 w.
R15	H212CRP211C	Deposited Carbon: 1k ohms ±5%, 1/4 w.
R16 and R17	H212CRP247C	Deposited Carbon: 4.7k ohms ±5%, 1/4 w.
R18	H212CRP347C	Deposited Carbon: 47k ohms ±5%, 1/4 w.
R19	19A116430P7	Cermet, variable; 5k ohms ± 10%, Linear, 0.75 w: sim to Helitrim model 79P.
R20 and R21	H212CRP247C	Deposited Carbon: 4.7k ohms ±5%, 1/4 w.
R22	H212CRP347C	Deposited Carbon: 47k ohms ±5%, 1/4 w.
R23	19A116430P7	Cermet, variable; 5k ohms ± 10%, Linear, 0.75 w: sim to Helitrim model 79P.
R24 thru R26	H212CRP410C	Deposited Carbon: 100k ohms ±5%, 1/4 w.
R27	H212CRP310C	Deposited Carbon: 10k ohms ±5%, 1/4 w.
R28	H212CRP347C	Deposited Carbon: 47k ohms ±5%, 1/4 w.
R29	H212CRP310C	Deposited Carbon: 10k ohms ±5%, 1/4 w.
R31 and R32	H212CRP315C	Deposited Carbon: 15k ohms ±5%, 1/4 w.
R33	H212CRP251C	Deposited Carbon: 5.1k ohms ±5%, 1/4 w.

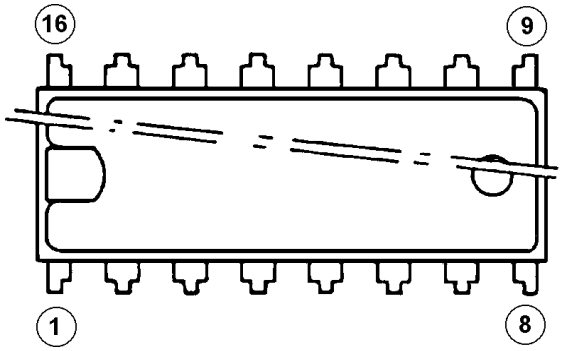
Continued

* COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

Continued

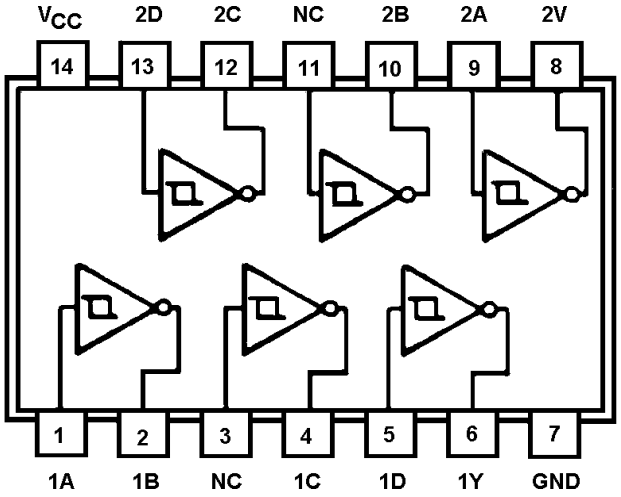
SYMBOL	PART NUMBER	DESCRIPTION
R35	H212CRP251C	Deposited Carbon: 5.1k ohms ±5%, 1/4 w.
		------TRANSFORMERS------
T1 and T2	344A3074P1	Transformer.
		------TEST POINTS------
TP1 thru TP5	19A701622P1	Pin: Cotter
		--INTEGRATED CIRCUITS--
U2	RYT109070	Quad Line Receiver; sim to 26C32.
U3	19A700037P313	Digital: Hex Schmitt-Trigger Inverter; sim to 74LS14.
U4	19A701789P1	Quad Operational Amplifier; sim to LM324
U5	19A700037P302	Digital: Quad 2-Input NAND gate with OC outputs; sim to 74S01.
U6	19A700037P45	Flip-Flop with preset & clear; sim to 74LS93.
U7 and U8	344A3064P10	Phase-Locked Loop with VCO; sim to 74HCT4046A.
U9 and U10	19A701865P1	555 Timer; sim to NE555P.
U11	19A701789P2	Linear: Dual Op Amp; sim ot LM358.
U12	19A700037P45	Flip-Flop with preset & clear; sim to 74LS93.
U13	19A700037P313	Digital: Hex Schmitt-Trigger Inverter; sim to 74LS14.
U14 and U15	19A701789P2	Linear: Dual Op Amp; sim ot LM358.
U16	19A700037P45	Flip-Flop with preset & clear; sim to 74LS93.
U17 and U18	19A700037P365	Quad 2-Line-to-1- Line Data Selector Multiplexer; sim to 74LS157D.
		----Zener Diode----
VR1	19A700025P2	2.7 Volt; sim to IN5986B

Quad Line Receiver U2
RYT109070 ***(26C32)***

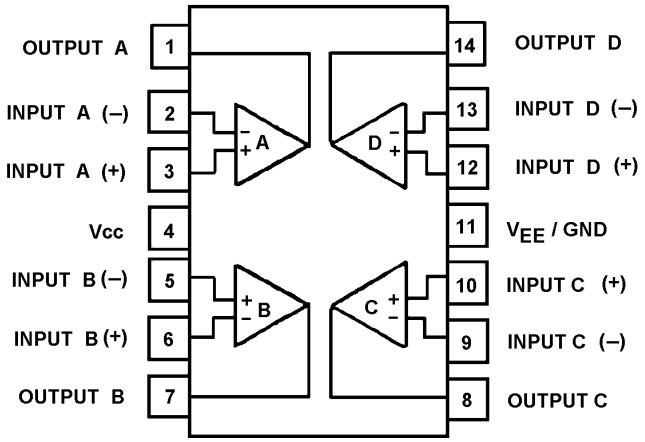


Terminal	Symbol	Function
8	GND	Ground
16	Vcc	Positive Supply
4	EN	Noninverting Enable Input
12	EN	Inverting Enable Input
Receiver 1		
1	IN-	Inverting Input
2	IN+	Noninverting Input
3	OUT	Output
Receiver 2		
5	OUT	Output
6	IN+	Noninverting Input
7	IN-	Inverting Input
Receiver 3		
9	IN-	Inverting Input
10	IN+	Noninverting Input
11	OUT	Output
Receiver 4		
13	OUT	Output
14	IN+	Noninverting Input
15	IN-	Inverting Input

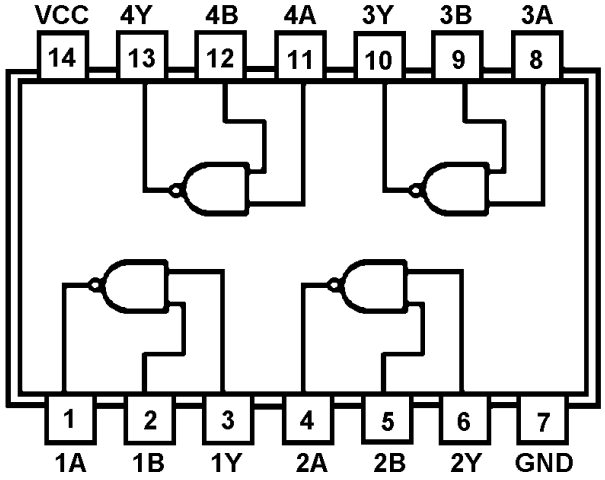
Digital: Hex Schmitt-Trigger Inverter U3, U13
19A700037P313 ***(74LS14)***



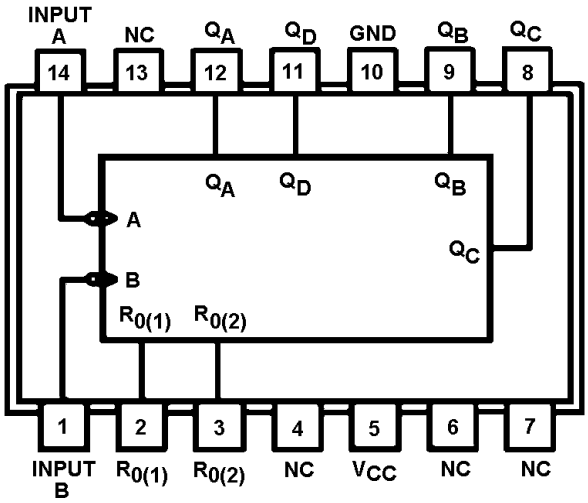
Quad Operational Amplifier U4, U14
19A701789P1 ***(LM324)***



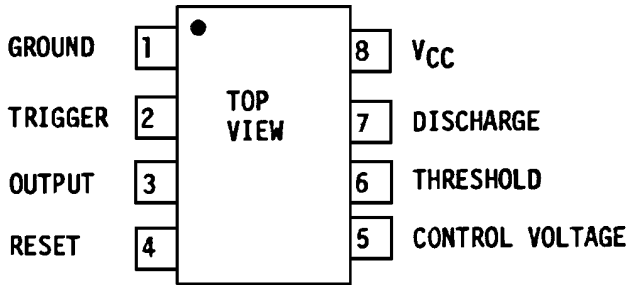
Digital: Quad 2-Input NAND Gate
With OpenCollector Outputs U5
19A700037P302 ***(74S01)***



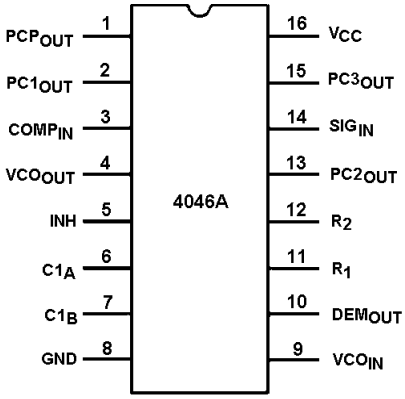
4-Bit Bianry Counters U6, U12, U16
19A700037P45 ***(74LS93)***

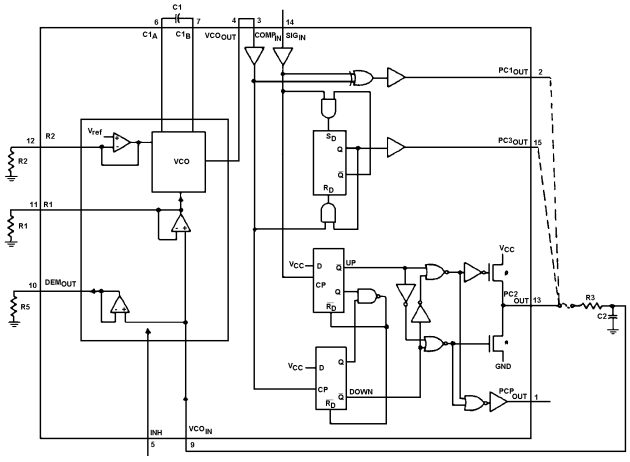


555 Timer U9, U10
19A701865P1*(NE555P)*



Phase-Locked Loop with VCO U7, U8
344A3064P10 ***(74HCT4046A)***

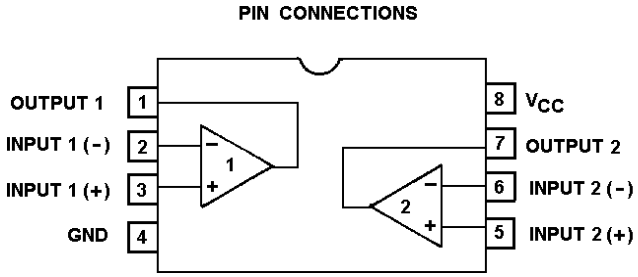




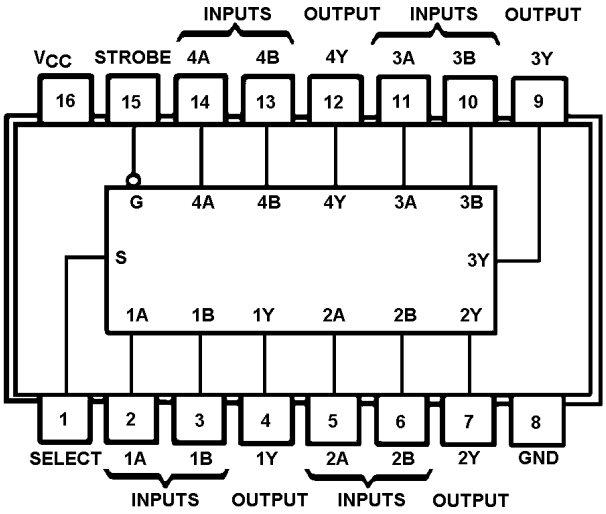
PIN IDENTIFICATION

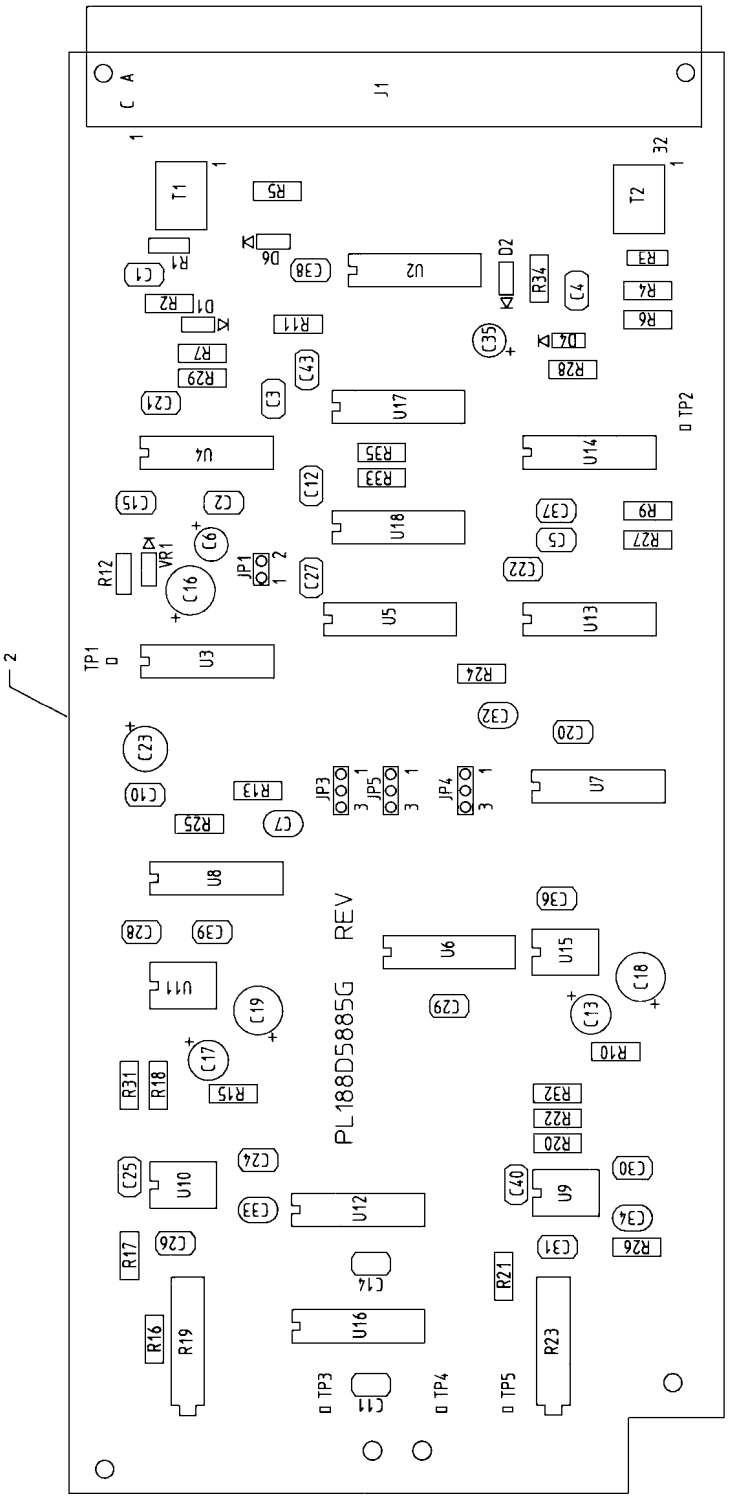
Pin No	Symbol	Name And Function
1	PCPout	Phase Comparator Pulse Output
2	PC1out	Phase Comparator 1 Output
3	COMPin	Comparator Input
4	VCOout	VCO output
5	INH	Inhibit Input
6	$C1_A$	Capacitor C1 Connection A
7	$C1_B$	Capacitor C1 Connection B
8	GND	Ground (0V)
9	VCOin	VCO Input
10	DEMout	Demodulator Output
11	R1	Resistor R1 Connection
12	R2	Resistor R2 Connection
13	PC2out	Phase Comparator 2 Output
14	SIGin	Signal Input
15	PC3out	Phase Comparator 3 Output
16	Vcc	Positive Supply Voltage

Linear: Dual Operational Amplifier U11, U15
19A701789P2 ***(LM358)***



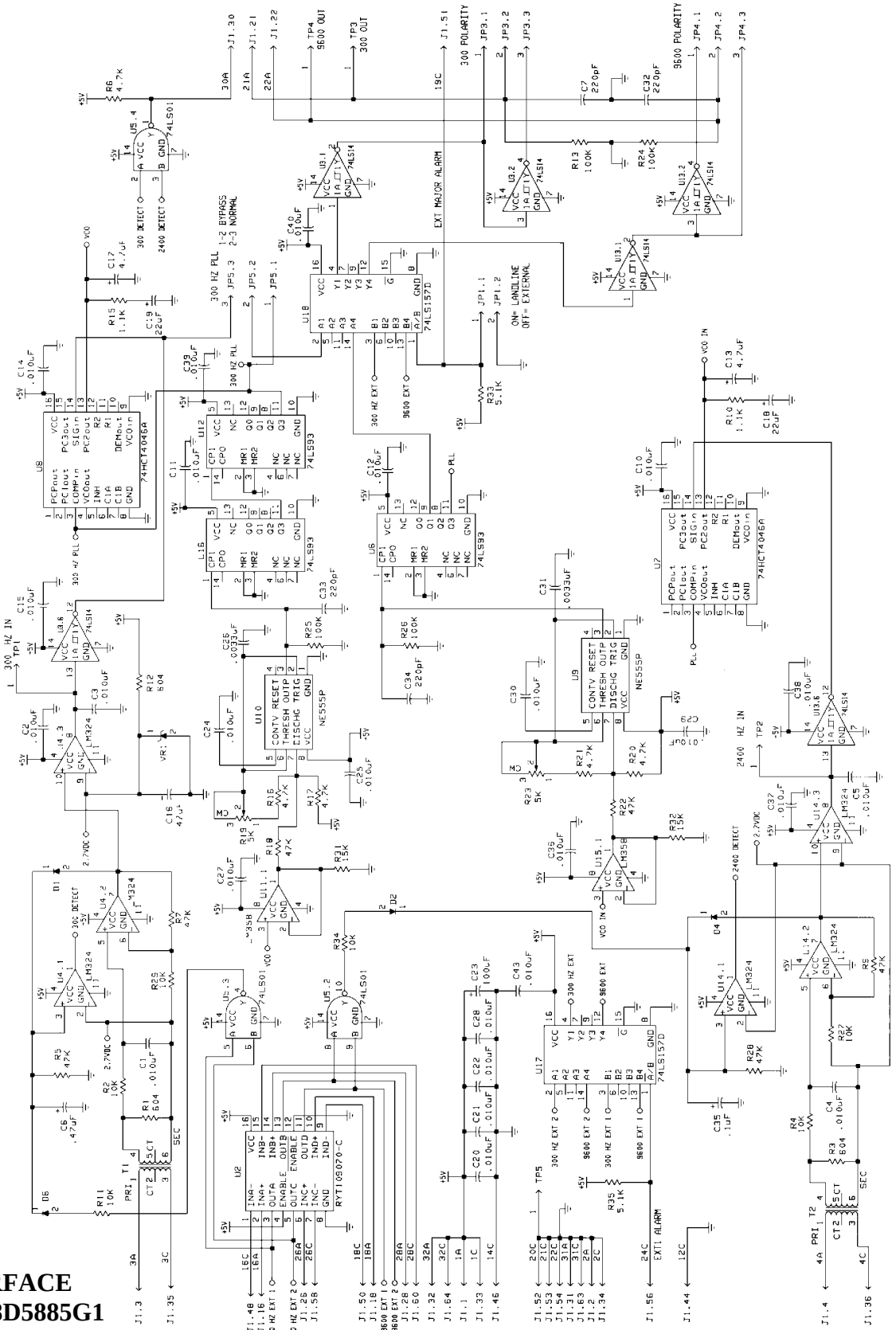
Quad 2-Line-to-1- Line Data Selector Multiplexer U18
19A700037P365 ***(74LS157D)***





TONE INTERFACE MODULE
188D5885G1

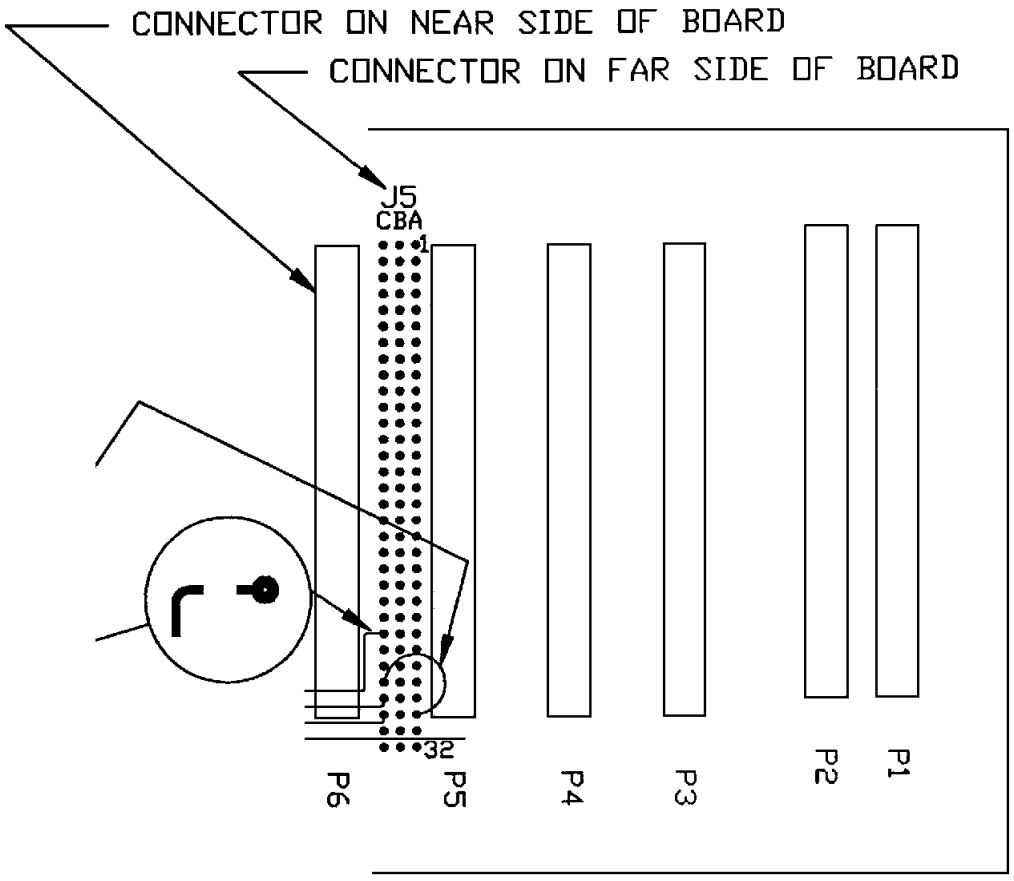
(188D5885, Rev. 3)



TONE INTERFACE MODULE 188D5885G1

(188D5883, Rev. 3)

1 MODIFY THE UNIVERSAL SYNC BACK PLANE, 19D902540G1 REV 0 FOR SIMULCAST TRANSMIT SITES AS SHOWN BELOW



CUT THE CIRCUIT RUN FROM THE BACK OF THE UNIVERSAL SYNC SHELF THAT LEAVES CONNECTOR J5 PIN 25-C TO STOP SELECTED CLOCK FROM GOING TO MASTER UNIVERSAL SYNC MODULE.

ADD JUMPER FROM J5-A30 TO J5-C28 TO ROUTE THE 9.6 OUTPUT FROM THE TONE INTERFACE MODULE TO THE 9.6 INPUT ON THE MASTER UNIVERSAL SYNC MODULE.

LABEL BOARD "MODIFIED PER 19B804272"

UNIVERSAL SYNC BACKPLANE
19D902540G1

(19B804272, Rev. 1)

Ericsson Inc.
Private Radio Systems
Mountain View Road
Lynchburg, Virginia 24502
1-800-528-7711 (Outside USA, 804-528-7711)

Printed in U.S.A.