MAINTENANCE MANUAL
SYSTEM MODULE 19D902590G6 & G7

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ILLUSTRATIONS

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DESCRIPTION

System Module 19D902590 contains all audio processing and control circuitry for the T/R and M/R shelves. The audio processing and routing is done using analog circuitry. The control circuitry utilizes high speed digital components and includes a microprocessor. Due to the high speed digital circuitry, the System Module is housed in an RFI and EMI shield.

There are four types of System Modules for various applications:

1. System Module 19D902590G6 incorporates System Board 188D5498G1 piggybacked with the Digital Signal Processing DSP Board 188D5682G1. This module is used in all MASTR IIe and MASTR III base station applications, including EDACS.

2. System Module 19D902590G7 is identical to System Module 19D903590G6, except for the chassis screen printing. This module is used in MASTR III Auxilliary Receiver Applications.

3. System Module 19D902590G1 incorporated System Board 19D903771G1 and was used in MASTR IIe DC remote applications only. This Board is no longer manufactured, but is functionally similar to the 188D5498G1 System Board. See LBI-38764.

4. System Module 19D902590G3 incorporates System Board 19D903771G1 piggybacked with the Digital Signal Processing DSP Board 19D902667G1. These Boards are no longer manufactured, but the module is functionally similar to the 19D902590G6 System Module. See LBI-38764.

Supply voltages for the System Module are generated by the Power Module and are applied to the System Module through the 96-Pin DIN connector on the backplane board.

CIRCUIT ANALYSIS

SYSTEM BOARD

Clock Circuitry

The 14.745 MHz clock drive for the System Module digital circuitry is derived from a gate oscillator circuit comprised of inverters U21C and U21D, 14.7456 MHz crystal Y1 and associated components. Resistor R110 keeps the inverter gate U21CV in the linear mode during power up for reliable clock start up. Resistor R111 and capacitor C3 provide AC and DC drives to Y1. Inverter U21D buffers the clock signal and transistors Q11 and Q12 allows microprocessor U1 to adjust the clock frequency.

When the microprocessor pulls P4.5 (Pin 60) low, Q11 and Q12 are turned on. Capacitors C52 and C53 are then switched into the circuit, changing the capacitive loading on Y1. This change causes the oscillation frequency to change approximately 300 PPM.

Reset and Watchdog Timer

The System Board contains a power up/manual reset circuit to initialize the programmed code and hardware devices on the board. The reset circuitry, consisting of digital supervisory circuit U19, monitors the +5V line. When the voltage on the +5V line is below +4.5V, U19 outputs a low going pulse on Pin 15. At the same time it also outputs a high going pulse on Pin 16. Manual reset is also possible by pulling the reset line on J1-18C low. This is accomplished through the reset switch S1 on the Power Module. Supervisory circuit U19 also provides added protection for EEPROM U6 to ensure data integrity. If the +5V line falls below 4.65V, U19 inhibits any chip select to U6 that might occur during power transients.

In addition, U19 provides a watchdog timer. The microprocessor must pulse U19, Pin 11 periodically or U19 will generate a reset. The microprocessor pulses the watchdog timer using U1, Pin 40 **(WDOG)**.

The reset pulse is applied to microprocessor U1, **P**rogrammable **P**eripheral **I**nterface **(PPI)** U34 and to the backplane Board on J1-18C.

Address Latch

The main controller on the System Board is microcomputer U1 (80C152JB). The microcomputer obtains instructions from the program stored in EPROM U4.

The lower eight bytes of the address from the microcomputer multiplex between address and data. Address latch U2 (74HC37) is used to secure the address from the microcomputer using the microcomputer ALE signal (U1-55). The upper eight bits of the address contains only address information and are applied directly to the devices needing these additional lines.

Address Decoding

One of eight de-multiplexers U3 (74HC138) is used for address decoding. The three most significant bits of the address bus (A13, A14, A15) are used to select one of eight, 8k-byte blocks of data (non-program) memory.

The microprocessor PSEN output signal at U1-54 is used to disable demultiplexer U3. This event causes all of the eight select outputs to go high so only the program EPROM U4 will be selected during accesses of program memory. This prevents bus contention on the AD lines. The following devices are mapped to an 8k-byte block of data memory:

U3-15	0000-1FFFH	EEPROM (U6)
U3-12	2000-3FFFH	RAM (U5)
U3-13	4000-5FFFH	Digital Signal Processor
U3-12	6000-7FFFH	Input/Output Latches (U7, U25)
U3-11	8000-9FFFH	82C54 Counter Timer (U29)
U3-10	A000-17	82C55 Programmable Peripheral Interface (U34)
U3-9	C000-DFFFH	not used
U3-7	E000-FFFFH	not used

Program/Data Memory

Three memory components are included on the System Board: UV EPROM U4, static RAM U5 and EEPROM U6. The microprocessor can address two 64k-byte memory segments; the program memory and the data memory. The program memory is stored in U4 and is selected by a low going pulse on microprocessor PSEN output U1-54.

The low going pulse on the PSEN output disables access to any data memory by disabling address decoder U3. This disables all chip selects to devices mapped to data memory locations (Refer to Address Decoding section for more information on devices mapped into data memory space).

The microprocessor executes program instructions fetched from EPROM U4. The microprocessor outputs the program address on AD[0:7] and A[8:15]. The address latch latches the address on AD[0:7] when ALE goes high. The EPROM inputs the 16 bit address and outputs the eight bit instruction found at the input address on AD[0:7] lines when PSEN goes low.

Data memory is stored in static RAM U5. Data can be written to and read from this device. However, all data is lost at power off. The RAM inputs the latched address output by the microprocessor when chip enable input U5-20 from address decoder U3 is low. If the RAM OE input U5-22 goes low, then the data contained in the RAM at the input address is output to the microprocessor on the AD[0:7] lines. If the RAM WE input U5-27 goes low, data on AD[0:7] is stored in the RAM at the input address.

Personality information is stored in EEPROM U6. Data can be written to and read from this device. Data stored in this device is not lost at power off. The EEPROM inputs the latched address from the microprocessor when the CE input is low. The chip enable input is generated by address decoder U3 and output on U3-15. However, the signal is routed through U19.

Supervisory circuit U19 disables the EEPROM chip enable when the board is in a reset condition. This ensures that no extraneous writes occur to the EEPROM during power-up or brown out conditions which could affect personality data.

If EPROM OE input U5-22 goes low while the CE is low, then data contained in the EEPROM at the input address is output to the microprocessor on the AD[0:7] lines. If EEPROM WE U5-27 goes low while the CE is low, then data on AD[0:7] is stored in the EEPROM at the input address.

Counter Timer IC

Counter timer U29 consists of three 16-bit timer/counters that are used for the different functions described below. The microprocessor can enable, disable and configure the counters, as well as read back counter status information using the AD bus. The input clock to the device is derived by dividing by two the 14.7456 MHz clock signal out of gate oscillator buffer U21D using D flip-flop U28. This same 7.3725 MHz clock signal is used for each counter/timer to give 135 ns resolution.

Counter 0 is used for Channel Guard decoding. It is configured to output a 135 ns pulse on U29-12 at eight times the Channel Guard decode frequency. This pulse is latched by flip-flop U18A. The output of this latch is applied to the INTO input of microprocessor U1-16, causing an interrupt. The microprocessor resets the latch, clearing the interrupt by pulsing U18A, Pin 4 using P1.6 (U1-10) output in the interrupt service routine.

The 135 ns pulse on U29-12 also causes a sample of the limited Channel Guard signal LIM_CG to be taken. This sample is brought into the microprocessor during the INTO service routine on P4.7 (U1-58) and used for Channel Guard decoding.

The second counter timer (counter 1) is used to generate a microprocessor interrupt. This interrupt is used by the microprocessor to generate Channel Guard and should occur at eight times the Channel Guard frequency. The counter is configured to send the output (U29-16) high upon timing out. This high is inverted by NPN transistor Q9 and resistors R1 and R18.

The inverted signal is then applied to the microprocessor INT1 input (U1-18) which causes an interrupt to occur. The counter is reloaded by the interrupt service routine software. This causes U29-16 to return low which clears the interrupt.

The third counter/timer (Counter 2) is used for tone generation. When a tone is desired, the microprocessor configures the counter/timer to output a square wave on U29-20 at the desired frequency. This square wave is then bandpass filtered by active filter stages U17C and U17D to remove undesired harmonics and to create a sine wave.

A resistor divider consisting of resistors R38 and R39 sets the level of the sine wave at U17-14 to approximately 800 mVrms. The microprocessor disables the counter/timer when no tone is desired.

Programmable Peripheral Interface

Programmable **P**eripheral **I**nterface **(PPI)** U34 provides three additional eight bit I/O ports. The reset generated by supervisory circuit U19 is input on U34-39 and serves to reset the U19 to the default state. Ports A and C are configured as output ports and Port B as an input port.

Port C outputs are used to load the Rx and Tx synthesizers as well as provide serial communications with the interface board. Port A outputs provide an interface to the GETC in GETC equipped stations. The system board loads the synthesizers and communicates with the interface board with the following Port C signals: RXF4/AUX2 (DATA), RXF2 (ENABLE), TXF1 (A0), TXF2 (A2), RXF1 (A2), and from Port A: SERIAL CLK (CLK). The remaining Port A and Port C inputs are used for several different interfaces.

Port B inputs several interface signals. Pull up resistors to +5V are used on all open collector type inputs. These signals are then buffered and/or level shifted where appropriate. Resistors are put in series with all of the inputs for spike protection.

Where level shifter/buffer U41 is not used, dual diodes are included to prevent over or under voltage conditions.

The RUS input uses NPN transistor Q4 to convert the signal to CMOS logic levels.

Additional I/O

Additional I/O is provided by input latch U25 and output latch U7. Each of these latches is mapped to address 6000H. However, input latch U25 is enabled by a low pulse on the microprocessor RD output while the output latch U7 is enabled by a low pulse on the microprocessor WR output.

The input latch is used to get DC CNTRL, BATT STDBY, REM PTT, TX DISABLE, CG MON and M3_STATUS signals onto the AD bus so they can be read by the microprocessor. The DC control currents are decoded elsewhere in the system and the decode current is passed to the microprocessor using DC CNTRL1, DC CNTRL2, and DC CNTRL3 inputs. These are CMOS level signals so no level shifting is required.

The BATT STDBY signal requires level shifting to convert the 22-volt high to a TTL level. This is achieved by resistors R4 and R5. Dual diode D2 limits the signal to be within -0.7 and +5.7 to guard against over or under voltage conditions. BATT STDBY is driven high when the station is operating from battery power.

Output latch U7 (74HC377) latches the data on the AD bus when the chip is selected by address decoder U3 and a low going WR pulse is received. This latched data goes into analog switch select lines used to select audio paths in the analog circuitry.

Microprocessor I/O

The microprocessor has some additional I/O pins. These pins are used to bring signals in and out of the microprocessor directly without going through any additional I/O devices such as latches or a PPI. The LOCAL PTT input is level shifted and buffered by U41E and brought into the microprocessor on U1-19.

The microprocessor also generates he AUX RX MUTE output used to mute an auxiliary receiver. The signal originates on U1-51 and is inverted by U26F. This gives an open collector active low output.

The EXT LSD SEL, LINE IN SEL, LSACQ, and 4W DUPLEX signals are also generated by the microprocessor. These signals go to the analog circuitry and control audio routing through analog switches.

The microprocessor is also capable of loading electronic potentiometers U35 and U36. Each of these potentiometers contains two 256-position variable resistors. The microprocessor must serially load all four variable resistors at the same time.

The microprocessor switches the potentiometers select line (U1-17) high. This enables the electronic potentiometer loading circuitry and allows the microprocessor to shift 34 bits of serial data into the electronic potentiometers, 17 bits of data into each IC.

Data is output on U1-20 and clocked into U35 and U36 on the rising edge of the clock signal generated by the microprocessor on U1-21. The microprocessor can also read back the current potentiometer settings.

When data is clocked into U35 and U36, the current potentiometer setting is clocked out and brought into the microprocessor on U1-22. After all 34 bits have been clocked into U35 and U36, the microprocessor pulls the potentiometer select line (U1-17) low. This ends the loading sequence, and causes the digital potentiometers to load the new resistance value.

A/D Converter

The system Board contains an A/D converter. This is used for metering DC inputs. Four external metering inputs are accommodated. These include PWR SNSR, TX MTR+ relative to TX MTR-, RX MTR+ relative to TX MTR-, and EXT JCK.

The PWR SNSR input will accommodate a DC level between zero and +5V relative to analog ground. The input is protected from over voltage conditions by a dual diode D7.

The control shelf routes TX MTR + and TX MTR - into a differential amplifier consisting of U17A, and resistors R140, R142, R145, and R146. This amplifier removes any common-mode voltage. The output of this differential amplifier is actually measured and must be between zero and 2.9 volts.

RX MTR+ input is assumed to be between zero and +5V relative to analog ground. No conditioning is performed except for dual diode D3 that protects from over or under voltage conditions.

The EXT JCK input is designed to input signals between zero and +10V relative to AGND. Operational amplifier U17B provides a high impedance and buffers the input signal. The output of this amplifier goes through a voltage divider network composed of resistors R3 and R6 that divides the DC level by two. This signal is then routed to multiplexer U33.

Analog multiplexer U33 gates one of four inputs to the A/D converter U27. The microprocessor determines which input is selected using U1-52 and U1-57. The microprocessor starts an A/D conversion by putting a rising edge on U27-5. U27 then converts the DC input voltage selected on U33 to a digital value.

The converted digital value is clocked out of U27 sequentially by the microprocessor, beginning with the most significant bit. The microprocessor selects U27 by setting U27-5 low. When the A/D converter is selected, it puts the MSB of the eight bit conversion data on U27-6. This is read by the microprocessor. Successive data bits are clocked out of the A/D converter on falling edges of its CLK output (U27-7).

When all eight bits have been clocked out, the A/D is deselected, and the next conversion cycle begins by the microprocessor setting U27-5 high.

DSP Interface

System Board 188D5498G1 is equipped with plugs to accommodate **D**igital **S**ignal **P**rocessor **(DSP) "piggy back"** board 188D5682G1. This board plugs into J2 and J3 of the system board.

The microprocessor communicates with the DSP board through the eight bit AD[0:7] bus and a dual port RAM located on the DSP board. This memory is mapped into an 8k-byte data memory segment using address decoder U3. Data can be written to and read from any of the 256 byte locations that can be addressed by AD[0:7].

The DSP board contains an address latch to latch the address information on AD[0:7] when ALE goes high. When the DSP CS is low and the microprocessor WR output is low, the data on AD[0:7] is written into the latched DSP data memory segment address. When the DSP CS is low and the microprocessor RD output is low, data on AD[0:7] is read into microprocessor U1 from the latched DSP data memory segment address.

Two handshake lines used for the DSP interface for synchronization are DSP TBLF and DSP RBLE. When the DSP has written a message to the dual port RAM, it signals the microprocessor U1 by asserting DSP TBLF low. The microprocessor then reads the message from the dual port RAM and then resets DSP TBLF high to tell the DSP that it is ready for another message.

When the microprocessor wants to send a message to the DSP it first looks at he DSP RBLE input. A high on this input indicates that the DSP receive buffer is empty and it is ready to accept a new message. When the microprocessor has written the message to the dual port RAM, it asserts the DSP RBLE low to signal the DSP that it should read the new message. The DSP resets DSP RBLE high after it has read the message.

The microprocessor can reset the DSP board by setting U1-7 high. The high is inverted by Q10, and the resulting low resets the DP board.

RS232 Interface

The system Board has an RS232 serial port for programming and diagnostics. RS232 data is received on the PGM RXD input and is converted to TTL Levels by U22A. The TTL data is brought into microprocessor internal UART on U1-14. Transmit data is output on U1-15 by the microprocessor, and level shifted to RS 232 levels by U22B. The RS232 data is output on PGM TXD.

GSC Interface

A high speed serial interface that is referred to as a global serial channel (GSC) is also included on the system board. Data is transferred bidirectionally over an RS485 differential pair made up of COMM+ and COMM.

When the microprocessor wants to send data over the GSC, it enables the drivers in U24 by outputting a low on U1-6. Data is generated internally in the microprocessor and output on U1-5. The data is converted to RS485 levels and output on the GSC by U24.

The receiver section of U24 is always enabled so the microprocessor receiver can monitor the transmitted data. This monitoring is to check for collisions on the GSC created by multiple GSC nodes transmitting simultaneously.

The drivers of U24 converts received data to TTL levels and outputs them on U24-1. The microprocessor brings the received data into its receiver on U1-4 for message decoding.

Transmitter Interface

In the 19D902590G6 system module, the system board is responsible for loading the TX Synthesizer module with the proper frequency information. When the micro-controller sees a PTT from an enabled source, it first drives ANT RLY active. This switches the antenna switch in stations with this option and also applies power to the TX synthesizer oscillator circuit. Next, data is shifted into the TX Synthesizer using A2, A1, A0, CLK and DATA. After the TX Synthesizer has been loaded with the data, enable goes active to allow the TX Synthesizer PLL Circuit time to acquire frequency lock. At the end of this ENABLE period, the micro-controller samples the TX synthesizer status bit supplied by the Interface Board. If there is no fault (synthesizer locked) then the microprocessor drives the TX OSC CNTRL (PA KEY) active which turns on the RF PA. Upon reset, or a channel change, the system board must also set the PA Power pot by sending the appropriate data to the interface board. Audio for the transmission is output on the TX AUDIO HI and the TX AUDIO LO outputs. Channel Guard is summed into TX AUDIO HI.

The 19D902590G7 system module does not utilize its transmitter interface.

Receiver Interface

At power up or upon channel change, the RX Synthesizer is programmed in the same manner as the TX Synthesizer in all system modules. Carrier activity on the selected channel is sensed by the receiver squelch circuitry and applied to the System Module on the CAS input. This active high input is level converted by transistor Q8, and applied to the microprocessor on U1-23. The microprocessor then routes audio according to the receiver or station configuration programming.

Local Controls

The system board has three switches and LED’s for local control. These switches and indicators have different functions according to the group of system module. In the 19D902590G6 system module, switch S2 is a REMOTE PTT switch. A low on this input causes the microprocessor to react as though a PTT has been received over the line. The line is also routed to an external module to activate the remote PTT input. Switch S3 is a TX DISABLE switch. When S3 is active the microprocessor inhibits all transmissions.

In the 19D902590G7 system module, switch S2 is not used. A low on this input is ignored by the microprocessor. Switch S3 is a SQ DEFEAT switch. When S3 is active the microprocessor unsquelches the receiver by setting the digital squelch pot on the interface board to zero.

All system boards are electrically equivalent. When not activated, S2 pulls the line to +5V. When activated, the switch pulls the line to ground. This switch is input on Pin 7 of input latch U25. In the case of S3, when not activated, resistor R136 pulls the line to +5V. When activated, the switch pulls the line to ground. This switch is input on Pin 8 of input latch U25.

In all system modules, switch S4 is a CG MONITOR switch. When not activated, resistor R137 pulls the line to +5V. When activated, the switch pulls the line to ground. This switch is input on Pin 9 of input latch U25. This line is also routed to the external connector. This allows an external module to activate the CG monitor input, or to examine the state of the CG MONITOR input. A low on this input causes the microprocessor to switch into Channel Guard monitor mode.

When the system module is in CG MONITOR, it lights LED DS3 by outputting a high on U1-66. This high is inverted by U2D. This allows current to flow through DS3, turning on the LED.

Putting the 19D902590G6 System Module in the transmit disable mode lights LED DS2 by outputting a high on U1-67. This high is inverted by U26C. This allows current to flow through DS2, turning on the LED. In the 19D902590G7 System Module, this LED indicates a UN SQuelch condition.

The 19D902590G6 System Module concurrently activates the TX switch output and LED DS1. The LED indicates Transmit activity. In the 19D902590G7 System Module, this LED indicates that the System Module is in Local Programming Mode.

CG High Pass and De-emphasis Filters

Receiver audio is applied to the system module VOL/SQ HI port on J1-2B. U37A buffers the input signal and removes any DC bias. With an input of 1Vrms at 1000 Hz, the output is typically 2 Vrms and is supplied to three places: Channel Guard reject filter, DSP board through DSP unfiltered audio, and Channel Guard decode.

U30A is a unity gain notch filter, centered at 205 Hz. The filter provides 25dB of attenuation. U30B, U30C, and U30D form a sixth order unity gain high pass filter with a cut off frequency of 280 Hz. U37B is a +1/-3 dB de-emphasis filter that rolls audio off at 6 dB/oct in the frequency range 300-3000 Hz.

With 1Vrms into VOL/SQ HI, the output of U37B will be 750 mVrms. This output is supplied to four places: U8A, TX Audio out, Line Audio out and the summing amplifier with the optional auxiliary receiver input. U8A is controlled by the microprocessor to switch between MIC and VOL/SQ audio to the DSP. The combination of U37A, U30A, U30B, U30C, U30D, and U37B provides the frequency envelope shaping requirements (roll-off) as shown in figure 7.

The TX Audio Out circuit consists of U15, U36A, U8C, and U37D. IC U15 is an analog multiplexer that is controlled by the microprocessor. Any of the following signals may be connected to the TX AUDIO HI output: LOCAL MIC, VOL/SQ, DSP LINE/TX AUDIO, DSP TX AUDIO, External High Speed Data, LINE Input, open (battery alarm), and ground (for no transmission). U8C is an analog multiplexer controlled by the microprocessor to sum CG into the TX audio output and increase the TX Audio gain on U37D.

Battery Alarm/Morse Code is summed with the output of U15. This allows for the transmission of the alarm signal when other signals are present. U36 is a dual digital potentiometer controlled by the microprocessor, and adjusts the transmit audio level. U37D, a gain stage that drives the TX AUDIO HI (J1-5C) and TX AUDIO LO (J1-6C), is adjustable between 40 and 250 mVrms.

U37C is the +2/-8 dB de-emphasis filter that provides a 6 dB/oct roll off from 300-3000 Hz for the local intercom or speaker audio. With a rated input of 1Vrms at 1000 Hz, the output level of this filter is 750 mVrms. This filter in combination with U37A, U30A, U30B, U30C, and U30D provides the frequency response shown in Figure 8.

U32 is the analog multiplexer for the INTERCOM Audio output. It allows for selection of VOL/SQ audio, Line input audio, Voice Guard summing, and DSP LINE/TX AUDIO. Amplifier U31C sums the multiplexed audio with Voice Guard Tone. The resulting Signal is applied to J1-7A.

CG/LSD Decode Filter

Received audio is coupled through a low pass filter to remove the audio, leaving only Channel Guard (CG) or Low Speed Data (LSD) information. A hard limiter then converts the signal into

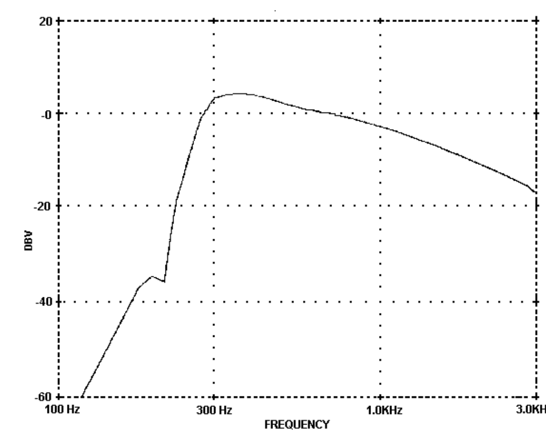


Figure 1 - Channel Guard Tone Reject (+1, -3 dBV)

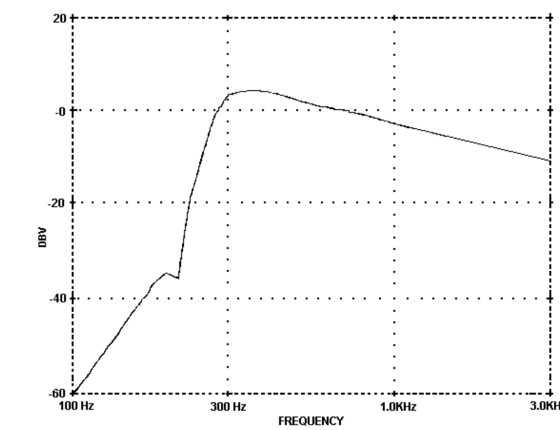


Figure 2 - Channel Guard Tone Rejct Filter (+2, -8 dBV)

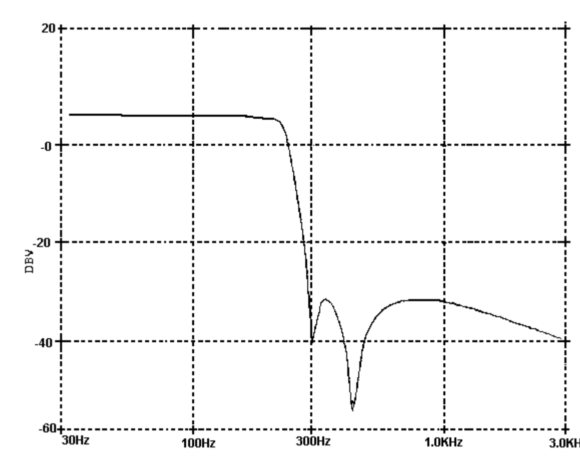


Figure 3 - Channel Guard Encode/Decode Filter

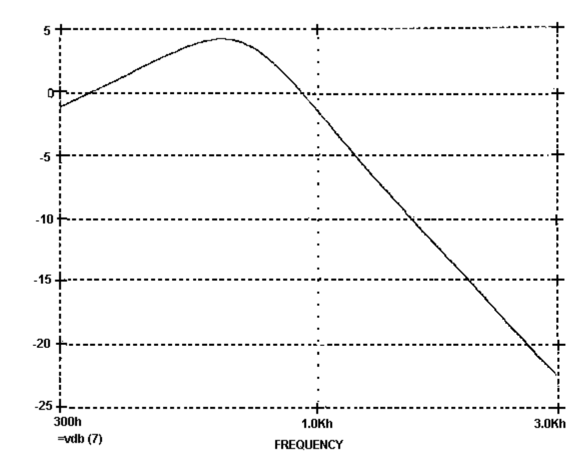


Figure 4 - Battery Alarm/Morse Code Band-Pass Filter

a digital square wave. The square wave is decoded in software as well as the 135 degree phase shift for STE.

U9A is a gain stage that supplies two frequency dependent negative resistor (FDNR) circuits. The first FDNR consists of U10A and U10B, and has a cut off at 205 Hz. The second FDNR formed by U10C and U10D, has a cut of at 230 Hz.

U11B is a low pass filter that provides added attenuation in the 300-3000 Hz range. These elements combine to provide 35 dB of attenuation for frequencies above 310 Hz. The resulting frequency response is shown in figure 9.

U11A, D5, and Q2 combine to convert the analog signal at the U11B output to a 0-5 Vdc square wave. This square wave is then supplied to U18B to be read and decoded by the microprocessor.

CG/LSD Encode Filter

U12C is used to select between external Low Speed data or Walsh bits. The Walsh bits are created by the microprocessor on U1-64 and U1-65, and form a rough sine wave. This signal is coupled through U9C to provide some gain.

U16A, U16B, U16C, and U16D form two FNDR circuits that have the same response as described in the CG/LSD Decode Filter section. U9D provides gain and drives U35A. U35A is a digital potentiometer that provides level adjustment and is controlled by the microprocessor. Also, U9B has a 3.3 K-ohm source impedance to allow a separate source to drive Channel Guard HI. This filter has the same response as shown in Figure 9.

Battery Alarm / Morse Code

The Battery Alarm / Morse Code tones are generated using U29, U17C and U17D. U29 is a clock timer that creates a square wave at the required frequency. Capacitor C113 and resistor R39 form a high pass filter to provide DC blocking. U17C is a second order low pass filter and U17D provides gain. These components combine to provide the response shown in figure 10.

The output of U17D sources the signal to U31B and U15. U15 is the TX Audio multiplexer discussed earlier in this section. U31B is an amplifier to sum the Battery Alarm signal with the Voice guard alert tone, which is then transferred to the LINE output.

Line Audio and Compression

The LINE output circuitry consists of U14, U8B, U36B, U31D, U13B, and U31A. The analog multiplexer U14 is used to connect one of the following signals to the line driver U31D: LOCAL MIC, VOL/SQ, auxiliary receiver, aux receiver/VOL/SQ, DSP LINE/TX audio, MODEM LINE data, open or ground. The open state is to transmit Battery alarm or Voice Guard alarm.

U31A sums the auxiliary receiver audio with the VOL/SQ audio. U36 B is a digital potentiometer and controls the audio level into the line driver U31D. The level at LINE A (J1-4B) and LINE B (J1-4A) is adjustable between -20 dBm and +11 dBm.

The LINE IN Audio is selected from LINE A and LINE B in a two wire system, and from DUPLEX LINE A and DUPLEX LINE B in a four wire system. Each input has a 600 ohm impedance to match the line impedance. U12B selects between two and four wire audio.

DSP BOARD

The **D**igital **S**ignal **P**rocessing **(DSP)** Board utilizes both digital and analog integrated circuits (IC's) to offer a compact, flexible, and reliable solution for audio signal analysis and modification. Most of the components are surface mounted.

The DSP Board operates with two channels of audio. It conditions audio inputs, digitizes the audio, and processes the audio data in software. The DSP Board then sends the transformed audio to analog outputs and the signal analysis information to its digital output.

Audio inputs from the system board are DSP FILT VOL/SQ, DSP UNFILT VOL/SQ, and DSP LINE IN. These signals are selected and conditioned through U10, U11, and U15. These signals are then sampled and digitized by U4 and U5. The digital audio data is then applied to U1 for processing. After processing, the audio data is then returned to U4 and U5 for digital to analog Conversion. The transformed audio is applied to the System Board on DSP TX AUDIO and DSP LINE/TX AUD.

All pertinent information from DSP analysis of the audio is communicated digitally to the system board through the dual port RAM U12. Messages are written to this memory space by the DSP microcomputer, U1. The messages are read from the memory by the System Board (via the digital signals of connector P3).

For clarity, the DSP circuitry is analyzed in the following order:
1) DSP and supporting circuitry
2) Analog input/output
3) Parallel communication port

DSP Microprocessor

The DSP Board performs its functions in the ADSP-2101 Digital Signal Processing microcomputer, U1. This chip requires external hardware to function.

Crystal Y1 provides the 8.192 MHz clock required by the DSP microprocessor. Capacitors C16 and C17 provide the loading required for reliable startup and stable oscillation.

DSP microprocessor, U1, operates form a 2K internal program memory. This program RAM is volatile; it is lost during power off sequences. Therefore, it is necessary to have non-volatile memory to safely hold the DSP Board Code. The 16K X 8 EPROM (U6) performs this function.

Upon reset, or during **"re-boot,"** up to 2K X 24 of internal program memory is loaded from this external "BOOT EPROM." The BOOT EPROM, U6, holds up to eight different pages that can be loaded. The selection of a 2K-page of code is software controlled except during reset when boot page zero is always loaded.

In essence, boot memory page is loading a sequence of read cycles. The BMS pin goes low in order to enable the boot memory chip. Addresses are sequenced on lines A0 through A13, D22 and D23. The /RD pin activates the data bus, D15 through D8, for each transfer of program memory into internal program memory space.

The boot EPROM circuitry also includes resistors R1 and R2. These resistors are zero ohms, and are the equivalents to jumper wires. If the capability of eight boot pages is necessary, R2 is removed and R1 is installed in the board. In this case, U6, Pin 1 acts as an extra address pin that is connected to D23. If the capability of four boot pages is necessary, R1 is removed and R2 is installed on the board. In this case, U6, Pin 1 acts as a program pin and is tied off to five volts.

Analog Inputs

The DSP Board inputs and processes audio both from the receiver and the line simultaneously. There are two possible receiver input settings and two possible line audio input settings. These are:
1) DSP FILT VOL/SQ
2) Two wire line input or four wire line input.

This audio selection is actuated directly by the DSP but is user programmable. The DSP uses the address multiplexer, U8, to select U7, a D flip flop register. This is accomplished by setting A13-A11 to binary 100 when /PMS goes low. Such a sequence will cause U8, Pin 14 to go low, enabling data to pass through the D flip flops upon /WR going low and then high. D8 and D9 are written to the outputs of U7 (Pins 2 and 5) as VOL/SQ SEL and CANCEL SEL.

Depending on these signals, digitally controlled analog switches (U10) route the appropriate signals to achieve the final audio input setting described above. If VOL/SQ SEL is a logic low, DSP FILT VOL/SQ is selected. If CANCEL SEL is a logic high, four wire audio is selected. If not a logic high, two wire audio is selected.

Each audio channel selection requires proper voltage level adjustment to insure an optimal conversion to the digital domain where it will be processed. This conversion is performed by codecs U4 and U5. In other words, the audio signals are conditioned to assure that their dynamic ranges can be accommodated by the codecs. The codecs will neither be under driven nor saturated. This results in a digital signal with uniform **S**ignal to **N**oise **R**atio **(SNR)** following the A/D conversion.

Filtered Receiver Input Conditioning

Filtered receiver input comes from the System Board following de-emphasis channel guard reject filtering at a maximum of 1.16 Vrms. This input channel requires no amplification to assure that codec U4 utilizes the dynamic range efficiently.

The amplification factor is determined by resistors R5 and R6. The gain is one. Therefore, the maximum input to the codec is 1.16 Vrms.

Four Wire Line Input Conditioning

Line input comes from the DPLX line input pair of the control shelf when it is in a four wire configuration. Its audio is not in contention with audio leaving the station because there are two lines independently dedicated for the output signal.

The line audio level adjustment is able to attenuate a 2.47 Vrms (+11 dBm) signal and amplify a 77.3 mVrms (-20 dBm) signal to the maximum input level of the codec (approximately 1.4 Vrms). This is to compensate for up to 30 dB of line loss that can occur between the remote control unit and the station.

In the four wire configuration, DSP LINE IN is propagated to TP1 with only a gain of 1.09 provided by the differential instrumentation circuit of U11 (A, B, C) and resistors R12-17. This occurs because the amount subtracted from DSP LINE IN is AGND (U10A, Pin 13).

Between TP1 and TP2 there is a digitally controlled variable gain stage. The gain stage is composed of U11D, U15 (1),and resistors R18 and R20. The DSP addresses (and serially loads) a resistance from 0 to 10K ohms into the dual programmable potentiometer, U15. The digitally controlled impedance, along with R18 and R20, form a gain through operational amplifier U11D.

The DSP uses address multiplexer U8 to select U7, a D flip flop register. This is accomplished by setting A13-11 to binary 100 when /PMS goes low. Such a sequence will cause U8, Pin 14 to go low, enabling data to pass through the D flip flops upon /WR going low and then high.

Data is written to the D10, D11 and D15 outputs of U7 (Pins 6, 9 and 19) known as POT CLK, POT LOAD EN, and POT IN. POT IN is serial data. POT LOAD EN is a serial load enable. During a load cycle, POT LOAD EN is held high. Seventeen POT IN values are set up and held with respect to the rising edges of POT CLK. The first value loaded into the dual programmable potentiometer is a "don't care" value. The following sixteen values comprise two 8-bit wiper positions. Wiper 1 gets loaded before wiper 0. Loading is specified from MSB to LSB.

Two Wire Input Line Conditioning

Two wire line input comes from the Line input of the system board when it is in a two wire configuration. This audio is in contention with audio which is leaving the station on the same two wire pair. The DSP Board must cancel out the interfering

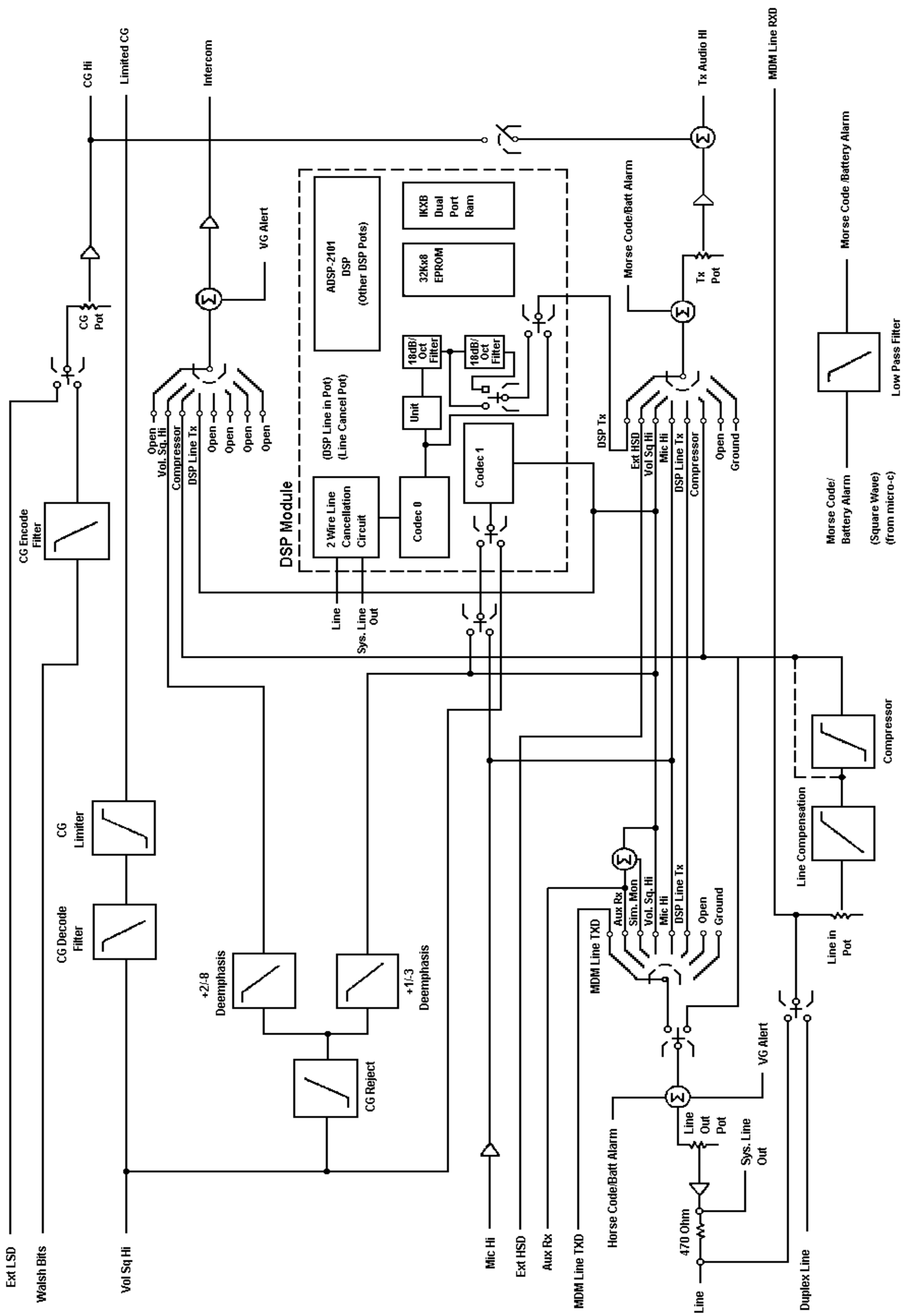


Figure 5 - Control Module Analog Section

output audio from the input. In addition, it must amplify the input signal to account for the line loss of up to 30 dB that can occur between the remote control unit and the station.

Cancellation of transmit audio from receive audio on the two wire pair is accomplished by differential instrumentation amplifier of U11 (A, B, C) and resistors R11-17 and the DSP-controlled resistance through U15(0) and R10. The SYSBD LINE OUT (a DSP Board input signal) is limited by U18A and level adjusted through the programmable potentiometer, U15(0), (as explained above) and then subtracted from the line input signal. The nulling signal line (TP1) is output to the back plane for convenience.

After subtraction, the remaining input (line audio) is level adjusted by the remaining programmable potentiometer U15(1) exactly as in the four wire case.

DSP Analog Outputs

The Rx output of codec U5, TX CODEC RX, passes through U16-B for pre-emphasis and hard limiting. Limiting action occurs when the instantaneous AC voltage exceeds the DC bias set by resistors R34, R36, and R37, at which point D1 becomes forward biased placing it in the feedback loop of U16-B. Due to the V-I characteristics of the diode, limiting action occurs. U16-B also provides +6 dB/oct pre-emphasis for transmitted audio in the 300 to 3000 Hz band. The pre-emphasis meets the EIA standard of +1/-3 gain flatness in the passband.

Following the pre-emphasis and the limiter, U16-C forms a third order low pass filter stage required by FCC regulations to filter the harmonics created by the preceding limiter. R35 and C29 compose a passive first order low pass filter while active filter U16-C provides an additional two poles for this filter stage. Following U16-C is another filter stage consisting of a second order passive low pass filter and a second order active low pass filter built around U16-D.

Analog switch U17 selects which filter stage output, if any, is routed to the transmitter. Depending upon the transmit frequency band, the FCC requires different filter characteristics for the post limiter filter. The output of analog switch U17-B DSP TX AUD is routed to P2-7 where it connects to the System Board.

The Rx output of U4 pin 2 DSP LINE/TX AUD is routed to P2-8 where it connects to the System board. This audio output typically dives the line out circuits on the system board.

Parallel Communications Hardware

The DSP Board is equipped with a full duplex parallel interface for communications between the system board microprocessor and the DSP microprocessor chip. Communications are accomplished through the dual port RAM, U12.

Byte wide messages are passed between system board and DSP chip by reading and writing data upon this common piece of memory.

The external eight bit system microprocessor can read and write to the dual port RAM. Address latch U13 (74HC373) is used by the 8 bit host to latch the address (AD7-AD0). The host uses its ALE signal to perform the actual clocking into the latch.

Once ALE has returned to logic one, AD7-AD0 become bi-directional data pins. During a "write" cycle, the host sets up data on AD7-AD0. During a "read" cycle, the system board microprocessor releases the data lines AD7-AD0 into their high impedance state.

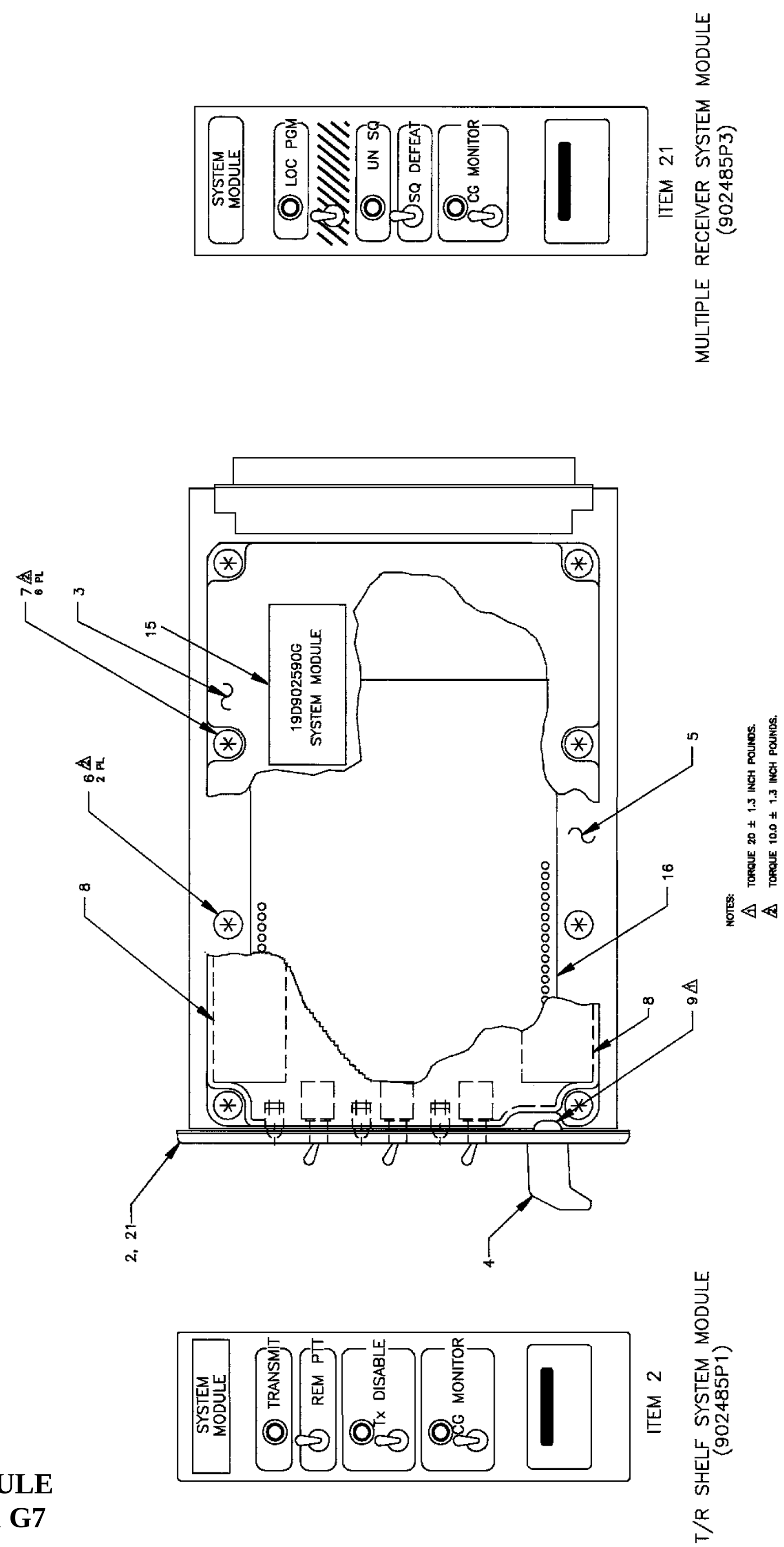
Finally, the System Board low-going /UPRD or /UPWR pulse executes the desired read/write function. Note that reading and writing are only accomplished when the DSP CS signal is held low. In this way, the system board microprocessor exclusively selects the dual port memory space to prevent contention upon the multiplexed address and data bus.

The DSP chip reads and writes from the dual port RAM by first selecting its communication memory space. This is accomplished by setting A13-11 to binary 010 when PMS goes low. Such a sequence will cause U8, Pin 13 to go low and thus enable dual port RAM, U12. Once enabled, the communications memory is accessed with address lines A9-A0 and data lines D15-D8, in conjunction with a low-going /RD and /WR pulse.

The DSP chip (U1) and host processor coordinate message handling through the RBLE and TBLF flags. The DSP chip sets TBLF by writing to location 3FFH of the dual port RAM.

Similarly, the host microprocessor can clear TBLF by reading from location 3FFH of the dual port RAM. It then sets RBLE by writing to location 3FEH of the dual port RAM. (Note that the flag is set when it is low; it is clear when it is high.) This way, both the microprocessors can monitor flag conditions in order to keep from trying to access the same locations in memory at the same time.

Tri-state buffer U9 is used by the DSP microprocessor in order to read the RBLE and TBLF flags. This alleviates the possibility of contention on the DSP data bus D15-D8. The RBLE and TBLF flags are read by first selecting U9. This is accomplished by setting A13-A11 to binary 100 when /PMS goes low. Such a sequence will cause U8 pin 14 to go low and thus enable data to pass through the tri-state buffer upon /RD going low. U9, Pins 2 and 3 appear on D8 and D9, and are latched into U1 when /RD returns high.



SYSTEM MODULE
19D902590G6 & G7

(19D902590, Rev. 4A)

SYSTEM MODULE

19D902590G7 - M III System Module with DSP
(Used in Multiple Receiver Applications)
19D902590G6 - M III System Module with DSP

SYMBOL	PART NO.	DESCRIPTION
2	19D902485P1	Chassis
3	19D902486P1	Cover
4	19D902555P1	Handle.
5	188D5498G1	System Board
6	19A702381P506	Screw, thread forming: TORX, No. M3.5-.6 x 6.
7	19A702381P513	Screw, thread forming: TORX, No. M3.5 - 0.6 X 13.
8	19B232682P20	Pad.
9	19A702381P508	Screw, thd. form: No. 3.5-0.6 x 8.
10	188D5682G1	DSP Board
12	19A701431P1	Silicon Compound
15	19B235310P1	Nameplate.
21	19D902485P3	Casting, System Module Auxiliary Receiver
		SYSTEM BOARD 188D5498 G1 - G2
		---------- CAPACITORS ---------
C1	19A702052P5	Ceramic: 1000 pF + or -10%, 50 VDCW.
C2	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C3	19A702061P13	Ceramic: 10 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C4	19A702052P5	Ceramic: 1000 pF + or -10%, 50 VDCW.
C5	19A702052P33	Ceramic: 0.1 uF + or -10%, 50 VDCW.
C6 and C7	19A702052P114	Ceramic: 0.01 uF + or - 5%, 50 VDCW.
C8	19A705205P5	Tantalum: 6.8 uF, 10 VDCW; sim to Sprague 293D.
C9	19A702052P28	Ceramic: 0.022 uF + or -10%, 50 VDCW.
C10 and C11	19A702052P114	Ceramic: 0.01 uF + or - 5%, 50 VDCW.
C12	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C13	19A705205P2	Tantalum: 1 uF, 16 VDCW; sim to Sprague 293D.
C14	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C15	19A702052P124	Ceramic: 0.068 uF + or - 5%, 50 VDCW.
C16	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C17	19A705205P5	Tantalum: 6.8 uF, 10 VDCW; sim to Sprague 293D.
C18	19A702052P24	Ceramic: 0.068 uF + or - 10%, 50 VDCW.
C19	19A702052P5	Ceramic: 1000 pF + or -10%, 50 VDCW.
C21	19A702061P77	Ceramic: 470 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C22	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C27 and C28	19A705205P111	Tantalum: 47 + or -10%, 10 VDCW; sim to Sprague 293D.
C29 thru C36	19A702052P5	Ceramic: 1000 pF + or -10%, 50 VDCW.
C38	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C39	19A705205P5	Tantalum: 6.8 uF, 10 VDCW; sim to Sprague 293D.
C40	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C42 thru C45	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C46	344A3431P1	Monolithic: 1.0 uF +80/-20%, 16 VDCW.
C47 thru C50	19A702052P114	Ceramic: 0.01 uF + or - 5%, 50 VDCW.
C51	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C52	19A702061P37	Ceramic: 33 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C.
C53	19A702061P45	Ceramic: 47 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C58	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C59 and C60	19A702052P122	Ceramic: 0.047 uF + or - 5%, 50 VDCW.
C61	19A702052P26	Ceramic: 0.1uF + or - 10%, 50 VDCW
C62 thru C67	19A149791P1	Metalized Polyprolyene: 0.022 uH + or - 1%, 100 VDCW.
C68 thru C71	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C72 and C73	19A702052P5	Ceramic: 1000 pF + or -10%, 50 VDCW.
C74 thru C79	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C80 thru C84	19A702052P5	Ceramic: 1000 pF + or -10%, 50 VDCW.
C87 thru C95	19A702052P5	Ceramic: 1000 pF + or -10%, 50 VDCW.
C96 and C97	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C98 and C99	19A702052P5	Ceramic: 1000 pF + or -10%, 50 VDCW.
C100 and C101	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C102	19A702052P5	Ceramic: 1000 pF + or -10%, 50 VDCW.
C103	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C104	19A705205P111	Tantalum: 47 + or -10%, 10 VDCW; sim to Sprague 293D.
C105 thru C108	19A702052P5	Ceramic: 1000 pF + or -10%, 50 VDCW.
C109 and C110	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C111	19A702052P114	Ceramic: 0.01 uF + or - 5%, 50 VDCW.
C112	19A702061P77	Ceramic: 470 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C113	19A702052P114	Ceramic: 0.01 uF + or - 5%, 50 VDCW.
C114 and C115	19A702236P17	Ceramic: 4.7 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
C116	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
		----------- DIODES ----------
D1 thru D5	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99.
D7	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99.
D8 and D9	19A702525P2	Silicon, PIN: sim to MMBV3401.
D10	19A705377P4	Silicon, Hot Carrier: sim to HSMS-2802.
D11	19A702525P2	Silicon, PIN: sim to MMBV3401.
		-------- INDICATING DEVICES -------
DS1 thru DS3	19A703595P10	Optoelectic: Red LED; sim to HP HLMP-1301-010.
		----------- JACKS -----------

SYMBOL	PART NO.	DESCRIPTION
J1	19B801587P7	Connector, DIN: 96 male contacts, right angle to AMP 650887-1.
J2 and J3	19A704852P334	Connector, printed wire board.
		- - - - - - - - - - INDUCTORS - - - - - - - - - -
L1 and L2	19A705470P53	Coil, fixed.
		- - - - - - - - - - TRANSISTORS - - - - - - - - -
Q2	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q4 and Q5	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q6	344A3855P1	Silicon, NPN.
Q7	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q8	19A700059P2	Silicon, PNP: sim to MMBT3906, low profile.
Q9 thru Q13	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R2	19B800607P473	Metal film: 47K ohms + or -5%, 1/8 w.
R3	19A702931P301	Metal film: 10K ohms + or -1%, 200 VDCW, 1/8 w.
R4	19B800607P153	Metal film: 15K ohms + or -5%, 1/8 w.
R5	19B800607P332	Metal film: 3.3K ohms + or -5%, 1/8 w.
R6	19A702931P301	Metal film: 10K ohms + or -1%, 200 VDCW, 1/8 w.
R7	19A702931P249	Metal film: 3160 ohms + or -1%, 200 VDCW, 1/8 w.
R8	19A702931P313	Metal film: 13.3K ohms + or -1%, 200 VDCW, 1/8 w.
R9	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R10	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R11	19B800607P562	Metal film: 5.6K ohms + or -5%, 1/8 w.
R12	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R13	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.
R14	19B800607P272	Metal film: 2.7K ohms + or -5%, 1/8 w.
R15	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R16	19B800607P1	Metal film: Jumper.
R17	19A702931P369	Metal film: 51.1K ohms + or -1%, 200 VDCW, 1/8 w.
R18	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R19	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R20	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R21	19B800607P223	Metal film: 22K ohms + or -5%, 1/8 w.
R22	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R23	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R24	19B800607P122	Metal film: 1.2K ohms + or -5%, 1/8 w.
R25	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R26	19A702931P384	Metal film: 73.2K ohms + or -1%, 200 VDCW, 1/8 w.
R27	19A702931P388	Metal film: 80.6K ohms + or -1%, 200 VDCW, 1/8 w/
R28	19A702931P358	Metal film: 39.2K ohms + or -1%, 200 VDCW, 1/8 w.
R29	19A702931P383	Metal film: 71.5K ohms + or -1%, 200 VDCW, 1/8 w.
R30	19A702931P384	Metal film: 73.2K ohms + or -1%, 200 VDCW, 1/8 w.
R31	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R32	19A702931P369	Metal film: 51.1K ohms + or -1%, 200 VDCW, 1/8 w.
R33	19A702931P325	Metal film: 17.8K ohms + or -1%, 200 VDCW, 1/8 w.
R34	19A702931P350	Metal film: 32.4K ohms + or -1%, 200 VDCW, 1/8 w.
R35	19A702931P383	Metal film: 71.5K ohms + or -1%, 200 VDCW, 1/8 w.
R36	19A702931P382	Metal film: 69.8K ohms + or -1%, 200 VDCW, 1/8 w.
R37	19A702931P383	Metal film: 71.5K ohms + or -1%, 200 VDCW, 1/8 w.
R39	19A702931P401	Metal film: 100K ohms + or -1%, 1/8 w.
R40	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.

SYMBOL	PART NO.	DESCRIPTION
R41	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R42	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R43	19B800607P684	Metal film: 680K ohms + or -5%, 1/8 w.
R44	19B800607P473	Metal film: 47K ohms + or -5%, 1/8 w.
R45	19B800607P683	Metal film: 68K ohms + or -5%, 1/8 w.
R46	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R47 and R48	19B800607P681	Metal film: 680 ohms + or -5%, 1/8 w.
R49	19A702931P301	Metal film: 10K ohms + or -1%, 200 VDCW, 1/8 w.
R50	19A702931P388	Metal film: 80.6K ohms + or -1%, 200 VDCW, 1/8 w.
R51 thru R53	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.
R54	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R55 and R56	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.
R57 and R58	19B800607P1	Metal film: Jumper.
R59	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R60	19B800607P471	Metal film: 470 ohms + or -5%, 1/8 w.
R61	19A702931P413	Metal film: 133K ohms + or -1%, 200 VDCW, 1/8 w.
R62	19A702931P327	Metal film: 18.7K ohms + or -1%, 200 VDCW, 1/8 w.
R63	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R64	19A702931P177	Metal film: 619 ohms + or -1%, 200 VDCW, 1/8 w.
R65	19B800607P682	Metal film: 6.8K ohms + or -5%, 1/8 w.
R66	19A702931P243	Metal film: 2740 ohms + or -1%, 200 VDCW, 1/8 w.
R67	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R68	19B800607P153	Metal film: 15K ohms + or -5%, 1/8 w.
R69	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R70	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R78	19A702931P222	Metal film: 1650 ohms + or -1%, 200 VDCW, 1/8 w.
R80 and R81	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R82	19B800607P562	Metal film: 5.6K ohms + or -5%, 1/8 w.
R83	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R84	19A702931P389	Metal film: 82.5K ohms + or -1%, 200 VDCW, 1/8 w.
R85	19A702931P434	Metal film: 221K ohms + or -1%, 200 VDCW, 1/8 w.
R86	19A702931P383	Metal film: 71.5K ohms + or -1%, 200 VDCW, 1/8 w.
R87	19B800607P105	Metal film: 1M ohms + or -5%, 1/8 w.
R88	19A702931P305	Metal film: 11K ohms + or -1%, 200 VDCW, 1/8 w.
R89	19B800607P1	Metal film: Jumper.
R90	19A702931P358	Metal film: 39.2K ohms + or -1%, 200 VDCW, 1/8 w.
R91	19A702931P383	Metal film: 71.5K ohms + or -1%, 200 VDCW, 1/8 w.
R92	19A702931P384	Metal film: 73.2K ohms + or -1%, 200 VDCW, 1/8 w.
R93	19A702931P383	Metal film: 71.5K ohms + or -1%, 200 VDCW, 1/8 w.
R94	19A702931P388	Metal film: 80.6K ohms + or -1%, 200 VDCW, 1/8 w.
R95	19A702931P325	Metal film: 17.8K ohms + or -1%, 200 VDCW, 1/8 w.
R96	19A702931P383	Metal film: 71.5K ohms + or -1%, 200 VDCW, 1/8 w.
R97	19A702931P382	Metal film: 69.8K ohms + or -1%, 200 VDCW, 1/8 w.
R98	19A702931P383	Metal film: 71.5K ohms + or -1%, 200 VDCW, 1/8 w.
R99	19A702931P350	Metal film: 32.4K ohms + or -1%, 200 VDCW, 1/8 w.
R100	19B800607P471	Metal film: 470 ohms + or -5%, 1/8 w.
R101	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R102	19B800607P563	Metal film: 56K ohms + or -5%, 1/8 w.
R103	19B800607P123	Metal film: 12K ohms + or -5%, 1/8 w.
R104 and R105	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.

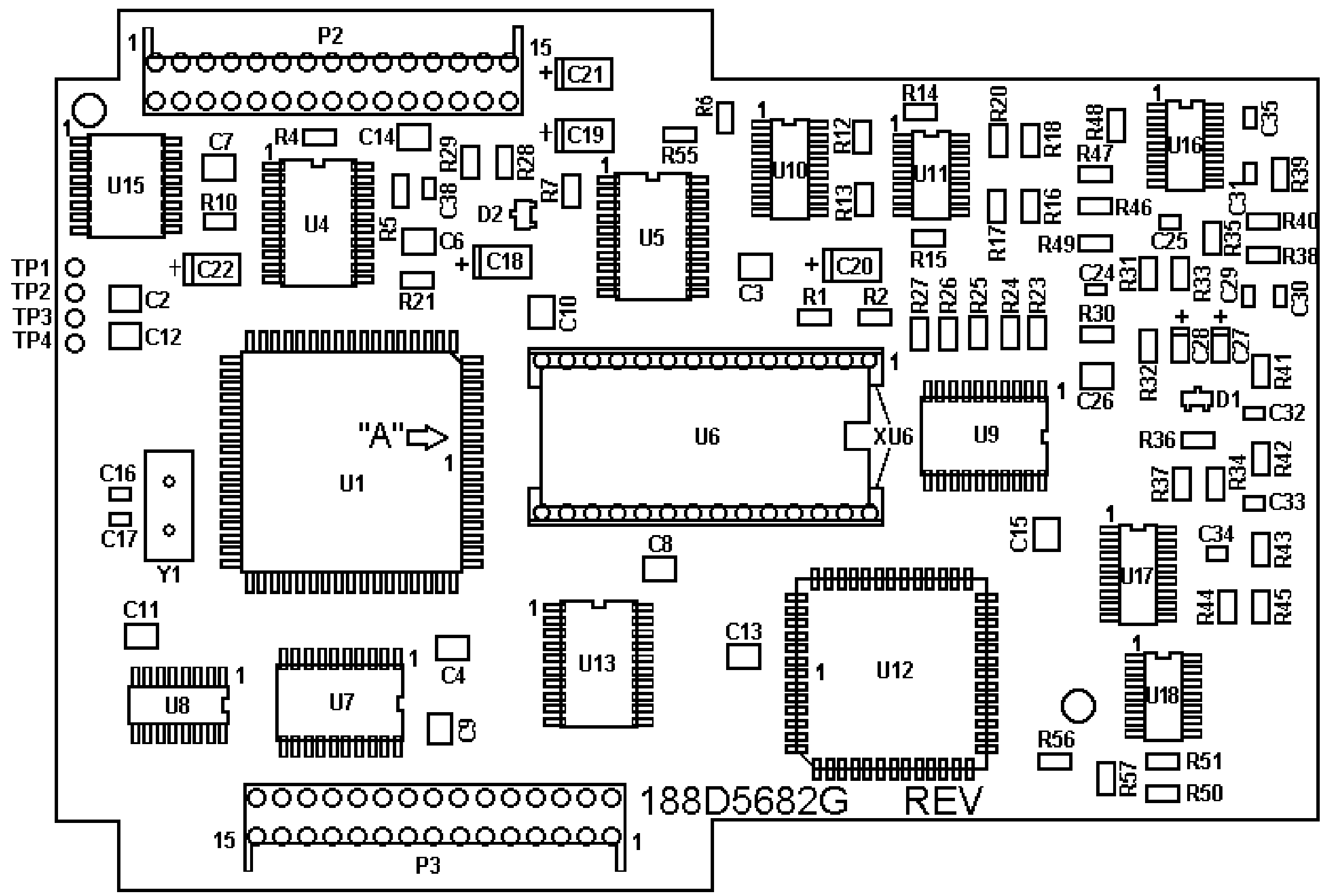
SYMBOL	PART NO.	DESCRIPTION
R106	19A702931P355	Metal film: 36.5K ohms + or -1%, 200 VDCW, 1/8 w.
R107	19A702931P285	Metal film: 7500 ohms + or -1%, 1/8 w.
R108	19A702931P177	Metal film: 619 ohms + or -1%, 200 VDCW, 1/8 w.
R109	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R110	19B800607P105	Metal film: 1M ohms + or -5%, 1/8 w.
R111	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R112 and R113	19A702931P401	Metal film: 100K ohms + or -1%, 1/8 w.
R114	19A702931P383	Metal film: 71.5K ohms + or -1%, 200 VDCW, 1/8 w.
R115 and R116	19B800607P391	Metal film: 390 ohms + or -5%, 1/8 w.
R117	19A702931P385	Metal film: 75K ohms + or -1%, 200 VDCW, 1/8 w.
R120	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R121	19A702931P342	Metal film: 26.7K ohms + or -1%, 200 VDCW, 1/8 w.
R122	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R124	19A702931P325	Metal film: 17.8K ohms + or -1%, 200 VDCW, 1/8 w.
R125	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R126	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.
R127	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R128 and R129	19A702931P222	Metal film: 1650 ohms + or -1%, 200 VDCW, 1/8 w.
R130	19A702931P422	Metal film: 165K ohms + or -1%, 200 VDCW, 1/8 w.
R132	19B800607P332	Metal film: 3.3K ohms + or -5%, 1/8 w.
R133 and R134	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R135	19A702931P313	Metal film: 13.3K ohms + or -1%, 200 VDCW, 1/8 w.
R136 and R137	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R138	19A702931P285	Metal film: 7500 ohms + or -1%, 1/8 w.
R139	19A702931P389	Metal film: 82.5K ohms + or -1%, 200 VDCW, 1/8 w.
R140	19B800607P224	Metal film: 220K ohms + or -5%, 1/8 w.
R141	19A702931P269	Metal film: 5110 ohms + or -1%, 1/8 w.
R142	19B800607P474	Metal film: 470K ohms + or -5%, 1/8 w.
R143	19A702931P436	Metal film: 232K ohms + or -1%, 200 VDCW, 1/8 w.
R144	19A702931P243	Metal film: 2740 ohms + or -1%, 200 VDCW, 1/8 w.
R145	19B800607P224	Metal film: 220K ohms + or -5%, 1/8 w.
R146	19B800607P474	Metal film: 470K ohms + or -5%, 1/8 w.
R147	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R148	19B800607P153	Metal film: 15K ohms + or -5%, 1/8 w.
R149 thru R151	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R152	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R153	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R155	19A702931P434	Metal film: 221K ohms + or -1%, 200 VDCW, 1/8 w.
R156	19A702931P406	Metal film: 113K ohms + or -1%, 200 VDCW, 1/8 w.
R157	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.
R158	19A702931P383	Metal film: 71.5K ohms + or -1%, 200 VDCW, 1/8 w.
R159	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.
R160	19A702931P177	Metal film: 619 ohms + or -1%, 200 VDCW, 1/8 w.
R161	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R162	19B800607P474	Metal film: 470K ohms + or -5%, 1/8 w.
R163	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R164	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.
R165	19B800607P682	Metal film: 6.8K ohms + or -5%, 1/8 w.
R166	19A702931P355	Metal film: 36.5K ohms + or -1%, 200 VDCW, 1/8 w.
R167	19A702931P325	Metal film: 17.8K ohms + or -1%, 200 VDCW, 1/8 w.

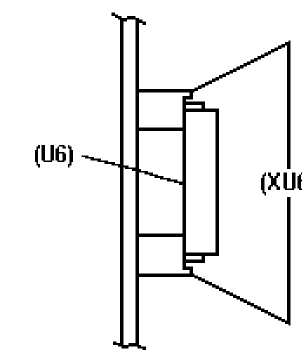
SYMBOL	PART NO.	DESCRIPTION
R168	19A702931P305	Metal film: 11K ohms + or -1%, 200 VDCW, 1/8 w.
R169	19A702931P393	Metal film: 90.9K ohms + or -1%, 200 VDCW, 1/8 w.
R170 and R171	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.
R172 and R173	19B800607P474	Metal film: 470K ohms + or -5%, 1/8 w.
R174	19A702931P313	Metal film: 13.3K ohms + or -1%, 200 VDCW, 1/8 w.
R175	19B800607P333	Metal film: 33K ohms + or -5%, 1/8 w.
R176	19A702931P222	Metal film: 1650 ohms + or -1%, 200 VDCW, 1/8 w.
R177	19A702931P269	Metal film: 5110 ohms + or -1%, 1/8 w.
R178	19B800607P474	Metal film: 470K ohms + or -5%, 1/8 w.
R179	19A702931P385	Metal film: 75K ohms + or -1%, 200 VDCW, 1/8 w.
R180	19A702931P413	Metal film: 133K ohms + or -1%, 200 VDCW, 1/8 w.
R181	19A702931P130	Metal film: 200 ohms + or -1%, 200 VDCW, 1/8 w.
R183	19B800607P183	Metal film: 18K ohms + or -5%, 1/8 w.
R185	19B800607P473	Metal film: 47K ohms + or -5%, 1/8 w.
R186	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.
R187	19B800607P473	Metal film: 47K ohms + or -5%, 1/8 w.
R188	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R189	19B800607P1	Metal film: 0 ohms + or -5%, 1/8 w.
R190	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R193	19B800607P561	Metal film: 560K ohms + or -5%, 1/8 w.
		- - - - - - - - - - - SWITCHES - - - - - - - - -
S2 thru S4	19A705959P3	Toggle, SPDT: right-angle mount; sim to C&K T101-M-H9-A-B-E.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - -
U1	19A705982P101	Microcomputer: 8-bit extended I/O; sim to INTEL 80C152JB-1.
U2	19A703471P302	Digital: Octal Data Latch; sim to 74HC373.
U3	19A703471P320	Digital: 3-Line To 8-Line Decoder; sim to 74HC138.
U4	344A3307G17	EPROM KIT.
U5	19A705603P6	Digital: 8K X8 bit Static CMOS SRAM; sim to K M6264AL-10.
U6	19A703952P102	EEPROM: 2K X 8, 5 Volts, programmable; sim to XICOR X2816CP-20.
U7	19A704380P319	Digital: CMOS Octal Data Flip-Flop; sim to 74HC377.
U8	19A702705P5	Digital: Triple 2-Channel Analog Multiplexer; sim to 4053BM.
U9	344A3070P3	Digital: JFET, Input quad Op Amp; sim to TL074.
U10	19A704883P2	Digital: Quad Op Amp; sim to MC3303D.
U11	19A116297P7	Linear: Dual Op Amp; sim to MC4558CD.
U12	19A702705P5	Digital: Triple 2-Channel Analog Multiplexer; sim to 4053BM.
U13	19A704883P2	Digital: Quad Op Amp; sim to MC3303D.
U14	19A702705P3	Digital: 8-Channel Analog Multiplexer; sim to 4051BM.
U15	344A3856P101	Analog: 8-Channel Single Ended Multiplexer; sim to SILICONIX DG408/409.
U16 and U17	19A704883P2	Digital: Quad Op Amp; sim to MC3303D.
U18	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U19	19A149895P1	Digital: Microprocessor Supervisory; sim to MAX 691C.
U20	19A116180P575	Digital: Hex Open Collector Inverter: sim to 7406.
U21	19A703995P3	Digital: High speed logic, hex inverter, unbuffered; sim to 74HCU0-4.
U22	344A3039P201	Digital: Driver/receiver, EIA-232D/V.28; sim to MC145406.
U24	19A705980P101	Tranxceiver, differential Bus; sim to SN751768.

SYMBOL	PART NO.	DESCRIPTION
U25	19A703471P316	Digital: Driver/receiver, octal 3-state non inverting buffer; sim
U26	19A116180P575	Digital: Hex Open Collector Inverter: sim to 7406.
U27	19A705979P101	Digital: CMOS A/D; sim to TL549CP.
U28	19A704380P302	Digital: CMOS Dual Data Flip-Flop; sim to 74HC74.
U29	19A149466P301	Digital: CH MOS, Programmable Timer; sim to Intel 82C54.
U30	19A704883P2	Digital: Quad Op Amp; sim to MC3303D.
U31	344A3070P3	Digital: JFET, Input quad Op Amp; sim to TL074.
U32 and U33	19A702705P3	Digital: 8-Channel Analog Multiplexer; sim to 4051BM.
U34	19A705991P101	Digital: Programmable interface; sim to Harris C82C55A.
U35 and U36	344A3041P201	Digital: dual in-line potentiometers, ceramic, to DS1267S-10.
U37	19A704883P2	Digital: Quad Op Amp; sim to MC3303D.
U40	19A116180P575	Digital: Hex Open Collector Inverter: sim to 7406.
U41	19A700176P101	Digital: Hex Inverting Buffer/Converter; sim to 4049UBD.
		- - - - - - - - - - - SOCKETS - - - - - - - - - -
XU4	19A705840P2	Socket: sim to Amp 643646-3.
		- - - - - - - - - - - CRYSTALS - - - - - - - - -
Y1	19A702511G37	Crystal, 14.7456 MHz.
		DSP BOARD 188D5682 G1
		- - - - - - - - - - CAPACITORS - - - - - - - - -
C2 thru C4	19A702052P26	Ceramic: 0.1uF + or - 10%, 50 VDCW
C6 thru C15	19A702052P26	Ceramic: 0.1uF + or - 10%, 50 VDCW
C16 and C17	19A702061P29	Ceramic: 22 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C18 thru C22	19A705205P6	Tantalum: 10 uF, 16 VDCW; sim to Sprague 293D.
C24	19A702052P107	Ceramic: 2200 pF + or - 5%, 50 VDCW.
C25	19A702061P53	Ceramic: 68 pF + or - 5%, 50 VDCW, temp coef 0 + or - 30 PPM.
C26	19A702052P120	Ceramic: 0.033 uF + or - 5%, 50 VDCW.
C27 and C28	19A705205P19	Tantalum: 2.2 uF, 10 VDCW; sim to Spargue 293D.
C29	19A702052P134	Ceramic: 0.1 uF + or - 5%, 25 VDCW.
C30	19A702052P112	Ceramic: 6800 pF + or - 5%, 50 VDCW.
C31	19A702052P105	Ceramic: 1000 pF + or - 5%, 50 VDCW.
C32	19A702052P142	Ceramic: 0.082 uF + or - 5%, 16 VDCW.
C33 and C34	19A702052P112	Ceramic: 6800 pF + or - 5%, 50 VDCW.
C35	19A702052P105	Ceramic: 1000 pF + or - 5%, 50 VDCW.
C38	19A702061P45	Ceramic: 47 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM.
		- - - - - - - - - - - DIODES - - - - - - - - - -
D1	19A700053P2	Silicon: 2 Diodes in Series; sim to BAV99.
D2	19A705377P4	Silicon, Hot Carrier: sim to HSMS-2802.
		- - - - - - - - - - - PLUGS - - - - - - - - - - -
P2 and P3	19A704779P14	Connector, 15 pin.

SYMBOL	PART NO.	DESCRIPTION
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R2	19B800607P1	Metal film: Jumper.
R4	19B800607P1	Metal film: Jumper.
R5 and R6	19B800607P683	Metal film: 68K ohms + or -5%, 1/8 w.
R7	19B800607P1	Metal film: Jumper.
R10	19B800607P682	Metal film: 6.8K ohms + or -5%, 1/8 w.
R12 and R13	19B800607P1	Metal film: Jumper.
R14 and R15	19A702931P355	Metal film: 36.5K ohms + or -1%, 200 VDCW, 1/8 w.
R16	19A702931P318	Metal film: 15K ohms + or -1%, 200 VDCW, 1/8 w.
R17	19A702931P401	Metal film: 100K ohms + or -1%, 1/8 w.
R18	19B800607P201	Metal film: 200 ohms + or -5%, 1/8 w.
R20	19B800607P392	Metal film: 3.9K ohms + or -5%, 1/8 w.
R21	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R23 thru R27	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R28 and R29	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R30	19A702931P418	Metal film: 150K ohms + or -1%, 200 VDCW, 1/8 w.
R31	19A702931P318	Metal film: 15K ohms + or -1%, 200 VDCW, 1/8 w.
R32	19A702931P209	Metal film: 1210 ohms + or -1%, 200 VDCW, 1/8 w.
R33	19A702931P369	Metal film: 51.1K ohms + or -1%, 200 VDCW, 1/8 w.
R34	19A702931P331	Metal film: 20.5K ohms + or -1%, 200 VDCW, 1/8 w.
R35	19A702931P201	Metal film: 1000 ohms + or -1%, 200 VDCW, 1/8 w.
R36	19A702931P317	Metal film: 14.7K ohms + or -1%, 200 VDCW, 1/8 w.
R37	19A702931P331	Metal film: 20.5K ohms + or -1%, 200 VDCW, 1/8 w.
R38	19A702931P377	Metal film: 61.9K ohms + or -1%, 200 VDCW, 1/8 w.
R39	19A702931P307	Metal film: 11.5K ohms + or -1%, 200 VDCW, 1/8 w.
R40	19A702931P347	Metal film: 30.1K ohms + or -1%, 200 VDCW, 1/8 w.
R41 and R42	19A702931P157	Metal film: 383 ohms + or -1%, 200 VDCW, 1/8 w.
R43	19A702931P339	Metal film: 24.9K ohms + or -1%, 200 VDCW, 1/8 w.
R44	19A702931P347	Metal film: 30.1K ohms + or -1%, 200 VDCW, 1/8 w.
R45	19A702931P307	Metal film: 11.5K ohms + or -1%, 200 VDCW, 1/8 w.
R46	19A702931P294	Metal film: 9310 ohms + or -1%, 200 VDCW, 1/8 w.
R47	19A702931P265	Metal film: 4640 ohms + or -1%, 200 VDCW, 1/8 w.
R48	19A702931P294	Metal film: 9310 ohms + or -1%, 200 VDCW, 1/8 w.
R49 thru R51	19A702931P201	Metal film: 1000 ohms + or -1%, 200 VDCW, 1/8 w.
R55	19A702931P301	Metal film: 10K ohms + or -1%, 200 VDCW, 1/8 w.
R56	19A702931P339	Metal film: 24.9K ohms + or -1%, 200 VDCW, 1/8 w.
R57	19A702931P301	Metal film: 10K ohms + or -1%, 200 VDCW, 1/8 w.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - -
U1	344A3038P101	Digital: DSP microcomputer, oper freq. 40.96 ADSP210KX-40.
U4 and U5	19A705827P1	Encoder/Decoder: sim to Texas Instruments TCM29C23.
U6	344A3309G5	EPROM KIT
U7	344A3064P203	Digital: Octal Data Flip-Flop; sim to 74HCT377.
U8	344A3064P201	Digital: 3-To-8 Line Decoder/Demultiplexer; sim to 74HCT138.
U9	344A3064P204	Digital: Octal Buffer/Line Driver; sim to 74HCT541.
U10	19A702705P5	Digital: Triple 2-Channel Analog Multiplexer; sim to 4053BM.
U11	19A704883P2	Digital: Quad Op Amp; sim to MC3303D.

SYMBOL	PART NO.	DESCRIPTION
U12	344A3040P201	Digital: SRAM, 1K X 8 Dual port; sim to IDT7130SA100.
U13	344A3064P202	Digital: Octal Transparent Latch; sim to 74HCT373.
U15	344A3041P201	Digital: dual in-line potentiometers, ceramic, to DS1267S-10.
U16	344A3070P3	Digital: JFET, Input quad Op Amp; sim to TL074.
U17	19A702705P5	Digital: Triple 2-Channel Analog Multiplexer; sim to 4053BM.
U18	344A3070P3	Digital: JFET, Input quad Op Amp; sim to TL074.
		- - - - - - - - - - - SOCKETS - - - - - - - - - -
XU6	19A705840P2	Socket: sim to Amp 643646-3.
		- - - - - - - - - - - CRYSTALS - - - - - - - - -
Y1	19A702511G30	Crystal, quartz: 8.192 MHz.





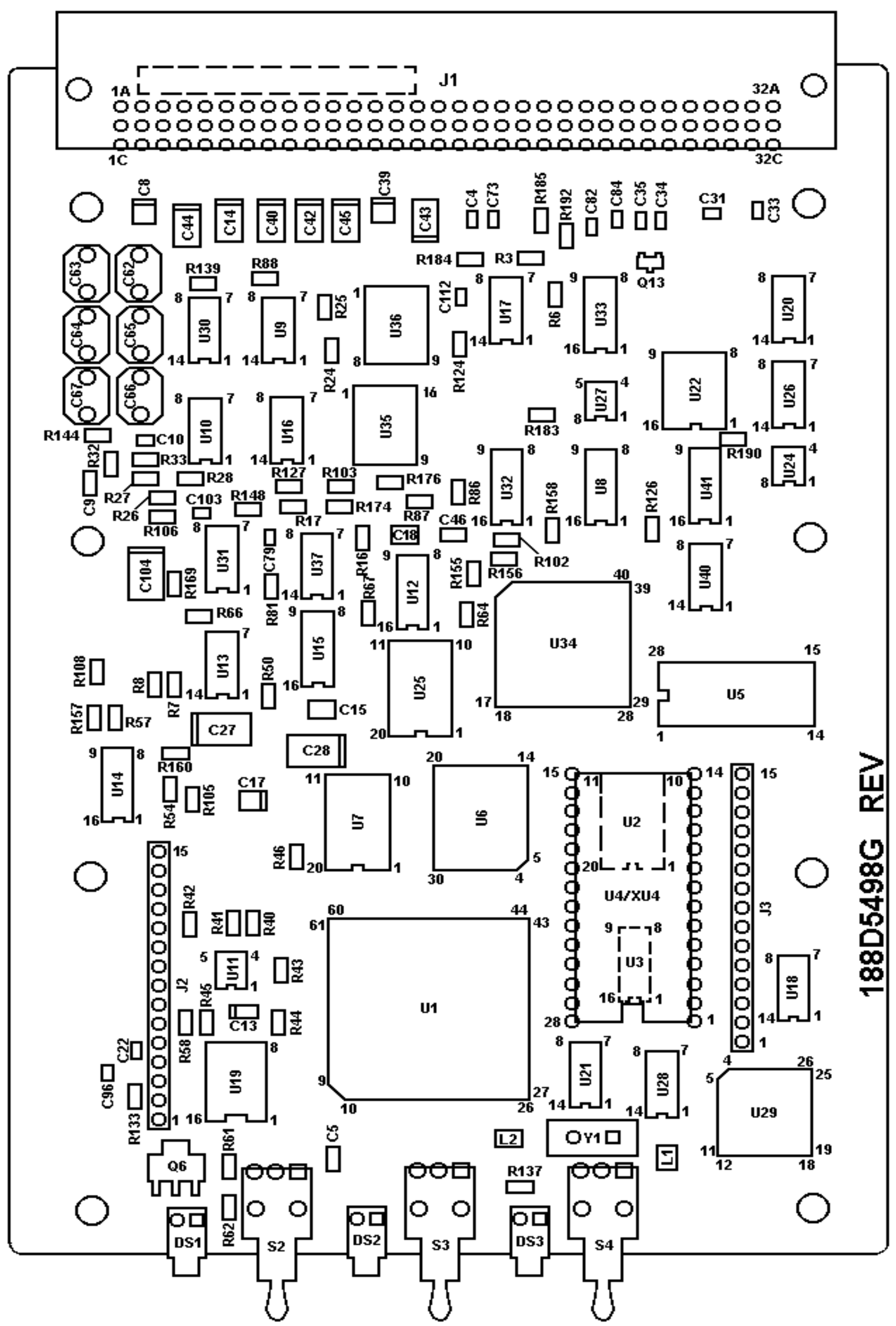
VIEW AT "A"
ORIENTATION OF XU6

CAUTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES

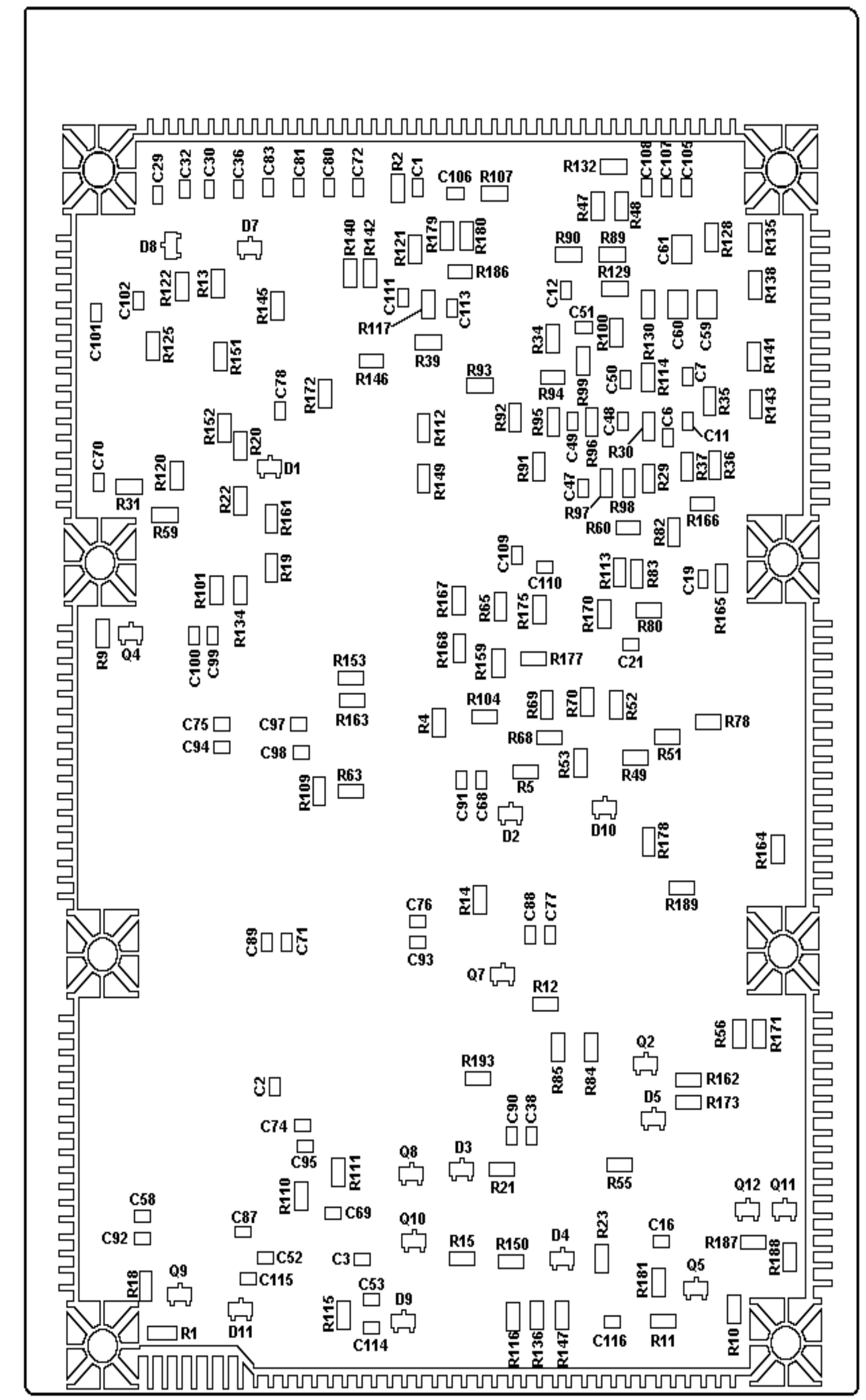
DSP BOARD
188D5682G1

(188D5682, Rev. 5)

COMPONENT SIDE



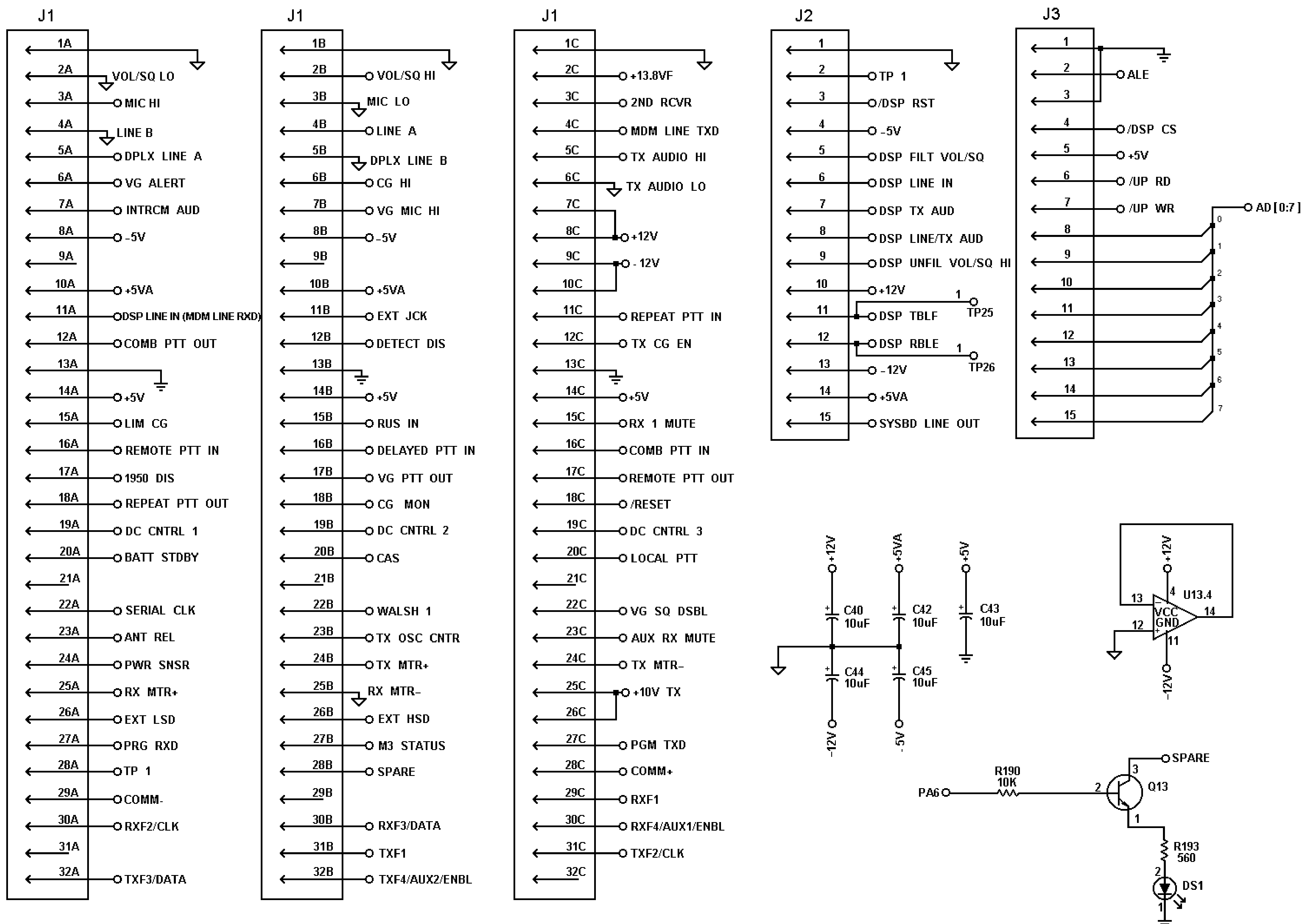
SOLDER SIDE



SYSTEM BOARD
188D5498G1

(188D5498, Rev. 2))

CAUTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

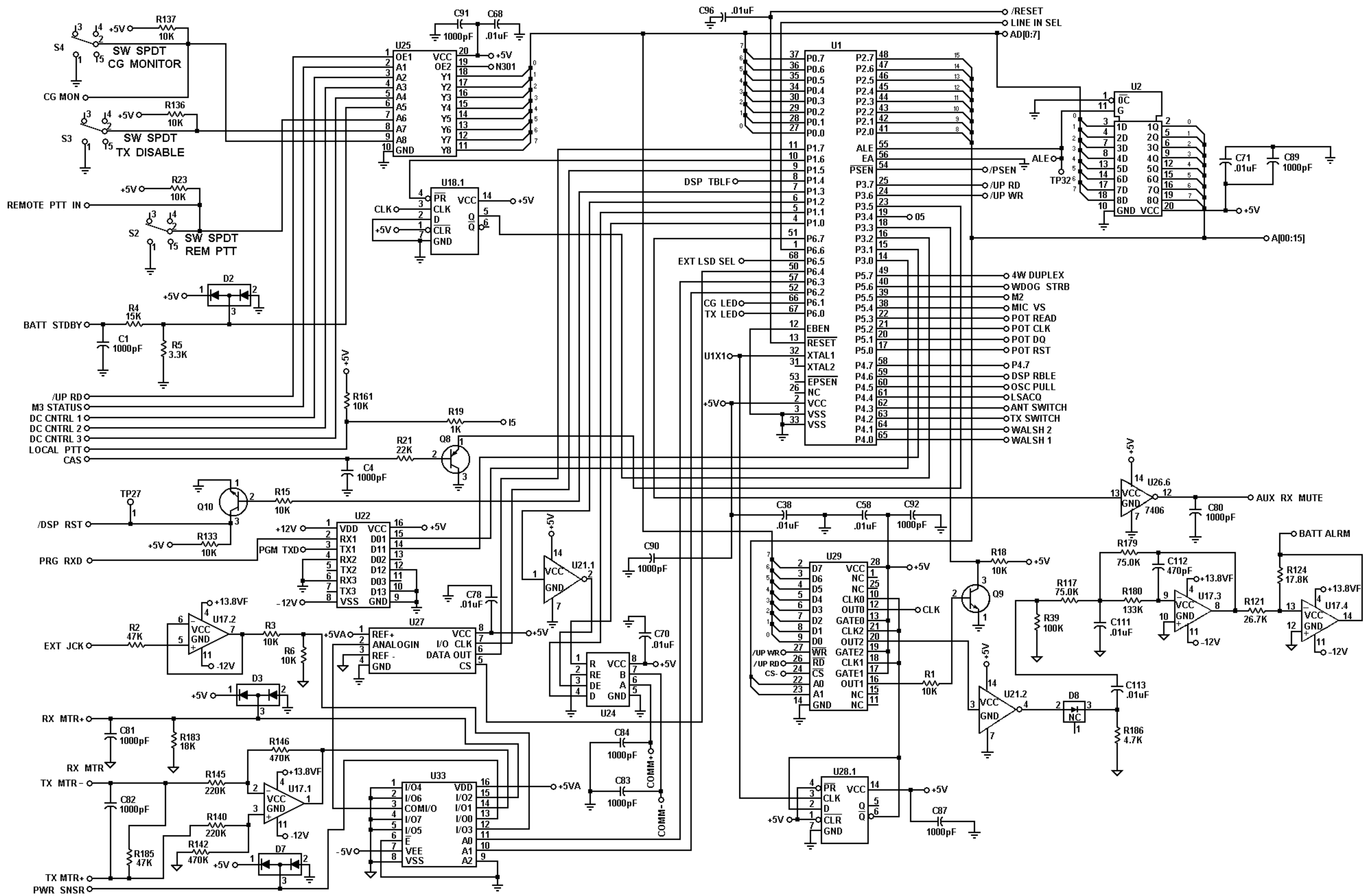


THIS SCHEMATIC DIAG APPLIES TO
MODEL NO. REV LETTER
PL188D5498G1

ALL RESISTORS ARE 1/8 WATT UNLESS OTHERWISE SPECIFIED AND RESISTORS VALUES ARE IN OHMS UNLESS FOLLOWED BY MULTIPLIER K OR M. CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER U, N OR P. INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER M OR U.

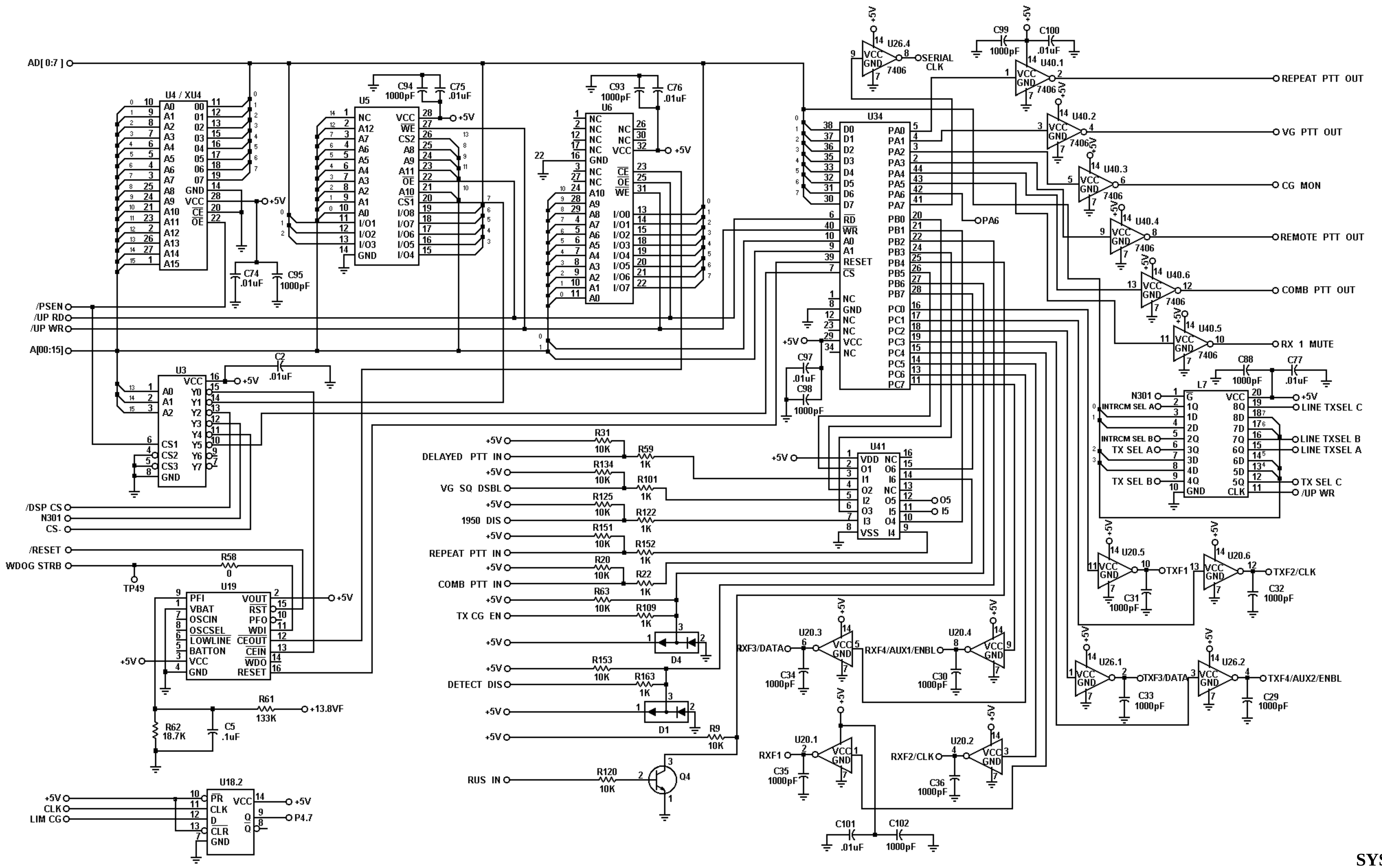
SYSTEM BOARD
188D5498G1

(188D5496, Sh. 1, Rev. 2)



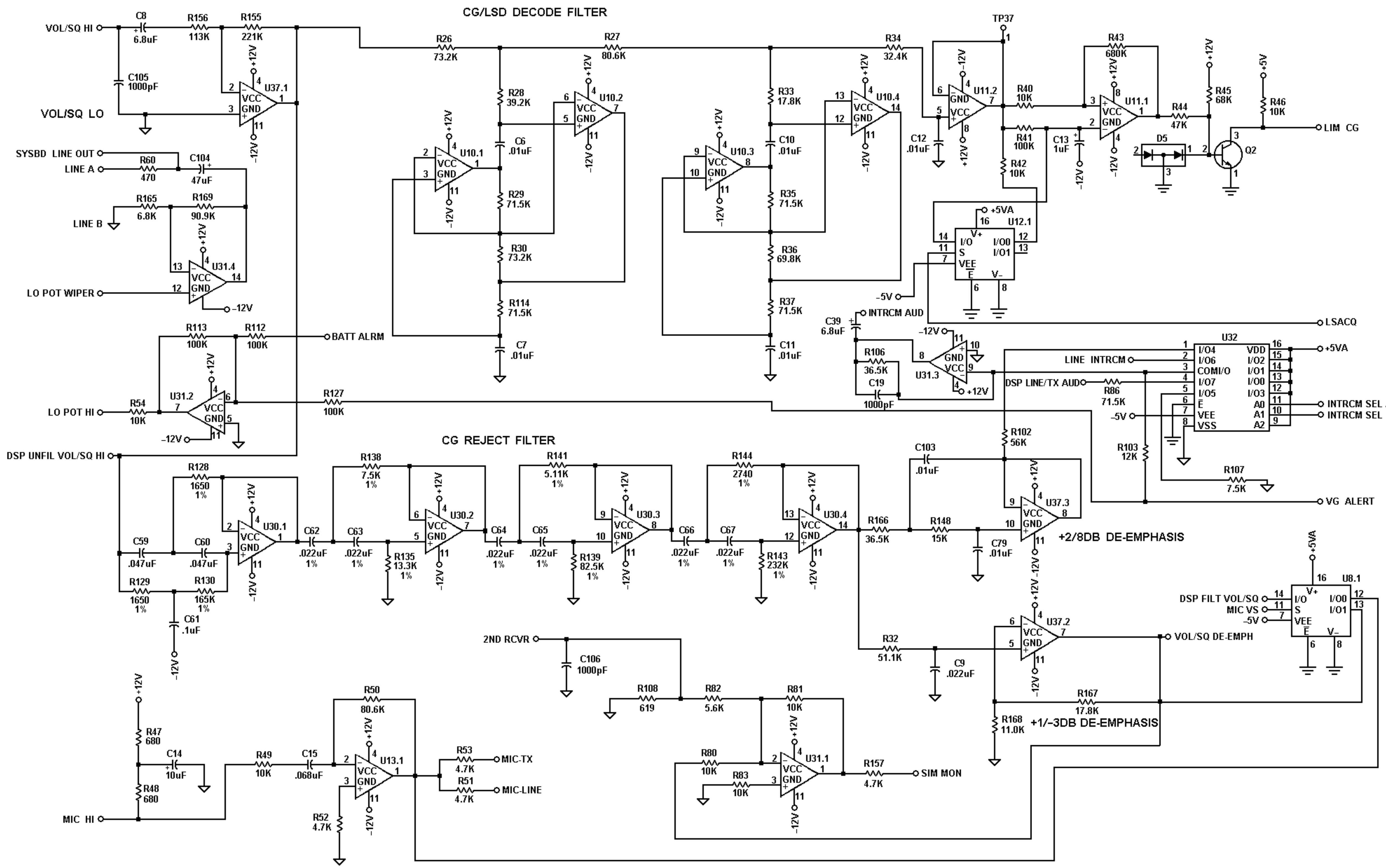
SYSTEM BOARD
188D5498G1

(188D5496, Sh. 2, Rev. 2)



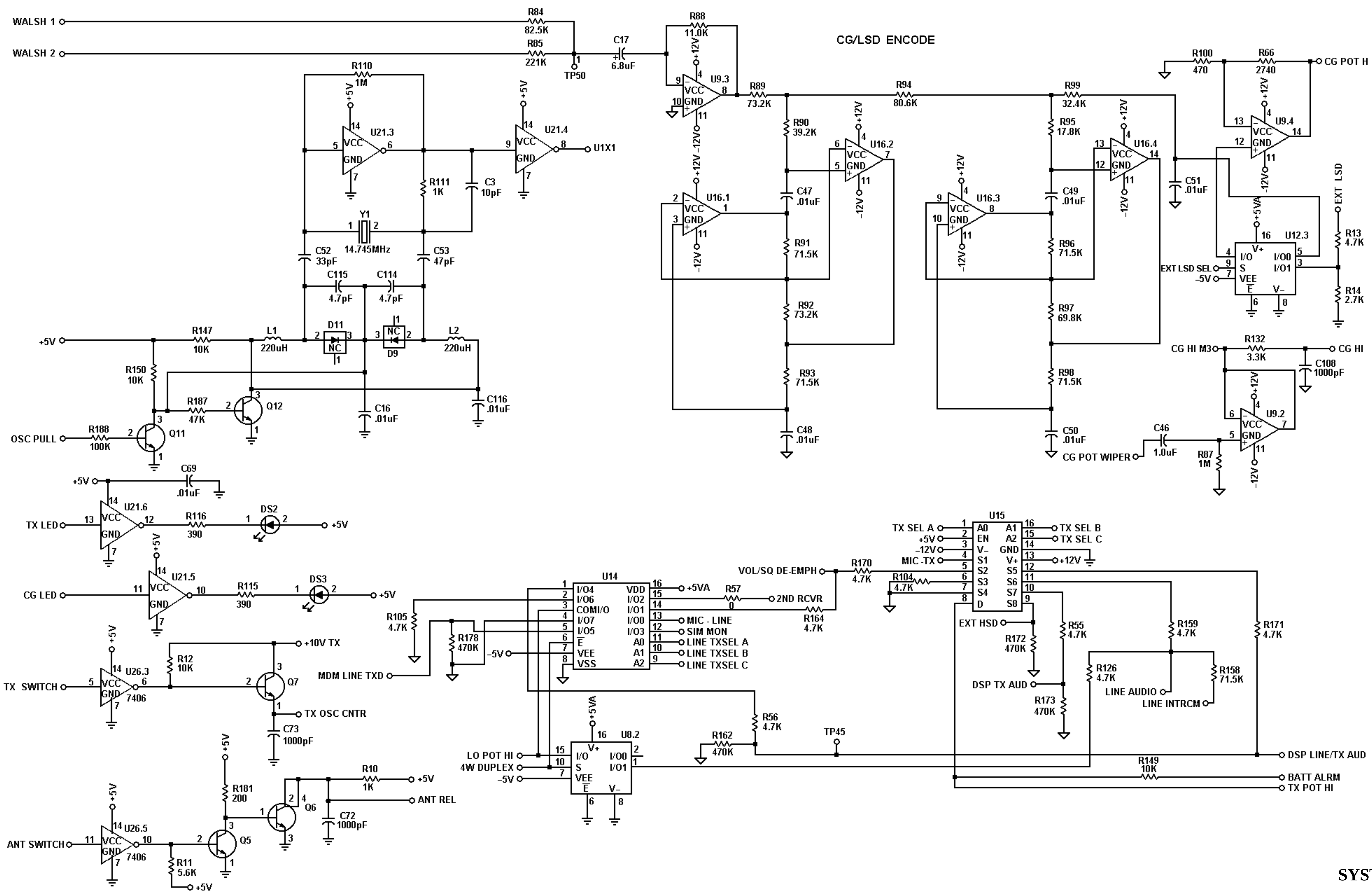
SYSTEM BOARD
188D5498G1

(188D5496, Sh. 3, Rev. 2)



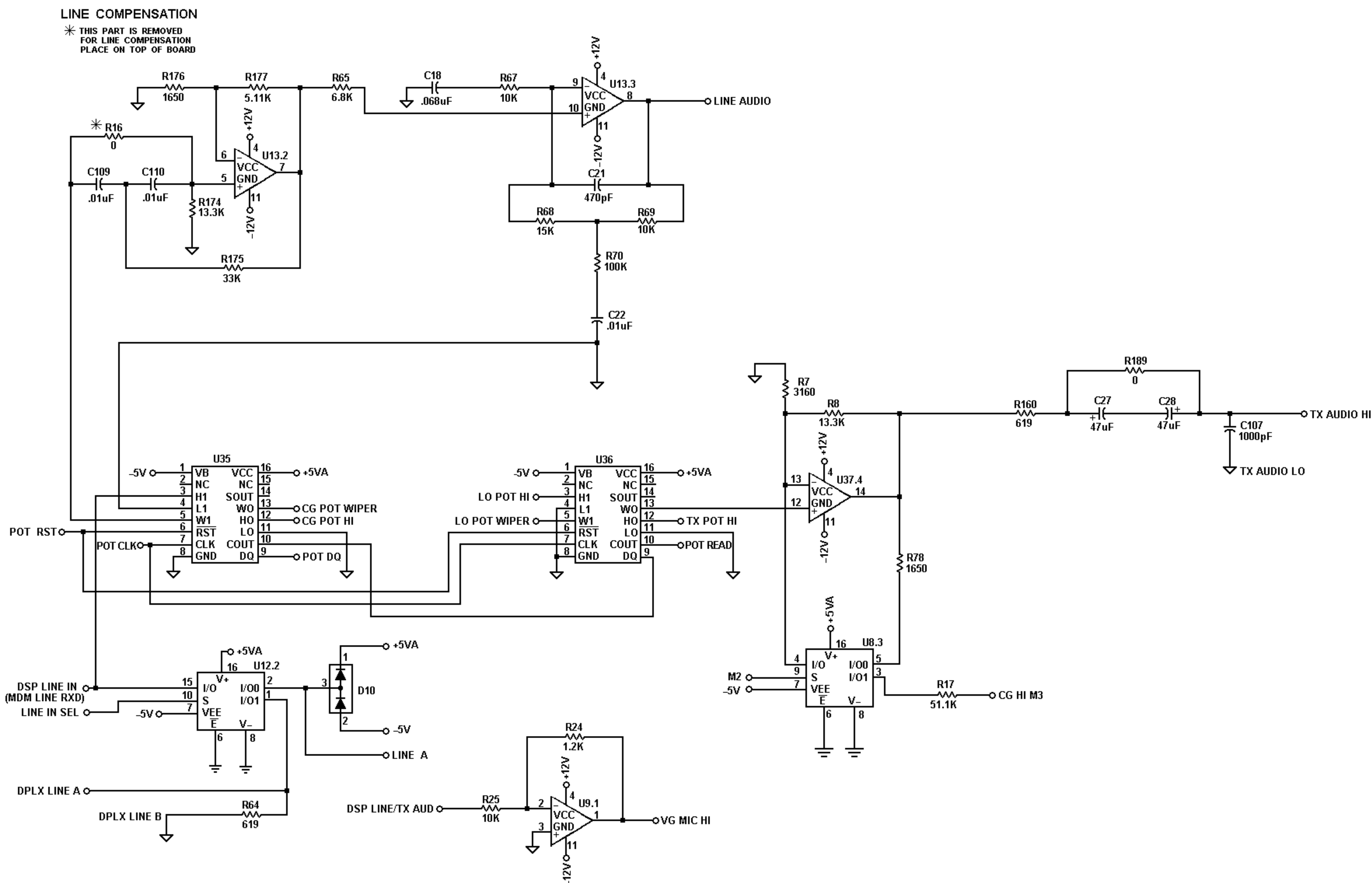
SYSTEM BOARD
188D5498G1

(188D5496, Sh. 4, Rev. 2)



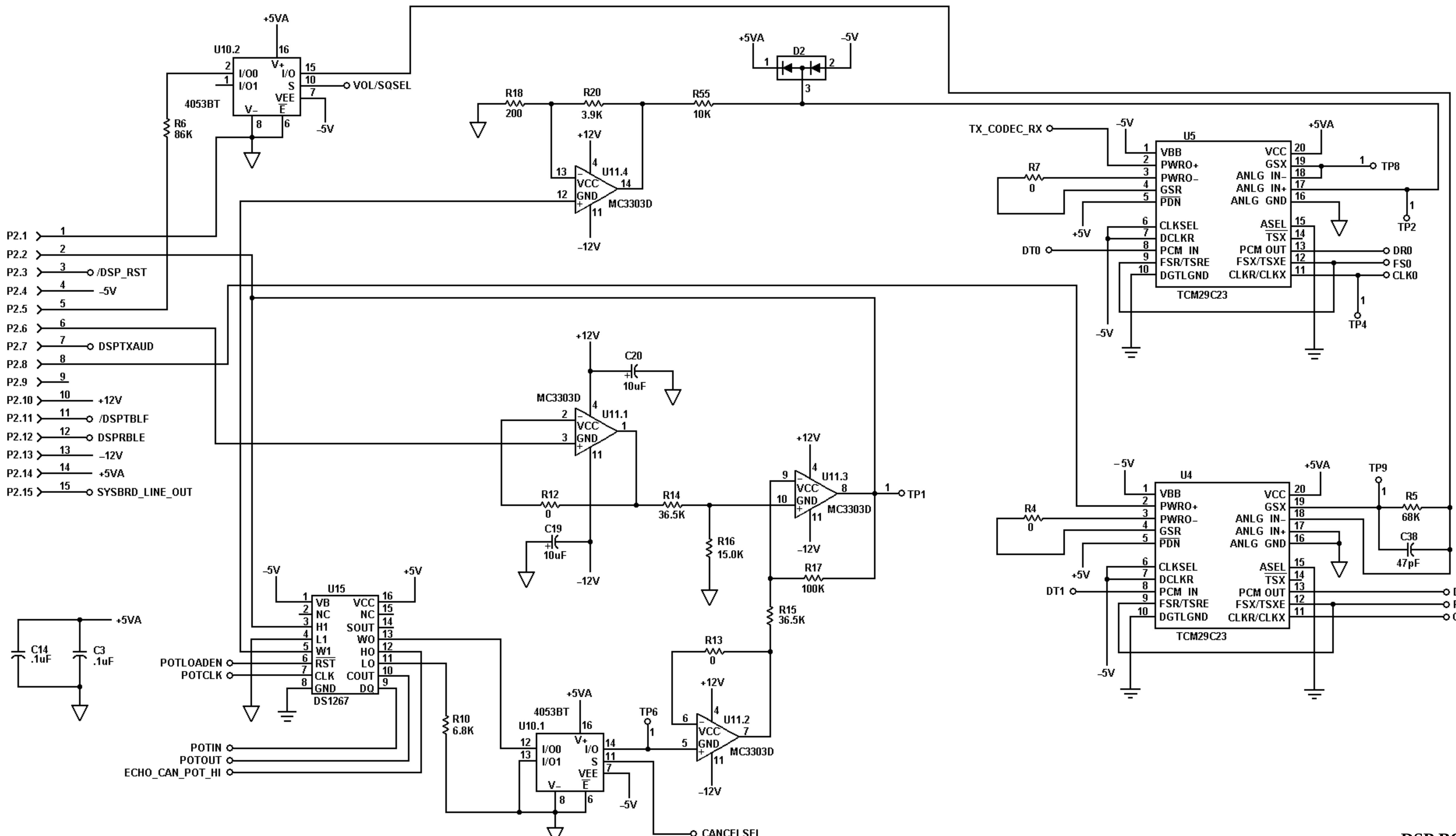
SYSTEM BOARD
188D5498G1

(188D5496, Sh. 5, Rev. 2)



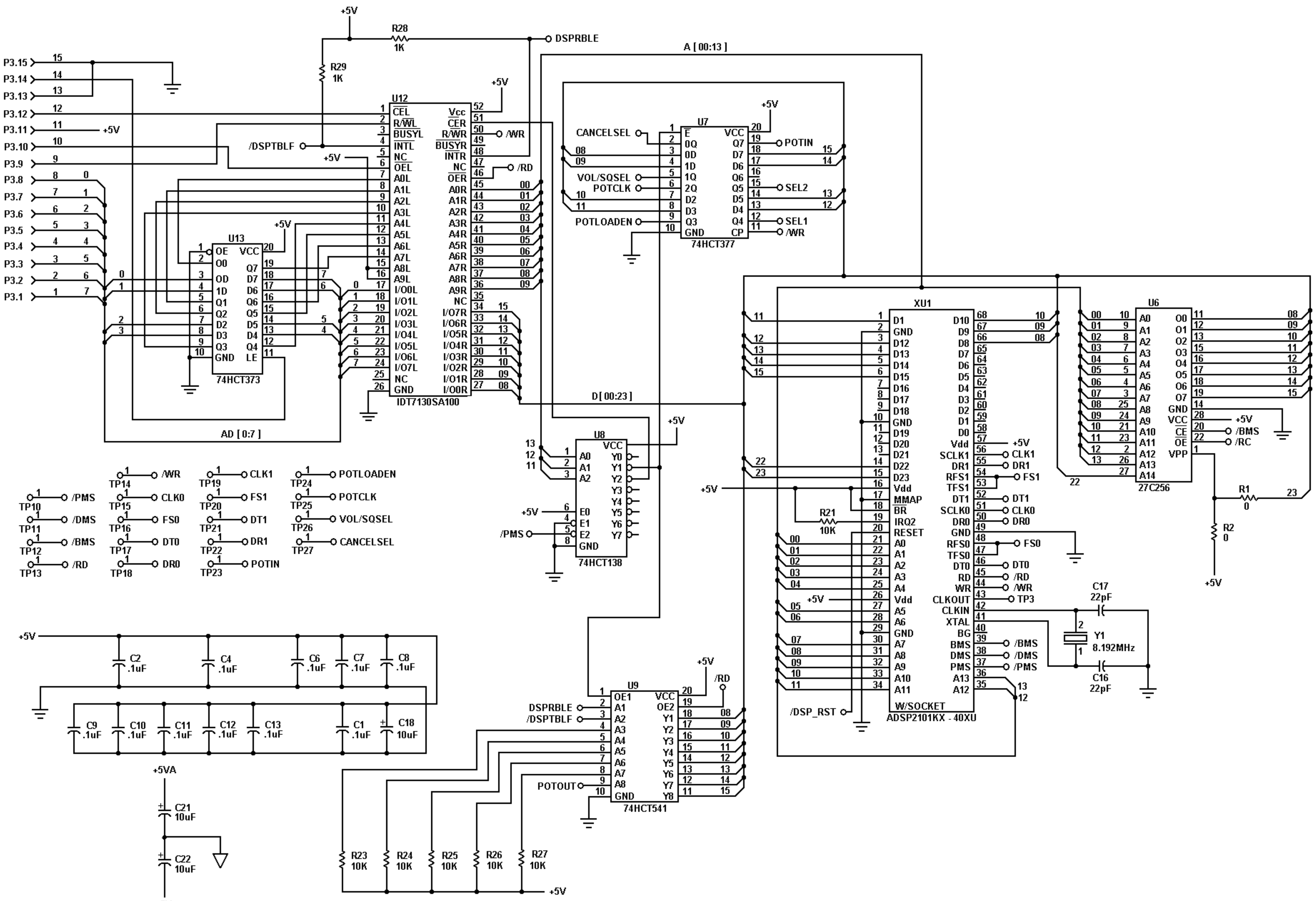
SYSTEM BOARD
188D5498G1

(188D5496, Sh. 6, Rev. 2)



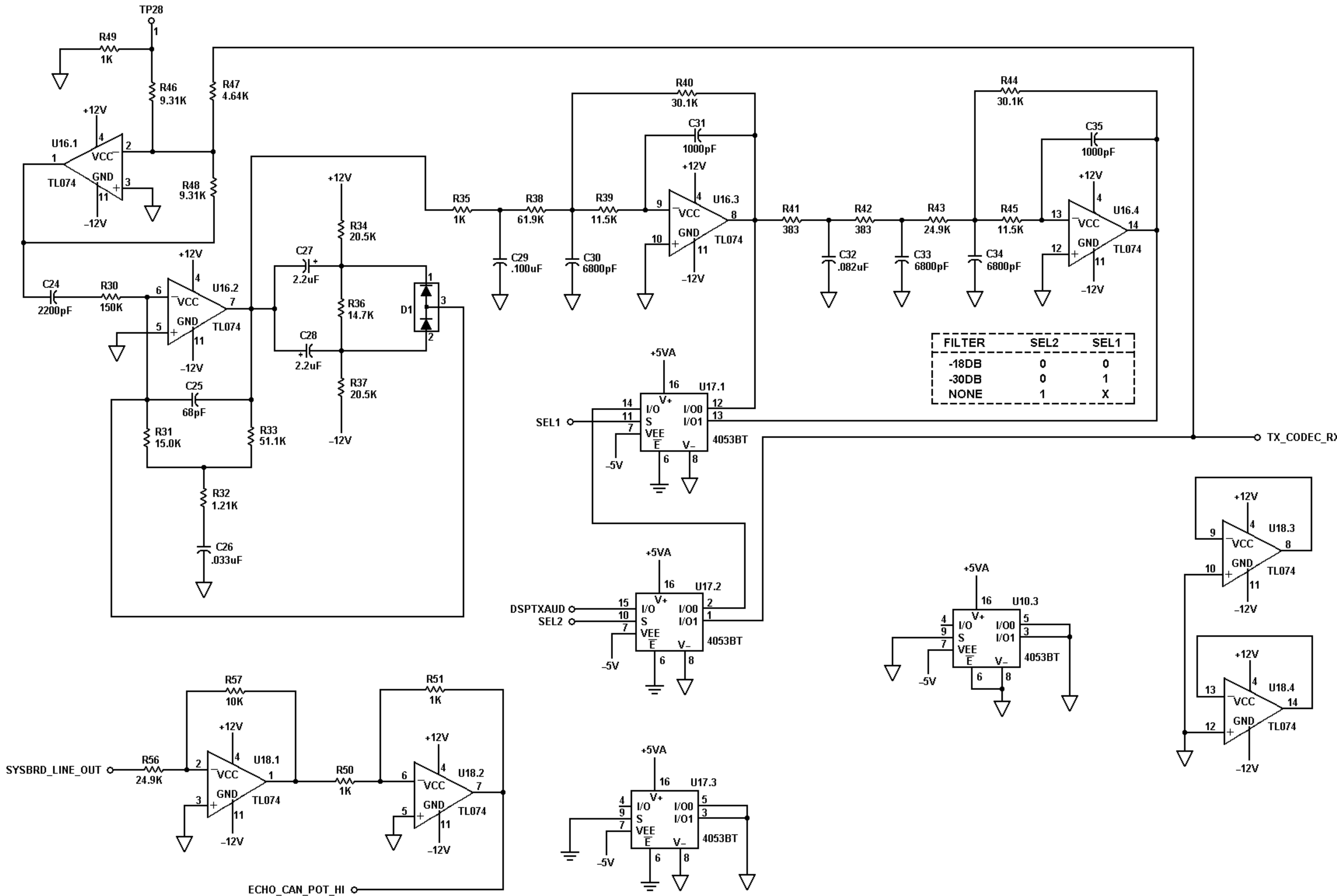
DSP BOARD
188D5682G1

(188D5680, Sh. 1, Rev. 0)



DSP BOARD
188D5682G1

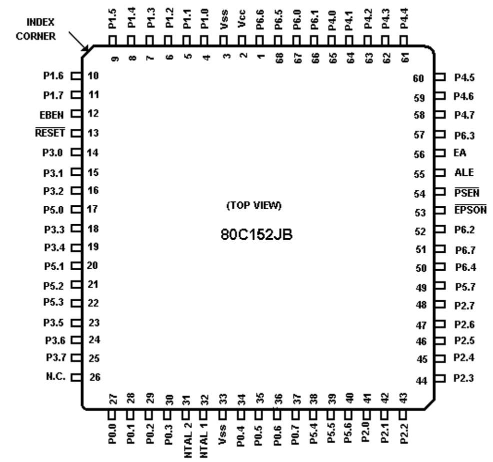
(188D5680, Sh. 2, Rev. 0)



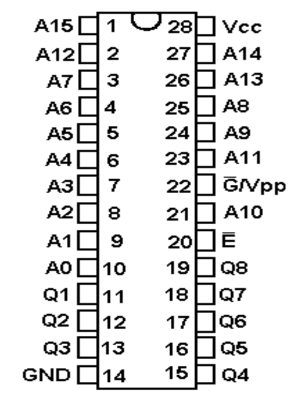
DSP BOARD
188D5682G1

(188D5680, Sh. 3, Rev. 0)

Microcomputer, U1
19A705982P101
(INTEL 80C152JB-1)



EPROM Kit U4
344A3307G17



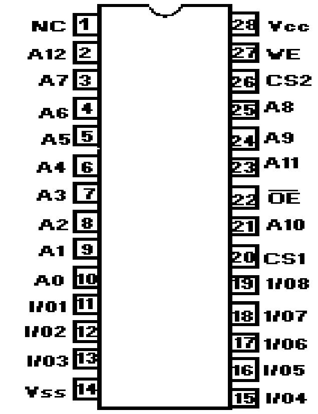
8K x 8-Bit Static CMOS RAM U5
19A705603P6 ***(KM6264AL-10)***

TRUTH TABLE

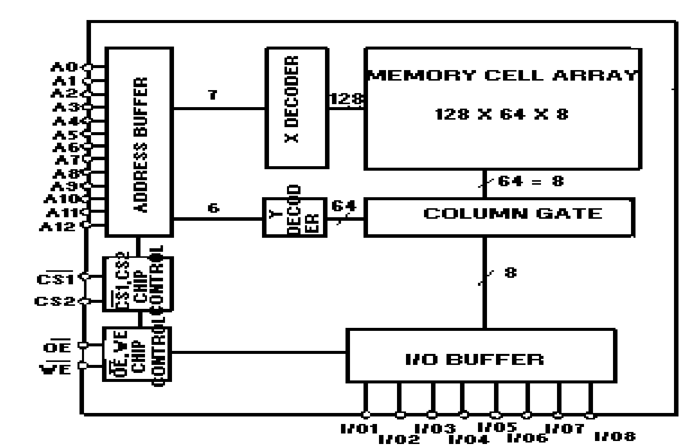
~WE	~CS1	CS2	~OE	MODE	I/O PIN
X	H	X	X	NOT SELECTED (POWER DOWN)	HIGH Z
X	X	L	X		HIGH Z
H	L	H	H	OUTPUT DISABLED	HIGH Z
H	L	H	L	READ	DOUT
L	L	H	H	WRITE	D IN
L	L	H	L		D IN

X=H OR L

PIN ARRANGEMENT

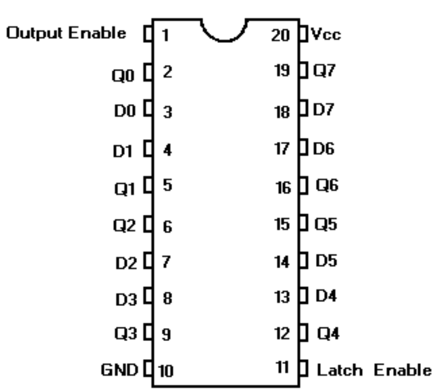


BLOCK DIAGRAM

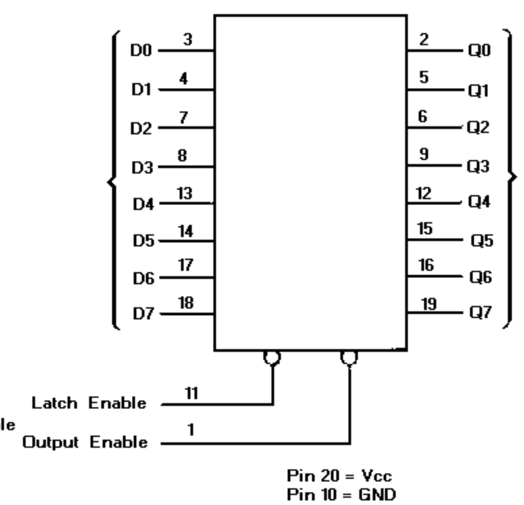


Octal Data Latch U2
19A703471P302 ***(74HC373)***

PIN ASSIGNMENT



BLOCK DIAGRAM

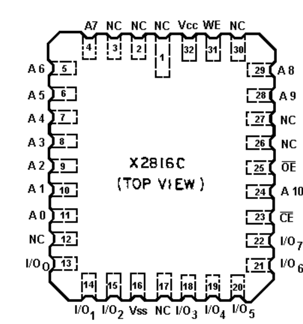


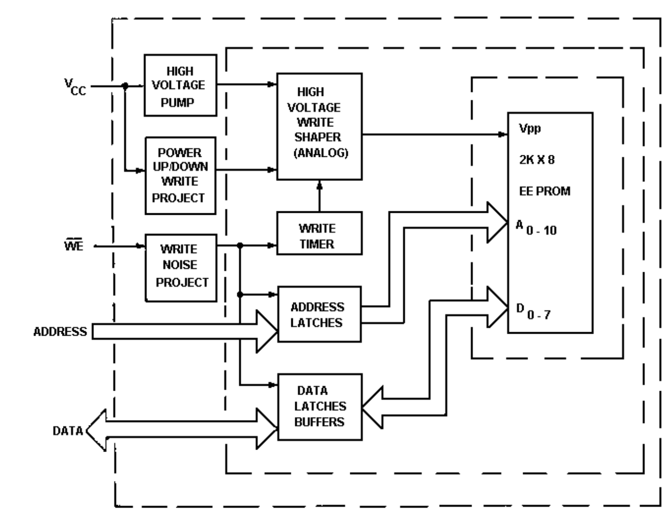
FUNCTION TABLE

Output Enable	Latch Enable	D	Output
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

X = don't care
Z = high impedance

Optoisolator U6
19A703952P102
(XICOR X2816CP-20)

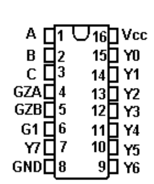


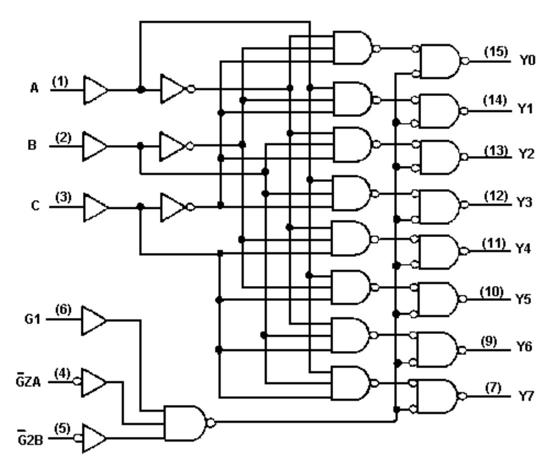


PIN NAMES

A 0 - A 10	ADDRESS INPUTS
I/O0 - I/O7	DATA INPUTS/OUTPUTS
~CE	CHIP ENABLE
~OE	OUTPUT ENABLE
~WE	WRITE ENABLE
Vcc	+5V
VxX	GROUND
NC	NO CONNECT

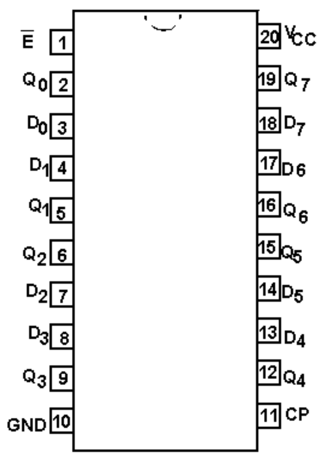
3-to-8 Decoder/Demultiplexer U3
19A703471P120 ***(74HC138)***





SYSTEM MODULE

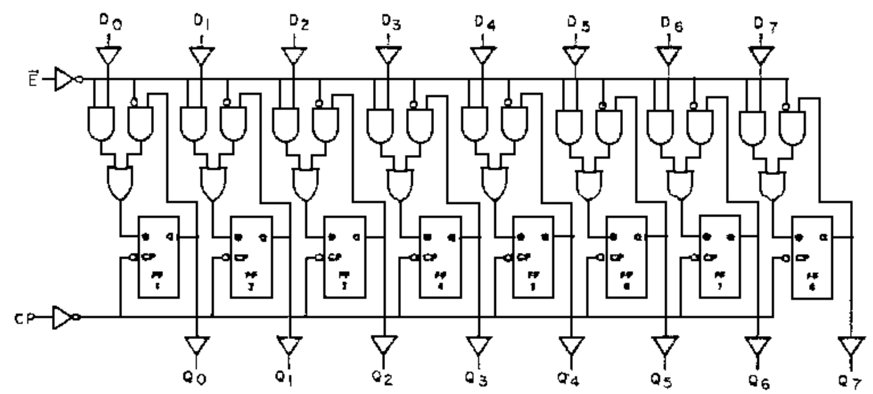
CMOS Octal Data Flip-Flop U7
19A704380P319 *(74HC377)*



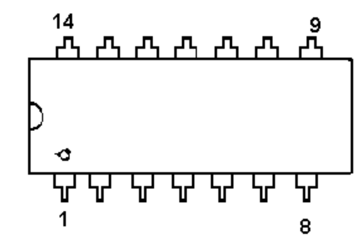
FUNCTION TABLE

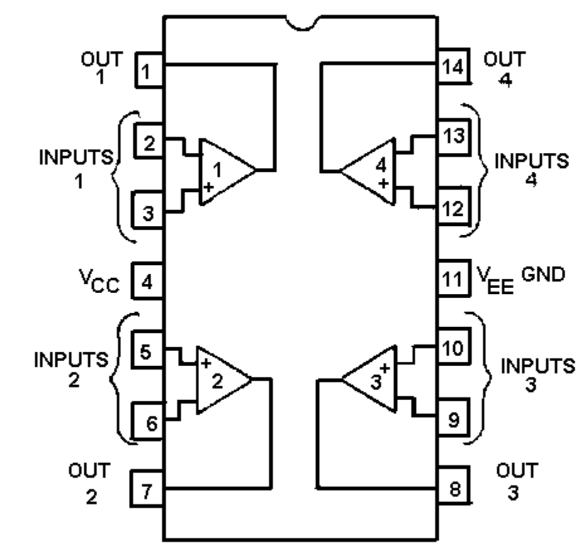
OPERATING MODES	INPUTS			OUTPUTS
	CP	E	Dn	On
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑ X	h H	X X	no change no change

H = HIGH voltage level
h = HIGH voltage level one setup tone prior to the LOW-to-HIGH CP transition.
L = LOW voltage level
l = LOW voltage level one setup tone prior to the LOW-to-HIGH CP transition
↑ = LOW-to-HIGH CP transition
X = Don't care

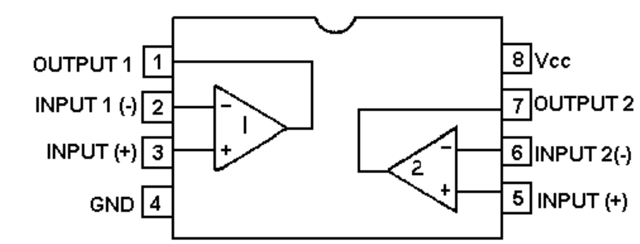


Operational Amplifier U9, U31
344A3070P3 *(TL074)*
Operational Amplifier U10, U13, U16, U17, U30, & U37
19A704883P2 *(MC3303D)*

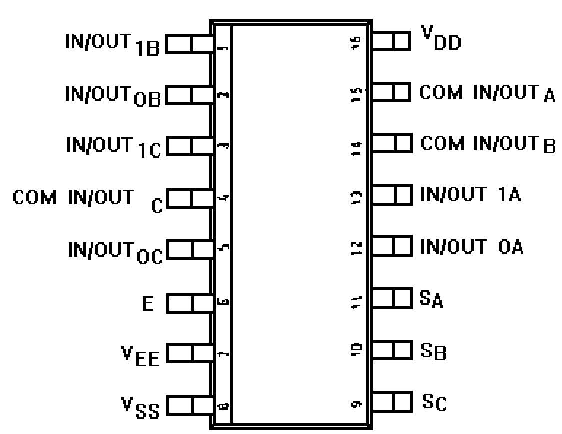


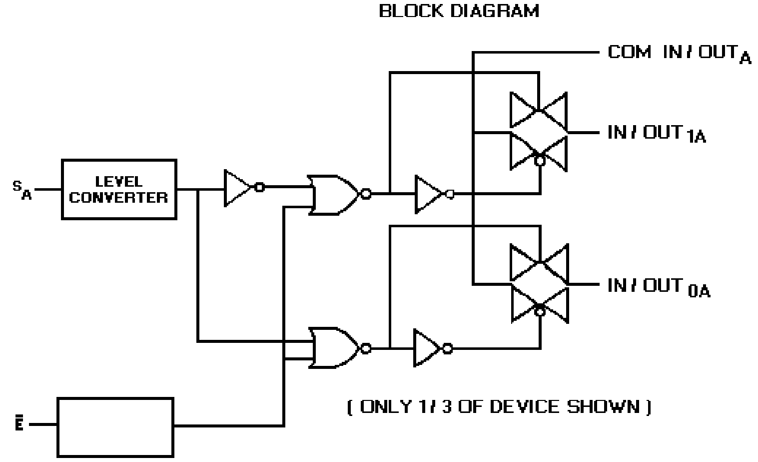


Daul Op Amp U11
19A116297P7 *(MC4558CD)*



Triple 2-Channel Analog Multiplexer U8, U12
19A702705P5 *(4053BM)*

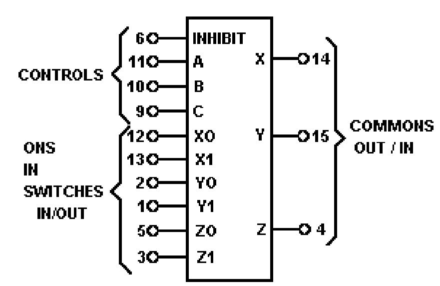




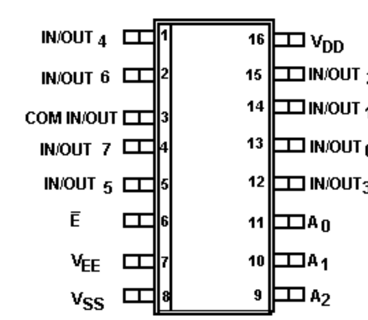
TRUTH TABLE

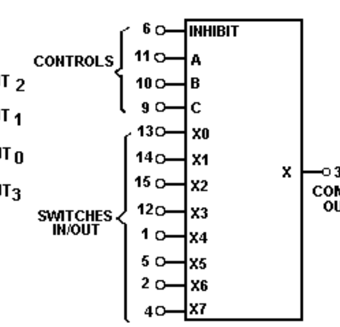
CONTROL INPUTS		ON-SWITCHES
INHIBIT	SELECT C B A	
0	0 0 0	Z0 Y0 X0
0	0 0 1	Z0 Y0 X1
0	0 1 0	Z0 Y1 X0
0	0 1 1	Z0 Y1 X1
0	1 0 0	Z1 Y0 X0
0	1 0 1	Z1 Y0 X1
0	1 1 0	Z1 Y1 X0
0	1 1 1	Z1 Y1 X1
1	x x x	NONE

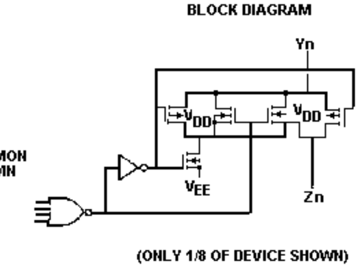
X = DON'T CARE



8-Channel Analog Multiplexer U14, U32, U33
19A702705P3 *(4051BM)*



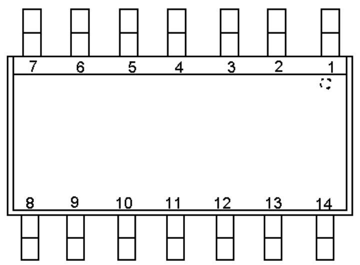


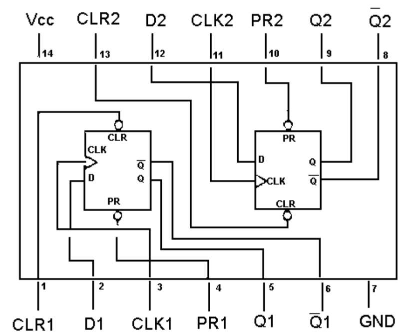


CONTROL INPUTS		ON-SWITCHES
INHIBIT	SELECT C B A	
0	0 0 0	X0
0	0 0 1	X1
0	0 1 0	X2
0	0 1 1	X3
0	1 0 0	X4
0	1 0 1	X5
0	1 1 0	X6
0	1 1 1	X7
1	X X X	NONE

X = DON'T CARE

CMOS Dual Data Flip-Flop U18, U28
19A704380P302 ***(74HC74)***



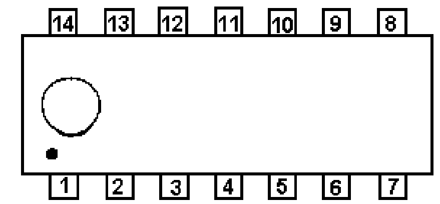


INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
K	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

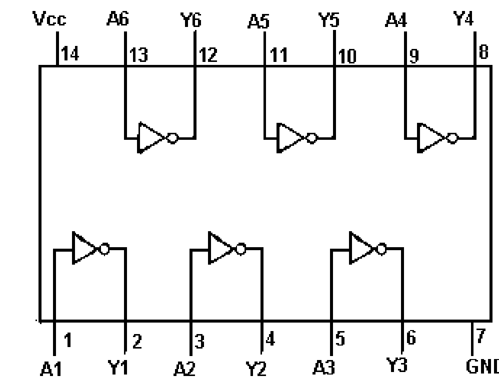
NOTE: Q0 = the level of Q before the indicated inout conditions were established.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Hex Inverters U21
19A703995P3 ***(74HCU0-4)***

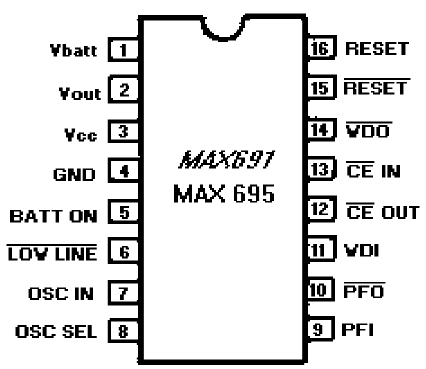
PIN CONFIGURATION



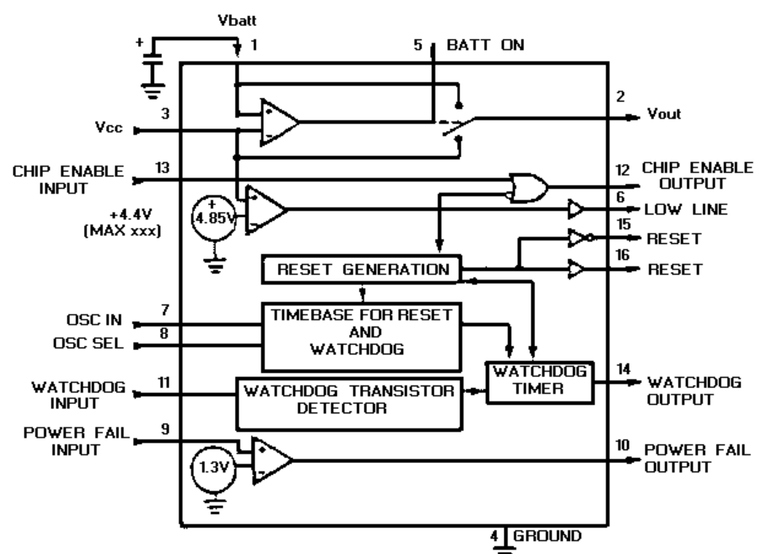
LOGIC DIAGRAM



Supervisory Circuit U19
19A149895P1 ***(MAX691C)***

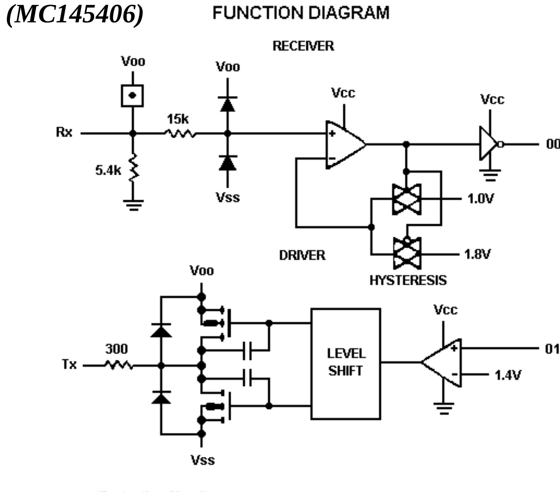


TOP VIEW

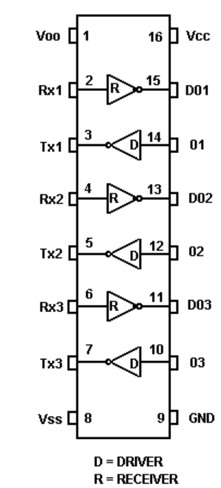


Driver/Receiver: EIA-232D/V.28 U22
344A3039P201 ***(MC145406)***

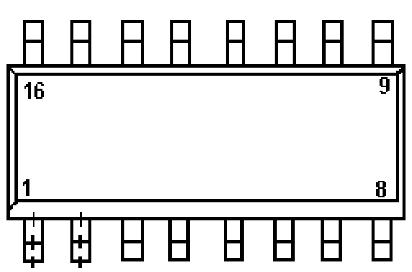
FUNCTION DIAGRAM



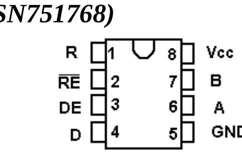
PIN ASSIGNMENT



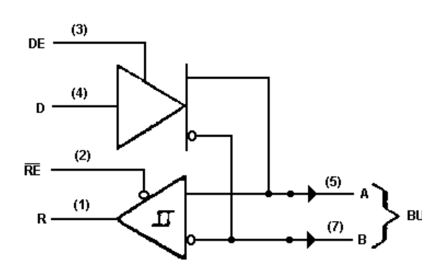
Hex Open Collector Inverter U20, U26, U40
19A116180P575 ***(7406)***



Differential Bus Transceiver U24
19A705980P101 ***(SN751768)***



logic diagram (positive logic)



FUNCTION TABLE (DRIVER)

INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

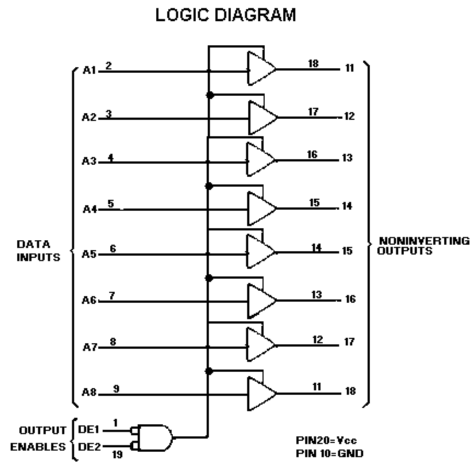
FUNCTION TABLE (RECEIVER)

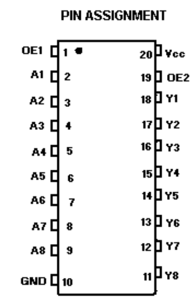
DIFFERENTIAL INPUTS A - B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} > 0.2V$	L	H
$-0.2V < V_{ID} < 0.2V$	L	?
$V_{ID} < -0.2V$	L	L
X	H	Z

H = high level, L = low level, ? = indeterminate.
X = irrelevant, z = high impedance (off)

SYSTEM MODULE

Octal Tri-State Transceiver U25
19A703471P316 *(74HC541)*



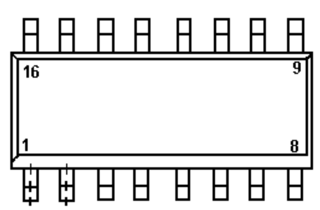


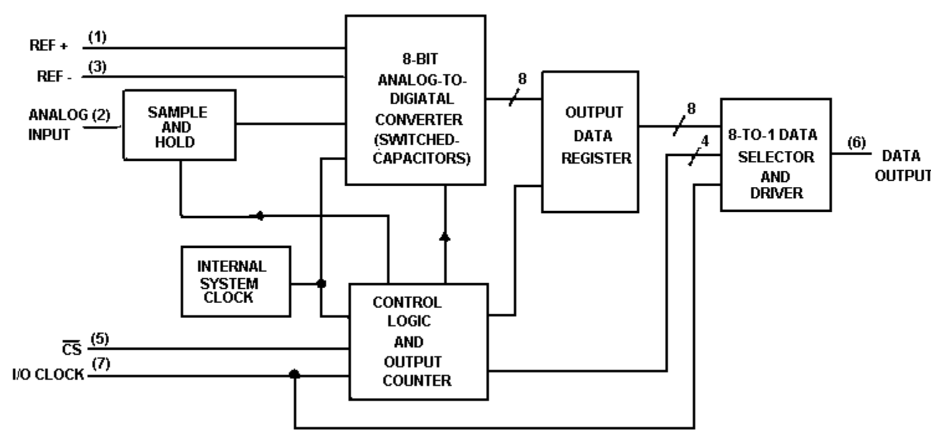
FUNCTION TABLE

INPUTS			OUTPUTS
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

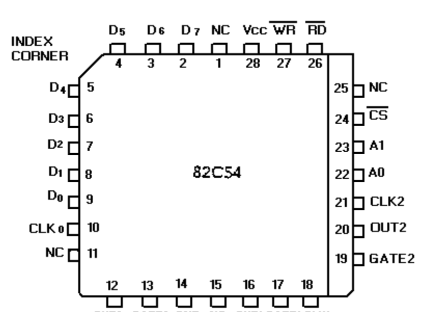
Z= high impedance
X=don't care

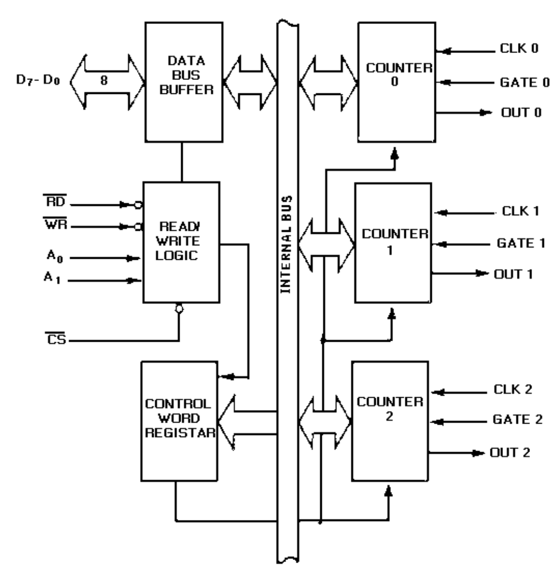
CMOS A/D Converter U27
19A705979P101 *(TL549CP)*



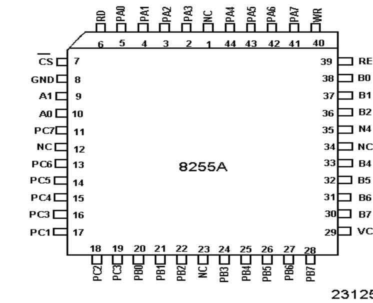


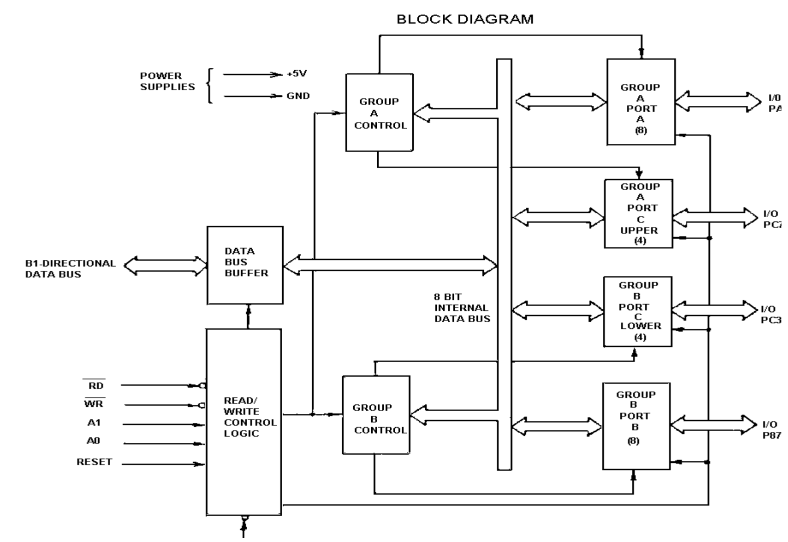
CH MOS Programmable Interval Timer U29
19A149466P301 *(INTEL 82C54)*



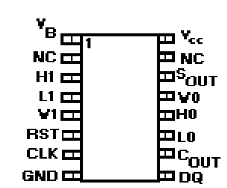


CH MOS Programmable Peripheral Interface U34
19A705991P101 *(C82C55A)*



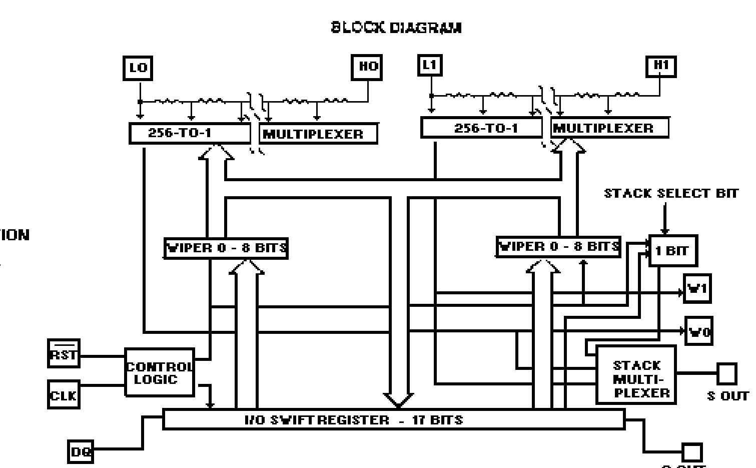


Digital Potentiometer U35, U36
344A3041P201 *(DS1267S-10)*



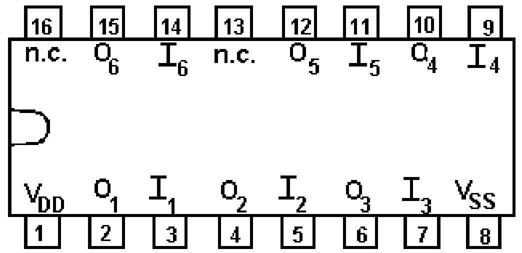
PIN NAMES

LO,L1 - LOWER END OF RESISTOR
H0,H1 - HIGHER END OF RESISTOR
W0,W1 - WIPER END OF RESISTOR
V_B - SUBSTRATE BIAS
S_{OUT} - WIPER FOR STACKED CONFIGURATION
RST - SERIAL PORT RESET INPUT
DQ - SERIAL PORT DATA INPUT/OUTPUT
CLK - SERIAL PORT CLOCK INPUT
C_{OUT} - CASCADE SERAIL PORT OUTPUT
V_{CC} - +5 VOLT INPUT
GND - GROUND
NC - NO CONNECTION



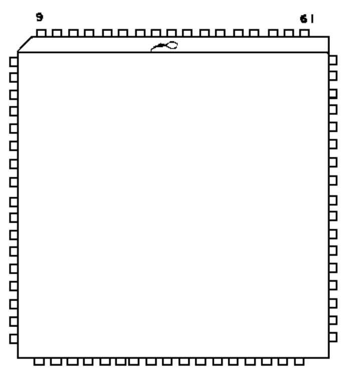
SYSTEM MODULE

Hex Inverting Buffer/Converter U41
19A700176P101 *(4049UBD)*

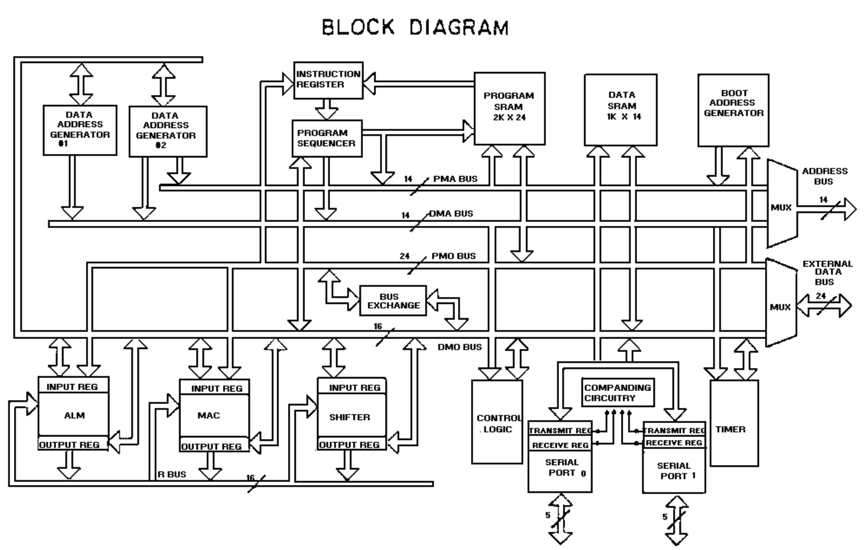


DSP BOARD

Digital Signal Processor U1
344A3038P101 *(ADSP210KX-40)*

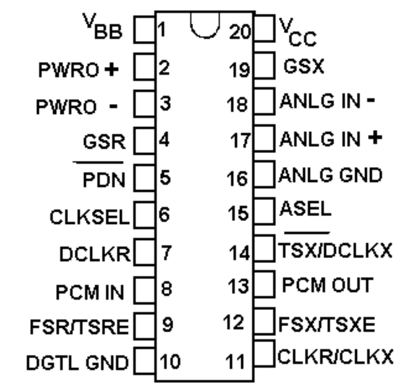


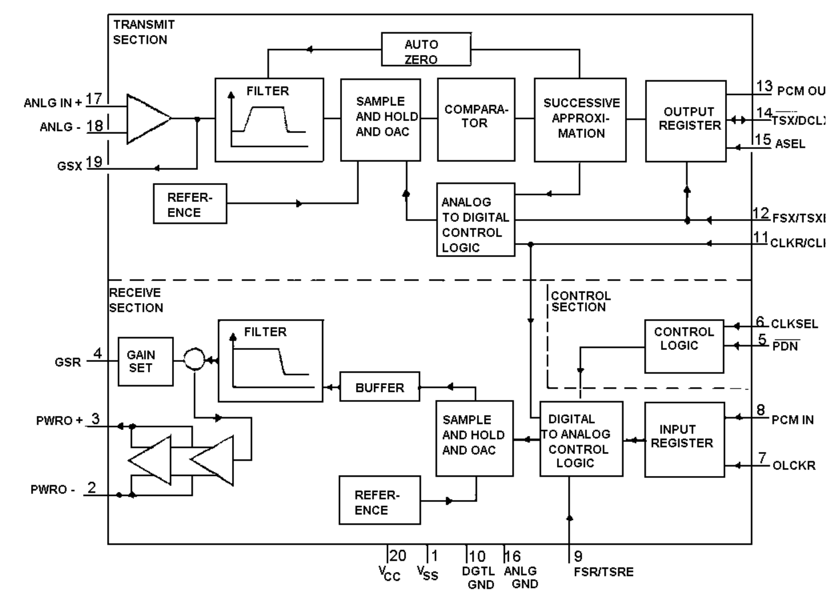
PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME
B1	GND	K11	$\overline{WR}$
B2	D19	K10	$\overline{RD}$
C1	D20	J11	DT0
C2	D21	J10	TFS0
D1	D22	H11	RFSQ
D2	D23	H10	GND
D1	V_{DD}	G11	DRO
D2	MMAP	G10	SCLK0
F1	BR	F11	DT1
F2	$\overline{1RQ2}$	F10	TFS1
G1	$\overline{RESET}$	E11	RFS1
G2	A0	E10	DR1
H1	A1	D11	SCLK1
H2	A2	D10	V_{DD}
J1	A3	C11	D0
J2	A4	C10	D1
K1	V_{DD}	B11	D2
L2	A5	A10	D3
K2	A6	B10	D4
L3	GND	A9	D5
K3	A7	B9	D6
L4	A8	A8	D7
K4	A9	B8	D8
L5	A10	A7	D9
K5	A11	B7	D10
L6	A12	A6	D11
K6	A13	B6	GND
L7	$\overline{PMS}$	A5	D12
K7	$\overline{DMS}$	B5	D13
L8	$\overline{BMS}$	A4	D14
K8	$\overline{BG}$	B4	D15
L9	XTAL	A3	D16
K9	CLKIN	B3	D17
L10	CLKOUT	A2	D18
C3	Index		



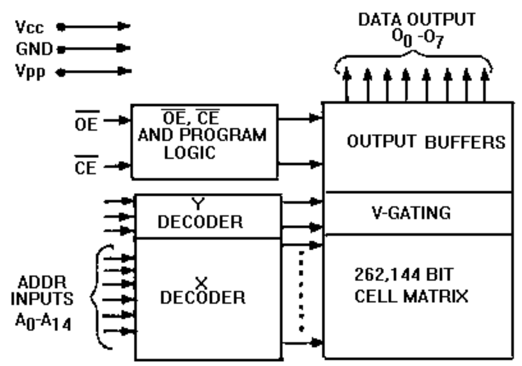
DSP BOARD

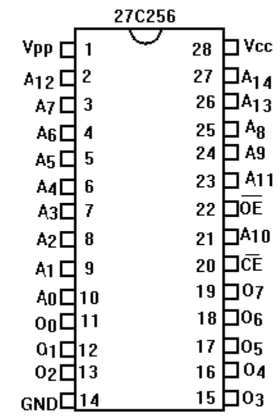
Encoder/Decoder U4, U5
19A705827P1 *(TCM29C23)*





EPROM Kit U6
344A3309G5

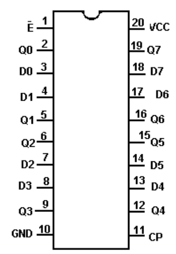




PIN NAME

A_0 - A_{14}	ADDRESSES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
O_0 - O_7	OUTPUTS

CMOS Hi-Speed Octal D Type Flip-Flop With Data Enable U7
344A3064P203 ***(74HCT377)***

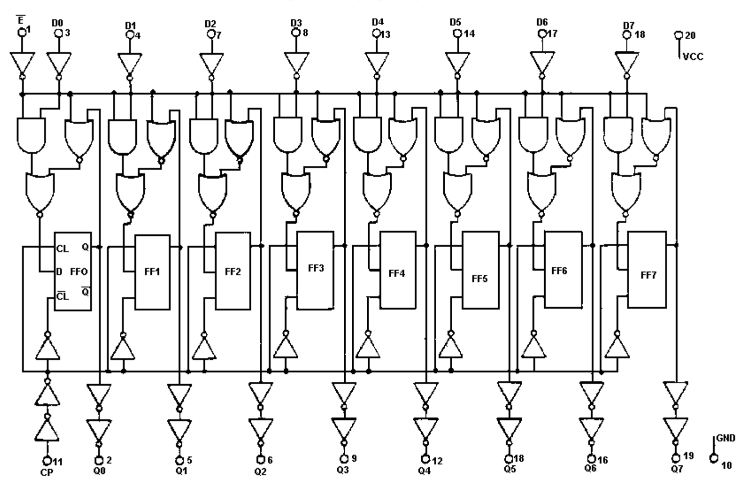


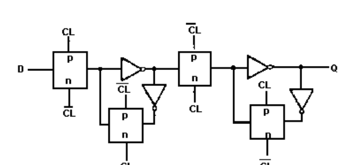
TRUTH TABLE

OPERATING MODE	INPUTS CP	E	Dn	OUTPUTS On
LOAD "1"	↗	l	h	H
LOAD "0"	↗	l	X	L
HOLD (do nothing)	↗	h	X	no change no change

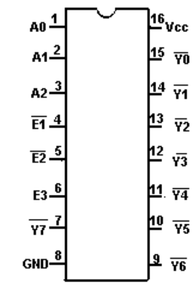
H= HIGH Voltage level steady state.
h= HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L= LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to - HIGH clock transition
X = Don't care
↗ = LOW to -HIGH clock

BLOCK DIAGRAM





CMOS Hi-Speed 3 To 8 Line Decoder/Demultiplexer U8
344A3064P201 ***(74HCT138)***

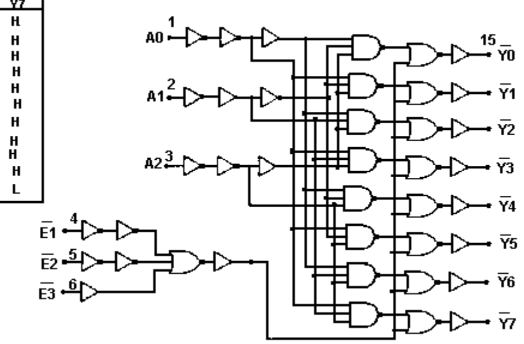


TRUTH TABLE

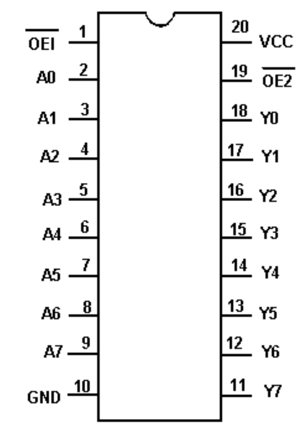
INPUTS ENABLE E3	$\overline{E2}$	$\overline{E1}$	ADDRESS A2	A1	A0	OUTPUTS $\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH LEVEL. L= LOW LEVEL. X = DON' T CARE

BLOCK DIAGRAM



CMOS Hi-Speed Octal Buffer/Line Driver, 3 State U9
344A3064P204 ***(74HCT541)***

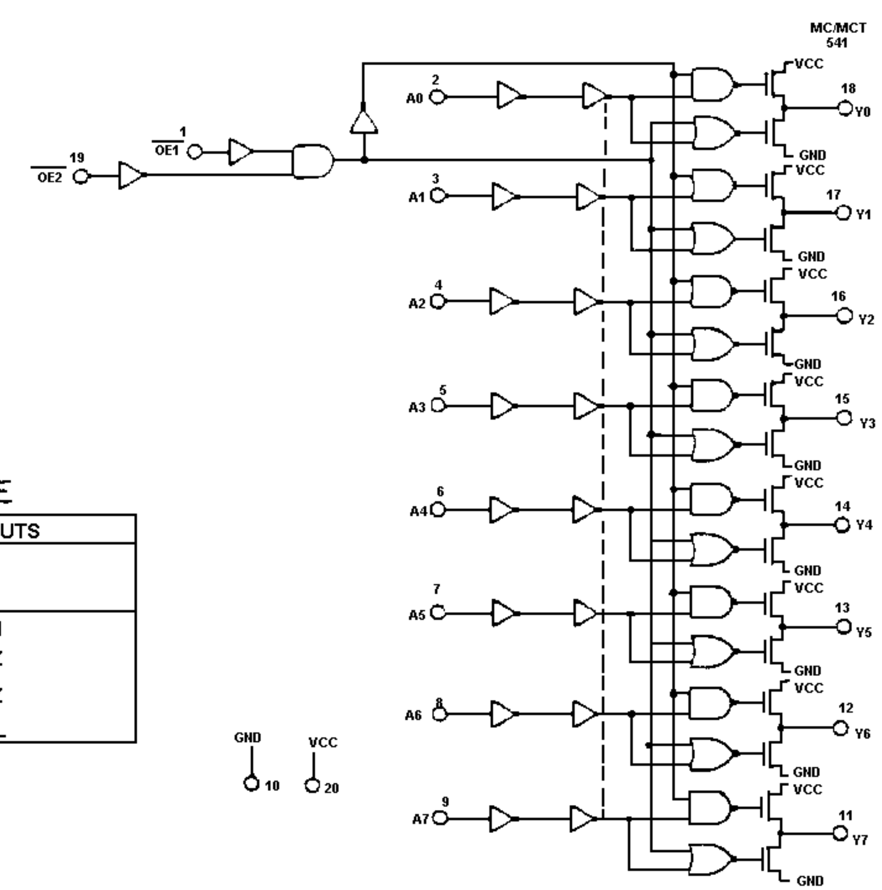


TRUTH TABLE

INPUTS $\overline{OE1}$	$\overline{OE2}$	An	OUTPUTS
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

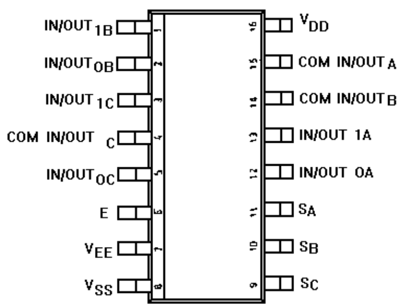
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

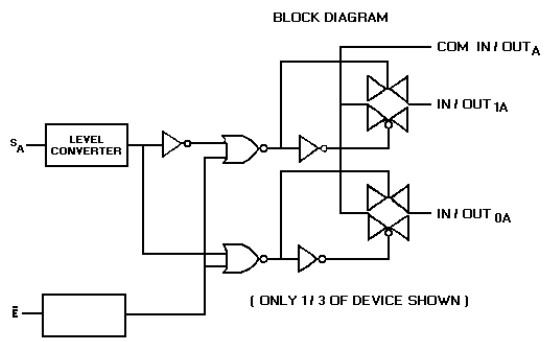
BLOCK DIAGRAM



DSP BOARD

Triple 2-Channel Analog Multiplexer U10
19A702705P5 ***(MC3303D)***

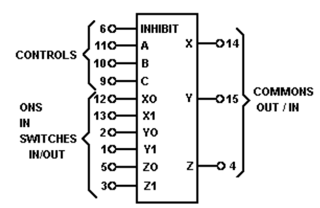




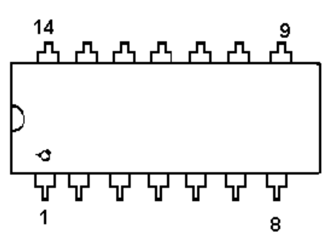
TRUTH TABLE

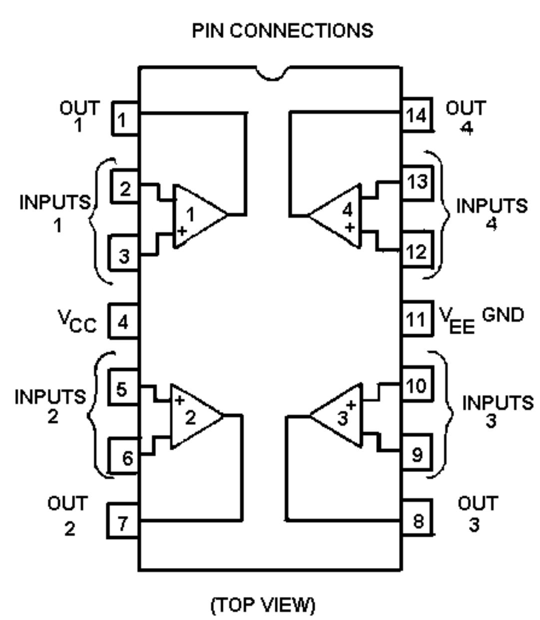
CONTROL INPUTS				ON-SWITCHES
	SELECT			
INHIBIT	C	B	A	
0	0	0	0	Z0 Y0 X0
0	0	0	1	Z0 Y0 X1
0	0	1	0	Z0 Y1 X0
0	0	1	1	Z0 Y1 X1
0	1	0	0	Z1 Y0 X0
0	1	0	1	Z1 Y0 X1
0	1	1	0	Z1 Y1 X0
0	1	1	1	Z1 Y1 X1
1	x	x	x	NONE

X = DON'T CARE

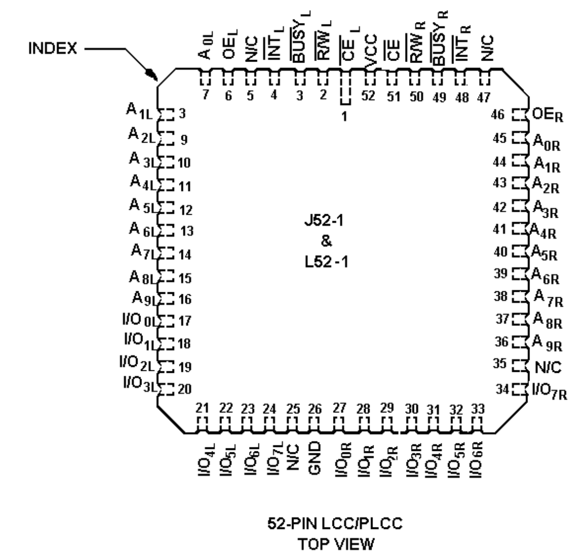


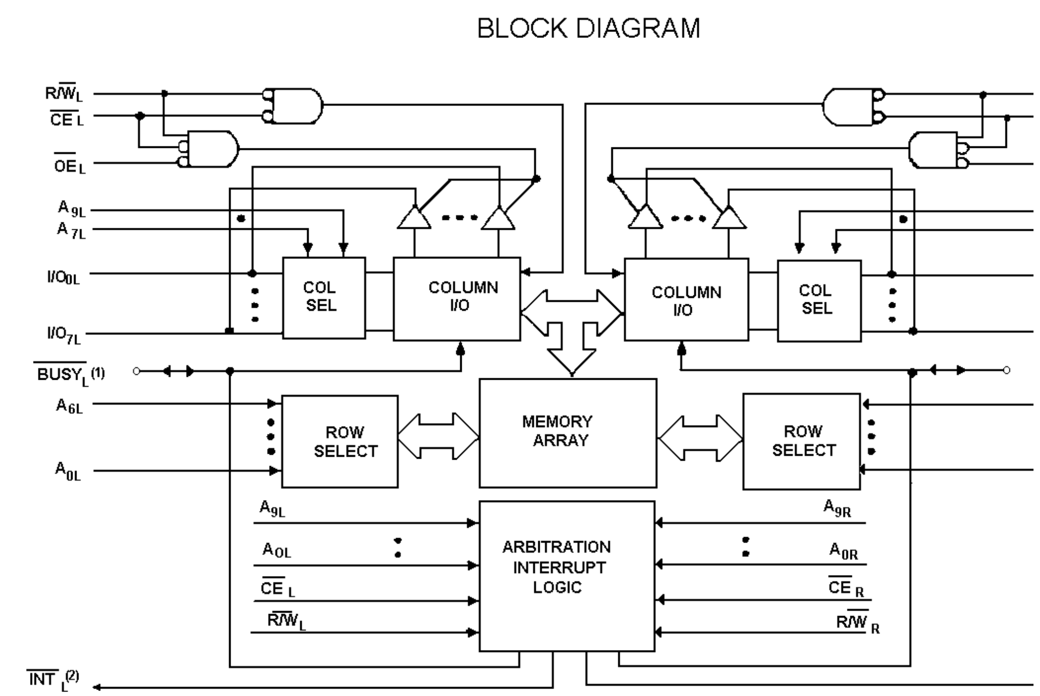
Quad Operational Amplifier U11
19A7048883P2 ***(MC4558CD)***





SRAM, 1K x 8, Dual Port U12
344A3040P201 ***(IDT7130SA100)***

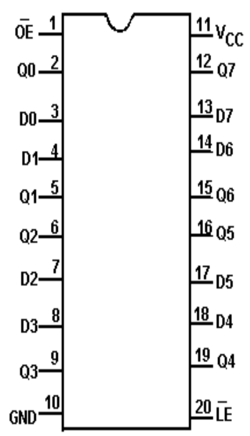




NOTES:
1. IDT7130 (MASTER): BUSY IS OPEN DRAIN OUTPUT AND REQUIRES PULLUP RESISTOR. IDT7140(SLAVE): BUSY IS INPUT.
2. OPEN DRAIN OUTPUT REQUIRES PULLUP RESISTOR.

DSP BOARD

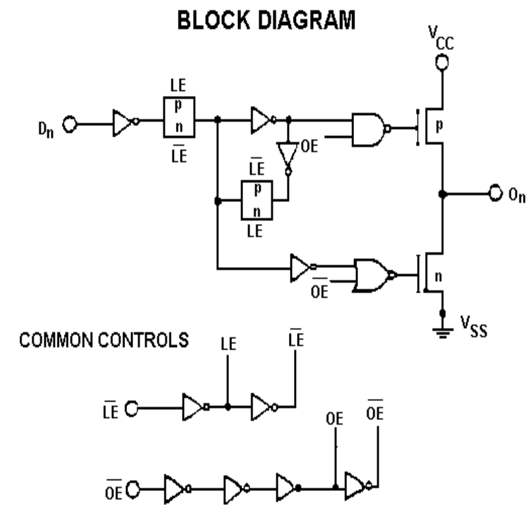
CMOS Hi-Speed Octal Transparent Latch U13
344A3064P202 ***(74HCT373)***



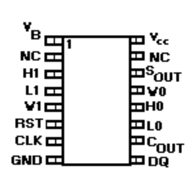
TRUTH TABLE

OUTPUT ENABLE	LATCH ENABLE	DATA	OUTPUT
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

NOTE:
L = Low voltage level X = Don't care
H = High voltage level Z = High impedance state
l = Low voltage level one set-up time prior to the high to low latch enable transition
h = High voltage level one set-up time prior to the high to low latch enable transition.

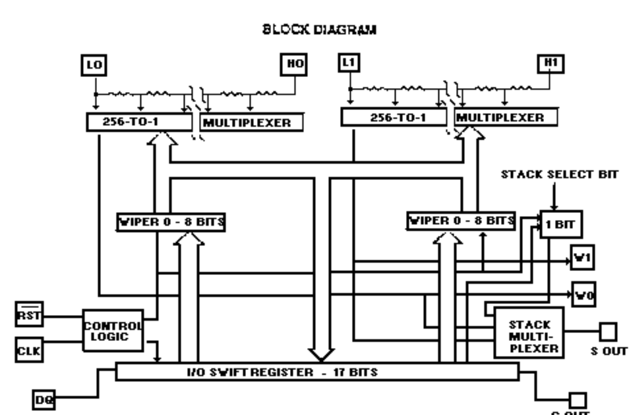


Digital Potentiometer U15
344A3041P201 ***(DS1267S-10)***

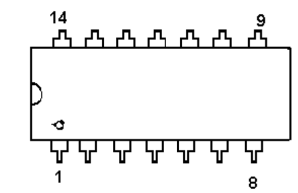


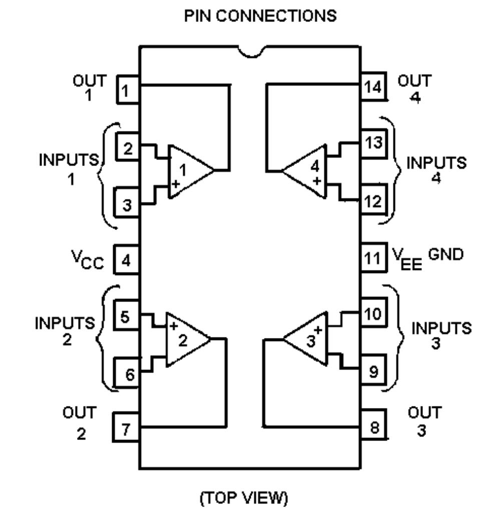
PIN NAMES

LO,L1 - LOWER END OF RESISTOR
H0,H1 - HIGHER END OF RESISTOR
W0,W1 - WIPER END OF RESISTOR
VB - SUBSTRATE BIAS
SOUT - WIPER FOR STACKED CONFIGURATION
RST - SERIAL PORT RESET INPUT
DQ - SERIAL PORT DATA INPUT/OUTPUT
CLK - SERIAL PORT CLOCK INPUT
COUT - CASCADE SERAIL PORT OUTPUT
VCC - +5 VOLT INPUT
GND - GROUND
NC - NO CONNECTION

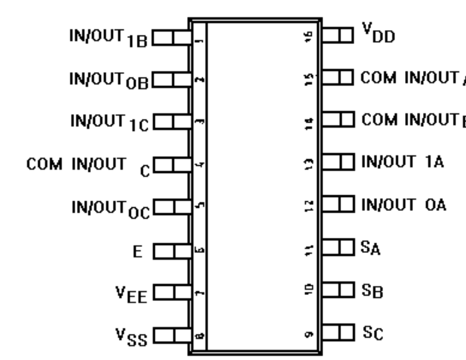


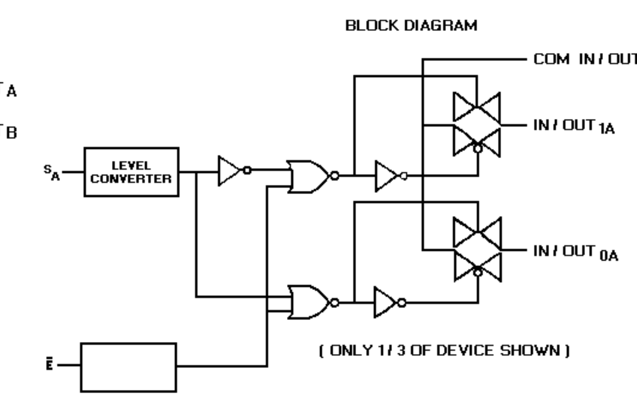
Operational Amplifier U16
344A3070P3 ***(TL075)***





Triple 2-Channel Analog Multiplexer U17
19A702705P5 ***(4053BM)***





TRUTH TABLE

CONTROL INPUTS				ON-SWITCHES
INHIBIT	SELECT			
	C	B	A	
0	0	0	0	Z0 Y0 X0
0	0	0	1	Z0 Y0 X1
0	0	1	0	Z0 Y1 X0
0	0	1	1	Z0 Y1 X1
0	1	0	0	Z1 Y0 X0
0	1	0	1	Z1 Y0 X1
0	1	1	0	Z1 Y1 X0
0	1	1	1	Z1 Y1 X1
1	x	x	x	NONE

X = DON'T CARE