



GE Mobile Communications

MASTR® II

PRIORITY SEARCH-LOCK MONITOR

19A130107G1

(OPTIONS 9552, 9553, & 9554)

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SPECIFICATIONS*

Search Rate (Each Channel)	Four times per second
Sample Time (Each Channel)	125 milliseconds
Priority Channel Search Rate	Four times per second
Priority Channel Sample Time	5 - 6 milliseconds
Priority Squelch Sensitivity	20-dB quieting
Input Power	45 milliamperes @+10 volts DC
Silicon Transistors	9
Integrated Circuit Modules	4
Light Emitting Diode	1
Temperature Range	-30°C to +60°C

* These specifications are intended primarily for the use of the serviceman. Refer to the appropriate Specification Sheet for the complete specifications.

WARNING

Under no circumstances should any person be permitted to handle any portion of the equipment that is supplied with high voltage, or to connect any external apparatus to the units while the units are supplied with power. KEEP AWAY FROM LIVE CIRCUITS.

DESCRIPTION

General Electric Priority Search-Lock Monitor provides two-channel monitoring by alternately searching a priority channel and a non-priority channel. The Priority Search-Lock Monitor (PSLM) assures reception of all signals received on the priority channel regardless of signal strength or which channel receives the first signal.

When a signal is received on the priority channel, the PSLM stops searching and locks on the priority channel for the duration of the message. When a signal is first received on the non-priority channel, the PSLM stops on that channel while monitoring the priority channel. If a signal is received on the priority channel while the PSLM is stopped on the non-priority channel, the PSLM reverts to the priority channel and locks on that channel for the duration of the message.

NOTE

The PSLM will operate only when the receiver is squelched. When the receiver is unsquelched, the PSLM will lock on the priority channel.

Also, operating the PSLM with the control unit squelch set at maximum (fully counterclockwise) may result in a repetitive thumping sound in the speaker. This is caused by a priority channel that is slightly weaker than the receiver maximum squelch sensitivity being rapidly accepted and rejected by the receiver squelch circuit.

In station applications, the priority channel is locked on either the F1 or F2 channel by simply changing a connection on the PSLM board. Instructions for making this change are contained on the Schematic Diagram (see Table of Contents).

In applications where a priority channel is not desired, the priority feature may be disabled by disconnecting C2 and C9. The PSLM will then alternately search both channels and will lock on the channel receiving the first signal.

The station option numbers and the application of each option are shown in the following chart.

Option Number	Station Control	Number of frequencies	
		Xmtr	Rcvr
9552	Extended Local/DC & Tone Remote	1 or 2	2
9553	DC Remote	1 or 2	2
9554	Tone Remote	1 or 2	2

STATION SWITCHING

LOCAL CONTROL STATIONS
(Refer to Figure 1)

In local control stations, the PSLM is controlled by the PSLM switch on the Local MASTR® Controller.

Pushing the PSLM switch removes the ground to either receiver oscillator, and applies a ground to the PSLM lead. This activates the PSLM which alternately applies ground to each of the receiver oscillators at a rate of four times per second. If a signal is received on either channel, the PSLM will lock on that channel for the duration of the message, or until a signal is received on the priority channel.

When the PSLM pushbutton is out and the R-F1/F2 switch is out the Receiver F1 is activated. When the R-F1/F2 pushbutton switch is pushed in the Receiver F2 is activated. In Local/Remote control stations the control of the PSLM is from the local control point only.

DC/TONE REMOTE CONTROL STATIONS
(Refer to Figure 2)

In DC/TONE Remote Control Stations three different control currents or Audio Tones on the control line select the receiver frequencies.

When -6A's of current for DC Control (or a tone of 1750 Hz for Tone Control) appears on the control line, this current (or tone) is detected and Q10 (or Q3) is turned on. This grounds the Rec F1 line to lock the receiver on F1.

When -11 mA's of current for DC Control (or tone of 1650 Hz for Tone Control) appears on the control line, this current (or tone) is detected and Q14 (or Q7) is turned on. This grounds the Rec F2 line to lock the receiver on F2.

STATION SWITCHING

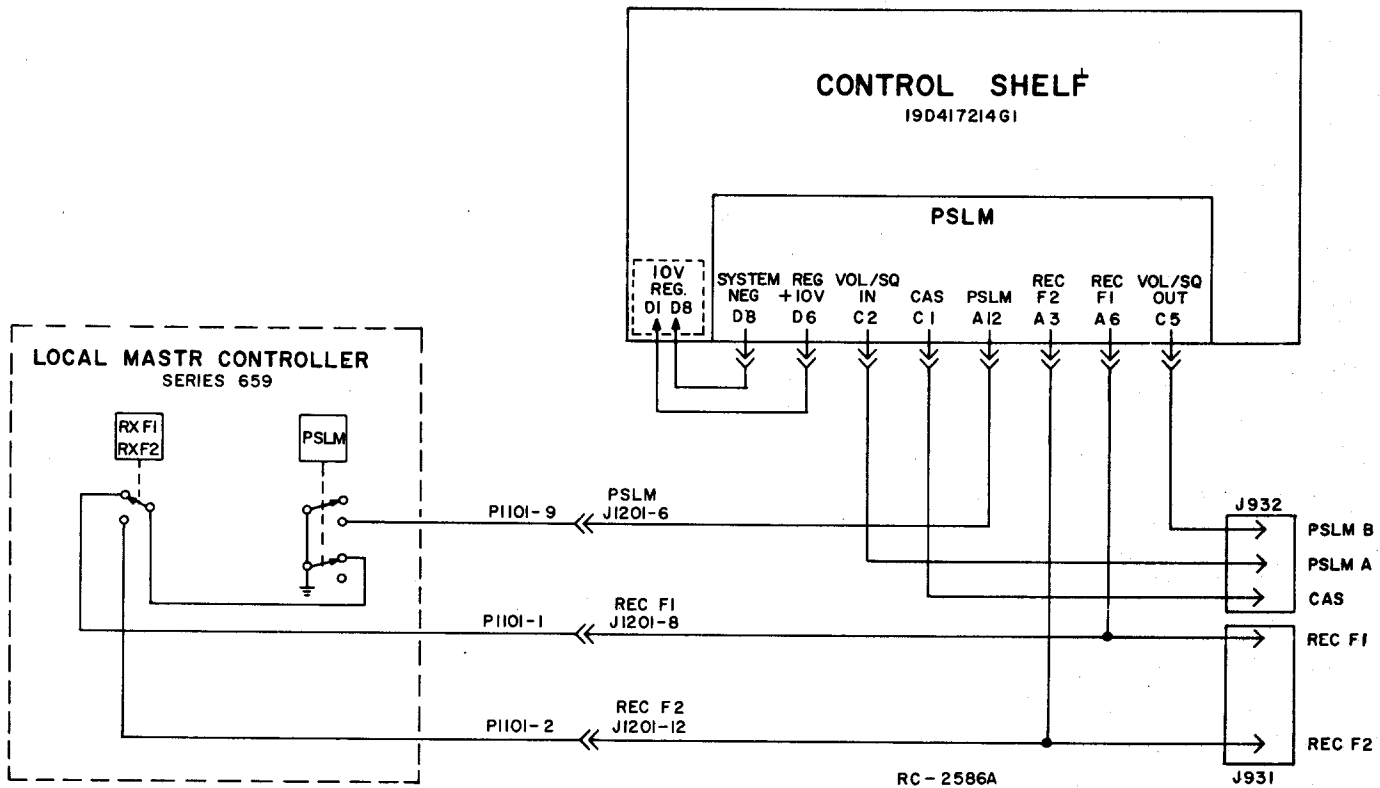


Figure 1 - Local Switching Diagram

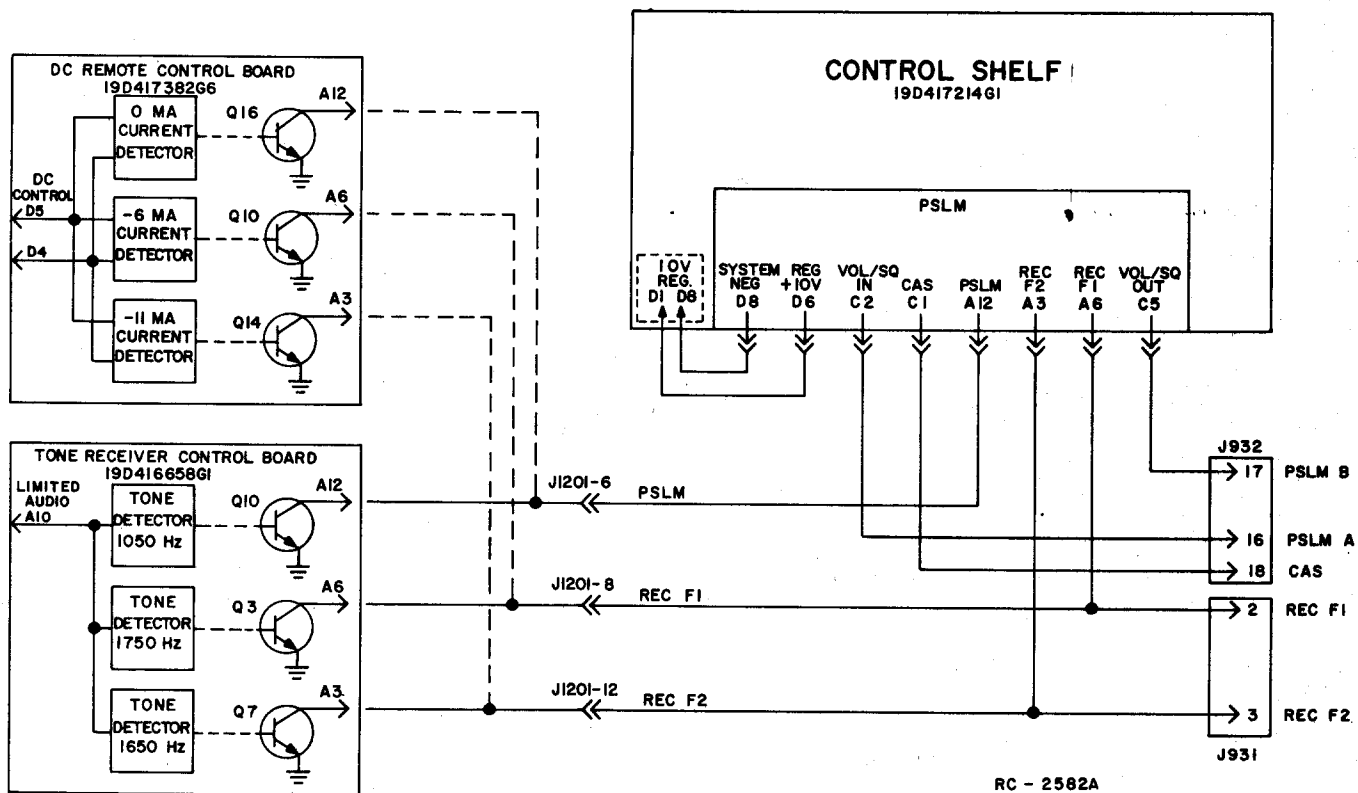


Figure 2 - Remote Switching Diagram

When 0 mA's of current for DC Control (or a tone of 1050 Hz for Tone Control) is present on the control line, this current (or tone) is detected and Q16 (or Q10) is turned on. This removes the ground from either receiver oscillator and applies ground to the PSLM. This activates the PSLM which alternately switches ground to each of the receiver oscillators at a rate of four times per second. If a signal is received on either channel, the PSLM will lock on that channel for the duration of the message, or until a signal is received on the priority channel.

NOTE

The PSLM is normally strapped for F1 priority. To change or disable the priority function, refer to notes 1, 2 and 3 on the Schematic Diagram for the PSLM.

CIRCUIT ANALYSIS

The Priority Search-Lock Monitor is fully transistorized, using both discrete components and integrated circuit modules (IC's) to achieve maximum reliability. Discrete components are used in the Master Pulse Generator, Regulator, Priority Sample One-Shot, Channel Switches and Priority Channel Indicator. IC's are used in the logic circuitry with a hybrid circuit used for audio muting and squelch control.

References to symbol numbers mentioned in the following text may be found on the Outline Diagram, Schematic Diagram and Parts List (see Table of Contents).

The input supply voltage for the PSLM is provided by the 10 Volt regulator on the Control Shelf. This 10 Volts feeds the 5 Volt Regulator on the PSLM board which supplies voltage for all the circuits on the PSLM board. Q9 is used as a switch to turn the PSLM on and off. Q9 is turned on when the PSLM lead A12 is grounded.

MASTER PULSE GENERATOR

The heart of the PSLM is the Master Pulse Generator. The pulse generator is made up of Q2 and Q3 which form a transistor pair that operates like a unijunction transistor. The pulse generator produces negative going pulses at 125 milliseconds or 250 milliseconds intervals. Capacitor C1 is charged thru R4 to give a 250 ms timing pulse. When Q1 is

off, R3 also charges C1 thru CR3, giving a shorter timing period of 125 ms. The 125 ms pulse is used to drive Clock Gate 1 U1D and the 250 ms pulse is used to drive Clock Gate 2 U1B which provide the timing pulses required for the different modes of operation. The PSLM sample rates and times discussed in the different modes of operation were selected to assure the reception of the first syllable of a message received on either channel, and to assure full intelligibility of messages received on the non-priority channel.

MODES OF OPERATION

Operation of the PSLM can be divided into three different modes. The three modes are:

- Receiver squelched
- Receiving priority channel
- Receiving non-priority channel

RECEIVER SQUELCHED

When the receiver is squelched (no signal applied), the PSLM alternately monitors each channel four times per second for a duration of 125 milliseconds. Associated timing waveforms for this mode of operation are shown in Figure 3.

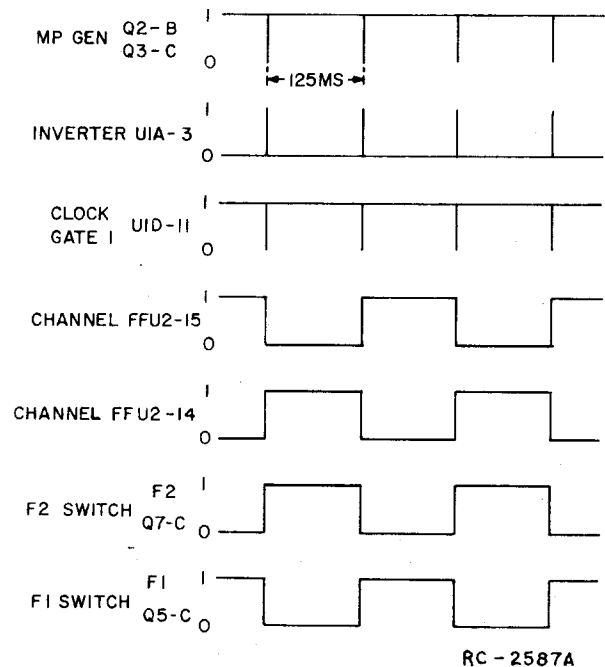


Figure 3 - Receiver Squelched Waveforms

NOTE

Logical "0" is less than +1.0 Volts. Logical "1" is greater than +2.5 Volts.

When the PSLM operation is selected a logical "0" is placed on the A12 lead which turns on Q9 and the Master Pulse Generator. Q2 and Q3 conduct every 125 milliseconds delivering a sharp negative pulse (logical "0") to inverter U1A-1. The inverter converts the logical "0" pulse to a logical "1" pulse which is fed to Clock Gate 1 U1D-12. Clock Gate 1 U1D also has a logical "1" on pin 13 because the CAS lead (C1) is at logical "0" which keeps Q4 turned off providing a continuous logical "1" at the collector of Q4 or pin 13 of U1D. With both inputs to clock Gate 1 at logical "1" the gate feeds a logical "0" pulse to the Channel FF U2-1 from the control of the Master Pulse Generator. The Channel FF is triggered every 125 milliseconds and alternately turns on F1 switch Q5 and F2 switch Q7. When turned on Q5 or Q7 provides a ground to the associated receiver ICOM to monitor that channel during the time it is being searched. The PSLM will continue switching until a signal un-squelches the receiver.

The Clock Gate 2 is held off by the logical "0" on the CAS lead. This keeps the Priority Sample One-Shot from operating since no pulses can get through U1B.

The Priority Channel Indicator CR6 is turned on and off at the same rate as the channels are being searched. A logical "0" on the base turns on Q6 forward biasing light emitting diode CR6.

RECEIVING PRIORITY CHANNEL

When a signal is received on the priority channel, the PSLM locks on that channel for the duration of the message.

Assume that F1 is the priority channel. Receiving a signal on the F1 channel unsquelches the receiver and the CAS lead goes to logical "1". A logical "1" on the CAS lead turns on Q1 and C1 is charged only through R4 to make Q2 and Q3 conduct every 250 milliseconds. Inverter U1A converts the logical "0" pulse from Q2 and Q3 to a logical "1" pulse to Clock Gate 1 (U1D-12). The logical "1" on the CAS lead also turns on Q4 placing a logical "0" on Clock Gate 1 (U1D-13). Clock Gate 1 (U1D) is now inhibited because of the logical "1" and "0" on the two inputs. The output of U1D will remain a logical "1".

Clock Gate 2 (U1B) is also inhibited because Q5, the priority channel switch, is conducting providing a logical "0" to U1B-5 through CR1. The output of U1B will remain a logical "1".

With Gates 1 and 2 inhibited the PSLM remains locked on the F1 channel until the message is completed (receiver squelches).

RECEIVING NON-PRIORITY CHANNEL

When a signal is received on the non-priority channel, the PSLM stops on that channel while switching to the priority channel four times per second for a duration of six milliseconds each time. If a signal is received on the priority channel while receiving the non-priority channel, the PSLM will revert from the non-priority channel and lock on the priority channel for the duration of the message. Timing waveforms for this mode of operation are shown in Figure 4.

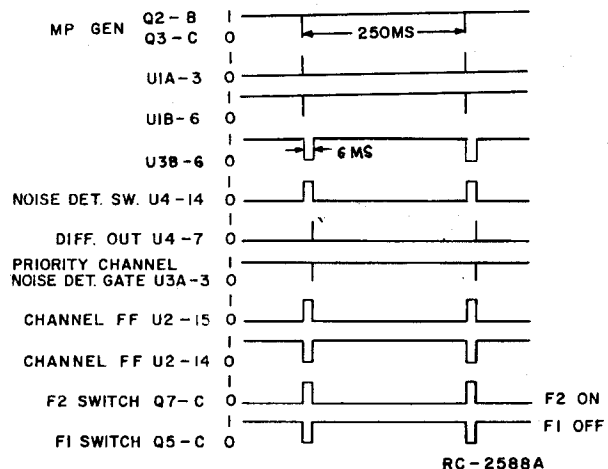


Figure 4 - Receiving Non-Priority Channel Waveforms

Assume that F2 is the non-priority channel. Receiving a signal on the F2 channel unsquelches the receiver and the CAS lead goes to logical "1". A logical "1" on the CAS lead turns on Q1 and C1 is charged only through R4 to make Q2 and Q3 conduct every 250 milliseconds. Inverter U1A converts the logical "0" pulse from Q2 and Q3 to a logical "1" pulse to Clock Gate 1 (U1D-12). The logical "1" on the CAS lead also turns on Q4 placing a logical "0" on Clock Gate 1 (U1D-13). Clock Gate 1 (U1D) is now inhibited because of the logical "0" on the input. The output of U1D will remain a logical "1".

Clock Gate 2 (U1B) with a logical "1" on U1B-5 from the CAS lead and a logical "1" pulse on U1B-4 from the inverter U1A provides a logical "0" pulse to U5-2. This triggers the Priority Sample One-Shot U5. A six millisecond logical "1" pulse is applied from U5-3 to the Audio Muting/Coupling of PSLM Hybrid U4-2.

In the audio Muting/Coupling circuit, audio and noise from the MASTR II receiver comes in on P12-C2 and is connected to pin 3 of the PSLM Hybrid U4, goes through the Audio Muting/Coupling and then goes from U4-4 to P12-C5 which is connected to Volume/Squelch high on the station combination. The Volume/Squelch HI lead is "broken" and the PSLM is inserted.

The six millisecond logical "1" pulse comes in to U4-2 to mute the Audio Muting/Coupling path for eight milliseconds, shunting the receiver audio and noise to ground. This prevents an objectionable noise burst from being heard at the speaker each time the priority channel is monitored (every 250 milliseconds).

At the same time the audio is muted, U5 applies a logical "1" to Inverter U3B. Inverter U3B converts the logical "1" to a logical "0" of 6 milliseconds duration. This six milliseconds logical "1" is applied to differentiator and noise mute circuit in PSLM Hybrid U4 Pin 9. Also, the logical "0" switches Channel Flip Flop U2 to the priority channel.

The fast squelch circuit consists of Noise Mute, Noise Filter, Noise Amp, and Noise Detector switch inside PSLM Hybrid U4. When the priority channel is not being monitored, audio and noise applied to the fast squelch circuit is normally shunted to ground by the noise Mute Circuit. When Channel Flip Flop U2 is switched to the priority channel via the output of U3B, the six millisecond logical "0" turns off the Noise Mute Circuit to pass the noise through the Noise Filter to the Squelch Adjust potentiometer R16 (Instructions for setting R16 are listed in the Table of Contents). The noise is amplified in the Noise Amp and fed to the Noise Detector Switch. The Noise Detector Switch supplies a logical "1" to the input of Priority Channel Noise Detect Gate U3A-2.

The Differentiator converts the six millisecond logical "0" to a logical "1" pulse on the trailing edge of the six millisecond logical "0" pulse. This logical "1" is fed to the Priority Channel Noise Detect Gate U3A-1. The two logical "1"'s on the input of the Priority Channel Noise Detect Gate U3A are converted to a logical "0" which is fed

to Channel Flip Flop U2-3. The logical "0" triggers the Channel Flip Flop causing it to switch back to the non-priority channel. The entire cycle is repeated every 250 milliseconds until a signal is received on the priority channel.

If a signal is received on the priority channel, the signal quiets the receiver. With the receiver quieted, there is a lack of noise to operate the fast squelch circuit so that the Noise Detector Switch provides a logical "0" to block the Priority Channel Noise Detect Gate U3A-2. With this gate blocked the Channel Flip Flop remains locked on the priority channel for the duration of the signal.

Priority Channel Indicator CR6 will flash on for 6 milliseconds and off for 250 milliseconds when receiving messages on the non-priority channel. Since a message is being received on the non-priority channel a logical "1" is applied to the base of Q6 keeping Q6 and Priority Channel Indicator CR6 off. However, when the priority channel is searched a 6 millisecond logical "0" pulse is applied to the base of Q6 turning Q6 and CR6 on for the duration of the search (6 milliseconds).

PRIORITY DISABLE

The PSLM can also be modified to operate without priority for either channel. To disable the priority function of the PSLM and revert to Search-Lock Monitor operation, remove C2 and C9.

VOLTAGE REGULATOR

The Voltage Regulator CR7 provides +5.0 Volts to the PSLM circuits. Transistor Q9 is a DC switch. DC Switch Q9 is turned on by grounding the PSLM lead A12.

MAINTENANCE

DISASSEMBLY

To service the PSLM Board turn off the power switch on the Base Station Power Supply and unplug the PSLM Board. The PSLM Board normally plugs into the J1212 position on the Control Shelf.

TROUBLESHOOTING

To troubleshoot the PSLM Board remove the power as described above and unplug the PSLM Board. Plug the PSLM Board into the extender board (19D417458G1). The extender board extends the connections at the system board jacks to the pin jacks on the PSLM

Board so that the PSLM circuits on the card are beyond other card mounted on the system board. This allows convenient access to the circuits for troubleshooting with all operating voltages applied.

SYSTEM MODIFICATION

Modifications are required in the MASTR II Station Combination when the priority Search-Lock Monitor options are installed. Refer to the Modification Drawing 19D417613 and Interconnection Drawing 19C320972.

Priority Squelch Adjust R16 was set at the factory for 20 dB quieting sensitivity on the priority channel, and will normally require no further adjustment. If it should become necessary to set R16, use one of the following procedures. Procedure A requires two signal generators (803A or equivalent) with a three way 6 dB pad. Procedure B requires a signal generator (803A or equivalent) with a 6 dB pad. Use the extender board (19C317762G1) to extend the PSLM board out so the Priority Squelch R16 can be adjusted.

PROCEDURE A

Before starting Procedure A, make sure that the receiver is properly aligned with the PSLM disabled (PSLM switch in the off position). Then measure and record the F1 (or priority channel) 20 dB quieting sensitivity.

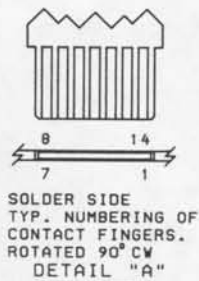
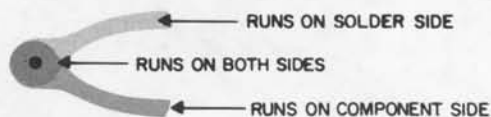
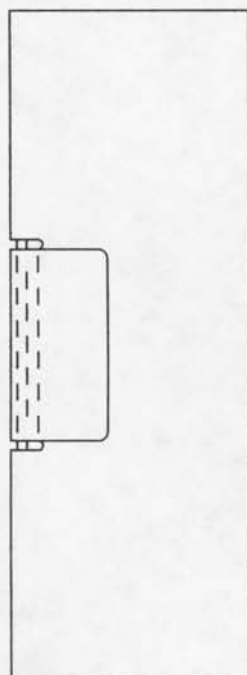
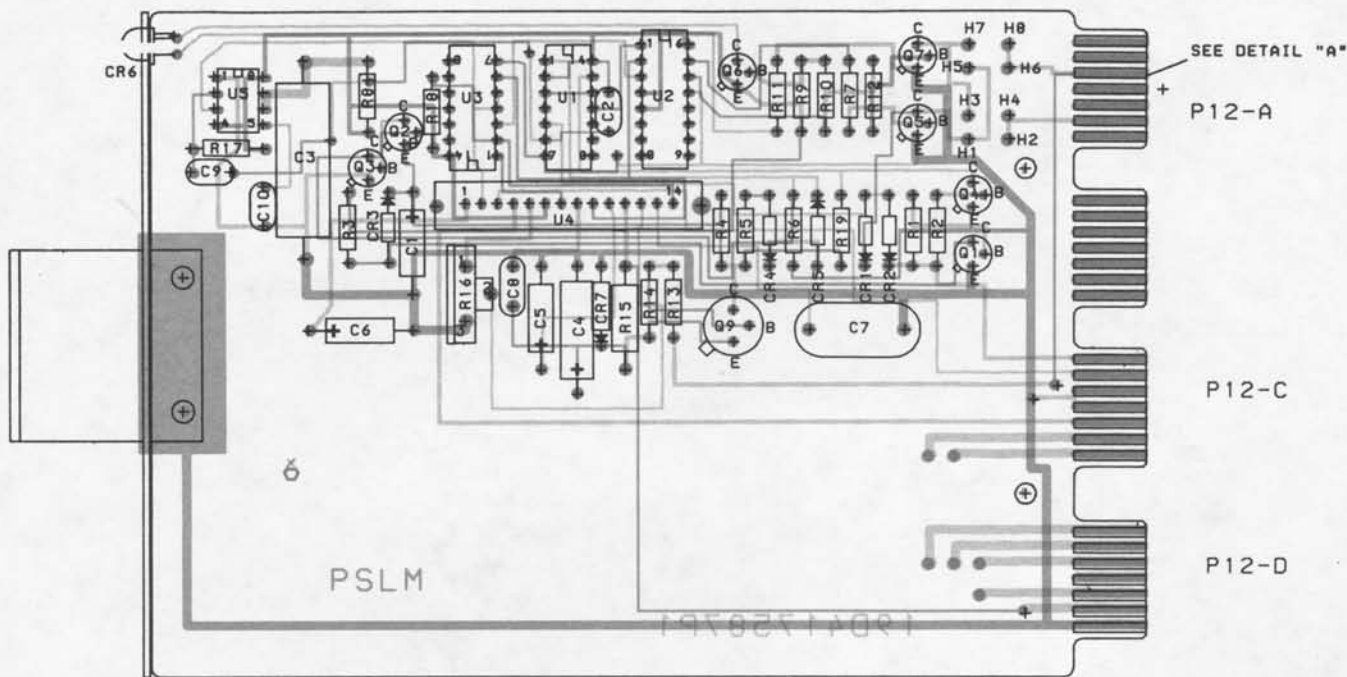
1. In local/remote stations push the PSLM switch. Set Priority Squelch Adjust R16 fully clockwise.
2. Set the receiver squelch at critical squelch. Apply a 100 microvolt signal from generator #2, with standard modulation, to Channel 2. Also apply a 20 dB quieting level modulated signal from generator #1 to Channel 1. Slowly turn the priority squelch adjust R16 counterclockwise until the PSLM locks on Channel 1 (priority channel). This will be shown by a steady flow of LED CR6 on the front panel.

PROCEDURE B

1. In local/remote stations, push the PSLM switch.
2. With the receiver squelched, apply a 100 microvolt signal on Channel 2 (non-priority channel).
3. Turn R16 fully counterclockwise, causing the receiver to false (a repeated thumping noise is heard in the speaker).
4. Carefully turn R16 clockwise until the falsing stops. Then continue turning R16 clockwise for an additional 15 to 20 percent of rotation.



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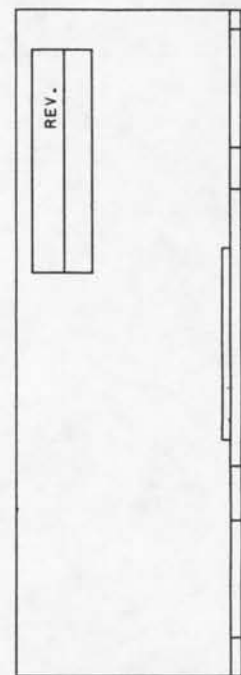


LEAD IDENTIFICATION
FOR Q1 - Q9



TRIANGULAR
TOP VIEW

NOTE: LEAD ARRANGEMENT, AND NOT
CASE SHAPE, IS DETERMINING
FACTOR FOR LEAD IDENTIFICATION.

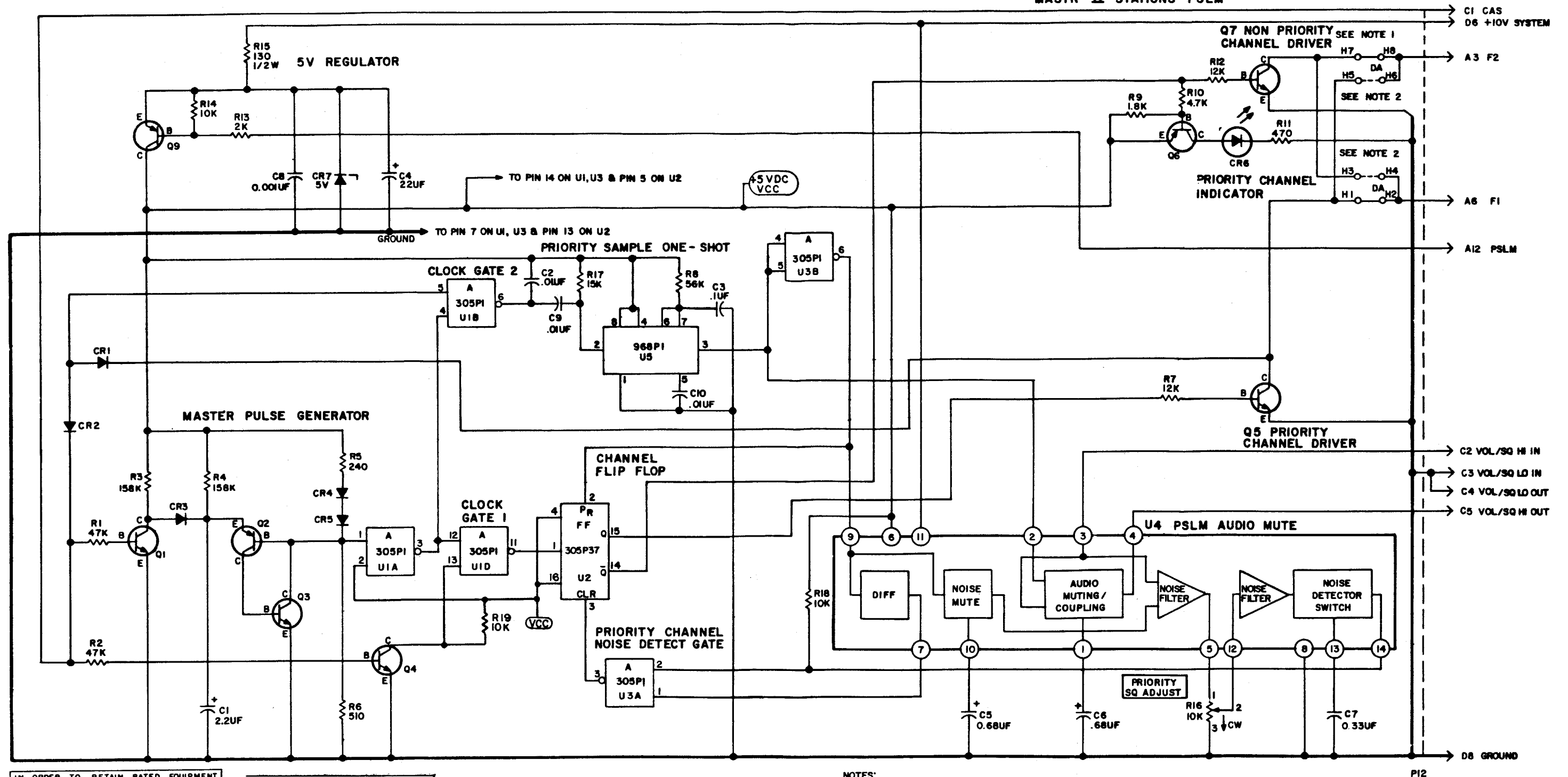


OUTLINE DIAGRAM

PRIORITY SEARCH-LOCK MONITOR

(19D417901, Rev. 3)
(19B226284, Sh. 1, Rev. 6)
(19B226284, Sh. 2, Rev. 6)

MASTR II STATIONS PSLM

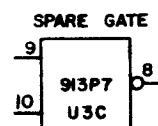


IN ORDER TO RETAIN RATED EQUIPMENT PERFORMANCE, REPLACEMENT OF ANY SERVICE PART SHOULD BE MADE ONLY WITH A COMPONENT HAVING THE SPECIFICATIONS SHOWN ON THE PARTS LIST FOR THAT PART.

ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY K=1000 OHMS OR MEG=1,000,000 OHMS. CAPACITOR VALUES IN PICOFARADS (EQUAL TO MICROMICROFARADS) UNLESS FOLLOWED BY UF= MICROFARADS. INDUCTANCE VALUES IN MICROHENRYS UNLESS FOLLOWED BY MH= MILLIHENRYS OR H= HENRYS.

SEE APPLICABLE PRODUCTION CHANGE SHEETS IN INSTRUCTION BOOK SECTION DEALING WITH THIS UNIT, FOR DESCRIPTION OF CHANGES UNDER EACH REVISION LETTER.

THIS ELEM DIAG APPLIES TO
MODEL NO PL19A130107G A
PL19D417588G1 D



NOTES:

- FOR F1 TO BE THE PRIORITY CHANNEL, JUMPERS SHOULD BE PRESENT BETWEEN H1 AND H2 AND BETWEEN H7 AND H8.
- FOR F2 TO BE THE PRIORITY CHANNEL, JUMPERS SHOULD BE PRESENT BETWEEN H3 AND H4 AND BETWEEN H5 AND H6.
- TO DISABLE PRIORITY FUNCTION OF PSLM AND REVERT TO SEARCH LOCK MONITOR, REMOVE C2 AND C9.

SCHEMATIC DIAGRAM

PRIORITY SEARCH-LOCK MONITOR

Issue 7

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PARTS LIST

LBI4692E
PRIORITY SEARCH LOCK MONITOR BOARD
19A130107G1

SYMBOL	GE PART NO.	DESCRIPTION
A1		COMPONENT BOARD 19D417588G1 REV. C
		----- CAPACITORS -----
C1	5496267P413	Tantalum: 2.2 uF $\pm 5\%$, 20 VDCW; sim to Sprague Type 150D.
C2	19A700005P7	Polyester: 0.01 uF $\pm 10\%$, 50 VDCW.
C3	19C300075P10002G	Polyester: .1 uF $\pm 2\%$, 100 VDCW; sim to GE Type 61F.
C4	5496267P10	Tantalum: 22 uF $\pm 20\%$, 15 VDCW; sim to Sprague Type 150D.
C5	5496267P29	Tantalum: 0.68 uF $\pm 20\%$, 35 VDCW; sim to Sprague Type 150D.
C6*	5496267P229	Tantalum: 0.68 uF $\pm 10\%$, 35 VDCW; sim to Sprague Type 150D.
		In 19D417588G1 earlier than REV A:
	19A116080P10	Polyester: 0.33 uF $\pm 20\%$, 50 VDCW.
C7	19A116080P110	Polyester: 0.33 uF $\pm 10\%$, 50 VDCW.
C8	5494481P111	Ceramic disc: 1000 pF $\pm 20\%$, 1000 VDCW; sim to RMC Type JF Discap.
C9 and C10	19A700005P7	Polyester: 0.01 uF $\pm 10\%$, 50 VDCW.
		----- DIODES AND RECTIFIERS -----
CR1 thru CR5	19A115250P1	Silicon, fast recovery, 225 mA, 50 PIV.
CR6	162B3011P0002	Diode, optoelectronic: red; sim to Hew. Packard 5082-4650.
CR7	4036887P56	Zener: 500 mW, 5.0 v. nominal.
		----- PLUGS -----
P12		Part of printed board 19D417587P1.
		----- TRANSISTORS -----
Q1	19A700023P1	Silicon, NPN; sim to Type 2N3904.
Q2	19A700022P1	Silicon, PNP; sim to Type 2N3906.
Q3 thru Q5	19A700023P1	Silicon, NPN; sim to Type 2N3904.
Q6	19A700022P1	Silicon, PNP; sim to Type 2N3906.
Q7	19A700023P1	Silicon, NPN; sim to Type 2N3904.
Q9	19A115562P2	Silicon, PNP; sim to Type 2N2904A.
		----- RESISTORS -----
R1 and R2	19A700106P103	Composition: 47K ohms $\pm 5\%$, 1/4 w.
R3 and R4	19A701250P420	Metal film: 158K ohms $\pm 1\%$, 1/4 w.
R5	3R152P241J	Composition: 240 ohms $\pm 5\%$, 1/4 w.
R6	3R152P511J	Composition: 510 ohms $\pm 5\%$, 1/4 w.
R7	19A700106P89	Composition: 12K ohms $\pm 5\%$, 1/4 w.
R8*	19A700106P105	Composition: 56K ohms $\pm 5\%$, 1/4 w.
		In 19A130107G1 earlier than REV A:
	19C314256P26812	Metal film: 68.1K ohms $\pm 1\%$, 1/4 w.

SYMBOL	GE PART NO.	DESCRIPTION
R9	19A700106P89	Composition: 1.8K ohms $\pm 5\%$, 1/4 w.
R10	19A700106P79	Composition: 4.7K ohms $\pm 5\%$, 1/4 w.
R11	19A700106P55	Composition: 470 ohms $\pm 5\%$, 1/4 w.
R12	19A700106P89	Composition: 12K ohms $\pm 5\%$, 1/4 w.
R13	3R152P202J	Composition: 2K ohms $\pm 5\%$, 1/4 w.
R14	19A700106P87	Composition: 10K ohms $\pm 5\%$, 1/4 w.
R15	3R77P131J	Composition: 130 ohms $\pm 5\%$, 1/2 w.
R16	19B209358P106	Variable, carbon film: approx 300 to 10K ohms $\pm 10\%$, 1/4 w; sim to CTS Type X-201.
R17	19A700106P91	Composition: 15K ohms $\pm 5\%$, 1/4 w.
R18	19A700106P87	Composition: 10K ohms $\pm 5\%$, 1/4 w.
R19	H212CRP310C	Deposited carbon: 10K ohms $\pm 5\%$, 1/4 w.
		----- INTEGRATED CIRCUITS -----
U1	19A700037P356	Digital: QUAD, 2-INPUT POSITIVE NAND GATE.
U2	19A700037P337	Digital: DUAL J-K FLIP-FLOP WITH PRESET & CLEAR.
U3	19A700037P301	Digital: QUAD, 2-INPUT POSITIVE NAND GATE; 74LS00.
U4	19D424078G1	Hybrid: Mute PSLM.
U5	19A116968P1	Linear, timer: DUAL IN-LINE 8 Pin Mini Dip Package; sim to Signetics SA555N.
		----- MISCELLANEOUS -----
	19A701332P4	Insulator, washer: nylon. (Used with Q9).
	19B219690G1	Handle assembly.

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by these revisions.

REV A - PRIORITY SEARCH LOCK MONITOR BOARD 19A130107G1
To increase priority sample time, changed R8.

REV A - COMPONENT BOARD 19D417588G1
To reduce the audio "thump" when receiving non-priority channel, changed C6.

REV B - COMPONENT BOARD 19D417588G1
To increase the audio level when the PSLM control unit is used, changed U4.

REV C - COMPONENT BOARD 19D417588G1
Changed DTL IC's to TTL LS. Deleted Q8, added U5.

REV D - COMPONENT BOARD 19D417588G1
To prevent flip-flop from possibly not changing correctly, added R19 and changed U1.

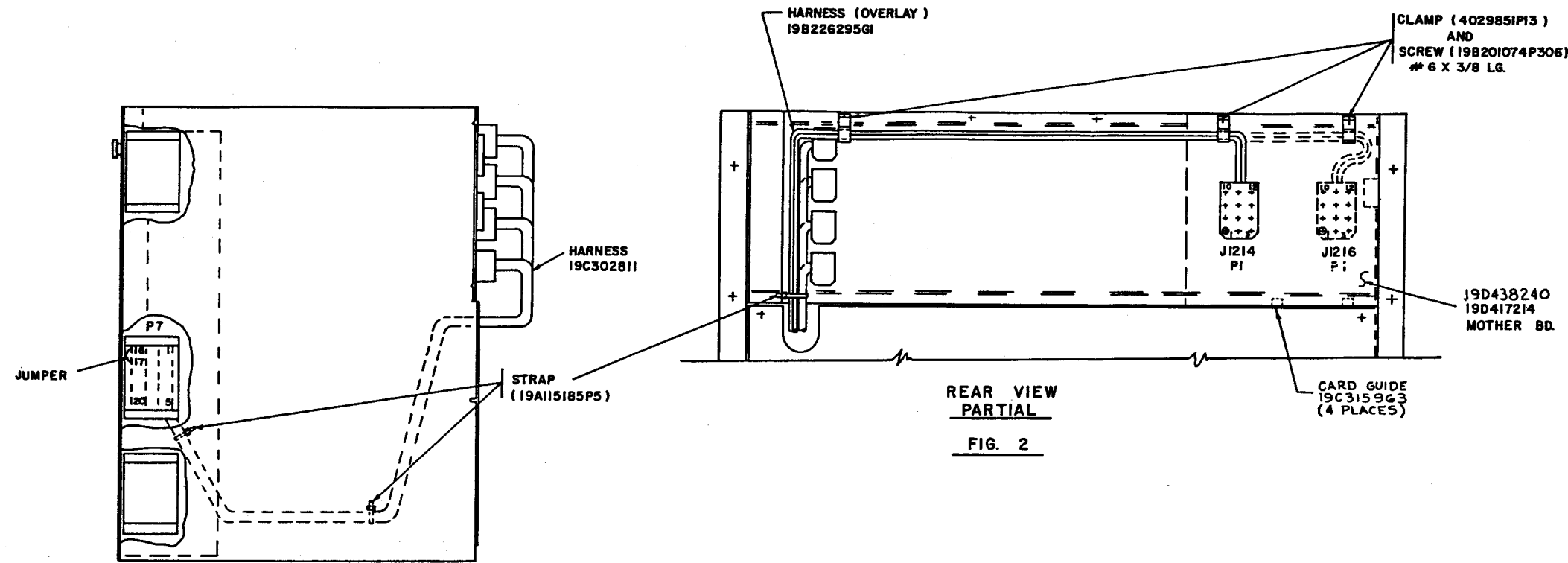
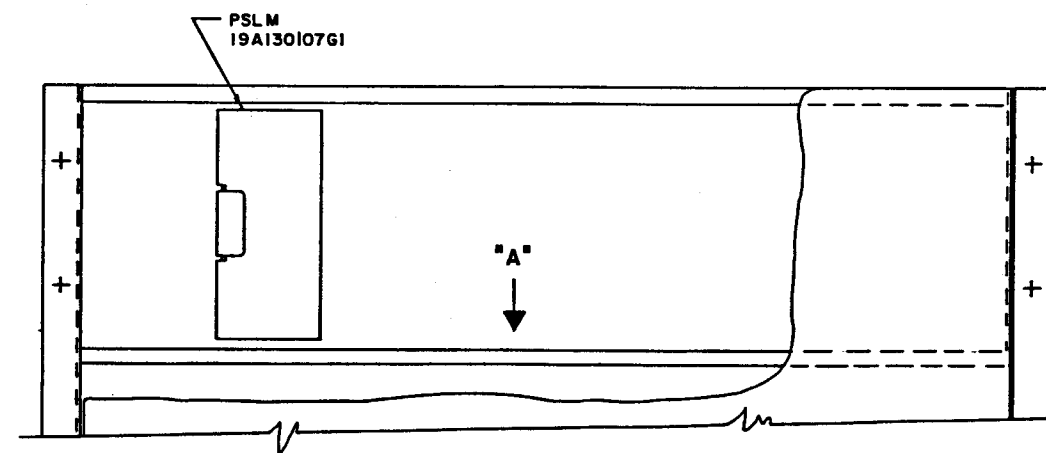
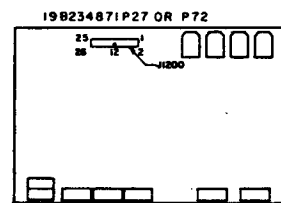


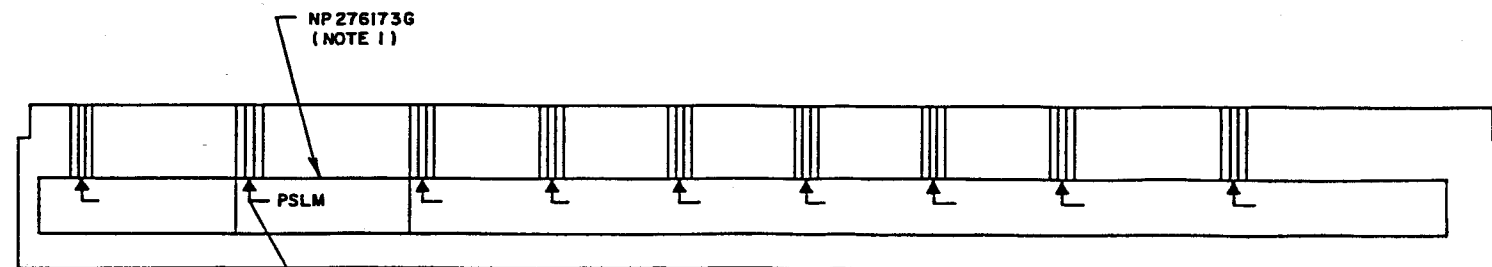
FIG. 1

REAR VIEW
PARTIAL

FIG. 2



FRONT VIEW
CONTROL SHELF



VIEW AT "A"

THESE INSTRUCTIONS COVER THE MODIFICATION OF THE CONTROL SHELF FOR INSTALLATION OF THE PSLM BOARD.

INSTRUCTIONS:

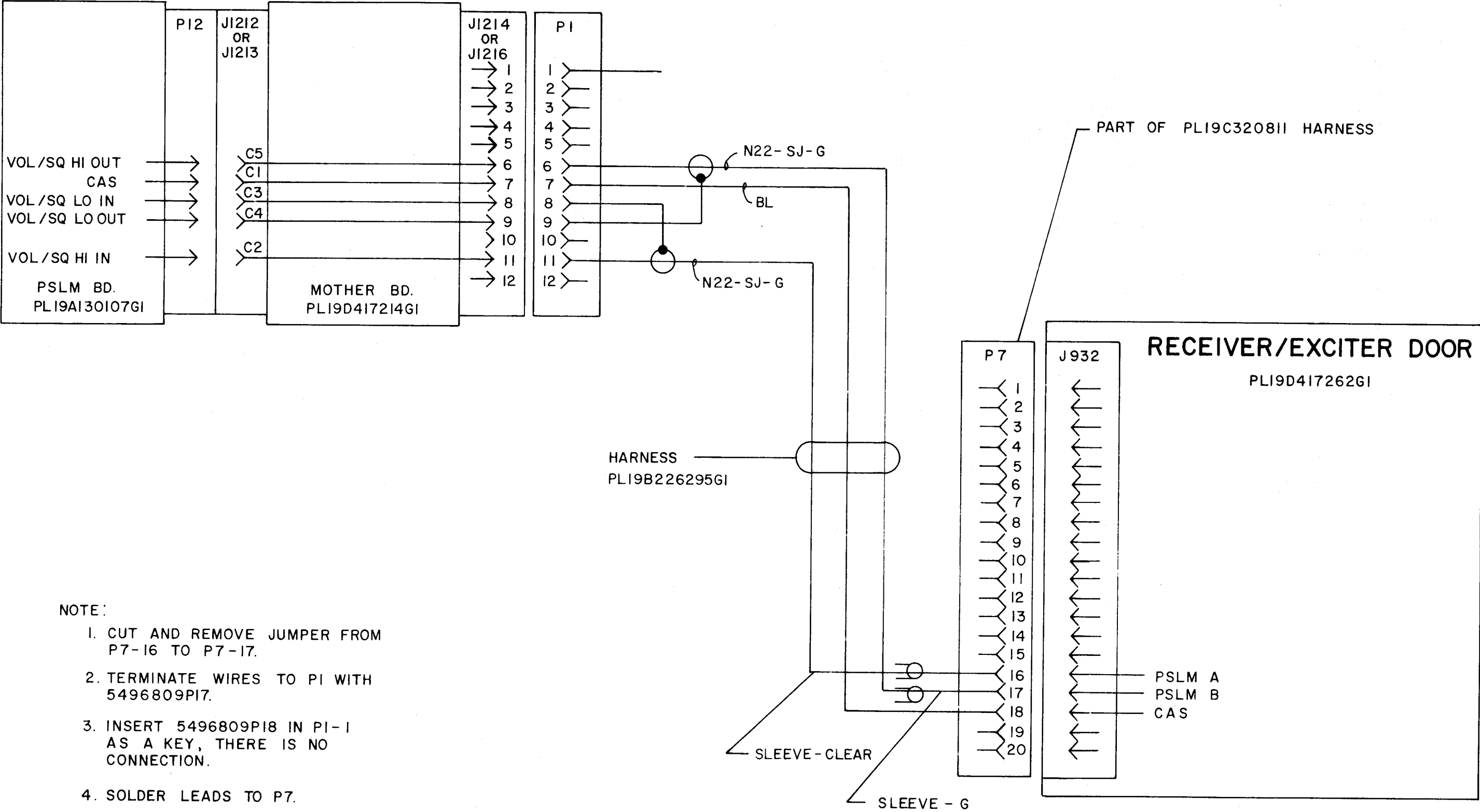
1. MOUNT 19D438240 BACKPLANE IF 19D417214 NOT PRESENT.
 - A. CUT OFF J1200-12.
 - B. CONNECT 19B234871 CABLE FROM 19D438240 J1218/J1219 TO 19B234871 PANEL J1200.
2. AFFIX NAMEPLATE NP276173G TO SHELF AS SHOWN IN FRONT OF SLOT IN WHICH PSLM IS TO BE INSTALLED.
3. INSTALL PSLM IN SECOND POSITION FROM LEFT IN SHELF, UNLESS THAT SLOT IS FILLED, IN WHICH CASE THE PSLM IS TO BE INSTALLED IN THE FIRST POSITION ON THE LEFT.
4. INSTALL PSLM OVERLAY HARNESS AS FOLLOWS:
 - A. INSTALL PSLM OVERLAY HARNESS (19B226295G1) AS SHOWN IN FIG. 2. INSTALL P1 OF PSLM OVERLAY HARNESS (19B226295G1) ON J1214 ON COMPONENT BOARD (19D417214) IF PSLM MODULE IS INSTALLED IN SECOND SLOT FROM LEFT IN CONTROL SHELF OR ON J1216 IF PSLM MODULE IS INSTALLED IN FIRST SLOT ON LEFT IN CONTROL SHELF.
 - B. INSTALL CABLE CLAMPS (4029851P13) AS SHOWN IN FIG. 2. REMOVE AND DISCARD THE TWO SCREWS PRESENT AT LOCATIONS WHERE CLAMPS ARE TO BE MOUNTED AND MOUNT CLAMPS USING THE TWO SCREWS (19B201074P306) SUPPLIED.
 - C. INSTALL (19A115185P5) STRAPS THREE PLACES, TO DRESS OVERLAY HARNESS WITH STATION HARNESS (19C302811). SEE FIG. 1 & 2.
 - D. REMOVE AND DISCARD JUMPER BETWEEN P7-16 AND P7-17 OF STATION HARNESS (19C302811). SOLDER CONNECTIONS FROM OVERLAY HARNESS (19B226295G1) (SEE FIG. 2) TO P7 PER INTERCONNECTION DIAGRAM (19C302972).
5. TEST PER 19A129945.

MODIFICATION & INSTALLATION DIAGRAM

MASTR II STATION PSLM

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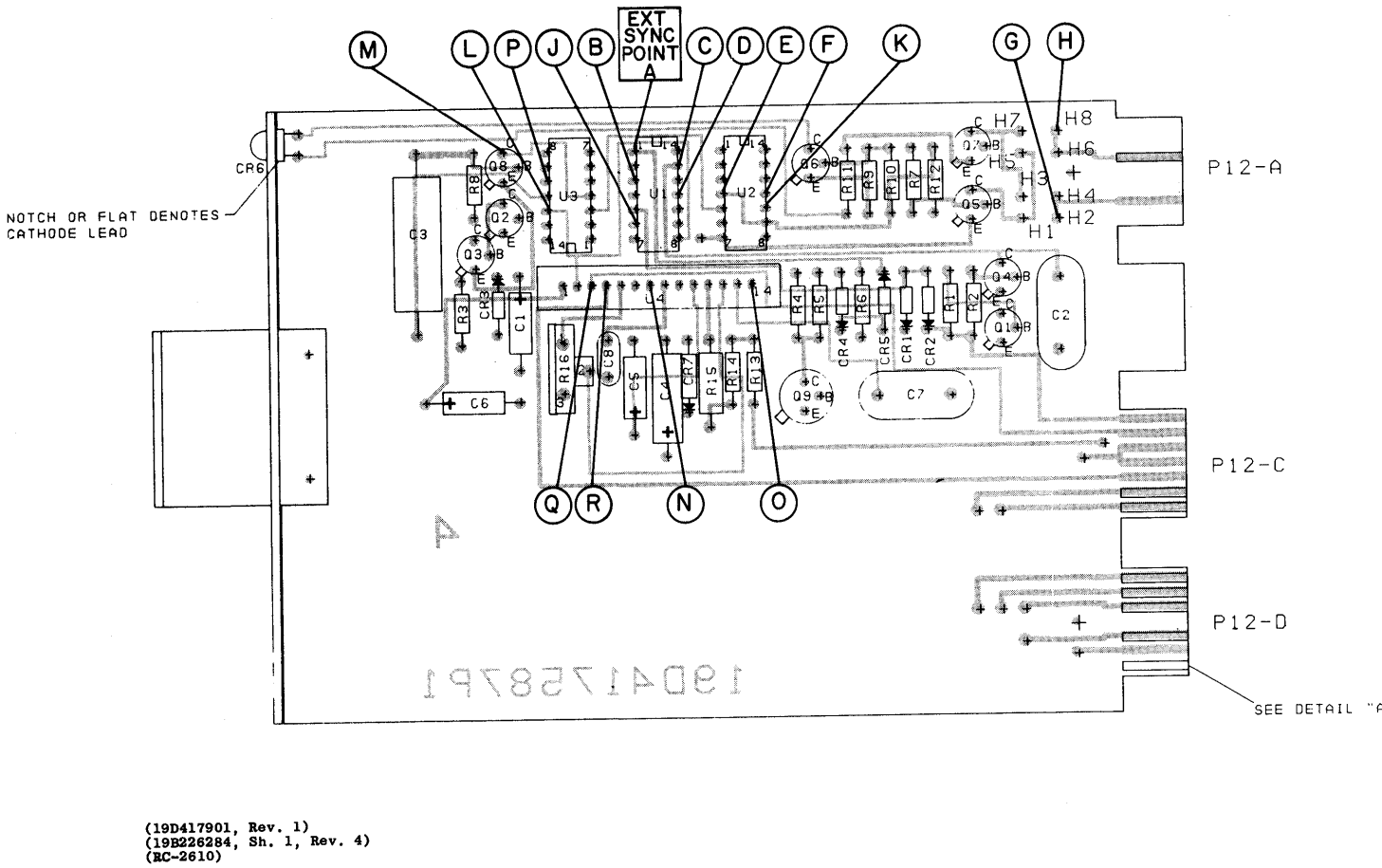


INTERCONNECTION DIAGRAM

MASTR II STATION PSLM

TRoubleshooting Procedure

PRIORITY SEARCH-LOCK MONITOR



TRoubleshooting Procedure

NOTE

The audio quality of the Non-Priority channel can best be checked with an unmodulated carrier or voice modulation. When the PSLM is on the Non-Priority channel, applying a constant tone to the receiver will result in a pulsed sound.

Preliminary Checks

1. Check for a regulated +10 volts DC at D6.
2. Check for +5 volts DC at collector of Q9 (with A12 grounded).

SYMPTOM	PROCEDURE
No receiver audio	<ol style="list-style-type: none">1. Check the receiver in a different system (with or without PSLM).2. Check waveforms at Test Points Q and R.3. Check P1 & P12 on Mother board and other overlay harness connections.4. Check that Receiver Mute circuit is not grounded.
No oscillator activity	Check waveforms at Test Points G and H with search mode disabled. Select F1 or F2 via local control.
Receiver rapidly alternates between F1 and F2 while trying to receive the Non-Priority channel. --- OR --- Obnoxious white noise received on the Non-Priority channel.	<ol style="list-style-type: none">1. Check the setting of Priority Squelch Adjust R16 (see Table of Contents).2. Check waveforms at Test Points Q and R.3. Check system interconnections (refer to Interconnection Diagram in the Maintenance Manual for the Control Unit.)4. Check for defective U4.
Fails to receive Priority channel	<ol style="list-style-type: none">1. Check setting of Priority Squelch Adjust R16 (see Table of Contents).2. Check voltage readings and waveforms at Test Points K, E, B, G, and H.
Incorrect Priority channel	<ol style="list-style-type: none">1. Check system interconnections (refer to Interconnection Diagram in the Control Unit Maintenance Manual).2. Check jumpers. Refer to notes on the wiring diagram.3. Check that F1 and F2 ICMS are not reversed.4. Check voltage readings and waveforms at Test Points E, B, G, and H.
Missed syllables on the first part of transmissions	<ol style="list-style-type: none">1. Check waveform at Test Point A for incorrect sample rate. Pulse Rep rate should be 125 MS with Q1 off; 250 MS with Q1 on.2. Check Station Squelch Control Adjustment.
Fails to receive Non-Priority Channel	In Channel Guard Stations, check the station squelch control setting with C. G. Disabled.
Does not remain on Non-Priority signal with no priority signal present --- OR --- Chops Non-Priority signals --- OR --- Search rate erratic	<ol style="list-style-type: none">1. Check setting of station squelch control.2. Check waveforms at N, Q, and P.

VOLTAGE READINGS

All voltage readings are DC readings measured with a 20,000 ohm-per-volt VOM with reference to system negative (D8). The readings are taken with the PSLM board connected for F1 priority (see Note 1 on the Schematic Diagram).

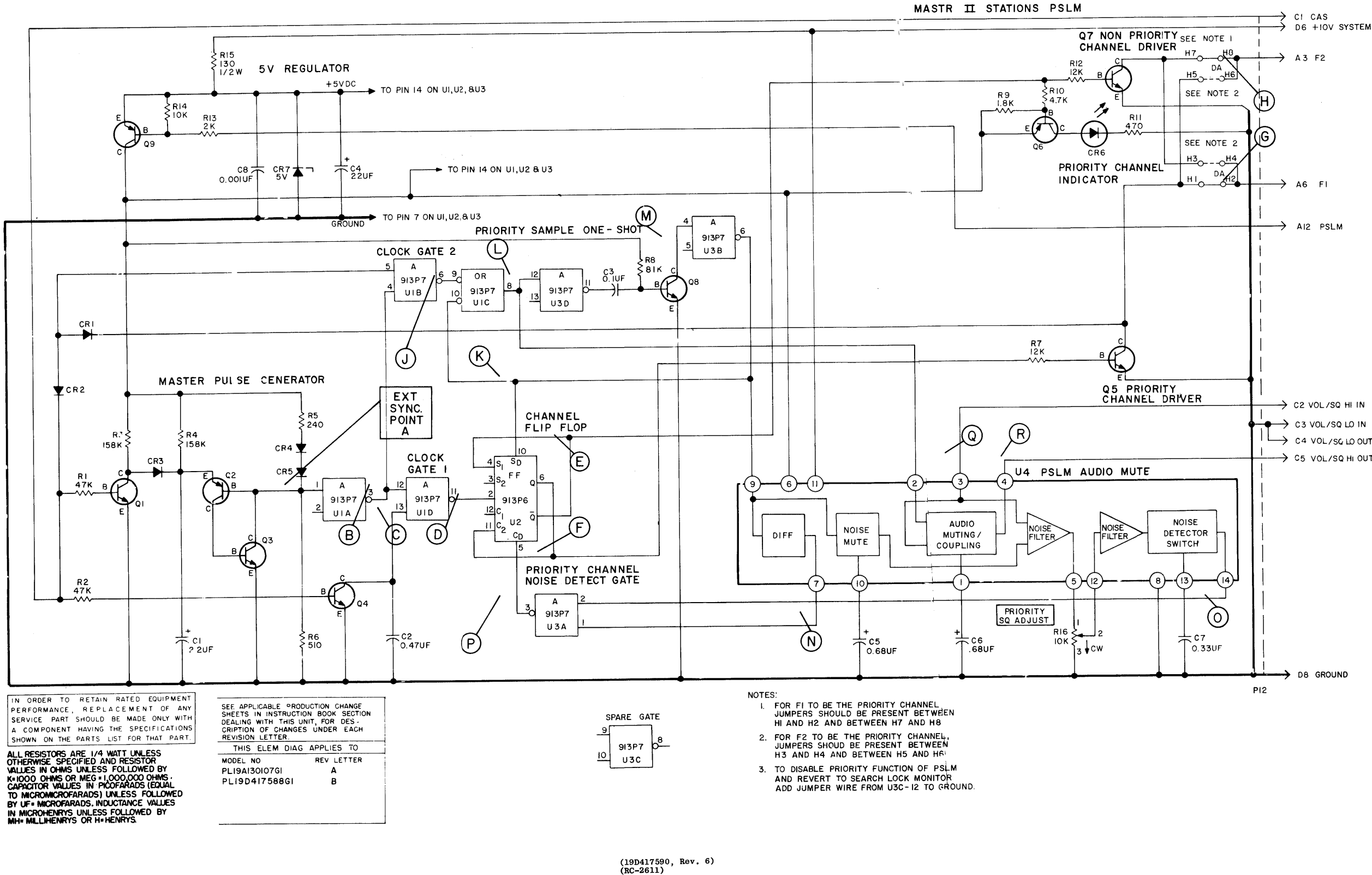
NOTE

Readings followed by a (P) are averages of pulsating meter deflections. These readings may vary widely due to the differences in meter ballistics, but may be used to determine that the circuit is operative (or switching) and not a DC or ground potential.

Preliminary Checks

1. Check for +10 volts at D6.
2. Check for +5 volts at collector of Q9 (with A12 grounded).

Test Point	Reading with Receiver Squelched (No Signal)	Reading with Receiver Receiving Signal on Non-Priority Channel	Reading with Receiver Receiving Signal on Priority Channel
A	2.5V	2.5V	2.5V
B	.15V	.15V	.15V
C	.45V	.05V	.05V
D	4.8V	4.8V	4.8V
E	2.0V (P)	4.0V	.1V
F	1.75V (P)	.2V (P)	3.6V
G	3.0V (P)	5.4V	.6V
H	6.5V (P)	.65V (P)	5.3V
J	4.8V	4.8V	4.8V
K	4.5V	4.5V	4.5V
L	.1V	.1V	.1V
M	.1V	.15V	.15V
N	.65V	.65V	.65V
O	.1V	.1V	.1V
P	4.9V	4.9V	4.9V
Q	4.6V	4.6V	4.6V
R	4.6V	4.6V	4.6V
C1 (CAS)	.1V	7.0V	7.0V
A12 (PSLM)	.05V	.05V	.05V
U4-6	5.0V	5.0V	5.0V
U4-11	10V	10V	10V



WAVEFORMS

All waveforms are taken at Test Points (A) thru (R) as shown in Figures A and B, and are taken with the PSLM board connected for F1 priority (see note 1 of the Schematic Diagram). When applicable, the waveforms are shown for three different modes of operations as follows:

- 1. Receiver Squelched (PSLM Searching)
- 2. Receiver Unsquelched (Receiving Non-Priority Channel)

NOTE

All waveforms are taken using Test Point A as the SYNC SOURCE (Trigger Pulse) except where NOTED.

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL
(A)	50ms/Div. 2V/Div.	50ms/Div. 2V/Div.
(B)	50ms/Div. 2V/Div.	50ms/Div. 2V/Div.
(C)	50ms/Div. .5V/Div.	
(D)	50ms/Div. 1V/Div.	50ms/Div. 1V/Div.
(E)	50ms/Div. 2V/Div.	50ms/Div. 2V/Div.

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL
(F)	50ms/Div. 2V/Div.	50ms/Div. 2V/Div.
(G)	50ms/Div. 2V/Div.	50ms/Div. 2V/Div.
(H)	50ms/Div. 5V/Div.	50ms/Div. 5V/Div.
(J)	50ms/Div. 1V/Div.	50ms/Div. 1V/Div.
(K)	50ms/Div. 1V/Div.	50ms/Div. 1V/Div.
(L)		50ms/Div. 1V/Div.

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL	RECEIVING NON-PRIORITY CHANNEL
(M)		50ms/Div. .5V/Div.	1ms/Div. .5V/Div. PULSE EXPANDED
(N)	50ms/Div. .5V/Div.	50ms/Div. .5V/Div.	1ms/Div. .5V/Div. PULSE EXPANDED
(O)		50ms/Div. .5V/Div.	2ms/Div. .5V/Div. PULSE EXPANDED
(P)	50ms/Div. 1V/Div.	50ms/Div. 1V/Div.	1ms/Div. 1V/Div. PULSE EXPANDED
(Q)	50ms/Div. 1V/Div.	50ms/Div. 1V/Div.	2ms/Div. 1V/Div. PULSE EXPANDED
(R)	50ms/Div. 1V/Div.	50ms/Div. 1V/Div.	2ms/Div. 1V/Div. PULSE EXPANDED

TROUBLESHOOTING PROCEDURE

MASTR II STATION PRIORITY SEARCH-LOCK MONITOR