



1. Theory Of Operation

1.1 LOWBAND RECEIVER

The received signal is applied to the radio's antenna input J1 and routed through the harmonic filter and antenna switch which are located on the PA deck. The signal is then routed via coax to J4 on the RF board and passes through a 4 pole bandpass filter.

The signal then passes through one stage of RF amplification Q1, which has a current source comprised of Q2, Q3, and Q4. This circuitry sets a bias current that does not vary regardless of DC Beta variations on Q1. CR2 located on the input side of Q1 is a protective diode that ensures Q1 will be protected from high level RF signals. The amplified signal then passes through a second 4 pole bandpass filter.

The amplified RF signal is then mixed with the receive VCO signal in the double balanced quad diode mixer, CR1. The desired 10.7 MHz IF signal is then amplified through Q51 and passes through a IF delay line used for extender operation. The 10.7 MHz IF signal proceeds through the extender blanker switches, Q52 and Q53. Q54 provides another stage of IF amplification to the signal.

The 10.7 MHz IF signal then passes through a 4 pole crystal filter. One more stage of amplification Q56, occurs before the IF signal is sent to the receiver subsystem IC, U51.

U51 (see Figure 1) is a complete receiver subsystem and the 10.7 MHz signal is mixed with a 10.245 MHz crystal to produce a 455 kHz second IF signal. The second IF signal is then amplified and filtered by 455 kHz ceramic filters, FL51 and FL52.

The audio detector is internal to the U51 IC. The quadrature detector detects the audio and routs it to the PL filter and carrier squelch amplifier. The carrier squelch amplifier amplifies the detected audio and routs it via U51-8 to the squelch control R70. The squelch control output is routed through a high pass filter to remove the receive audio components. The remaining noise above the audio band is

detected via U51-6 by the carrier squelch detector which generates a DC voltage. This voltage controls the audio mute circuits. The detected audio is then sent to the logic board audio circuitry via U51-5 to J6-3.

1.2 EXTENDER OPERATION

After the first mixer stage CR1, the RF signal passes through post mixer filtering comprised of bandpass selectivity circuits surrounding L51, L52, and L53. First IF amplification is provided by Q51. The IF signal divides at the base of Q51. The extender pulse detector and blanker circuits are fed by one path while the first IF amplifier Q51 is driven by the other.

The first IF amplifier Q51 amplifies the signal where it couples into the IF delay line section comprised of circuits associated with L55 and L56. After the signal passes through the delay line the signal can be blanked with the appropriate signal applied to Q52 and Q53. Post blanker isolation is provided by Q54. The signal then passes into the first 4 pole filtering section of the 10.7 MHz IF.

The Extender samples RF from the base of Q51 and drives the extender isolation amplifier Q351. Q351 in turn amplifies the signal and pulse which is then applied to the gain block U351. Q352 detects the output of U351 for further processing. Pulse shaping and amplification are accomplished by Q353 and Q354. Q355 is driven to toggle Q52 and Q53 in the IF to blank the noise pulse as it exits the IF delay line. The output of Q354 also drives a three stage AGC detector comprised of Q356, Q357, and Q358 which reduces the gain of U351 under large signal and high pulse repetition rate conditions.

1.3 VHF RECEIVER

The received signal is applied to the radio's antenna input and routed through the harmonic filter/ antenna switch. The output is then routed via coax to J4 on the RF board. The input at J4 is matched to a fixed tuned 4 pole filter. The 4 pole filter has a 3 dB bandwidth of 40 MHz and 1 dB bandwidth of 35 MHz centered at about 160 MHz.

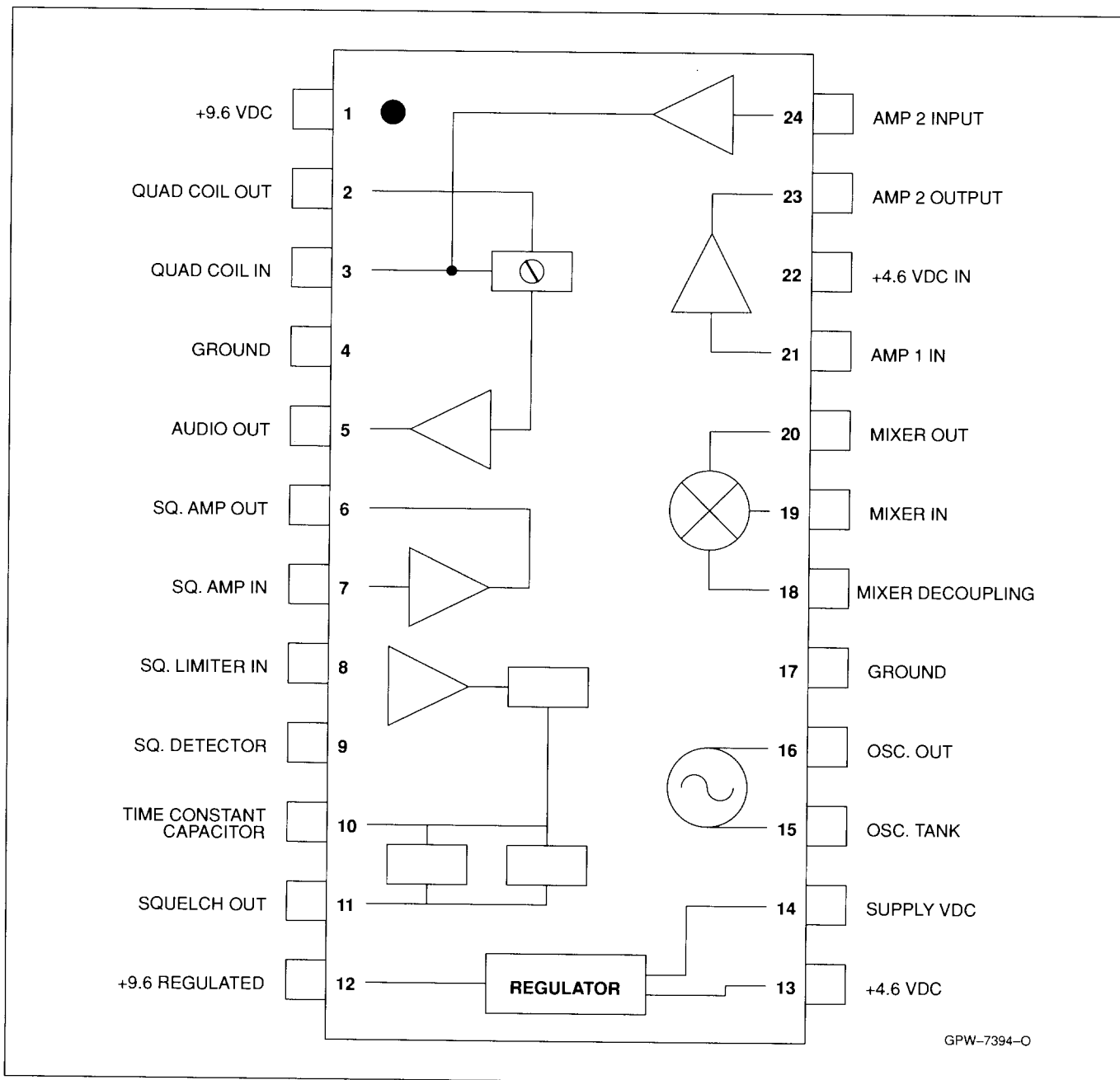


Figure 1. Receiver IC Block Diagram

The output of the filter is matched to the base of RF amplifier Q1. Q1 has a current source, Q2, to set a bias current of 16 mA regardless of DC Beta variations of Q1. The Q1 emitter resistors are used to provide voltage feedback to limit Q1's gain to about 14 dB. CR2, located on Q1's input, is a protective diode that ensures Q1 is protected from high level RF signals.

The output of Q1 is applied to a 3 pole filter centered at about 160 MHz. The first 4 pole filter, RF amplifier and the 3 pole filter provide image spur rejection.

The quad diode mixer, CR1, is a passive double balanced mixer. The output of the mixer goes to the diplexer circuit

which allows the mixer to be matched to the First IF amplifier, Q51, at the IF frequency of 45.1 MHz.

Q51 amplifies the IF signal by approximately 20 dB. The output of Q51 is filtered by matched ceramic filters Y51A and Y51B. The first IF is then amplified by Q52 by approximately 18 dB and sent to the receiver subsystem IC U51-19 (see Figure 1).

The 45.1 MHz first IF signal is applied to the second mixer section of U51. A 44.645 MHz crystal oscillator provides the low side injection signal for the second mixer via U51-19. The second mixer takes the 45.1 MHz and the 44.645 MHz and produces a 455 kHz second IF signal. The second IF

filtering is achieved by using multiple resonators, FL51 and FL52. These filters are tuned to 455kHz.

The audio detector is internal to the U51 IC. The Quadrature detector detects the audio and routs it to the PL filter and to the carrier squelch amplifier. The carrier squelch amplifies the detected audio and routs it via U51-8 to the squelch control R60. The squelch control output is routed through a high pass filter to remove the receive audio components. The remaining noise above the audio band is detected via U51-6 by the carrier squelch detector which generates a D.C. voltage that controls the audio mute circuits. The detected audio is then sent over to the logic board via U51-5/J6-3.

1.4 UHF RECEIVER

The receiver signal is applied to the radio's antenna input and routed through the harmonic filter and antenna switch, which are located on the PA deck. The output is then routed via coax to J4 on the RF board.

The incoming signal at J4 passes through a 3 pole bandpass filter. A stage of RF amplification, Q1, amplifies the signal which passes to a 4 pole bandpass filter. The filtered signal then passes to the first mixer stage, CR1. The voltage controlled oscillator output is fed to the first mixer as a low side local oscillator. The resultant signal of 45.1 MHz is then amplified by the first IF amplifier Q51. Then amplified 45.1 MHz IF signal then passes through a 4 pole crystal filter consisting of Y51A and Y51B. Another stage of amplification, Q52, occurs before the RF signal passes into the receiver subsystem IC, U51 (see Figure 1).

The 45.1 MHz first IF signal is applied to the second mixer section of U51. A 44.645 MHz crystal oscillator provides the low side injection signal for the second mixer via U51-19. Y52 is a 44.645 MHz crystal which feeds the oscillator via U51-15. The second mixer takes the 45.1 MHz and the 44.645 MHz signal and produces a 455kHz second IF signal. The second IF filtering is achieved by using multiple resonators, FL51 and FL52. These filters are tuned to 455kHz.

The audio detector is internal to the U51 IC. The quadrature detector detects the audio and routs it to the PL filter and to the carrier squelch amplifier. The carrier squelch amplifies the detected audio and routs it via U51-8 to the squelch control R60. The squelch control output is routed through a high pass filter to remove the receive audio components. The remaining noise above the audio band is detected via U51-6 by the carrier squelch detector which generates a D.C. voltage that controls the audio mute circuits. The detected audio is then sent over to the logic board via U51-5/J6-3.

1.5 800 MHz RECEIVER

The received signal is applied to the radio's antenna input and routed through the harmonic filter and antenna switch, which are located on the PA deck. The output is then routed via coax to J4 on the RF board.

The incoming signal passes through a bandpass filter, FL1 and then through one stage of RF amplification, Q1. The amplified output of Q1 is then sent through another section of filtering, FL2.

The filtered signal then passes to the first mixer, U1. The voltage controlled oscillator output is fed into the mixer and the resultant 45.1 MHz IF signal is then sent to the first IF amplifier, Q51. The amplified 45.1 MHz signal then passes through a 4 pole crystal filter consisting of Y51A and Y51B. Another stage of amplification, Q52, occurs before the signal passes into the receiver subsystem IC, U51 (see Figure 1).

The 45.1 MHz first IF signal is applied to the second mixer section of U51. A 44.645 MHz crystal oscillator provides the low side injection signal for the second mixer via U51-19. Y52 is a 44.645 MHz crystal which feeds the oscillator via U51-15. The second mixer takes the 45.1 MHz and the 44.645 MHz signals produces a 455 kHz second IF signal. The second IF filtering is achieved by using multiple resonators, FL51 and FL52. These filters are tuned to 455kHz.

The audio detector is internal to the U51 IC. The quadrature detector detects the audio and routs it to the PL filter and to the carrier squelch amplifier. The carrier squelch amplifier amplifies the detected audio and routs it via U51-8 to the squelch control R60. The squelch control output is routed through a high pass filter to remove the receive audio components. The remaining noise above the audio band is detected via U51-6 by the carrier squelch detector which generates a D.C. voltage that controls the audio mute circuits. The detected audio is then sent over to the logic board via U51-5/J6-3.

1.6 SYNTHESIZER OPERATION

Before frequency synthesis can begin the microprocessor must load frequency divider information into the PLL IC U101 (see Figure 2). The PLL IC contains 3 programmable dividers. The program is serially loaded via a common data line U101-10. The data is loaded one bit at a time, with each low-to-high transition of the CLOCK at U101-11 latching data from shift registers into the reference divider (R), divide-by-N, or divide-by-A latches depending on the control bit. A logic of the control bit selects the reference counter latch, while a logic low selects the divide-by-N, or divide-by-A counter latch.

After the microprocessor loads data into the PLL IC, SYNTH LATCH ENABLE line goes low. The synthesizer is then ready to generate a transmit or receive first injection frequency.

As an example for the 800MHz trunk models, the latches are loaded with data to give the following:

12.5 kHz at the output of the divided-by-R counter when the reference oscillator signal is applied at U101-1.

12.5 kHz at the output of the divided-by-N counter when the VCO is operating at the desired receive injection or transmit frequency.

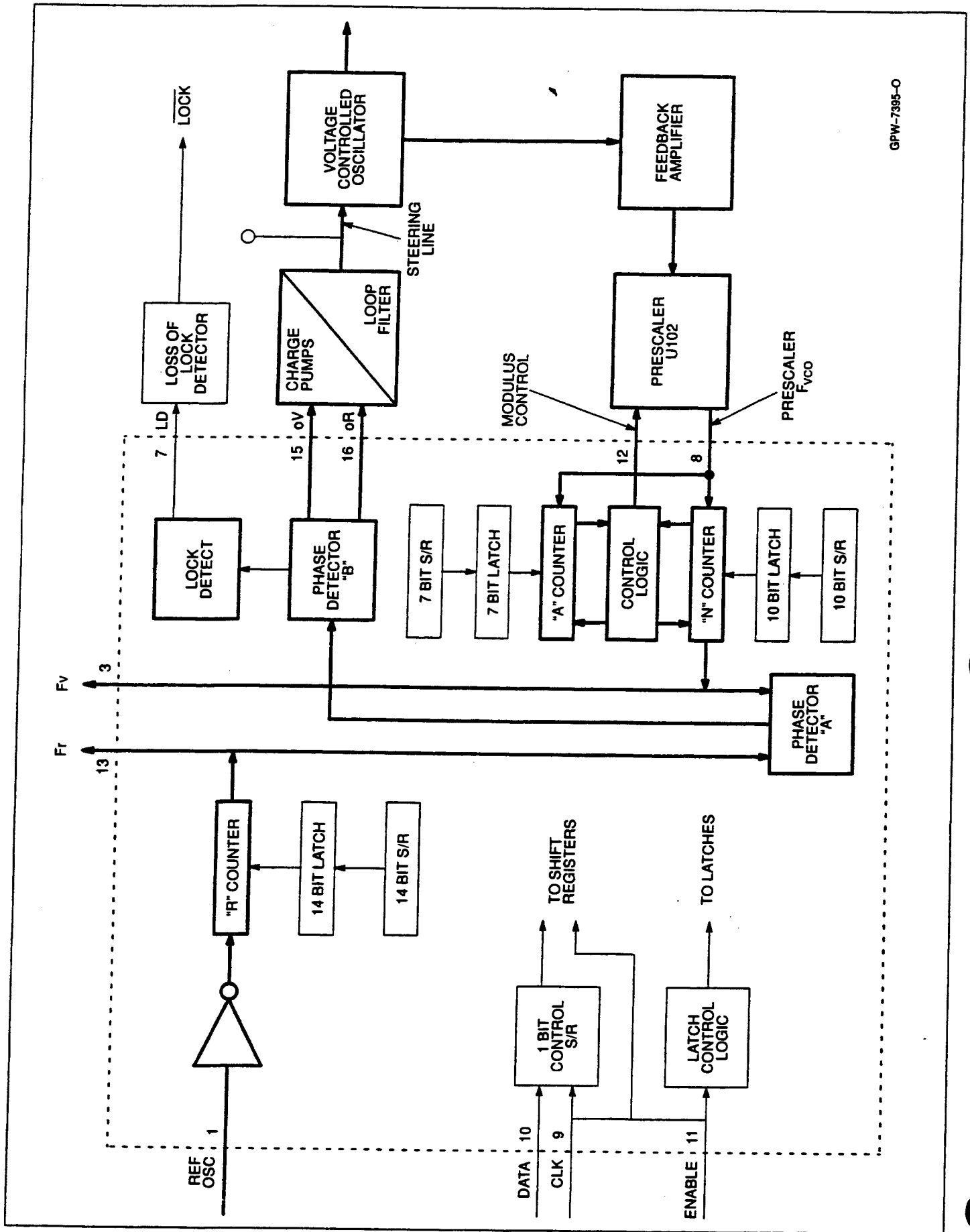


Figure 2. Synthesizer Section Block Diagram

During the frequency synthesis, the divide-by-A and divide-by-N counters begin counting down from the programmed values (A and N respectively) at the same time. The MOD CON line U101-12 is low so the divide-by-127/128 prescaler divides by 128. Therefore, the effect of the prescaler U102 is to divide the VCO output by 128 and apply it to U102-8. When the divide-by-A counter completes counting down, the control logic sets the MOD CON line high, and the divide-by-127/128 prescaler divides by 127 until the divide-by-N counter completes the programmed value on N. After the divide-by-N counter completes counting down, the counters are set back to their programmed values. The MOD CON line is set low and the counters begin counting down again. The effect of the prescaler and divide-by-A, divide-by-N counters is to divide the VCO frequency by a number, N_T , where:

$$N_T = 128 \times A + 127 \times (N - A) \\ = 127 \times N + A$$

The output of the divide-by-N counter is equal to:

$$\frac{f_{VCO}}{127 \times N + A}$$

where f_{VCO} is the output frequency of the VCO

When the phase-locked loop is locked:

$$\frac{f_{VCO}}{127 \times N + A} = 12.5 \text{ kHz} = \frac{f_{VCO}}{N_T}$$

The reference oscillator frequency is 14.4 MHz and the output of the divide-by-R must be 12.5 kHz. Therefore:

$$R = \frac{14.4 \text{ MHz}}{12.5 \text{ kHz}} = 115210 = 0100 \ 1000 \ 00002$$

The values of A and N are dependent on the desired VCO frequency and the VCO frequency is dependent of the transmit frequency or receive frequency as shown:

$$f_{VCO} = f_T \text{ or } (f_R - 45.1 \text{ MHz}) \\ \text{where } f_T = \text{the transmit frequency} \\ f_R = \text{the receive frequency}$$

The values of A and N can be determined from the desired frequency of the VCO, where:

$$N = \text{integer part of } \frac{N_T}{127}$$

$$A = \text{remainder of } \frac{N_T}{127}$$

For example, if the receive frequency is 851.0125 MHz

$$f_{VCO} = 851.0125 \text{ MHz} - 45.1 \text{ MHz} = 805.9125 \text{ MHz}$$

$$\text{then } N_T = \frac{805.9125 \text{ MHz}}{12.5 \text{ MHz}}$$

$$\begin{array}{r} 510 \text{ INTEGER PART OF QUOTIENT} \\ 127 \overline{) 64793} \\ \underline{635} \\ 129 \\ \underline{127} \\ 23 \text{ REMAINDER} \end{array}$$

$$N = 510 = 010 \ 1111 \ 11102$$

$$A = 23 = 012 \ 0111$$

The 12.5 kHz outputs of the divide-by-A and divide-by-N counters are applied to phase detector A. The output of phase detector A is applied to phase detector B. There are 2 output signals for phase detector B (phase R and phase V). Signals phase R (U101-16) and phase V (U101-15) consist of pulses with a pulse width that depends on the phase error for the two signals at phase detector A. If the frequency f_v is greater than f_r , then error information is provided by phase V pulsing low, while phase R remains essentially high. When f_v and f_r are both in phase, both phase V and phase R remain high, except for a small minimum time period, and they both pulse low in phase. These pulses are applied to the charge pump and are used to correct VCO frequency.

The *MaxTrac* VHF model uses a divide-by-64/65 prescaler, while the UHF and 800 MHz models use the divide-by-127/128 prescaler. The working principles for the LOWBAND, VHF, UHF and 800 MHz models are the same.

When the synthesizer is locked, U101-7 applies a high level signal with very narrow negative going pulses to the loss-of-lock detector. The very narrow negative going pulses have a high average DC level that is not sufficient to turn on transistor Q101. This keeps the voltage across C102 low which indicates a lock condition.

When the synthesizer is out of lock, the output of U101-7 becomes a pulsating DC signal with an average DC level that varies between 0.5V and 4.4V. This turns on Q101 and charges up C102 to at least 3.0V indicating a out-of-lock condition.

1.6.1 Charge Pump

The charge pump consists of Q102-Q105. The phase V (U101-15) signal from the PLL IC is applied to Q103 while phase R (U101-16) is applied to Q102. When the synthesizer is locked, both signals consist of a pulse train with a period of 80 uSec and negative going pulses. The phase R negative pulse turns off Q102 and brings the emitter of Q104 to 9.6V which turns on Q104. The negative pulse of phase V turns Q103 off which reduces the current flow to R114 and in turn reduces the voltage across R114. This will cause Q105 to turn on and sink current from Q104. When the synthesizer reaches lock, the voltage at the steering line test point (SL) will be between 1.3V to 7.8V. When the synthesizer is reprogrammed with a new frequency, the previous SL voltage would now give a wrong frequency and will cause the phase R and phase V to have differing pulse widths. This will result in a situation whereby Q104 and Q105 turn on and off at different times resulting in a series of summed current pulses to the loop filter that charges or discharges C110 producing the new SL voltage. If the frequency of the VCO is higher than that of phase R, then C110 discharges. The reverse happens when the frequency of the VCO is lower.

1.6.2 Loop Filter

The loop filter consists of R119 and R120, capacitors C109 through C111. This loop filter is a low pass filter that attenuates noise and rejects the loop reference frequency so that these signals cannot modulate the VCO. The voltage across C110 is the steering line voltage that controls the VCO frequency.

1.6.3 Reference Oscillator

The 14.4 MHz reference oscillator is supplied from a 14.4 MHz crystal Y151. This crystal has a 8 digit temperature coefficient that needs to be keyed into the radio during unified chassis auto tune. The reference oscillator is warped into the desired range at room temperature by adjusting L151 manually (new field adjustment). The oscillator is temperature compensated by varactors CR151 and CR152. A change in DC voltage at frequency control J6-9 changes the varactor capacitance and warps the frequency of the oscillator. It is very important that this control voltage be defined when tuning L151 i.e. 5.2V +0.01V DC at J6-9. During the 7 digit code generation this control voltage is changed between 4.9V DC to 5.5V DC and the transmit frequency noted. During auto-tuning of the unified chassis, the electronic warping of the reference oscillator is performed by changing this control voltage. During temperature compensation, the radio "reads" the temperature of Y151 by sensing the forward bias across CR176 and its translation via amplifier U176 to give temp sense voltage at J6-14.

The temp sense voltage is proportional to the actual temperature measured. The reference oscillator will be warped according to the temperature of the oscillator in order to correct the drift in frequency due to heating of the crystal Y151. Analysis of this temp sense circuit centers around the DC voltage measurements of the various nodes. All the resistors associated with this circuit have a 1% tolerance, therefore any component damage or part value change will affect the translated voltage at J6-14. The diode, CR176, needs to be flush to the board to ensure an accurate temp sensing. During transmissions with PL/DPL tones, the reference oscillator will be modulated. Potentiometer R164 controls the reference modulation level.

1.7 VOLTAGE CONTROLLED OSCILLATOR

MaxTrac models for LOWBAND, VHF, and UHF use two separate VCO's, one for transmit and one for receive. The *MaxTrac* 800 MHz radio uses one VCO for transmit and receive. Switching between the transmit and receive VCO's is accomplished by the use of a switching circuit consisting of transistors Q277, Q278, and Q279. Transistor Q276 provides the 8.5 volt source to these transistors to power the VCO's. During the transmit mode, J6-4, the Transmit/Receive Shift Line, is at .1V DC. This will cause Q277 and Q278 to turn on and switch 8.5 volts to the transmit VCO. Q279 is turned off and keeps the 8.5 volts from reaching the receive VCO. During the receive mode, the voltage on J6-4 goes to 9.6 volts. This turns Q277, Q278 off and Q279 on. The 8.5 volts is applied to receive VCO and the transmit VCO is shut off.

The transmit and receive VCO's are very similar in design. The transmit VCO has a modulation circuit added and will be discussed later. The steering line D.C. voltage from the synthesizer is applied to each VCO. L213 in the transmit VCO and L202 in the receive VCO are tuned for a steering line voltage of 7.8V DC at the high end of the band. Varactors CR210-213 in the transmit VCO and CR202-205 in the receive VCO are used to change the frequency of the VCO.

The steering line D.C. voltage is applied to the varactors whose capacitance changes as the voltage increases or decreases. The steering line voltage is checked for greater than 1.8 volts at the low end of the band. This is to ensure that the tuning range is made as large as possible by the synthesizer.

In the transmit mode, the modulating signal applied to J6-10 changes the varactor capacitance of CR209 and modulates the VCO. Resistors R222, R223, and R225 act as potential dividers and only a fraction of the modulating signal is seen by CR209. The resistor combination also helps by attenuating any stray unwanted signals.

Q206 in the transmit VCO and Q203 in the receive VCO are the FET oscillators.

Transistors Q207, Q208 in the transmit VCO and Q204, Q205 in the receive VCO are the buffer amplifiers. A sample of the VCO frequency is fed back to the synthesizer circuit from the base of Q208 (transmit) and Q205 (receive). This sample is necessary for the synthesizer to "know" if the VCO is at the required frequency. The output of Q208 goes to the PA deck to be amplified. The output of Q205 makes up the local oscillator and is fed to the first mixer CR1.

The UHF VCO has an added circuit where the VCO frequency can be shifted by changing the voltage at J6-12. At the lower range, transistor Q209 is turned on and switches 9.6 volts to pin diodes CR201 and CR208. This causes C226 (transmit) and C203 (receive) to be added to the VCO and shifts the frequency of the VCO.

In the 800 MHz radio, there is only one VCO and it is contained in module U201. The transmit frequency range is 806-825 MHz while the receive frequency range is 851-870 MHz. The receive local oscillator signal is extracted from Q202. The transmitter signal is also extracted from Q202 with an additional buffer Q203. During the receive mode, the VCO signal from transistor Q203 is attenuated by turning off Q204. An attenuated VCO output is still available at J5 during the receive mode and the receive injection frequency can be measured. In the 800 MHz talk around radio, there is a similar pin diode shift circuitry like that used in the UHF radios to shift the VCO frequency to the 851-870 MHz range.

2. Troubleshooting Guide

2.1 RECEIVER SECTION

The theory of operation and schematics along with the troubleshooting chart "RECEIVER" will aid the servicer in isolating to the faulty component.

The use of proper test equipment such as the R2021D or R2001D with TEK-10 probe will also help in making accurate comparison measurements.

Refer to the proper schematic for each band for the voltages and waveforms. Observe the notes for information on how to set up for the measurements. When using the TEK-10 probe, be sure of a good RF ground before assuming the reading is correct.

Although many of the components are located on the solder side, the schematics can be used to isolate before having to pull the board from the chassis.

2.2 SYNTHESIZER SECTION

The synthesizer uses a phase locked loop design. Before troubleshooting this section the servicer may wish to review the theory of operation before continuing.

The synthesizer can be checked for an "out-of-lock" condition by looking at the lock detect line at J6-5. When in lock, the voltage will be 0V DC and when out of lock, the line will typically be 3V DC.

Be sure the DC voltages to the synthesizer are correct before proceeding. Troubleshoot the voltage regulators if wrong voltage levels are recorded.

Next, check Fr which is pin 13 of the synthesizer. Depending on the model of radio, a frequency of either 12.5 kHz, 6.25 kHz, or 5 kHz will be seen. This proves that the reference oscillator's output and the programming of the synthesizer are good.

If Fr is bad, check to see that the reference oscillator's output is on frequency and at the proper level. If the reference oscillator is off frequency, use the Radio Service software to try and warp the oscillator frequency on. Do not attempt to warp L151 on the RF board. This coil is factory adjusted and should not be field adjusted.

If the frequency will not warp on, check to make sure the DC voltages around the reference oscillator are correct. Board replacement will have to be done if the fault does not clear after programming.

The use of an open loop test will help to isolate between the synthesizer and VCO. By using a variable DC supply and breaking the steering line voltage away from the VCO, you can insert a DC voltage and observe the VCO's output. If the VCO tracks with the external DC voltage, the problem is in the synthesizer and prior to the steering line.

Tracing the signal through the feedback amplifier, it is important to pay close attention to the signal levels. Refer to the schematics for proper signal level for each band.

At the prescaler, the frequency can be calculated by dividing F_{vco} by 128 for 800 and UHF. Dividing by 64 is for the VHF model. Check the Modulus Control line on pin 6 of the prescaler. There should be a pulse train at the loop rate (12.5, 6.25, 5 kHz). If this is not present, then either the prescaler is loading down the signal or the synthesizer is bad.

Finally, check Fv. This should be a pulse train at the reference rate. It should be in lock with Fr. If there is no pulse train but you have a good signal from the prescaler, then the synthesizer's internal dividers are bad.

If Fv is okay then check the outputs to the Charge Pumps. The ground pulse will be at the reference rate. When Fv leads Fr, the pulse from pin 15 will have an increased pulse width. If Fr leads Fv, then the pulse out pin 16 will have an increased pulse width.

If the DC power supply is still connected on the steering line, disconnect it. Reattach the steering line circuitry and attach a DC DVM to the steering line test point. While monitoring the DVM, momentarily touch the base of Q103. The steering line voltage should drop to almost 0V DC. Next, ground the base of Q102. The DVM should increase to almost +9.6V DC. If either of these checks do not work, troubleshoot that particular side of the pumps.

Finally, if everything in the Phase Locked Loop appears to be normal, except for lock detect J6-5, check out the Lock Detect circuit. Synthesizer pin 7 should be very narrow ground pulses when in lock and the pulse width will be random when out of lock.

3. Extender Field Test

The purpose of this test is to give field technicians the ability to verify extender functionality without using a pulse generator box (such as the TEK-47A or TEK-21). This test does not take the place of factory testing of the extender.

3.1 TEST EQUIPMENT

R2001D Motorola Communication System Analyzer or Equivalent.

3.2 TEST PROCEDURE

- (1) Ensure that the radio is turned off; then connect the RF generator output to the antenna port of the radio. Tune the RF generator to the receive (RX) frequency of the radio mode to be tested.
- (2) Adjust the RF output level from the R2001D to -47 dBm (1 millivolt).
- (3) Modulate the RF signal with 100% AM modulation at a frequency of 10 kHz. Use either tone A or B modulation from R2001D with AM limit (RF Section) set to Minimum.
- (4) Locate the VAGC Test Point (see Figure 3) in the extender section of the RF board. Short the test point pad to ground using a small piece of wire soldered from the pad to the coil can (L352/L353) nearby.
- (5) Turn the radio on. The extender is in the "ON" state when the radio is turned on.
- (6) Observe the Extender Test Point (see Figure 3) with a 10:1 oscilloscope probe. Pulses at the repetition rate of 10 kHz should be seen.
- (7) Turn the extender off by depressing the monitor button on the control head for 3 to 4 seconds; listen for the three low-pitched tones. There should be no pulses at the test point. Turn the extender on again by depressing the monitor button on the control head for 3 to 4 seconds; listen for three high-pitched "beeps." The pulses should be seen at the test point.
- (8) Turn the radio off and remove the wire used in Step 4. This concludes the extender functionality test.

Note

If the Extender does not function as described above, replace the RF board.

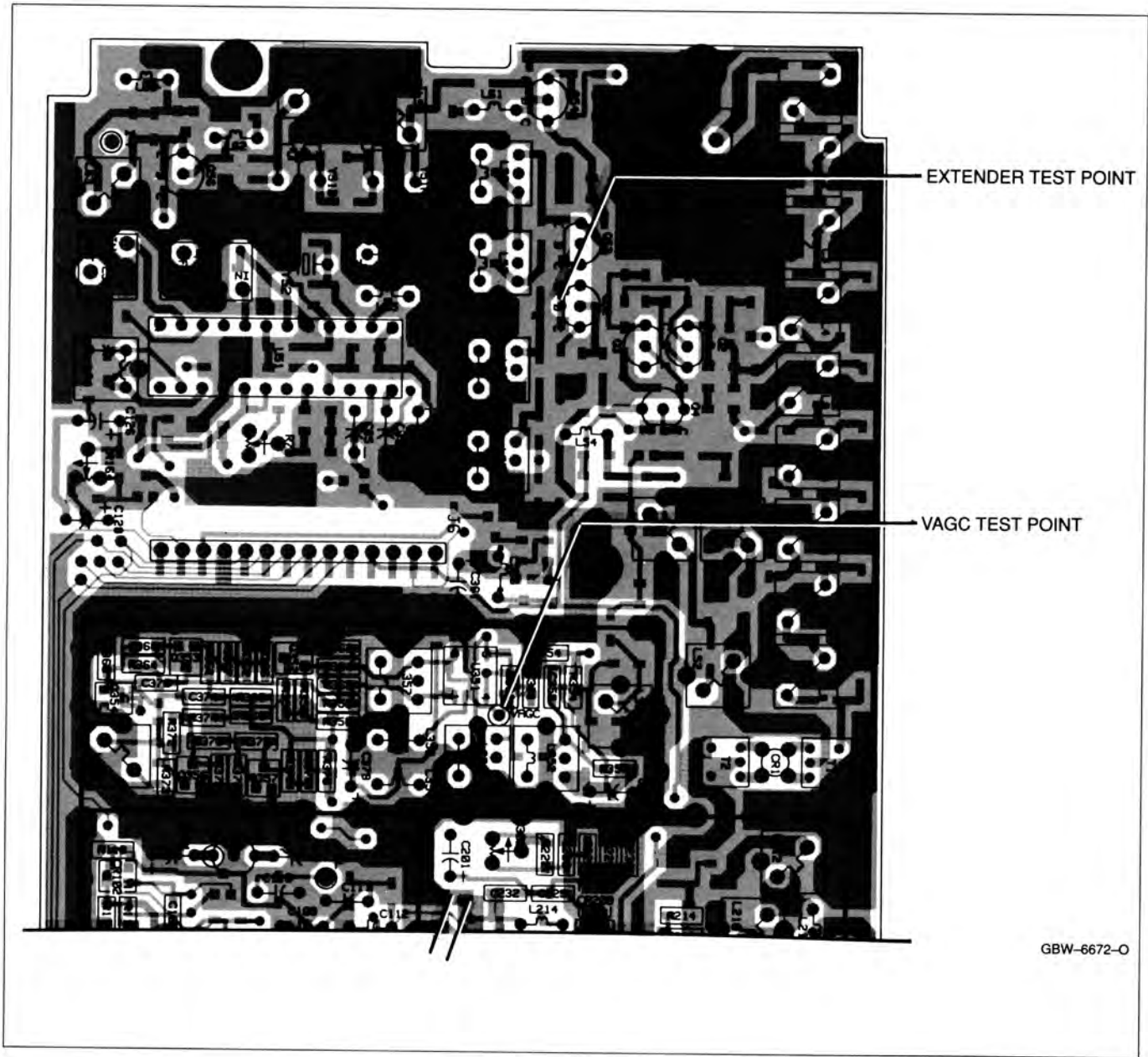
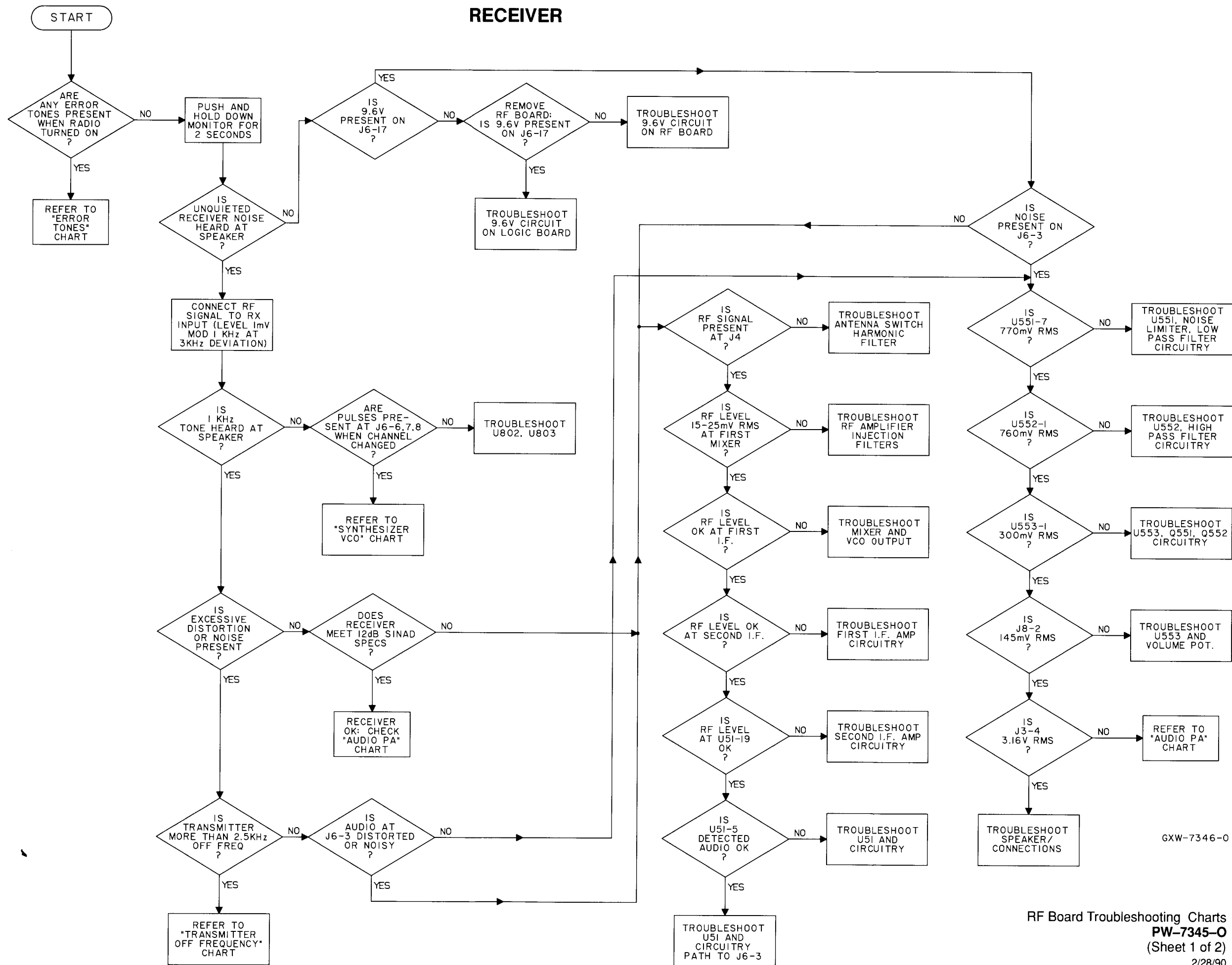


Figure 3. Extender Test Points

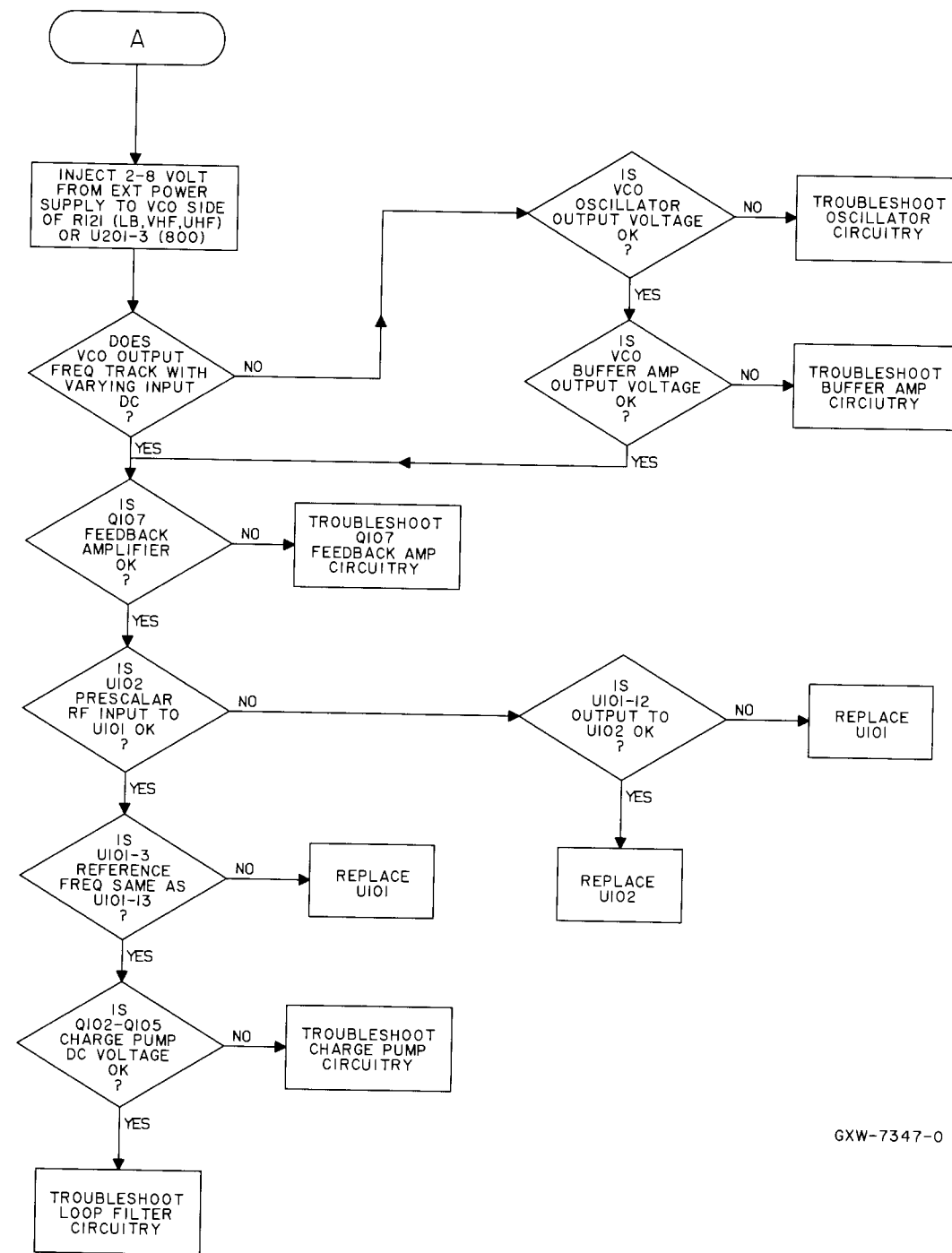
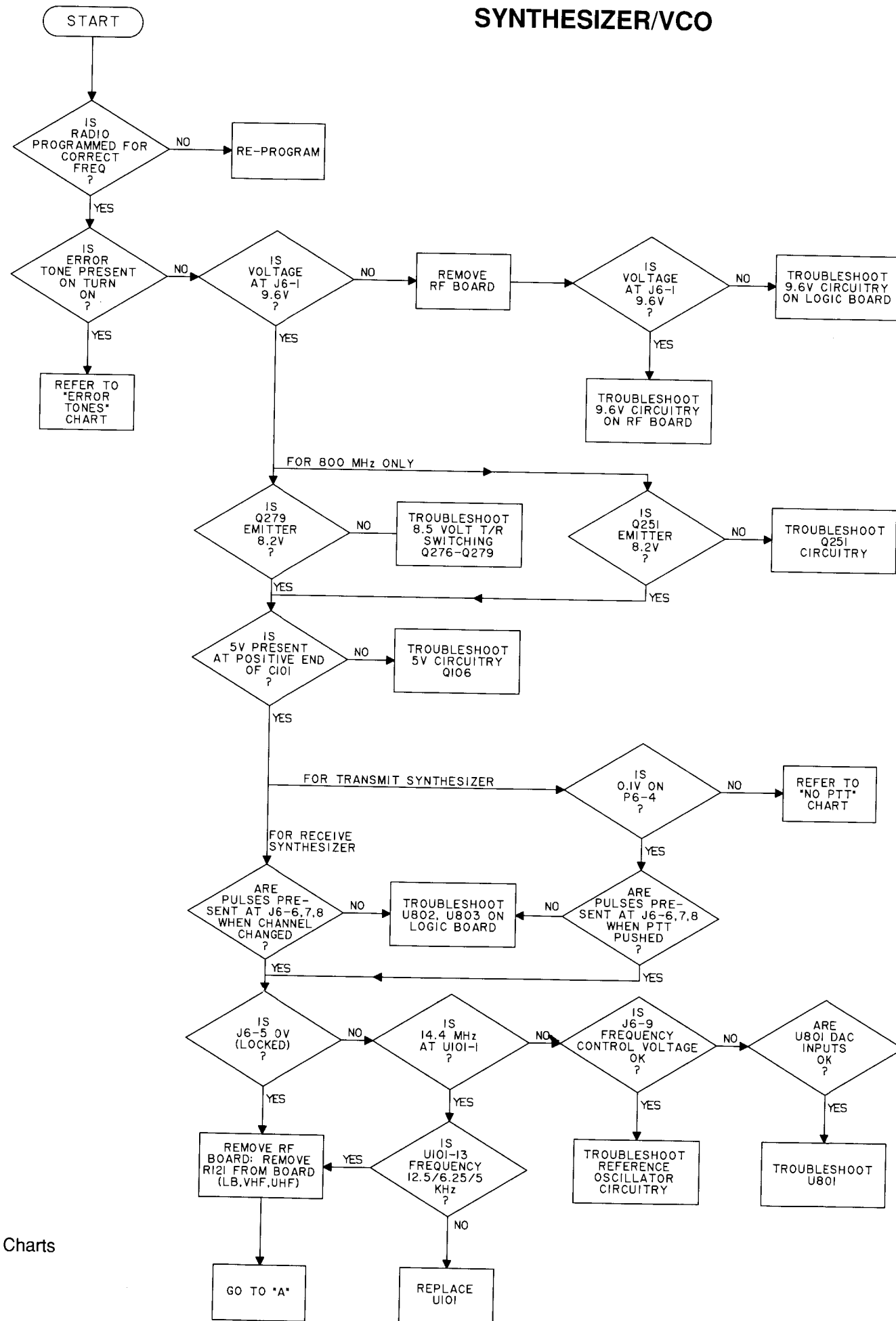
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RECEIVER

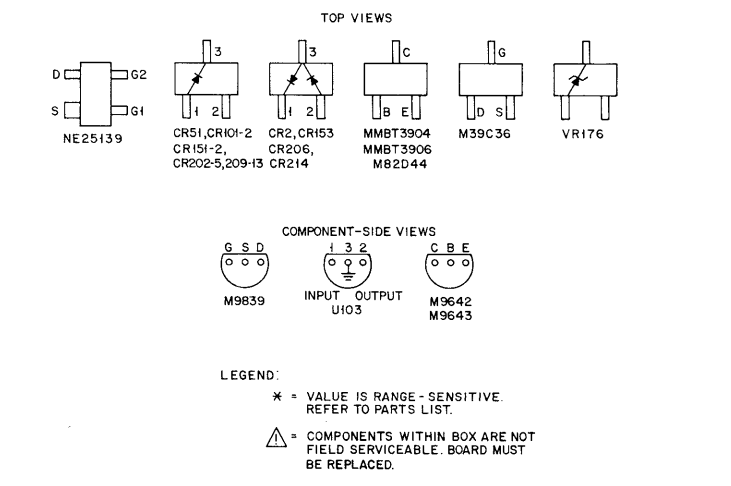
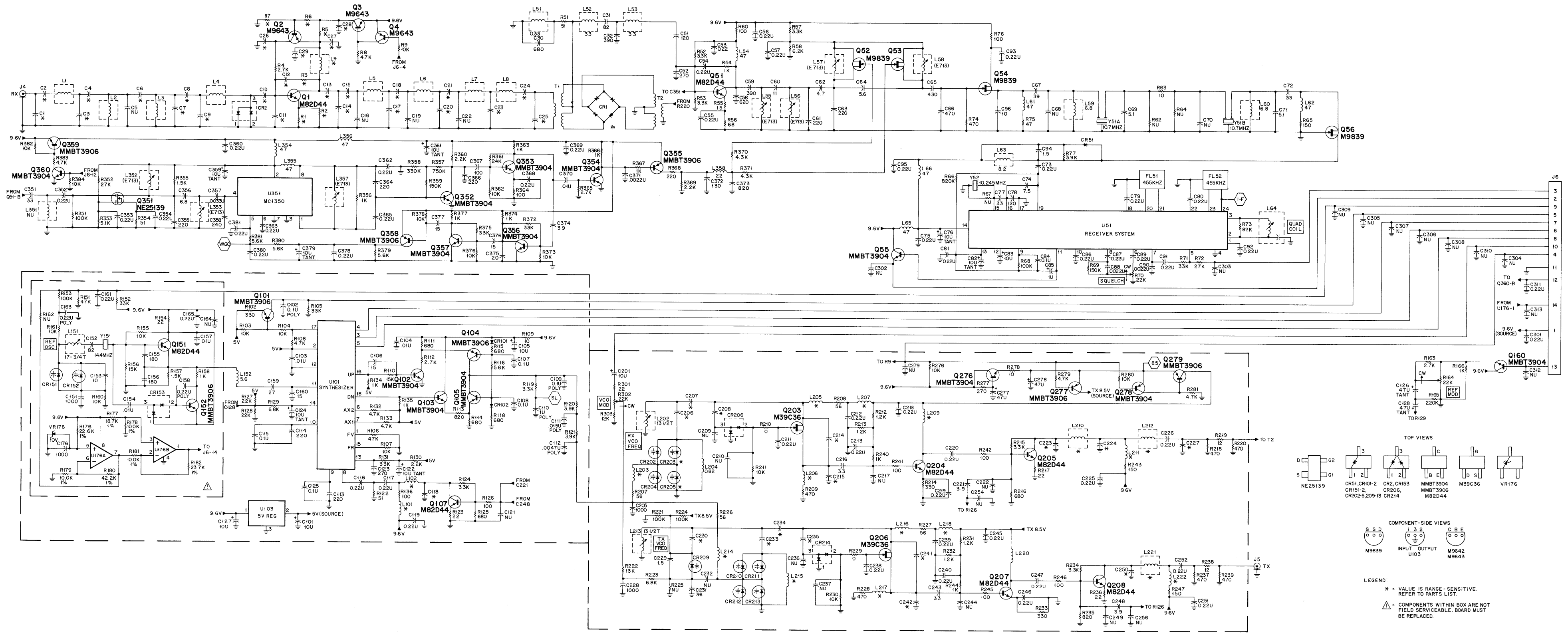


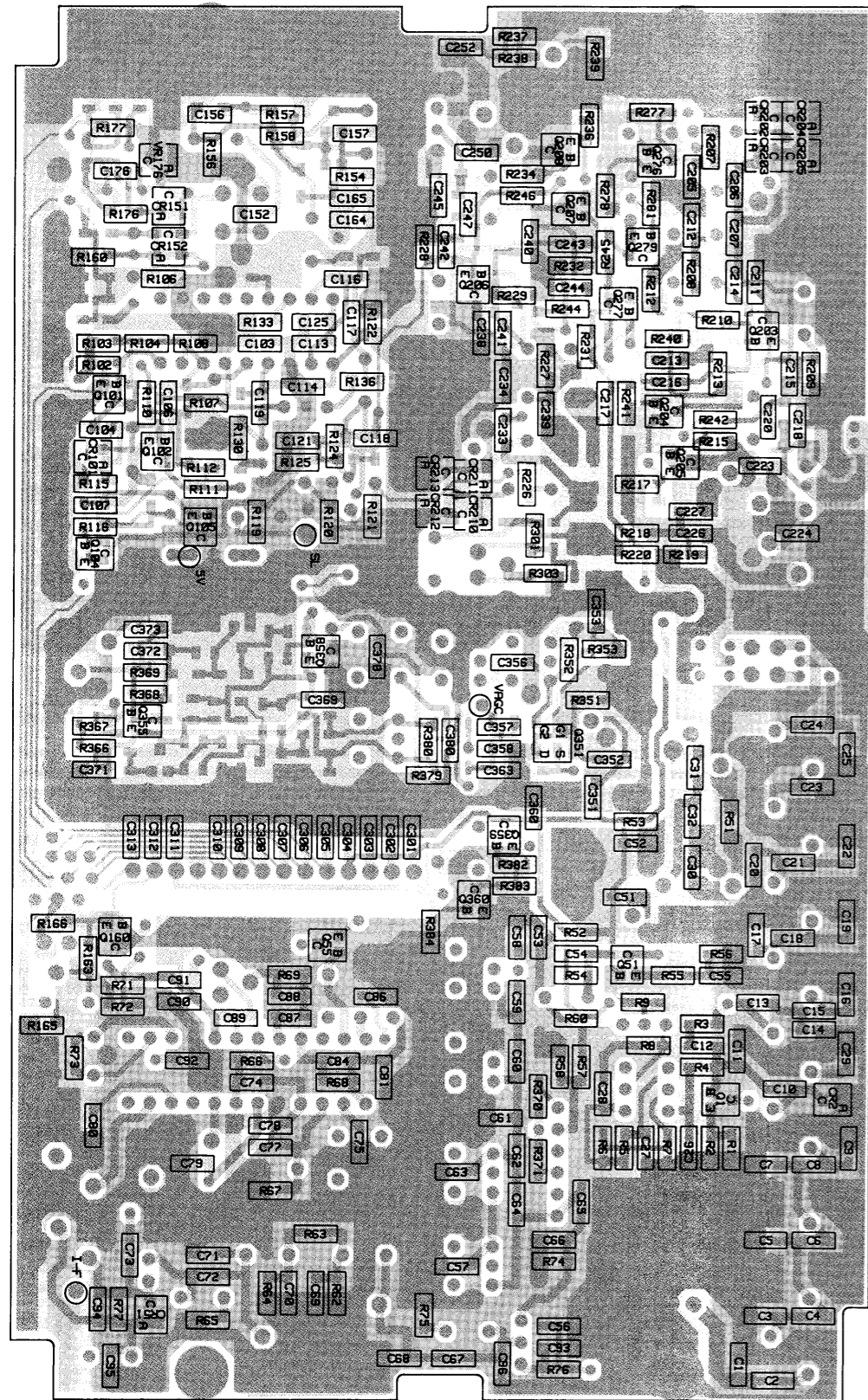
GXW-7346-0

SYNTHESIZER/VCO



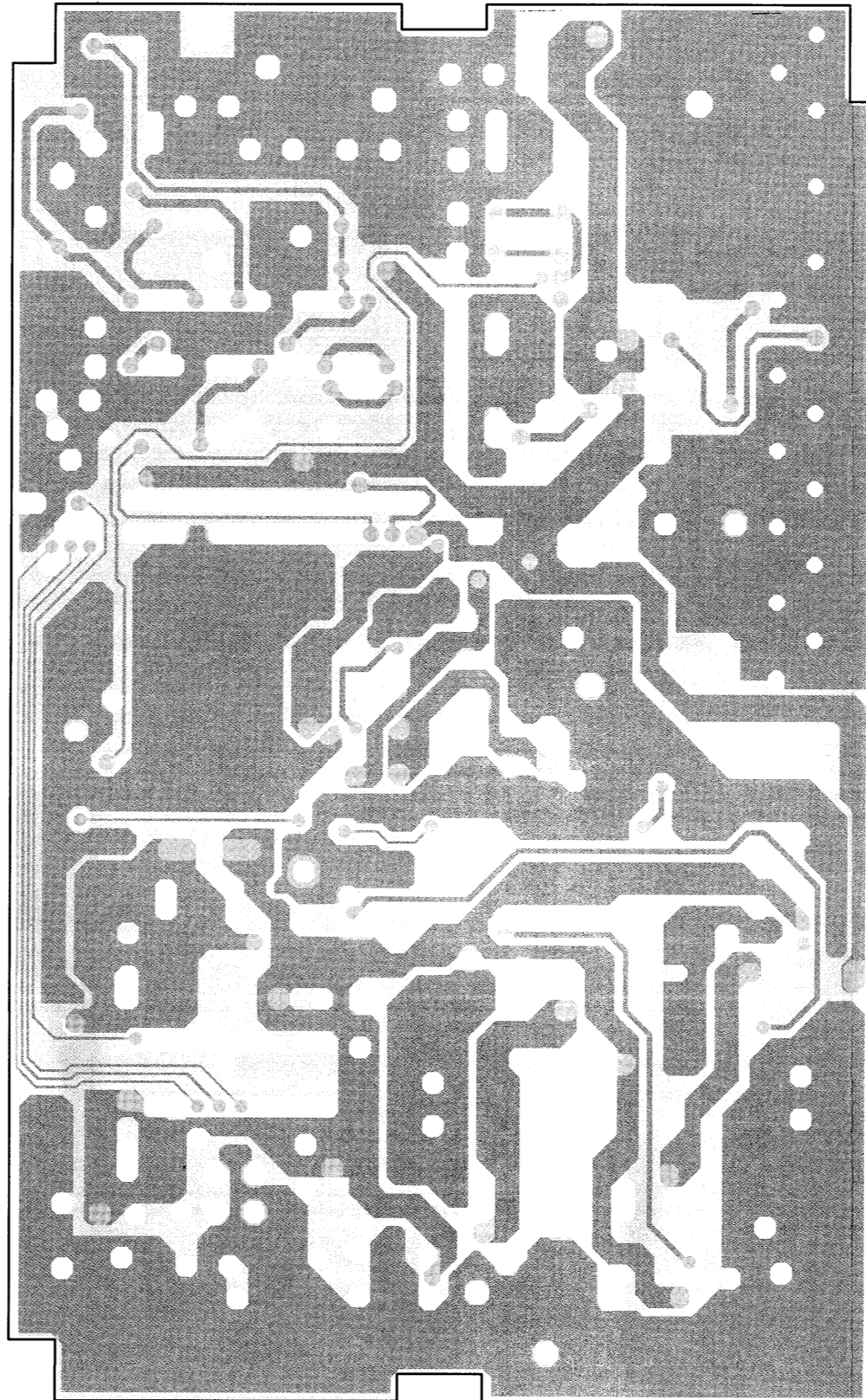
GXW-7347-0





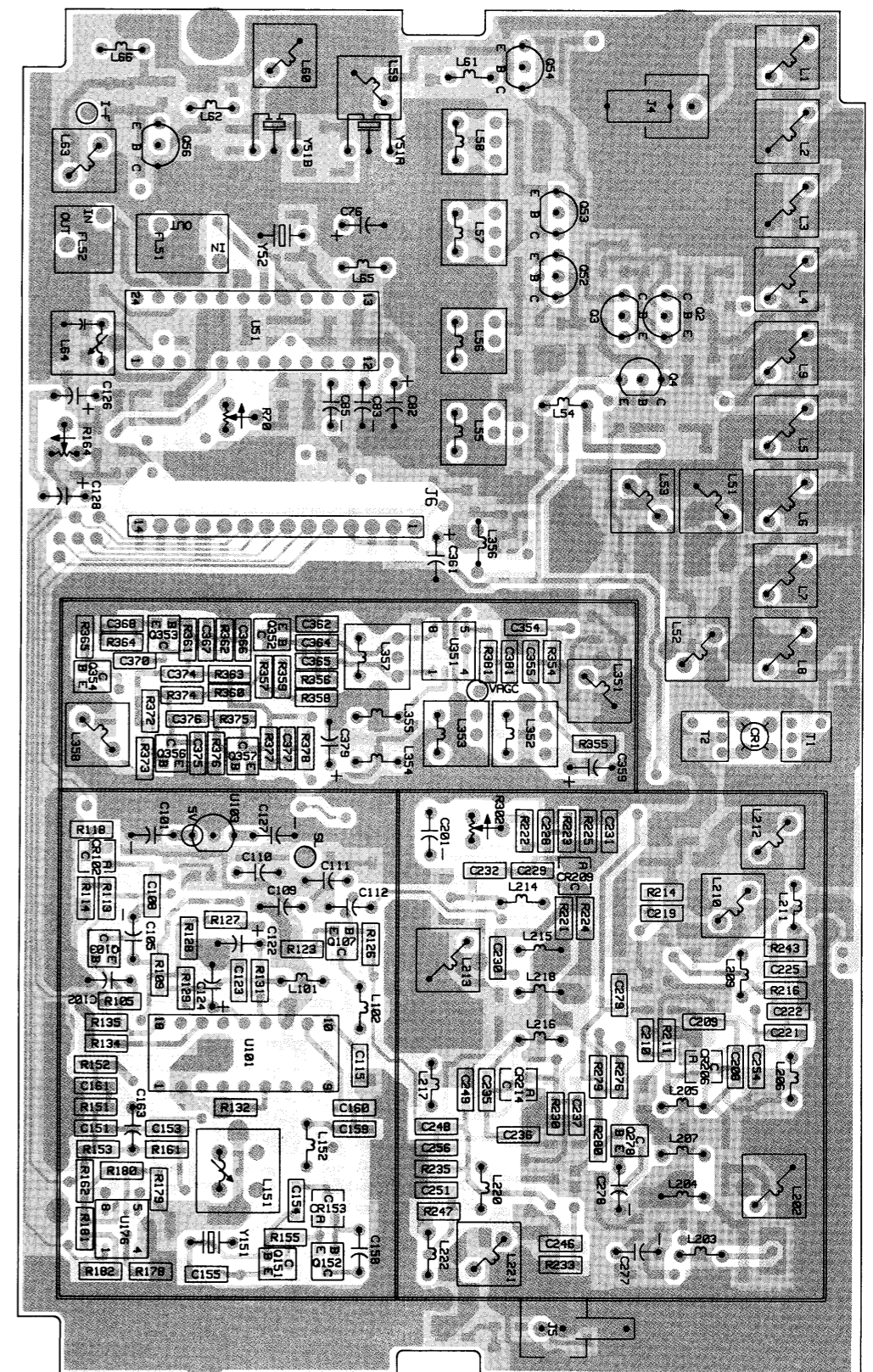
SOLDER SIDE VIEW

SOLDER SIDE GBW-6349-O
 COMPONENT SIDE GBW-6350-O
 OVERLAY GBW-6351-O



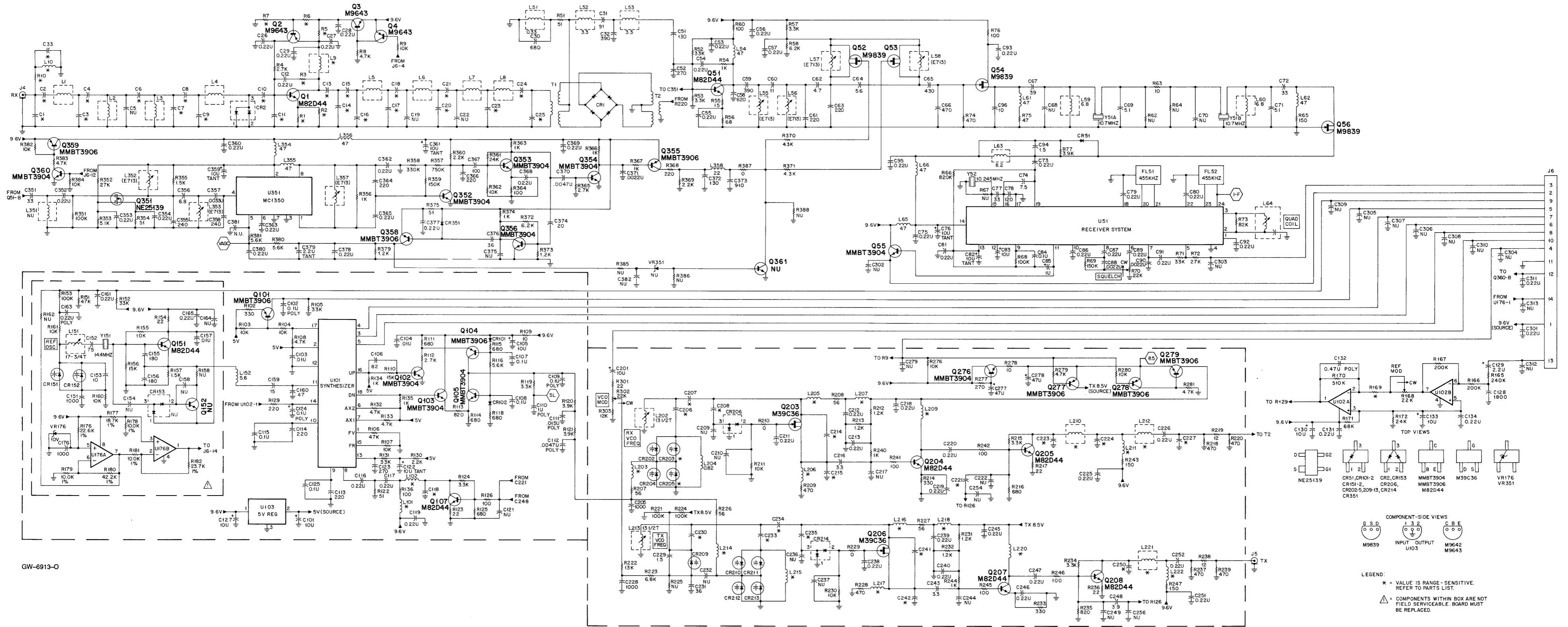
INNER LAYERS

SOLDER INNER LAYER GCW-6389-O
 COMPONENT INNER LAYER GCW-6390-O

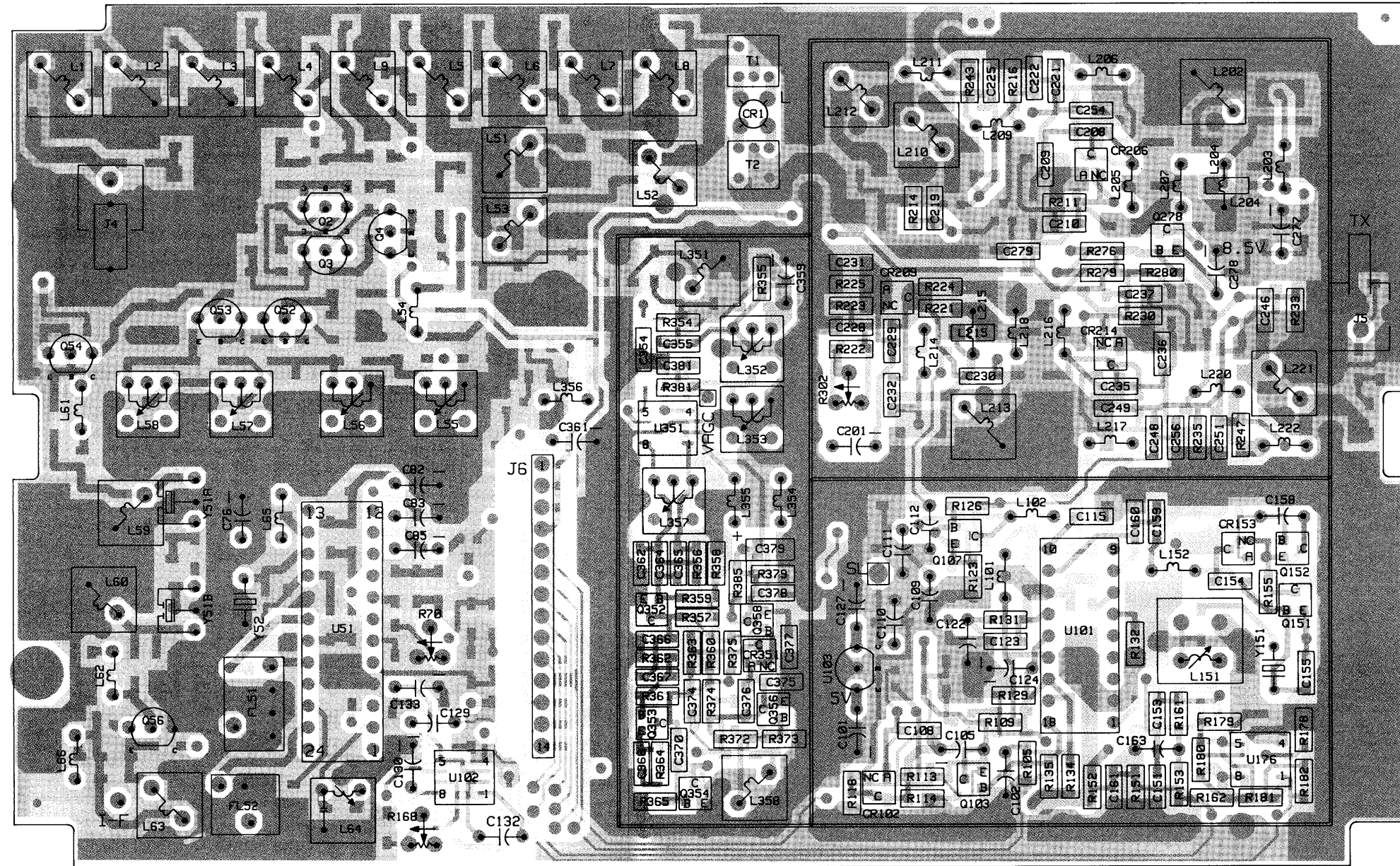


COMPONENT SIDE VIEW

SOLDER SIDE GBW-6349-O
 COMPONENT SIDE GBW-6350-O
 OVERLAY GBW-6391-O

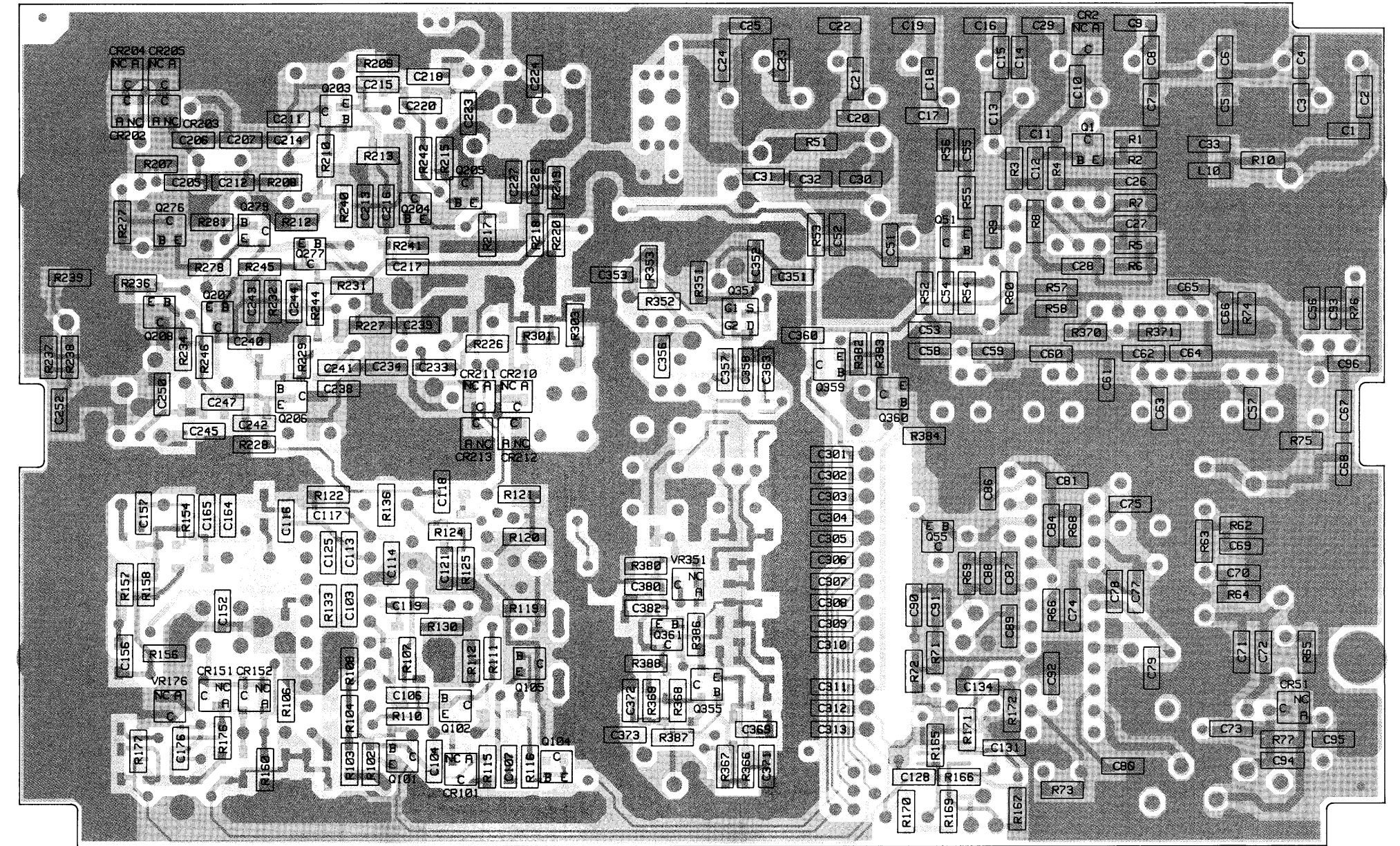


Schematic, Circuit Board Diagram, and Parts List for HLB4100A Low Band RF Board (Early Version)
PW-6916-A
(Sheet 1 of 3)
3/31/90



COMPONENT SIDE

COMPONENT SIDE ●
 SOLDER SIDE ○
 OVERLAY — GW-6914W01-O

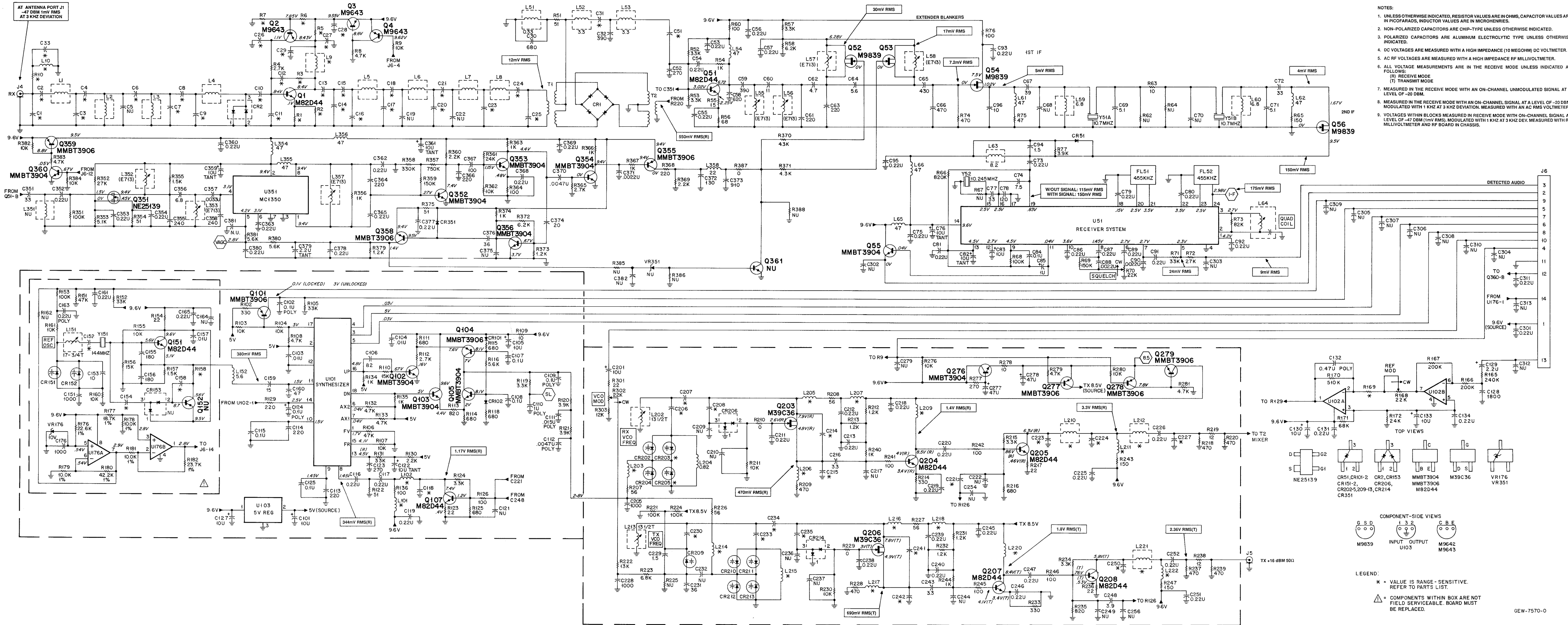


SOLDER SIDE

COMPONENT SIDE ●
 SOLDER SIDE ○
 OVERLAY — GW-6914W02-O

Low Band RF Board Transistor D.C. Voltage Table

Transistor Ref. No.	VOLTAGE			VOLTAGE		
	BASE	EMITTER	COLLECTOR	GATE	SOURCE	DRAIN
Q1	0.8	0.1	8.4	—	—	—
Q2	7.8	8.4	1.1	—	—	—
Q3	8.8	9.6	9.5	—	—	—
Q4	9.6	9.6	8.8	—	—	—
Q51	3.0	2.3	6.7	—	—	—
Q52	—	—	—	0	6.3	6.3
Q53	—	—	—	0	6.3	6.3
Q54	—	—	—	0	1.1	7.5
Q55	.04	0	9.6	—	—	—
Q56	—	—	—	0	1.7	9.5
Q101	5.0	5.0	0.1	—	—	—
Q102	0.7	0	0.1	—	—	—
Q103	5.0	4.4	9.6	—	—	—
Q104	8.1	2-8v	2-8v	—	—	—
Q105	8.1	2.0	2-8v	—	—	—
Q107	1.2	0.4	7.4	—	—	—
Q151	5.6	5.1v	9.6	—	—	—
Q152	8.7v	9.5	5.8	—	—	—
Q160	4.3	3.6	9.6	—	—	—
Q203	—	—	—	2.6(R)	4.8(R)	7.9(R)
Q204	4.0(R)	3.4(R)	8.5(R)	—	—	—
Q205	.86(R)	.46(R)	6.3(R)	—	—	—
Q206	—	—	—	3.0(T)	4.9(T)	7.8(T)
Q207	4.1(T)	3.4(T)	8.4(T)	—	—	—
Q208	.76(T)	.53(T)	5.8(T)	—	—	—
Q276	9.6	8.5	9.6	—	—	—
Q277	9.5	8.5	9.5	—	—	—
Q278	9.6	8.5	7.8	—	—	—
Q279	7.8	8.5	8.5	—	—	—
Q352	.27	0	7.4	—	—	—
Q353	1.2	.48	4.4	—	—	—
Q354	0	0	9.4	—	—	—
Q355	9.4	9.4	0	—	—	—
Q356	.67	0	3.7	—	—	—
Q357	.67	0	3.7	—	—	—
Q358	9.5	9.4	1.4	—	—	—
Q359	8.8	9.6	9.5	—	—	—
Q360	.67	0	.05	—	—	—



- NOTES:
- UNLESS OTHERWISE INDICATED, RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN PICOFARADS, INDUCTOR VALUES ARE IN MICROHENRIES.
 - NON-POLARIZED CAPACITORS ARE CHIP-TYPE UNLESS OTHERWISE INDICATED.
 - POLARIZED CAPACITORS ARE ALUMINUM ELECTROLYTIC TYPE UNLESS OTHERWISE INDICATED.
 - DC VOLTAGES ARE MEASURED WITH A HIGH IMPEDANCE (10 MEGOHM) DC VOLTMETER.
 - AC RF VOLTAGES ARE MEASURED WITH A HIGH IMPEDANCE RF MILLIVOLTMETER.
 - ALL VOLTAGE MEASUREMENTS ARE IN THE RECEIVE MODE UNLESS INDICATED AS FOLLOWS:
(R) RECEIVE MODE
(T) TRANSMIT MODE
 - MEASURED IN THE RECEIVE MODE WITH AN ON-CHANNEL UNMODULATED SIGNAL AT A LEVEL OF -20 DBM.
 - MEASURED IN THE RECEIVE MODE WITH AN ON-CHANNEL SIGNAL AT A LEVEL OF -20 DBM, MODULATED WITH 1 KHZ AT 3 KHZ DEVIATION. MEASURED WITH AN AC RMS VOLTMETER.
 - VOLTAGES WITHIN BLOCKS MEASURED IN RECEIVE MODE WITH ON-CHANNEL SIGNAL AT A LEVEL OF -47 DBM (1mV RMS), MODULATED WITH 1 KHZ AT 3 KHZ DEV. MEASURED WITH RF MILLIVOLTMETER AND RF BOARD IN CHASSIS.

parts list

HLB4099B Low Band RF Board 29.7-36.0 MHz (Range 1) MXW-7571-O

HLB4099B Low Band RF Board 29.7-36.0 MHz (Range 1) MXW-7571-O (2)

HLB4099B Low Band RF Board 29.7-36.0 MHz (Range 1) MXW-7571-O (3)

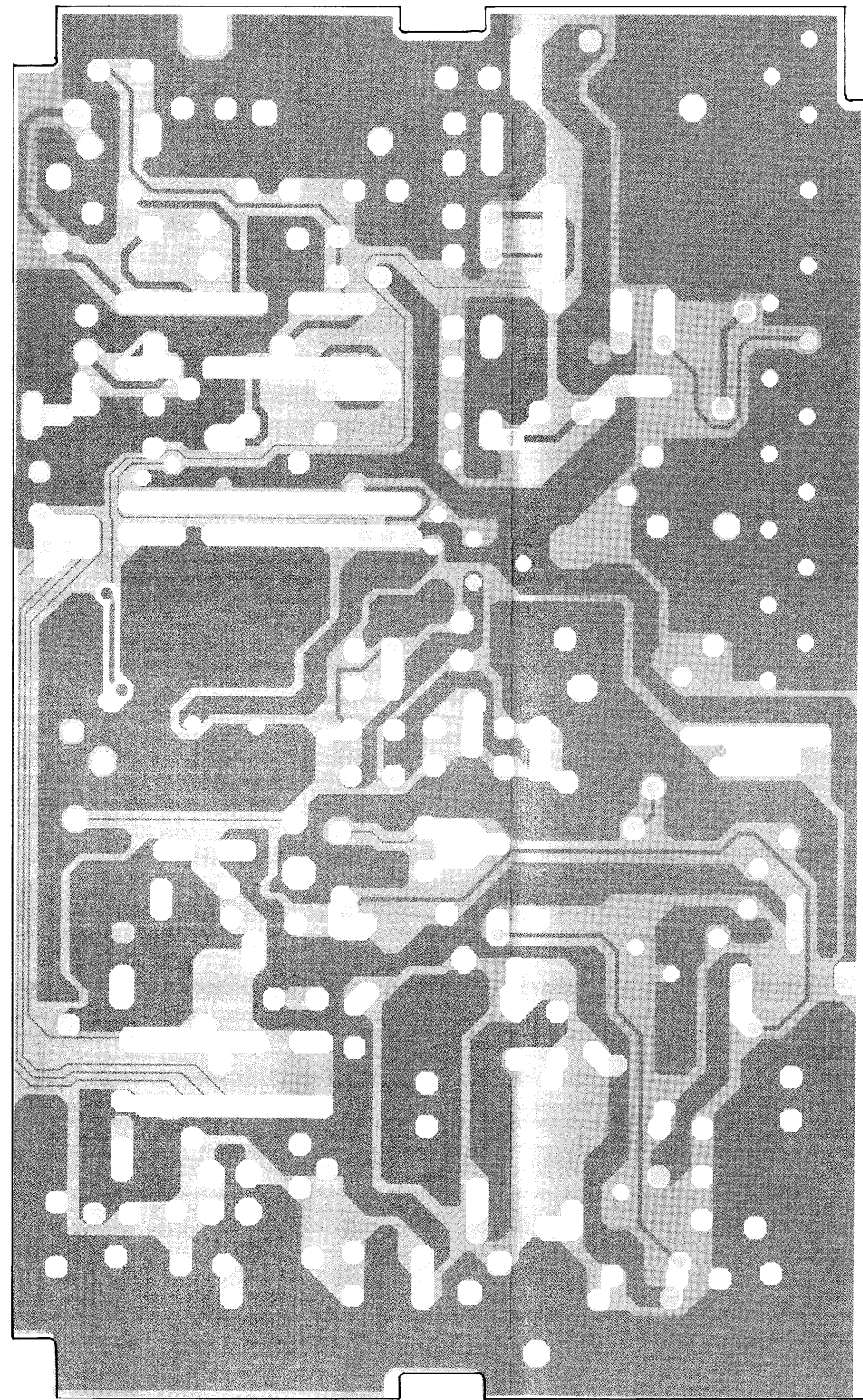
HLB4099B Low Band RF Board 29.7-36.0 MHz (Range 1) MXW-7571-O (4)

HLB4099B Low Band RF Board 29.7-36.0 MHz (Range 1) MXW-7571-O (5)

HLB4099B Low Band RF Board 29.7-36.0 MHz (Range 1) MXW-7572-O (2)

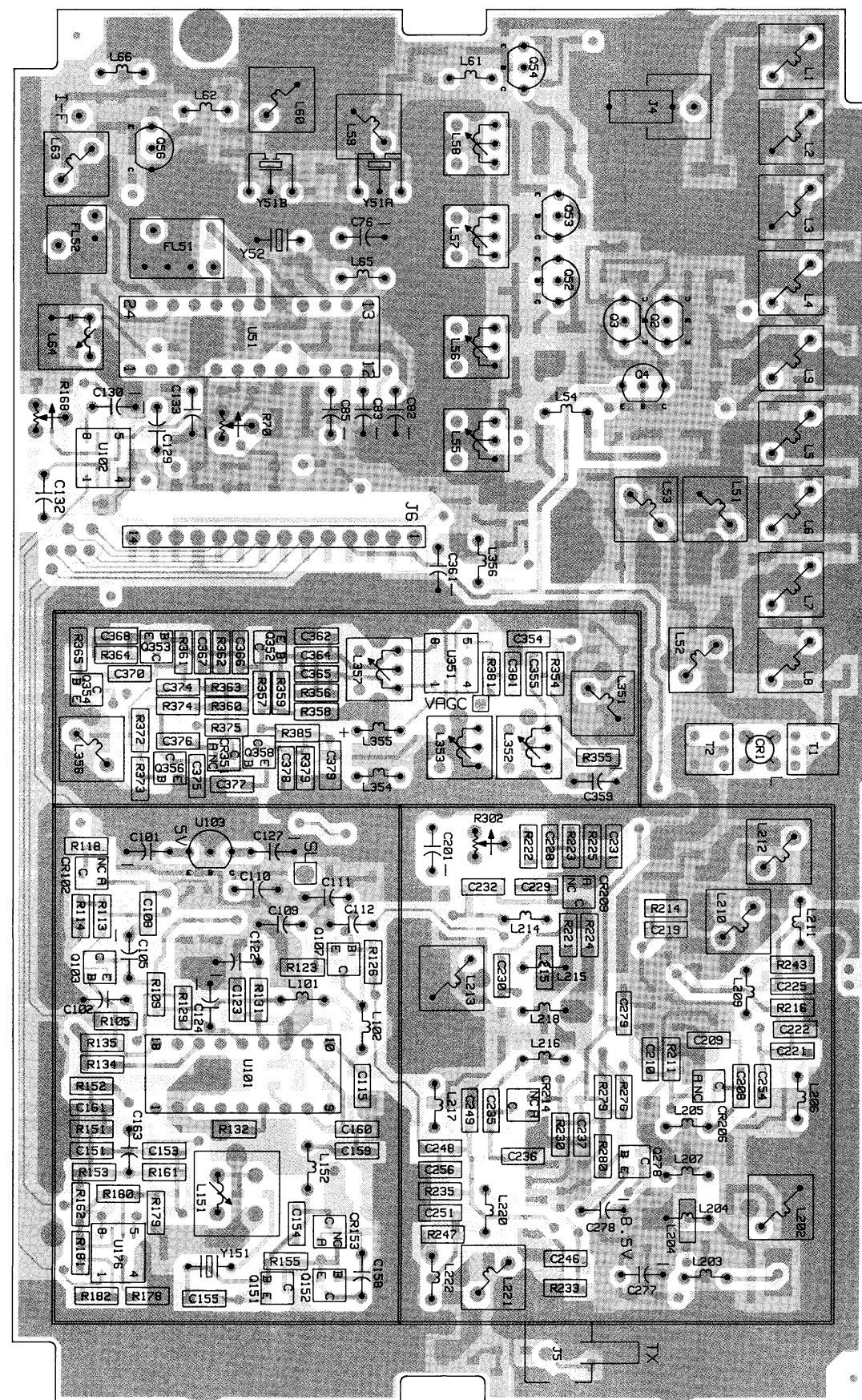
HLB4099B Low Band RF Board 29.7-36.0 MHz (Range 1) MXW-7572-O (3)

Schematic, Circuit Board Diagrams, and Parts Lists for HLB4100A/4099B/4101B Low Band RF Board PW-7569-O (Sheet 2 of 4)



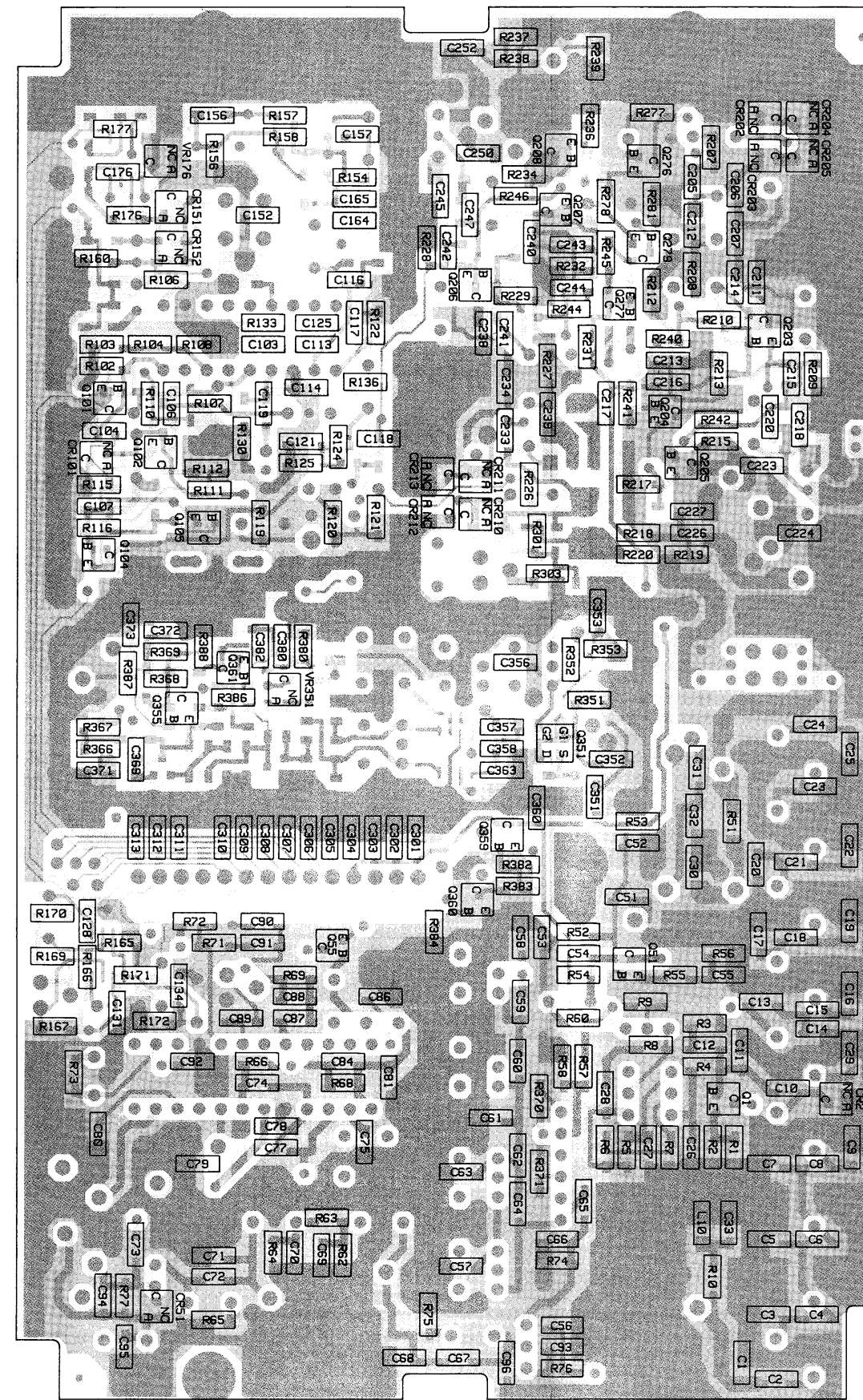
INNER LAYERS

INNER LAYER 1	RED	GAW-7688-O
INNER LAYER 2	GREY	GAW-7689-O
OVERLAY	BLACK	GDW-7690-O



COMPONENT SIDE VIEW

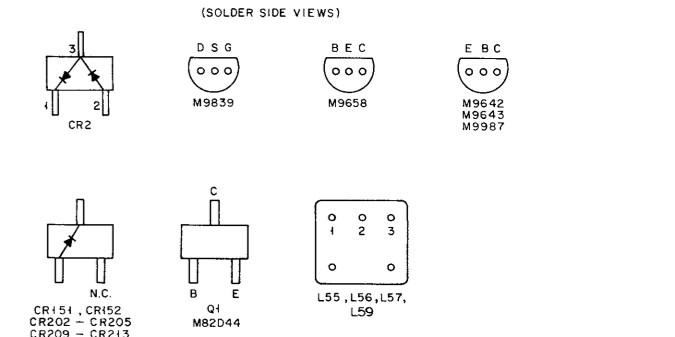
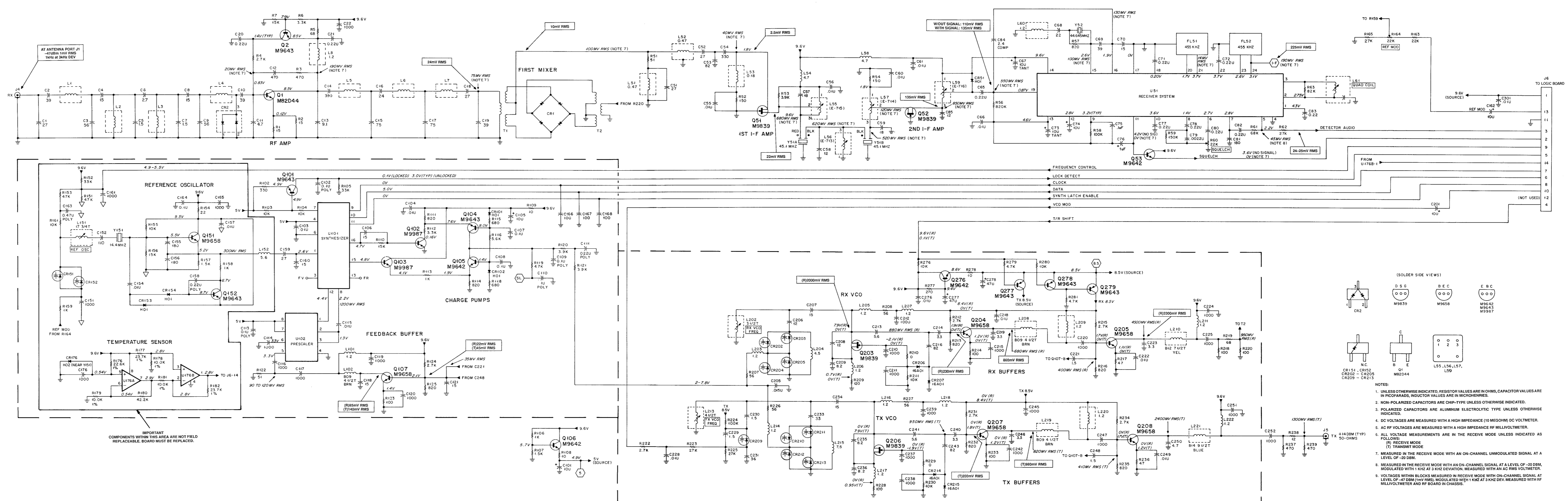
SOLDER SIDE	RED	GAW-7685-O
COMPONENT SIDE	GREY	GAW-7686-O
OVERLAYS	BLACK	GDW-7687-O



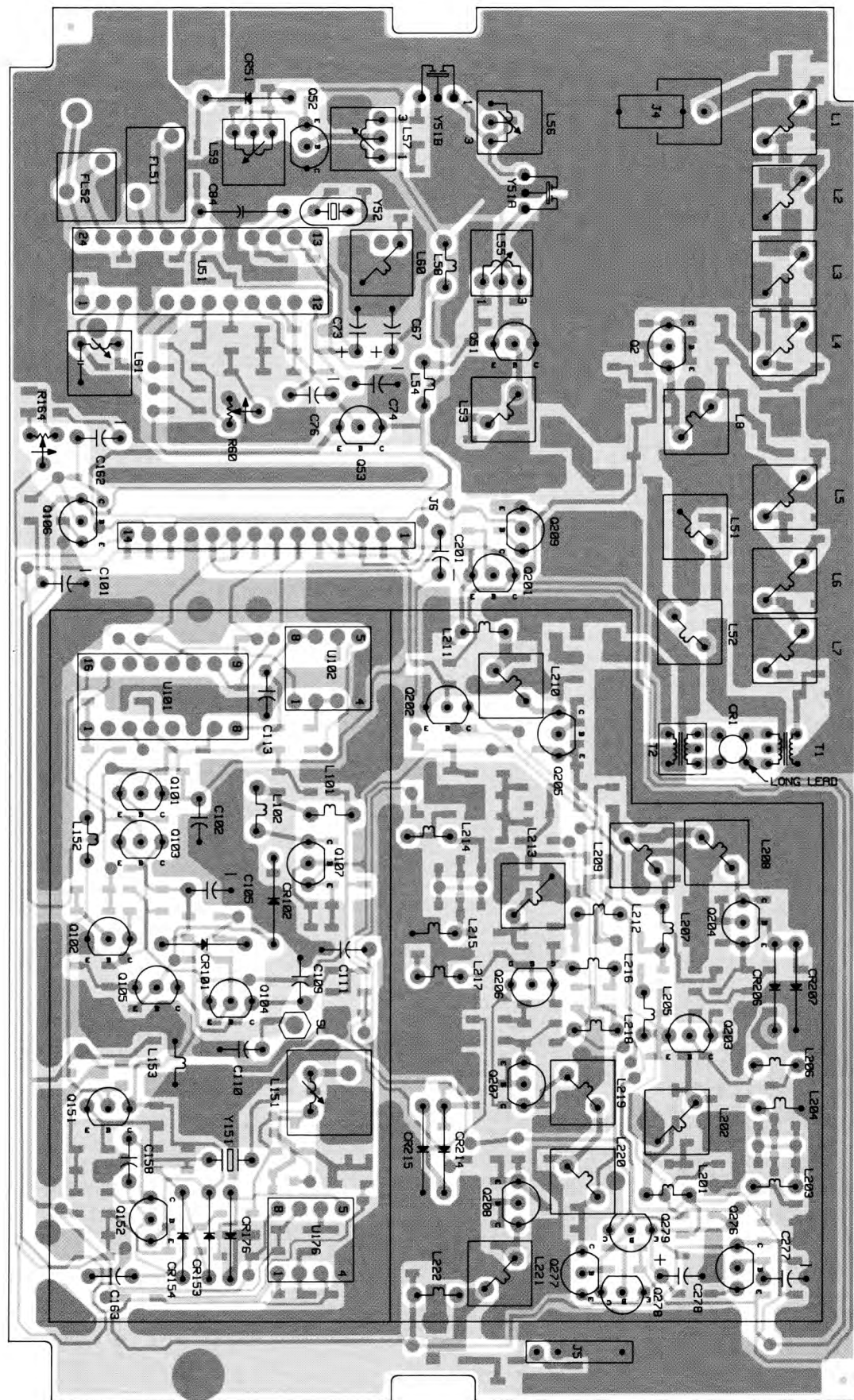
SOLDER SIDE VIEW

VHF RF Board Transistor D.C. Voltage Table

Transistor Ref. No.	VOLTAGE			VOLTAGE		
	BASE	EMITTER	COLLECTOR	GATE	SOURCE	DRAIN
Q1	.83	.12	8.5	—	—	—
Q2	7.9	8.5	1.1	—	—	—
Q51	—	—	—	0	1.8	9.6
Q52	—	—	—	0	1.8	9.6
Q53	4.2	3.6	9.6	—	—	—
Q101	5.0	5.0	.1 (LOCKED)	—	—	—
Q102	0.7	0	0	—	—	—
Q103	4.8	4.1	9.6	—	—	—
Q104	8.1	7.6	2-8v	—	—	—
Q105	1.4	1.9	2-8v	—	—	—
Q106	5.7	4.9	9.6	—	—	—
Q107	2.1	1.4	9.6	—	—	—
Q151	5.5	5.2	9.5	—	—	—
Q152	8.7	9.5	6.7	—	—	—
Q203	—	—	—	-2.1(R)	.7(R)	7.9
Q204	1.9(R)	1.2(R)	8.5	—	—	—
Q205	1.7(R)	1.1(R)	9.6	—	—	—
Q206	—	—	—	-1.9(T)	.95(T)	7.9
Q207	1.8(T)	1.2(T)	8.5	—	—	—
Q208	1.7(T)	1.2(T)	9.6	—	—	—
Q276	9.5	8.6	9.6	—	—	—
Q277	9.6	8.5(T)	8.5	—	—	—
Q278	9.6(R)	8.5	8.5	—	—	—
Q279	7.6(R)	8.5	8.5	—	—	—

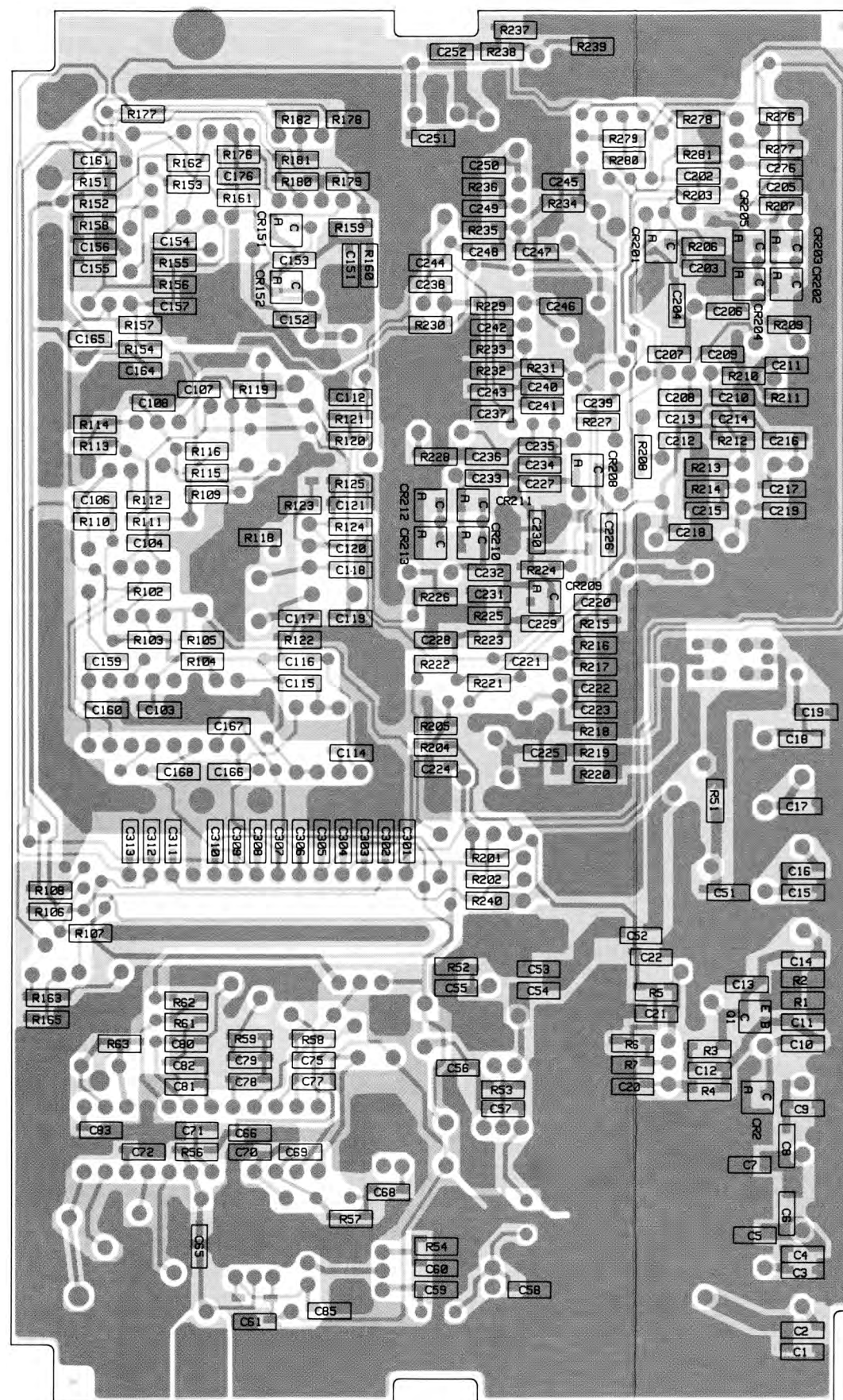


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 - (R) RECEIVE MODE
 - (T) TRANSMIT MODE
 - MEASURED IN THE RECEIVE MODE WITH AN ON-CHANNEL UNMODULATED SIGNAL AT A LEVEL OF -20 DBM.
 - MEASURED IN THE RECEIVE MODE WITH AN ON-CHANNEL SIGNAL AT A LEVEL OF -20 DBM, MODULATED WITH 1 KHZ AT 3 KHZ DEVIATION, MEASURED WITH AN AC RMS VOLTMETER.
 - VOLTAGES WITHIN BLOCKS MEASURED IN RECEIVE MODE WITH ON-CHANNEL SIGNAL AT LEVEL OF -47 DBM (1mV RMS), MODULATED WITH 1 KHZ AT 3 KHZ DEV. MEASURED WITH RF MILLIVOLTMETER AND RF BOARD IN CHASSIS.

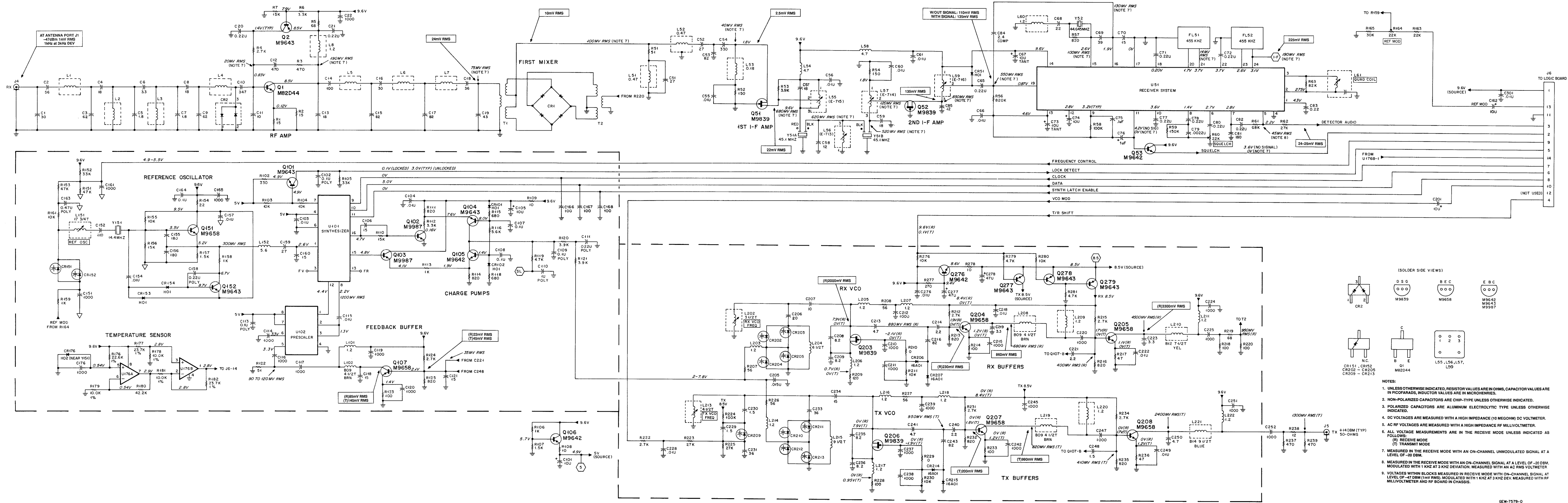


COMPONENT SIDE VIEW

SOLDER SIDE	RED	GAW-7702-O
COMPONENT SIDE	GREY	GAW-7701-O
OVERLAYS	BLACK	GDW-7703-O

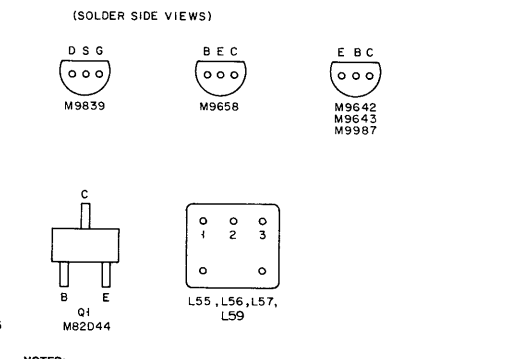


SOLDER SIDE VIEW

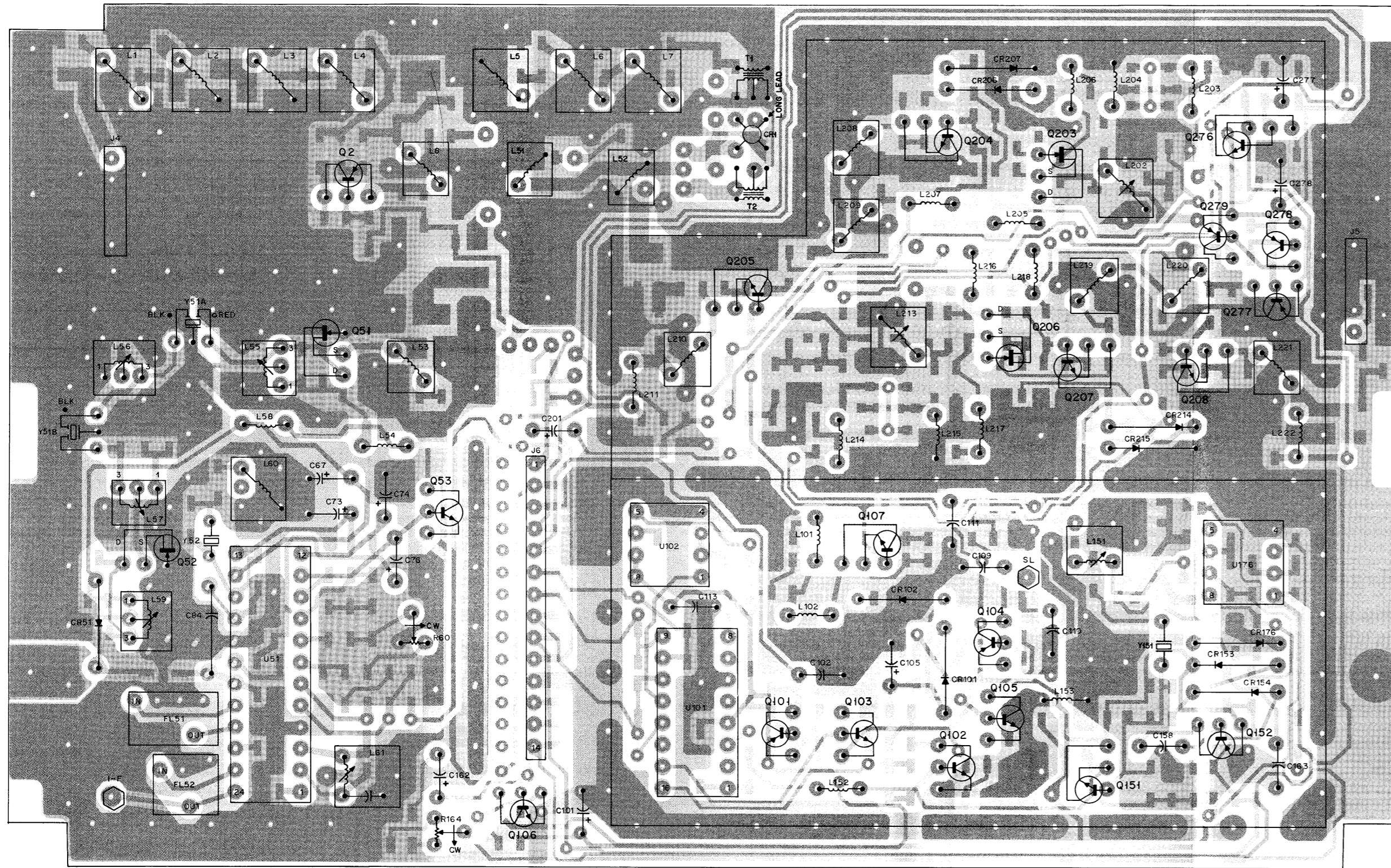


VHF RF Board Transistor D.C. Voltage Table

Transistor Ref. No.	VOLTAGE			VOLTAGE		
	BASE	EMITTER	COLLECTOR	GATE	SOURCE	DRAIN
Q1	.83	.12	8.5	—	—	—
Q2	7.9	8.5	1.1	—	—	—
Q51	—	—	—	0	1.8	9.6
Q52	—	—	—	0	1.8	9.6
Q53	4.2	3.6	9.6	—	—	—
Q101	5.0	5.0	.1 (LOCKED)	—	—	—
Q102	0.7	0	0	—	—	—
Q103	4.8	4.1	9.6	—	—	—
Q104	8.1	7.6	2-8v	—	—	—
Q105	1.4	1.9	2-8v	—	—	—
Q106	5.7	4.9	9.6	—	—	—
Q107	2.1	1.4	9.6	—	—	—
Q151	5.5	5.2	9.5	—	—	—
Q152	8.7	9.5	6.7	—	—	—
Q203	—	—	—	-2.1(R)	.7(R)	7.9
Q204	1.9(R)	1.2(R)	8.5	—	—	—
Q205	1.7(R)	1.1(R)	9.6	—	—	—
Q206	—	—	—	-1.9(T)	.95(T)	7.9
Q207	1.8(T)	1.2(T)	8.5	—	—	—
Q208	1.7(T)	1.2(T)	9.6	—	—	—
Q276	9.5	8.6	9.6	—	—	—
Q277	9.6	8.5(T)	8.5	—	—	—
Q278	9.6(R)	8.5	8.5	—	—	—
Q279	7.6(R)	8.5	8.5	—	—	—

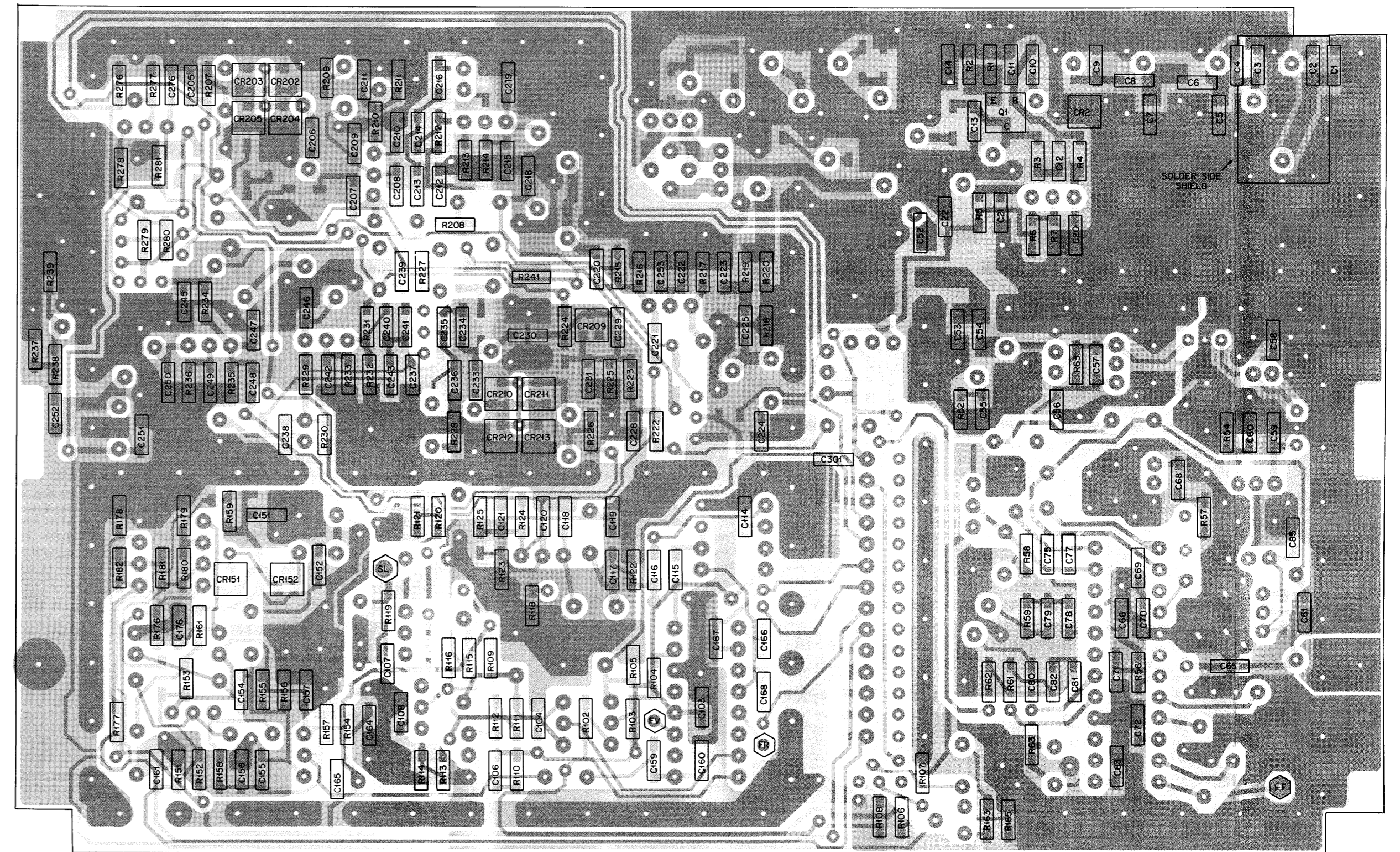


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 - MEASURED IN THE RECEIVE MODE WITH AN ON-CHANNEL SIGNAL AT A LEVEL OF -20 DBM, MODULATED WITH 1 KHZ AT 3 KHZ DEVIATION. MEASURED WITH AN AC RMS VOLTMETER.
 - VOLTAGES WITHIN BLOCKS MEASURED IN RECEIVE MODE WITH ON-CHANNEL SIGNAL AT LEVEL OF -47 DBM (TYP RMS), MODULATED WITH 1 KHZ AT 3 KHZ DEV. MEASURED WITH RF MILLIVOLTMETER AND RF BOARD IN CHASSIS.



SOLDER SIDE RED GAW-7714-0
 COMPONENT SIDE GRAY GAW-7715-0
 OVERLAY BLACK GDW-7716-0

COMPONENT SIDE VIEW

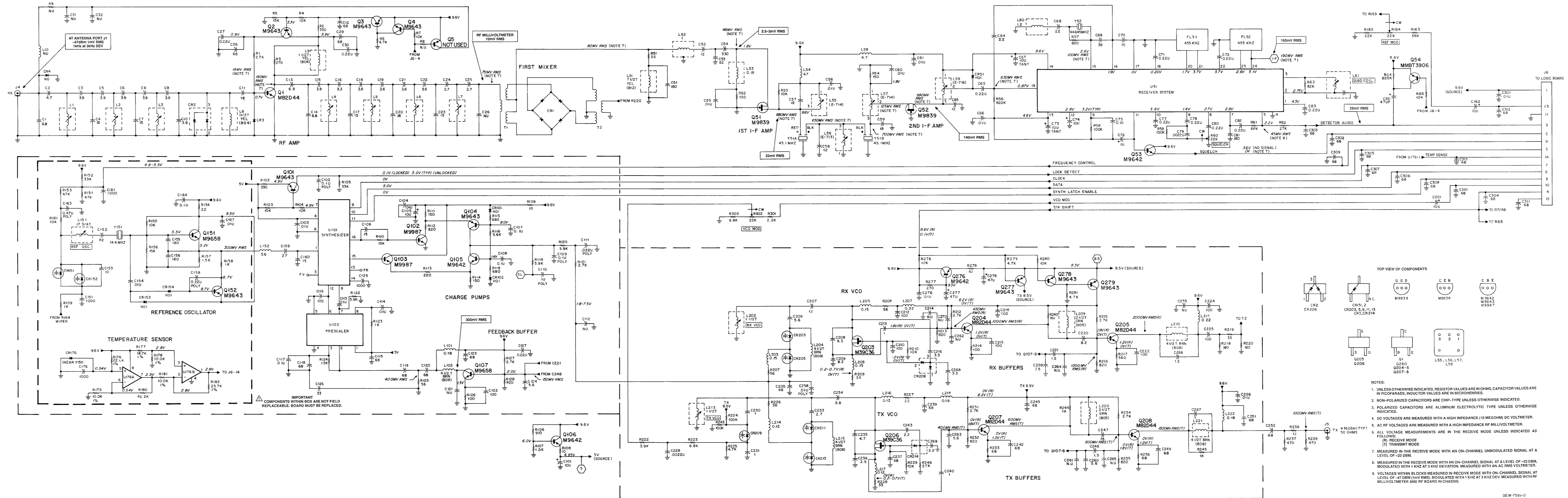


SOLDER SIDE RED GAW-7714-0
 COMPONENT SIDE GRAY GAW-7715-0
 OVERLAY BLACK GDW-7889-0

SOLDER SIDE VIEW

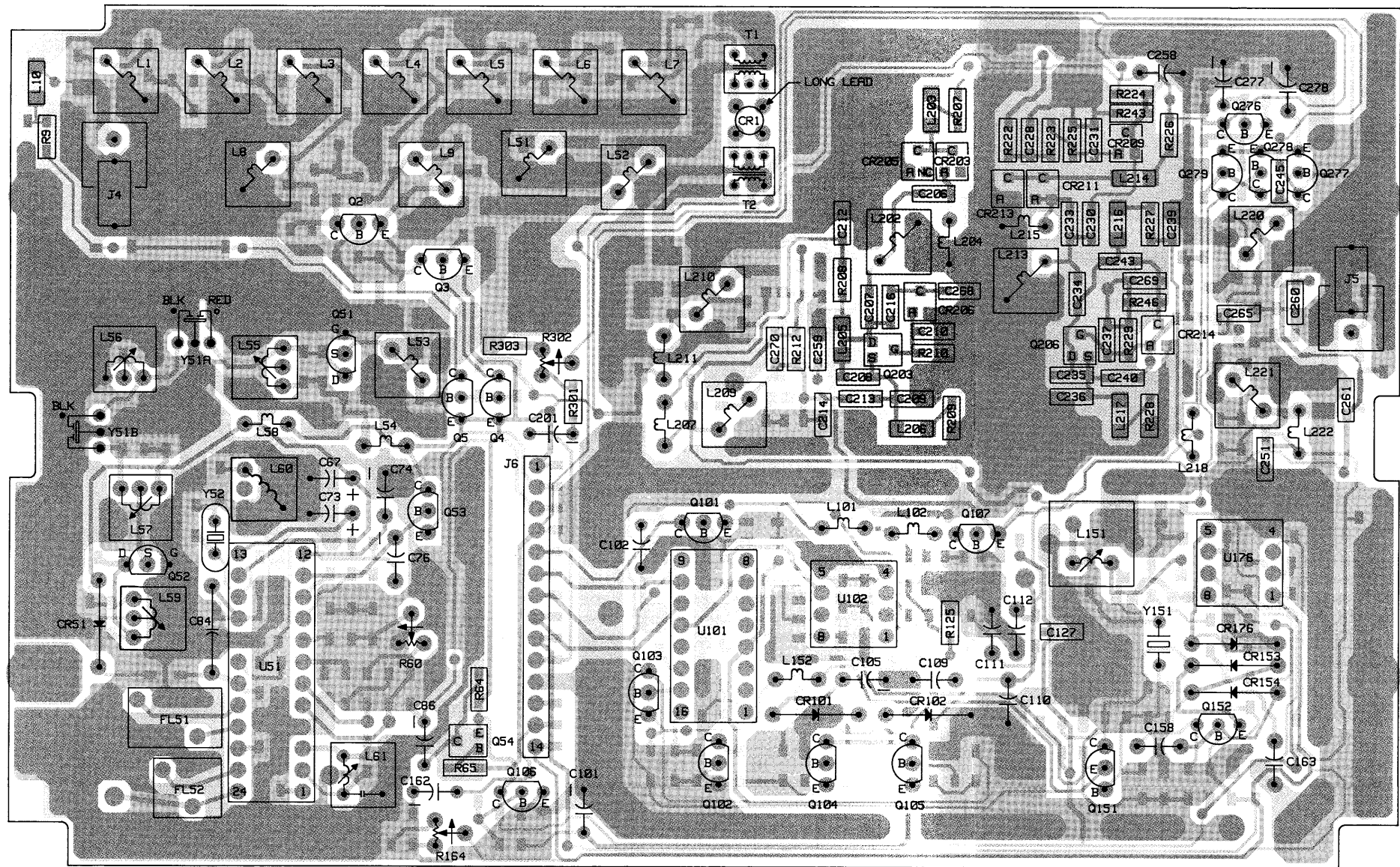
MaxTrac UHF RF Board Transistor D.C. Voltage Table

Transistor Ref. No.	VOLTAGE			VOLTAGE		
	BASE	EMITTER	COLLECTOR	GATE	SOURCE	DRAIN
Q1	.7	0	5.9	—	—	—
Q2	5.3	5.9	.9	—	—	—
Q51	—	—	—	0	1.8	9.6
Q52	—	—	—	0	1.8	9.6
Q53	0	0 (W/ SIG)	9.6	—	—	—
Q101	5.0	4.9	.1 (LOCKED)	—	—	—
Q102	.7	0	0.1	—	—	—
Q103	5.0	4.4	9.6	—	—	—
Q104	8.1	2.8V	2-8V	—	—	—
Q105	1.4	VAR.	2-8V	—	—	—
Q106	6.0	5.0	9.6	—	—	—
Q107	2.0	1.3	9.6	—	—	—
Q151	5.5	5.2	9.5	—	—	—
Q152	8.7	9.5	6.7	—	—	—
Q201	—	9.6	0(U) 9.3(L)	U=UPPER L=LOWER RANGE		
Q202	0(U) 7(L)	0	6.7(U) 0(L)	—	—	—
Q203	—	—	—	2.6(R)	4.8(R)	7.9(R)
Q204	1.8(R)	1.2(R)	8.2(R)	—	—	—
Q205	1.8(R)	1.2(R)	9.6	—	—	—
Q206	—	—	—	-5(T)	1.1(T)	7.8(T)
Q207	1.8(T)	1.2(T)	8.5(T)	—	—	—
Q208	1.8(T)	1.2(T)	9.6	—	—	—
Q276	9.5	8.6	9.6	—	—	—
Q277	9.6	8.5(T)	8.5	—	—	—
Q278	9.6	8.3	7.6(R)	—	—	—
Q279	7.6(R)	8.5	8.5	—	—	—



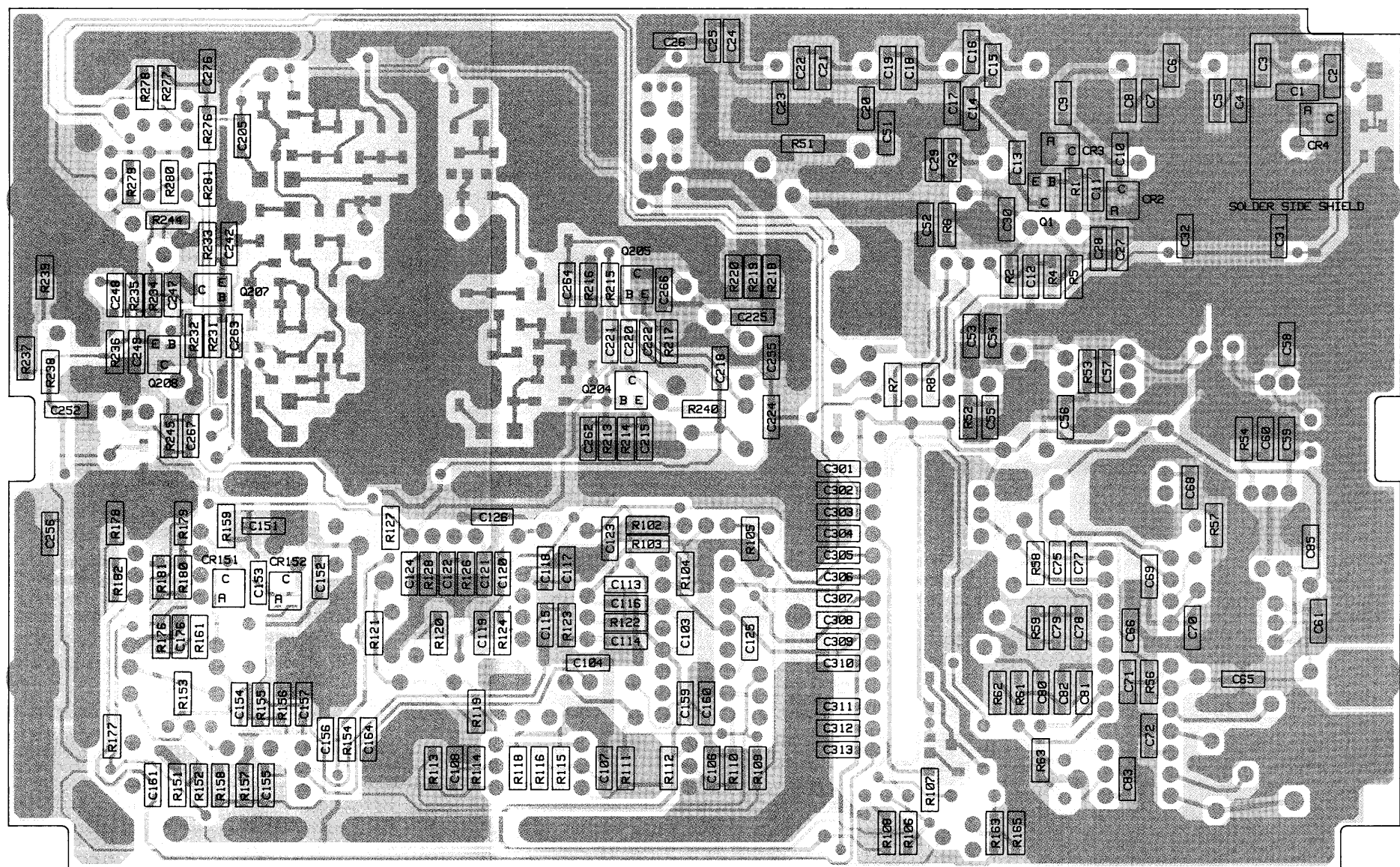
Schematic, Circuit Board Diagrams, and Parts List for HLE9310A UHF RF Board PW-7580-O (Sheet 1 of 3) 3/31/90

- NOTES:
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 - MEASURED IN THE RECEIVE MODE WITH AN ON-CHANNEL UNMODULATED SIGNAL AT A LEVEL OF -20 DBM.
 - MEASURED IN THE RECEIVE MODE WITH AN ON-CHANNEL SIGNAL AT A LEVEL OF -20 DBM, MODULATED WITH 1 KHZ AT 3 KHZ DEVIATION, MEASURED WITH AN AC RMS VOLTMETER.
 - VOLTAGES WITHIN BLOCKS MEASURED IN RECEIVE MODE WITH ON-CHANNEL SIGNAL AT LEVEL OF -47 DBM (1MV RMS), MODULATED WITH 1 KHZ AT 3 KHZ DEVIATION, MEASURED WITH RF MILLIVOLTMETER AND RF BOARD IN CHARGE.



SOLDER SIDE GCW-7617-O
 COMPONENT SIDE GCW-7616-O
 OVERLAY GCW-7618-O

COMPONENT SIDE VIEW

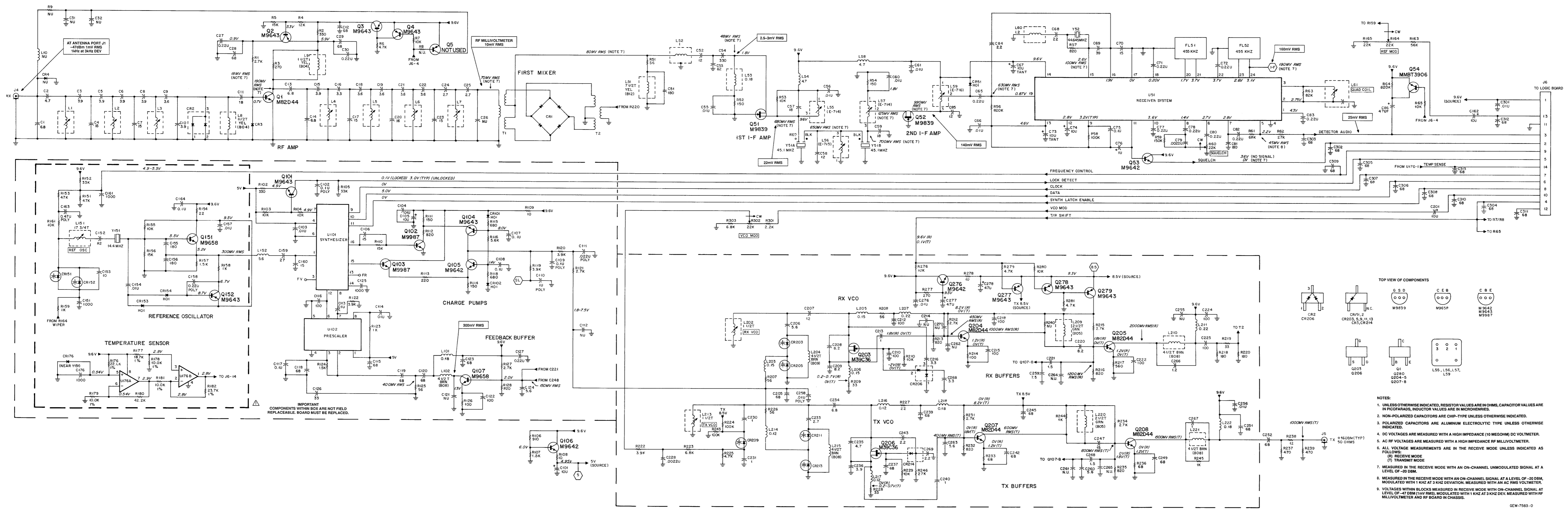


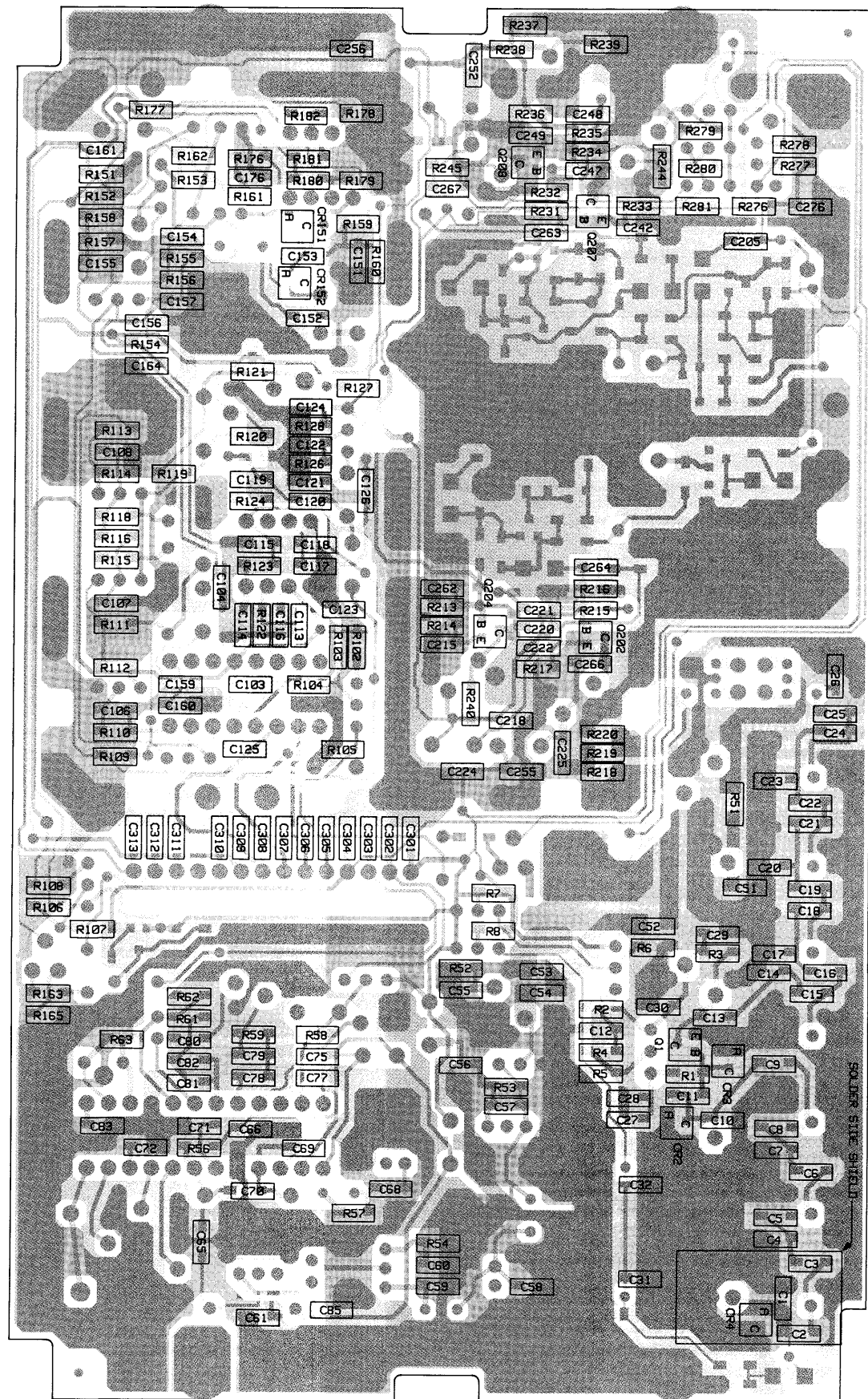
SOLDER SIDE GCW-7617-O
 COMPONENT SIDE GCW-7616-O
 OVERLAY GCW-7619-O

SOLDER SIDE VIEW

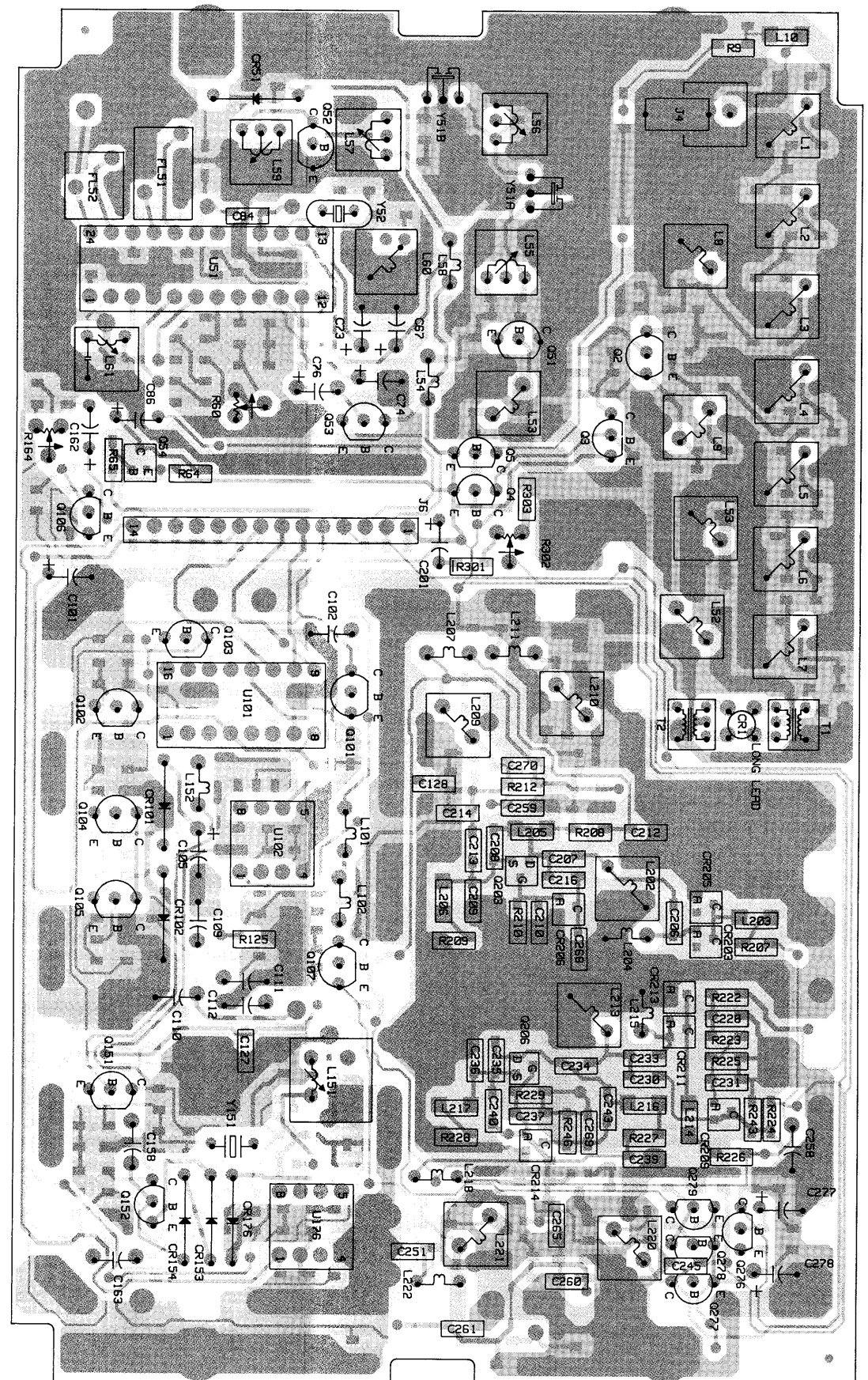
UHF RF Board Transistor D.C. Voltage Table

Transistor Ref. No.	VOLTAGE			VOLTAGE		
	BASE	EMITTER	COLLECTOR	GATE	SOURCE	DRAIN
Q1	.7	0	5.9	—	—	—
Q2	5.3	5.9	.9	—	—	—
Q51	—	—	—	0	1.8	9.6
Q52	—	—	—	0	1.8	9.6
Q53	0	0 (W/ SIG)	9.6	—	—	—
Q101	5.0	4.9	.1 (LOCKED)	—	—	—
Q102	.7	0	0.1	—	—	—
Q103	5.0	4.4	9.6	—	—	—
Q104	8.1	2.8V	2-8V	—	—	—
Q105	1.4	VAR.	2-8V	—	—	—
Q106	6.0	5.0	9.6	—	—	—
Q107	2.0	1.3	9.6	—	—	—
Q151	5.5	5.2	9.5	—	—	—
Q152	8.7	9.5	6.7	—	—	—
Q201	—	9.6	0(U) 9.3(L)	U=UPPER L=LOWER RANGE		
Q202	0(U) 7(L)	0	6.7(U) 0(L)	—	—	—
Q203	—	—	—	2.6(R)	4.8(R)	7.9(R)
Q204	1.8(R)	1.2(R)	8.2(R)	—	—	—
Q205	1.8(R)	1.2(R)	9.6	—	—	—
Q206	—	—	—	-5(T)	1.1(T)	7.8(T)
Q207	1.8(T)	1.2(T)	8.5(T)	—	—	—
Q208	1.8(T)	1.2(T)	9.6	—	—	—
Q276	9.5	8.6	9.6	—	—	—
Q277	9.6	8.5(T)	8.5	—	—	—
Q278	9.6	8.3	7.6(R)	—	—	—
Q279	7.6(R)	8.5	8.5	—	—	—





SOLDER SIDE VIEW



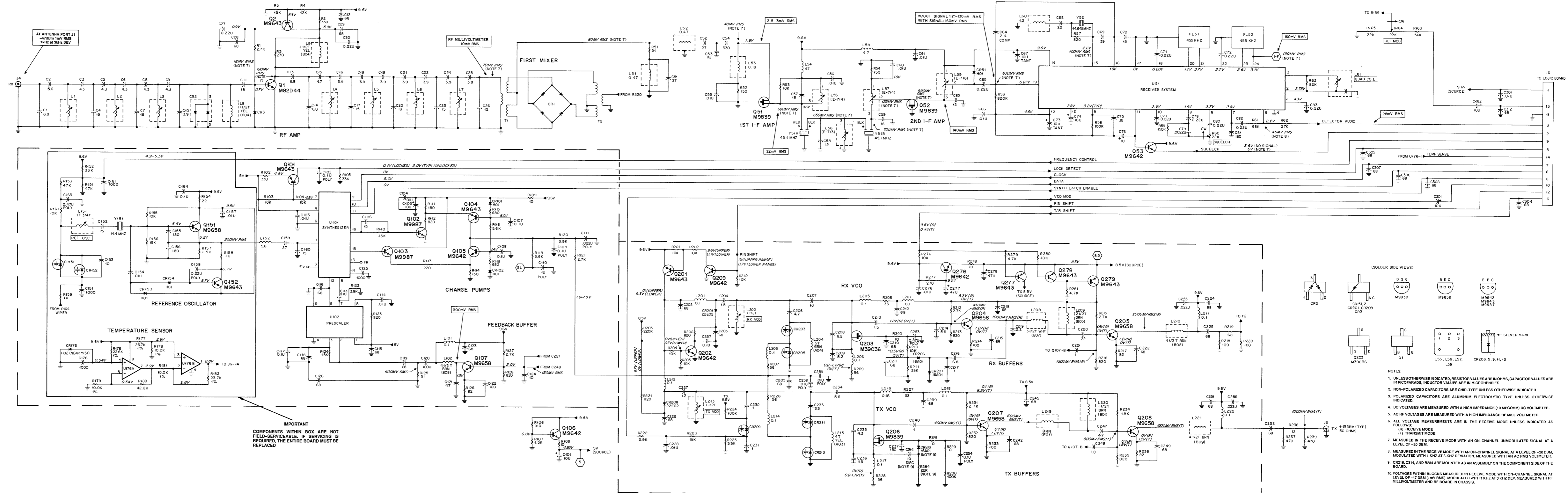
COMPONENT SIDE VIEW

Schematic, Circuit Board Diagrams, and
Parts List for HLE9310B UHF RF Board
PW-7582-O
(Sheet 2 of 3)
3/31/90

SOLDER SIDE RED GAW-7704-O
COMPONENT SIDE GREY GAW-7705-O
OVERLAYS BLACK GDW-7706-O

UHF RF Board Transistor D.C. Voltage Table

Transistor Ref. No.	VOLTAGE			VOLTAGE		
	BASE	EMITTER	COLLECTOR	GATE	SOURCE	DRAIN
Q1	.7	0	5.9	—	—	—
Q2	5.3	5.9	.9	—	—	—
Q51	—	—	—	0	1.8	9.6
Q52	—	—	—	0	1.8	9.6
Q53	0	0 (W/ SIG)	9.6	—	—	—
Q101	5.0	4.9	.1 (LOCKED)	—	—	—
Q102	.7	0	0.1	—	—	—
Q103	5.0	4.4	9.6	—	—	—
Q104	8.1	2.8V	2-8V	—	—	—
Q105	1.4	VAR.	2-8V	—	—	—
Q106	6.0	5.0	9.6	—	—	—
Q107	2.0	1.3	9.6	—	—	—
Q151	5.5	5.2	9.5	—	—	—
Q152	8.7	9.5	6.7	—	—	—
Q201	—	9.6	0(U) 9.3(L)	U-UPPER L-LOWER RANGE		
Q202	0(U) 7(L)	0	6.7(U) 0(L)	—	—	—
Q203	—	—	—	2.6(R)	4.8(R)	7.9(R)
Q204	1.8(R)	1.2(R)	8.2(R)	—	—	—
Q205	1.8(R)	1.2(R)	9.6	—	—	—
Q206	—	—	—	-5(T)	1.1(T)	7.8(T)
Q207	1.8(T)	1.2(T)	8.5(T)	—	—	—
Q208	1.8(T)	1.2(T)	9.6	—	—	—
Q276	9.5	8.6	9.6	—	—	—
Q277	9.6	8.5(T)	8.5	—	—	—
Q278	9.6	8.3	7.6(R)	—	—	—
Q279	7.6(R)	8.5	8.5	—	—	—

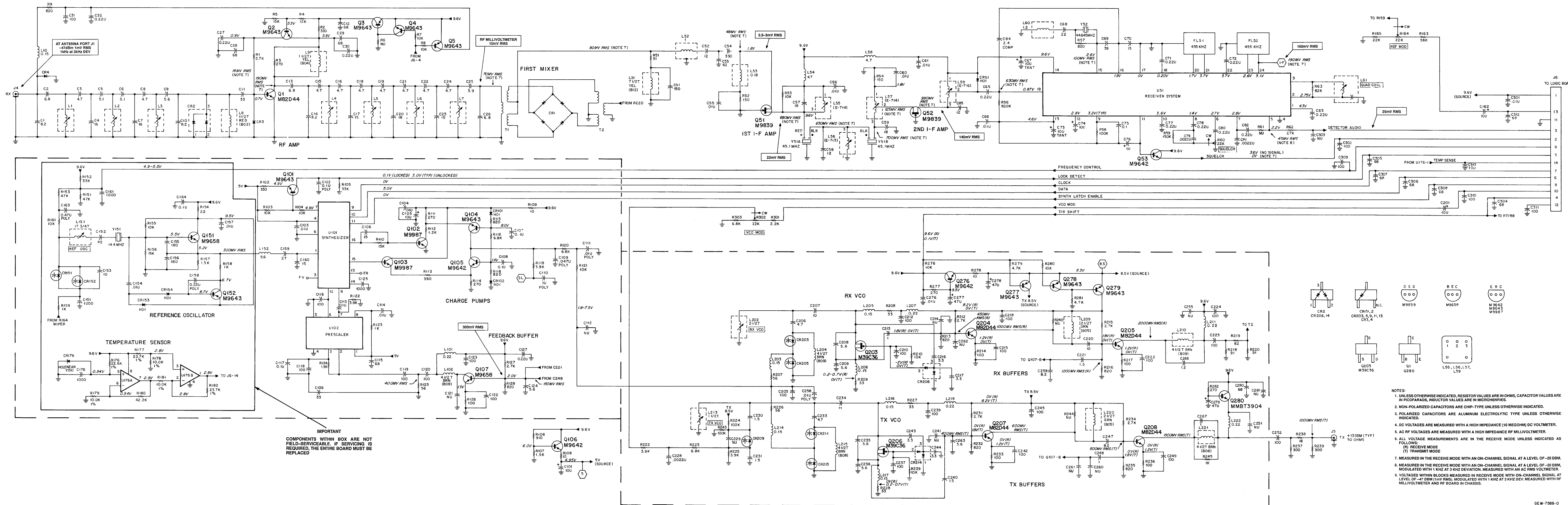


IMPORTANT
COMPONENTS WITHIN BOX ARE NOT FIELD-SERVICEABLE. IF SERVICING IS REQUIRED, THE ENTIRE BOARD MUST BE REPLACED.

- NOTES:
- UNLESS OTHERWISE INDICATED, RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN PROPORTIONS, INDUCTOR VALUES ARE IN MICROHENRIES.
 - NON-POLARIZED CAPACITORS ARE OHM-TYPE UNLESS OTHERWISE INDICATED.
 - POLARIZED CAPACITORS ARE ALUMINUM ELECTROLYTIC TYPE UNLESS OTHERWISE INDICATED.
 - DC VOLTAGES ARE MEASURED WITH A HIGH IMPEDANCE (10 MEGOHM) DC VOLTMETER.
 - AC RF VOLTAGES ARE MEASURED WITH A HIGH IMPEDANCE RF MILLIVOLTMETER.
 - ALL VOLTAGE MEASUREMENTS ARE IN THE RECEIVE MODE UNLESS INDICATED AS FOLLOWS:
(R) RECEIVE MODE
(T) TRANSMIT MODE
 - MEASURED IN THE RECEIVE MODE WITH AN ON-CHANNEL UNMODULATED SIGNAL AT A LEVEL OF -20 DBM.
 - MEASURED IN THE RECEIVE MODE WITH AN ON-CHANNEL SIGNAL AT A LEVEL OF -20 DBM, MODULATED WITH 1 KHZ AT 3 KHZ DEVIATION. MEASURED WITH AN AC RMS VOLTMETER.
 - CR14, CR14, AND R204 ARE MOUNTED AS AN ASSEMBLY ON THE COMPONENT SIDE OF THE BOARD.
 - VOLTAGES WITHIN BLOCKS MEASURED IN RECEIVE MODE WITH ON-CHANNEL SIGNAL AT LEVEL OF -47 DBM (100 RMS), MODULATED WITH 1 KHZ AT 3 KHZ DEV. MEASURED WITH RF MILLIVOLTMETER AND RF BOARD IN CIRCUIT.

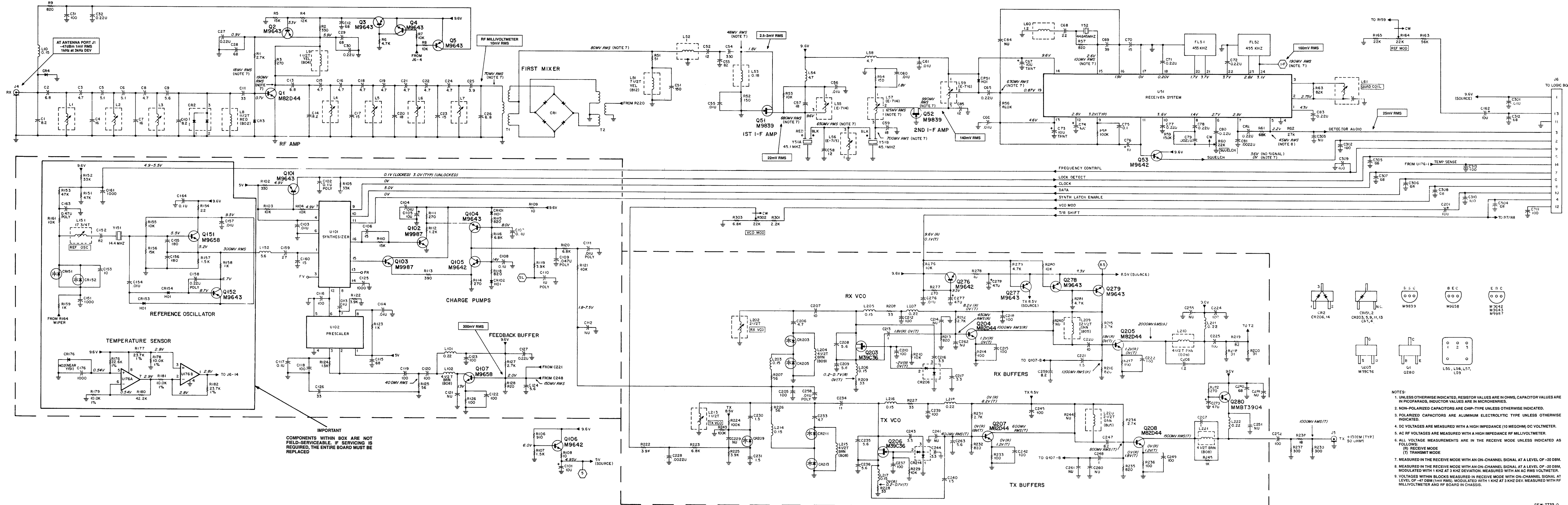
UHF RF Board Transistor D.C. Voltage Table

Transistor Ref. No.	VOLTAGE			VOLTAGE		
	BASE	EMITTER	COLLECTOR	GATE	SOURCE	DRAIN
Q1	.7	0	5.9	—	—	—
Q2	5.3	5.9	.9	—	—	—
Q51	—	—	—	0	1.8	9.6
Q52	—	—	—	0	1.8	9.6
Q53	0	0 (W/ SIG)	9.6	—	—	—
Q101	5.0	4.9	.1 (LOCKED)	—	—	—
Q102	.7	0	0.1	—	—	—
Q103	5.0	4.4	9.6	—	—	—
Q104	8.1	2.8V	2-8V	—	—	—
Q105	1.4	VAR.	2-8V	—	—	—
Q106	6.0	5.0	9.6	—	—	—
Q107	2.0	1.3	9.6	—	—	—
Q151	5.5	5.2	9.5	—	—	—
Q152	8.7	9.5	6.7	—	—	—
Q201	—	9.6	0(U) 9.3(L)	U=UPPER L=LOWER RANGE		
Q202	0(U) 7(L)	0	6.7(U) 0(L)	—	—	—
Q203	—	—	—	2.6(R)	4.8(R)	7.9(R)
Q204	1.8(R)	1.2(R)	8.2(R)	—	—	—
Q205	1.8(R)	1.2(R)	9.6	—	—	—
Q206	—	—	—	-5(T)	1.1(T)	7.8(T)
Q207	1.8(T)	1.2(T)	8.5(T)	—	—	—
Q208	1.8(T)	1.2(T)	9.6	—	—	—
Q276	9.5	8.6	9.6	—	—	—
Q277	9.6	8.5(T)	8.5	—	—	—
Q278	9.6	8.3	7.6(R)	—	—	—
Q279	7.6(R)	8.5	8.5	—	—	—



UHF RF Board Transistor D.C. Voltage Table

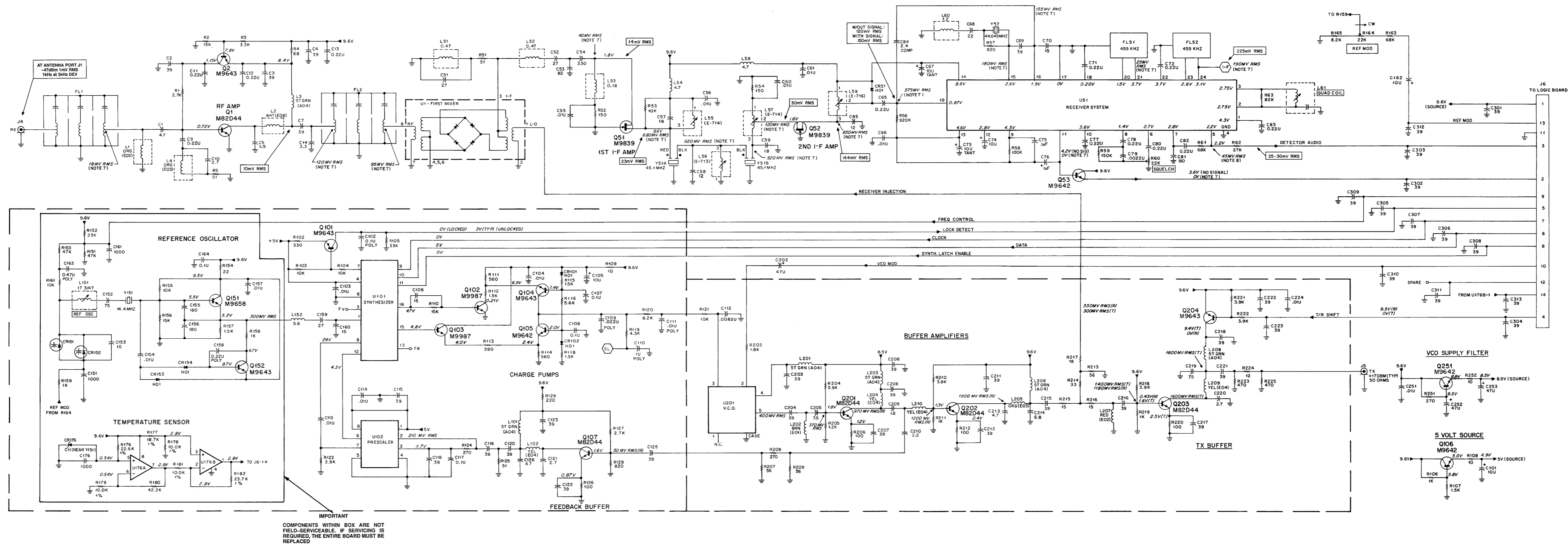
Transistor Ref. No.	VOLTAGE			VOLTAGE		
	BASE	EMITTER	COLLECTOR	GATE	SOURCE	DRAIN
Q1	.7	0	5.9	—	—	—
Q2	5.3	0	.9	—	—	—
Q51	—	—	—	0	1.8	9.6
Q52	—	—	—	0	1.8	9.6
Q53	0	0 (W/SIG)	9.6	—	—	—
Q101	5.0	4.9	.1 (LOCKED)	—	—	—
Q102	.7	0	0.1	—	—	—
Q103	5.0	4.4	9.6	—	—	—
Q104	8.1	2.8V	2-8V	—	—	—
Q105	1.4	VAR.	2-8V	—	—	—
Q106	6.0	5.0	9.6	—	—	—
Q107	2.0	1.3	9.6	—	—	—
Q151	5.5	5.2	9.5	—	—	—
Q152	8.7	9.5	6.7	—	—	—
Q201	—	9.6	0(U) 9.3(L)	U-UPPER L-LOWER RANGE		
Q202	0(U) 7(L)	0	6.7(U) 0(L)	—	—	—
Q203	—	—	—	2.6(R)	4.8(R)	7.9(R)
Q204	1.8(R)	1.2(R)	8.2(R)	—	—	—
Q205	1.8(R)	1.2(R)	9.6	—	—	—
Q206	—	—	—	-.5(T)	1.1(T)	7.8(T)
Q207	1.8(T)	1.2(T)	8.5(T)	—	—	—
Q208	1.8(T)	1.2(T)	9.6	—	—	—
Q276	9.5	8.6	9.6	—	—	—
Q277	9.6	8.5(T)	8.5	—	—	—
Q278	9.6	8.3	7.6(R)	—	—	—
Q279	7.6(R)	8.5	8.5	—	—	—



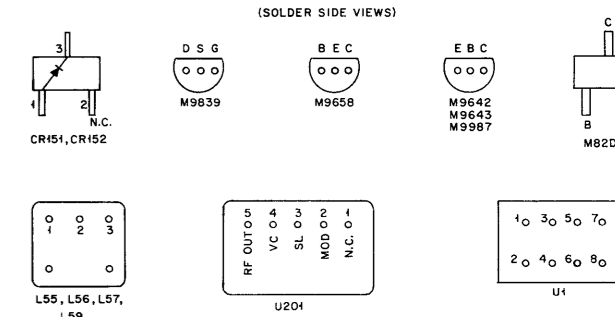
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800 MHz RF Board Transistor D.C. Voltage Table

Transistor Ref. No.	VOLTAGE			VOLTAGE		
	BASE	EMITTER	COLLECTOR	GATE	SOURCE	DRAIN
Q1	7.2	0	8.4	—	—	—
Q2	7.8	8.4	1.2	—	—	—
Q51	—	—	—	0	1.8	9.6
Q52	—	—	—	0	1.8	9.6
Q53	0(SIG)	0(SIG)	9.6	—	—	—
Q101	4.8	4.8	0(LOCK)	—	—	—
Q102	.72(R)	0	.21	—	—	—
Q103	4.8	4.0	9.6	—	—	—
Q104	7.4	6.9	2-8V	—	—	—
Q105	2.0	2.4	2-8V	—	—	—
Q106	5.8	5.0	9.6	—	—	—
Q107	1.6	.87	9.6	—	—	—
Q151	5.5	5.2	9.5	—	—	—
Q152	8.7	9.5	6.7	—	—	—
Q201	1.8	1.2	8.5	—	—	—
Q202	1.3	2.4	9.6	—	—	—
Q203	1.6(T)	2.5(T)	9.4(T)	—	—	—
Q204	9.5(R)	9.6	9.4(T)	—	—	—
Q251	9.5	8.8	9.6	—	—	—



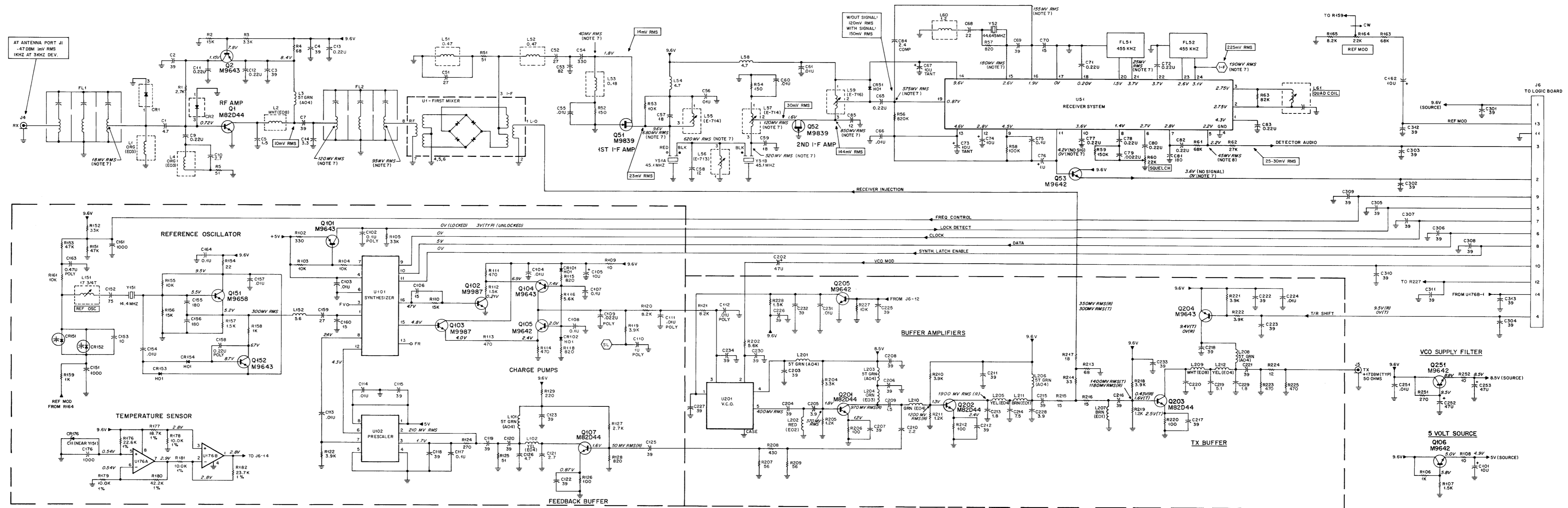
- NOTES:
- UNLESS OTHERWISE INDICATED, RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN PICOFARADS, INDUCTOR VALUES ARE IN MICROHENRIES.
 - NON-POLARIZED CAPACITORS ARE CHIP-TYPE UNLESS OTHERWISE INDICATED.
 - POLARIZED CAPACITORS ARE ALUMINUM ELECTROLYTIC TYPE UNLESS OTHERWISE INDICATED.
 - DC VOLTAGES ARE MEASURED WITH A HIGH IMPEDANCE (10 MEGOHM) DC VOLTMETER.
 - AC RF VOLTAGES ARE MEASURED WITH A HIGH IMPEDANCE RF MILLIVOLTMETER.
 - ALL VOLTAGE MEASUREMENTS ARE IN THE RECEIVE MODE UNLESS INDICATED AS FOLLOWS:
(R) RECEIVE MODE
(T) TRANSMIT MODE
 - MEASURED IN THE RECEIVE MODE WITH AN ON-CHANNEL SIGNAL AT A LEVEL OF -20 DBM.
 - MEASURED IN THE RECEIVE MODE WITH AN ON-CHANNEL SIGNAL AT A LEVEL OF -20 DBM, MODULATED WITH 1 KHZ AT 3% RIC DEVIATION, MEASURED WITH AN AC RMS VOLTMETER.
 - VOLTAGES WITHIN BLOCKS MEASURED IN RECEIVE MODE WITH ON-CHANNEL SIGNAL AT LEVEL OF -47 DBM (1mV RMS), MODULATED WITH 1 KHZ AT 3 KHZ DEV. MEASURED WITH RF MILLIVOLTMETER AND RF BOARD IN CHASSIS.



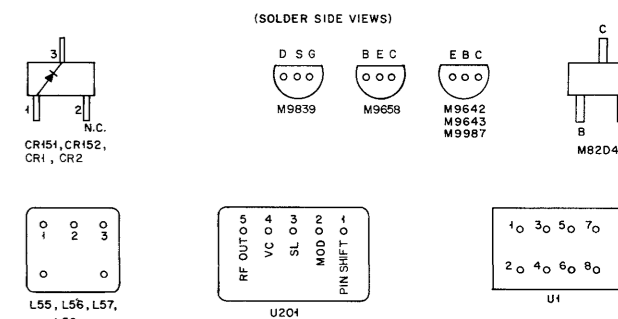
GEW-7590-D

800 MHz RF Board Transistor D.C. Voltage Table

Transistor Ref. No.	VOLTAGE			VOLTAGE		
	BASE	EMITTER	COLLECTOR	GATE	SOURCE	DRAIN
Q1	7.2	0	8.4	—	—	—
Q2	7.8	8.4	1.2	—	—	—
Q51	—	—	—	0	1.8	9.6
Q52	—	—	—	0	1.8	9.6
Q53	0(SIG)	0(SIG)	9.6	—	—	—
Q101	4.8	4.8	0 (LOCK)	—	—	—
Q102	.72(R)	0	.21	—	—	—
Q103	4.8	4.0	9.6	—	—	—
Q104	7.4	6.9	2-8V	—	—	—
Q105	2.0	2.4	2-8V	—	—	—
Q106	5.8	5.0	9.6	—	—	—
Q107	1.6	.87	9.6	—	—	—
Q151	5.5	5.2	9.5	—	—	—
Q152	8.7	9.5	6.7	—	—	—
Q201	1.8	1.2	8.5	—	—	—
Q202	1.3	2.4	9.6	—	—	—
Q203	1.6(T)	2.5(T)	9.4(T)	—	—	—
Q204	9.5(R)	9.6	9.4(T)	—	—	—
Q251	9.5	8.8	9.6	—	—	—



- NOTES:
- UNLESS OTHERWISE INDICATED, RESISTOR VALUES ARE IN OHMS, CAPACITOR VALUES ARE IN PICO FARADS, INDUCTOR VALUES ARE IN MICROHERRIES.
 - NON-POLARIZED CAPACITORS ARE CHIP-TYPE UNLESS OTHERWISE INDICATED.
 - POLARIZED CAPACITORS ARE ALUMINUM ELECTROLYTIC TYPE UNLESS OTHERWISE INDICATED.
 - DC VOLTAGES ARE MEASURED WITH A HIGH IMPEDANCE (10 MEGOHM) DC VOLTMETER.
 - AC RF VOLTAGE MEASUREMENTS ARE WITH A HIGH IMPEDANCE RF MILLIVOLTMETER.
 - ALL VOLTAGE MEASUREMENTS ARE IN THE RECEIVE MODE UNLESS INDICATED AS FOLLOWS: (R) RECEIVE MODE (T) TRANSMIT MODE
 - MEASURED IN THE RECEIVE MODE WITH AN ON-CHANNEL SIGNAL AT A LEVEL OF -20 DBM.
 - MEASURED IN THE RECEIVE MODE WITH AN ON-CHANNEL SIGNAL AT A LEVEL OF -20 DBM MODULATED WITH 1 KHZ AT 3 KHZ DEVIATION. MEASURED WITH AN AC RMS VOLTMETER.
 - VOLTAGES WITHIN BLOCKS MEASURED IN RECEIVE MODE WITH ON-CHANNEL SIGNAL AT A LEVEL OF -47 DBM (10V RMS), MODULATED WITH 1 KHZ AT 3 KHZ DEV. MEASURED WITH RF MILLIVOLTMETER AND RF BOARD IN CHASSIS.



GEW-7592-0

