1. Theory Of Operation

The Logic Board consists of 5 segments:

- Microprocessor
- Voltage regulation
- Receive audio circuitry
- Transmit audio circuitry
- Power control circuitry

1.1 MICROPROCESSOR

1.1.1 Description

MaxTrac radios use the Motorola 68HC11A8 microprocessor U802, which consists of:

- 8 MHz Clock rate
- Multiplexed 8 bit address/data lines
- 16 bit addressing
- Internal watchdog circuitry
- Analog to digital input ports.

The control logic surrounding U802 consists of:

1) Custom Gate Array U803. This device expands the input/output capabilities of the control logic. U802 and U803 exchange information which tells the microprocessor the input port status and the desired state of the output ports.

2) NOVRAM U805. This is a Non-Volatile Random Access Memory device which consists of a static RAM with a built-in lithium battery to maintain its memory after removing power. The NOVRAM acts as the radio’s code plug, storing any operating information pertinent to a particular radio. This information includes operating frequencies, control channels, time out timer, and other special functions.

(3) EPROM U804. This is an Erasable Programmable Read Only Memory. U804’s function is to store the microcomputer’s operating program.

(4) Static Random Access Memory U806. This RAM is used for scratch pad operations in the trunked MaxTrac.

(5) Digital-to-Analog IC U801. This IC is used to generate precision analog voltages.

1.1.2 Operation

When the radio is connected to the battery, UNSW B+ is applied via J7–5 and to zener diode VR402 and R410. The voltage produced from zener diode VR402 is +5 volts and is labeled RAM 5V. RAM 5V is sent to the microprocessor U802 and is used to maintain the radio’s current operating conditions (scan list, current mode, etc.). This voltage will be present as long as the battery voltage is present to the radio.

1.1.3 Power Up/Low-Line Reset

When the radio is turned on, the +5V DC is turned on. This will charge up C858 through R893. The time constant established by C858 and R893 will be of long enough duration for C858’s charge to pass the +3.2V DC reference voltage on U807A’s negative input. RESET line is held low while this is taking place and enough time elapses so that the microcomputers clock and all other voltages stabilize before the internal program starts running. When C858’s charge goes above +3.2V DC, RESET goes inactive where it will remain during normal operation.

If SWB+ should decrease in voltage, the decrease will be sensed on the positive input to U807B. The decreased output from U807B will go to the positive input to U807A. This voltage will be compared to the +3.2 reference voltage. If this voltage should decrease below +3.2V DC, RESET will go low and reset the Custom Gate Array U803 and Microcomputer U802. The MaxTrac 800 series has the Power Up/Low line RESET circuitry built into the +5V DC regulator U402.

1.1.4 Microcomputer Start-Up Routine

The microcomputer is stabilized and operational after the RESET line is released to an inactive state. Y801, the crystal oscillator, should be stable at this point. The frequency of
Y801 is divided by four with circuitry internal to U802. The resultant frequency is called the “E CLOCK” and can be seen at U802–5. This frequency is used by the Microcomputer and Custom Gate Array as an internal data clock.

The Microcomputer will then do a self test of the control logic. If any failure is detected, an error tone will sound. Refer to the ERROR TONES tables for more information.

1.1.5 Microcomputer Normal Operation

A successful self test of the control logic will activate the multiplexed address/data bus. The Microcomputer comes equipped with an eight bit address/data bus and an eight bit address only bus. These bus lines are connected to the Custom Gate Array for I/O port information and the external memory IC’s to send and receive data.

The Custom Gate Array must de–multiplex the lower order address byte from the address/data bus (ADO–AD7) in order to address a particular function or memory location.

The Microcomputer puts the address information on ADO–7 and the information is then passed to U803. The Address Strobe “A$” is pulsed low and the byte is latched. The de–multiplexed address byte A0–7 is then available on U803. The bus is now ready for the transmission of data. The higher order address byte A8–A15 is not multiplexed and is readily available at the Microcomputer U802.

1.1.6 Reading Or Writing In Memory

The specified memory IC must first be enabled before a read/write operation can take place. Each memory IC has it’s own “chip select” line. SRAM SEL originates at U803–15, NOVRAM SEL at U803–14, and EPROM SEL at U803–13. These lines will all remain logic level high until one is pulsed low to select the IC chosen.

The R/W line which originates from U803–16, tells the system what operation is being performed. If a read condition exists, the R/W line will go logic level high. If a write condition exists, R/W line goes low. In the case of EPROM U804, it is a read only memory and does not require a R/W input.

The Output Enable line “OE” will enable the tri–state output gates to pass the contents of the desired address out onto the A/D, analog to digital, bus. This line is active when pulsed low.

1.2 VOLTAGE REGULATION

The source for B+ is taken off the ignition sense jumper JU801. It is then passed to the switch PCB via J8–6 and is routed to one side of the on/off switch. The output, SWB+, comes back into the logic board via J8–5.

U402, on the logic board, is the +5 volt regulator. SWB+ is applied to U402 and the +5V DC output is sent out to the logic board, RF board, and display boards.

When SWB+ is applied to U401A–8, the +9.6V DC regulator will turn on and produce a positive voltage input. This output is divided by CR402, R404, and R405. The voltage drop across R405 is then sent into the negative input of U401A. Zener diode VR401 will produce a +5.03 reference voltage for the positive input. The 9.6 volt sample is compared to the reference and an error voltage inversely proportional to the status of the +9.6 volt rail is generated at U401A–1. This error voltage will turn on and control the conduction of Q402. The higher the drive voltage, the harder Q402 conducts. Q402 controls the amount of conduction through Q401. The harder Q401 conducts, the higher the +9.6 volt line will go.

If the +9.6 volt line should increase, the voltage at U402–2 would rise causing the voltage at U402–1 to decrease. Q401 will now source less current and reduce the +9.6 volt line drops.

Diode CR401 is used to protect Q401 in the event that the 9.6 volt line should be grounded. When this happens, Q402’s base can only be .7V DC maximum and Q401 will turn off.

The +4.8V DC is formed by the divider network of R408 and R409. This voltage is fed into the unity gain op amp U401B. Isolation and current amplification take place at U401B.

1.3 RECEIVE AUDIO FILTER

The detected audio is applied to the receiver audio filter on the logic board via J6–3. The filter consists of a 3 kHz low pass filter U551, a 300 Hz high–pass filter U552, a de–emphasis circuit U553A and audio mute gate circuit consisting of Q551 and Q552. U553B sums the detected audio signal with the alert tone generated by the microprocessor U802. The 3 kHz low pass filter U551, is necessary to filter any unwanted high frequency noise from reaching the speaker. The 300 Hz high pass filter U552 restricts PL/DPL tones from reaching the speaker. The receiver audio mute gate, Q551, and Q552, operates by switching out the detected audio signal from the audio power amplifier. The microprocessor controls the “RX Mute” line out of U803–6. This line goes high during unmuted mode causing Q551 and Q552 to turn on. PL/DPL along with the squeal setting will cause the microprocessor to switch “RX Mute” line. The filtered audio is then routed to the audio power amplifier via U553B and the volume control pot.

1.3.1 Audio Power Amplifier

The audio power amplifier is a Class A−B amplifier with a differential input stage. Input to this stage comes from the volume control potentiometer wiper which is connected to J8–2.

The audio signal is routed through C501, C501, C502, and R501 are used to form an active filter with a 12 dB/octave roll off below 300 Hz to help attenuate the PL tones.

Capacitors C503, C505, C506, C511, C512, and C513 are used to prevent high level RF from causing the small signal diode junction to degrade audio amplifier performance.
Capacitor C507 and resistor R507 set the power amplifiers closed loop AC gain to 27 dB. The amplifier is a non-inverting type whose AC gain is determined by the equation:

$$V_{out} = \frac{(R508 + R507)}{R507} \times V_{in}$$

Transistors Q501 and Q502 are a small signal differential pair. The half supply voltage reference for Q501 is set by R502 and R503. C504 is used to remove any alternator whine from the half supply reference voltage. Q502 receives 100% DC feedback from the output via R508. R504 and R508 are the same value to help maintain the best differential offset so that the DC output voltage is exactly half-supply voltage as set by the reference voltage at Q501.

Q503 is a Class A driver that causes the output stage to swing within one volt of supply and ground reference. To fully saturate the upper complimentary output pair Q506 and Q504, C509 is used to allow the junction of R509, R510, and C509 to swing about 3 volts higher than supply voltage. C510 from the collector to base of Q503 is a Miller effect capacitance causing the open loop gain to roll off at about 3 kHz and guarantee the amplifier's stability under all open loop operating conditions.

The pre-drivers Q504 and Q505 are Class A and help prevent low level crossover distortion. At high level signals, crossover will be caused by Class B amplifiers Q506 and Q507. The large amount of negative feedback relative to the close loop gain keeps distortion low. The open loop gain is approximately 80 dB and the close loop gain or operating AC gain is 27 dB. There is about 53 dB of negative feedback to help reduce distortion of the output from Q506 and Q507.

The output stage of the audio power amplifier consists of complimentary Darlington pairs in a push–pull configuration. The upper pair consists of the PNP power device Q506 and small signal NPN driver Q504. Together they work like an NPN power device. The compliment of Q506, Q504 is made up of NPN power device Q507 and PNP small signal device Q505. Together this pair works like an NPN power device. Q506 and Q507 are biased at .2 volts base to emitter and are turned off at DC or small signal AC drive levels. At high AC signal levels, Q506 and Q507 turn on. The pre-drivers Q504 and Q505 are biased off by CR501 and CR502. The bias current is stabilized by emitter feedback resistors R513 and R514. Diodes CR501 and CR502 are placed near transistors Q504, Q505, Q506, and Q507. They help the output stages from turning on to large DC currents as the output stages become hot.

Q508 and Q509 are low current switches controlled by the PA MUTE line from the microprocessor. The audio amplifier can be turned on or off by PA MUTE in about 5 milliseconds. PA MUTE is affected by the PL/DPL and squelch circuitry.

C514 couples the output signal from the audio power amplifier to the speaker. It also provides DC blocking to the speaker and couples the AC signal down to 80 Hz in frequency.

1.3.2 Low-Speed Data Filter

This circuit filters the signal higher than 300 Hz from the detected audio with a low pass filter (U602B and U603A). The PL tone between 67–257 Hz or DPL signal between 10–140 Hz is covered. The signal is then pulse shaped to 5V p/p by U603B and Q601. The PL/DPL signal is then routed to the microprocessor U802–33 via R839 (DLO RX). U602A is a PL/DPL cancellation circuit for duplex radios so that the receiver does not decode its own PL/DPL signal modulating the reference oscillator. In duplex radios, the receiver and transmitter VCO are in operation simultaneously. A reference modulation signal will be seen in both the receiver injection and transmitter output. The receiver will detect this reference modulation and without the cancellation effect provided by U602A, will be given a PL decoding error.

1.3.3 High Speed Data Filter

U601A contains the circuitry for the High Speed Data filter. Data sent to this circuit can be information such as the MDC data found in certain special options or the different handshakes found in the trunking signaling scheme for trunked radios. U601A's output is a 5V p/p pulse which is routed and processed by the microprocessor.

1.4 TRANSMIT AUDIO

The microphone signal is made available to the emitter of Q651 and allowed to pass by turning Q652 on via the MIC EN during the transmit mode. The MIC signal gets pre-emphasized, amplified and limited by U651A. The output is then fed into summation amplifier U652A and voltage control attenuator U653A. The VCA controls the signal level fed to the transmitter VCO for modulation. Voltage changes at U653–3 change the attenuation of the MIC signal. This controlled signal is filtered by the splatter filter U652 to get rid of high frequency signals. The output of U652B goes to P6–10 as VCO Modulation. The Reference Modulation is routed from U651A to P6–13.

1.4.1 High-Speed Transmit Data

High-Speed Transmit Data from the microprocessor is applied to U701A. The output of U701A is routed to the summation amplifier U652A.

1.4.2 Low-Speed Transmit Data

The PL and DPL data from the microprocessor is applied to U701B. U701B takes the PL and DPL data and transforms it into a four step stair-step waveform. This stair-step waveform is applied to U651B where it is turned into a PL tone or the analog representation of the DPL code. The output of U651B is applied to the summation amplifier U652A.
1.5 POWER CONTROL CIRCUIT

The power control circuitry used to control the RF power amplifier is explained in detail in the Power Amplifier section of this manual.

2. Troubleshooting Guide

2.1 MICROPROCESSOR SECTION

The MaxTrac radio uses a microprocessor U802, along with support IC's. U803, the Custom Gate Array, U804 the EPROM, and U805 the NOVRAM.

Most of the problems encountered in this section will be difficult to localize to one particular device. All the devices interact with each other by passing information back and forth on the bus lines.

A very common problem encountered is the Code Plug Error. This is characterized by a 163 Hz tone for a 5 second duration. The ERROR TONE charts will help the servicer in isolating to the Logic Board but will not give the exact IC at fault. The Code Plug information is contained not only in the microprocessor but the NOVRAM as well.

Replacement of the Logic Board is the safest way to make sure the problem is fixed. Before replacing the board, the servicer can attempt to reprogram the radio code plug. Stepping through the Radio Service Software's service menu will sometimes clear the fault if the microprocessor is not the problem. The RF Board Level Replacement procedures can also be followed step by step. Sometimes a system fault can be cleared this way. If these procedures do not clear the problem, board replacement and re-calibration must be done.

Other error tones will point to problems that can be traced back to defective IC's or components not actually in the shielded area of the Logic Board. By observing the logic voltage levels and waveforms on the schematics, the fault can be found.

2.2 RECEIVE AUDIO

Troubleshoot the Receive Audio path by observing voltage and waveforms on the schematics. Troubleshooting chart “BAD SQUELCH OR PI/DPL” will help isolate to a specific section. Review the theory of operation before attempting to find the faulty component.

2.3 TRANSMIT AUDIO

The Transmit Audio path is also serviceable by using the “BAD TX MODULATION” troubleshooting chart and schematics. By inserting a tone from an external oscillator and by passing the microphone, the servicer can keep a consistent tone and amplitude as he troubleshoots through the different stages.

2.4 AUDIO POWER AMPLIFIER

Troubleshoot the Receive Audio Power Amplifier using the “NO/LOW AUDIO” chart and the schematics and theory of operation. To help isolate which stage the problem is in under full power out conditions, use a dummy load instead of a speaker and monitor the voltage on the load.

2.5 POWER CONTROL CIRCUITRY

Refer to the Transmitter Troubleshooting section to isolate problems in the Power Control Circuity part of the Logic Board. This power control loop is very difficult to troubleshoot without breaking the loop and inserting a fixed voltage to certain parts of the circuit. Follow the schematic and theory of operation carefully. Voltages on each device are noted and can be used for comparison.