



MOTOROLA INC.

Communications
Sector

MULTI-CODED SQUELCH MODULE

OPTION C369AA FACTORY INSTALLED

MODEL TLN2704A FIELD INSTALLED

Option C369AA Model Complement

Item	Description
TLN2420A	Multi-Coded Squelch Module (MCS)
TRN5182A	Escutcheon
TRN5844A	Code Plug

TLN2704A Model Complement

Item	Description
TLN2420A	Multi-Coded Squelch Module (MCS)
TRN5182A	Escutcheon
TRN5194A	Station Control Code Plug
TRN5843A	Miscellaneous Parts
TRN5844A	MCS Code Plug

TLN2420A MCS Breakdown

Item	Description
TRN4372A	Digital to Analog Hybrid
TRN5180A	MCS Circuit Board
TRN5181A	MCS Software Program EPROM

1. DESCRIPTION

1.1 INTRODUCTION

The Multi-Coded Squelch (MCS) module is an option to the *MSF 5000* Base Station/Repeater. A C369AA factory or TLN2704A field installed module adds the capabilities of detecting PL/DPL modulation on the received rf carrier frequency, generating PL or DPL codes for the transmitter carrier frequency, and responding to inputs other than PL/DPL detection.

1.2 PHYSICAL

The MCS option consists of software changes to the base station's control board and the addition of a MCS board to the expansion tray. The software change is accomplished by replacing two pre-programmed ROMs on the station control board. The expansion tray with MCS board (inside tray) is shown in Figure 1.

1.3 ELECTRICAL

The MCS board is microprocessor controlled and contains a full complement of RAM and ROM integrated circuits for data and program storage. A single 34 pin ribbon cable interconnects the board to the electronic circuitry of the station.

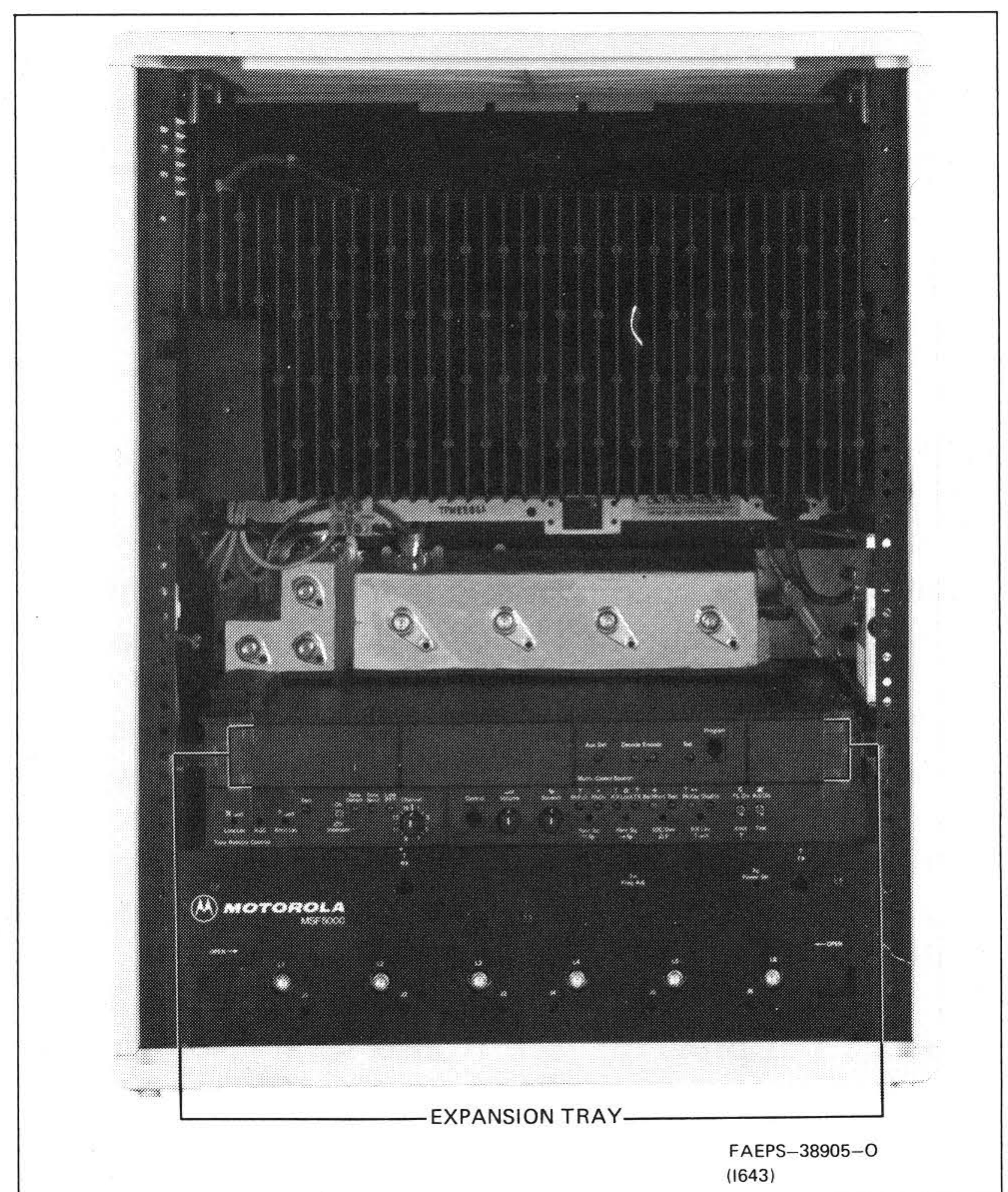


Figure 1. Internal View of Typical MSF 5000 Base Station with Expansion Tray

1.4 FUNCTIONAL

The module can identify 30 PL codes and any 24 of all the possible DPL codes. Upon detection of a PL/DPL code on the carrier, the module checks a user defined list

(code plug) to determine what action is to be taken. If the PL/DPL code detected is not enabled in the list, the module will continue searching until a valid code is received.

Upon detection of a valid code, the module will execute a series of commands defined by the user in the module's code plug. By properly defining the commands, the MCS module can be configured as a multi-user repeater and/or perform multi-PL/DPL functions.

The MCS module incorporates an Electrically Erasable Programmable Read Only Memory (EEPROM) as a code plug. An onboard serial interface allows code plug information to be changed at the site without removing the module. The following attributes are code plug definable: enabling/disabling individual users, PL/DPL code decoded, PL/DPL code encoded, time-out timer for each user, priority access, and channel mapping.

Multi-Coded Squelch LEDs are color coded according to their function. A red LED is on to indicate a servicing or failure status and green LEDs are on to show active operation of the named signal.

CAUTION
DO NOT ALLOW STATION TO CONTINUE OPERATION WITH RED LED ON.

Four LEDs are present (See Figure 2) on the front panel of the Multi-Coded Squelch module and have the following functions. The TEST LED (red) is off during normal station operation and is used to give station diagnostic information. The DECODE LED (green) indicates that the processor is successfully decoding a PL or DPL signal. Likewise, the ENCODE LED (green) indicates that the processor is actively encoding a PL or DPL code. The AUX DET LED (green) is reserved for future expansion. During a Multi-Coded Squelch module reset, all four LEDs will momentarily turn on, indicating that the LEDs are operational.

The six pin program jack is also located on the front panel. The connector allows access to the on-board serial interface. A portable programming terminal can be plugged into this jack to change the code plug contents of the MCS board. NOTE. A local handset should not be plugged into this jack. While no harm will be done, the handset will not function properly.

1.5 FEATURES

1.5.1 General

- Serves both multi-user repeater and multi-PL/DPL requirements.
- 30 PL codes and 24 DPL codes at 12 dBq

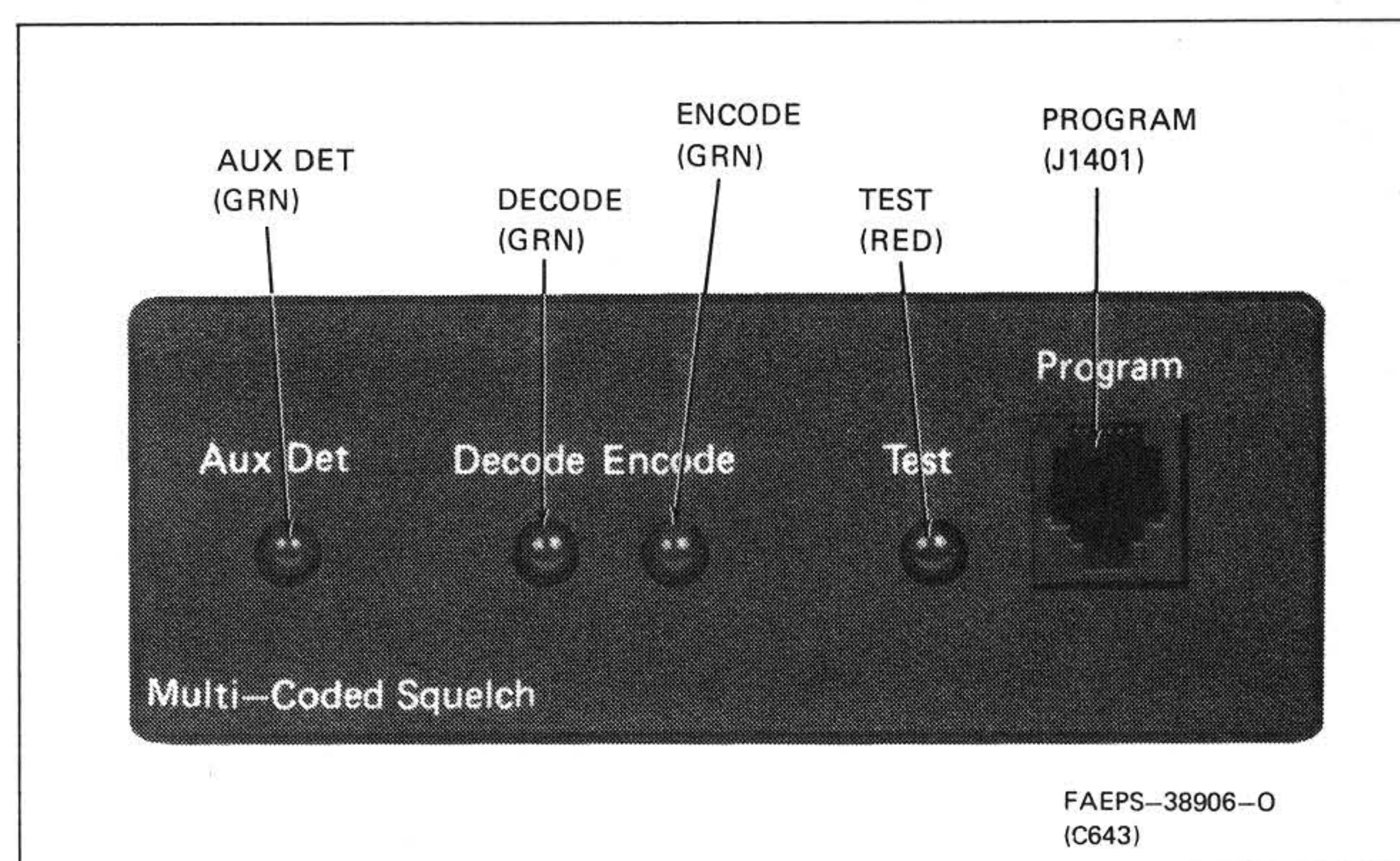


Figure 2. Front Panel of Multi-Coded Squelch Module

- DPL capability at 6 dBq.
- Code regeneration—cross coding—all combinations

1.5.2 Service/Diagnostics

- Self diagnostics on power up
- Capability for keying with selected PL/DPL code
- Front panel LEDs—module status
- R1800 compatible

1.5.3 On-Site Programming

- EEPROM allows convenient programming
- Each user's characteristics easily changeable
 - Add or delete users
 - Individual TOT and lockout capability
 - PL/DPL decoded
 - PL/DPL encoded
 - Priority user access
 - Channel Mapping

1.5.4 Expanded Functions

- Read/write to *MSF 5000* MUXbus control
 - Wild Card bits
 - Status of station (repeater setup/knockdown)
- Reset and idle functions executable—allows action independent of PL/DPL detection.
- Functions allow defined sequences to occur—i.e. keying the station, reset of entire station, etc.

- Direct control of other on board functions—i.e. IPCB, etc.
- Flexible—code plug definable

2. INSTALLATION (FIELD)

(Refer to the *MSF 5000* Instruction Manual for Station Assembly Detail)

2.1 INTRODUCTION

The installation procedure consists of modifying the existing station control board and mounting the Multi-Coded Squelch (MCS) board into the expansion tray. Modifications to the station control board must be made to permit operation with the MCS board. Specifically, the station control program ROM (U804) and the station control code plug (U803) must be changed to allow for MCS compatibility. Also, to sum the MCS generated PL/DPL audio signal into the transmit audio path of the station, resistor R8110 (33K) must be added. The modifications to the station control board are performed first.

2.2 ROM REPLACEMENT

Step 1. Slide the rf tray out of the cabinet and swing open the control tray to gain access to the station control board.

Step 2. Disconnect the board: unplug P801, P701, and P804. Unsnap the front panel and slide the board forward in the tray until the back edge of the board is clear of the tabs along the back inside wall.

Step 3. Lift the board out, back edge first. P901 from the remote control board may have to be unplugged to allow room to lift the board out.

Step 4. Laying the board on the flat surface, remove the code plug (U803) by sliding the screwdriver between the IC and the socket. Prying gently, the ROM should come out of the socket.

Step 5. Remove the replacement ROM from the envelope marked TRN5194A and place it in the socket. Make sure pin 1 of the IC coincides with the white dot screened onto the PC board and that the IC is firmly seated. From the side, look under the IC and check that all IC pins have entered the socket. A bent or incorrectly inserted pin should be quite visible.

Step 6. If the station was purchased after April 1, 1984 or the part number of the Station Control board program ROM (U804) is 51-90006C24, then U804 does not need to be replaced. Otherwise, repeat steps 4 and 5 for the station control program ROM (U804). The replacement ROM is in the envelope marked TRN5843A.

2.3 RESISTOR INSTALLATION

(Refer to Figures 3 and 4)

Step 1. For P.C. Boards with part number 8482059N04, install jumper JU15. If the board has the part number 8482059N03, first check to see if R8110 is in place. If it is, cut out the zero-ohm resistor (R8175) by U832. If R8110 is not already in place, then it must be installed. Two holes are reserved for this resistor which is to be mounted in a stand up position. Boards with part numbers of 8482059N01 and N02 also require that R8110 be installed, but do not have a position reserved for it, so R8110 must be soldered in existing feedthrough holes with the body of the resistor straddling the top of U835. The station control schematic in the *MSF 5000* Instruction Manual shows R8110 in the circuit.

Step 2. If R8110 is already in place, proceed to Step 3. Clean the solder from the indicated circuit board holes. Using the supplied tubing to keep the resistor leads from shorting to other components, insert R8110 and solder in place. This completes the modification of the station control board.

Step 3. To remount the board in the control tray, lay the board in position, front edge first. Push the board forward in the tray until the back edge of the board clears the tabs along the back wall of the tray and drops into place. Push the board back, under the tabs, until it is firmly seated. Snap on the escutcheon to hold the board in place and reconnect P801, P701, and P804. If P901 was disconnected while removing the board, plug it back into J901 on the remote control board. Close the control tray cover and prepare to install the expansion tray.

2.4 MULTI-CODED SQUELCH BOARD

Step 1. Check the cardboard insulator for proper placement so that the flat ribbon cables of the expansion tray are underneath it. Remove the two middle escutcheons and put the MCS board in place, front edge first. The MCS board must be mounted in the two expansion tray slots immediately next to the expansion power supply. Slide the board forward so its rear edge clears the tabs on the back wall of the tray and drops into place. Push the board back, under the tabs and install the front escutcheons. The board should be firmly locked in place. Plug P1402 into J1402 on the MCS board and installation is complete.

Step 2. Close the expansion tray cover. Slide the rf, control, and expansion tray assembly into the station.

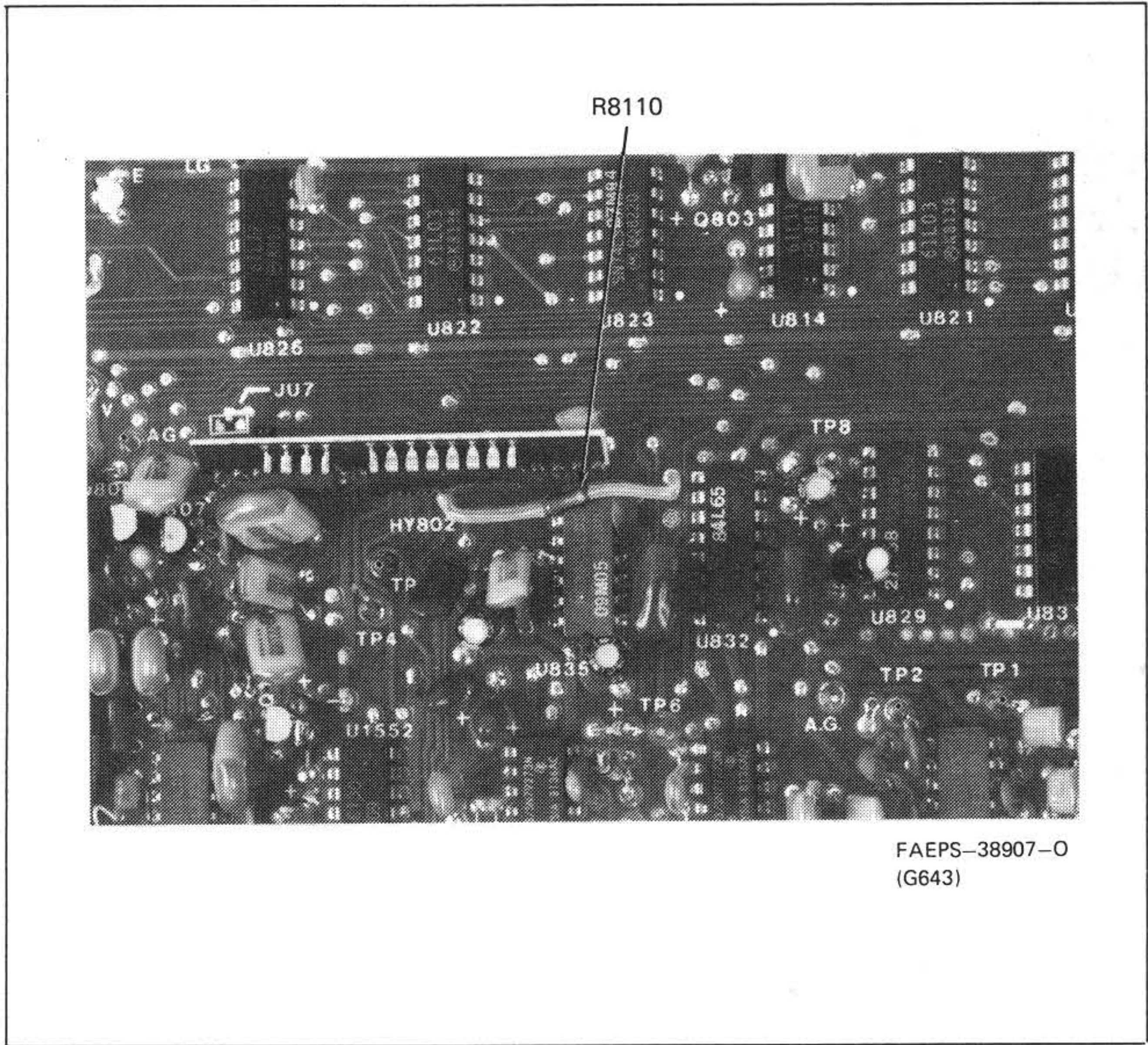


Figure 3. N01 and N02 Station Control Board with Resistor R8110 Installed

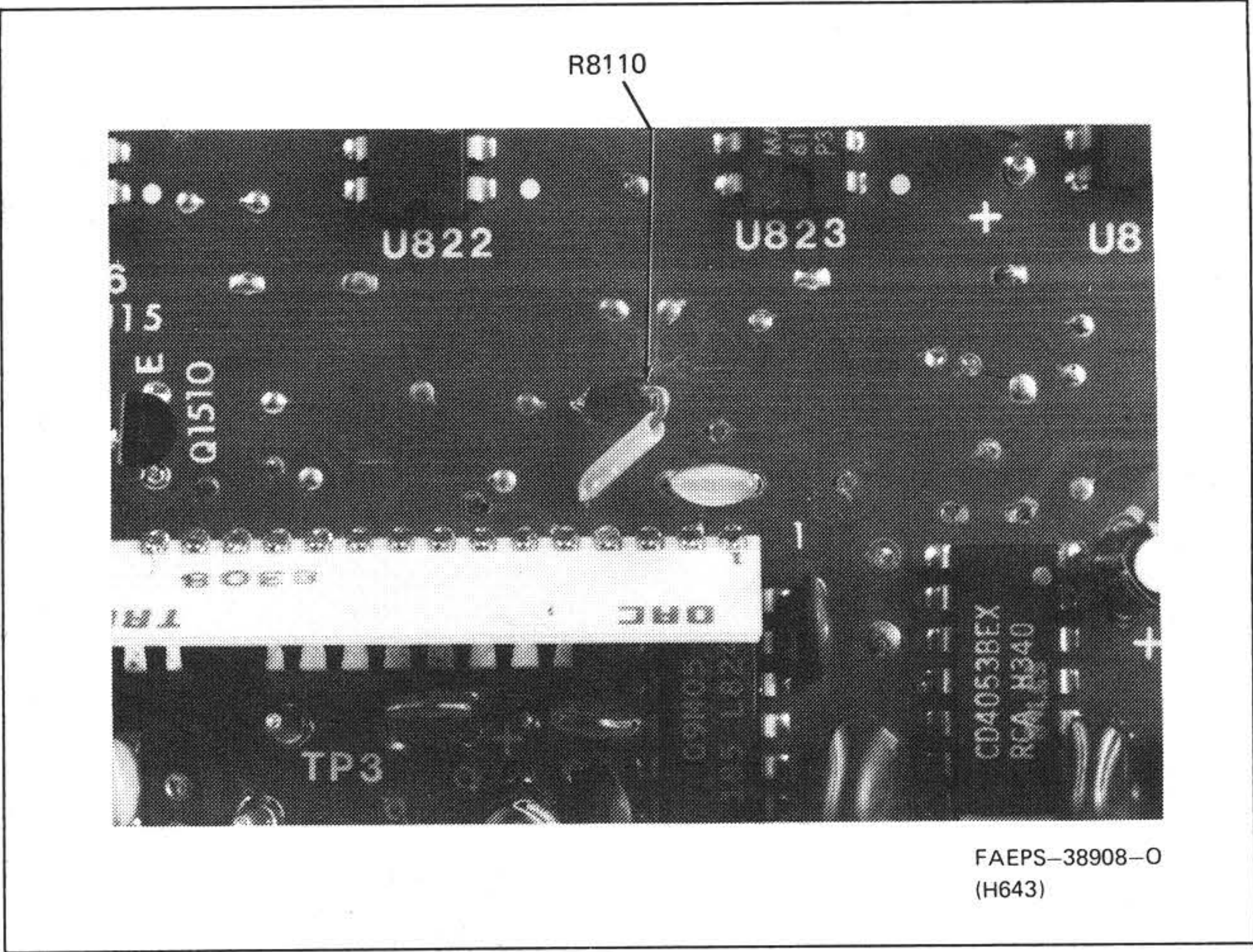


Figure 4. N03 Station Control Board with Resistor R8110 Installed

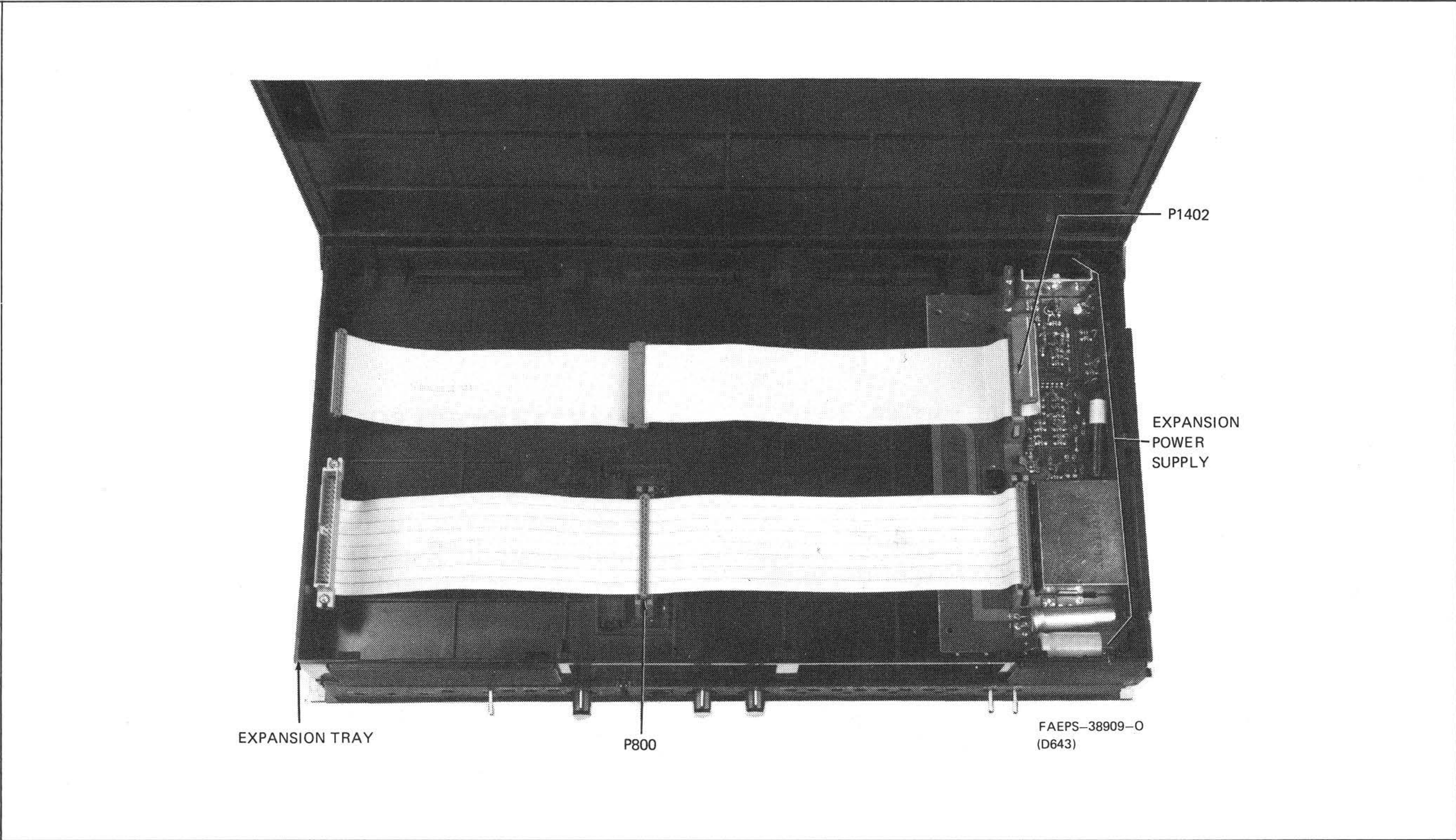


Figure 5. Expansion Tray Before Installation of MCS Board

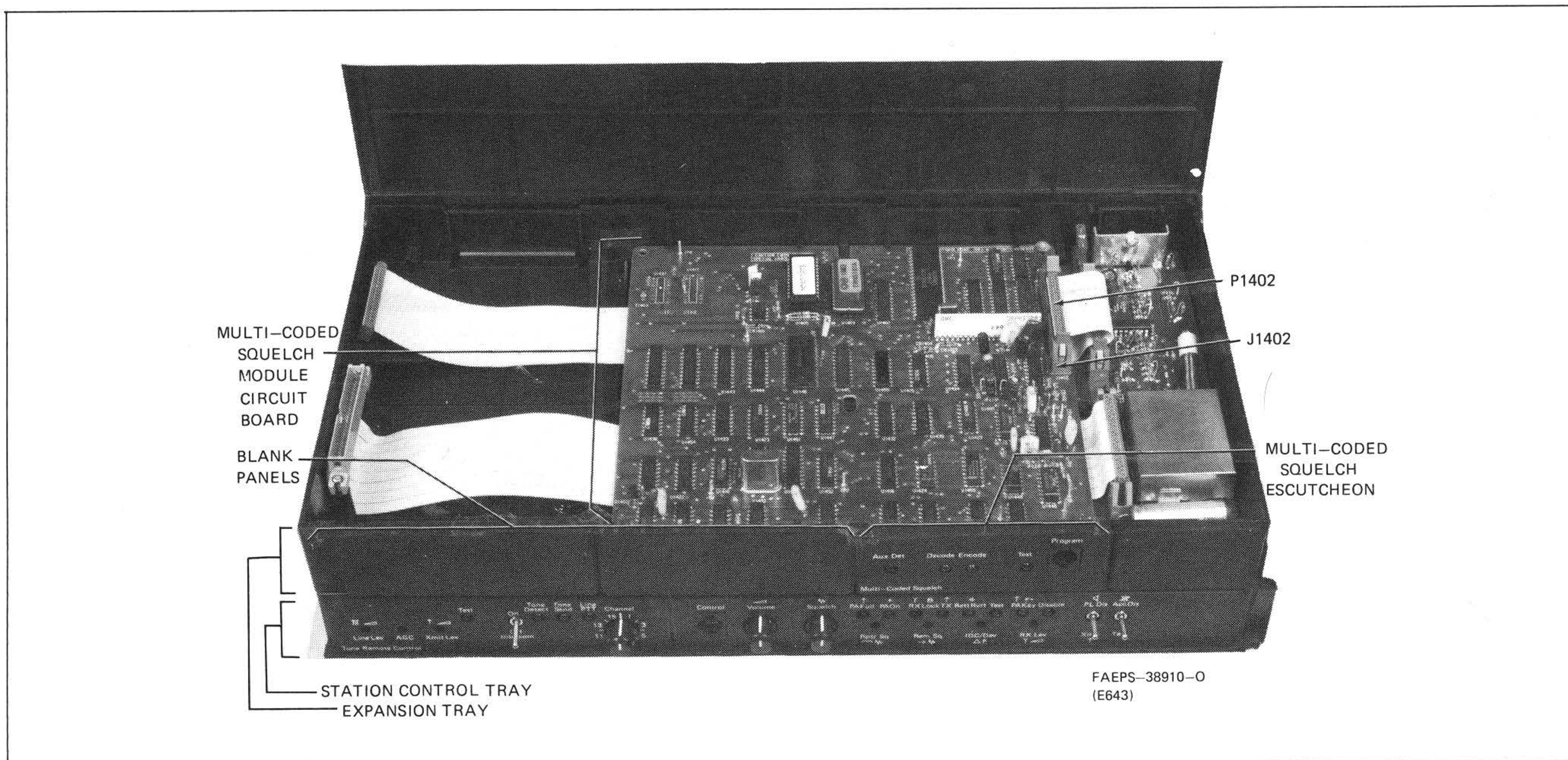


Figure 6. MCS Board Installed in Expansion Tray

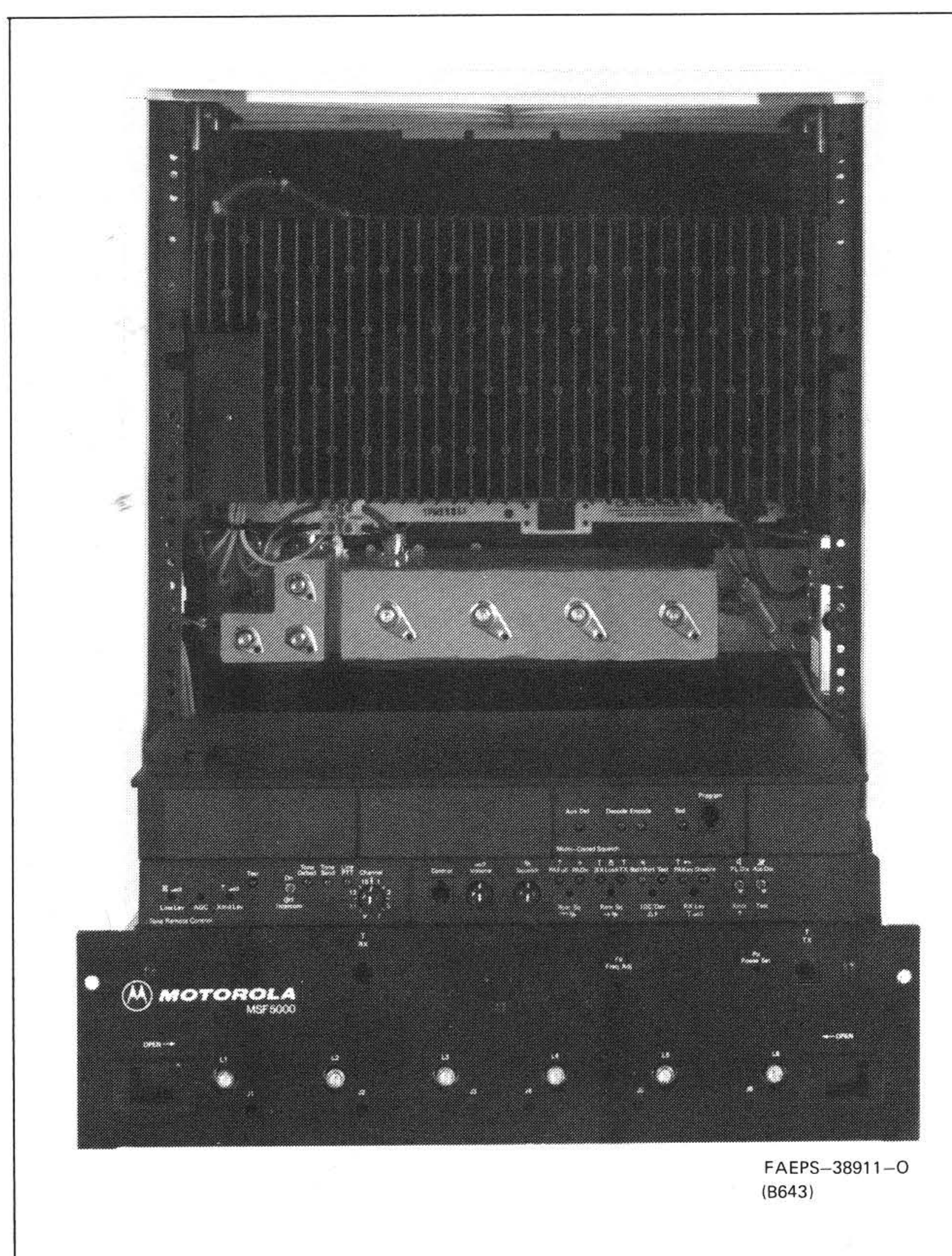
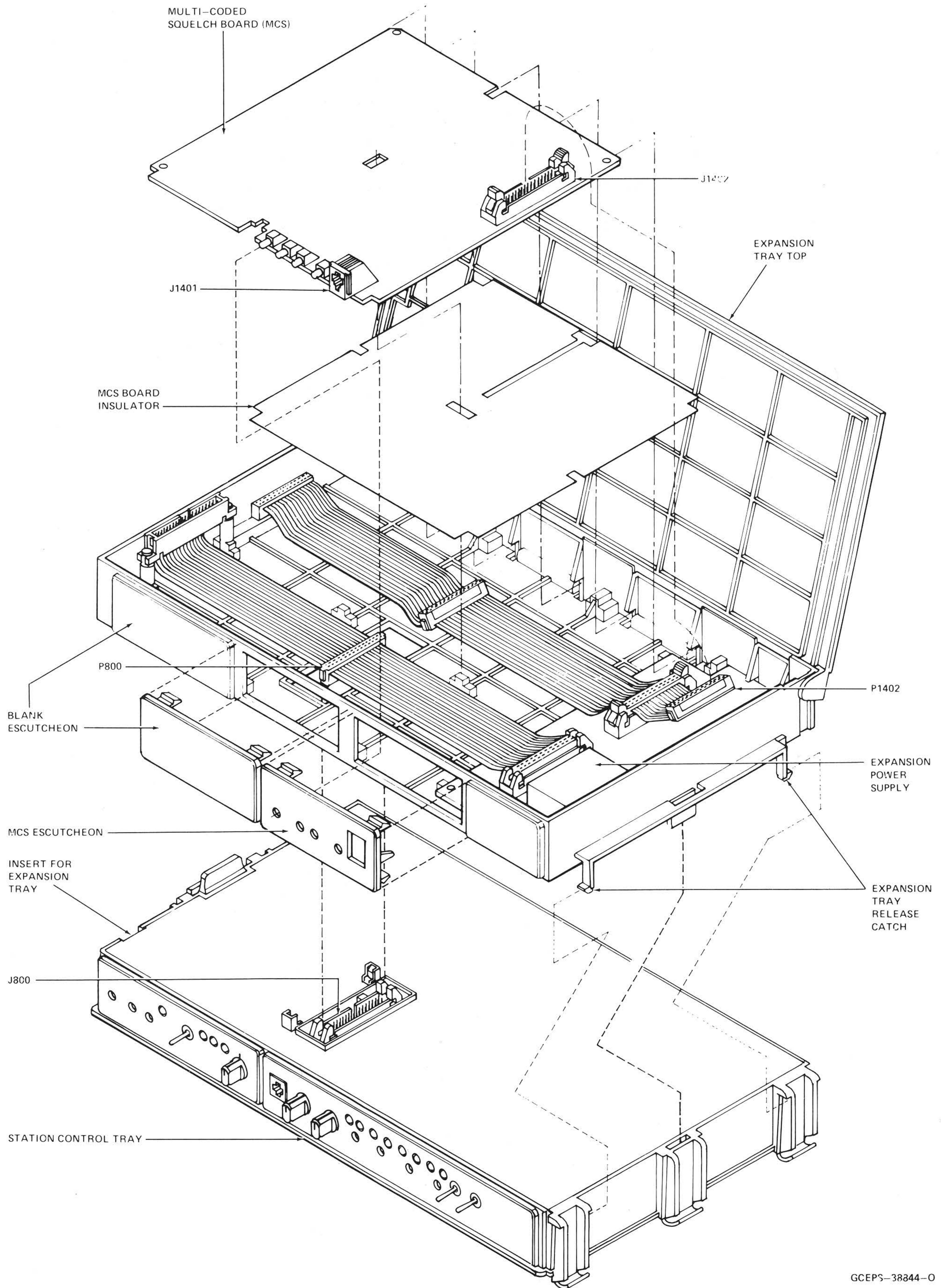


Figure 7. MCS Module Installed



GCEPS-38844-O

Figure 8. Multi-Coded Squelch Module Installation

3. THEORY OF OPERATION

(Refer to the block and schematic diagrams)

3.1 INTRODUCTION

The theory of operation for the Multi-Coded Squelch Module described in the following paragraphs is written for the person experienced in microprocessor and support software and hardware. The description starts with the microprocessor support and interface circuitry on the MCS board. It is followed by the decode filter/limiter and decoder circuitry, and then finally by the encoder circuitry.

3.2 MICROPROCESSOR AND RELATED SUPPORT CIRCUITRY

3.2.1 Microprocessor

A 6803 microprocessor (U1401) is the heart of the control system. It is programmed to operate in the mode which has multiplexed lower order address/data, internal RAM, external interrupt vectors, and no internal ROM. The clock source for the processor is a 4.9068 MHz crystal. The configuration of the processor consists of 4 ports in addition to several control signals.

All of the processor Port 1 signals are utilized except for P15. P10 is used as an output and enables the PL/DPL Loop Diagnostic test. P11 is an output and controls the TEST LED while P12 controls the DECODE LED. P13, External Reset, is used to reset the station. The Watch Dog Timer (WDT) tickle signal, P14, provides pulses to the Watch Dog circuitry to prevent it from resetting the processor during normal operation. P16, DPL Detect, is an input to the processor indicating when a valid DPL code has been detected. P16 can also be configured as an output to allow the processor access to the RAM (U1446). EEPROM Write Setup, P17, is an output from the processor to the EEPROM write protection circuitry.

Port 2 consists of 5 bits, P20 thru P24. The processor mode is determined by the diode configuration on mode programming pins P20, P21, and P22. With the diode in the circuit, the particular port bit is configured as a logic 0 on the rising edge of the processor reset signal (RES). Thus, with diodes in for P22 and P20 and out for P21, the processor is configured in Mode 2. All three of the mode programming pins are also used for other functions. P20 is an input to the processor for the filtered and limited incoming PL signal. P21, Output Compare, is the result from the Output Compare Timer and is used for timing purposes. P22, MIDIRQ, is an output used to generate a processor interrupt for the single PL/DPL code detect algorithm. The remaining two port 2 signals (P23, P24) are the serial communications receive and transmit lines, respectively. The 2 signals are connected to a bidirectional interprocessor communication bus (IPCB) between Multi-Coded Squelch, Station Control, option modules, and/or service equipment.

Port 3 is dedicated to multiplexed lower order address and data signals. Port 4 of the processor is dedicated to upper order addresses.

Six processor signals, AS, R/W, E, NMI, IRQ, and RES are not configured in any of the 4 ports. The Address Strobe (AS) signal is a control signal used to demultiplex port 3 via the Address Latch. The Read/Write (R/W) is an output used to control the direction of data bus transfers. The Enable (E) signal is an output and provides the main clocking for the microprocessor system. The non-maskable interrupt, NMI, is used to interrupt the processor at intervals of approximately 310 microseconds for software timing purposes. The maskable interrupt, IRQ, is used to generate an interrupt when either the MUXbus Read Latch needs servicing or the single PL/DPL code detect needs servicing. The last signal, RES, is activated by failure to tickle the Watch Dog circuitry properly or by an active Expansion Reset signal. During a processor reset the following conditions are present on the other processor pins: Ports 1 and 2 become high impedance. Port 3 becomes high impedance, R/W and AS are actively pulled high, Port 4 is high impedance but the processor provides internal pull-up resistors, and the E signal is active.

3.2.2 Watch Dog Timer

When the processor is operating properly, it outputs "tickle" pulses at U1401-17 with a predetermined repetition rate. The Watch Dog Timer (WDT) circuit monitors the period of the WDT tickle pulse. If it is not within the predetermined range, the WDT circuitry will reset the processor. The WDT circuitry also prevents other circuits from being affected by the malfunction by holding them reset until the processor is again operating correctly.

Multivibrators U1414A and U1415A are used to set the tickle pulse period range by forming a window in which the pulse must occur. In normal operation, U1414A will be kept retriggered by the falling edge of the processor tickle pulse. The U1414A time constant determines the maximum allowable tickle period. If tickle pulses occur too far apart, U1414A will time out and a processor reset will result. The minimum tickle pulse period is determined by U1415A and U1430A. In normal operation, U1415A is also triggered by the falling edge of the tickle pulses and is allowed to time out. If tickle pulses occur too close together, however, the output of U1415A is still active when the second tickle pulse occurs. The output of U1430A then goes low and a processor reset will result.

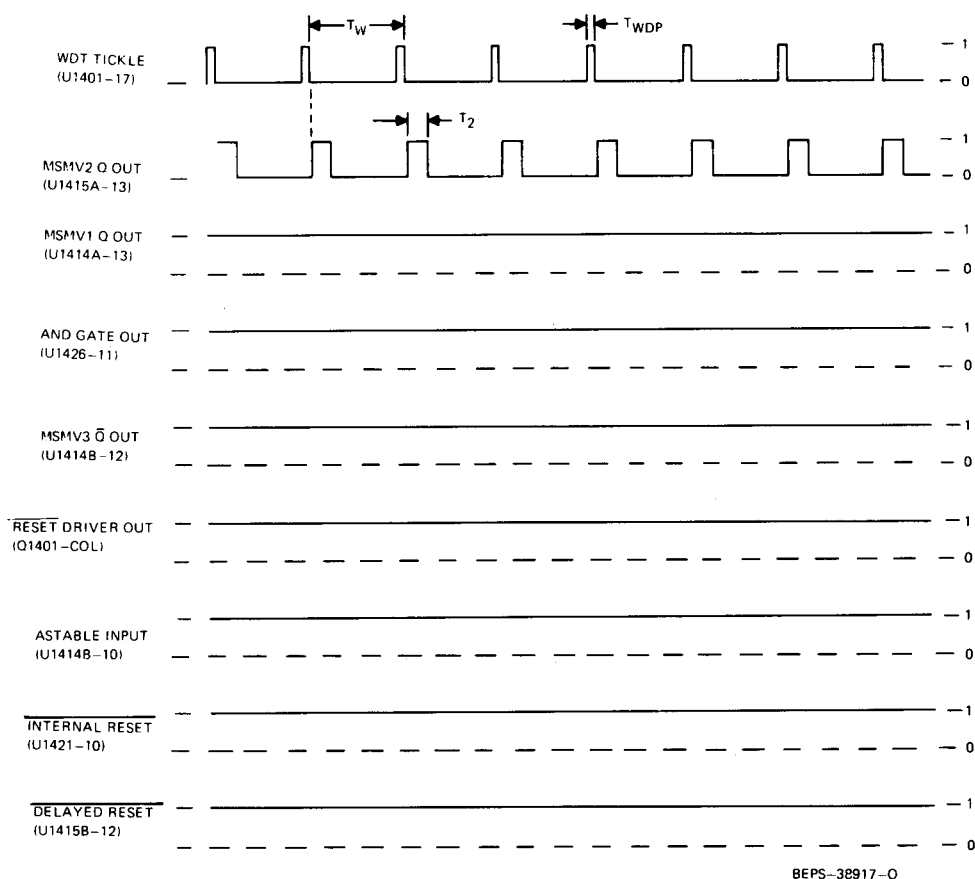
The processor reset occurs as follows. U1414B generates a reset pulse whose duration is determined by the U1414B time constant. This occurs when the U1414-9 input goes active as a result of improper tickling. As part of the resetting procedure, the U1414-10 input will be taken inactive to give the processor time to go through its start-up routines and to start outputting

proper tickle pulses. The first tickle should occur about 4 milliseconds after the reset trailing edge. If no tickle occurs, U1414-9 remains active and another reset pulse will be generated by U1414-10 input going active. This astabling operation will continuously attempt to reset the processor when improper tickling occurs. If after being reset the processor generates a tickle pulse, the U1414-9 input goes inactive preventing any additional reset pulses from occurring due to the astabling function.

The Internal Reset signal is incorporated into the WDT circuitry in the following manner. As long as Internal Reset is held active, U1414B will astable as described earlier and the processor will be held in reset. In this case the astabling operation is not needed to reset the

processor, but instead is used to retrigger the Delayed Reset circuitry (U1415B). Internal Reset is also used to clear U1415A so that when the WDT tickle signal is pulled high as a result of a reset, another reset does not occur due to a low output on U1430A.

The Delayed Reset signal will hold other parts of the circuitry (i.e. NMI and IOW) inactive until the processor is properly tickling the WDT circuitry and astabling operation has ceased. The time constant is such that Delayed Reset is active long enough to guarantee that two proper tickle pulses occur after the final reset. (Delayed Reset is not allowed to go inactive after one tickle because a single tickle could be the result of a processor malfunction.)



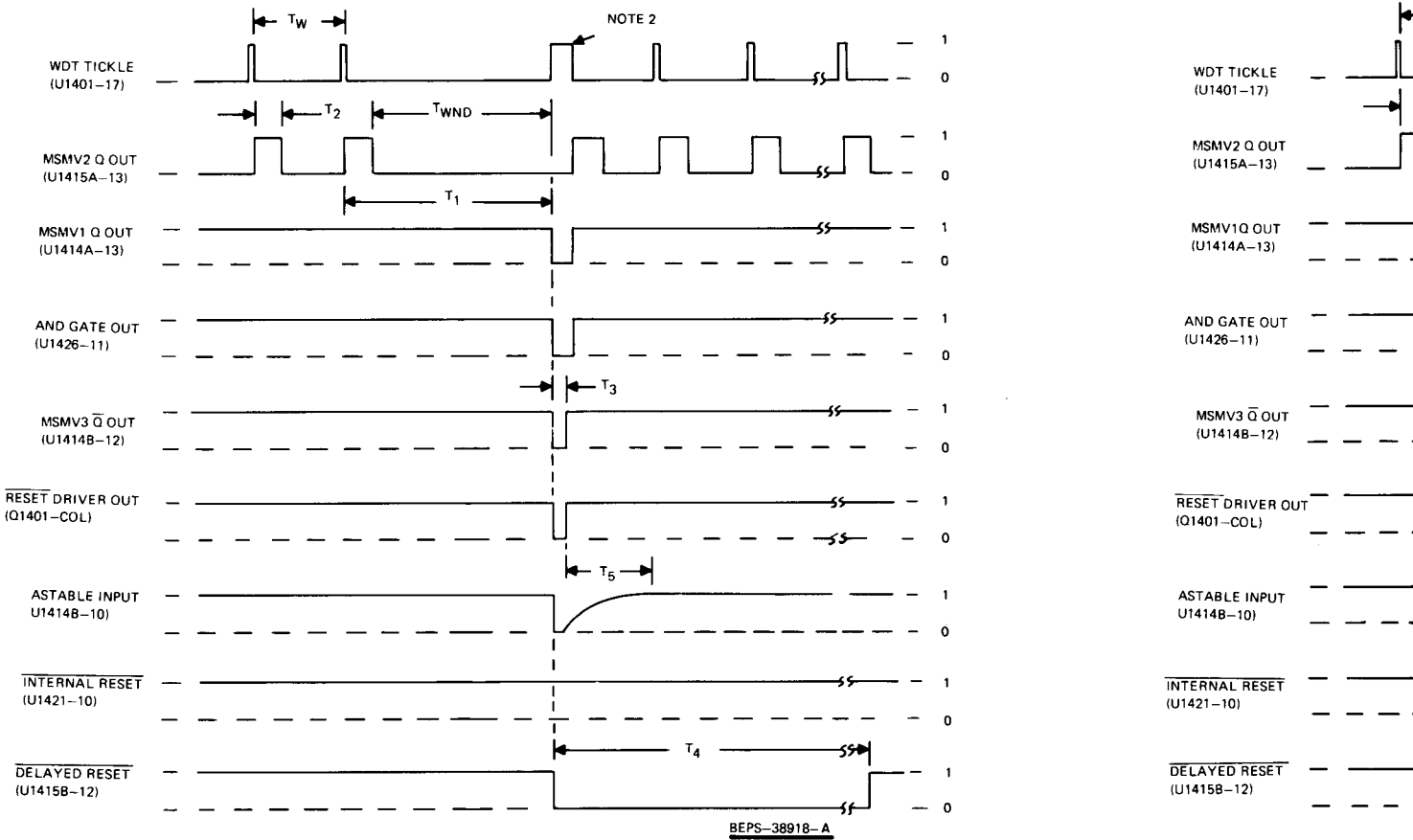
NOTES:

1. All timing is approximate, due to component variation.

Figure 9.
Normal Operation Timing Diagram

Table 1. Timing Parameter Chart

Parameter	Description	Timing Range	Average
t_w	Watchdog Timer Tickle Period	35-71	53
t_{WDP}	Watchdog Timer Tickle Pulse Width	40-300	170
t_1	MSMV U1414A Time Constant	89-214	151
t_2	MSMV U1415A Time Constant	9-21	15
t_{WND}	Window Width (t_1-t_2)	68-205	136
t_3	MSMV U1414B Time Constant	2.5-4.5	3.5
t_4	MSMV U1415B Time Constant	490-1389	935
t_5	Astable Time Constant (C1408, R1470)	14-230	122



NOTES:

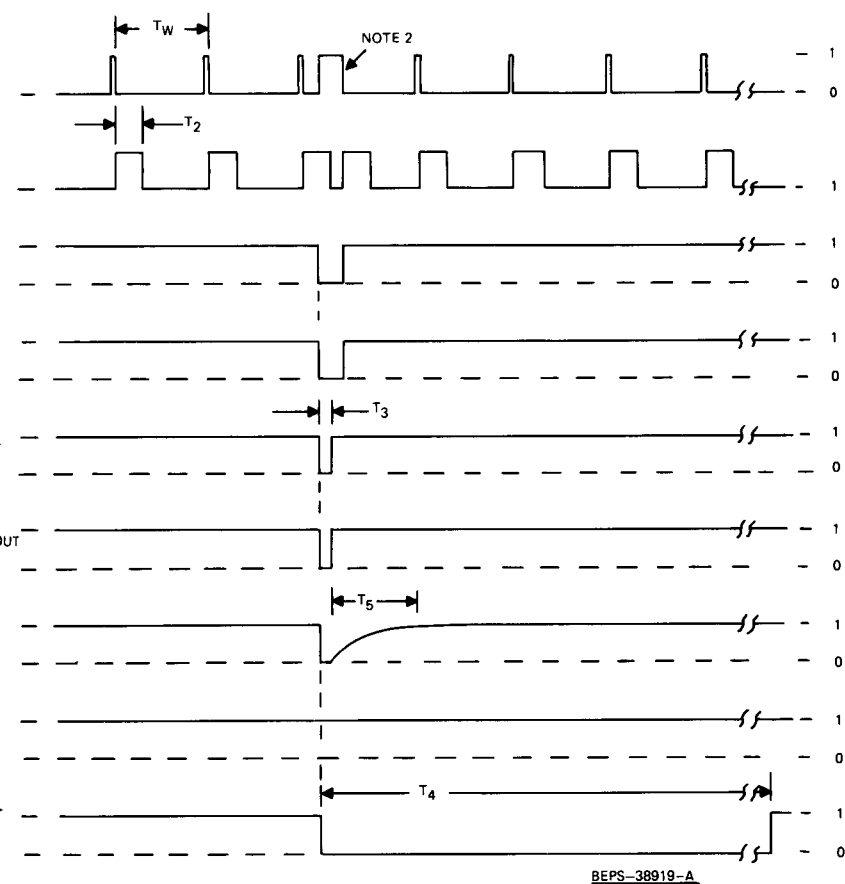
1. All timing is approximate, due to component variation.
2. The Watchdog Timer (WDT) tickle signal is pulled low approximately 4 ms after the RESET signal to the processor goes inactive (high).

NOTES:

1. All timing is approximate, due to component variation.
2. The Watchdog Timer (WDT) tickle signal is pulled low approximately 4 ms after the RESET signal to the processor goes inactive (high).

Figure 10.
Abnormal Operation Timing Diagram
(Tickle Pulse Late or Missing)

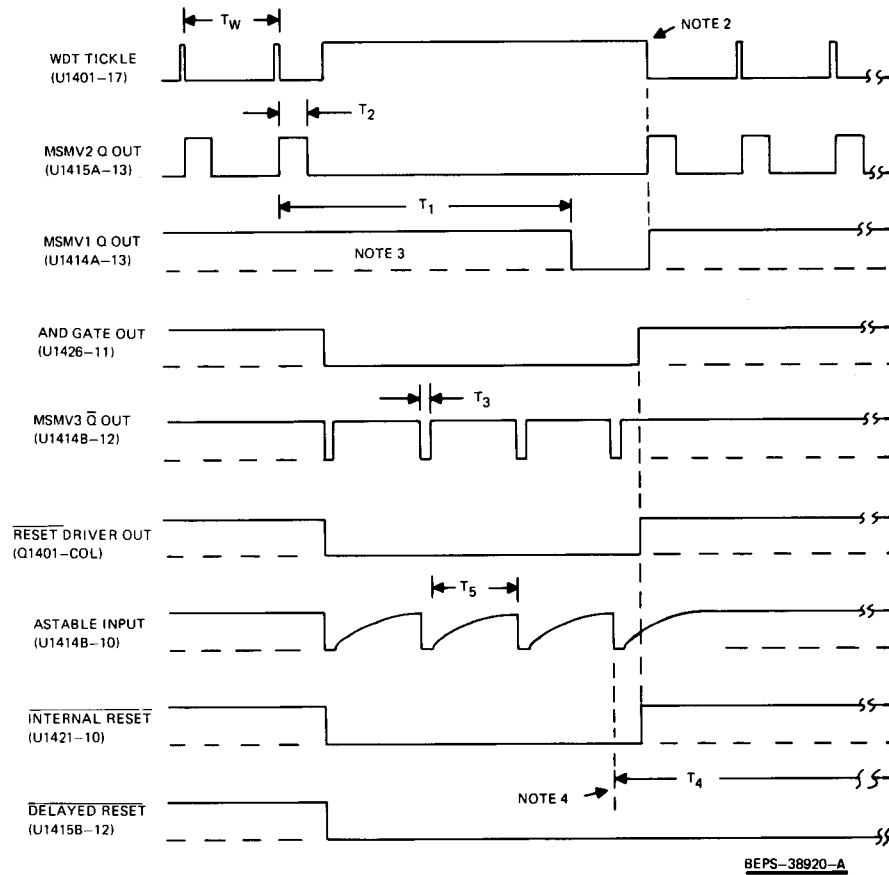
Average	Units
53	ms
170	uS
151	ms
15	ms
136	ms
3.5	ms
935	ms
122	ms



NOTES:

1. All timing is approximate, due to component variation.
2. The Watchdog Timer (WDT) tickle signal is pulled low approximately 4 ms after the RESET signal to the processor goes inactive (high).

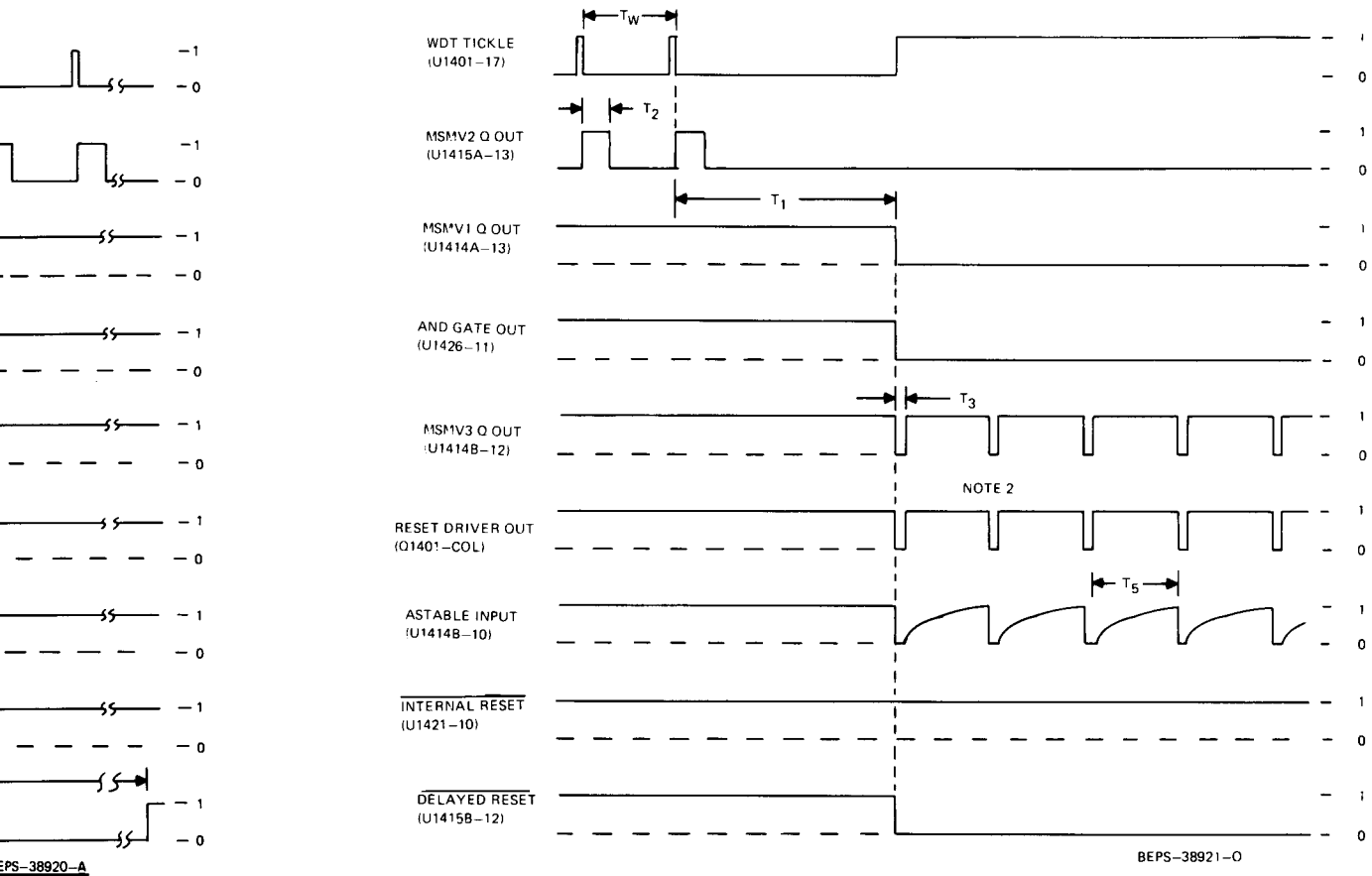
Figure 11.
Abnormal Operation Timing Diagram
(Tickle Pulse Early)



NOTES:

1. All timing is approximate, due to component variations.
2. The Watchdog Timer (WDT) tickle pulse is pulled low approximately 4 ms after the RESET signal to the processor goes inactive (high).
3. The MSMV1 Q Output will not change state (High to Low) if the INTERNAL RESET signal is held active (low) for less than the remaining T_1 time.
4. Since MSMV4 (U1415B) is kept retriggered, the DELAYED RESET time T_4 begins with the falling edge of the last output from U1414B-12.

Figure 12.
Timing Diagram Showing Effects of
Internal Reset Signal



NOTES:

1. All timing is approximate, due to component variation.
2. The astable operation of MSMV3 (U1414B) generates pulses in an attempt to reset the processor.

Figure 13.
Timing Diagram Showing Effects of MPU Malfunction

3.2.3 Address Latch

The Address Latch (U1402) is used to latch the lower order addresses from the multiplexed address/data lines of the processor Port 3. The part is transparent while (AS) is high and latches the addresses on the falling edge of AS. The latched address lines are output to the address/control bus.

3.2.4 Memory Map Decoder

Two control signals, I/O Read ($\overline{\text{IOR}}$) at U1434-6 and I/O Write ($\overline{\text{IOW}}$) at U1423-6, are generated for use in selecting I/O devices. $\overline{\text{IOR}}$ provides an enable for the group of I/O devices from which the processor reads, while the $\overline{\text{IOW}}$ provides an enable for those to which the processor writes. For both groups, the control signal only provides one enable to the device while an address line is needed to provide the other. Security is provided to the system by gating Delayed Reset and R/W in to the formation of $\overline{\text{IOW}}$. If the Watch Dog circuitry detects a processor failure, Delayed Reset will prevent a write to the I/O devices. If the processor fails in such a manner that the Watch Dog circuitry is still tickled properly, R/W adds an extra level of security.

3.2.5 Memory Devices

The main executable code for the processor system is stored in the Program EPROM (U1403). It is an $8k \times 8$ device with an access time of 250 nanoseconds (ns). Both the layout and memory map are also suitable for use with $8k \times 8$, $16k \times 8$, and $32k \times 8$ ROM and EPROM devices with access times less than 390ns. For the $8k \times 8$ and $16k \times 8$ EPROM devices, note that although A14 is not used for the chip enable to the device, it is required to be high for proper operation since it connects to the Program (PGM) pin on these devices.

Another memory device for the processor system is the Code Plug (U1405) which stores the user configuration (personality) data. It is a $2k \times 8$ EEPROM device with a 350 nanoseconds access time. Both the layout and memory map are suitable for use with $4k \times 8$ EPROM or $2k \times 8$ RAM devices with access times less than 390 nanoseconds.

The last memory device for the processor system is the Multi-DPL RAM (U1446). It is a $2k \times 8$ static RAM with a 150ns access time. It serves two distinct functions. First, it contains a reflection of the valid DPL codes present in the code plug. Secondly, it is used as a scratch pad RAM when it is not required for multi-DPL detection.

3.2.6 Output Compare Flag/NMI

The Output Compare Flag/NMI (OCF) circuit is used to interrupt the processor via $\overline{\text{NMI}}$ at a predetermined frequency. A processor interrupt each 310 microseconds is required to meet software timing restrictions.

When the OCF from the processor (P21) toggles, a logic 1 is clocked into either U1411A or U1411B, activating the NMI signal. (Refer to the MC6801 Reference Manual for further information on P21.) The processor then clears the OCF flip flops by means of U1413B and U1426B. The circuit is now ready for the next transition of P21. Delayed Reset is gated into U1426B to initially clear the OCF circuitry and to disable the NMI interrupt during power-up tests.

3.2.7 Options Buffer

Only 3 inputs of the Options Buffer (U1408) are used for distinct functions. The DPL Decode Data (U1408-2) signal is the lowpass filtered and limited DPL data to be decoded by the processor after a multiple detect. The DPL Rotate bit (U1408-9) signals the processor to rotate the DPL code. The $\overline{\text{MUXIRQ}}$ (U1408-8) bit informs the processor that the MUXbus Read Latch (U1406) is updated and needs to be serviced. The other five bits are reserved for future expansion.

3.3 INTERFACE CIRCUITRY

3.3.1 MUXbus Circuitry

All MUXbus lines are referenced to logic ground. The 4 address (J1402-5 thru 8) and 4 data lines (J1402-9 thru 12) form a multidirectional digital communications path. The bus is time multiplexed to conserve interconnections (64 connections reduced to 9) and to increase future expansion capability. The data strobe (DS) and the 4 address lines are driven by the Station Control Module. The data lines are inverted and open collector driven. This allows multiple hardware modules to drive the bit in a nondestructive, wired OR fashion.

The MUXbus Data Latch (U1409) latches information from the processor which is to be written to the MUXbus data lines. The processor updates the latch every 310 microseconds in order to meet the MUXbus timing restrictions. The $\overline{\text{DS}}$ input signal is used to generate an $\overline{\text{IRQI}}$ interrupt which results in the properly timed update of the MUXbus Data Latch.

Four inputs to the MUXbus Read Data Latch (U1406) are used to read the 4 MUXbus address bits while the remaining 4 are used to read the multiplexed data bits which are present at the expansion connector. (The data at the connector is inverted from that which is written to the MUXbus Data Latch.) At the rising edge of $\overline{\text{DS}}$, the MUXbus address and data bits are latched into the MUXbus Read Data Latch and an $\overline{\text{IRQI}}$ interrupt occurs. This interrupt is sent to the processor indicating that the latch has been updated.

3.3.2 Reset Driver Circuitry

The Reset Driver circuitry is designed to allow two separate functions. First, the processor is able to activate Expansion Reset via the External Reset signal. When

External Reset goes low, Q1403 charges up C1427. The time constant of R1477 and C1427 maintains an active Expansion Reset signal for at least 6 μ S after External Reset goes inactive. A minimum Expansion Reset pulse width of 6 microseconds is necessary to ensure that all other modules will see the reset. The second function allows the MCS module to be reset by an Expansion Reset signal generated external to the MCS module. The MCS module will be reset regardless of the origin of the Expansion Reset signal.

3.4 PL/DPL DECODE LOW-PASS FILTERS/LIMITERS

The PL/DPL Decode Low-Pass Filter/Limiters U1428, U1440, U1427, and U1441 essentially eliminate non-PL/DPL signals from the incoming Quad Audio (J1402-31) line. The resulting potential PL or DPL signal is then checked against valid codes. This process includes limiting the signal to form a square wave as well as limiting the peak amplitude to an acceptable TTL level. The PL/DPL input signal (Quad Audio) must be between 192 mV (p-p) and 384 mV (p-p) with a 4.8 V \pm \pm 0.45 Vdc offset.

The PL filter is a 5 pole low-pass filter with an upper 3 dB frequency of approximately 250 Hz. The maximum ripple is specified at 2 dB. The PL limiter transforms the sinusoidal PL signal into a square wave of the same frequency with a peak amplitude of 5 volts. Hysteresis is included in the limiter to improve noise rejection. The TTL output then goes to P20 of the processor. Delayed Reset is gated into the limiter to essentially disconnect the PL signal from the processor during reset, enabling P20 to be used as mode programming bit 0. When Delayed Reset goes low, Q1405 is held in cutoff regardless of the state of the PL signal.

The DPL filter is a 5 pole low-pass filter with an upper cutoff frequency of 150 Hz. (The first three poles share common circuitry with the PL filter.) The maximum ripple is also 2 dB. The limiter sends a clean digital signal to the Multi-DPL Sample Code Shift Register and to the Options Buffer.

3.5 DECODE CIRCUITRY

3.5.1 General

The Multi-DPL Decode circuitry is used for detection of valid DPL codes. The basic function of DPL detection consists of 2 operations. First, the incoming DPL code must be identified as one of a given number of valid DPL codes. This is called multiple DPL detection and is the function performed by the Multi-DPL Decoder circuitry. After this occurs, a software algorithm is used to verify that the identified code is properly detecting. This is called single-DPL detection. This algorithm is also used to detect dropout and turn-off of the code.

PL detection occurs in a manner similar to DPL detection, except that it does not occur in the hardware. Rather, software algorithms are used for both multiple PL detection and single PL detection. Dropout is also identified by the PL single detect software algorithm. Because PL detection is accomplished solely through software algorithms, this text section will describe the DPL decode hardware.

The basic operation of the Multi-DPL Decoder circuitry consists of a comparison between reference DPL codes and an incoming filtered and limited DPL signal. The reference codes are stored in RAM and are downloaded, one at a time, for comparison to the incoming code. When the 2 codes correlate properly, the circuitry is halted and the detected code is identified. A single detect then occurs and is monitored until a turn-off or coast-off occurs. The Multi-DPL Decoder circuitry is then restarted and continues operating (comparing codes) until a new multiple detect occurs.

3.5.2 Sample Code Shift Register

The Sample Code Shift Register (U1448, U1449, and U1450) is a 96 bit shift register used to store the current incoming DPL signal. The register input is the filtered and limited Quad Audio signal. The sample shift register is divided into 2 smaller 48 bit registers so that 2 sample bits can be compared to 2 reference bits simultaneously. Thus, U1449A contains the first 48 bits of the sample code and U1449B contains the last 48 bits. Each of these 48 bit registers is recirculated during the comparison process.

3.5.3 Reference Code Generator

The Reference Code Generator (U1444, U1445, U1455, and U1446) performs two main functions. One of these functions deals with Multi-DPL detection. The RAM (U1446) has been previously loaded with the valid DPL codes and is configured in the read only mode. The RAM is then addressed by the Address Generator circuitry (U1456 and U1457) such that the appropriate data is output to the Reference Code Shift Registers (U1447 and U1451) at the proper time.

The second function performed by the RAM circuitry requires that the DPL Detect line be brought active by processor port P16 in order to halt the detection of DPL codes. When DPL Detect is active the processor can read from and write to the RAM. This function is needed initially to download the valid DPL codes into the RAM from the Code Plug. Exactly 144 bytes of the RAM are dedicated to Multi-DPL detection. This section of memory is used to store two representations (dual phases) of each enabled DPL code. The use of dual phase codes instead of single phase codes (one representation) greatly improves the DPL code detect time.

The RAM is also needed to function in this non-multiple detect mode after a code has detected. At this time the

RAM is used in conjunction with the single detect algorithm.

3.5.4 Reference Code Shift Register

Each of the two Reference Code Shift Registers (U1447 and U1451) is simultaneously loaded with 4 bits of valid DPL code. These bits are shifted out as they are compared to the data in the Sample Code Shift register (U1449A and U1449B). This must be repeated 3 times in order to download the entire DPL code into the Reference Code Shift Register. Reference Code Shift Register A (U1451) is loaded with the first 12 DPL bits in order to be compared with Sample Shift Register A (U1449A). Reference Code Shift Register B (U1447) is loaded with the last 12 DPL code bits in order to be compared to Sample Code Shift Register B (U1449B).

3.5.5 Address Generator

The Address Generator circuitry (U1456 and U1457) is used to generate the RAM addresses which contain the reference codes. The two 4-bit counters, U1456 and U1457, are set up as synchronous down counters. When a detect occurs the counters are stopped and the DPL Data Buffer (U1443) is used to read the counter output. This 8-bit address is used to identify the detected code by means of a software look-up table.

3.5.6 Clock Circuitry

The purpose of the clock circuitry (Y1402, U1412, U1422, U1410, U1420, U1436, and U1454) is to generate the clock signals necessary to properly coordinate the operation of the other sections of the Multi-DPL Decoder circuitry. The crystal oscillator circuit containing Y1402 serves as the origin of the clock circuitry and operates at 2.4785 MHz.

The main clock signals generated by this circuitry are as follows:

Clk A is used to clock the result of the sample and reference bit comparison to the counter (U1452). This clock continues to operate after a detect occurs.

Clk B is used to preset the flip-flop (U1416A) after each comparison. This flip-flop is used to increment the threshold counter by 2. This clock continues to operate after a detect occurs.

Clk C results in the shifting of the Sample Shift Register and continues to operate after a detect occurs.

Clk D shifts the Reference Shift Register contents.

Clk F is used to reset the threshold counter after all 24 bits (3 bytes) of each reference code have been compared. The divide-by-3 circuitry needed to perform this function is provided by U1420, U1436C, and U1436D.

Clk G is normally in a logic high state to keep the sample registers in the recirculated mode. Clk G is taken to a logic low state in order to shift a new sample bit into the register. Clk G is also held low after a detect occurs. This is needed in order to fill the register with samples of the most recent input signal. This prevents the circuit from redetecting on the same (old) code immediately after it is restarted.

3.5.7 Correlation Circuitry

The purpose of the Correlation Circuitry (U1453, U1452, U1416A, and U1424) is to count the number of correct comparisons between the reference code and the incoming code, and to activate the $\overline{\text{DPL Detect}}$ line if this number is above the predetermined threshold level.

The sampled code is compared, two bits at a time, to the reference code. The outputs of U1424A and U1424B will be a logic 1 level if the sample bits match the reference bits. The U1452 counter is clocked once if the output of either U1424A or U1424B is high, and twice if both outputs are high. The outputs of these gates are clocked to the counter by Clk A. The counter output is fed into the U1453 comparator where it is checked against the threshold level. If the threshold level is exceeded, $\overline{\text{DPL Detect}}$ goes active signaling that the incoming code is a valid DPL code. If the threshold level is not exceeded after all bits in the code are compared, the counter is reset. At this point, a new reference code will be compared to the same sample code. This sequence repeats until a detect occurs.

3.6 ENCODE CIRCUITRY

3.6.1 General

The encode circuitry generates and provides the PL/DPL signals for the transmitter carrier frequency. The related circuits are as follows:

- DAC Latch
- PL/DPL Encoder

3.6.2 DAC Latch

The DAC Latch (U1404) latches the 5 bits necessary to encode PL or DPL. These outputs are routed to the DAC circuitry in the audio section where they are used to generate the proper code for the transmit audio signal. The DPL rotate bit (U1404-16) is routed to the Options Buffer (U1408-9). It is used to signal the processor to rotate the DPL encode word by one bit. This rotation occurs every 7440 microseconds in order to feed a new encode bit to the DAC circuitry. The encode bit (U1404-15) is used to drive the ENCODE LED. This line is only active when the processor is encoding a PL or DPL code. The remaining latch output bit (U1404-19) is unused.

3.6.3 PL/DPL Encoder

The PL/DPL Encoder regenerates a PL or DPL code to be sent to the transmitter. The primary component in the encoder is a digital-to-analog converter/lowpass filter hybrid, HY1401. The amplitude of the analog signal to be generated is determined by 5 bits B0 thru B4, from the DAC Latch (U1404). The output of HY1401-17, is the PL or DPL signal riding on a dc offset of 4.8 volts. This signal is then routed to the TX DATA AUDIO line, J1402-26.

4. MAINTENANCE AND TROUBLESHOOTING

4.1 GENERAL

In order to operate a Multi-Coded Squelch board, it should be connected to a working Station Control board via an Expansion Power Supply board. For DC power connections to the Station Control board when operating outside a station, refer to the Station Control Module section.

4.2 MULTI-CODED SQUELCH BOARD TESTS

4.2.1 Self-Diagnostics

The Multi-Coded Squelch board features self-diagnostic routines that make it possible to troubleshoot the digital circuits with standard bench test equipment (e.g., oscilloscope) in most cases. The board is equipped with a self-diagnostic routine that it performs when the station is first powered up, or whenever S801 (on the Station Control front panel) is put into the TEST position. The routine checks the integrity of MPU U1401, program EPROM U1403, Code Plug U1405, the MUXbus read/write circuits, the serial port (IPCB) read/write circuits, and the Reference Code Generator circuits. If any of these basic blocks fail the self test, the MPU flashes the TEST LED repeatedly, a specified number of times (one, two, three, four or five times), to indicate the failure that was discovered. Except in cases of a Code Plug failure, it then waits about 1.5 seconds and resets the board by failing to tickle the watchdog circuits. Refer to the Watchdog Timer paragraphs in this section of the manual. When the watchdog circuit resets the board, the TEST LED flashes once, with a flash that is shorter than the failure indication flashes. After the watchdog circuit resets the board, the diagnostic routine is repeated. If the board fault remains unchanged, the routine locates it again, flashes the TEST LED, and resets the board again. The sequence of flashes follows the reset by about 4 seconds. The result is that the board sends a sequence of flashes, a short flash, another sequence of flashes, a short flash, etc. If a Code Plug failure occurs, the MPU flashes the TEST LED twice, and then again checks the integrity of the Code Plug. If it fails again, the LED is flashed twice again, resulting in approximately 10 seconds between sequences of flashes.

Note that the entire diagnostic routine is not repeated for this type of failure.

Note that the TEST LED on the Multi-Coded Squelch board is different from that on the Station Control board. If the Station Control TEST LED indicates a problem on that board, then the Multi-Coded Squelch TEST LED will probably also be lit since if the MUXbus (which is run by Station Control) is not operating, Multi-Coded Squelch will not pass the MUXbus power-up diagnostic routine. Generally, if both TEST LEDS are on, the problem probably lies on the Station Control board. This may be verified by disconnecting the ribbon cable to the Multi-Coded Squelch connector J1402 to determine if the TEST LED on Station Control goes out without Multi-Coded Squelch connected. The Station Control Board should be capable of running with or without the Multi-Coded Squelch board connected. If the TEST LED on the Station Control board is still on after Multi-Coded Squelch is disconnected, the problem lies on either the Station Control or Expansion Power Supply board.

A recurring sequence of flashes on the Multi-Coded Squelch board indicates that the self-diagnostic routine is running and is detecting a fault in the Multi-Coded Squelch circuits. The meaning of the different sets of flashes is as follows:

- One Flash — This indicates that either MPU U1401 or Program EPROM U1403 is defective and should be replaced.
- Two Flashes — This indicates that Code Plug U1405 is either defective or not properly programmed. First, try reprogramming the Code Plug, checking to be sure that JU1 is in place. The Code Plug can be reprogrammed via the Program Plug while the DECODE LED is on. If after reprogramming the fault still exists, U1405 should be replaced.
- Three Flashes — This indicates that the Multi-Coded Squelch board has detected a failure during the MUXbus test. The board first tests to see if the MUXbus address lines are cycling properly. A failure results if either the addresses are not cycling (a Station Control failure) or the Multi-Coded Squelch board cannot read the lines properly. The board then tests whether it can read and write onto the 4 MUXbus data lines. If this test is failed, check to see that the Station Control board is toggling the MUXbus address lines, BA0-BA3. Next, check to see that the \overline{DS} signal from Station Control is reaching U1416B-11 and that a rising edge at this point (U1416B-11) causes a low signal at U1416B-8 and U1401-5. Next, check that U1409-15 is low. If not, look for a malfunction in the Delayed Reset circuitry. Also, check that the outputs of U1406 and U1409 are toggling.
- Four Flashes — This indicates that interprocessor communication bus (IPCB) J1402-3 or J1401-1 is not

operating properly. The self-diagnostic routine determines this by writing a string of high and low levels to the IPCB and reading the string back. If the read and write circuits fail or if the IPCB line on J1402-3 is shorted, the self-diagnostic routine indicates a failure.

The self-diagnostic routine has another added feature to aid in troubleshooting the IPCB circuits when a fault is indicated. If Test Pin 1 (TP1) is shorted to ground with a jumper, the Watchdog Timer is disabled, preventing a Watchdog reset to the MPU. When this is done, the self-diagnostic routine writes a series of alternating high and low levels to the IPCB line via IPCB Out pin of the MPU, U1401-12. The line continues to switch from high to low indefinitely until the MPU is again reset. With this continuous signal coming from the MPU, the IPCB read and write circuits can be checked with an oscilloscope.

- **Five Flashes** — This indicates that the Reference Code Generator circuitry is not operating properly. The self-diagnostic routine determines this by writing data to the RAM (U1446) and reading it back. If the associated circuitry (U1455, U1445, U1446, U1444, U1432C, U1435B) fails, the diagnostic routine indicates a failure by generating 5 flashes of the TEST LED.

4.2.2 Watchdog Reset Failure

The Multi-Coded Squelch board may fail in such a way that the program routines cannot be run, including the power-up self diagnostic routine described previously. This indicates a major digital circuit failure. The watchdog circuit aids in determining these failures, yet keeps the station in a benign state until the program routines are again running correctly. When this type of failure occurs, the TEST LED is on steadily, or else flashing at a rapid rate (many times per second). When this major digital circuit failure indication is seen, the following procedure should aid in finding the failed circuit.

Step 1. Use an oscilloscope in the dc coupled mode of operation, to look at the signal at the reset ($\overline{\text{RES}}$) pin of the MPU, U1401-6. The normal signal at this pin is always high. A series of low pulses, of 2 milliseconds duration, approximately, occurring every 10 milliseconds to 250 milliseconds, indicates a type of reset caused by the MPU watchdog circuit when it finds a fault in the series of MPU tickle pulses. If this type of signal is present at U1401-6, proceed to Step 2. If the signal at U1401-6 is always low, the fault is probably in the reset circuit. Proceed to the Reset circuitry paragraphs in this section of the manual.

Step 2. Look at the signal at the watchdog tickle (WDT Tickle) pin of the MPU, U1401-17. The signal should be high during the short reset pulse. The signal should switch low within 6 ms of the time that the reset pin (U801-6) switches high. After this point, a high pulse should occur approximately every 53 milliseconds.

If the WDT Tickle signal does not switch low after the reset pulse, this indicates that the board is failing at the beginning of the self-diagnostic routine. The board fault is probably in one of four areas: either MPU U1401 is faulty, program EPROM U1403 is faulty, Address Latch U1402 is faulty, or there is a short circuit on one of the MPU address or data lines. Proceed to Step 6. If the WDT Tickle signal does go low after the reset signal, then either the WDT Tickle signal pulses are not spaced properly (approximately 53 milliseconds apart), or there is a failure in the watchdog timer circuitry. To troubleshoot this type of failure, proceed to Step 3.

Step 3. When WDT Tickle pin U1401-17 goes low, U1414-13 should switch high, making U1426-12, 11, and U1414-9 all high. Look for these signals to occur before proceeding. If they do not, look for some fault causing this malfunction.

Step 4. Check the signal at U1415-13. It should go high when WDT Tickle pin U1401-17 goes low, and stay high for approximately 9 to 21 milliseconds, and then switch low until the WDT Tickle signal switches from high to low again. If the WDT Tickle signal goes high sometime before U1415-13 goes low, then both pins U1430-1 and U1430-2 are high making U1430-3 low. This will reset the MPU via U1414A and U1414B. This action indicates that the self-diagnostic routines are not running properly. Proceed to Step 7.

Step 5. Check U1414-13 again. If this pin is staying high for more than 80 milliseconds before switching low, this indicates that the self-diagnostic routines are not running properly. Proceed to Step 7.

Step 6. Look at the E (Enable) pin U1401-40. The signal on this pin should be a square wave that is low for 408 nanoseconds and high for 408 nanoseconds. If this signal is not present, or has the wrong duty-cycle, check the supply lines to the MPU and the connections to crystal Y1401 and capacitors C1410 and C1411. If all these connections are correct and the proper signal is not present, replace MPU U1401.

Step 7. Look at Address Strobe (AS) pin U1401-39. The signal on this pin should be a square wave that is high for 200 nanoseconds and low for 600 nanoseconds. If this pin is not changing, or has the wrong duty-cycle, look for a short circuit on the line. If there is no short, either MPU U1401 or Address U1402 is defective.

Step 8. Look at: the High-Order Address pins U1401-22 through -29; the Low-Order Address pins U1401-2, -5, -6, -9, -12, -15, -16, and -19, and the data pins at U1401-30 through -37. If any of these pins are not changing state (are either always high or always low), look for a short circuit on that line.

Step 9. Look at MPU programming pins U1401-8 and U1401-10. When U1401-6 goes low, these pins should also be low. When U1401-6 switches high, the pins also

switch high, momentarily. If these pins do not go low, check programming diodes CR1403 and CR1405. MPU U1401-6 can be forced low by putting S801 on the Station Control board front panel to the TEST position.

Step 10. If none of the previous steps reveals a fault, then probably either Program EPROM U1403 or MPU U1401 is damaged and should be replaced. Return to Step. 1.

4.2.3 Reset Driver Circuitry

The following procedure describes and examines faults that are indicated when reset pin U1401-6 of the MPU is always low.

Step. 1 Look at the Expansion Reset signal on U1419-8 or J1402-4. If this signal is always low, check the External Reset signal at U1401-16. This signal should always be high if the MPU is always reset. Also check that U1421-6 and U1419-9, -11 are low. Check that pull-up resistor R1425 on the Expansion Reset line is connected. If no fault is found on these areas, another module is holding Expansion Reset low through J1402. Check for a short on these modules.

Step. 2. If the Expansion Reset signal is high, but the MPU Reset pin U1401-6 is low, then look for a fault in the logic circuitry between those points: U1421D, E, U1430B, U1401.

4.2.4 PL/DPL Decode Filter Circuits

The network from J1402-31 to U1440-7 is a low-pass filter for DPL with nearly unity gain below 150Hz and falling rapidly above 150Hz. U1427A is used as a limiter that converts the DPL signal at U1440-7 to a sharp square wave signal. This square wave signal is routed to the Multi-DPL circuitry for decoding. The same signal is routed to the MPU via a logic gate on hybrid HY1401 which converts the square wave to TTL logic levels. The network from J1402-31 to U1440-8 is a low-pass filter for PL with nearly unit gain below 250Hz and falling rapidly above 250Hz. The circuits from U1440-8 to U1427-2 and including Q1405 comprise a limiter with hysteresis which converts the PL signal to a square wave signal with TTL logic levels.

4.2.5 PL/DPL Encode Digital-to-Analog Converter (DAC) and Filter Circuit

The circuits on hybrid HY1401 convert data inputs from DAC Latch U1404 into PL or DPL signals for transmission. The PL/DPL Encode Tones at output HY1401-17 have only about 1% distortion and need no further filtering. The PL/DPL signal level is about 3.1 V peak-to-peak.

4.2.6 Multi-DPL Circuitry

When a failure occurs with the detection of a DPL code, refer to the troubleshooting flowchart.

4.3 SERVICING

While servicing, it may be desirable to key the station with a specific PL or DPL code. The Multi-Coded Squelch module offers this capability. (The Diagnostic Metering Panel, option C668AA, must be installed.) This section will describe step by step how to execute this function.

Step 1. Determine the MCS identifier number for the desired PL or DPL code. (Refer to Section 5, Acceptable PL/DPL Codes, of this manual.)

Step 2. Use Table 2 to convert the first digit of the two-digit identifier number from hexadecimal to binary representation. Next, enter this binary number into the 4 Data toggle switches on the DMP. A Data switch in the 'UP' position represents a logic '1', while a Data switch in the 'DOWN' position represents a logic '0'. Then, write this data to MUXbus Address 11.

Step 3. Flip the Access Disable/Test switch on the Station Control board front panel to the Access Disable position. The ACC DIS bit on the DMP MUXbus display should turn on.

Step 4. Following the procedure outlined in Step 2 above, enter the second digit of the Identifier number into MUXbus address 10.

Step 5. Plug a handset or microphone into the Control jack (J812) on the front panel of the Station Control board. Keying the microphone or handset (an active MIC PTT signal) will now encode the desired PL or DPL code.

Example:

To encode PL code 7A (192.8 Hz), the following steps would be taken. Section 5 lists the MCS Identifier number for PL code 7A as hexadecimal \$9D. Therefore, binary 1001 would be written to MUXbus address 11 and the Access Disable switch activated. Binary 1101 (equivalent to hexadecimal 'D') would then be written to MUXbus address 10. A handset plugged into the Control jack on the Station Control board can now be used to key up on PL code 7A.

5. ACCEPTABLE PL/DPL CODES

The Multi-Coded Squelch board is capable of detecting 103 DPL codes and 37 PL codes. However, not all of these codes can be easily detected. Of the 103 DPL codes, 83 are recommended. The remaining 20 have poor falsing and quieting characteristics and conse-

quently are not normally recommended. Of the 41 defined PL codes, 30 are standard EIA codes and are easily detected. Seven codes are not recommended because their frequencies are close to the cutoff frequency of the PL Low-Pass Filter. As a result, the sensitivity of these 7 codes is degraded. The remaining 4 defined PL codes cannot be decoded by the standard MCS module.

Each PL or DPL has an MCS Identifier number associated with it. This number is used by the processor to identify a given code by means of a software look-up table.

The following table lists the standard (recommended) DPL codes as well as the MCS Identifier number.

Table 2. Hexadecimal/Binary Conversion

Hexadecimal	Binary D3 D2 D1 D0
\$0	0000
\$1	0001
\$2	0010
\$3	0011
\$4	0100
\$5	0101
\$6	0110
\$7	0111
\$8	1000
\$9	1001
\$A	1010
\$B	1011
\$C	1100
\$D	1101
\$E	1110
\$F	1111

Table 3. Standard DPL Codes and Identifier Numbers

DPL Code	Identifier (Hex)	DPL Code	Identifier (Hex)	DPL Code	Identifier (Hex)
023	\$01	174	\$1D	445	\$39
025	\$02	205	\$1E	464	\$3A
026	\$03	223	\$1F	465	\$3B
031	\$04	226	\$20	466	\$3C
032	\$05	243	\$21	503	\$3D
043	\$06	244	\$22	506	\$3E
047	\$07	245	\$23	516	\$3F
051	\$08	251	\$24	532	\$40
054	\$09	261	\$25	546	\$41
065	\$0A	263	\$26	565	\$42
071	\$0B	265	\$27	606	\$43
072	\$0C	271	\$28	612	\$44
073	\$0D	306	\$29	624	\$45
074	\$0E	311	\$2A	627	\$46
114	\$0F	315	\$2B	631	\$47
115	\$10	331	\$2C	632	\$48
116	\$11	343	\$2D	654	\$49
125	\$12	346	\$2E	662	\$4A
131	\$13	351	\$2F	664	\$4B
132	\$14	364	\$30	703	\$4C
134	\$15	365	\$31	712	\$4D
143	\$16	371	\$32	723	\$4E
152	\$17	411	\$33	731	\$4F
155	\$18	412	\$34	732	\$50
156	\$19	413	\$35	734	\$51
162	\$1A	423	\$36	743	\$52
165	\$1B	431	\$37	754	\$53
172	\$1C	432	\$38		

Table 4. DPL Codes Held in Reserve*

DPL Code	Identifier (Hex)	DPL Code	Identifier (Hex)	DPL Code	Identifier (Hex)
053	\$54	325	\$5B	552	\$62
122	\$55	425	\$5C	564	\$63
212	\$56	446	\$5D	645	\$64
225	\$57	452	\$5E	652	\$65
246	\$58	455	\$5F	725	\$66
252	\$59	521	\$60	726	\$67
266	\$5A	525	\$61		

* Held in reserve due to poor falsing and quieting characteristics.

Table 5. Recommended PL Codes and Identifier Numbers

PL Code	Identifier (Hex)	Frequency (Hz)	PL Code	Identifier (Hex)	Frequency (Hz)
XZ	\$80	67.0	2B	\$8F	118.8
XA	\$81	71.9	3Z	\$90	123.0
WA	\$82	74.4	3A	\$91	127.3
XB	\$83	77.0	3B	\$92	131.8
WB	\$84	79.7	4Z	\$93	136.5
YZ	\$85	82.5	4A	\$94	141.3
YA	\$86	85.4	4B	\$95	146.2
YB	\$87	88.5	5Z	\$96	151.4
ZZ	\$88	91.5	5A	\$97	156.7
ZA	\$89	94.8	5B	\$98	162.2
1Z	\$8A	100.0	6Z	\$99	167.9
1A	\$8B	103.5	6A	\$9A	173.8
1B	\$8C	107.2	6B	\$9B	179.9
2Z	\$8D	110.9	7Z	\$9C	186.2
2A	\$8E	114.8	7A	\$9D	192.8

Table 6. PL Codes Held in Reserve

PL Code	Identifier (Hex)	Frequency (Hz)	PL Code	Identifier (Hex)	Frequency (Hz)
M1	\$9E	203.5	M5	\$A2	223.6
M2	\$9F	210.7	M6	\$A3	241.8
M3	\$AO	218.1	M7	\$A4	250.3
M4	\$A1	225.7			

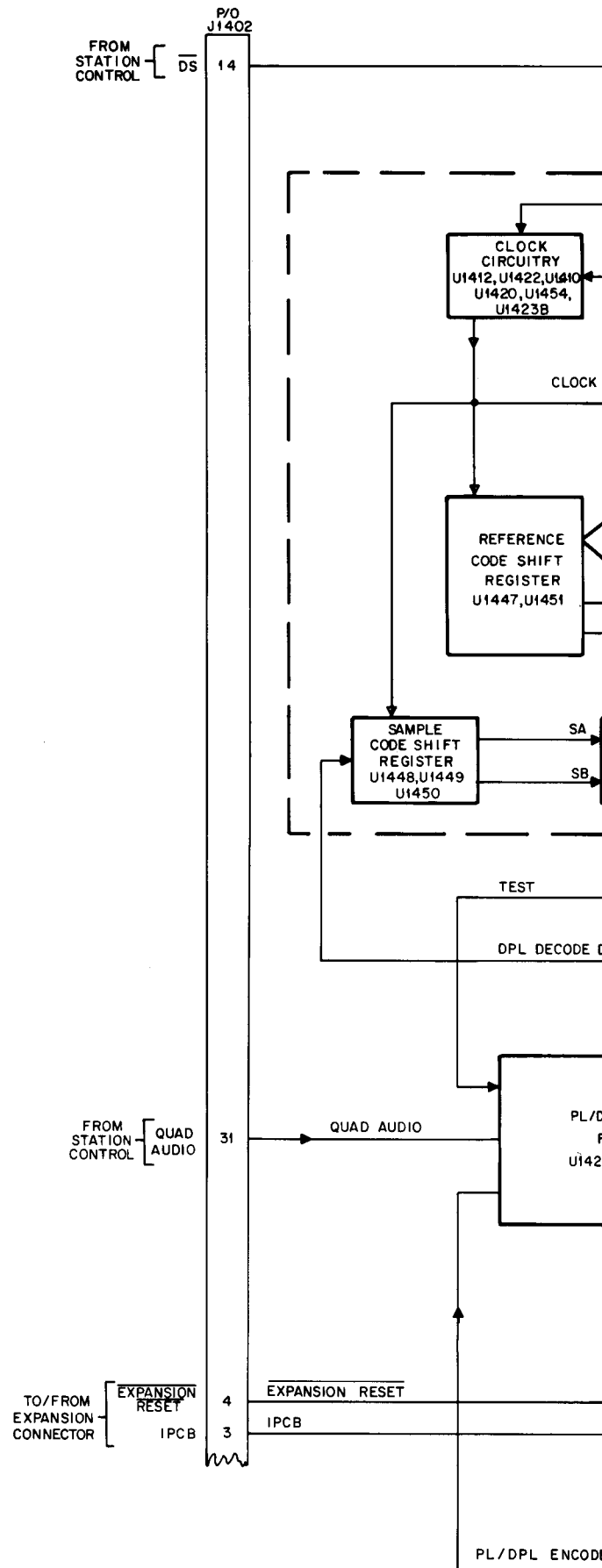
Table 7. PL Codes Not Decoded by MCS Module

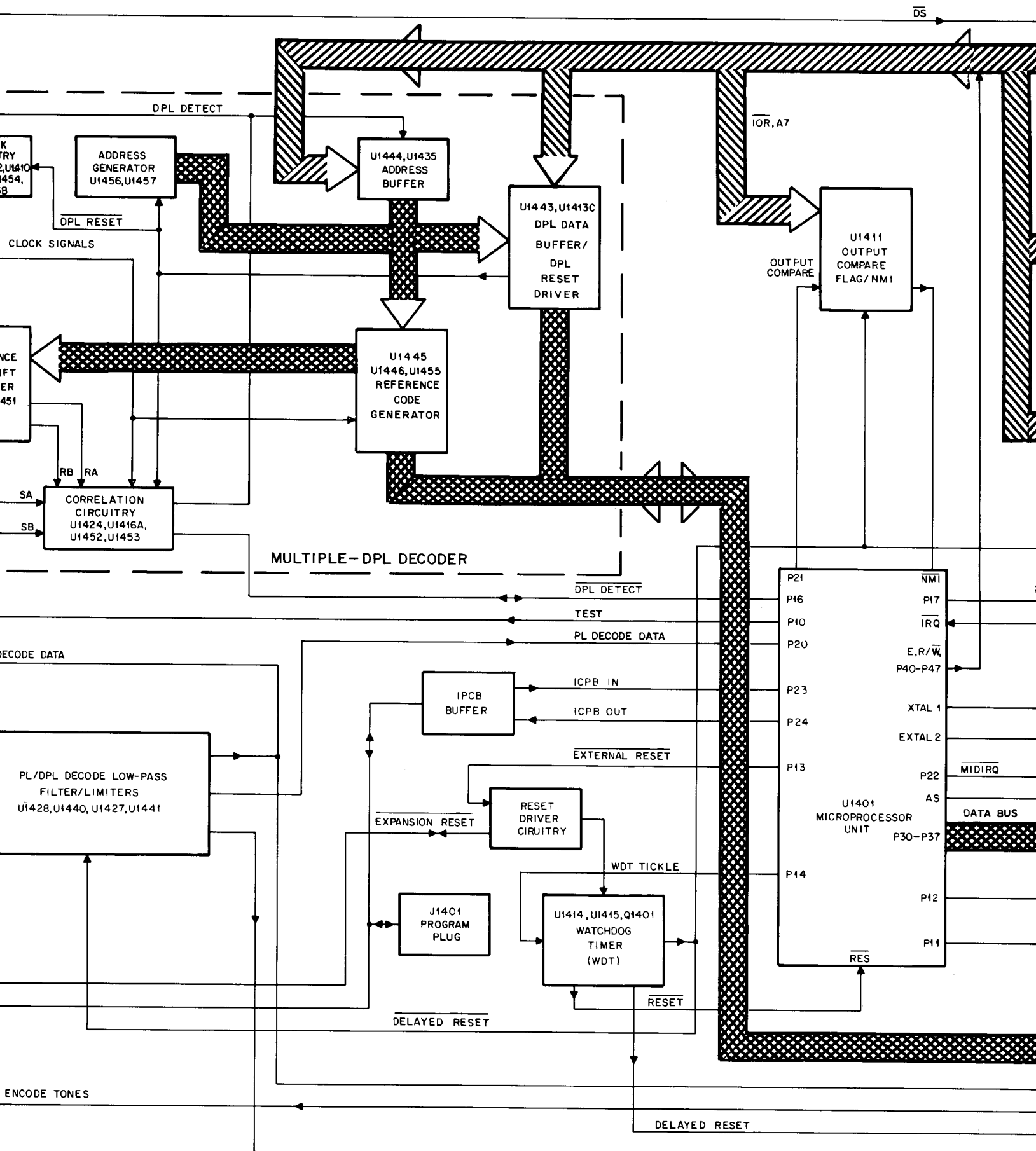
PL Code	Frequency (Hz)	PL Code	Frequency (Hz)
WZ	69.3	8Z	206.5
ZB	97.4	9Z	229.1

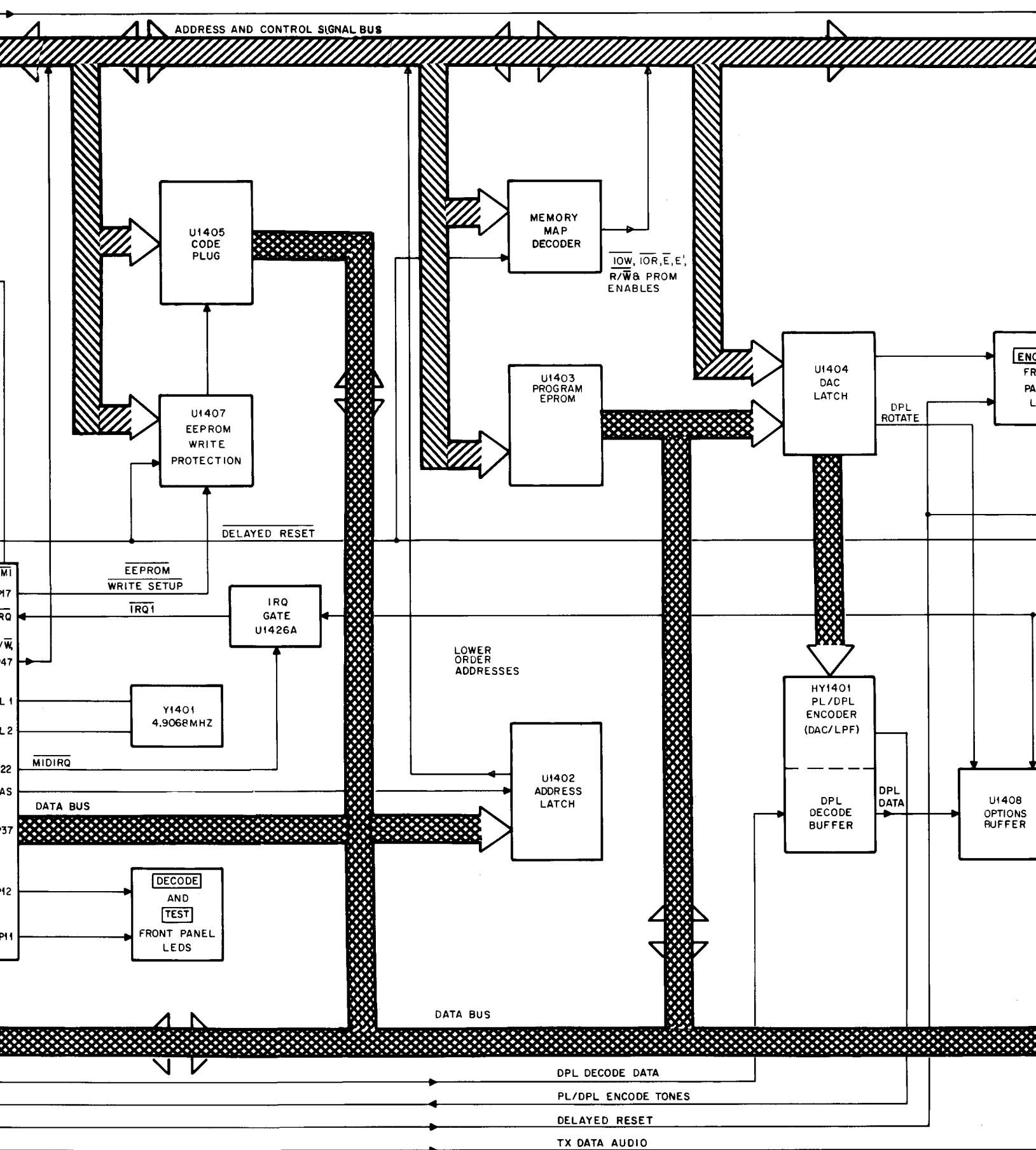
**Page 20 was
a blank sheet.**

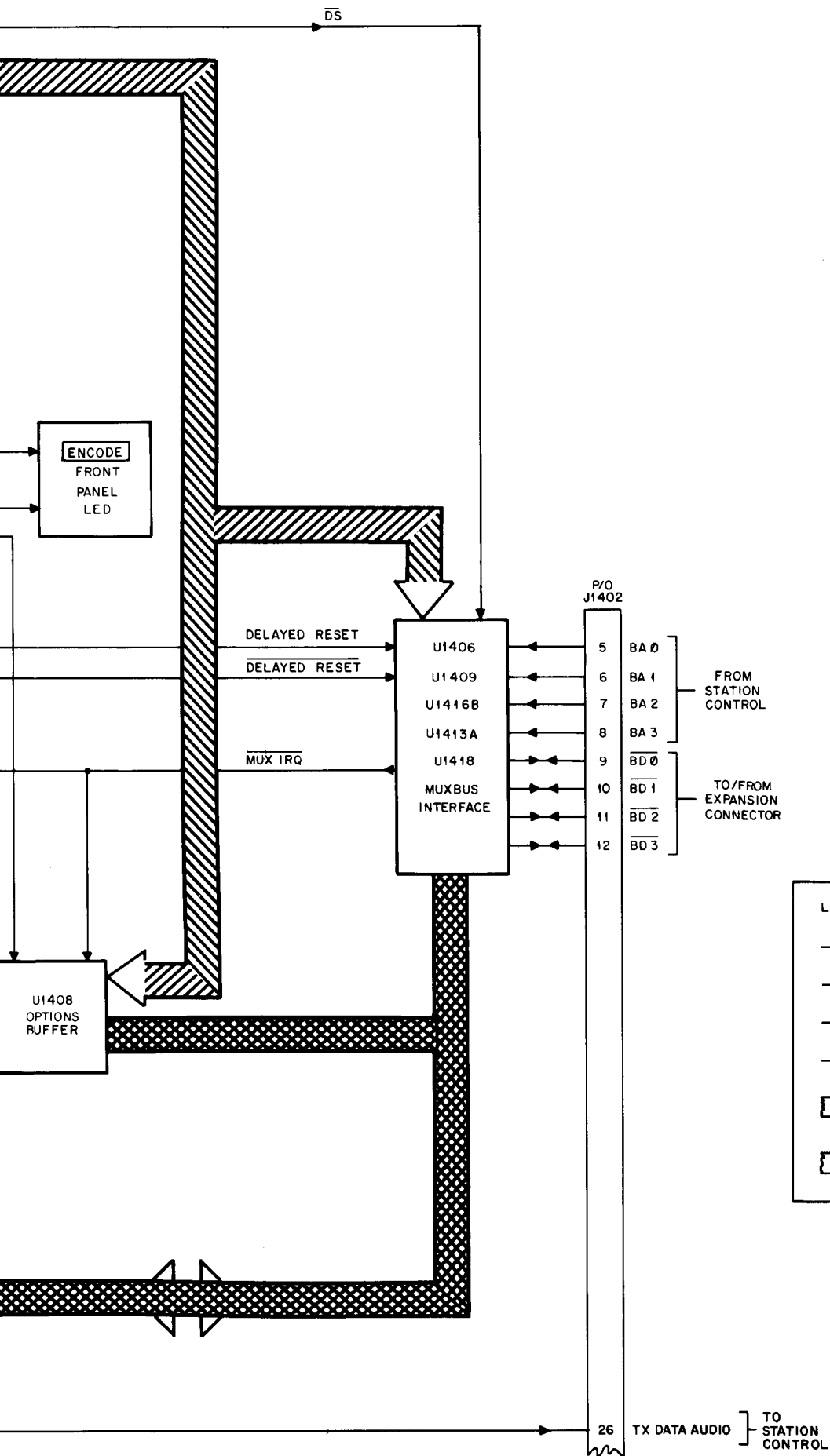
**Page 21 was the
Troubleshooting
Flow Chart Diagram**

*Multi-Coded Squelch Module
Block Diagram
Motorola No. EEPS-38305-O
6/12/84-PHI*









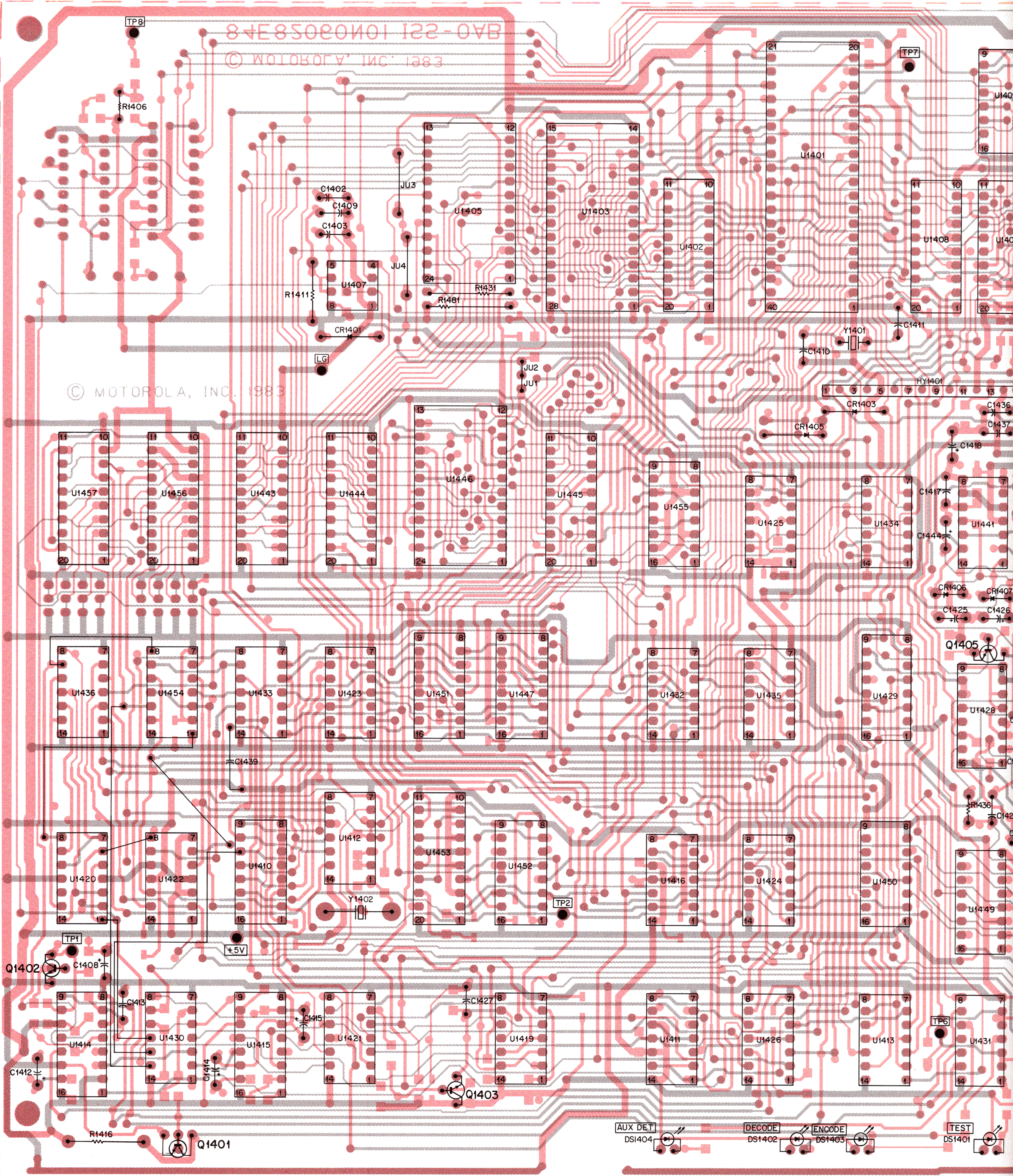
LEGEND:

- ▶— = INDIVIDUAL LOGIC OR SIGNAL LINE
- ▶— = MULTIPLE SIGNALS
- ◄—▶ = TWO-WAY SIGNAL (NOT SIMULTANEOUS)
- ◄—▶ = SIMULTANEOUS TWO WAY SIGNAL
- ◄—▶ = ONE-WAY BUS SIGNALS
- ◄—▶ = TWO-WAY BUS SIGNALS (NOT SIMULTANEOUS)

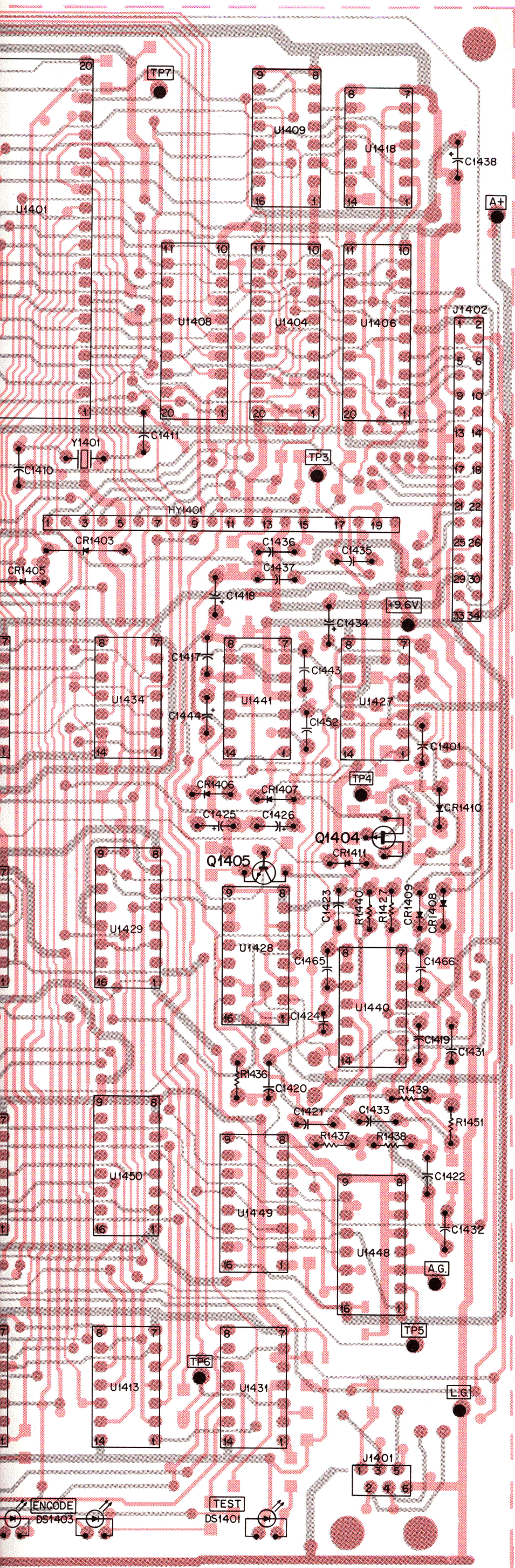
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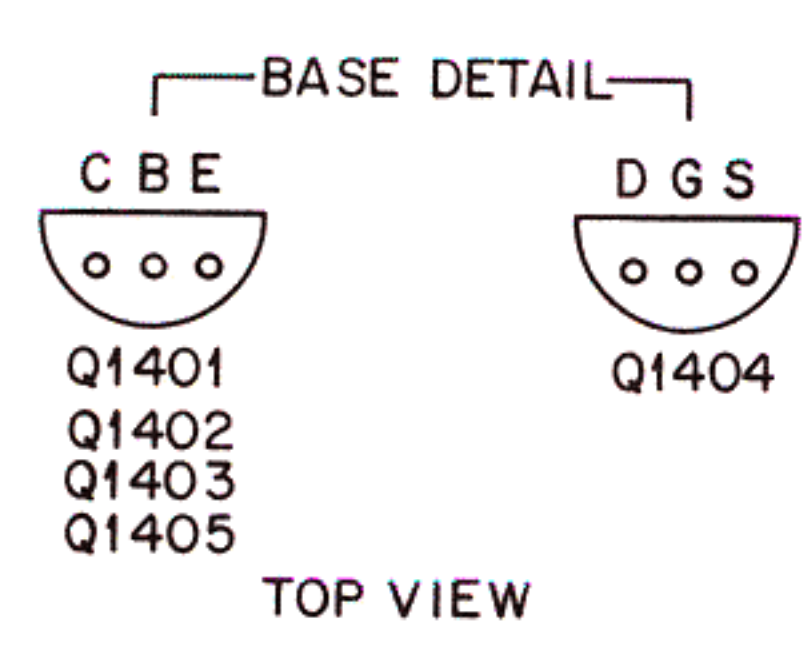
© MOTOROLA, INC. 1983



EARLIER VERSION

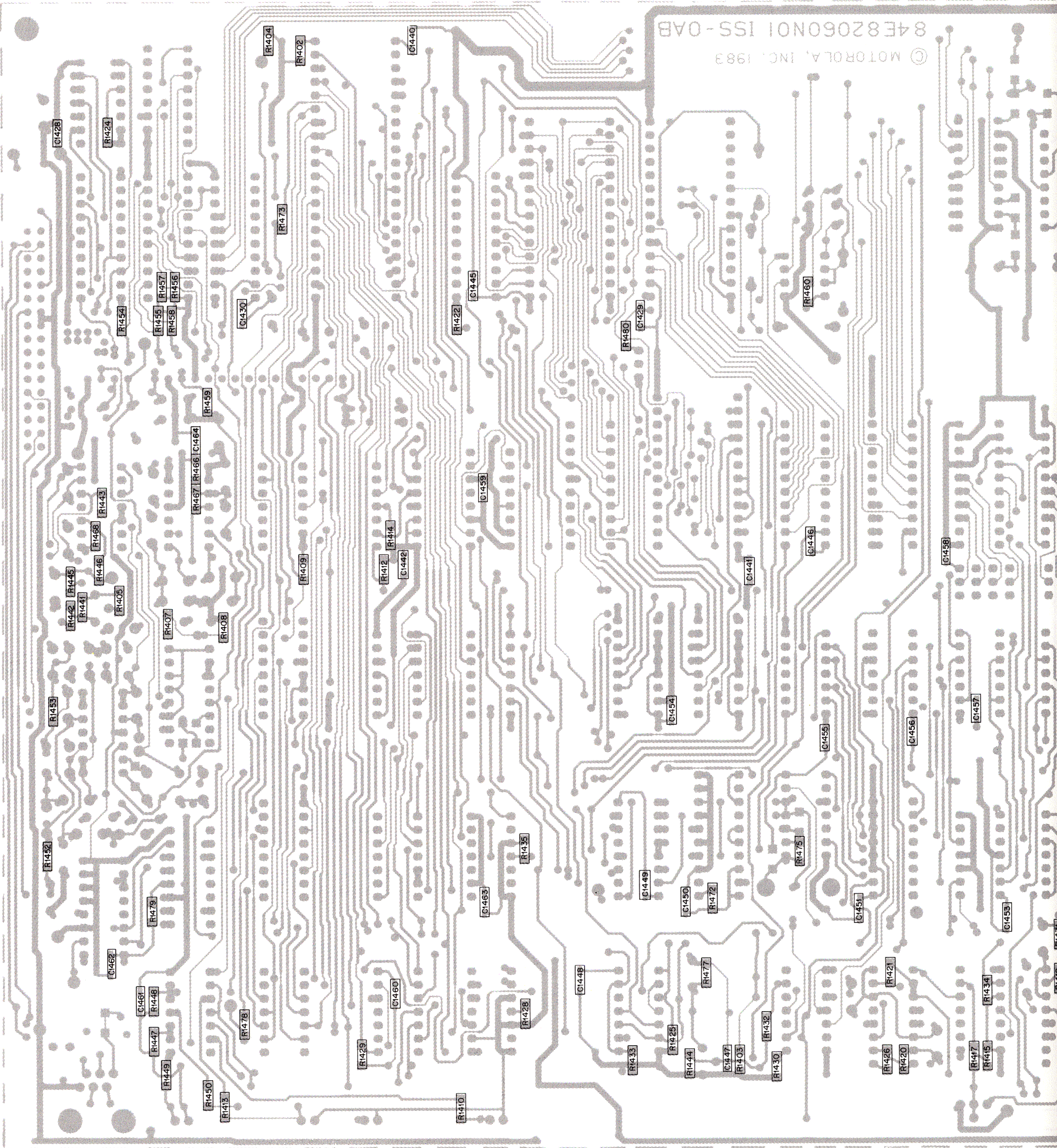


J1402	
+5V	1 2 +5V
IPCB	3 4 EXPANSION RESET
BA0	5 6 BA1
BA2	7 8 BA3
BD0	9 10 BD1
BD2	11 12 BD3
LOGIC GROUND (L.G.)	13 14 DS
LOGIC GROUND (L.G.)	15 16 N.C.
N.C.	17 18 N.C.
N.C.	19 20 N.C.
N.C.	21 22 N.C.
N.C.	23 24 SELECT AUDIO
LOCAL AUDIO	25 26 TX DATA AUDIO
RX2 AUDIO	27 28 TX AUDIO
AUDIO GROUND (A.G.)	29 30 RX 1 AUDIO
QUAD AUDIO	31 32 AUDIO REF
+9.6V	33 34 +13.8V



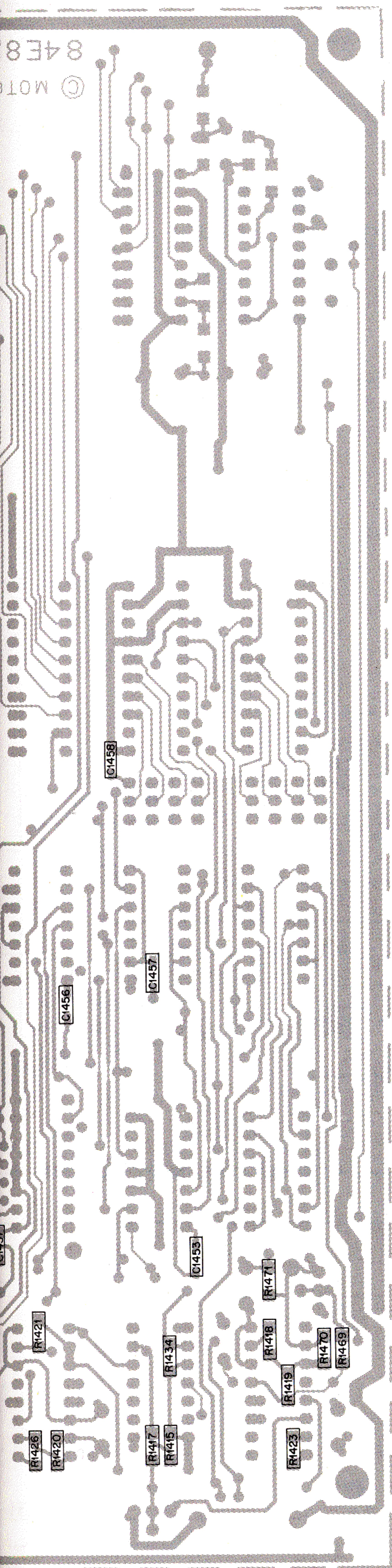
COMPONENT SIDE * BD-EEPS-38306-A
SOLDER SIDE * BD-EEPS-38307-A
OL-EEPS-38308-A

SHOWN FROM COMPONENT SIDE



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84E82060N01 ISS-0AB

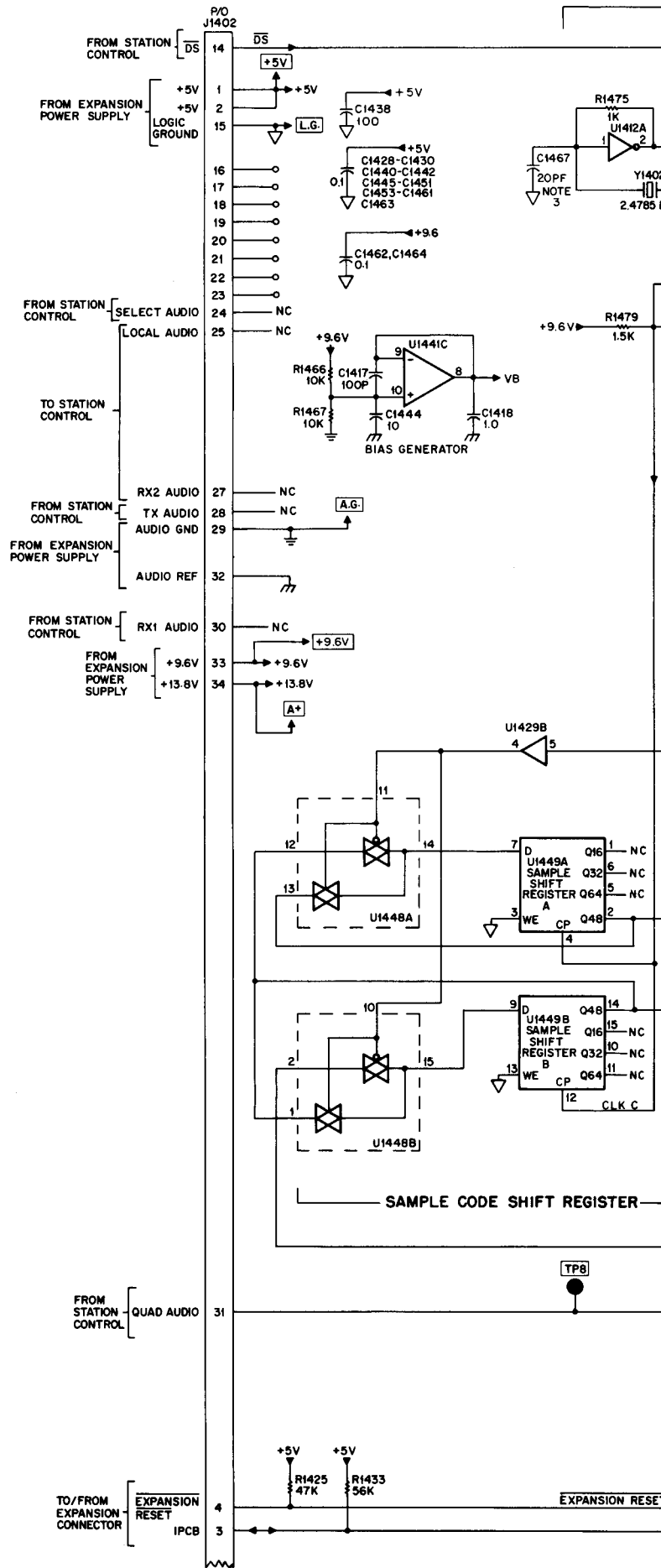
SHOWN FROM SOLDER SIDE



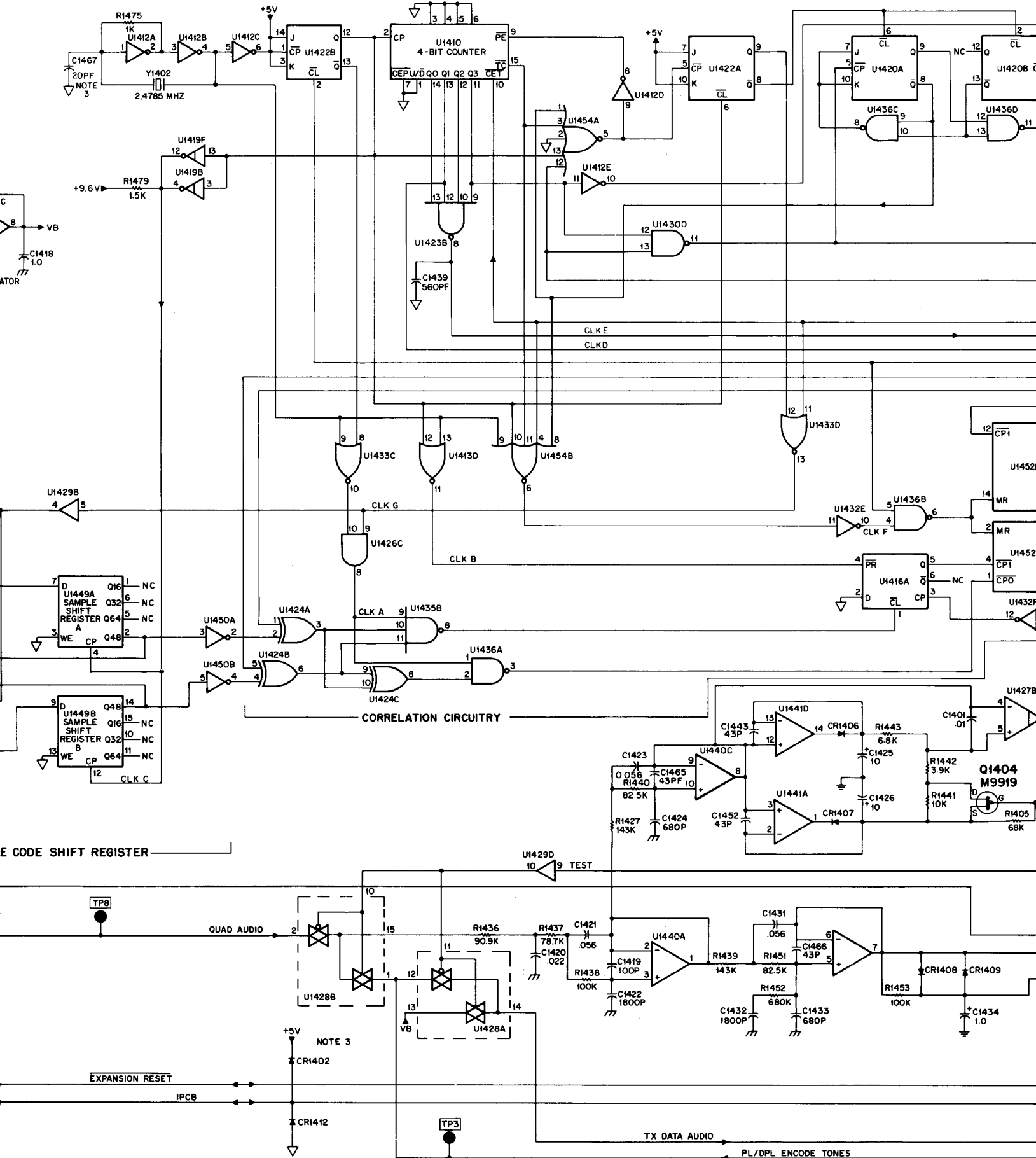
SOLDER SIDE ■ BD-EEPS-38692-0
OL-EEPS-38693-0

*Multi-Coded Squelch Module
Earlier Version Circuit Board Detail
Motorola No. PEPS-38310-A
(Sheet 1 of 6)
3/1/84-PHI*

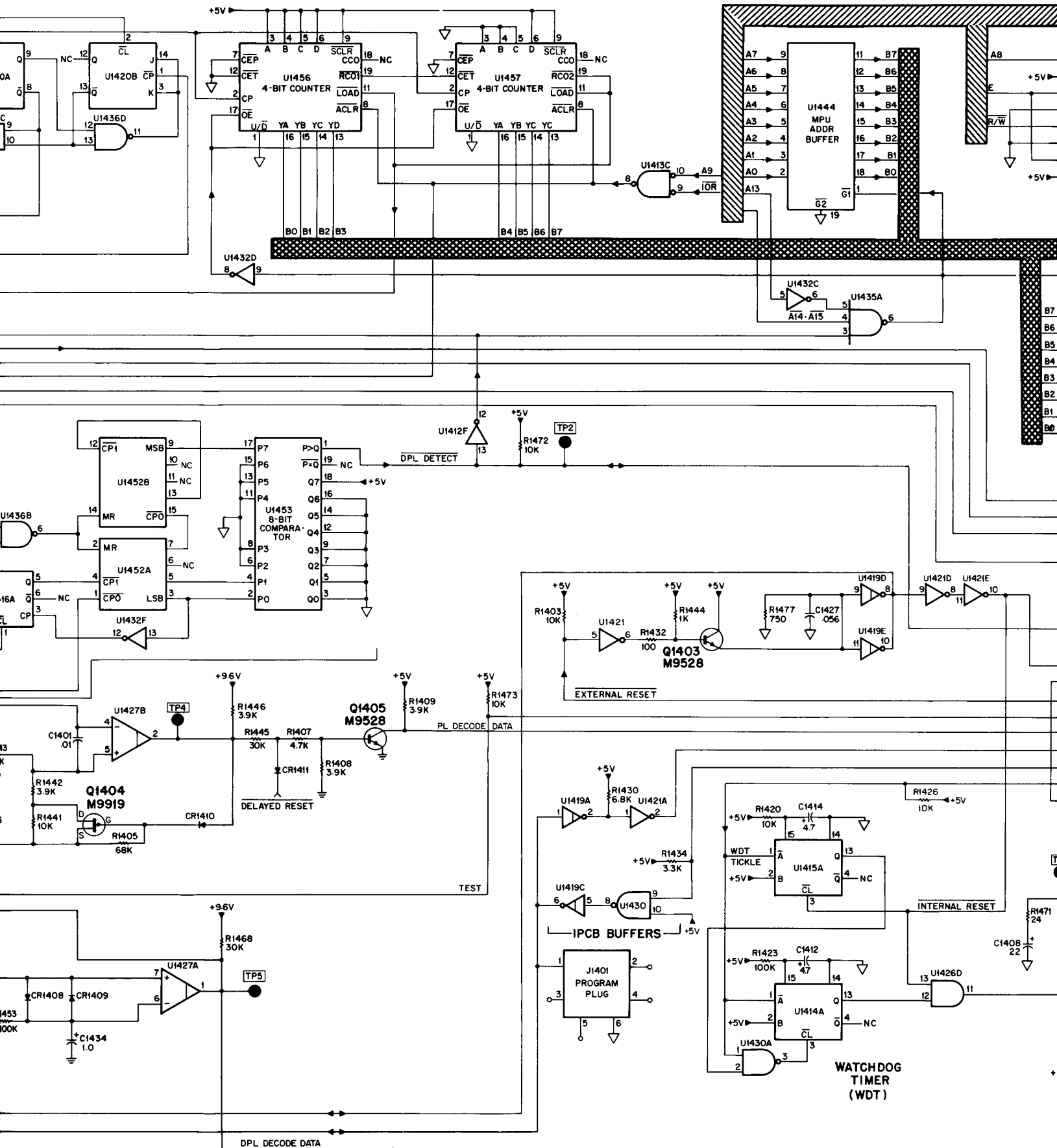
Multi-Coded Squelch Module
Schematic Diagram
Motorola No. PEPS-38310-A
(Sheet 2 of 6)
3/1/84-PHI



CLOCK CIRCUITRY



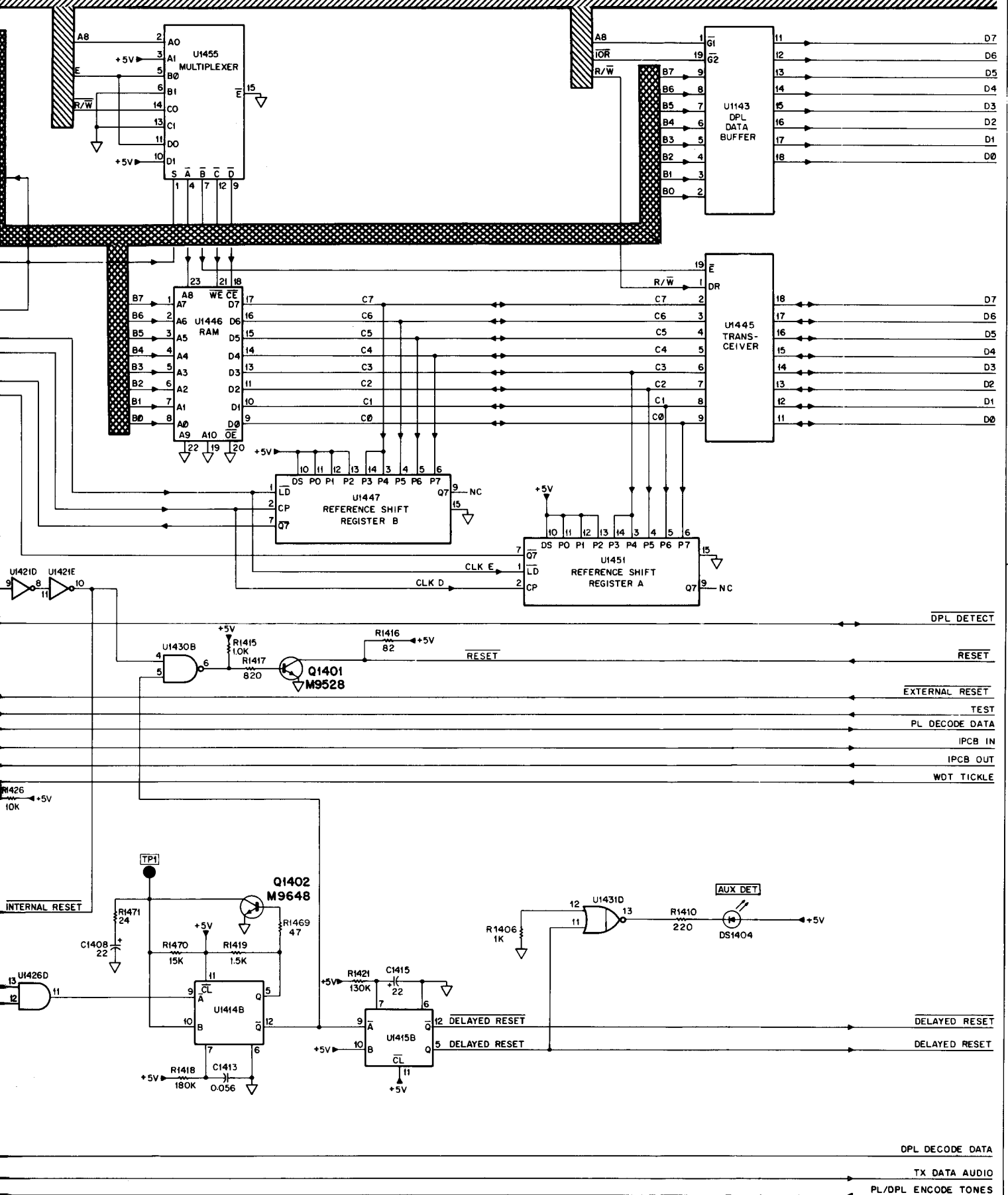
ADDRESS GENERATOR



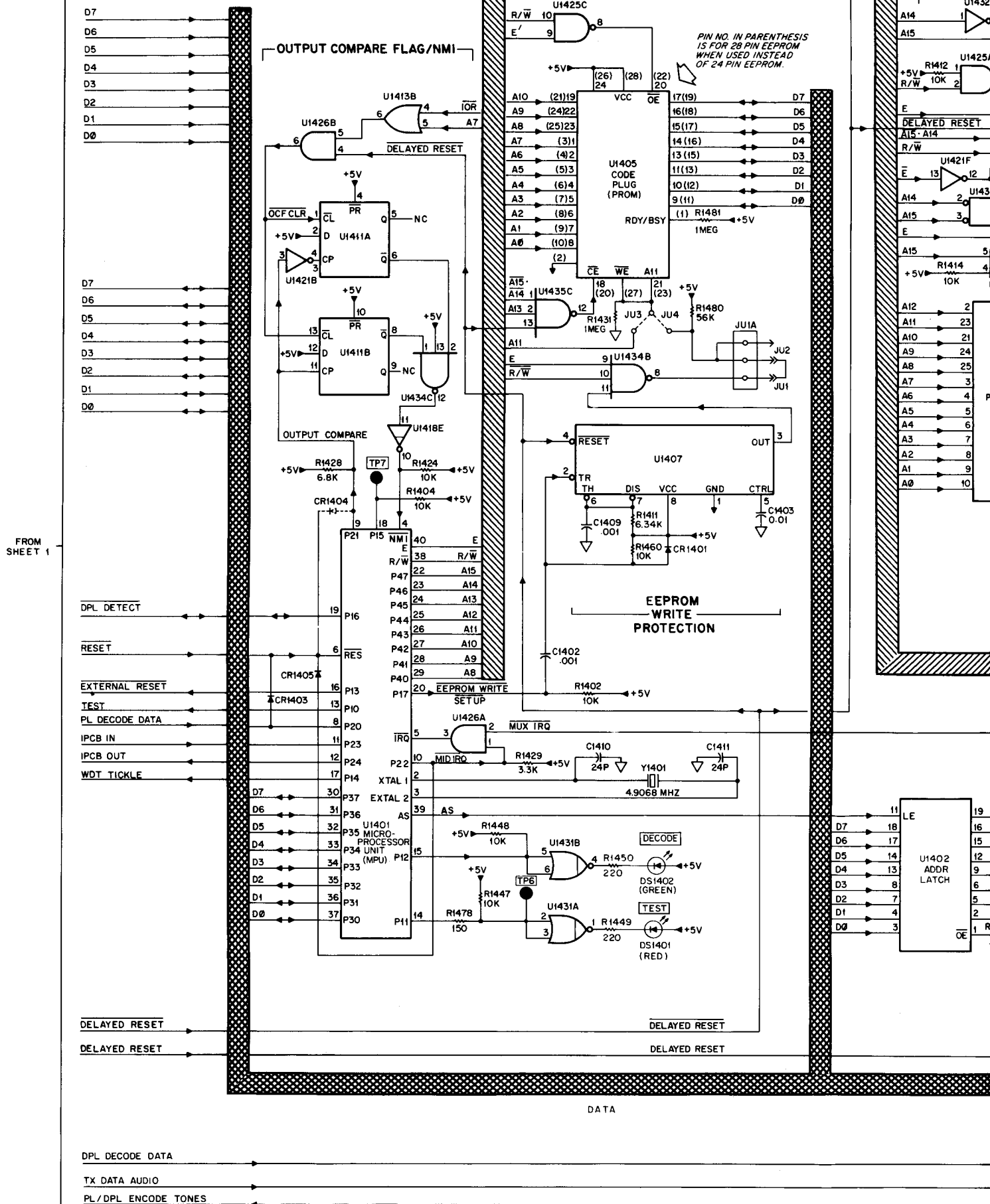
REFERENCE CODE GENERATOR

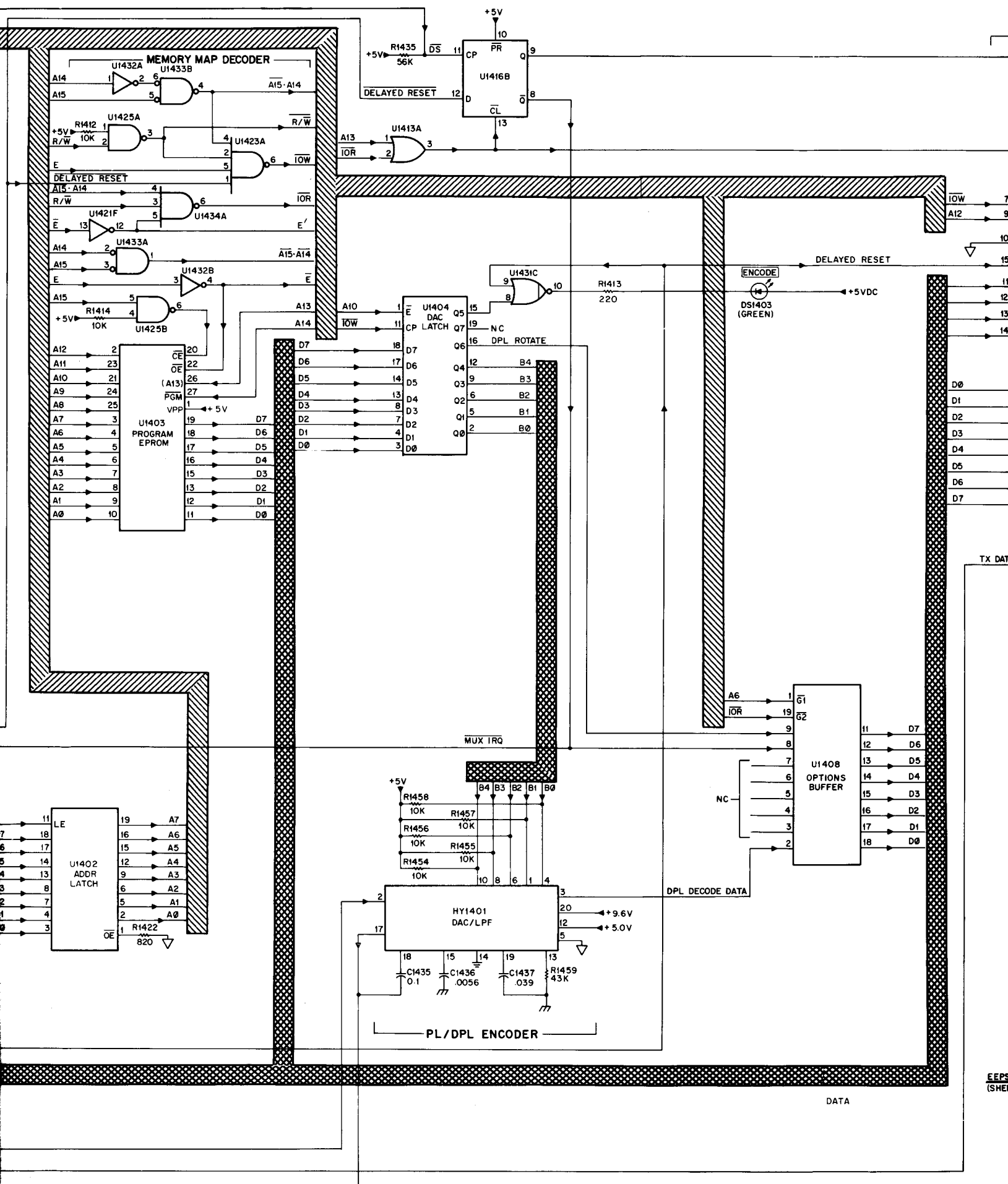
05

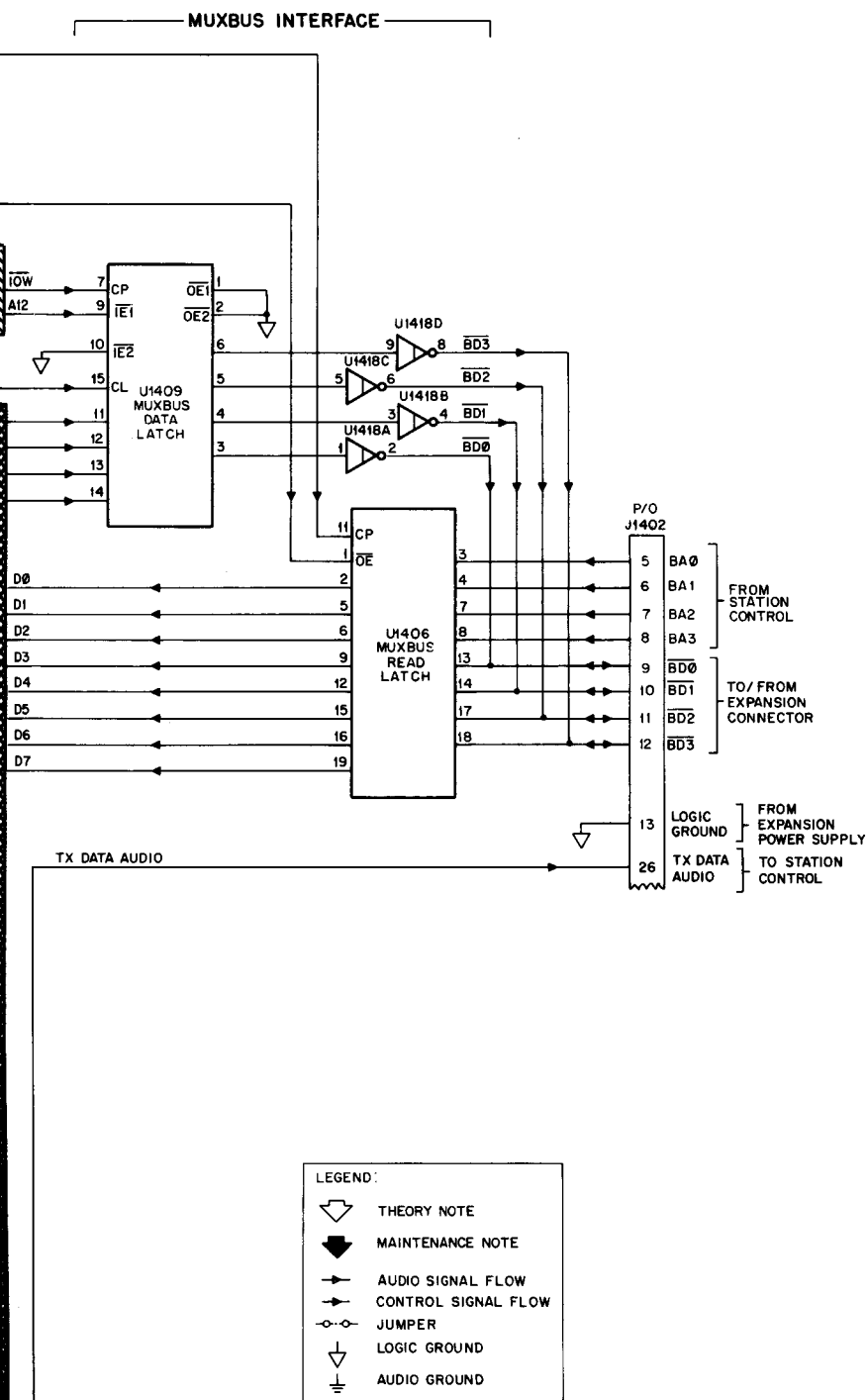
ADDRESS/CONTROL



TO
SHEET 2







NOTES:

1. Unless otherwise specified, all resistor values are in ohms and all capacitor values are in microfarads.
2. Voltage values are dc unless otherwise specified.
3. C1467, CR1402, and CR1412 are not used on PC board part number 84-82060N01.

Integrated Circuit Data Chart

IC No.	+ 5 V (VCC)	+ 9.6 V	Logic GND
U1401	7, 21		1
U1402	20		10
U1403	28		14
U1404	20		10
U1405	28		14
U1406	20		10
U1407	8		1
U1408	20		10
U1409	16		8
U1410	16		8
U1411	14		7
U1412	14		7
U1413	14		7
U1414	16		8
U1415	16		8
U1416	14		7
U1418	14		7
U1419	14		7
U1420	4		11
U1421	14		7
U1422	4		11
U1423	14		7
U1424	14		7
U1425	14		7
U1426	14		7
U1427		3	
U1428		16	
U1429	1, 13	16	8
U1430	14		7
U1431	14		7
U1432	14		7
U1433	14		7
U1434	14		7
U1435	14		7
U1436	14		7
U1440		4	
U1441		4	
U1443	20		10
U1444	20		10
U1445	20		10
U1446	24		12
U1447	16		8
U1448		16	
U1449		16	
U1450	1		8
U1451	16		8
U1452	16		8
U1453	20		10
U1454	14		7
U1455	16		8
U1456	20		10
U1457	20		10

Jumper/Diode Data

Jumper	Normal Position	Description
JU1401	In	Out to disable U1405 EEPROM write
JU1402	Out	In to disable U1405 EEPROM write
JU1403	Out	In for 2732 EPROM code plug.
JU1404	In	Out for 2732 EPROM code plug.
CR1403	In	Microprocessor mode Programming jumper. In = 0 Out = 1
CR1404	Out	
CR1405	In	

NOTES:

1. Unless otherwise specified, all resistor values are in ohms and all capacitor values are in microfarads.
2. Voltage values are dc unless otherwise specified.
3. C1467, CR1402, and CR1412 are not used on PC boards with a 84-82060N01 part number.

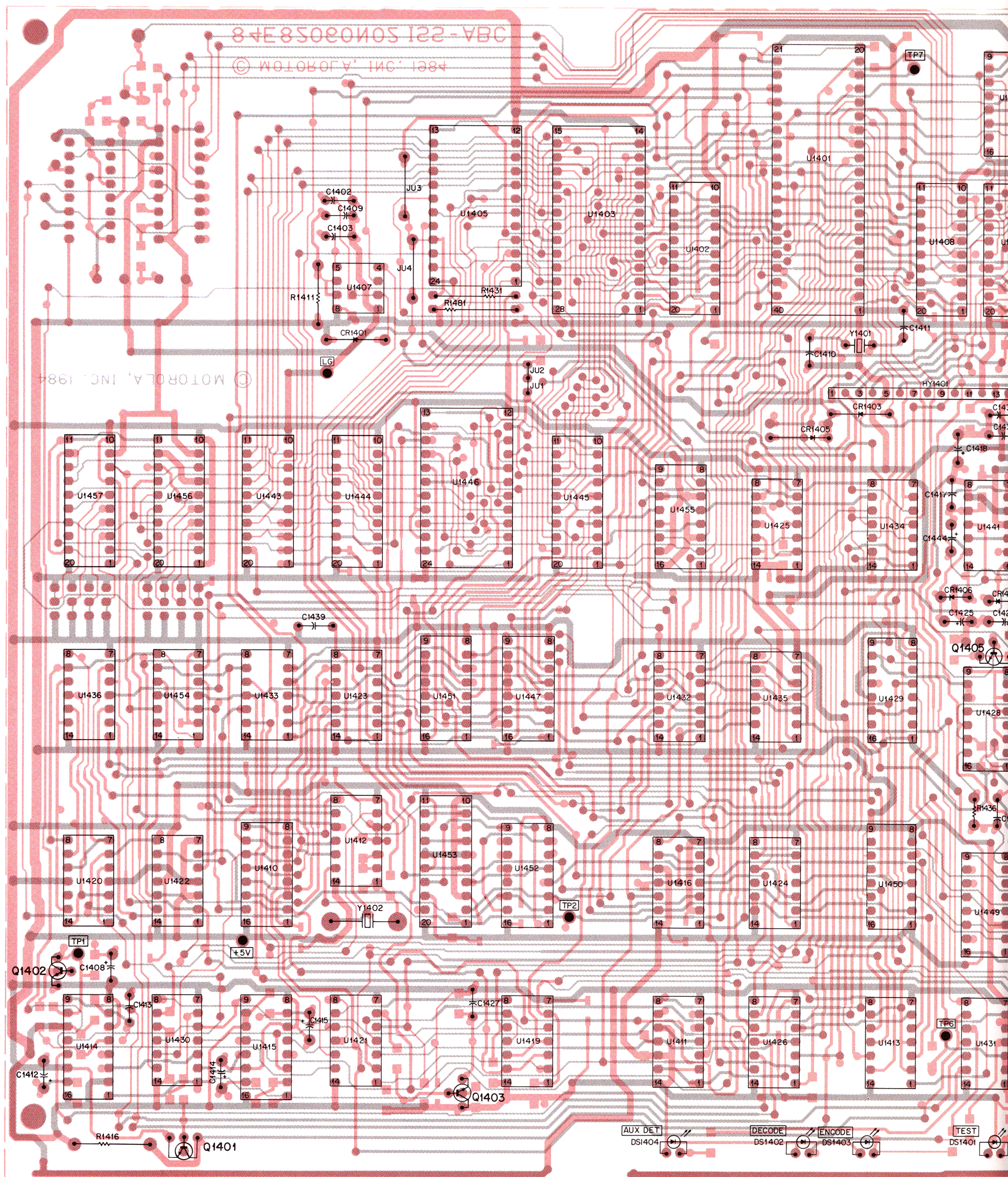
Integrated Circuit Data Chart

IC No.	+ 5 V (VCC)	+ 9.6 V	Logic GND	Audio GND
U1401	7, 21		1	
U1402	20		10	
U1403	28		14	
U1404	20		10	
U1405	28		14	
U1406	20		10	
U1407	8		1	
U1408	20		10	
U1409	16		8	
U1410	16		8	
U1411	14		7	
U1412	14		7	
U1413	14		7	
U1414	16		8	
U1415	16		8	
U1416	14		7	
U1418	14		7	
U1419	14		7	
U1420	4		11	
U1421	14		7	
U1422	4		11	
U1423	14		7	
U1424	14		7	
U1425	14		7	
U1426	14		7	
U1427		3		12
U1428		16		6, 7, 8
U1429	1, 13	16	8	
U1430	14		7	
U1431	14		7	
U1432	14		7	
U1433	14		7	
U1434	14		7	
U1435	14		7	
U1436	14		7	
U1440		4		11
U1441		4		11
U1443	20		10	
U1444	20		10	
U1445	20		10	
U1446	24		12	
U1447	16		8	
U1448		16		6, 7, 8
U1449		16		8
U1450	1		8	
U1451	16		8	
U1452	16		8	
U1453	20		10	
U1454	14		7	
U1455	16		8	
U1456	20		10	
U1457	20		10	

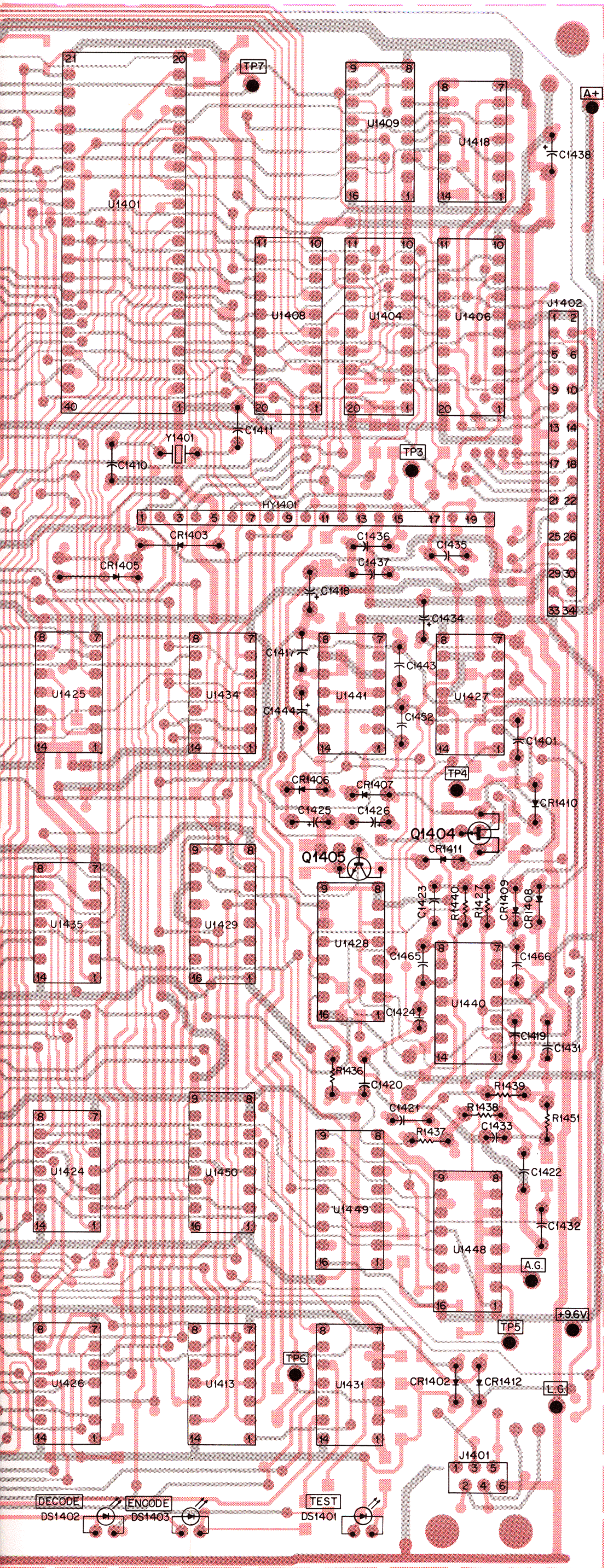
Jumper/Diode Data

Jumper	Normal Position	Description
JU1401	In	Out to disable U1405 EEPROM write.
JU1402	Out	In to disable U1405 EEPROM write.
JU1403	Out	In for 2732 EPROM code plug.
JU1404	In	Out for 2732 EPROM code plug.
CR1403	In	Microprocessor mode
CR1404	Out	Programming jumper.
CR1405	In	In = 0 Out = 1

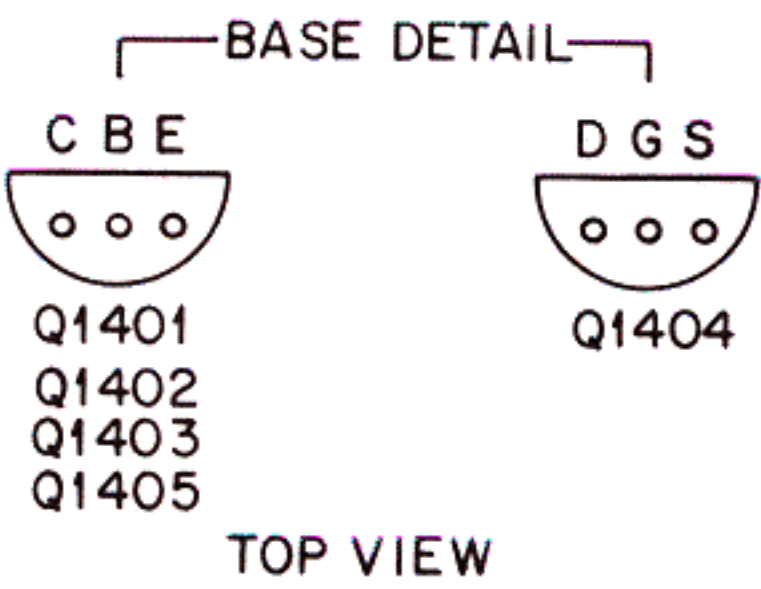
Multi-Coded Squelch Module
Schematic Diagram
Motorola No. PEPS-38310-A
(Sheet 3 of 6)
3/1/84-PHI



LATER VERSION



J1402			
+5V	1	2	+5V
PCB	3	4	EXPANSION RESET
BA0	5	6	BA1
BA2	7	8	BA3
BD0	9	10	BD1
BD2	11	12	BD3
LOGIC GROUND (L.G.)	13	14	DS
LOGIC GROUND (L.G.)	15	16	N.C.
N.C.	17	18	N.C.
N.C.	19	20	N.C.
N.C.	21	22	N.C.
N.C.	23	24	SELECT AUDIO
LOCAL AUDIO	25	26	TX DATA AUDIO
RX2 AUDIO	27	28	TX AUDIO
AUDIO GROUND (A.G.)	29	30	RX 1 AUDIO
QUAD AUDIO	31	32	AUDIO REF
+9.6V	33	34	+13.8V



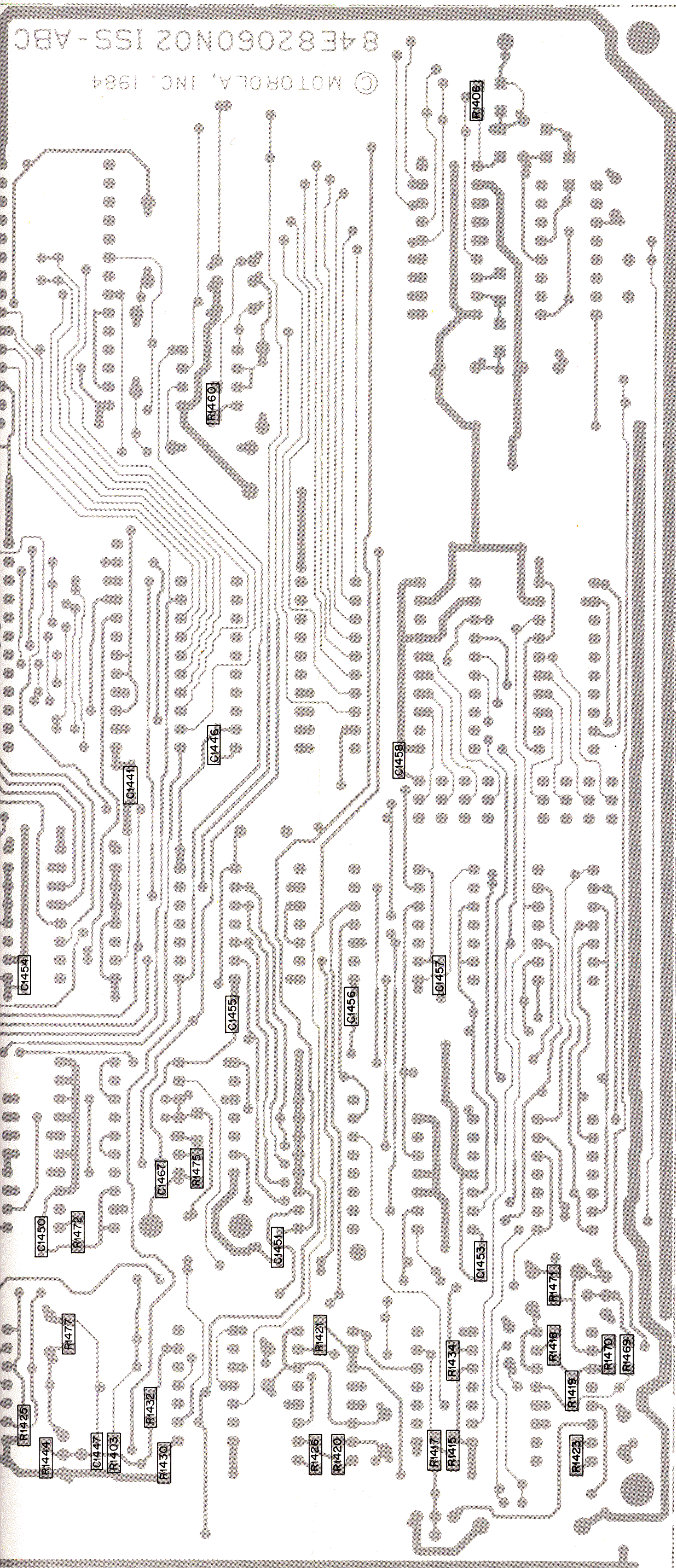
COMPONENT SIDE * BD-EEPS-39774-0
SOLDER SIDE * BD-EEPS-39775-0
OL-EEPS-39776-0

SHOWN FROM COMPONENT SIDE

84E82060N02 ISS - ABC
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SHOWN FROM SOLDER SIDE



SOLDER SIDE * BD-EEPS-39777-0
OL-EEPS-39778-0

parts list

TRN5180A Multi Coded Squelch

PL-8866-A

REFERENCE NUMBER	MOTOROLA PART NO.	DESCRIPTION
C1401	8-11017A08	capacitor, fixed: UF
C1402	8-11017A01	.01 ± 5%: 50 V
C1403	8-11017A08	.01 ± 5%: 50 V
C1408	23-11013C11	22 ± 10%: 15 V
C1409	8-11017A01	.001 ± 5%: 50 V
C1410, 1411	21-11022G39	24pF ± 5%: 50 V
C1412	23-11013E09	4.7 ± 10%: 25 V
C1413	8-11017A15	.056 ± 5%: 50 V
C1414	23-11013E09	4.7 ± 10%: 25 V
C1415	23-11013C11	22 ± 10%: 15 V
C1417	21-11022K42	100pF ± 5%: 50 V
C1418	23-11019A09	1.0 ± 20%: 50 V
C1419	21-11022K42	100pF ± 5%: 50 V
C1420	8-11017A11	.022 ± 5%: 50 V
C1421	8-11017A15	.056 ± 5%: 50 V
C1422	21-84393M02	1800pF ± 5%: 50 V
C1423	8-11017A15	.056 ± 5%: 50 V
C1424	21-84393M01	680pF ± 5%: 50 V
C1425, 1426	23-11019A20	10 ± 20%: 25 V
C1427	8-11017A15	.056 ± 5%: 50 V
C1428 thru 1430	21-11032B13	0.10 ± 80-20%: 50 V (chip)
C1431	8-11017A15	.056 ± 5%: 50 V
C1432	21-84393M02	1800pF ± 5%: 50 V
C1433	21-84393M01	680pF ± 5%: 50 V
C1434	23-11019A09	1.0 ± 20%: 50 V
C1435	8-11017A17	0.1 ± 5%: 50 V
C1436	8-11017A19	.0056 ± 5%: 50 V
C1437	8-11017A30	.039 ± 5%: 50 V
C1438	23-11019A46	100 ± 20%: 20 V
C1439	21-82187B06	560pF ± 10%: 500V
C1440 thru 1442	21-11032B13	0.10 ± 80-20%: 50 V (chip)
C1443	21-11022G45	43pF ± 5%: 50 V
C1444	23-11019A20	10 ± 20%: 25V
C1445 thru 1451	21-11032B13	0.10 ± 80-20%: 50 V (chip)
C1452	21-11022G45	43pF ± 5%: 50 V
C1453 thru 1464	21-11032B13	0.10 ± 80-20%: 50 V (chip)
C1465, C1466	21-11022G45	43 pF ± 5%: 50 V
C1467	21-11031A22	20 pF ± 5%: 50 V (chip) (note 3)
CR1401	48-83654H01	diode: (see note)
CR1402	48-11034D01	silicon
CR1403	48-84616A09	silicon (note 3)
CR1405	48-84616A09	Hot carrier
CR1406 thru 1409	48-11034D01	Hot carrier
CR1410, 1411	48-84616A09	silicon
CR1412	48-11034D01	silicon (note 3)
DS1401	48-88245C28	light emitting, diode: (see note)
DS1402 thru 1404	48-88245C29	Red
HY1401	TRN4372A	Green
J1401	9-83112N01	hybrid:
J1402	28-83136N05	Digital to Analog, LPF
JU1401A	28-84729L02	connector, plug:
JU1401	9-84728L01	female: 6-contact
JU1403, 1404	06-11009B23	male: 34-contact
Q1401	48-869528	jumper:
Q1402	48-869648	3 Contact Jumper Male PCB
Q1403	48-869528	female: 2-contact
Q1404	48-869919	0 OHM Resistor
Q1405	48-869528	transistor: (see note)
		NPN: type M9528
		NPN: type M9648
		NPN: type M9528
		FET: type M9919
		NPN: type M9528
R1402 thru 1404	6-11024A73	resistor fixed: ± 5%: 1/8 W;
R1405	6-11024A93	unless otherwise stated
R1406	6-11009A49	10k (chip)
R1406	6-11024A49	68k (chip)
R1407	6-11024A65	1K
R1408, 1409	6-11024A63	1k (chip)
R1411	6-10621C72	4.7k (chip)
R1412	6-11024A73	3.9k (chip)
R1413	6-11024A33	6340 ± 1%: 1/4 W
R1414	6-11024A73	10k (chip)
R1415	6-11024A49	220 (chip)
R1416	6-125A23	10k (chip)
R1417	6-11024A47	1k (chip)
R1418	6-11024B04	82; 1/2 W
R1419	6-11024A53	820 (chip)
R1420	6-11024A73	180k (chip)
R1421	6-11024B01	1.5k (chip)
		10k (chip)
		130k (chip)

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R1422	6-11024A47	820 (chip)
R1423	6-11024A97	100k (chip)
R1424	6-11024A73	10k (chip)
R1425	6-11024A89	47k (chip)
R1426	6-11024A73	10k (chip)
R1427	6-10621E04	143K ± 1%: 1/4 W
R1428	6-11024A69	6.8k (chip)
R1429	6-11024A61	3.3k (chip)
R1430	6-11024A69	6.8k (chip)
R1431	6-11009B22	1MEG, 1/4 W
R1432	6-11024A25	100 (chip)
R1433	6-11024A91	56k (chip)
R1434	6-11024A61	3.3k (chip)
R1435	6-11024A91	56k (chip)
R1436	6-10621D84	90.9K ± 1%: 1/4 W
R1437	6-10621D78	78.7K ± 1%: 1/4 W
R1438	6-10621D88	100K ± 1%: 1/4 W
R1439	6-10621E04	143K ± 1%: 1/4 W
R1440	6-10621D80	82.5K ± 1%: 1/4 W
R1441	6-11024A73	10k (chip)
R1442	6-11024A63	3.9k (chip)
R1443	6-11024A69	6.8k (chip)
R1444	6-11024A49	1k (chip)
R1445	6-11024A84	30k (chip)
R1446	6-11024A63	3.9k (chip)
R1447, 1448	6-11024A73	10k (chip)
R1449, 1450	6-11024A33	220 (chip)
R1451	6-10621D80	82.5K ± 1%: 1/4 W
R1452	6-11024B18	680k (chip)
R1453	6-11024A97	100k (chip)
R1454 thru 1458	6-11024A73	10k (chip)
R1459	6-11024A88	43k (chip)
R1460	6-11024A73	10k (chip)
R1466, 1467	6-11024A73	10k (chip)
R1468	6-11024A84	30k (chip)
R1469	6-11024A17	47 (chip)
R1470	6-11024A77	15k (chip)
R1471	6-11024A10	24 (chip)
R1472, 1473	6-11024A73	10k (chip)
R1475	6-11024A49	1k (chip)
R1477	6-11024A46	750 (chip)
R1478	6-11024A29	150 (chip)
R1479	6-11024A53	1.5k (chip)
R1480	6-11024A91	56k (chip)
R1481	6-11009B22	1 MEG 1/4 W
TP1 thru 14	29-10271A15	test point:
		Terminal, pin
U1401	51-83625M66	integrated circuit (see note)
U1402	51-83627M03	8-Bit Microcomputer/Microprocessor
U1404	51-82609M77	Octal Transparent Latch
U1406	51-82609M67	Octal D-Flip-Flop with Enable
U1407	51-84371K65	Octal D-Flip-Flop/3-State output
U1408	51-83627M96	Timer
U1409	51-83627M95	Octal Bus/Line Driver
U1410	51-84561L50	Quad Tri-State Latch
U1411	51-84561L34	4-Bit Binary Up/Down Sync Counter
U1412	51-84561L03	Dual D-Flip-Flop
U1413	51-84561L36	Dual D-Flip-Flop
U1414, 1415	51-84561L11	Hex Inverter
U1416	51-84561L34	Quad 2-Input Pos OR Gate
U1418, 1419	51-84561L78	Dual Retrigger 1-Shot w/Clear
U1420	51-82609M02	Dual D-Flip-Flop
U1421	51-84561L03	Hex Inverter
U1422	51-82609M02	Dual J-K Flip-Flop
U1423	51-84371K84	Dual J-K Flip-Flop
U1424	51-82609M79	Dual 4-Input NAND Gate
U1425	51-83627M84	Quad Exclusive OR Gate
U1426	51-84561L07	Quad 2-Input NAND Gate
U1427	51-84371K74	Quad 2-Input AND Gate
U1428	51-82884L65	Comparator
U1429	51-83627M88	Triple 2-Input Analog Switch
U1430	51-83627M94	Hex TTL Level Shifter
U1431	51-84561L46	Quad 2-Input NAND Gate
U1432	51-84561L03	Quad 2-Input NOR Buffer
U1433	51-84561L06	Hex Inverter
U1434, 1435	51-84561L08	Quadruple 2-Input NOR Gate
U1436	51-83627M94	Triple 3-Input NAND Gate
U1440, 1441	51-82609M05	Quad 2-Input NAND Gate
		Quad Differential-Input Operational Amplifier

Multi-Coded Squelch Module
Parts Lists
Motorola No. PEPS-38310-A
(Sheet 5 of 6)
3/1/84-PHI

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
U1443, 1444	51-83627M96	Octal Bus/Line-Driver
U1445	51-82609M57	Octal Bus Transceivers/3-State Output
U1446	51-84944N21	2KX8 RAM
U1447	51-84561L13	Shift Register-Parallel Load 8-Bit
U1448	51-82884L65	Triple 2-Input Analog Switch
U1449	51-83548N77	Dual 64-Bit Shift Register
U1450	51-11991B08	Hex Level Shifter/Inverter
U1451	51-84561L13	Shift Register-Parallel Load 8-Bit
U1452	51-82609M68	Dual 4-Bit Decade Counter
U1453	51-83548N75	8-Bit Comparator
U1454	51-82609M61	Dual 5-Input NOR Gate
U1455	51-83627M38	Quad 2-Input Inverting Multiplexer
U1456, 1457	51-83548N76	Binary Up/Down Counter (3-state)
crystal: (see note)		
Y1401	48-82611M15	4.9068 MHz
Y1402	48-82611M22	2.4785 MHz
mechanical parts		
	9-84881F02	SOCKET, 28-contact
	14-84583B02	INSULATOR
	14-84602K01	INSULATOR
	9-84924E06	SOCKET, 24-contact

note: For PC Boards with part #84-82060N01, the 6-11009A49 part is used for R1406; The 06-11024A49 part is used for R1406 on all other boards.

TRN5181A Software Program PL-8901-A

REFERENCE NUMBER	MOTOROLA PART NO.	DESCRIPTION
U1403	51-90006C74	integrated circuit: (see note) EPROM 8k x 8
non-referenced item		
	54-84691N04	LABEL

TRN5844A Code Plug PL-8902-A

REFERENCE NUMBER	MOTOROLA PART NO.	DESCRIPTION
U1405	51-90013B01	EPROM 2048 x 8
non-referenced item		
	54-84594N03	CARD, Instructions

TRN5182A Escutcheon PL-8903-A

REFERENCE NUMBER	MOTOROLA PART NO.	DESCRIPTION
	13-84202N02	BEZEL

TRN5843A Miscellaneous Parts PL-8937-A

REFERENCE NUMBER	MOTOROLA PART NO.	DESCRIPTION
R8110	6-11009E85	33k \pm 5%: 1/4 W
U804	51-90006C24	integrated circuit: (see note) 8k x 8 EPROM

TRN5194A Station Control Code Plug PL-8938-A

REFERENCE NUMBER	MOTOROLA PART NO.	DESCRIPTION
U803	51-90002B02	integrated circuit: (see note) 4k x 8 EPROM
mechanical parts		
	42-84595N01	BIN INSTRUCTION CARD
	54-84594N01	CARD INSTRUCTIONS; 3 used
	54-84594N02	CARD INSTRUCTIONS; 3 used

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EPS-34440-B

Multi-Coded Squelch Module
Parts Lists
Motorola No. PEPS-38310-A
(Sheet 6 of 6)
 3/1/84-PHI

instruction manual revision

GENERAL

This revision outlines changes that have occurred since the printing of your instruction manual. Use this information to correct your manual.

INSTRUCTION MANUAL AFFECTED:

68P81114E60-A	Multi-Coded Squelch Module Option C369AA
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REVISION DETAILS:

The parts for the TRN5180A Multi-Coded Squelch Module has been revised as follows:

Reference Symbol	Motorola Part No.	Description	Change
C1468	23-11019A09	capacitor, fixed: 1 uF $\pm 20\%$, 50 V	Added

Please note the above change on PL-8866 on PEPS-38310 in your manual. The capacitor is connected between pin 4 of U1427 and ground. Note the appropriate changes on the schematic diagram and circuit board detail contained in PEPS-38310.

instruction manual revision

GENERAL

This revision outlines changes that have occurred since the printing of your instruction manual. Use this information to correct your manual.

INSTRUCTION MANUAL AFFECTED:

68P81114E60-A MSF 5000 Base Station Multi-Coded Squelch
Module Option C369AA and Model TLN2704A

REVISION DETAILS:

1. The TLN2704A Multi-Coded Squelch Module (MCS) has been replaced with Model QLN2917A which has an identical structure. Replace the Model Complement Chart on page 1 with the following chart. Also, change the model which appears in the title heading and the second sentence of paragraph 1.1 from TLN2704A to QLN2917A.

QLN2917A MODEL COMPLEMENT

ITEM	DESCRIPTION
TLN2420A	Multi-Coded Squelch Module (MCS)
TRN5182A	Escutcheon
TRN5843A	Miscellaneous Parts
*TRN5194A	Station Control Code Plug
*TRN5844A	MCS Code Plug

*The MCS code plug and the station control code plug are not part of the field installed MCS module and must be ordered separately.

2. Add the following note to page 3, paragraph 2 Installation (Field):

IMPORTANT

Upon installing the QLN2917A MCS module, resistors R898 and R8175 must be removed and R8110 must be present on the station control board.