FUNCTIONAL DESCRIPTION

APPLICATIONS ................................................. 68P81062E59
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RF-CONTROL CHASSIS

RF-CONTROL CHASSIS (TLN2472B, 74B, 75B) (B VERSION) .......... 68P81070E88

REMOTE CONTROL

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   LINE DRIVER (TRN5235A, 36A, 37A) ....................... 68P81062E13
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   F2 TONE CONTROL (TLN2444A, 49A, TRN5256A, 5325A) ..... 68P81062E21
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   SQUELCH, REPEATER, AND PRIVATE-LINE CONTROL
     OPTION DECODER (TRN1249A, 50A, 51A) ................ 68P81062E28
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AUDIO & SQUELCH

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R1 AUDIO & SQUELCH MODULE (TRN9688A, 69A) ................ 68P81062E57
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Spectra-TAC 4-WIRE LINE DRIVER MODULE (TRN5294A) ......... 68P81062E41
Spectra-TAC ENCODER MODULE (TRN5293A) ..................... 68P81062E42
Spectra-TAC SQUELCH GATE MODULE (TRN5331A) ............... 68P81062E43
   MSR 2000 BASE AND REPEATER STATION MULTIPLE TONE
   PL OPTIONS (C158, C261, C262, C263) ...................... 68P81112E80
   MULTIPLE PL MATRIX CONTROL MODULE (TRN5303A) .......... 68P81062E67
   MULTIPLE PL ENCODER MODULE (TRN5282A) ................ 68P81062E68
   MULTIPLE PL ENCODER MODULE (TRN5329A) ................ 68P81062E69

68P81061E40
1. GENERAL

1.1 PHYSICAL DESCRIPTION

The TRN9688A, 89A R1 Audio & Squelch Modules are plug-in modules designed for use with Motorola base and repeater stations. All components and circuitry are mounted on a sturdy circuit card with connecting terminals that mate with the backplane interconnect board of the station’s rf control chassis.

1.2 FUNCTIONAL DESCRIPTION

Either the Model TRN9688A R1 Audio & Squelch Module or Module TRN9689A with intercom circuitry (option) functions as an audio amplifier between the receiver detector output and line driver module. Either module also accepts microphone audio and PTT signals for local operation of the transmitter.

The receiver detector circuit feeds an audio signal to the R1 Audio & Squelch Module for amplification (U1A) and input to the carrier squelch circuitry and line driver module (pin 17). The line driver module returns audio to the R1 audio and squelch module (pin 18) for amplification and output to a local speaker (pin 22). The squelch circuitry operates from rf carrier, coded squelch, or a combination of carrier and coded squelch. For local operation of the station, the operator uses a handset or microphone audio for audio (J1-5) and MIC PTT (J1-6) inputs to the R1 Audio & Squelch Module. The audio is amplified (U1B) for modulation of the exciter (pin 16). The MIC PTT signal mutes the local speaker (U4B), enables intercom audio (optional) output (U4D), and produces a local PTT signal output (pin 4) for keying the transmitter. During intercom operation (optional), the NORMAL-INTERCOM switch S1 must be placed in the INTERCOM position to insure that the MIC PTT signal does not key the transmitter, via the local PTT output (pin 5). Intercom audio is routed, via the line driver module, to the remote control console. Remote control console intercom audio is routed from the line driver module to R1 Audio & Squelch Module (pin 18), as described previously.

2. DETAILED THEORY OF OPERATION

(Refer to the functional block and schematic diagrams at the end of this instruction section.)

2.1 VARIABLE GAIN AMPLIFIER CIRCUIT

The gain of U1A is adjustable by means of gain adjust R4. The gain is adjusted to provide a nominal voltage (380 mV rms) to the squelch circuit input (U101A-1). U1A also supplies receiver audio to the tone PL module and level adjust R7. The output of R7 drives the audio mute gate U4A. If the station is equipped with tone PL, JU1 is cut. When JU1 is cut, the R1 DET audio signal is routed through a PL filter, which is located on the tone PL module, and then applied to U4A.

2.2 AUDIO MUTE GATE CIRCUIT

U4A is a CMOS transmission gate. With a logic high control voltage, the gate is placed in the ON state. When in the ON state, audio mute gate U4A will supply audio to de-emphasis amplifier U3A. When the control voltage is switched to a logic low control voltage the gate is placed in the off (high impedance) state. In this condition, the audio signal is muted.

2.3 DE-EMPHASIS AMPLIFIER CIRCUIT

De-emphasis amplifier U3A amplifies the low level signal to provide the drive necessary for proper line driver operation. Feedback elements C7 and R13 also provide 6 dB per octave de-emphasis. Additional frequency response shaping is provided by the combination of C6, R12 & C9, R15.

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2.4 AUDIO AMPLIFIER CIRCUIT

Amplifier U3B provides the necessary drive to the audio power amplifier. Frequency response shaping is provided by C12 and R20. Limit adjust R18 is adjusted to limit maximum audio power output to 1 watt. Drive to the power amplifier is first routed through audio mute gate U4B and volume control R25. U4B mutes the speaker audio during a MIC PTT signal.

2.5 AUDIO POWER AMPLIFIER CIRCUIT

Volume control R25 output is coupled to the audio power amplifier U2 by C17. U2 provides 1 watt of audio power into an 8-ohm speaker, at less than 5% distortion.

2.6 MIC AUDIO AMPLIFIER CIRCUIT

During local operation, mic audio is supplied to pin 5 of mic connector J1. For local transmission, this audio is amplified by U1B to provide the necessary drive to the exciter for proper operation.

2.7 INTERCOM OPTION CIRCUITRY

When the intercom option is present (TRN9689A only), mic audio is coupled through intercom mute gate U4D to the line driver. U4C inverts mic PTT to control intercom mute gate U4D. Intercom audio is muted by U4D when there is no mic PTT signal (GND) at U4C-6.

2.8 NOISE ACTIVATED SQUELCH CIRCUIT

2.8.1 Remote Controlled Squelch Circuit

With the remote controlled squelch option, JU101 is removed and JU102 and JU103 are installed. Then the R1 disc input signal, for the squelch circuit, is first routed through a remote controlled squelch module (option). This module provides the capability of remotely adjusting the squelch opening sensitivity. The remotely adjusted squelch signal is returned to the R1 Audio & Squelch Module as the R1 SQ ATTENUATOR signal, at pin 6.

2.8.2 Squelch Input Circuitry

The input to first amplifier/limiter U101A is a pre-emphasis network. This circuit boosts the noise content of the input signals above 5 kHz, for squelch processing the first amplifier/limiter is driven into limit to prevent audio signals from squelching the receiver. The amplified and limited noise signal is sent through a frequency shaping network to squelch control R25.

The squelch control wiper provides signal to second amplifier/limiter U101B. U101B amplifies the noise signal and relimits audio signals to provide further protection against audio signals squelching the receiver. The output signal of U101B is frequency shaped and sent to noise detector U101C.

2.8.3 Noise Detector and Switching Circuits

Noise detector U101C is a half wave rectifier-amplifier which produces negative going spikes at its output, U101C-12. The average dc value of these spikes is a function of received signal strength. The lowest average dc output voltage corresponds to a no signal input (maximum noise) condition. As the received signal strength increases, the noise level decreases, and the average dc output voltage increases.

The squelch switching circuitry operates in two modes. With a receive signal just above the opening sensitivity, squelch closing is slow (approximately 150 ms), which produces the squelch tail heard at the end of a received message. The 150 ms delay is present to prevent the received message from being chopped during a weak fluttering signal. With a strong signal (approximately 10 dB above opening sensitivity), squelch closing occurs immediately after the end of a received signal. This prevents the squelch tail from being heard.

Active integrator U101D provides squelch opening and slow squelch closing. U101D compares the detector’s average dc output voltage with a reference voltage to determine squelch opening and closing.

Fast squelch closing is provided by Q102. A strong signal charges C116 through R120, turning Q102 on. With Q102 on, the collector voltage lowers to approximately 3.9 V dc. At the end of a strong signal, noise spikes from the detector are captured by CR103. This immediately discharges C116, turning off Q102. When Q102 turns off, its collector voltage goes to 9.4 volts, and C118 forces Q103 to close the squelch.

2.9 SQUELCH LOGIC CIRCUITRY

The squelch logic circuitry performs the necessary switching functions to provide proper squelch operation. This circuitry can operate in one of three different modes by selecting proper jumper cuts. Refer to the jumper table on the schematic diagram. For noise activated squelch operation only, JU105 is cut. In this mode, Q107 is always turned on. Squelching is controlled by the squelch noise circuit, through Q104. For coded (PL or DPL) squelch activation, both JU104 and JU105 remain in. In this mode, squelch turn-on is controlled by a proper coded squelch detection only. A proper coded squelch detection pulls the PL indicate line high, turning on Q105 and Q107. When PL DISABLED in this configuration, Q107 is turned on. This allows either a proper coded squelch detection or a noise activated squelch detection to open the squelch. This provides the OR squelch function.

In the third mode of operation, JU104 is cut and JU105 remains in. This produces the AND squelch function. AND squelch means that both a proper coded squelch
detection and a noise activated squelch detection are required to open squelch. A proper coded squelch detection turns on Q107 and a noise activated squelch detection turns on Q104. Both are required to open squelch. When PL DISABLED in this configuration, both Q106 and Q107 are turned on. Again, this provides the OR squelch function, where either a proper coded squelch detection or a noise activated squelch detection will open squelch. With Q107 on, and either Q104 or Q105 on, Q108 and Q109 are turned off. This enables audio mute gate U4A, creating an open squelch condition.
R1 AUDIO & SQUELCH MODELS
MODELS TRN5068A, 69A

Model Table

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRN5068A</td>
<td>Standard</td>
</tr>
<tr>
<td>TRN5069A</td>
<td>Standard with Intercom</td>
</tr>
</tbody>
</table>

1. GENERAL

1.1 PHYSICAL DESCRIPTION

The TRN5068A, 69A R1 Audio & Squelch Modules are plug-in modules designed for use with Motorola base and repeater stations. All components and circuitry are mounted on a sturdy circuit card with connecting terminals that mate with the backplane interconnect board of the station’s rf control chassis.

1.2 FUNCTIONAL DESCRIPTION

Either the Model TRN5068A R1 Audio & Squelch Module or Module TRN5069A with intercom circuitry (option) functions as an audio amplifier between the receiver detector output and line driver module. Either module also accepts microphone audio and PTT signals for local operation of the transmitter.

The receiver detector circuit feeds an audio signal to the R1 Audio & Squelch Module for amplification (U1A) and input to the carrier squelch circuitry and line driver module (pin 17). The line driver module returns audio to the R1 audio and squelch module (pin 18) for amplification and output to a local speaker (pin 22). The squelch circuitry operates from rf carrier, coded squelch, or a combination of carrier and coded squelch. For local operation of the station, the operator uses a handset or microphone for audio (J1-5) and MIC PTT (J1-6) inputs to the R1 Audio & Squelch Module. The audio is amplified (U1B) for modulation of the exciter (pin 16). The MIC PTT signal mutes the local speaker (U4B), enables intercom audio (optional) output (U4D), and produces a local PTT signal output (pin 4) for keying the transmitter. During intercom operation (optional), the NORMAL-INTERCOM switch S1 must be placed in the INTERCOM position to insure that the MIC PTT signal does not key the transmitter, via the local PTT output (pin 5). Intercom audio is routed, via the line driver module, to the remote control console. Remote control console intercom audio is routed from the line driver module to R1 Audio & Squelch Module (pin 18), as described previously.

2. DETAILED THEORY OF OPERATION
(Refer to the functional block and schematic diagrams attached to this instruction section.)

2.1 VARIABLE GAIN AMPLIFIER CIRCUIT

The gain of U1A is adjustable by means of gain adjust R4. The gain is adjusted to provide a nominal voltage (380 mV rms) to the squelch circuit input (U101A-1). U1A also supplies receiver audio to the tone PL module and level adjust R7. The output of R7 drives the audio mute gate U4A. If the station is equipped with tone PL, JU1 is cut. When JU1 is cut, the R1 DET audio signal is routed through a PL filter, which is located on the tone PL module, and then applied to U4A.

2.2 AUDIO MUTE GATE CIRCUIT

U4A is a CMOS transmission gate. With a logic high control voltage, the gate is placed in the ON state. When in the ON state, audio mute gate U4A will supply audio to de-emphasis amplifier U3A. When the control voltage is switched to a logic low control voltage the gate is placed in the off (high impedance) state. In this condition, the audio signal is muted.

2.3 DE-EMPHASIS AMPLIFIER CIRCUIT

De-emphasis amplifier U3A amplifies the low level signal to provide the drive necessary for proper line driver operation. Feedback elements C7 and R13 also provide 6 dB per octave de-emphasis. Additional frequency response shaping is provided by the combination of C6, R12 & C9, R15.
2.4 AUDIO AMPLIFIER CIRCUIT

Amplifier U3B provides the necessary drive to the audio power amplifier. Frequency response shaping is provided by C12 and R20. Limit adjust R18 is adjusted to limit maximum audio power output to 1 watt. Drive to the power amplifier is first routed through audio mute gate U4B and volume control R25. U4B mutes the speaker audio during a MIC PTT signal.

2.5 AUDIO POWER AMPLIFIER CIRCUIT

Volume control R25 output is coupled to the audio power amplifier U2 by C17. U2 provides 1 watt of audio power into an 8-ohm speaker, at less than 5% distortion.

2.6 MIC AUDIO AMPLIFIER CIRCUIT

During local operation, mic audio is supplied to pin 5 of mic connector J1. For local transmission, this audio is amplified by U1B to provide the necessary drive to the exciter for proper operation.

2.7 INTERCOM OPTION CIRCUITY

When the intercom option is present (TRN5069A only), mic audio is coupled through intercom mute gate U4D to the line driver. U4C inverts mic PTT to control intercom mute gate U4D. Intercom audio is muted by U4D when there is no mic PTT signal (GND) at U4C-6.

2.8 NOISE ACTIVATED SQUELCH CIRCUIT

2.8.1 Remote Controlled Squelch Circuit

With the remote controlled squelch option, JU101 is removed and JU102 and JU103 are installed. Then the R1 disc input signal, for the squelch circuit, is first routed through a remote controlled squelch module (option). This module provides the capability of remotely adjusting the squelch opening sensitivity. The remotely adjusted squelch signal is returned to the R1 Audio & Squelch Module as the R1 SQ ATTENUATOR signal, at pin 6.

2.8.2 Squelch Input Circuitry

The input to first amplifier/limiter U101A is a pre-emphasis network. This circuit boosts the noise content of the input signals above 5 kHz, for squelch processing the first amplifier/limiter is driven into limit to prevent audio signals from squelching the receiver. The amplified and limited noise signal is sent through a frequency shaping network to squelch control R25.

The squelch control wiper provides signal to second amplifier/limiter U101B. U101B amplifies the noise signal and relimits audio signals to provide further protection against audio signals squelching the receiver. The output signal of U101B is frequency shaped and sent to noise detector U101C.

2.8.3 Noise Detector and Switching Circuits

Noise detector U101C is a half wave rectifier-amplifier which produces negative going spikes at its output, U101C-12. The average dc value of these spikes is a function of received signal strength. The lowest average dc output voltage corresponds to a no signal input (maximum noise) condition. As the received signal strength increases, the noise level decreases, and the average dc output voltage increases.

The squelch switching circuitry operates in two modes. With a receive signal just above the opening sensitivity, squelch closing is slow (approximately 150 ms), which produces the squelch tail heard at the end of a received message. The 150 ms delay is present to prevent the received message from being chopped during a weak fluttering signal. With a strong signal (approximately 10 dB above opening sensitivity), squelch closing occurs immediately after the end of a received signal. This prevents the squelch tail from being heard.

Active integrator U101D provides squelch opening and slow squelch closing. U101D compares the detector's average dc output voltage with a reference voltage to determine squelch opening and closing.

Fast squelch closing is provided by Q102. A strong signal charges C116 through R120, turning Q102 on. With Q102 on, the collector voltage lowers to approximately 3.9 V dc. At the end of a strong signal, noise spikes from the detector are captured by CR103. This immediately discharges C116, turning off Q102. When Q102 turns off, its collector voltage goes to 9.4 volts, and C118 forces Q103 to close the squelch.

2.9 SQUELCH LOGIC CIRCUITRY

The squelch logic circuitry performs the necessary switching functions to provide proper squelch operation. This circuitry can operate in one of three different modes by selecting proper jumper cuts. Refer to the jumper table on the schematic diagram. For noise activated squelch operation only, JU105 is cut. In this mode, Q107 is always turned on. Squelching is controlled by the squelch noise circuit, through Q104. For coded (PL or DPL) squelch activation, both JU104 and JU105 remain in. In this mode, squelch turn-on is controlled by a proper coded squelch detection only. A proper coded squelch detection pulls the PL indicate line high, turning on Q105 and Q107. When PL DISABLED in this configuration, Q107 is turned on. This allows either a proper coded squelch detection or a noise activated squelch detection to open the squelch. This provides the OR squelch function.

In the third mode of operation, JU104 is cut and JU105 remains in. This produces the AND squelch function. AND squelch means that both a proper coded squelch
detection and a noise activated squelch detection are required to open squelch. A proper coded squelch detection turns on Q107 and a noise activated squelch detection turns on Q104. Both are required to open squelch. When PL DISABLED in this configuration, both Q106 and Q107 are turned on. Again, this provides the OR squelch function, where either a proper coded squelch detection or a noise activated squelch detection will open squelch. With Q107 on, and either Q104 or Q105 on, Q108 and Q109 are turned off. This enables audio mute gate U4A, creating an open squelch condition.
### Parts List

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<tr>
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<tr>
<td>C1</td>
<td>Capacitor</td>
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<tr>
<td>L1</td>
<td>Inductor</td>
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<tr>
<td>D1</td>
<td>Diode</td>
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</tr>
<tr>
<td>U1</td>
<td>IC</td>
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</tbody>
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**Notes:**
- All parts are from the manufacturer's catalog.
- Refer to the latest version for any updates.
- Safety precautions should be followed when handling components.

**Diagram:**
- The diagram shows the layout of the circuit components.
- Soldering connections are indicated with solid lines.
- Power sources and ground connections are marked with dashed lines.

**Additional Information:**
- This document is for reference only and should not be used for commercial purposes without proper authorization.
### Model Table

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tr>
<td>TRN9690A</td>
<td>With Carrier Squelch</td>
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<tr>
<td>TRN9691A</td>
<td>With Carrier &amp; PL Squelch</td>
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<tr>
<td>TRN9692A</td>
<td>With Carrier &amp; DPL Squelch</td>
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</table>

### 1. GENERAL

#### 1.1 PHYSICAL DESCRIPTION

The TRN9690A, 91A, and 92A R2 Audio & Squelch Modules are plug-in modules designed for use with Motorola base and repeater stations. All components and circuitry are mounted on a sturdy circuit card with connecting terminals that mate with the backplane interconnect board of the station's RF Control Chassis. These modules are used only with two receiver stations.

#### 1.2 FUNCTIONAL DESCRIPTION

Each of these modules function as an audio amplifier between the second receiver's detector output and the line driver module. They also can perform a carrier squelch function for the second receiver. Additionally, Model TRN9691A can perform a PL squelch function, and Model TRN9692A can perform a DPL squelch function.

The second receiver detector circuit feeds an audio signal to the R2 Audio & Squelch Module for amplification (U1), input to the carrier squelch circuitry, and output to the line driver module (pin 17). The line driver module returns audio to the R1 audio & squelch module (pin 18) for amplification and output to a local speaker (pin 22). The on-board squelch circuitry operates from rf carrier, coded squelch, or a combination of carrier and coded squelch.

### 2. DETAILED THEORY OF OPERATION

(Refer to the functional block and schematic diagrams at the end of this instruction section.)

#### 2.1 VARIABLE GAIN AMPLIFIER CIRCUIT

The gain of U1 is adjustable by means of gain adjust R3. The gain is adjusted to provide a nominal voltage (380 mV rms) to the squelch circuit input (U101A-1). U1 also supplies receiver audio to possible on-board PL or DPL circuitry, and level adjust R7. The output of R7 drives audio mute gate Q1. If the station is equipped with tone PL, JU1 is cut. When JU1 is cut, the R2 DET Audio signal is routed through an on-board PL filter, and then applied to Q1.

#### 2.2 AUDIO MUTE GATE CIRCUIT

Q1 is a P-Channel Field Effect Transistor (FET). With a logic low control voltage, the FET is placed in the ON state. When in the ON state, audio mute gate Q1 will supply audio to de-emphasis amplifier U2. When the control voltage is switched to a logic high, the gate is placed in the OFF (high impedance) state. In this condition, the audio signal is muted.

#### 2.3 DE-EMPHASIS AMPLIFIER CIRCUIT

De-emphasis amplifier U2 amplifies the low level signal to provide the drive necessary for proper line driver operation. Feedback elements C9 and R12 also provide 6 dB per octave de-emphasis. Additional frequency response shaping is provided by the combination of C8 and R11, and R14 (on TRN9690A, 91A), or C8 and R11, and C10 and R14 (on TRN9692A).

#### 2.4 NOISE ACTIVATED (CARRIER) SQUELCH CIRCUIT

##### 2.4.1 Squelch Input Circuity

The input to first amplifier/limiter U101A is a preemphasis network. This circuit boosts the noise content of the input signals above 5 kHz, for squelch processing with the first amplifier/limiter is driven into limit to prevent audio signals from squelching the receiver. The amplified and limited noise signal is sent through a frequency shaping network to SQUELCH control R105.

The squelch control wiper provides signal to second amplifier/limiter U101B. U101B amplifies the noise signal and relimits audio signals to provide further protection against audio signals squelching the receiver.

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output signal of U101B is frequency shaped and sent to noise detector U101C.

2.4.2 Noise Detector and Switching Circuits

Noise detector U101C is a half wave rectifieramplifier which produces negative going spikes at its output, U101C-10. The average dc value of these spikes is a function of received signal strength. The lowest average dc output voltage corresponds to a no signal input (maximum noise) condition. As the received signal strength increases, the noise level decreases, and the average dc output voltage increases.

The squelch switching circuitry operates in two modes. With a receive signal just above the opening sensitivity, squelch closing is slow (approximately 150 ms), which produces the squelch tail heard at the end of a received message. The 150 ms delay is present to prevent the received message from being chopped during a weak fluttering signal. With a strong signal (approximately 10 dB above opening sensitivity), squelch closing occurs immediately after the end of a received signal. This prevents the squelch tail from being heard.

Active integrator U101D provides squelch opening and slow squelch closing. U101D compares the detector's average dc output voltage with a reference voltage to determine squelch opening and closing.

Fast squelch closing is provided by Q102. A strong signal charges C112 through R120, turning Q102 on. With Q102 on, the collector voltage lowers to approximately 3.9 V dc. At the end of a strong signal, noise spikes from the detector are captured by CR104. This immediately discharges C112, turning Q102 off. When Q102 turns off, its collector voltage goes to 9.4 volts, and C114 forces Q103 to close the squelch.

2.5 PRIVATE-LINE TONE CODED SQUELCH CIRCUIT

2.5.1 General

Essentially, the on-board PL decoder circuit of Model TRN9691A R2 Audio & Squelch Module detects a received PL tone and unsculches the receiver when the proper PL tone is received. In addition, PL tone filtering is provided so that the PL tone is not heard in normal received audio.

Received R2 audio enters the PL circuit as R2 DISC INPUT (from U1-6), and is routed through an active low pass filter (Q201 and 202) before being applied to the input of the tone decoder IC U201-8. When the proper PL tone is decoded, U201 produces a square wave at the decode output (U201-13), unloaded. The square wave is detected by detector switch circuitry (Q204 and 205), which then enables PL INDICATOR output switch (Q206).

PL filter circuitry is utilized (JU1 out) to remove (attenuate) PL tones from the received audio. The received audio is filtered, first by a high pass filter, and then by a notch filter. A gyrator circuit is used for the notch filter to provide high "Q" inductance, without employing inductors.

2.5.2 PL Decoder Circuit Description

NOTE
The decoder IC U201 generates a high PL INDICATOR output (on the collector of Q206) when a proper PL tone is detected.

2.5.2.1 LOW PASS FILTER

The 5-pole low pass filter (Q201 and 202) attenuates high frequency noise above 192.8 Hz from the received R2 DISC INPUT audio. This provides the balance of the decoder circuitry additional taising and blocking immunity.

2.5.2.2 DECODER AND REED

The filtered PL tone is applied to the decoder tone input (U201-8), where it is amplified and limited. The PL tone is then fed to the decoding reed Z201, pins 2 and 3. If the PL tone is of the proper frequency, it will cause the reed to resonate. The reed secondary (pins 1 and 4) reacts to the sympathetic vibration and returns the PL tone to the decoder reed secondary input U201-11. The decoder then amplifies and limits the PL tone once again, and provides an output at U201-13, Decode Output.

NOTE
If no proper PL tone is detected, the output of U1-13 stays high.

2.5.2.3 DETECTOR SWITCH

When an output is present (indicating a proper PL tone detection) at the decode output of U201 (pin 13), it is waveshaped by capacitor C212 into a sawtooth waveform at a level of approximately 0.8 V p-p. If a high (no detect) is present at U201-13, the level of this same waveform is constant, approximately 2.2 V. The balance of the detector switch circuitry inverts, filters, and amplifies the sawtooth waveform to produce a true logic level (logic high) at the collector of Q206 (PL INDICATOR).

2.5.2.4 NOISE GATE

Noise Gate Q203 allows a small amount of high frequency noise (with 1-pole of low pass filtering) to be fed to the decoder input, U201-8 when the PL INDICATOR output at the collector of Q206 is low. This tends to minimize noise falsing of the decoder. When the PL INDICATOR output is high, the high frequency noise sam-
ple is shunted to ground. This allows the onboard PL circuit to be more sensitive, once it receives a signal, and helps to prevent decoder dropout during brief signal fades.

2.5.2.5 8.4 V REGULATOR

The Q207 regulator circuit provides a constant 8.4 V dc (E+) to the PL decoder IC, U201.

2.6 DIGITAL PRIVATE-LINE CODED SQUELCH CIRCUIT

2.6.1 General

Essentially, the on-board DPL decoder circuit of Model TRN9692A R2 Audio & Squelch Module detects a received DPL code, and unmutes the receiver when the proper code is received. Received R2 audio enters the DPL circuit as R2 DISC INPUT (from U1-6), and is routed through an active low pass filter (Q301 and 302), where frequencies above the DPL code range are attenuated. The output of the low pass filter is applied to phase-lock-loop (PLL) data conditioner U302, which squares the shape of the incoming code word. The output of the data conditioner is routed, via level shifter Q303, to the input of the decoder IC U301-11.

The decoder circuit consists of IC U301, a 50 kHz clock (Y301 and Q304), and the information stored in the code plug (J301). When the proper code has been detected, the decoder provides a logic high at U301-7. That high provides a logic low, via audio enable Q305, to enable the PL INDICATOR output switch (Q306).

The logic high at U301-7 is also applied to sensitivity switch U304C, to disable the constant current source of U304D-U304E. With the constant current source disabled, the voltage at U302-8 is lowered, causing the sensitivity of U302 to increase. This provides additional immunity to audio interference and improved squaring of the incoming code word.

When the incoming (received) signal ceases, the sending transmitter produces a turn-off code. When the turn-off code is detected by the decoder, the detected output at U301-7 switches low. This decreases the sensitivity of the data conditioner and causes receiver audio to be muted.

2.6.2 DPL Decoder Circuit Description

NOTE

The decoder IC U301 generates a high (PL INDICATOR) output on the collector of Q206 when a proper DPL code is detected.

2.6.2.1 LOW PASS FILTER

The low pass filter circuit is similar to the one previously described for the PL decoder circuit in this section. However, the filter's output is fed through a PLL data conditioner (U302) for waveshaping, and a level shifter (Q303) to properly process the incoming code word, before presenting it to the decoder (U301) circuitry.

2.6.2.2 DECODER AND CODE PLUG

The processed code word is applied to the decoder's data input (U301-11), where it is compared to the data stored in the code plug (J301), at a 50 kHz rate. If the incoming code word is correct, U301 will provide a logic high at the decoder's detected output U301-7.

NOTE

If no proper code word is detected, the output of U301-7 stays low.

2.6.2.3 AUDIO ENABLE

When a high output is present at U301-7 (indicating a proper DPL code detection), it is inverted by Q305 to enable Q306. Output switch Q306 then produces a true logic level (logic high) at its collector (PL INDICATOR).

2.6.2.4 REGULATOR CIRCUIT

Regulator Q307 provides three regulated dc voltages from station A+ (13.9 V). These voltages, in addition to A-, power all circuitry in the DPL decoder section of the module. The regulated voltages are:

- 10.5 V (C+), 6.2 V (D+), and 11.1 V (E+).

2.7 AND-OR SQUELCH LOGIC CIRCUITRY

The squelch logic circuitry performs the necessary switching functions to provide proper squelch operation. This circuitry can operate in one of three different modes by selecting proper jumper cuts. Refer to the jumper table on the schematic diagram. First, for noise activated squelch operation only, JU102 is cut. In this mode, Q107 is always turned on. Squelching is controlled by the squelch noise circuit, through Q104. For coded (PL or DPL) squelch activation, both JU101 and JU102 remain in. In this mode, squelch turn-on is controlled by a proper coded squelch detection only. A proper coded squelch detection pulls the PL INDICATOR line high, turning on Q105 and Q107. Second, when PL DISABLED in this configuration, Q107 is turned on. This allows either a proper coded squelch detection or a noise activated squelch detection to open the squelch. This provides the OR squelch function.

In the third mode of operation, JU101 is cut and JU102 remains in. This produces the AND squelch function.
AND squelch means that both a proper coded squelch detection and a noise activated squelch detection are required to open squelch. A proper coded squelch detection turns on Q107 and a noise activated squelch detection turns on Q104. Both are required to open squelch. When PL DISABLED in this configuration both Q106 and Q107 are turned on. Again, this provides the OR squelch function, where either a proper coded squelch detection or a noise activated squelch detection will open squelch.

With Q107 on, and either Q104 or Q105 on, Q108 and Q109 are turned off. This enables audio mute gate Q1, creating an open squelch condition.
1. GENERAL

1.1 PHYSICAL DESCRIPTION

The TRN5070A, 71A, and 72A R2 Audio & Squelch Modules are plug-in modules designed for use with Motorola base and repeater stations. All components and circuitry are mounted on a sturdy circuit card with connecting terminals that mate with the backplane interconnect board of the station's RF Control Chassis. These modules are used only with two receiver stations.

1.2 FUNCTIONAL DESCRIPTION

Each of these modules function as an audio amplifier between the second receiver's detector output and the line driver module. They also can perform a carrier squelch function for the second receiver. Additionally, Model TRN5071A can perform a PL squelch function, and Model TRN5072A can perform a DPL squelch function.

The second receiver detector circuit feeds an audio signal to the R2 Audio & Squelch Module for amplification (U1), input to the carrier squelch circuitry, and output to the line driver module (pin 17). The line driver module returns audio to the R1 audio & squelch module (pin 18) for amplification and output to a local speaker (pin 22). The on-board squelch circuitry operates from rf carrier, coded squelch, or a combination of carrier and coded squelch.

2. DETAILED THEORY OF OPERATION

(Refer to the functional block and schematic diagrams attached to this instruction section.)

2.1 VARIABLE GAIN AMPLIFIER CIRCUIT

The gain of U1 is adjustable by means of gain adjust R3. The gain is adjusted to provide a nominal voltage (380 mV rms) to the squelch circuit input (U101A-1). U1 also supplies receiver audio to possible on-board PL or DPL circuitry, and level adjust R7. The output of R7 drives audio mute gate Q1. If the station is equipped with tone PL, JU1 is cut. When JU1 is cut, the R2 DET AUDIO signal is routed through an on-board PL filter, and then applied to Q1.

2.2 AUDIO MUTE GATE CIRCUIT

Q1 is a P-Channel Field Effect Transistor (FET). With a logic low control voltage, the FET is placed in the ON state. When in the ON state, audio mute gate Q1 will supply audio to de-emphasis amplifier U2. When the control voltage is switched to a logic high, the gate is placed in the OFF (high impedance) state. In this condition, the audio signal is muted.

2.3 DE-EMPHASIS AMPLIFIER CIRCUIT

De-emphasis amplifier U2 amplifies the low level signal to provide the drive necessary for proper line driver operation. Feedback elements C9 and R12 also provide 6 dB per octave de-emphasis. Additional frequency response shaping is provided by the combination of C8 & R11, and R14 (on TRN5070A, 71A), or C8 & R11, and C10 & R14 (on TRN5072A).

2.4 NOISE ACTIVATED (CARRIER) SQUELCH CIRCUIT

2.4.1 Squelch Input Circuitry

The input to first amplifier/limiter U101A is a pre-emphasis network. This circuit boosts the noise content of the input signals above 5 kHz, for squelch processing the first amplifier/limiter is driven into limit to prevent audio signals from squelching the receiver. The amplified and limited noise signal is sent through a frequency shaping network to SQUELCH control R105.

The squelch control wiper provides signal to second amplifier/limiter U101B. U101B amplifies the noise signal and relimits audio signals to provide further protection against audio signals squelching the receiver. The
output signal of U101B is frequency shaped and sent to noise detector U101C.

2.4.2 Noise Detector and Switching Circuits

Noise detector U101C is a half wave rectifier-amplifier which produces negative going spikes at its output, U101C-10. The average dc value of these spikes is a function of received signal strength. The lowest average dc output voltage corresponds to a no signal input (maximum noise) condition. As the received signal strength increases, the noise level decreases, and the average dc output voltage increases.

The squelch switching circuitry operates in two modes. With a receive signal just above the opening sensitivity, squelch closing is slow (approximately 150 ms), which produces the squelch tail heard at the end of a received message. The 150 ms delay is present to prevent the received message from being chopped during a weak fluttering signal. With a strong signal (approximately 10 dB above opening sensitivity), squelch closing occurs immediately after the end of a received signal. This prevents the squelch tail from being heard.

Active integrator U101D provides squelch opening and slow squelch closing. U101D compares the detector's average dc output voltage with a reference voltage to determine squelch opening and closing.

Fast squelch closing is provided by Q102. A strong signal charges C112 through R120, turning Q102 on. With Q102 on, the collector voltage lowers to approximately 3.9 V dc. At the end of a strong signal, noise spikes from the detector are captured by CR104. This immediately discharges C112, turning off Q102. When Q102 turns off, its collector voltage goes to 9.4 volts, and C114 forces Q103 to close the squelch.

2.5 PRIVATE-LINE TONE CODED SQUELCH CIRCUIT

2.5.1 General

Essentially, the on-board PL decoder circuit of Model TRN5071A R2 Audio & Squelch Module detects a received PL tone and unsexleshes the receiver when the proper PL tone is received. In addition, PL tone filtering is provided so that the PL tone is not heard in normal received audio.

Received R2 audio enters the PL circuit as R2 DISC INPUT (from U1-6), and is routed through an active low pass filter (Q201 & 202) before being applied to the input of the tone decoder IC U201-8. When the proper PL tone is decoded, U201 produces a square wave at the decode output (U201-13), unloaded. The square wave is detected by detector switch circuitry (Q204 & 205), which then enables PL INDICATOR output switch (Q206).

PL filter circuitry is utilized (JU1 out) to remove (attenuate) PL tones from the received audio. The received audio is filtered, first by a high pass filter, and then by a notch filter. A gyrator circuit is used for the notch filter to provide high “Q” inductance, without employing inductors.

2.5.2 PL Decoder Circuit Description

NOTE
The decoder IC U201 generates a high PL INDICATOR output (on the collector of Q206) when a proper PL tone is detected.

2.5.2.1 LOW PASS FILTER

The 5-pole low pass filter (Q201 & 202) attenuates high frequency noise above 192.8 Hz from the received R2 DISC INPUT audio. This provides the balance of the decoder circuitry additional fading and blocking immunity.

2.5.2.2 DECODER AND REED

The filtered PL tone is applied to the decoder tone input (U201-8), where it is amplified and limited. The PL tone is then fed to the decoding reed Z201, pins 2 and 3. If the PL tone is of the proper frequency, it will cause the reed to resonate. The reed secondary (pins 1 and 4) reacts to the sympathetic vibration and returns the PL tone to the decoder reed secondary input U201-11. The decoder then amplifies and limits the PL tone once again, and provides an output at U201-13, Decode Output.

NOTE
If no proper PL tone is detected, the output of U1-13 stays high.

2.5.2.3 DETECTOR SWITCH

When an output is present (indicating a proper PL tone detection) at the decode output of U201 (pin 13), it is wave shaped by capacitor C212 into a sawtooth waveform at a level of approximately 0.8 V p-p. If a high (no detect) is present at U201-13, the level of this same waveform is constant, approximately 2.2 V. The balance of the decoder switch circuitry inverts, filters, and amplifies the sawtooth waveform to produce a true logic level (logic high) at the collector of Q206 (PL INDICATOR).

2.5.2.4 NOISE GATE

Noise Gate Q203 allows a small amount of high frequency noise (with 1-pole of low pass filtering) to be fed to the decoder input, U201-8 when the PL INDICATOR output at the collector of Q206 is low. This tends to minimize noise falsing of the decoder. When the PL INDICATOR output is high, the high frequency noise sam-
ple is shunted to ground. This allows the onboard PL circuit to be more sensitive, once it receives a signal, and helps to prevent decoder dropout during brief signal fades.

2.5.2.5 8.4 V REGULATOR

The Q207 regulator circuit provides a constant 8.4 V dc (E+) to the PL decoder IC, U201.

2.6 DIGITAL PRIVATE-LINE CODED SQUELCH CIRCUIT

2.6.1 General

Essentially, the on-board DPL decoder circuit of Model TRN5072A R2 Audio & Squelch Module detects a received DPL code, and unmutes the receiver when the proper code is received. Received R2 audio enters the DPL circuit as R2 DISC INPUT (from U1-6), and is routed through an active low pass filter (Q301 & 302), where frequencies above the DPL code range are attenuated. The output of the low pass filter is applied to phase-lock-loop (PLL) data conditioner U302, which squares the shape of the incoming code word. The output of the data conditioner is routed, via level shifter Q303, to the input of the decoder IC U301-11.

The decoder circuit consists of IC U301, a 50 kHz clock (Y301 & Q304), and the information stored in the code plug (J301). When the proper code has been detected, the decoder provides a logic high at U301-7. That high provides a logic low, via audio enable Q305, to enable the PL INDICATOR output switch (Q306).

The logic high at U301-7 is also applied to sensitivity switch U304C, to disable the constant current source of U304D-U304E. With the constant current source disabled, the voltage at U302-8 is lowered, causing the sensitivity of U302 to increase. This provides additional immunity to audio interference and improved squaring of the incoming code word.

When the incoming (received) signal ceases, the sending transmitter produces a turn-off code. When the turn-off code is detected by the decoder, the detected output at U301-7 switches low. This decreases the sensitivity of the data conditioner and causes receiver audio to be muted.

2.6.2 DPL Decoder Circuit Description

NOTE

The decoder IC U301 generates a high (PL INDICATOR) output on the collector of Q206 when a proper DPL code is detected.

2.6.2.1 LOW PASS FILTER

The low pass filter circuit is similar to the one previously described for the PL decoder circuit in this section. However, the filter's output is fed through a PLL data conditioner (U302) for waveshaping, and a level shifter (Q303) to properly process the incoming code word, before presenting it to the decoder (U301) circuitry.

2.6.2.2 DECODER AND CODE PLUG

The processed code word is applied to the decoder's data input (U301-11), where it is compared to the data stored in the code plug (J301), at a 50 kHz rate. If the incoming code word is correct, U301 will provide a logic high at the decoder's detected output U301-7.

NOTE

If no proper code word is detected, the output of U301-7 stays low.

2.6.2.3 AUDIO ENABLE

When a high output is present at U301-7 (indicating a proper DPL code detection), it is inverted by Q305 to enable Q306. Output switch Q306 then produces a true logic level (logic high) at its collector (PL INDICATOR).

2.6.2.4 REGULATOR CIRCUIT

Regulator Q307 provides three regulated dc voltages from station A+ (13.9 V). These voltages, in addition to A+, power all circuitry in the DPL decoder section of the module. The regulated voltages are:

10.5 V (C+), 6.2 V (D+), and 11.1 V (E+).

2.7 AND-OR SQUELCH LOGIC CIRCUITRY

The squelch logic circuitry performs the necessary switching functions to provide proper squelch operation. This circuitry can operate in one of three different modes by selecting proper jumper cuts. Refer to the jumper table on the schematic diagram. First, for noise activated squelch operation only, JU102 is cut. In this mode, Q107 is always turned on. Squelching is controlled by the squelch noise circuit, through Q104. For coded (PL or DPL) sqeuich activation, both JU101 and JU102 remain in. In this mode, squelch turn-on is controlled by a proper coded squelch detection only. A proper coded squelch detection pulls the PL INDICATOR line high, turning on Q105 and Q107. Second, when PL DISABLED in this configuration, Q107 is turned off. This allows either a proper coded sqeuich detection or a noise activated squelch detection to open the squelch. This provides the OR squelch function.

In the third mode of operation, JU101 is cut and JU102 remains in. This produces the AND squelch function.
AND squelch means that both a proper coded squelch detection and a noise activated squelch detection are required to open squelch. A proper coded squelch detection turns on Q107 and a noise activated squelch detection turns on Q104. Both are required to open squelch. When PL DISABLED in this configuration both Q106 and Q107 are turned on. Again, this provides the OR squelch function, where either a proper coded squelch detection or a noise activated squelch detection will open squelch.

With Q107 on, and either Q104 or Q105 on, Q108 and Q109 are turned off. This enables audio mute gate Q1, creating an open squelch condition.
1. DESCRIPTION

The TRN5073A/74A/75A Tone Private-Line (PL) Encoder-Decoder Modules are plug-in modules designed for use with Motorola base and repeater stations. All components and circuitry are mounted on a sturdy circuit card with connecting terminals that mate with the backplane interconnect board of the station's rf control chassis. These modules are used with the following types of stations: Simplex TARA and TARb and Duplex TARA.

NOTE

TARA means that the PL encoder-decoder module employs the same PL code (one reed used) for transmit and receive. TARb means that the PL encoder-decoder module employs a different PL code for transmit and receive (two reeds used).

2. FUNCTIONS

Each of these modules encodes and decodes Private-Line tones. The encoder modulates the transmitter and delays transmitter turn-off 180 ms to allow transmission of a turn-off reverse tone burst. The decoder detects a received PL tone and unquestions the receiver when the proper PL tone is received. In addition, PL tone filtering is provided so that the PL tone is not heard in normal received audio.

3. FUNCTIONAL OPERATION

Refer to the functional block and schematic diagrams attached to this instruction section.

3.1 SIMPLEX TARa AND TARb PL MODULES

The TARa PL module incorporates one integrated circuit (U1) and one resonant reed (Z1) for both encoding and decoding purposes. Similarly, the TARb PL module also incorporates one integrated circuit (U1), but uses two resonant reeds (Z1 and Z2) which allows the user to receive on one PL code and transmit on a different PL code. Other than these differences both modules function identically.

In the decode (receive) mode, received audio enters the PL module at the R1 DISC INPUT (pin 17), and is routed through an active low pass filter (Q1 and Q2) before being applied to the input of the tone decoder-encoder IC U1-8. When the proper PL tone is decoded, U1 produces a square wave at the decode output (pin 13) of U1, unloaded. The square wave is detected by detector switch circuitry (Q4 and Q5), which then enables PL INDICATOR output switch (Q6).

In the encode (transmit) mode, U1 (or U101) drives the PL reed primary. The code output at U1-3, which is sinusoidal is sampled by AGC circuitry which controls the amount of drive to the primary of the PL reed. By controlling the drive amount to the PL reed, a constant output voltage is present at PL CODE OUT, pin 21.

At the end of a transmission, the loss of KEYED A + triggers delayed keyed A + timing circuit U2. U2 now provides delayed keyed A + for 180 ms, and enables the phase shifter network so that a reverse burst (a phase shifted version of the PL tone) can be transmitted. Reverse burst causes the on-channel PL receivers to squelch rapidly.

PL filter circuitry is utilized to remove (attenuate) PL tones from the received audio. The received audio is filtered, first by a high pass filter, and then by a notch filter. Gyrorator circuits are used to provide high "Q" inductance, without employing inductors.
3.2 DUPLEx TaRs PL MODULE

This module is essentially the same as the simplex versions, except that it permits the user to decode (receive) and encode (transmit) simultaneously. In addition, the encode and decode codes may be different. This is accomplished by using two PL reeds, and two integrated circuits U1 and U101. In this configuration, one reed and one IC are dedicated for decoding purposes, while the other reed and IC are dedicated for encoding purposes.

4. DECODER CIRCUIT DESCRIPTION

4.1 LOW PASS FILTER

The 5-pole low pass filter attenuates high frequency noise above 192.8 Hz from the audio spectrum. This provides the balance of the decoder circuitry additional falsing and blocking immunity.

4.2 DECODER AND REED

The filtered PL tone is applied to the decoder tone input (U1-8) where it is amplified and limited. The PL tone is then fed to the decoding reed (Z1 for TaRs and Z2 for TaRs on Duplex applications), pins 2 and 3. If the PL tone is of the proper frequency, it will cause the reed to resonate. The reed secondary (pins 1 and 4) reacts to the sympathetic vibration and returns the PL tone to the decoder reed secondary input U1-11. The decoder now amplifies and limits the PL tone again, and provides an output at U1-13, Decode Output.

NOTE
If no PL tone is detected, the output of U1-13 is high.

4.3 DETECTOR SWITCH

When an output is present (indicating a proper PL tone detection) at the decode output of U1 (pin 13), it is waveshaped by capacitor C14 into a sawtooth waveform at a level of approximately 0.8 V p-p. If a high (no detect) is present at U1-13, the level of this same waveform is constant, approximately 2.2 V. The balance of the detector switch circuitry inverts, filters, and amplifies the sawtooth waveform (or high) to produce a true logic level at the PL INDICATOR output at pin 5 of the PL module.

4.4 NOISE GATE

Noise Gate Q3, allows a small amount of high frequency noise (with 1-pole of low pass filtering) to be fed to the decoder input, U1-8 when the PL INDICATOR output at pin 5 of the PL module is low. This tends to minimize noise falsing of the decoder. When the PL INDICATOR output is high, the high frequency noise sample is shunted to ground. This allows the PL module to be more sensitive once it receives a signal, and helps to prevent decoder dropout during brief signal fades.

5. ENCODER CIRCUIT DESCRIPTION

5.1 PL ENCODE SWITCH

The PL Encode Switch (Q8) is normally on unless one of the following conditions exist:

- Keyed A+ (pin 13) or Delayed Keyed A+ (pin 7) is low.
- PL Tone Inhibit (pin 14) is low.

When Q8 is on, the collector of Q9 is high (8.4 V).

5.2 ENCODER AND REED

When the PL Encode Switch is on, U1-16 (Encode Enable) and U1-14 goes high enabling the encoder, which in turn drives encode reed Z1. Encode reed Z1 now vibrates at its own resonant frequency, and U1 then produces a sine wave of the proper frequency at its output (Code Out), U1-3. The code output is fed back to Z1, via Q7 (which controls the drive to Z1) providing an automatic gain control which keeps the encoder output constant.

5.3 DELAYED KEYED A+ TIMING CIRCUIT

When keyed A+ (module pin 13) goes low after being high, U2-3 goes high for 180 ms. The high output of U2-3 causes pin 7 of the PL module to be high for the same time period, producing delayed keyed A+. When keyed A+ goes low, U2-6, 7 (which were low) go high at a rate determined by the RC time constant of R31 and C33.
When the voltage at U2-6, 7 is at the same level as the voltage at U2-5, delayed keyed A + ceases.

5.4 AMPLIFIER AND REVERSE BURST PHASE SHIFTER

When keyed A + is high, Q11 and Q12 are off. The Q13 amplifier circuitry amplifies the PL code output from U1-3 (or U101-3) of the encoder. When keyed A + goes low, delayed keyed A + goes high and turns on Q11 and Q12 which then change the phase of the PL code output (at pin 21 of the module) approximately 240° resulting in an amplified PL reverse burst.

5.5 8.4 V REGULATOR

This circuit provides a constant 8.4 V dc to various points in the PL encode switch circuitry.

5.6 PL FILTER

The PL filter provides PL tone filtering of receiver detected audio. The filter consists of a 3-pole high pass filter and a 1-pole notch filter. The PL filter incorporates capacitors and gyrator (an active, high "Q" inductance) circuits to provide attenuation of PL frequencies from 67 to 192.8 Hz.
1. GENERAL

1.1 PHYSICAL DESCRIPTION

The TRN5076A, 77A, 78A Digital Private-Line (DPL) Encoder-Decoder Modules are plug-in modules designed for use with Motorola base and repeater stations. All components and circuitry are mounted on a sturdy circuit card with connecting terminals that mate with the backplane interconnect board of the station rf-control chassis.

1.2 FUNCTIONAL DESCRIPTION

Each of these modules can encode and decode subaudible Digital Private-Line codes. The encoder modulates the transmitter, and when the PTT signal is removed, the circuitry delays transmitter turn-off by approximately 180 ms to allow transmission of a receiver turn-off code. The decoder detects a received DPL code, and unmutes the receiver when the proper code is received.

2. DESCRIPTION OF OPERATION

Refer to the functional block and schematic diagrams attached to this instruction section.

2.1 SIMPLEX TĀRā AND TĀRās DPL MODULES

2.1.1 General

The TRN5077A Simplex TĀRā Module incorporates one integrated circuit (U1) and one code plug (connected to J1) for both encoding and decoding. The TRN5078A Simple TĀRās Module also incorporates U1, but uses two code plugs (J250 and J251). The code plug designated J250 is used for the transmit code, and the code plug designated J251 is used for the receive code.

2.1.2 Decode Mode

In the decode (receive) mode, receiver audio is applied to the DPL module at pin 17, R1 DISC INPUT, and is routed through active low pass filter Q2-Q3, where frequencies above the DPL code range are attenuated. The output of the low pass filter is applied to phase-lock loop data conditioner U2, which squares the shape of the incoming code word. The output of the data conditioner is routed, via level shifter Q4, to the input of the decoder circuitry.

The decoder circuit consists of encoder-decoder U1, a 50 kHz clock (Y1, Q5), and the information stored in the code plug. When the proper code has been detected, the decoder provides a logic high at U1-7. This provides a logic high, via audio enable circuit Q15 & Q16, to pin 5, PL INDICATOR. This signal controls the audio mute gate on the station R1 audio and squelch module.

The logic high at U1-7 is also applied to sensitivity switch U3C, to disable the constant current source of U3D-U3E. With the constant current source disabled, the voltage at U2-8 is lowered, causing the sensitivity of U2 to increase. This provides additional immunity to audio interference and improved squaring of the incoming code word.

When the incoming (received) signal ceases, the sending transmitter produces a turn-off code. When the turn-off code is detected by the decoder, the detected output at U1-7 switches low. This decreases the sensitivity of the data conditioner and mutes receiver audio.

2.1.3 Encode Mode

When the station PTT signal is present, KEYED A+ is generated within the station. With KEYED A+ high, a high is generated at the collector of Q6, and is applied to encoder-decoder U1-9 (XMIT ENABLE). This causes U1 to switch to the encode mode. Encoder U1 then generates the transmit DPL code according to information stored in the code plug. The transmit DPL code signal is routed through the encoder low pass filter circuit (Q12 & Q13) to remove audio-frequency harmonics. The output
of the low pass filter is applied to the exciter via pin 21, DPL CODE OUT. During transmission, C22 is used in the circuit to shift the corner frequency of the filter. During the time when only turn-off code is transmitted, C22 is out of the circuit in order to unshift the corner frequency of the filter. When the PTT signal ceases, the loss of KEYED A+ triggers the delayed keyed A+ circuit (Q8, Q9, & Q10). This circuit provides DELAYED KEYED A+ to the station, via pin 7, for a period of approximately 180 ms, during which time the encoder sends the turn-off code to the exciter for transmission.

The transmit DPL code signal is inhibited during transmission (required for proper paging operation) by applying a low to pin 14, TRANSMIT PL INHIBIT. The low turns Q14 on, which shunts the junction of R17, R18, R20, and C20 to ac ground.

2.2 DUPLEX TAhs DPL MODULE

The TRN5076A Duplex TAhs Module is the same as the simplex versions, except that the module allows the station to decode (receive) and encode (transmit) simultaneously. This is accomplished by using separate, dedicated encoder and decoder integrated circuits and code plugs. In duplex operation, U1 is a decoder only, and U100 is an encoder only.

3. CIRCUIT DESCRIPTIONS

3.1 DELAYED KEYED A+ TIMING CIRCUIT

The delayed keyed A+ timing circuit is used to maintain transmitter turn-on long enough for the DPL encoder to send the turn-off code. This period is approximately 180 ms.

When pin 13, KEYED A+, goes low at the end of a transmission (loss of PTT), the negative side of C27 approaches A+. It should be noted that since the voltage on C27 cannot change instantaneously, the voltage at the junction of R53, R54 & CR5 is increased. When this voltage is larger than the anode voltage of CR5, the diode does not conduct. Thus, the collector of Q9 swings low (approaches ground), the base of Q10 approaches A+, and the collector of Q10 swings low, which turns off Q10. Therefore, the delayed keyed A+ line switches low, which causes station transmission to cease.

3.2 TWO-CODE SWITCH CIRCUIT

The two-code switch circuit (Q250 & Q251) on simplex TAhs models is used to select and enable the proper code plug for transmit and receive modes. Code plug J250 is active in the transmit mode, and code plug J251 is active in the receive mode.

During the receive mode, the collector of keyed A+ switch Q6 is low. This low is inverted by Q250, and is applied as a high to code plug J250, to disable the transmit code. The high from Q250 is inverted by Q251, and applied as a low to code plug J251, to enable the receive code.

During the transmit mode, the collector of keyed A+ switch Q6 is high, which causes the transmit code from J250 to be enabled (inverted low by Q250), and the receive code from J251 to be disabled (inverted high by Q251).

3.3 REGULATOR CIRCUIT

Regulator Q1 provides three regulated dc voltages from station A+ (13.9 V). These voltages, in addition to A+, power all circuitry on the DPL board. The regulated voltages are 11.1 V (B+), 10.5 V (C+), and 6.2 V (D+).