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Model Table

Model	Description
TRN9688A	Standard
TRN9689A	Standard with Intercom

1. GENERAL

1.1 PHYSICAL DESCRIPTION

The TRN9688A, 89A R1 Audio & Squelch Modules are plug-in modules designed for use with Motorola base and repeater stations. All components and circuitry are mounted on a sturdy circuit card with connecting terminals that mate with the backplane interconnect board of the station's rf control chassis.

1.2 FUNCTIONAL DESCRIPTION

Either the Model TRN9688A R1 Audio & Squelch Module or Module TRN9689A with intercom circuitry (option) functions as an audio amplifier between the receiver detector output and line driver module. Either module also accepts microphone audio and PTT signals for local operation of the transmitter.

The receiver detector circuit feeds an audio signal to the R1 Audio & Squelch Module for amplification (U1A) and input to the carrier squelch circuitry and line driver module (pin 17). The line driver module returns audio to the R1 audio and squelch module (pin 18) for amplification and output to a local speaker (pin 22). The squelch circuitry operates from rf carrier, coded squelch, or a combination of carrier and coded squelch. For local operation of the station, the operator uses a handset or microphone for audio (J1-5) and MIC PTT (J1-6) inputs to the R1 Audio & Squelch Module. The audio is amplified (U1B) for modulation of the exciter (pin 16). The MIC PTT signal mutes the local speaker (U4B), enables intercom audio (optional) output (U4D), and produces a local PTT signal output (pin 4) for keying the transmitter. During intercom operation (optional), the NORMAL-INTERCOM switch S1 must be placed in the INTERCOM position to insure that the MIC PTT signal

does not key the transmitter, via the local PTT output (pin 5). Intercom audio is routed, via the line driver module, to the remote control console. Remote control console intercom audio is routed from the line driver module to R1 Audio & Squelch Module (pin 18), as described previously.

2. DETAILED THEORY OF OPERATION

(Refer to the functional block and schematic diagrams at the end of this instruction section.)

2.1 VARIABLE GAIN AMPLIFIER CIRCUIT

The gain of U1A is adjustable by means of gain adjust R4. The gain is adjusted to provide a nominal voltage (380 mV rms) to the squelch circuit input (U101A-1). U1A also supplies receiver audio to the tone PL module and level adjust R7. The output of R7 drives the audio mute gate U4A. If the station is equipped with tone PL, JU1 is cut. When JU1 is cut, the R1 DET audio signal is routed through a PL filter, which is located on the tone PL module, and then applied to U4A.

2.2 AUDIO MUTE GATE CIRCUIT

U4A is a CMOS transmission gate. With a logic high control voltage, the gate is placed in the ON state. When in the ON state, audio mute gate U4A will supply audio to de-emphasis amplifier U3A. When the control voltage is switched to a logic low control voltage the gate is placed in the off (high impedance) state. In this condition, the audio signal is muted.

2.3 DE-EMPHASIS AMPLIFIER CIRCUIT

De-emphasis amplifier U3A amplifies the low level signal to provide the drive necessary for proper line driver operation. Feedback elements C7 and R13 also provide 6 dB per octave de-emphasis. Additional frequency response shaping is provided by the combination of C6, R12 & C9, R15.

2.4 AUDIO AMPLIFIER CIRCUIT

Amplifier U3B provides the necessary drive to the audio power amplifier. Frequency response shaping is provided by C12 and R20. Limit adjust R18 is adjusted to limit maximum audio power output to 1 watt. Drive to the power amplifier is first routed through audio mute gate U4B and volume control R25. U4B mutes the speaker audio during a MIC PTT signal.

2.5 AUDIO POWER AMPLIFIER CIRCUIT

Volume control R25 output is coupled to the audio power amplifier U2 by C17. U2 provides 1 watt of audio power into an 8-ohm speaker, at less than 5% distortion.

2.6 MIC AUDIO AMPLIFIER CIRCUIT

During local operation, mic audio is supplied to pin 5 of mic connector J1. For local transmission, this audio is amplified by U1B to provide the necessary drive to the exciter for proper operation.

2.7 INTERCOM OPTION CIRCUITRY

When the intercom option is present (TRN9689A only), mic audio is coupled through intercom mute gate U4D to the line driver. U4C inverts mic PTT to control intercom mute gate U4D. Intercom audio is muted by U4D when there is no mic PTT signal (GND) at U4C-6.

2.8 NOISE ACTIVATED SQUELCH CIRCUIT

2.8.1 Remote Controlled Squelch Circuit

With the remote controlled squelch option, JU101 is removed and JU102 and JU103 are installed. Then the R1 disc input signal, for the squelch circuit, is first routed through a remote controlled squelch module (option). This module provides the capability of remotely adjusting the squelch opening sensitivity. The remotely adjusted squelch signal is returned to the R1 Audio & Squelch Module as the R1 SQ ATTENUATOR signal, at pin 6.

2.8.2 Squelch Input Circuitry

The input to first amplifier/limiter U101A is a pre-emphasis network. This circuit boosts the noise content of the input signals above 5 kHz, for squelch processing the first amplifier/limiter is driven into limit to prevent audio signals from squelching the receiver. The amplified and limited noise signal is sent through a frequency shaping network to squelch control R25.

The squelch control wiper provides signal to second amplifier/limiter U101B. U101B amplifies the noise signal and relimits audio signals to provide further protection against audio signals squelching the receiver. The output signal of U101B is frequency shaped and sent to noise detector U101C.

2.8.3 Noise Detector and Switching Circuits

Noise detector U101C is a half wave rectifier-amplifier which produces negative going spikes at its output, U101C-12. The average dc value of these spikes is a function of received signal strength. The lowest average dc output voltage corresponds to a no signal input (maximum noise) condition. As the received signal strength increases, the noise level decreases, and the average dc output voltage increases.

The squelch switching circuitry operates in two modes. With a receive signal just above the opening sensitivity, squelch closing is slow (approximately 150 ms), which produces the squelch tail heard at the end of a received message. The 150 ms delay is present to prevent the received message from being chopped during a weak fluttering signal. With a strong signal (approximately 10 dB above opening sensitivity), squelch closing occurs immediately after the end of a received signal. This prevents the squelch tail from being heard.

Active integrator U101D provides squelch opening and slow squelch closing. U101D compares the detector's average dc output voltage with a reference voltage to determine squelch opening and closing.

Fast squelch closing is provided by Q102. A strong signal charges C116 through R120, turning Q102 on. With Q102 on, the collector voltage lowers to approximately 3.9 V dc. At the end of a strong signal, noise spikes from the detector are captured by CR103. This immediately discharges C116, turning off Q102. When Q102 turns off, its collector voltage goes to 9.4 volts, and C118 forces Q103 to close the squelch.

2.9 SQUELCH LOGIC CIRCUITRY

The squelch logic circuitry performs the necessary switching functions to provide proper squelch operation. This circuitry can operate in one of three different modes by selecting proper jumper cuts. Refer to the jumper table on the schematic diagram. For noise activated squelch operation only, JU105 is cut. In this mode, Q107 is always turned on. Squelching is controlled by the squelch noise circuit, through Q104. For coded (PL or DPL) squelch activation, both JU104 and JU105 remain in. In this mode, squelch turn-on is controlled by a proper coded squelch detection only. A proper coded squelch detection pulls the PL indicate line high, turning on Q105 and Q107. When PL DISABLED in this configuration, Q107 is turned on. This allows either a proper coded squelch detection or a noise activated squelch detection to open the squelch. This provides the OR squelch function.

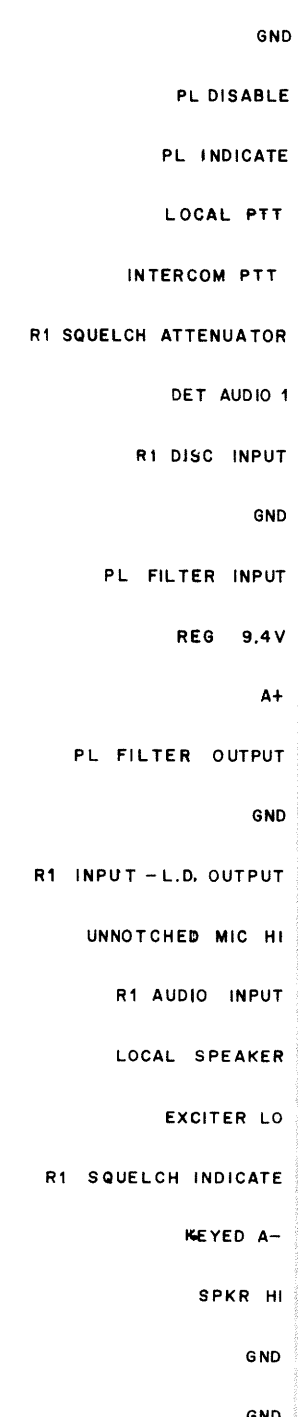
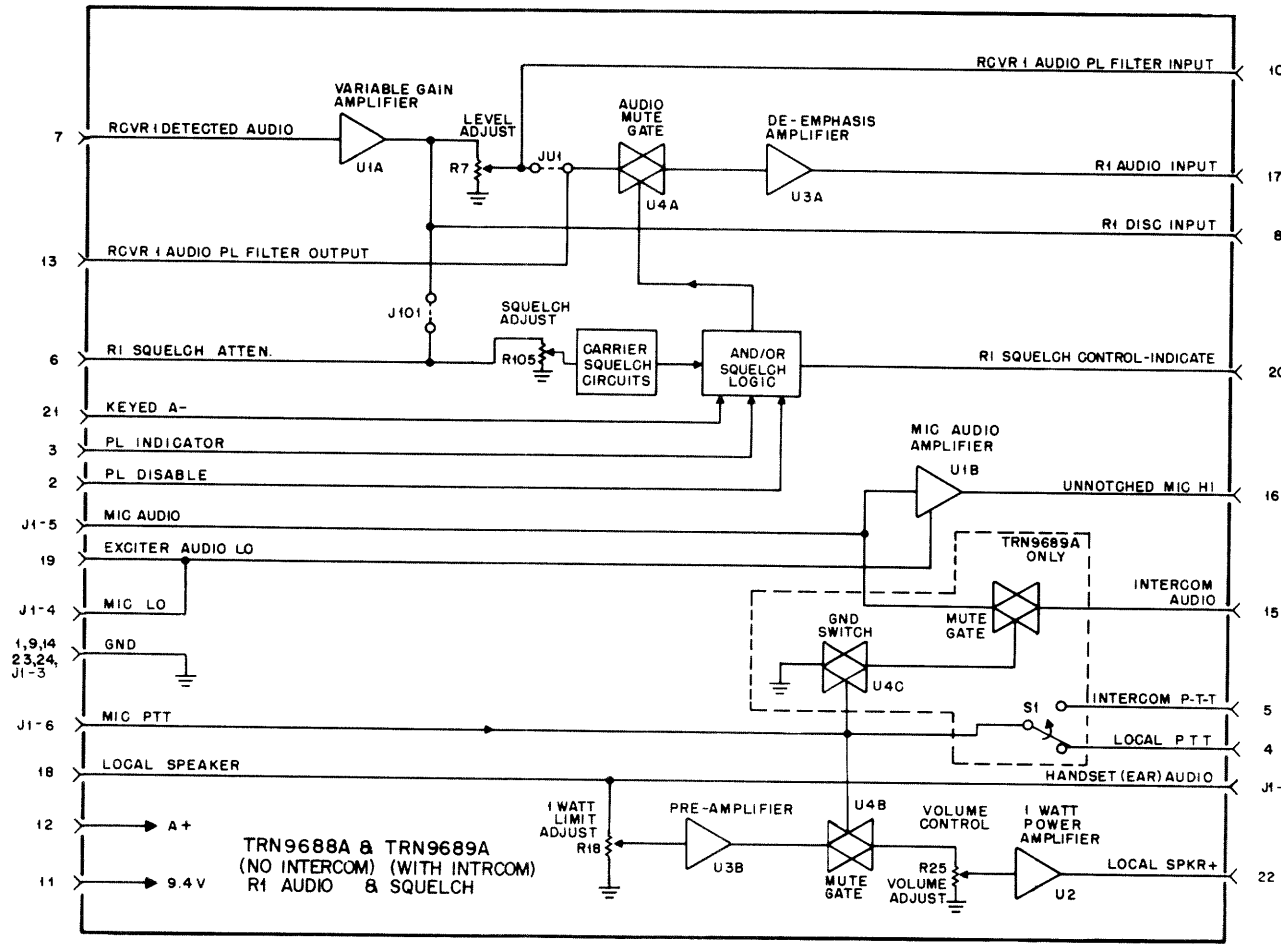
In the third mode of operation, JU104 is cut and JU105 remains in. This produces the AND squelch function. AND squelch means that both a proper coded squelch

detection and a noise activated squelch detection are required to open squelch. A proper coded squelch detection turns on Q107 and a noise activated squelch detection turns on Q104. Both are required to open squelch. When PL DISABLED in this configuration, both Q106 and Q107 are turned on. Again, this provides

the OR squelch function, where either a proper coded squelch detection or a noise activated squelch detection will open squelch. With Q107 on, and either Q104 or Q105 on, Q108 and Q109 are turned off. This enables audio mute gate U4A, creating an open squelch condition.

R1 AUDIO AND SQUELCH MODULES

MODELS TRN9688A, 89A



parts list

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R8, 9	6-11009E73	10k
R10, 11	6-11009F14	470k
R12	6-11009E69	6.8k
R13	6-11009F14	470k
R14	6-11009E61	3.3k
R15	6-11009E49	1k
R16, 17	6-11009E97	100k
R18	18-83083G01	variable; 100k
R19	6-11009E97	100k
R20	6-11009F02	150k
R21, 22	6-11009E97	100k
R23, 24	6-11009F14	470k
R25	18-83083G16	variable; 25k
R26	6-124D55	2.7
R27	6-11009A49	1k
R28	6-11009A43	560
R29	6-11009E75	12k
R30	6-11009E87	39k
R31, 32	6-11009E97	100k
R33	6-11009E45	680
R34, 35	6-11009A73	10k
R36 (B)	6-11009E69	6.8k
R37 (B)	6-11009A53	1.5k
R38, 39 (B)	6-11009B14	470k
R40 (B)	6-11009A51	1.2k
R41 (B)	6-11009A97	100k
R42	6-11009A49	1k
R43 thru 100	—	NOT USED
R101	6-11009E83	27k
R102	6-11009A83	27k
R103	6-11009E99	120k
R105	18-83083G28	variable; 1k
R106	6-11009E73	10k
R107	6-11009E99	120k
R108	6-11009E41	470
R109	6-11009E96	91k
R110	6-11009B06	220k
R111	6-11009E73	10k
R112	6-11009B02	150k
R113	6-11009A75	12k
R114	6-11009A61	3.3k
R115, 116	6-11009A33	220
R117	6-11009E61	3.3k
R118	6-11009E45	680
R119	6-11009A69	6.8k
R120	6-11009B02	150k
R121	6-11009A73	10k
R122	6-11009B06	220k
R123	6-11009B20	820k
R124	6-11009A53	1.5k
R125	6-11009A59	2.7k
R126	6-11009A77	15k
R127	6-11009A73	10k
R128	6-11009A65	4.7k
R129	6-11009A73	10k
R130	6-11009B04	180k
R131	6-11009A61	3.3k
R132, 133	6-11009A73	10k
R134	6-11009A53	1.5k
R135, 136, 137	6-11009A73	10k
R138	6-11009A65	4.7k
R139, 140	6-11009A73	10k
R141	6-11009A65	4.7k
R142	6-11009A97	100k
R143	6-11009E53	1.5k
S1 (B)	40-84979B15	switch, pushbutton: 2-pole; push-push
U1	51-80067C03	integrated circuit: (see note) dual op-amplifier
U2	51-83629M22	1 watt audio
U3	51-80067C03	dual op-amplifier
U4	51-82864L14	antenna switch
U5 thru 100	—	NOT USED
U101	51-83629M06	op-amplifier
VR1	48-83696E07	voltage regulator: (see note) Zener type; 6.2 V
VR2 thru 100	—	NOT USED
VR101 thru 104	48-82256C33	Zener type; 2.6 V
mechanical parts		
3-84256M01	SCREW, tapping; 4-10 x 5/16"; 2 used	
5-84220B01	GROMMET	
9-83497F01	RECEPTACLE, female; 8-contact; 3 used (circuit board edge connector)	
14-84360C01	INSULATOR, switch (TRN5069A)	
38-84962D01	PUSHBUTTON (TRN5069A)	
43-82721C01	BUSHING, snap; 2 used	
64-82865N01	PANEL, front (TRN5069A)	
64-82865N02	PANEL, front (TRN5068A)	
note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.		

TRN9688A, 89A R1 Audio & Squelch Modules
With and Without Intercom
Functional Block Diagram, Circuit Board Detail
and Parts List
Motorola No. PEPS-41742-A
(Sheet 1 of 2)
5/15/86-UP

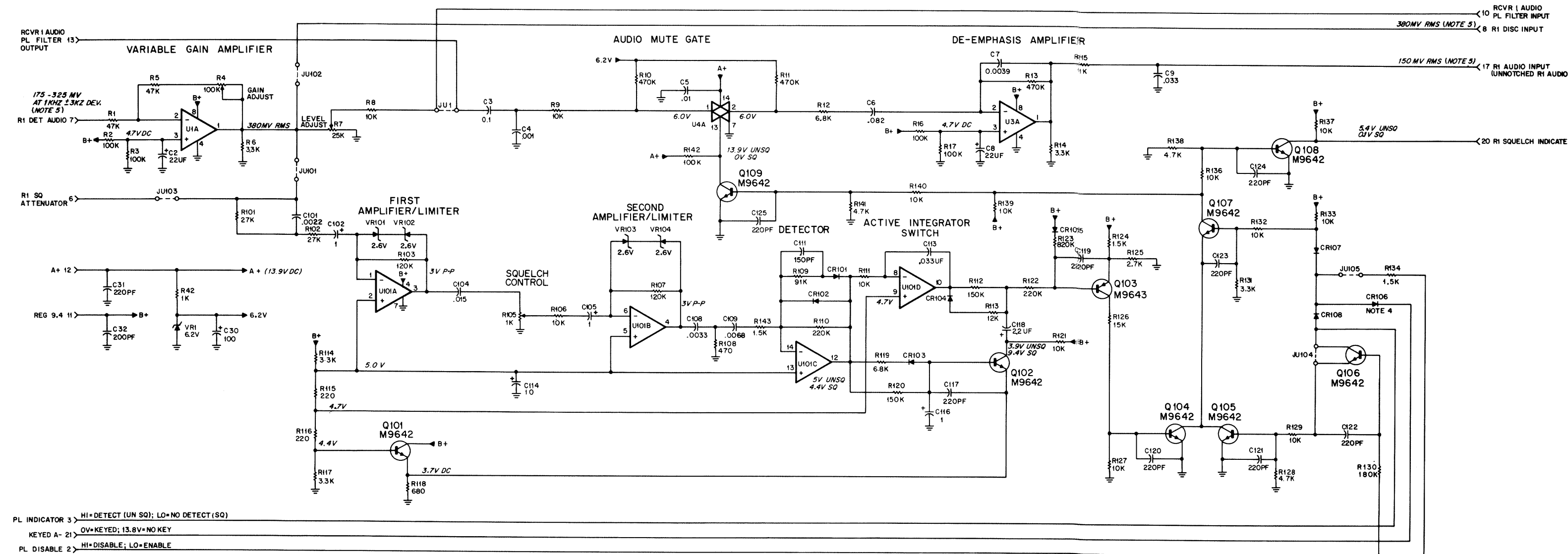
SHOWN FROM SOLDER SIDE

SOLDER SIDE: BD-DEPS-3 4469-0
COMPONENT SIDE: BD-DEPS-3 4470-0
OL-DEPS-3 4471-0

R1 6-11009E89
R2, 3 6-11009E97
R4 18-82374N02
R5 6-11009A89
R6 6-11009E61
R7 18-82374N01

R1 AUDIO AND SQUELCH MODULES

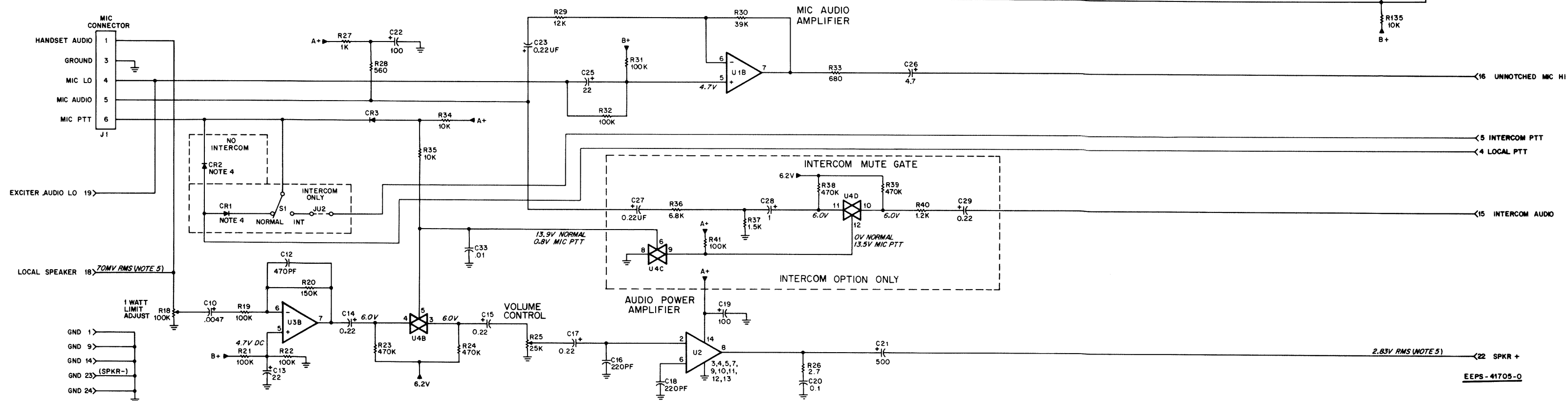
MODELS TRN9688A, 89A



- NOTES:
1. Unless otherwise indicated, resistors in ohms, and capacitors in microfarads.
 2. Local speaker connected to pins 22 (SPKR ±) and 23 (SPKR -).
 3. C27, 28, 29, CR1, JU2, R36 thru 41, and 51 present on TRN9689A only.
 4. Refer to jumper table for usage.
 5. System Adjustment Procedure:
 - A. Apply 1 mV rms of received frequency, modulated with a 1 kHz tone ± 3 kHz deviation, to the receiver 1 RF input.
 - B. Install JU102. Set R4 for 380 mV rms at pin 8-R1 disc input. Remove JU102.
 - C. Set R7 for 150 mV rms at pin 17-R1 audio input.
 - D. Set R25 max clockwise, adjust R18 for 2.83 V rms.

Jumper Table

Jumper	IN	OUT
JU1	No PL Filter Used	PL Filter Used
JU2	For Spectra-TAC Option	Normally
JU101	Normally	For Remote Squelch Option
JU102	For PL, DPL, Repeater, Single Tone Decoder, and Remote Squelch Option	Normally
JU103	For Remote Squelch Option	Normally
JU104	For PL "OR" Squelch	For PL "AND" Squelch
JU105	For PL Squelch	For Carrier Squelch
Diode	IN	OUT
CR1	For Intercom Option	Normally
CR2	Normally	For Intercom Option
CR106	Normally	For Repeater



TRN9688A, 89A R1 Audio & Squelch Modules
 With and Without Intercom
 Schematic Diagram
 Motorola No. PEPS-41742-A
 (Sheet 2 of 2)
 5/15/86-UP



Model Table

Model	Description
TRN5068A	Standard
TRN5069A	Standard with Intercom

1. GENERAL

1.1 PHYSICAL DESCRIPTION

The TRN5068A, 69A R1 Audio & Squelch Modules are plug-in modules designed for use with Motorola base and repeater stations. All components and circuitry are mounted on a sturdy circuit card with connecting terminals that mate with the backplane interconnect board of the station's rf control chassis.

1.2 FUNCTIONAL DESCRIPTION

Either the Model TRN5068A R1 Audio & Squelch Module or Module TRN5069A with intercom circuitry (option) functions as an audio amplifier between the receiver detector output and line driver module. Either module also accepts microphone audio and PTT signals for local operation of the transmitter.

The receiver detector circuit feeds an audio signal to the R1 Audio & Squelch Module for amplification (U1A) and input to the carrier squelch circuitry and line driver module (pin 17). The line driver module returns audio to the R1 audio and squelch module (pin 18) for amplification and output to a local speaker (pin 22). The squelch circuitry operates from rf carrier, coded squelch, or a combination of carrier and coded squelch. For local operation of the station, the operator uses a handset or microphone for audio (J1-5) and MIC PTT (J1-6) inputs to the R1 Audio & Squelch Module. The audio is amplified (U1B) for modulation of the exciter (pin 16). The MIC PTT signal mutes the local speaker (U4B), enables intercom audio (optional) output (U4D), and produces a local PTT signal output (pin 4) for keying the transmitter. During intercom operation (optional), the NORMAL-INTERCOM switch S1 must be placed in the INTERCOM position to insure that the MIC PTT signal

does not key the transmitter, via the local PTT output (pin 5). Intercom audio is routed, via the line driver module, to the remote control console. Remote control console intercom audio is routed from the line driver module to R1 Audio & Squelch Module (pin 18), as described previously.

2. DETAILED THEORY OF OPERATION

(Refer to the functional block and schematic diagrams attached to this instruction section.)

2.1 VARIABLE GAIN AMPLIFIER CIRCUIT

The gain of U1A is adjustable by means of gain adjust R4. The gain is adjusted to provide a nominal voltage (380 mV rms) to the squelch circuit input (U101A-1). U1A also supplies receiver audio to the tone PL module and level adjust R7. The output of R7 drives the audio mute gate U4A. If the station is equipped with tone PL, JU1 is cut. When JU1 is cut, the R1 DET audio signal is routed through a PL filter, which is located on the tone PL module, and then applied to U4A.

2.2 AUDIO MUTE GATE CIRCUIT

U4A is a CMOS transmission gate. With a logic high control voltage, the gate is placed in the ON state. When in the ON state, audio mute gate U4A will supply audio to de-emphasis amplifier U3A. When the control voltage is switched to a logic low control voltage the gate is placed in the off (high impedance) state. In this condition, the audio signal is muted.

2.3 DE-EMPHASIS AMPLIFIER CIRCUIT

De-emphasis amplifier U3A amplifies the low level signal to provide the drive necessary for proper line driver operation. Feedback elements C7 and R13 also provide 6 dB per octave de-emphasis. Additional frequency response shaping is provided by the combination of C6, R12 & C9, R15.

2.4 AUDIO AMPLIFIER CIRCUIT

Amplifier U3B provides the necessary drive to the audio power amplifier. Frequency response shaping is provided by C12 and R20. Limit adjust R18 is adjusted to limit maximum audio power output to 1 watt. Drive to the power amplifier is first routed through audio mute gate U4B and volume control R25. U4B mutes the speaker audio during a MIC PTT signal.

2.5 AUDIO POWER AMPLIFIER CIRCUIT

Volume control R25 output is coupled to the audio power amplifier U2 by C17. U2 provides 1 watt of audio power into an 8-ohm speaker, at less than 5% distortion.

2.6 MIC AUDIO AMPLIFIER CIRCUIT

During local operation, mic audio is supplied to pin 5 of mic connector J1. For local transmission, this audio is amplified by U1B to provide the necessary drive to the exciter for proper operation.

2.7 INTERCOM OPTION CIRCUITRY

When the intercom option is present (TRN5069A only), mic audio is coupled through intercom mute gate U4D to the line driver. U4C inverts mic PTT to control intercom mute gate U4D. Intercom audio is muted by U4D when there is no mic PTT signal (GND) at U4C-6.

2.8 NOISE ACTIVATED SQUELCH CIRCUIT

2.8.1 Remote Controlled Squelch Circuit

With the remote controlled squelch option, JU101 is removed and JU102 and JU103 are installed. Then the R1 disc input signal, for the squelch circuit, is first routed through a remote controlled squelch module (option). This module provides the capability of remotely adjusting the squelch opening sensitivity. The remotely adjusted squelch signal is returned to the R1 Audio & Squelch Module as the R1 SQ ATTENUATOR signal, at pin 6.

2.8.2 Squelch Input Circuitry

The input to first amplifier/limiter U101A is a pre-emphasis network. This circuit boosts the noise content of the input signals above 5 kHz, for squelch processing the first amplifier/limiter is driven into limit to prevent audio signals from squelching the receiver. The amplified and limited noise signal is sent through a frequency shaping network to squelch control R25.

The squelch control wiper provides signal to second amplifier/limiter U101B. U101B amplifies the noise signal and relimits audio signals to provide further protection against audio signals squelching the receiver. The output signal of U101B is frequency shaped and sent to noise detector U101C.

2.8.3 Noise Detector and Switching Circuits

Noise detector U101C is a half wave rectifier-amplifier which produces negative going spikes at its output, U101C-12. The average dc value of these spikes is a function of received signal strength. The lowest average dc output voltage corresponds to a no signal input (maximum noise) condition. As the received signal strength increases, the noise level decreases, and the average dc output voltage increases.

The squelch switching circuitry operates in two modes. With a receive signal just above the opening sensitivity, squelch closing is slow (approximately 150 ms), which produces the squelch tail heard at the end of a received message. The 150 ms delay is present to prevent the received message from being chopped during a weak fluttering signal. With a strong signal (approximately 10 dB above opening sensitivity), squelch closing occurs immediately after the end of a received signal. This prevents the squelch tail from being heard.

Active integrator U101D provides squelch opening and slow squelch closing. U101D compares the detector's average dc output voltage with a reference voltage to determine squelch opening and closing.

Fast squelch closing is provided by Q102. A strong signal charges C116 through R120, turning Q102 on. With Q102 on, the collector voltage lowers to approximately 3.9 V dc. At the end of a strong signal, noise spikes from the detector are captured by CR103. This immediately discharges C116, turning off Q102. When Q102 turns off, its collector voltage goes to 9.4 volts, and C118 forces Q103 to close the squelch.

2.9 SQUELCH LOGIC CIRCUITRY

The squelch logic circuitry performs the necessary switching functions to provide proper squelch operation. This circuitry can operate in one of three different modes by selecting proper jumper cuts. Refer to the jumper table on the schematic diagram. For noise activated squelch operation only, JU105 is cut. In this mode, Q107 is always turned on. Squelching is controlled by the squelch noise circuit, through Q104. For coded (PL or DPL) squelch activation, both JU104 and JU105 remain in. In this mode, squelch turn-on is controlled by a proper coded squelch detection only. A proper coded squelch detection pulls the PL indicate line high, turning on Q105 and Q107. When PL DISABLED in this configuration, Q107 is turned on. This allows either a proper coded squelch detection or a noise activated squelch detection to open the squelch. This provides the OR squelch function.

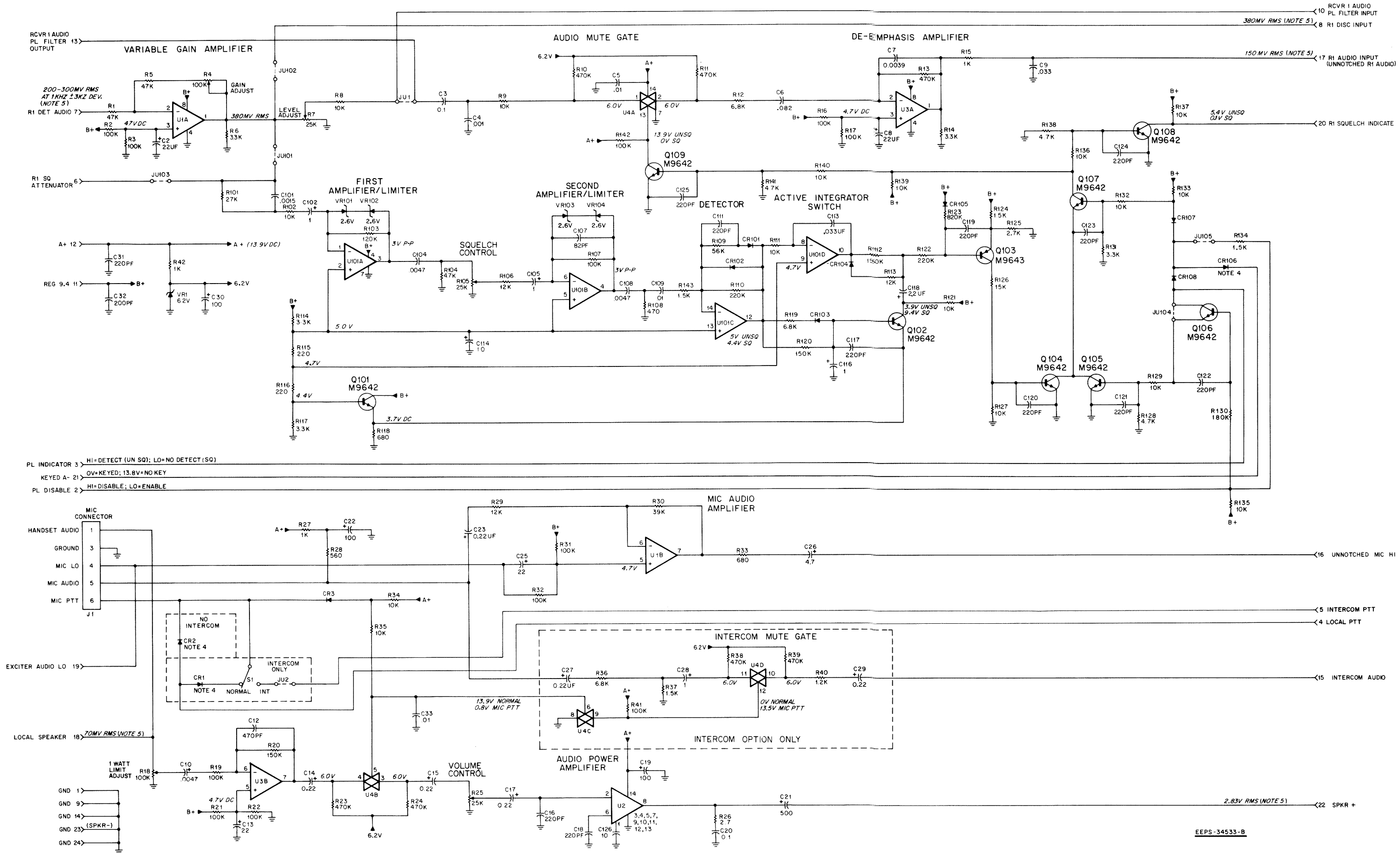
In the third mode of operation, JU104 is cut and JU105 remains in. This produces the AND squelch function. AND squelch means that both a proper coded squelch

detection and a noise activated squelch detection are required to open squelch. A proper coded squelch detection turns on Q107 and a noise activated squelch detection turns on Q104. Both are required to open squelch. When PL DISABLED in this configuration, both Q106 and Q107 are turned on. Again, this provides

the OR squelch function, where either a proper coded squelch detection or a noise activated squelch detection will open squelch. With Q107 on, and either Q104 or Q105 on, Q108 and Q109 are turned off. This enables audio mute gate U4A, creating an open squelch condition.

R1 AUDIO & SQUELCH MODULES

MODELS TRN5068A, 69A



- NOTES:
- Unless otherwise indicated, resistors in ohms, and capacitors in microfarads.
 - Local speaker connected to pins 22 (SPKR ±) and 23 (SPKR -).
 - C27, 28, 29, CR1, JU2, R36 thru 41, and 51 present on TRN5069A only.
 - Refer to jumper table for usage.
 - System Adjustment Procedure:
 - Apply 1 mV rms of received frequency, modulated with a 1 kHz tone ± 3 kHz deviation, to the receiver 1 RF input.
 - Install JU102. Set R4 for 380 mV rms at pin 8-R1 disc input. Remove JU102.
 - Set R7 for 150 mV rms at pin 17-R1 audio input.
 - Set R25 max clockwise, adjust R18 for 2.83 V rms.

Jumper Table

Jumper	IN	OUT
JU1	No PL Filter Used	PL Filter Used
JU2	For Spectra-TAC Option	Normally
JU101	Normally	For Remote Squelch Option
JU102	For PL, DPL, Repeater, Single Tone Decoder, and Remote Squelch Option	Normally
JU103	For Remote Squelch Option	Normally
JU104	For PL "OR" Squelch	For PL "AND" Squelch
JU105	For PL Squelch	For Carrier Squelch
Diode	IN	OUT
CR1	For Intercom Option	Normally
CR2	Normally	For Intercom Option
CR106	Normally	For Repeater

With and Without Intercom
Schematic Diagram
Motorola No. PEPS-34906-B
(Sheet 2 of 2)
11/1/85- UP



Model Table

Model	Description
TRN9690A	With Carrier Squelch
TRN9691A	With Carrier & PL Squelch
TRN9692A	With Carrier & DPL Squelch

1. GENERAL

1.1 PHYSICAL DESCRIPTION

The TRN9690A, 91A, and 92A R2 Audio & Squelch Modules are plug-in modules designed for use with Motorola base and repeater stations. All components and circuitry are mounted on a sturdy circuit card with connecting terminals that mate with the backplane interconnect board of the station's RF Control Chassis. These modules are used only with two receiver stations.

1.2 FUNCTIONAL DESCRIPTION

Each of these modules function as an audio amplifier between the second receiver's detector output and the line driver module. They also can perform a carrier squelch function for the second receiver. Additionally, Model TRN9691A can perform a PL squelch function, and Model TRN9692A can perform a DPL squelch function.

The second receiver detector circuit feeds an audio signal to the R2 Audio & Squelch Module for amplification (U1), input to the carrier squelch circuitry, and output to the line driver module (pin 17). The line driver module returns audio to the R1 audio & squelch module (pin 18) for amplification and output to a local speaker (pin 22). The on-board squelch circuitry operates from rf carrier, coded squelch, or a combination of carrier and coded squelch.

2. DETAILED THEORY OF OPERATION

(Refer to the functional block and schematic diagrams at the end of this instruction section.)

2.1 VARIABLE GAIN AMPLIFIER CIRCUIT

The gain of U1 is adjustable by means of gain adjust R3. The gain is adjusted to provide a nominal voltage

(380 mV rms) to the squelch circuit input (U101A-1). U1 also supplies receiver audio to possible on-board PL or DPL circuitry, and level adjust R7. The output of R7 drives audio mute gate Q1. If the station is equipped with tone PL, JU1 is cut. When JU1 is cut, the R2 DET AUDIO signal is routed through an on-board PL filter, and then applied to Q1.

2.2 AUDIO MUTE GATE CIRCUIT

Q1 is a P-Channel Field Effect Transistor (FET). With a logic low control voltage, the FET is placed in the ON state. When in the ON state, audio mute gate Q1 will supply audio to de-emphasis amplifier U2. When the control voltage is switched to a logic high, the gate is placed in the OFF (high impedance) state. In this condition, the audio signal is muted.

2.3 DE-EMPHASIS AMPLIFIER CIRCUIT

De-emphasis amplifier U2 amplifies the low level signal to provide the drive necessary for proper line driver operation. Feedback elements C9 and R12 also provide 6 dB per octave de-emphasis. Additional frequency response shaping is provided by the combination of C8 and R11, and R14 (on TRN9690A, 91A), or C8 and R11, and C10 and R14 (on TRN9692A).

2.4 NOISE ACTIVATED (CARRIER) SQUELCH CIRCUIT

2.4.1 Squelch Input Circuitry

The input to first amplifier/limiter U101A is a pre-emphasis network. This circuit boosts the noise content of the input signals above 5 kHz, for squelch processing the first amplifier/limiter is driven into limit to prevent audio signals from squelching the receiver. The amplified and limited noise signal is sent through a frequency shaping network to SQUELCH control R105.

The squelch control wiper provides signal to second amplifier/limiter U101B. U101B amplifies the noise signal and relimits audio signals to provide further protection against audio signals squelching the receiver. The

output signal of U101B is frequency shaped and sent to noise detector U101C.

2.4.2 Noise Detector and Switching Circuits

Noise detector U101C is a half wave rectifier amplifier which produces negative going spikes at its output, U101C-10. The average dc value of these spikes is a function of received signal strength. The lowest average dc output voltage corresponds to a no signal input (maximum noise) condition. As the received signal strength increases, the noise level decreases, and the average dc output voltage increases.

The squelch switching circuitry operates in two modes. With a receive signal just above the opening sensitivity, squelch closing is slow (approximately 150 ms), which produces the squelch tail heard at the end of a received message. The 150 ms delay is present to prevent the received message from being chopped during a weak fluttering signal. With a strong signal (approximately 10 dB above opening sensitivity), squelch closing occurs immediately after the end of a received signal. This prevents the squelch tail from being heard.

Active integrator U101D provides squelch opening and slow squelch closing. U101D compares the detector's average dc output voltage with a reference voltage to determine squelch opening and closing.

Fast squelch closing is provided by Q102. A strong signal charges C112 through R120, turning Q102 on. With Q102 on, the collector voltage lowers to approximately 3.9 V dc. At the end of a strong signal, noise spikes from the detector are captured by CR104. This immediately discharges C112, turning off Q102. When Q102 turns off, its collector voltage goes to 9.4 volts, and C114 forces Q103 to close the squelch.

2.5 PRIVATE-LINE TONE CODED SQUELCH CIRCUIT

2.5.1 General

Essentially, the on-board PL decoder circuit of Model TRN9691A R2 Audio & Squelch Module detects a received PL tone and unsquelches the receiver when the proper PL tone is received. In addition, PL tone filtering is provided so that the PL tone is not heard in normal received audio.

Received R2 audio enters the PL circuit as R2 DISC INPUT (from U1-6), and is routed through an active low pass filter (Q201 and 202) before being applied to the input of the tone decoder IC U201-8. When the proper PL tone is decoded, U201 produces a square wave at the decode output (U201-13), unloaded. The square wave is detected by detector switch circuitry (Q204 and 205), which then enables PL INDICATOR output switch (Q206).

PL filter circuitry is utilized (JU1 out) to remove (attenuate) PL tones from the received audio. The received audio is filtered, first by a high pass filter, and then by a notch filter. A gyrator circuit is used for the notch filter to provide high "Q" inductance, without employing inductors.

2.5.2 PL Decoder Circuit Description

NOTE

The decoder IC U201 generates a high PL INDICATOR output (on the collector of Q206) when a proper PL tone is detected.

2.5.2.1 LOW PASS FILTER

The 5-pole low pass filter (Q201 and 202) attenuates high frequency noise above 192.8 Hz from the received R2 DISC INPUT audio. This provides the balance of the decoder circuitry additional falsing and blocking immunity.

2.5.2.2 DECODER AND REED

The filtered PL tone is applied to the decoder tone input (U201-8), where it is amplified and limited. The PL tone is then fed to the decoding reed Z201, pins 2 and 3. If the PL tone is of the proper frequency, it will cause the reed to resonate. The reed secondary (pins 1 and 4) reacts to the sympathetic vibration and returns the PL tone to the decoder reed secondary input U201-11. The decoder then amplifies and limits the PL tone once again, and provides an output at U201-13, Decode Output.

NOTE

If no proper PL tone is detected, the output of U1-13 stays high.

2.5.2.3 DETECTOR SWITCH

When an output is present (indicating a proper PL tone detection) at the decode output of U201 (pin 13), it is waveshaped by capacitor C212 into a sawtooth waveform at a level of approximately 0.8 V p-p. If a high (no detect) is present at U201-13, the level of this same waveform is constant, approximately 2.2 V. The balance of the detector switch circuitry inverts, filters, and amplifies the sawtooth waveform to produce a true logic level (logic high) at the collector of Q206 (PL INDICATOR).

2.5.2.4 NOISE GATE

Noise Gate Q203 allows a small amount of high frequency noise (with 1-pole of low pass filtering) to be fed to the decoder input, U201-8 when the PL INDICATOR output at the collector of Q206 is low. This tends to minimize noise falsing of the decoder. When the PL INDICATOR output is high, the high frequency noise sam-

ple is shunted to ground. This allows the onboard PL circuit to be more sensitive, once it receives a signal, and helps to prevent decoder dropout during brief signal fades.

2.5.2.5 8.4 V REGULATOR

The Q207 regulator circuit provides a constant 8.4 V dc (E+) to the PL decoder IC, U201.

2.6 DIGITAL PRIVATE-LINE CODED SQUELCH CIRCUIT

2.6.1 General

Essentially, the on-board DPL decoder circuit of Model TRN9692A R2 Audio & Squelch Module detects a received DPL code, and unmutes the receiver when the proper code is received. Received R2 audio enters the DPL circuit as R2 DISC INPUT (from U1-6), and is routed through an active low pass filter (Q301 and 302), where frequencies above the DPL code range are attenuated. The output of the low pass filter is applied to phase-lock-loop (PLL) data conditioner U302, which squares the shape of the incoming code word. The output of the data conditioner is routed, via level shifter Q303, to the input of the decoder IC U301-11.

The decoder circuit consists of IC U301, a 50 kHz clock (Y301 and Q304), and the information stored in the code plug (J301). When the proper code has been detected, the decoder provides a logic high at U301-7. That high provides a logic low, via audio enable Q305, to enable the PL INDICATOR output switch (Q306).

The logic high at U301-7 is also applied to sensitivity switch U304C, to disable the constant current source of U304D-U304E. With the constant current source disabled, the voltage at U302-8 is lowered, causing the sensitivity of U302 to increase. This provides additional immunity to audio interference and improved squaring of the incoming code word.

When the incoming (received) signal ceases, the sending transmitter produces a turn-off code. When the turn-off code is detected by the decoder, the detected output at U301-7 switches low. This decreases the sensitivity of the data conditioner and causes receiver audio to be muted.

2.6.2 DPL Decoder Circuit Description

NOTE

The decoder IC U301 generates a high (PL INDICATOR) output on the collector of Q206 when a proper DPL code is detected.

2.6.2.1 LOW PASS FILTER

The low pass filter circuit is similar to the one previously described for the PL decoder circuit in this section. However, the filter's output is fed through a PLL data conditioner (U302) for waveshaping, and a level shifter (Q303) to properly process the incoming code word, before presenting it to the decoder (U301) circuitry.

2.6.2.2 DECODER AND CODE PLUG

The processed code word is applied to the decoder's data input (U301-11), where it is compared to the data stored in the code plug (J301), at a 50 kHz rate. If the incoming code word is correct, U301 will provide a logic high at the decoder's detected output U301-7.

NOTE

If no proper code word is detected, the output of U301-7 stays low.

2.6.2.3 AUDIO ENABLE

When a high output is present at U301-7 (indicating a proper DPL code detection), it is inverted by Q305 to enable Q306. Output switch Q306 then produces a true logic level (logic high) at its collector (PL INDICATOR).

2.6.2.4 REGULATOR CIRCUIT

Regulator Q307 provides three regulated dc voltages from station A+ (13.9 V). These voltages, in addition to A+, power all circuitry in the DPL decoder section of the module. The regulated voltages are:

10.5 V (C+), 6.2 V (D+), and 11.1 V (E+).

2.7 AND-OR SQUELCH LOGIC CIRCUITRY

The squelch logic circuitry performs the necessary switching functions to provide proper squelch operation. This circuitry can operate in one of three different modes by selecting proper jumper cuts. Refer to the jumper table on the schematic diagram. First, for noise activated squelch operation only, JU102 is cut. In this mode, Q107 is always turned on. Squelching is controlled by the squelch noise circuit, through Q104. For coded (PL or DPL) squelch activation, both JU101 and JU102 remain in. In this mode, squelch turn-on is controlled by a proper coded squelch detection only. A proper coded squelch detection pulls the PL INDICATOR line high, turning on Q105 and Q107. Second, when PL DISABLED in this configuration, Q107 is turned on. This allows either a proper coded squelch detection or a noise activated squelch detection to open the squelch. This provides the OR squelch function.

In the third mode of operation, JU101 is cut and JU102 remains in. This produces the AND squelch function.

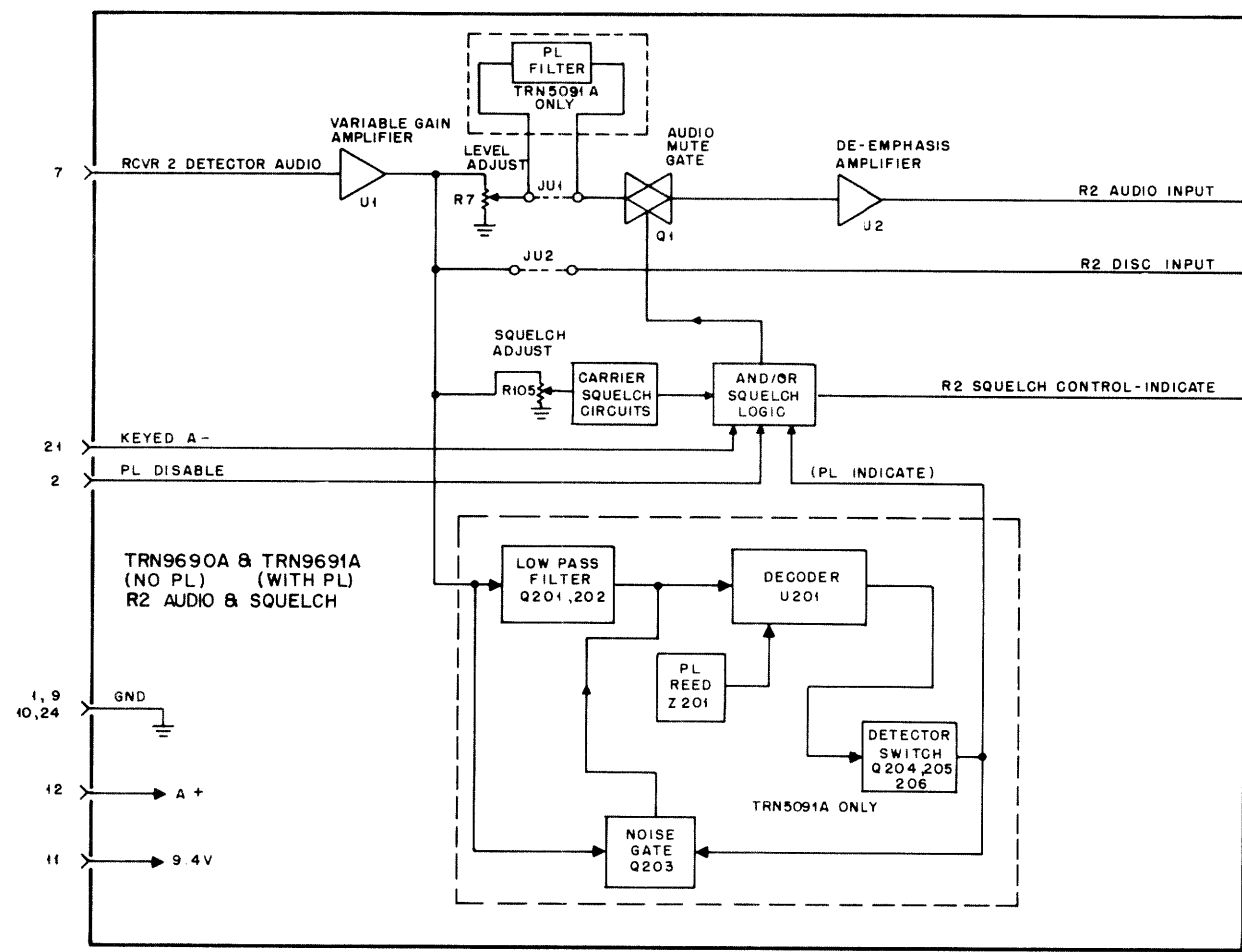
AND squelch means that both a proper coded squelch detection and a noise activated squelch detection are required to open squelch. A proper coded squelch detection turns on Q107 and a noise activated squelch detection turns on Q104. Both are required to open squelch. When PL DISABLED in this configuration both Q106 and Q107 are turned on. Again, this provides

the OR squelch function, where either a proper coded squelch detection *or* a noise activated squelch detection will open squelch.

With Q107 on, and either Q104 or Q105 on, Q108 and Q109 are turned off. This enables audio mute gate Q1, creating an open squelch condition.

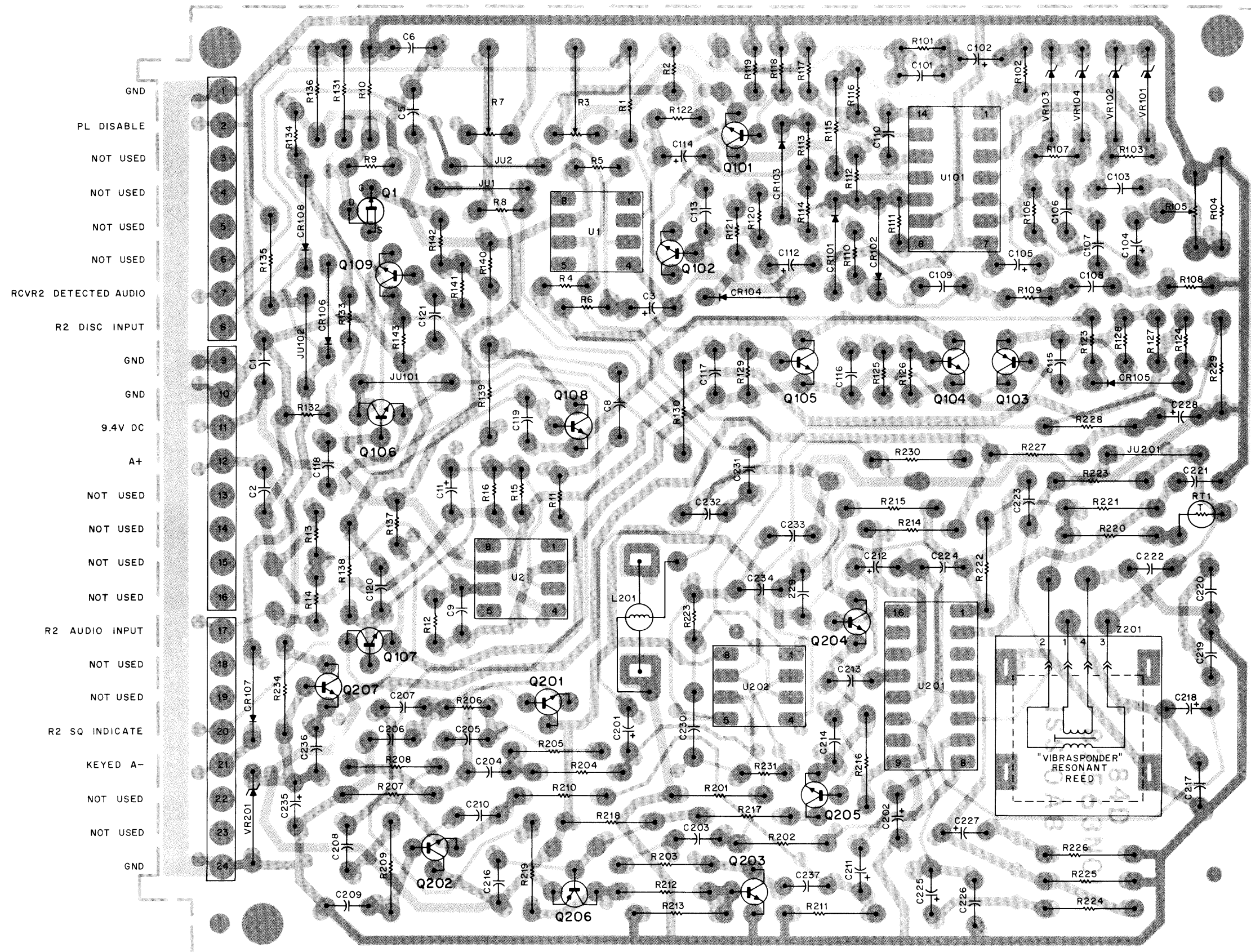
R2 AUDIO AND SQUELCH MODULES

MODELS TRN9690A, 91A



CEPS-4170B-0

TRN9690A (Carrier Only), 91A (with PL),
R2 Audio & Squelch Modules
Functional Block Diagram, Circuit Board Detail,
and Parts List
Motorola No. PEPS-41743-A
(Sheet 1 of 2)
5/15/86-UP



SHOWN FROM SOLDER SIDE

SOLDER SIDE BD-DEPS-34534-C
COMPONENT SIDE BD-DEPS-34535-C
OL-DEPS-34536-A

parts list

reference symbol suffix application all models TRN9690A TRN9691A

This parts list covers 2 models of the R2 Audio and Squelch Modules. Where differences exist, a letter code is added to the reference symbol to indicate the applicable unit.

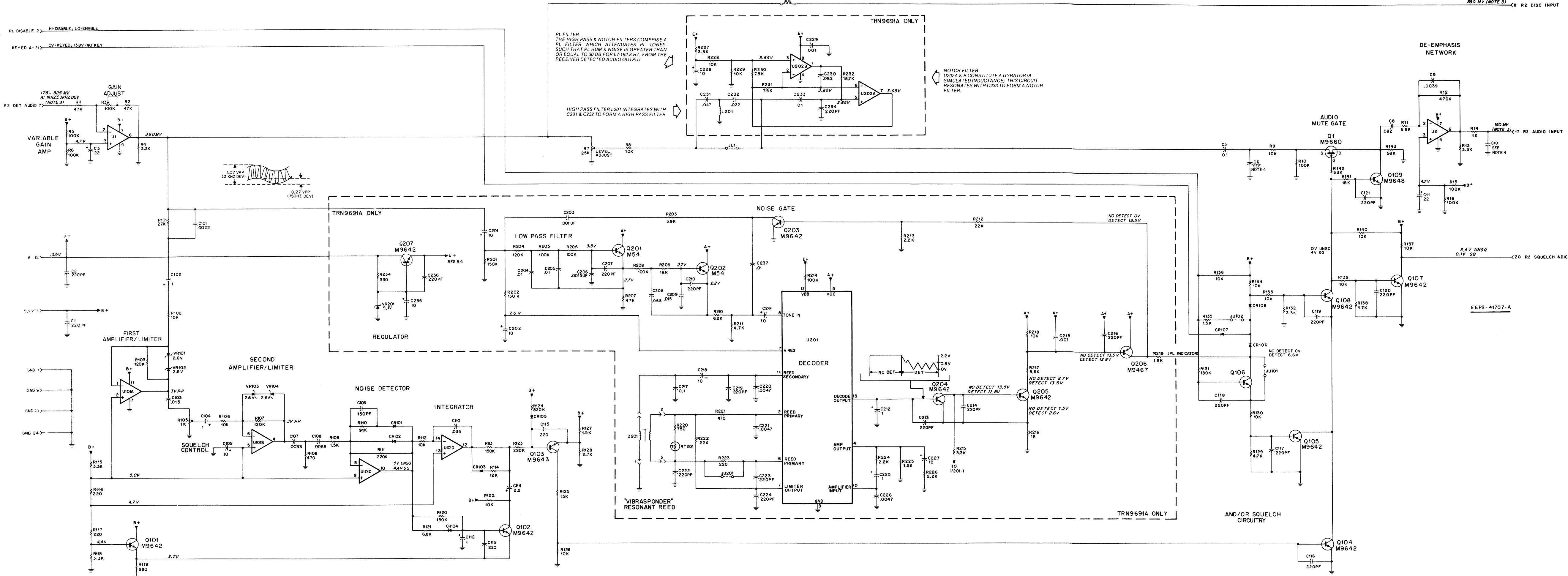
TRN9690A R2 Audio and Squelch TRN9691A R2 Audio and Squelch with PL Module PL-9670-C

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
C1, 2	21-11015B05	capacitor, fixed: uF ± 5%; 50 V; unless otherwise stated
C2	23-11019A27	220 pF ± 20%; 100 V
C3	22 ± 20%; 25 V	
C4	—	NOT USED
C5	8-11017A17	0.1
C6	—	NOTE 2
C7	—	NOT USED
C8	8-84637L36	.022 100 V
C9	8-11017A18	.0039
C10	—	NOTE 1
C11	23-11019A27	22 ± 20%; 25 V
C12 thru 100	—	NOT USED
C101	8-11017A03	.022 ± 10%
C102	23-11019A09	1 ± 20%
C103	8-11017A09	.015
C104	23-11019A09	1 ± 20%
C105	23-11019A20	10 ± 20%; 25 V
C106	8-11017A05	.0033
C107	8-11017A07	.0068
C108	21-11022G59	150 pF
C109	8-11017A13	.033
C110	23-11019A09	1 ± 20%
C111	21-11015B05	220 pF ± 10%; 100 V
C112	23-11019A11	2.2 ± 20%
C113 thru 121	21-11015B05	220 pF ± 10%; 100 V
C122 thru 200	—	NOT USED
C201, 202 (B)	23-11019A20	10 ± 20%; 25 V
C203 (B)	8-11017B01	.001 ± 10%
C204, 205 (B)	8-11017B08	.01
C206 (B)	8-11017B02	.0015 ± 10%
C207 (B)	21-11015B05	220 pF ± 10%; 100 V
C208 (B)	8-11017B16	.068
C209 (B)	8-11017B09	.015
C210 (B)	21-11015B05	220 pF ± 10%; 100 V
C211 (B)	23-11019A20	10 ± 20%; 25 V
C212 (B)	23-11019A09	1 ± 20%
C213, 214 (B)	21-11015B05	220 pF ± 10%; 100 V
C215 (B)	8-11017B01	.001 ± 10%
C216 (B)	21-11015B05	220 pF ± 10%; 100 V
C217 (B)	8-11017A17	0.1
C218 (B)	23-11019A20	10 ± 20%; 25 V
C219 (B)	21-11015B05	220 pF ± 10%; 100 V
C220, 221 (B)	8-11017B06	.0047 ± 10%
C222, 223, 224 (B)	21-11015B05	220 pF ± 10%; 100 V
C225 (B)	23-11019A09	1 ± 20%
C226	8-11017B06	.0047 ± 10%
C227, 228 (B)	23-11019A20	10 ± 20%; 25 V
C229 (B)	8-11017B01	.001 ± 10%
C230 (B)	8-84637L36	.022 ± 10%; 250 V
C231 (B)	8-11017A14	.047
C232 (B)	8-11017A11	.022
C233 (B)	8-11017A17	0.1
C234 (B)	21-11015B05	220 pF ± 10%; 100 V
C235 (B)	23-11019A20	10 ± 20%; 25 V
C236 (B)	21-11015B05	220 pF ± 10%; 100 V
C237 (B)	8-11017B08	.01
CR101 thru 108	48-83654H01	diode: (see note 3) silicon
JU1 (A)	6-11009B23	jumper: 0 ohms
JU2	6-11009B23	0 ohms
JU3 thru 100	—	NOT USED
JU101, 102	6-11009B23	0 ohms
JU103 thru 200	—	NOT USED
JU201 (B)	6-11009B23	0 ohms
L201 (B)	24-84003A01	coil, rf; choke: 6 H
Q1	48-869660	transistor: (see note 3) FET, p-channel; type M9660
Q2 thru 100	—	NOT USED
Q101, 102	48-869642	NPN; type M9642
Q103	48-869643	PNP; type M9643
Q104 thru 108	48-869642	NPN; type M9642
Q109	48-869648	NPN; type M9648
Q110 thru 200	—	NOT USED
Q201	48-869660	transistor: (see note 3) FET, p-channel; type M9660
Q202	—	NOT USED
Q203	48-869642	NPN; type M9642
Q204	48-869643	PNP; type M9643
Q205 (B)	48-869642	NPN; type M9642
Q206 (B)	48-869648	NPN; type M9648
Q207 (B)	—	NOT USED
Q208 (B)	—	NOT USED
Q209 (B)	—	NOT USED
Q210 (B)	—	NOT USED
Q211 (B)	—	NOT USED
Q212 (B)	—	NOT USED
Q213 (B)	—	NOT USED
Q214 (B)	—	NOT USED
Q215 (B)	—	NOT USED
Q216 (B)	—	NOT USED
Q217 (B)	—	NOT USED
Q218 (B)	—	NOT USED
Q219 (B)	—	NOT USED
Q220 (B)	—	NOT USED
Q221 (B)	—	NOT USED
Q222 (B)	—	NOT USED
Q223 (B)	—	NOT USED
Q224 (B)	—	NOT USED
Q225 (B)	—	NOT USED
Q226 (B)	—	NOT USED
Q227 (B)	—	NOT USED
Q228, 229 (B)	—	NOT USED
Q230, 231 (B)	—	NOT USED
Q232 (B)	—	NOT USED
Q233 (B)	—	NOT USED
Q234 (B)	—	NOT USED
R1	6-11009A89	47k
R2	6-11009E69	47k
R3	18-82374N02	variable; 100k
R4	6-11009E61	3.3k
R5, 6	6-11009E97	100k
R7	18-82374N01	variable; 25k
R8, 9	6-11009E73	10k
R10	6-11009A97	100k
R11	6-11009E69	6.8k
R12	6-11009F14	470k
R13	6-11009E61	3.3k
R14	6-11009E49	1k
R15, 16	6-11009E97	100k
R17 thru 100	—	NOT USED
R101	6-11009A83	27k
R102	6-11009A73	10k
R103	6-11009E99	120k
R105	18-83083G28	variable; 1k
R106	6-11009E73	10k
R107	6-11009E99	120k
R108	6-11009E41	470
R109	6-11009E53	1.5k
R110	6-11009E96	91k
R111	6-11009F06	220k
R112	6-11009E73	10k
R113	6-11009F02	150k
R114	6-11009E75	12k
R115	6-11009A61	3.3k
R116, 117	6-11009E33	220
R118	6-11009E61	3.3k
R119	6-11009E45	680
R120	6-11009F02	150k
R121	6-11009E69	6.8k
R122	6-11009E73	10k
R123	6-11009F06	220k
R124	6-11009F20	820k
R125	6-11009E77	15k
R126	6-11009E73	10k
R127	6-11009E53	1.5k
R128	6-11009E59	2.7k
R129	6-11009E65	4.7k
R130	6-11009A73	10k
R131	6-11009B04	180k
R132	6-11009E61	3.3k
R133, 134	6-11009E73	10k
R135	6-11009A53	1.5k
R136	6-11009A73	10k
R137	6-11009E73	10k
R138	6-11009A65	4.7k
R139	6-11009A73	10k
R140	6-11009E73	10k
R141	6-11009E77	15k
R142	6-11009E85	33k
R143	6-11009E91	56k
R144 thru 200	—	NOT USED
R201, 202 (B)	6-11009B02	150k
R203 (B)	6-11009A63	3.9k
R204 (B)	6-11009A99	120k
R205 (B)	6-11009A97	100k
R206 (B)	6-11009E97	100k
R207 (B)	6-11009A89	47k
R208 (B)	6-11009A97	100k
R209 (B)	6-11009A78	16k
R210 (B)	6-11009A68	6.2k
R211 (B)	6-11009A85	4.7k
R212 (B)	6-11009A81	22k
R213 (B)	6-11009A57	2.2k
R214 (B)	6-11009A97	100k
R215 (B)	6-11009A61	3.3k
R216 (B)	6-11009A49	1k
R217 (B)	6-11009A67	5.6k
R218 (B)	6-11009A73	10k
R219 (B)	6-11009A53	1.5k
R220 (B)	6-11009A46	750
R221 (B)	6-11009A41	470
R222 (B)	6-11009A81	22k
R223 (B)	6-11009A33	220
R224 (B)	6-11009A57	2.2k
R225 (B)	6-11009A53	1.5k
R226 (B)	6-11009A57	2.2k
R227 (B)	6-11009A61	3.3k
R228, 229 (B)	6-10621C91	10k ± 1%; 1/8 W
R230, 231 (B)	6-10621C79	7.5k ± 1%; 1/8 W
R232 (B)	6-10621D18	18.7k ± 1%; 1/8 W
R233	—	NOT USED
R234 (B)	6-11009A37	330
RT201 (B)	6-865641	thermistor: 300 @ 25°C

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
Q201, 202 (B)	48-134674	NPN; type M54
Q203, 204, 205 (B)	48-869642	NPN; type M9642
Q206 (B)	48-869647	PNP; type M9467
Q207 (B)	48-869642	NPN; type M9642
R1	6-11009A89	47k
R2	6-11009E69	47k
R3	18-82374N02	variable; 100k
R4	6-11009E61	3.3k
R5, 6	6-11009E97	100k
R7	18-82374N01	variable; 25k
R8, 9	6-11009E73	10k
R10	6-11009A97	100k
R11	6-11009E69	6.8k
R12	6-11009F14	470k
R13	6-11009E61	3.3k
R14	6-11009E49	1k
R15, 16	6-11009E97	100k
R17 thru 100	—	NOT USED
R101	6-11009A83	27k
R102	6-11009A73	10k
R103	6-11009E99	120k
R105	18-83083G28	variable; 1k
R106	6-11009E73	10k
R107	6-11009E99	120k
R108	6-11009E41	470
R109	6-11009E53	1.5k
R110	6-11009E96	91k
R111	6-11009F06	220k
R112	6-11009E73	10k
R113	6-11009F02	150k
R114	6-11009E75	12k
R115	6-11009A61	3.3k
R116, 117	6-11009E33	220
R118	6-11009E61	3.3k
R119	6-11009E45	680
R120	6-11009F02	150k
R121	6-11009E69	6.8k
R122	6-11009E73	10k
R123	6-11009F06	220k
R124	6-11009F20	820k
R125	6-11009E77	15k
R126	6-11009E73	10k
R127	6-11009E53	1.5k
R128	6-11009E59	2.7k
R129	6-11009E65	4.7k
R130	6-11009A73	10k
R131	6-11009B04	180k
R132	6-11009E61	3.3k
R133, 134	6-11009E73	10k
R135	6-11009A53	1.5k
R136	6-11009A73	10k
R137	6-11009E73	10k
R138	6-11009A65	4.7k
R139	6-11009A73	10k
R140	6-11009E73	10k
R141	6-11009E77	15k
R142	6-11009E85	33k
R143	6-11009E91	56k
R144 thru 200	—	NOT USED
R201, 202 (B)	6-11009B02	150k
R203 (B)	6-11009A63	3.9k
R204 (B)	6-11009A99	120k
R205 (B)	6-11009A97	100k
R206 (B)	6-11009E97	100k
R207 (B)	6-11009A89	47k
R208 (B)	6-11009A97	100k
R209 (B)	6-11009A78	16k
R210 (B)	6-11009A68	6.2k
R211 (B)	6-11009A85	4.7k
R212 (B)	6-11009A81	22k
R213 (B)	6-11009A57	2.2k
R214 (B)	6-11009A97	10

R2 AUDIO AND SQUELCH MODULES

MODELS TRN9690A, 91A



- NOTES:
- Unless otherwise indicated, resistors in ohms, capacitors in microfarads.
 - Refer to jumper table for usage.
 - System adjustment procedure:
 - Apply 1 mV rms of received frequency, modulated with a 1 kHz tone ± 3 kHz deviation, to the receiver 2 RF input.
 - Install JU2. Set R3 for 380 mV rms at pin 8-R2 disc input. Remove JU2.
 - Set R7 for 150 mV rms at pin 17-R2 audio input.

Jumper Table

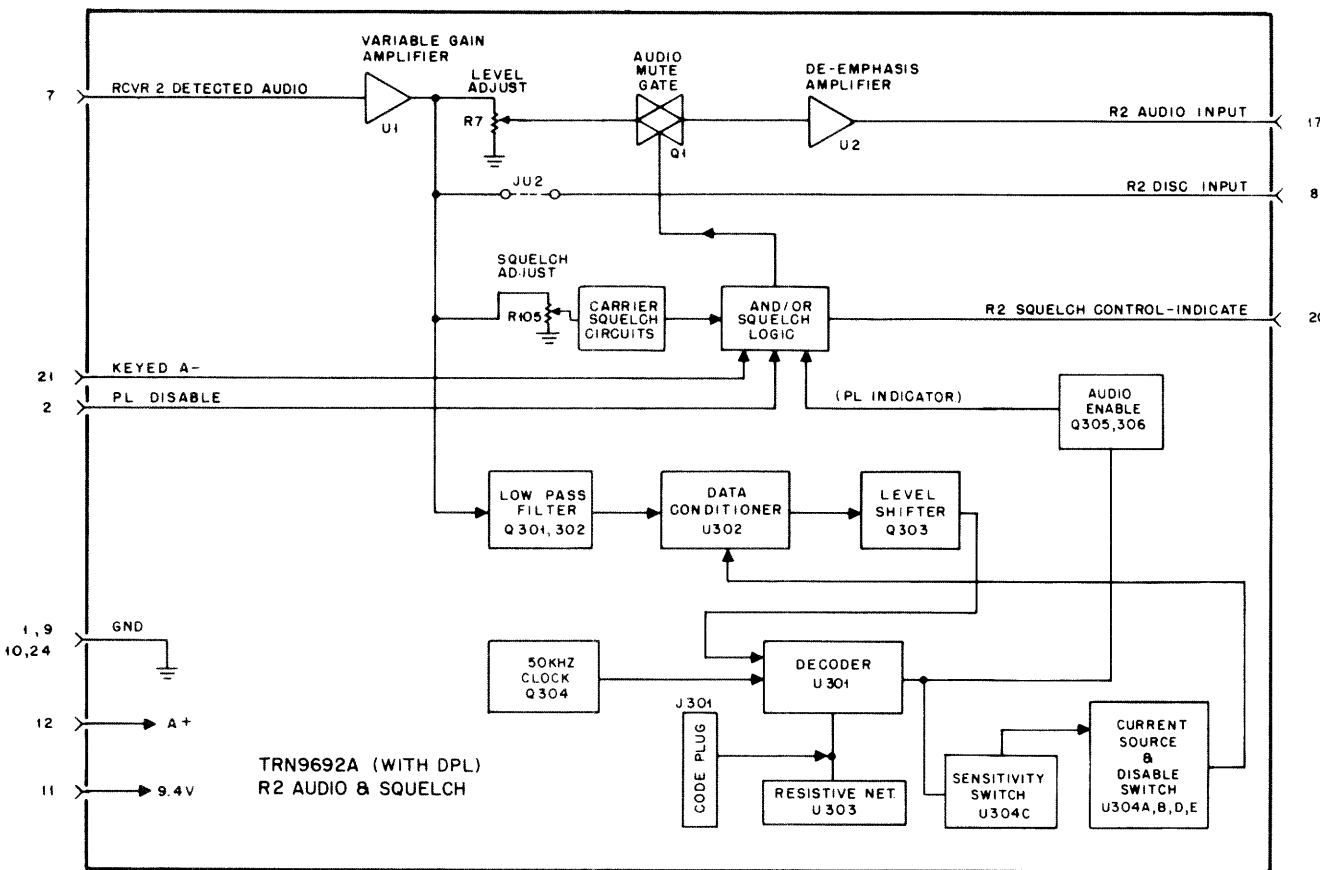
Jumper	IN	OUT
JU1	For Carrier Squelch	For PL Squelch
JU2	For Factory Test	Normally
JU101	Normally	For PL "AND" Squelch
JU102	Normally	For Carrier Squelch
JU201	Normally	When using 67 Hz Reed

TRN9690A (Carrier Only), 91A (With PL),
R2 Audio & Squelch Modules
Schematic Diagram
Motorola No. PEPS-41743-A
(Sheet 2 of 2)
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R2 AUDIO & SQUELCH MODULES

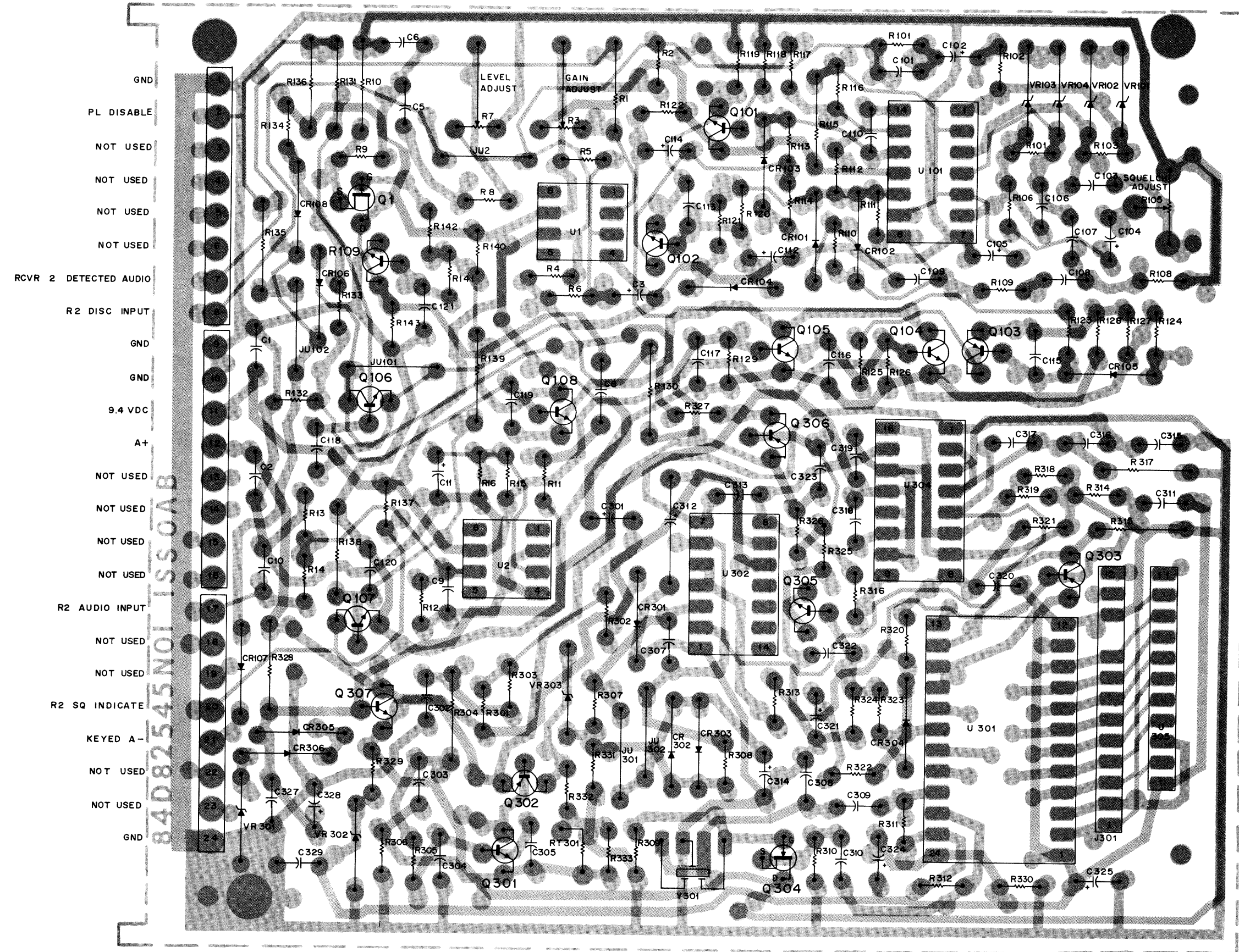
R2 AUDIO AND SQUELCH MODULE

MODEL TRN9692A



CEPS-41771-0

TRN9692A (with DPL)
R2 Audio & Squelch Module
Block Diagram, Circuit Board Detail, and Parts List
Motorola No. PEPS-41744-B
(Sheet 1 of 2)
5/11/86-UP



SHOWN FROM SOLDER SIDE

COMPONENT SIDE ● BD-DEPS-34539-0
SOLDER SIDE ○ BD-DEPS-34538-0
OL-DEPS-34540-B

parts list

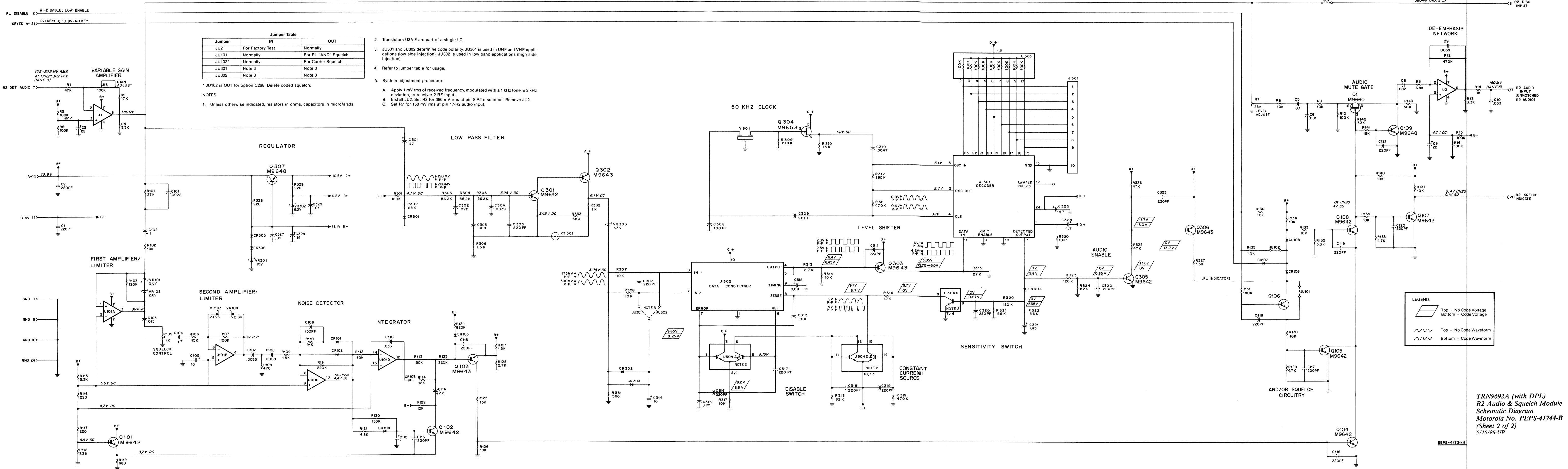
TRN9692A R2 Audio and Squelch with DPL Module PL9671-B

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
C1, 2	21-11015B05	capacitor, fixed: uF ± 5%; 50 V; unless otherwise stated
C3	23-11019A27	22 pF ± 20%; 25 V
C4	—	NOT USED
C5	8-11017A17	0.1
C6	8-11017B01	.001
C7	—	NOT USED
C8	8-84637L36	.002; 100 V
C9	8-11017A18	.0039
C10	8-11017A13	.033
C11	23-11019A27	22 ± 20%; 25 V
C12 thru 100	—	NOT USED
C101	8-11017A03	.0022
C102	23-11019A09	1 ± 20%
C103	8-11017A09	.015
C104	23-11019A09	1 ± 20%
C105	23-11019A20	10 ± 20%; 25 V
C106	—	NOT USED
C107	8-11017A05	.0033
C108	8-11017A07	.0068
C109	21-11022G59	100 pF
C110	8-11017A13	.033
C112	23-11019A09	1 ± 20%
C113	21-11015B05	220 pF ± 10%; 100 V
C114	23-11019A11	2.2 ± 20%
C115 thru 121	21-11015B05	220 pF ± 10%; 100 V
C122 thru 300	—	NOT USED
C301	23-84612M20	47 ± 10%; 25 V
C302	8-11017A11	.022
C303	8-11017A16	.068
C304	8-11017A18	.0039
C305	21-11015B05	220 pF ± 10%; 100 V
C306	—	NOT USED
C307	21-11015B05	220 pF ± 10%; 100 V
C308	21-11022A55	100 pF
C309	21-11022A37	20 pF
C310	21-11021A21	.0047 ± 10%
C311	21-11015B05	220 pF ± 10%; 100 V
C312	23-82783B48	0.68; 35 V
C313	21-11015B13	.001 ± 10%; 100 V
C314	23-84612M18	10 ± 10%; 25 V
C315	21-11015B13	.001 ± 10%; 100 V
C316 thru 320	21-11015B05	220 pF ± 10%; 100 V
C321	23-84612M17	6.8 ± 10%; 25 V
C322, 323	21-11015B05	220 pF ± 10%; 100 V
C324, 325	23-11019A16	4.7 ± 20%; 35 V
C326	—	NOT USED
C327	21-11021F04	0.1 ± 20%
C328	23-84612M19	15 ± 10%; 25 V
C329	21-11021F04	.01 ± 20%
CR101 thru 108	48-83654H01	diode: (see note) silicon
CR109 thru 300	—	NOT USED
CR301	48-83654H02	silicon
CR302, 303	48-84616A01	hot carrier
CR304, 305, 306	48-83654H01	silicon
J301	9-82071K01	connector, receptacle: female; 12-contact (DPL plug)
JU2	42-11060A01	jumper: 0 ohms
JU3 thru 100	—	NOT USED
JU101, 102	42-11060A01	0 ohms
JU103 thru 300	—	NOT USED
JU301, 302	42-11060A01	0 ohms
Q1	48-869660	transistor: (see note) FET, p-channel; type M9660
Q2 thru 100	—	NOT USED
Q101, 102	48-869642	NPN; type M9642
Q103	48-869643	PNP; type M9643
Q104	48-869642	NPN; type M9642
Q109	48-869648	NPN; type M9648
Q110 thru 300	—	NOT USED
Q301	48-869642	NPN; type M9642
Q302, 303	48-869643	PNP; type M9643
Q304	48-869653	FET, N-channel; type M9653
Q305	48-869642	NPN; type M9642
Q306	48-869643	PNP; type M9643
Q307	48-869648	NPN; type M9648
R1	6-11009A89	resistor, fixed: ± 5%; 1/4 W; unless otherwise stated
R2	6-11009E89	47k
R3	18-82374N02	variable; 100k
R4	6-11009E61	3.3k
R5, 6	6-11009E97	100k
R7	18-82374N01	variable; 25k
R8, 9	6-11009E73	10k
R10	6-11009A97	100k
R11	6-11009E69	6.8k
R12	6-11009F14	470k
R13	6-11009E61	3.3k
R14	6-11009E49	1k
R15, 16	6-11009E97	100k
R17 thru 100	—	NOT USED
R101	6-11009E83	27k
R102	6-11009E73	10k
R103	5-84220B01	120k
R104	—	NOT USED
R105	18-83083G28	variable; 1k
R106	6-11009E73	10k
R107	6-11009E99	120k
R108	6-11009E41	470
R109	6-11009E53	1.5k
R110	6-11009E96	91k
R111	6-11009F06	220k
R112	6-11009E73	10k
R113	6-11009F02	150k
R114	6-11009E75	12k
R115	6-11009A61	3.3k
R116, 117	6-11009E33	220
R118	6-11009E61	3.3k
R119	6-11009E45	680
R120	6-11009F02	150k
R121	6-11009E69	6.8k
R122	6-11009E73	10k
R123	6-11009F06	220k
R124	6-11009F20	820k
R125	6-11009E77	15k
R126	6-11009E73	10k
R127	6-11009E53	1.5k
R128	6-11009E59	2.7k
R129	6-11009E65	4.7k
R130	6-11009A73	10k
R131	6-11009B04	180k
R132	6-11009E61	3.3k
R133, 134	6-11009E73	10k
R135	6-11009A53	1.5k
R136	6-11009A73	10k
R137	6-11009E73	10k
R138	6-11009A65	4.7k
R139	6-11009A73	10k
R140	6-11009E73	10k
R141	6-11009E77	15k
R142	6-11009E85	33k
R143	6-11009E91	56k
R144 thru 300	—	NOT USED
R301	6-11009E99	120k
R302	6-11009E93	68k
R303, 304, 305	6-10621D64	56.2k ± 1%; 1/8 W
R306	6-11009E53	1.5k
R307, 308	6-11009E73	10k
R309	6-11009F08	270k
R310	6-11009E77	15k
R311	6-11009F14	470k
R312	6-11009F04	180k
R313	6-11009E59	2.7k
R314	6-11009E73	10k
R315	6-11009A83	27k
R316	6-11009E89	47k
R317	6-11009A73	10k
R318	6-11009E95	82k
R319	6-11009F14	470k
R320	6-11009E99	120k
R321, 322	6-11009E91	56k
R323	6-11009E99	120k
R324	6-11009E95	82k
R325, 326	6-11009E89	47k
R327	6-11009E53	1.5k
R328	6-11009A33	220
R329	6-11009E33	220
R330	6-11009E97	100k
R331	6-11009E43	560
R332	6-11009E49	1k
R333	6-11009E45	680
RT301	6-83241P01	thermistor: 305 @ 25°C
U1, 2	51-80067C02	integrated circuit: (see note) single op-amplifier
U3 thru 100	—	NOT USED
U101	51-83629M06	op-amplifier
U102 thru 300	—	NOT USED
U301	51-80074C01	encoder/decoder
U302	51-83629M01	phase lock loop
U303	51-82142K02	resistor network
U304	51-83629M10	transistor array
VR101 thru 104	48-82256C33	voltage regulator: Zener type; 2.6 V
VR105 thru 300	—	NOT USED
VR301	48-82256C11	Zener type; 10 V
VR302	48-83696E07	Zener type; 6.2 V
VR303	48-82256C26	Zener type; 3.3 V

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
Y301	48-82003K01	crystal: (see note) 50 kHz
mechanical parts		
	3-84256M01	SCREW, tapping; 4-10 x 5/16"; 2 used
	5-84220B01	GROMMET, 2 used
	9-82071K01	PLUG, socket
	9-83497F01	RECEPTACLE, female; 8-contact; 3 used (circuit board edge connector)
	64-83858N03	PANEL, screened

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

R2 AUDIO AND SQUELCH MODULE MODEL TRN962A

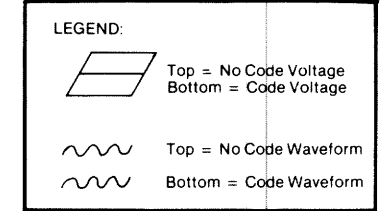


Jumper Table

Jumper	IN	OUT
JU2	For Factory Test	Normally
JU101	Normally	For PL "AND" Squelch
JU102*	Normally	For Carrier Squelch
JU301	Note 3	Note 3
JU302	Note 3	Note 3

* JU102 is OUT for option C268. Delete coded squelch.
NOTES
1. Unless otherwise indicated, resistors in ohms, capacitors in microfarads.

- Transistors U3A-E are part of a single I.C.
- JU301 and JU302 determine code polarity. JU301 is used in UHF and VHF applications (low side injection). JU302 is used in low band applications (high side injection).
- Refer to jumper table for usage.
- System adjustment procedure:
A. Apply 1 mV rms of received frequency, modulated with a 1 kHz tone ± 3 kHz deviation, to receiver 2 RF input.
B. Install JU2. Set R3 for 380 mV rms at pin 8-R2 disc input. Remove JU2.
C. Set R7 for 150 mV rms at pin 17-R2 audio input.



TRN962A (with DPL)
R2 Audio & Squelch Module
Schematic Diagram
Motorola No. PEPS-41744-B
(Sheet 2 of 2)
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R2 AUDIO & SQUELCH MODELS

MODELS TRN5070A, 71A, 72A

Model Table

Model	Description
TRN5070A	With Carrier Squelch
TRN5071A	With Carrier & PL Squelch
TRN5072A	With Carrier & DPL Squelch

1. GENERAL

1.1 PHYSICAL DESCRIPTION

The TRN5070A, 71A, and 72A R2 Audio & Squelch Modules are plug-in modules designed for use with Motorola base and repeater stations. All components and circuitry are mounted on a sturdy circuit card with connecting terminals that mate with the backplane interconnect board of the station's RF Control Chassis. These modules are used only with two receiver stations.

1.2 FUNCTIONAL DESCRIPTION

Each of these modules function as an audio amplifier between the second receiver's detector output and the line driver module. They also can perform a carrier squelch function for the second receiver. Additionally, Model TRN5071A can perform a PL squelch function, and Model TRN5072A can perform a DPL squelch function.

The second receiver detector circuit feeds an audio signal to the R2 Audio & Squelch Module for amplification (U1), input to the carrier squelch circuitry, and output to the line driver module (pin 17). The line driver module returns audio to the R1 audio & squelch module (pin 18) for amplification and output to a local speaker (pin 22). The on-board squelch circuitry operates from rf carrier, coded squelch, or a combination of carrier and coded squelch.

2. DETAILED THEORY OF OPERATION

(Refer to the functional block and schematic diagrams attached to this instruction section.)

2.1 VARIABLE GAIN AMPLIFIER CIRCUIT

The gain of U1 is adjustable by means of gain adjust R3. The gain is adjusted to provide a nominal voltage

(380 mV rms) to the squelch circuit input (U101A-1). U1 also supplies receiver audio to possible on-board PL or DPL circuitry, and level adjust R7. The output of R7 drives audio mute gate Q1. If the station is equipped with tone PL, JU1 is cut. When JU1 is cut, the R2 DET AUDIO signal is routed through an on-board PL filter, and then applied to Q1.

2.2 AUDIO MUTE GATE CIRCUIT

Q1 is a P-Channel Field Effect Transistor (FET). With a logic low control voltage, the FET is placed in the ON state. When in the ON state, audio mute gate Q1 will supply audio to de-emphasis amplifier U2. When the control voltage is switched to a logic high, the gate is placed in the OFF (high impedance) state. In this condition, the audio signal is muted.

2.3 DE-EMPHASIS AMPLIFIER CIRCUIT

De-emphasis amplifier U2 amplifies the low level signal to provide the drive necessary for proper line driver operation. Feedback elements C9 and R12 also provide 6 dB per octave de-emphasis. Additional frequency response shaping is provided by the combination of C8 & R11, and R14 (on TRN5070A, 71A), or C8 & R11, and C10 & R14 (on TRN5072A).

2.4 NOISE ACTIVATED (CARRIER) SQUELCH CIRCUIT

2.4.1 Squelch Input Circuitry

The input to first amplifier/limiter U101A is a pre-emphasis network. This circuit boosts the noise content of the input signals above 5 kHz, for squelch processing the first amplifier/limiter is driven into limit to prevent audio signals from squelching the receiver. The amplified and limited noise signal is sent through a frequency shaping network to SQUELCH control R105.

The squelch control wiper provides signal to second amplifier/limiter U101B. U101B amplifies the noise signal and relimits audio signals to provide further protection against audio signals squelching the receiver. The

output signal of U101B is frequency shaped and sent to noise detector U101C.

2.4.2 Noise Detector and Switching Circuits

Noise detector U101C is a half wave rectifier-amplifier which produces negative going spikes at its output, U101C-10. The average dc value of these spikes is a function of received signal strength. The lowest average dc output voltage corresponds to a no signal input (maximum noise) condition. As the received signal strength increases, the noise level decreases, and the average dc output voltage increases.

The squelch switching circuitry operates in two modes. With a receive signal just above the opening sensitivity, squelch closing is slow (approximately 150 ms), which produces the squelch tail heard at the end of a received message. The 150 ms delay is present to prevent the received message from being chopped during a weak fluttering signal. With a strong signal (approximately 10 dB above opening sensitivity), squelch closing occurs immediately after the end of a received signal. This prevents the squelch tail from being heard.

Active integrator U101D provides squelch opening and slow squelch closing. U101D compares the detector's average dc output voltage with a reference voltage to determine squelch opening and closing.

Fast squelch closing is provided by Q102. A strong signal charges C112 through R120, turning Q102 on. With Q102 on, the collector voltage lowers to approximately 3.9 V dc. At the end of a strong signal, noise spikes from the detector are captured by CR104. This immediately discharges C112, turning off Q102. When Q102 turns off, its collector voltage goes to 9.4 volts, and C114 forces Q103 to close the squelch.

2.5 PRIVATE-LINE TONE CODED SQUELCH CIRCUIT

2.5.1 General

Essentially, the on-board PL decoder circuit of Model TRN5071A R2 Audio & Squelch Module detects a received PL tone and unsquelches the receiver when the proper PL tone is received. In addition, PL tone filtering is provided so that the PL tone is not heard in normal received audio.

Received R2 audio enters the PL circuit as R2 DISC INPUT (from U1-6), and is routed through an active low pass filter (Q201 & 202) before being applied to the input of the tone decoder IC U201-8. When the proper PL tone is decoded, U201 produces a square wave at the decode output (U201-13), unloaded. The square wave is detected by detector switch circuitry (Q204 & 205), which then enables PL INDICATOR output switch (Q206).

PL filter circuitry is utilized (JU1 out) to remove (attenuate) PL tones from the received audio. The received audio is filtered, first by a high pass filter, and then by a notch filter. A gyrator circuit is used for the notch filter to provide high "Q" inductance, without employing inductors.

2.5.2 PL Decoder Circuit Description

NOTE

The decoder IC U201 generates a high PL INDICATOR output (on the collector of Q206) when a proper PL tone is detected.

2.5.2.1 LOW PASS FILTER

The 5-pole low pass filter (Q201 & 202) attenuates high frequency noise above 192.8 Hz from the received R2 DISC INPUT audio. This provides the balance of the decoder circuitry additional falsing and blocking immunity.

2.5.2.2 DECODER AND REED

The filtered PL tone is applied to the decoder tone input (U201-8), where it is amplified and limited. The PL tone is then fed to the decoding reed Z201, pins 2 and 3. If the PL tone is of the proper frequency, it will cause the reed to resonate. The reed secondary (pins 1 and 4) reacts to the sympathetic vibration and returns the PL tone to the decoder reed secondary input U201-11. The decoder then amplifies and limits the PL tone once again, and provides an output at U201-13, Decode Output.

NOTE

If no proper PL tone is detected, the output of U1-13 stays high.

2.5.2.3 DETECTOR SWITCH

When an output is present (indicating a proper PL tone detection) at the decode output of U201 (pin 13), it is waveshaped by capacitor C212 into a sawtooth waveform at a level of approximately 0.8 V p-p. If a high (no detect) is present at U201-13, the level of this same waveform is constant, approximately 2.2 V. The balance of the detector switch circuitry inverts, filters, and amplifies the sawtooth waveform to produce a true logic level (logic high) at the collector of Q206 (PL INDICATOR).

2.5.2.4 NOISE GATE

Noise Gate Q203 allows a small amount of high frequency noise (with 1-pole of low pass filtering) to be fed to the decoder input, U201-8 when the PL INDICATOR output at the collector of Q206 is low. This tends to minimize noise falsing of the decoder. When the PL INDICATOR output is high, the high frequency noise sam-

ple is shunted to ground. This allows the onboard PL circuit to be more sensitive, once it receives a signal, and helps to prevent decoder dropout during brief signal fades.

2.5.2.5 8.4 V REGULATOR

The Q207 regulator circuit provides a constant 8.4 V dc (E+) to the PL decoder IC, U201.

2.6 DIGITAL PRIVATE-LINE CODED SQUELCH CIRCUIT

2.6.1 General

Essentially, the on-board DPL decoder circuit of Model TRN5072A R2 Audio & Squelch Module detects a received DPL code, and unmutes the receiver when the proper code is received. Received R2 audio enters the DPL circuit as R2 DISC INPUT (from U1-6), and is routed through an active low pass filter (Q301 & 302), where frequencies above the DPL code range are attenuated. The output of the low pass filter is applied to phase-lock-loop (PLL) data conditioner U302, which squares the shape of the incoming code word. The output of the data conditioner is routed, via level shifter Q303, to the input of the decoder IC U301-11.

The decoder circuit consists of IC U301, a 50 kHz clock (Y301 & Q304), and the information stored in the code plug (J301). When the proper code has been detected, the decoder provides a logic high at U301-7. That high provides a logic low, via audio enable Q305, to enable the PL INDICATOR output switch (Q306).

The logic high at U301-7 is also applied to sensitivity switch U304C, to disable the constant current source of U304D-U304E. With the constant current source disabled, the voltage at U302-8 is lowered, causing the sensitivity of U302 to increase. This provides additional immunity to audio interference and improved squaring of the incoming code word.

When the incoming (received) signal ceases, the sending transmitter produces a turn-off code. When the turn-off code is detected by the decoder, the detected output at U301-7 switches low. This decreases the sensitivity of the data conditioner and causes receiver audio to be muted.

2.6.2 DPL Decoder Circuit Description

NOTE

The decoder IC U301 generates a high (PL INDICATOR) output on the collector of Q206 when a proper DPL code is detected.

2.6.2.1 LOW PASS FILTER

The low pass filter circuit is similar to the one previously described for the PL decoder circuit in this section. However, the filter's output is fed through a PLL data conditioner (U302) for waveshaping, and a level shifter (Q303) to properly process the incoming code word, before presenting it to the decoder (U301) circuitry.

2.6.2.2 DECODER AND CODE PLUG

The processed code word is applied to the decoder's data input (U301-11), where it is compared to the data stored in the code plug (J301), at a 50 kHz rate. If the incoming code word is correct, U301 will provide a logic high at the decoder's detected output U301-7.

NOTE

If no proper code word is detected, the output of U301-7 stays low.

2.6.2.3 AUDIO ENABLE

When a high output is present at U301-7 (indicating a proper DPL code detection), it is inverted by Q305 to enable Q306. Output switch Q306 then produces a true logic level (logic high) at its collector (PL INDICATOR).

2.6.2.4 REGULATOR CIRCUIT

Regulator Q307 provides three regulated dc voltages from station A+ (13.9 V). These voltages, in addition to A+, power all circuitry in the DPL decoder section of the module. The regulated voltages are:

10.5 V (C+), 6.2 V (D+), and 11.1 V (E+).

2.7 AND-OR SQUELCH LOGIC CIRCUITRY

The squelch logic circuitry performs the necessary switching functions to provide proper squelch operation. This circuitry can operate in one of three different modes by selecting proper jumper cuts. Refer to the jumper table on the schematic diagram. First, for noise activated squelch operation only, JU102 is cut. In this mode, Q107 is always turned on. Squelching is controlled by the squelch noise circuit, through Q104. For coded (PL or DPL) squelch activation, both JU101 and JU102 remain in. In this mode, squelch turn-on is controlled by a proper coded squelch detection only. A proper coded squelch detection pulls the PL INDICATOR line high, turning on Q105 and Q107. Second, when PL DISABLED in this configuration, Q107 is turned on. This allows either a proper coded squelch detection or a noise activated squelch detection to open the squelch. This provides the OR squelch function.

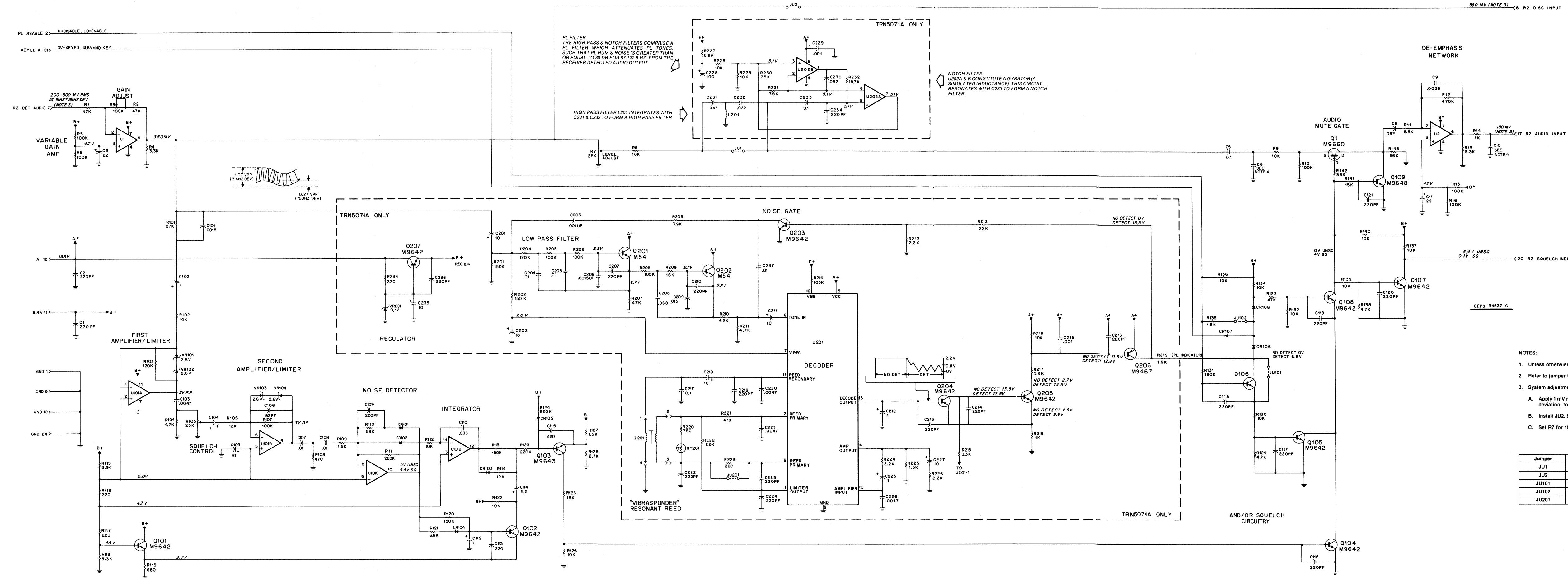
In the third mode of operation, JU101 is cut and JU102 remains in. This produces the AND squelch function.

AND squelch means that both a proper coded squelch detection and a noise activated squelch detection are required to open squelch. A proper coded squelch detection turns on Q107 and a noise activated squelch detection turns on Q104. Both are required to open squelch. When PL DISABLED in this configuration both Q106 and Q107 are turned on. Again, this provides

the OR squelch function, where either a proper coded squelch detection *or* a noise activated squelch detection will open squelch.

With Q107 on, and either Q104 or Q105 on, Q108 and Q109 are turned off. This enables audio mute gate Q1, creating an open squelch condition.

R2 AUDIO & SQUELCH MODULES
 MODELS TRN5070A (CARRIER ONLY),
 71A (WITH PL)



- NOTES:
1. Unless otherwise indicated, resistors in ohms, capacitors in microfarads.
 2. Refer to jumper table for usage.
 3. System adjustment procedure:
 - A. Apply 1 mV rms of received frequency, modulated with a 1 kHz tone ± 3 kHz deviation, to the receiver 2 RF input.
 - B. Install JU2. Set R4 for 380 mV rms at pin 8-R2 disc input. Remove JU2.
 - C. Set R7 for 150 mV rms at pin 17-R2 audio input.

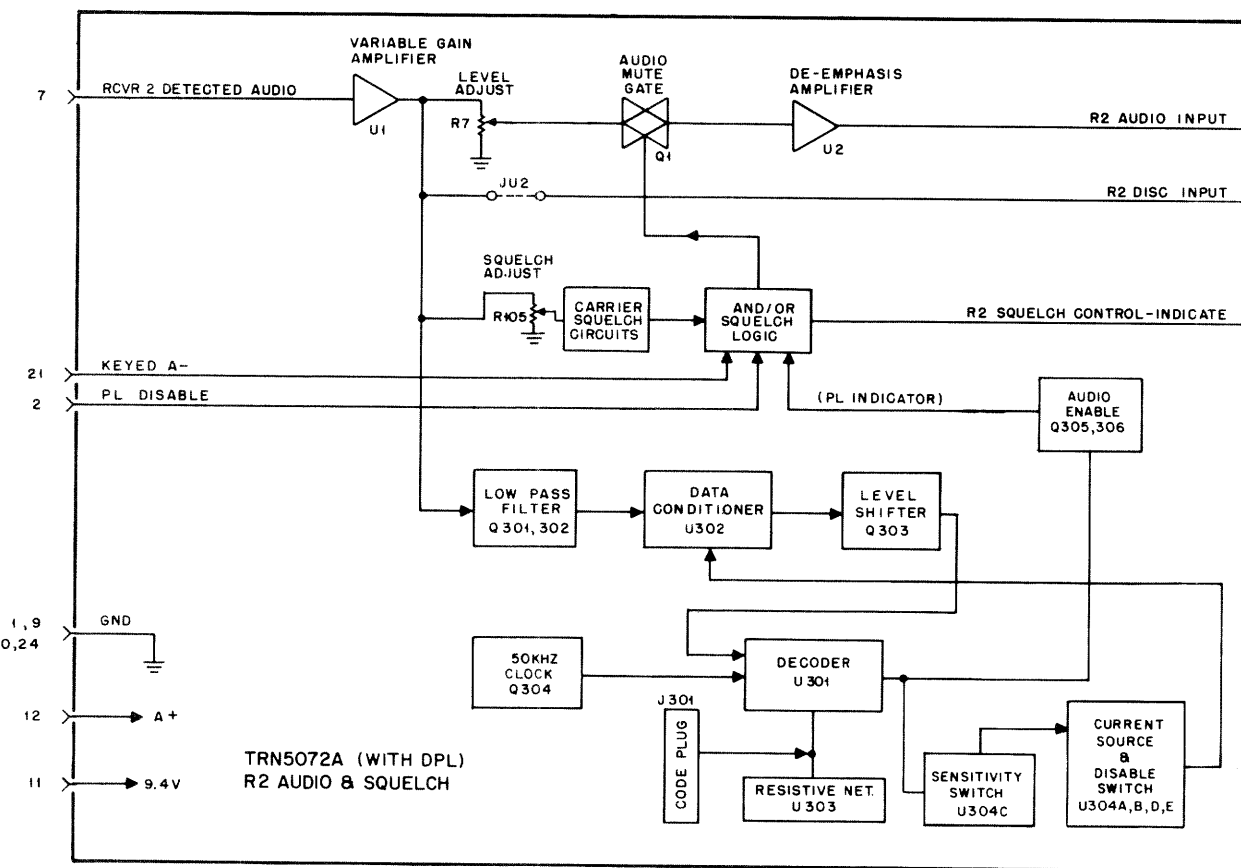
Jumper Table

Jumper	IN	OUT
JU1	For Carrier Squelch	For PL Squelch
JU2	For Factory Test	Normally
JU101	Normally	For PL "AND" Squelch
JU102	Normally	For Carrier Squelch
JU201	Normally	When using 67 Hz Reed

Schematic Diagram
 Motorola No. PEPS-34957-C
 (Sheet 2 of 2)
 11/1/85-UP

R2 AUDIO & SQUELCH MODULE

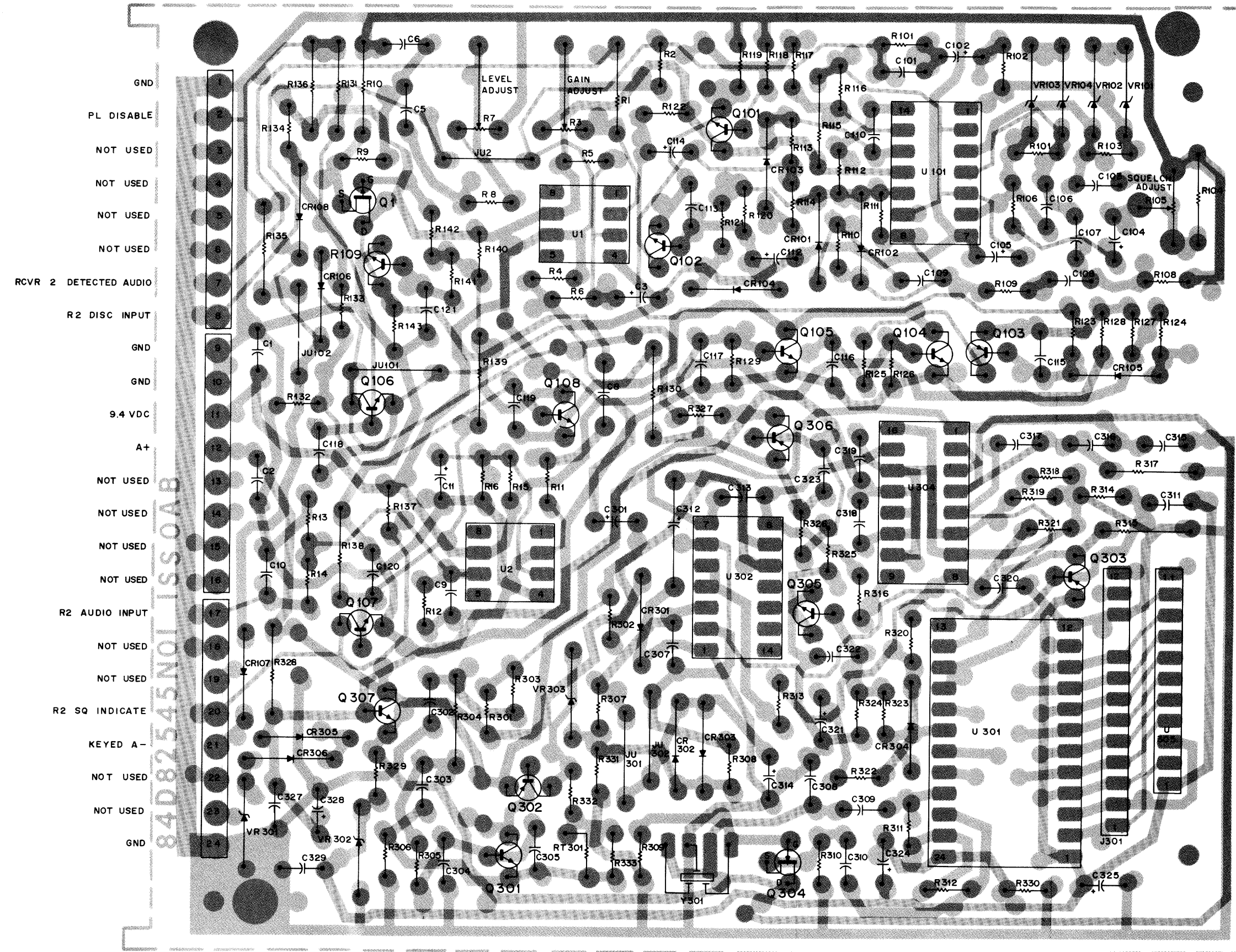
MODEL TRN5072A (WITH DPL)



CEPS-34838-0

Block Diagram, Circuit Board Detail, and Parts List
Motorola No. PEPS-34958-C
(Sheet 1 of 2)

11/1/85-UP



COMPONENT SIDE Ⓢ BD-DEPS-34539-0
SOLDER SIDE Ⓢ BD-DEPS-34538-0
OL-DEPS-34540-A

parts list

TRN5072A R2 Audio and Squelch with DPL Module PL-7953-C

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
C1, 2	21-11015B05	capacitor, fixed; uF ± 5%; 50 V; unless otherwise stated
C3	23-11019A27	220 pF ± 20%; 100 V
C4	—	NOT USED
C5	8-11017A17	0.1
C6	8-11017B01	.001
C7	—	NOT USED
C8	8-84637L36	.082, 100 V
C9	8-11017A18	.0039
C10	8-11017A13	.033
C11	23-11019A27	22 ± 20%; 25 V
C12 thru 100	—	NOT USED
C101	8-11017B02	.0015 ± 10%
C102	23-11019A09	.0047 ± 10%
C103	8-11017B06	.0047
C104	23-11019A09	1 ± 20%
C105	23-11019A20	10 ± 20%; 25 V
C106	21-11014B47	82 pF; 100 V
C107	8-11017B06	.0047 ± 10%
C108	8-11017B08	.01 ± 10%
C109	21-11015B05	220 pF ± 10%; 100 V
C110	8-11017A13	.033
C111	23-11019A09	1 ± 20%
C112	21-11015B05	220 pF ± 10%; 100 V
C113	21-11015B05	220 pF ± 10%; 100 V
C114	23-11019A11	2.2 ± 20%
C115 thru 121	21-11015B05	220 pF ± 10%; 100 V
C122 thru 300	—	NOT USED
C301	23-84612M20	47 ± 10%; 25 V
C302	8-11017A11	.022
C303	8-11017A16	.068
C304	8-11017A18	.0039
C305	21-11015B05	220 pF ± 10%; 100 V
C306	—	NOT USED
C307	21-11015B05	220 pF ± 10%; 100 V
C308	21-11022A55	100 pF
C309	21-11022A57	20 pF
C310	21-11021A21	.0047 ± 10%
C311	21-11015B05	220 pF ± 10%; 100 V
C312	23-82783B48	0.68; 35 V
C313	21-11015B13	.001 ± 10%; 100 V
C314	23-84612M18	10 ± 10%; 25 V
C315	21-11015B13	.001 ± 10%; 100 V
C316 thru 320	21-11015B05	220 pF ± 10%; 100 V
C321, 322	23-84612M17	6.8 ± 10%; 25 V
C323	21-11015B05	220 pF ± 10%; 100 V
C324, 325	23-11019A16	4.7 ± 20%; 35 V
C326	—	NOT USED
C327	21-11021F04	.01 ± 20%
C328	23-84612M19	15 ± 10%; 25 V
C329	21-11021F04	.01 ± 20%
CR101 thru 108	48-83654H01	diode; (see note)
CR109 thru 300	—	NOT USED
CR301	48-83654H02	silicon
CR302, 303	48-84616A01	hot carrier
CR304, 305, 306	48-83654H01	silicon
J301	9-82071K01	connector, receptacle; female; 12-contact (DPL plug)
JU2	42-11060A01	0 ohms
JU3 thru 100	—	NOT USED
JU101, 102	42-11060A01	0 ohms
JU103 thru 300	—	NOT USED
JU301, 302	42-11060A01	0 ohms
Q1	48-869660	FET, p-channel; type M9660
Q2 thru 100	—	NOT USED
Q101, 102	48-869642	NPN; type M9642
Q103	48-869643	PNP; type M9643
Q104 thru 108	48-869642	NPN; type M9642
Q109	48-869648	NPN; type M9648
Q110 thru 300	—	NOT USED
Q301	48-869642	NPN; type M9642
Q302, 303	48-869643	PNP; type M9643
Q304	48-869653	FET, N-channel; type M9653
Q305	48-869642	NPN; type M9642
Q306	48-869643	PNP; type M9643
Q307	48-869648	NPN; type M9648
R1, 2	6-11009E89	resistor, fixed; ± 5%; 1/4 W; unless otherwise stated
R3	18-8237AN02	47k
R4	6-11009E81	variable; 100k
R5, 6	6-11009E97	100k
R7	18-8237AN01	variable; 25k
R8, 9	6-11009E73	10k
R10	6-11009A97	100k
R11	6-11009E69	6.8k
R12	6-11009F14	470k
R13	6-11009E61	3.3k
R14	6-11009E49	1k
R15, 16	6-11009E97	100k
VR101 thru 104	48-82256C33	voltage regulator; Zener type; 2.6 V
VR105 thru 300	—	NOT USED
VR301	48-82256C11	Zener type; 10 V
VR302	48-8369E07	Zener type; 6.2 V
VR303	48-82256C03	Zener type; 4.7 V
Y301	48-82003K01	crystal; (see note) 50 kHz
mechanical parts		
3-84256M01	5-84220B01	SCREW, tapping; 4-10 x 5/16"; 2 used
5-84220B01	—	GROMMET, 2 used

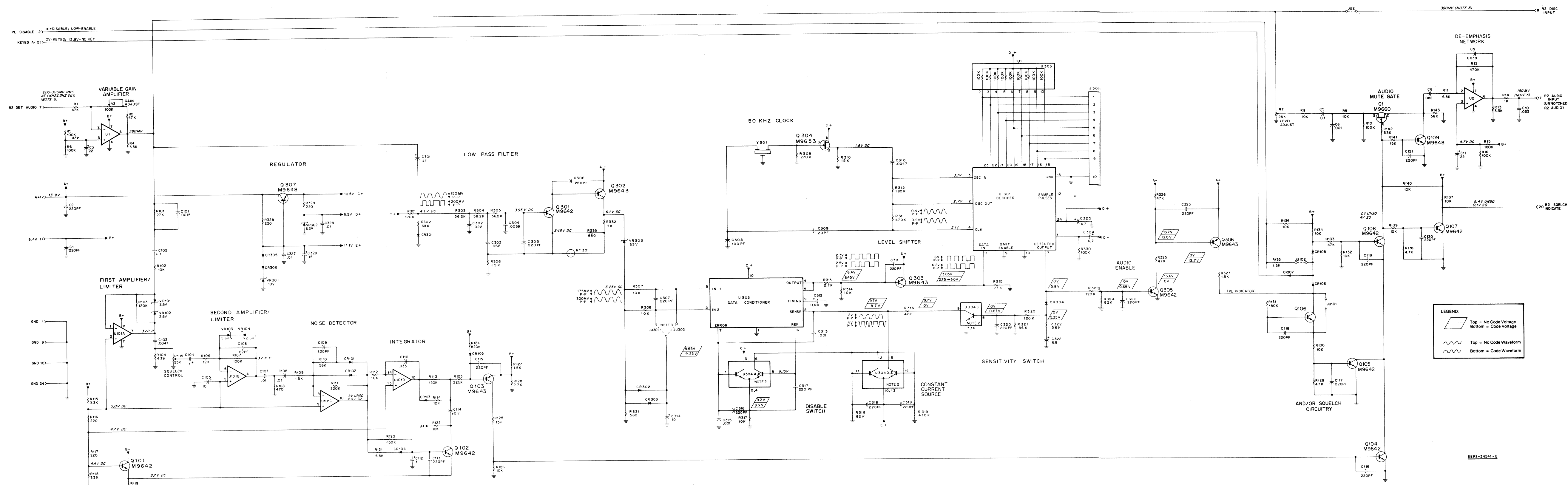
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
R17 thru 100	—	NOT USED
R101	6-11009E83	27k
R102	6-11009E73	10k
R103	6-11009E99	120k
R104	6-11009A65	4.7k
R105	6-11009A65	variable; 25k
R106	6-11009E75	12k
R107	6-11009E97	100k
R108	6-11009E41	470
R109	6-11009E53	1.5k
R110	6-11009E91	50k
R111	6-11009F06	220k
R112	6-11009E73	10k
R113	6-11009F02	150k
R114	6-11009E75	12k
R115	6-11009A61	3.3k
R116, 117	6-11009E33	220
R118	6-11009E61	3.3k
R119	6-11009E45	680
R120	6-11009F02	150k
R121	6-11009E69	6.8k
R122	6-11009E73	10k
R123	6-11009F06	220k
R124	6-11009F20	820k
R125	6-11009E77	15k
R126	6-11009E73	10k
R127	6-11009E53	1.5k
R128	6-11009E59	2.7k
R129	6-11009E85	4.7k
R130	6-11009A73	10k
R131	6-11009B04	180k
R132	6-11009E61	3.3k
R133, 134	6-11009E73	10k
R135	6-11009A53	1.5k
R136	6-11009A73	10k
R137	6-11009E73	10k
R138	6-11009A65	4.7k
R139	6-11009A73	10k
R140	6-11009E73	10k
R141	6-11009E77	15k
R142	6-11009E85	33k
R143	6-11009E91	56k
R144 thru 300	—	NOT USED
R301	6-11009E99	120k
R302	6-11009E83	68k
R303, 304, 305	6-10621D64	56.2k ± 1%; 1/8 W
R306	6-11009E53	1.5k
R307, 308	6-11009E73	10k
R309	6-11009F08	270k
R310	6-11009E77	15k
R311	6-11009F14	470k
R312	6-11009F04	180k
R313	6-11009E59	2.7k
R314	6-11009E73	10k
R315	6-11009A83	27k
R316	6-11009E89	47k
R317	6-11009A73	10k
R318	6-11009E85	82k
R319	6-11009F14	470k
R320	6-11009E99	120k
R321, 322	6-11009E91	56k
R323	6-11009E99	120k
R324	6-11009E85	82k
R325, 326	6-11009E89	47k
R327	6-11009E53	1.5k
R328	6-11009A33	220
R329	6-11009E33	220
R330	6-11009E97	100k
R331	6-11009E43	560
R332	6-11009E49	1k
R333	6-11009E45	680
RT301	6-83241P01	thermistor; 300 @ 25°C
U1, 2	51-80067C02	integrated circuit; (see note) single op-amplifier
U3 thru 100	—	NOT USED
U101	51-83629M06	op-amplifier
U102 thru 300	—	NOT USED
U301	51-80074C01	encoder/decoder
U302	51-83629M01	phase lock loop
U303	51-82142K02	resistor network
U304	51-83629M10	transistor array

revisions

CHASSIS AND SUFFIX NO.	REF. SYMBOL	CHANGE	LOCATION
C111	OMITTED	21-11015B05; 200 pF ± 10%; 100 V	

SHOWN FROM SOLDER SIDE

R2 AUDIO & SQUELCH MODULE MODEL TRN5072A (WITH DPL)



Jumper Table

Jumper	IN	OUT
JU2	For Factory Test	Normally
JU101	Normally	For PL "AND" Squelch
JU102	Normally	For Carrier Squelch
JU301	Note 3	Note 3
JU302	Note 3	Note 3

- NOTES**
- Unless otherwise indicated, resistors in ohms, capacitors in microfarads.
 - Transistors U3A-E are part of a single I.C.
 - JU301 and JU302 determine code polarity. JU301 is used in UHF and VHF applications (low side injection). JU302 is used in low band applications (high side injection).
 - Refer to jumper table for usage.
 - System adjustment procedure:
 - Apply 1 mV rms of received frequency, modulated with a 1 kHz tone \pm 3 kHz deviation, to receiver 2 RF input.
 - Install JU2. Set R4 for 380 mV rms at pin 8-R2 disc input. Remove JU2.
 - Set R7 for 150 mV rms at pin 17-R2 audio input.

Schematic Diagram
Motorola No. PEPS-34958-C
(Sheet 2 of 2)
11/1/85-UP



Model Table

Model	Description
TRN5073A	Duplex (T _{ARB})
TRN5074A	Simplex (T _{ARA})
TRN5075A	Simplex (T _{ARB})

1. DESCRIPTION

The TRN5073A/74A/75A Tone *Private-Line* (PL) Encoder-Decoder Modules are plug-in modules designed for use with Motorola base and repeater stations. All components and circuitry are mounted on a sturdy circuit card with connecting terminals that mate with the backplane interconnect board of the station's rf control chassis. These modules are used with the following types of stations: Simplex T_{ARA} and T_{ARB} and Duplex T_{ARB}.

NOTE

T_{ARA} means that the PL encoder-decoder module employs the same PL code (one reed used) for transmit and receive. T_{ARB} means that the PL encoder-decoder module employs a different PL code for transmit and receive (two reeds used).

2. FUNCTIONS

Each of these modules encodes and decodes *Private-Line* tones. The encoder modulates the transmitter and delays transmitter turn-off 180 ms to allow transmission of a turn-off reverse tone burst. The decoder detects a received PL tone and unquelsches the receiver when the proper PL tone is received. In addition, PL tone filtering is provided so that the PL tone is not heard in normal received audio.

3. FUNCTIONAL OPERATION

Refer to the functional block and schematic diagrams attached to this instruction section.

3.1 SIMPLEX T_{ARA} AND T_{ARB} PL MODULES

The T_{ARA} PL module incorporates one integrated circuit (U1) and one resonant reed (Z1) for both encoding and decoding purposes. Similarly, the T_{ARB} PL module also incorporates one integrated circuit (U1), but uses two resonant reeds (Z1 and Z2) which allows the user to receive on one PL code and transmit on a different PL code. Other than these differences both modules function identically.

In the decode (receive) mode, received audio enters the PL module at the R1 DISC INPUT (pin 17), and is routed through an active low pass filter (Q1 and Q2) before being applied to the input of the tone decoder-encoder IC U1-8. When the proper PL tone is decoded, U1 produces a square wave at the decode output (pin 13) of U1, unloaded. The square wave is detected by detector switch circuitry (Q4 and Q5), which then enables PL INDICATOR output switch (Q6).

In the encode (transmit) mode, U1 (or U101) drives the PL reed primary. The code output at U1-3, which is sinusoidal is sampled by AGC circuitry which controls the amount of drive to the primary of the PL reed. By controlling the drive amount to the PL reed, a constant output voltage is present at PL CODE OUT, pin 21.

At the end of a transmission, the loss of KEYED A+ triggers delayed keyed A+ timing circuit U2. U2 now provides delayed keyed A+ for 180 ms, and enables the phase shifter network so that a reverse burst (a phase shifted version of the PL tone) can be transmitted. Reverse burst causes the on-channel PL receivers to squelch rapidly.

PL filter circuitry is utilized to remove (attenuate) PL tones from the received audio. The received audio is filtered, first by a high pass filter, and then by a notch filter. Gyrator circuits are used to provide high "Q" inductance, without employing inductors.

3.2 DUPLEX T_AR_B PL MODULE

This module is essentially the same as the simplex versions, except that it permits the user to decode (receive) and encode (transmit) simultaneously. In addition, the encode and decode codes may be different. This is accomplished by using two PL reeds, and two integrated circuits U1 and U101. In this configuration, one reed and one IC are dedicated for decoding purposes, while the other reed and IC are dedicated for encoding purposes.

4. DECODER CIRCUIT DESCRIPTION

NOTE

The decoder portion of IC U1 generates a high at the PL INDICATOR output (pin 5) when a proper PL tone is detected.

4.1 LOW PASS FILTER

The 5-pole low pass filter attenuates high frequency noise above 192.8 Hz from the audio spectrum. This provides the balance of the decoder circuitry additional falsing and blocking immunity.

4.2 DECODER AND REED

The filtered PL tone is applied to the decoder tone input (U1-8) where it is amplified and limited. The PL tone is then fed to the decoding reed (Z1 for T_AR_A and Z2 for T_AR_B on Duplex applications), pins 2 and 3. If the PL tone is of the proper frequency, it will cause the reed to resonate. The reed secondary (pins 1 and 4) reacts to the sympathetic vibration and returns the PL tone to the decoder reed secondary input U1-11. The decoder now amplifies and limits the PL tone again, and provides an output at U1-13, Decode Output.

NOTE

If no PL tone is detected, the output of U1-13 is high.

4.3 DETECTOR SWITCH

When an output is present (indicating a proper PL tone detection) at the decode output of U1 (pin 13), it is waveshaped by capacitor C14 into a sawtooth waveform at a level of approximately 0.8 V p-p. If a high (no detect) is present at U1-13, the level of this same waveform is constant, approximately 2.2 V. The balance of the detector switch circuitry inverts, filters, and amplifies the sawtooth waveform (or high) to produce a true logic level at the PL INDICATOR output at pin 5 of the PL module.

4.4 NOISE GATE

Noise Gate Q3, allows a small amount of high frequency noise (with 1-pole of low pass filtering) to be fed to the decoder input, U1-8 when the PL INDICATOR output at pin 5 of the PL module is low. This tends to minimize noise falsing of the decoder. When the PL INDICATOR output is high, the high frequency noise sample is shunted to ground. This allows the PL module to be more sensitive once it receives a signal, and helps to prevent decoder dropout during brief signal fades.

5. ENCODER CIRCUIT DESCRIPTION

NOTE

The encoder portion of U1 (for T_AR_A or T_AR_B applications) or U101 (for Duplex applications), generates a PL tone of the same frequency as that of the resonant PL reed, and produces a PL CODE output at pin 21 of the PL module.

5.1 PL ENCODE SWITCH

The PL Encode Switch (Q8) is normally on unless one of the following conditions exist:

- Keyed A+ (pin 13) or Delayed Keyed A+ (pin 7) is low,
- PL Tone Inhibit (pin 14) is low.

When Q8 is on, the collector of Q9 is high (8.4 V).

5.2 ENCODER AND REED

When the PL Encode Switch is on, U1-16 (Encode Enable) and U1-14 goes high enabling the encoder, which in turn drives encode reed Z1. Encode reed Z1 now vibrates at its own resonant frequency, and U1 then produces a sine wave of the proper frequency at its output (Code Out), U1-3. The code output is fed back to Z1, via Q7 (which controls the drive to Z1) providing an automatic gain control which keeps the encoder output constant.

5.3 DELAYED KEYED A+ TIMING CIRCUIT

When keyed A+ (module pin 13) goes low after being high, U2-3 goes high for 180 ms. The high output of U2-3 causes pin 7 of the PL module to be high for the same time period, producing delayed keyed A+. When keyed A+ goes low, U2-6, 7 (which were low) go high at a rate determined by the RC time constant of R31 and C33.

When the voltage at U2-6, 7 is at the same level as the voltage at U2-5, delayed keyed A + ceases.

5.4 AMPLIFIER AND REVERSE BURST PHASE SHIFTER

When keyed A + is high, Q11 and Q12 are off. The Q13 amplifier circuitry amplifies the PL code output from U1-3 (or U101-3) of the encoder. When keyed A + goes low, delayed keyed A + goes high and turns on Q11 and Q12 which then change the phase of the PL code output (at pin 21 of the module) approximately 240° resulting in an amplified PL reverse burst.

5.5 8.4 V REGULATOR

This circuit provides a constant 8.4 V dc to various points in the PL encode switch circuitry.

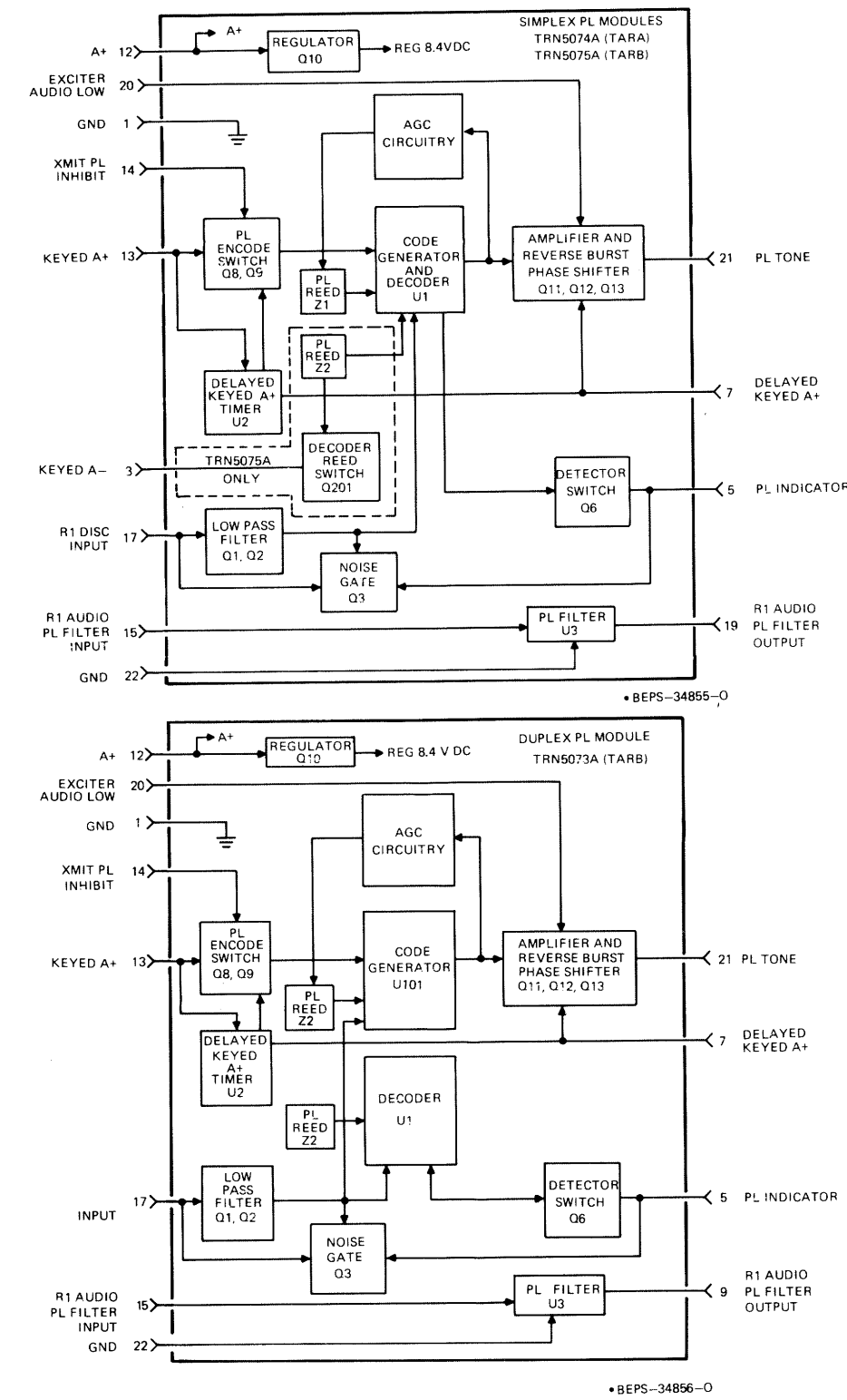
5.6 PL FILTER

The PL filter provides PL tone filtering of receiver detected audio. The filter consists of a 3-pole high pass filter and a 1-pole notch filter. The PL filter incorporates capacitors and gyrator (an active, high "Q" inductance) circuits to provide attenuation of PL frequencies from 67 to 192.8 Hz.

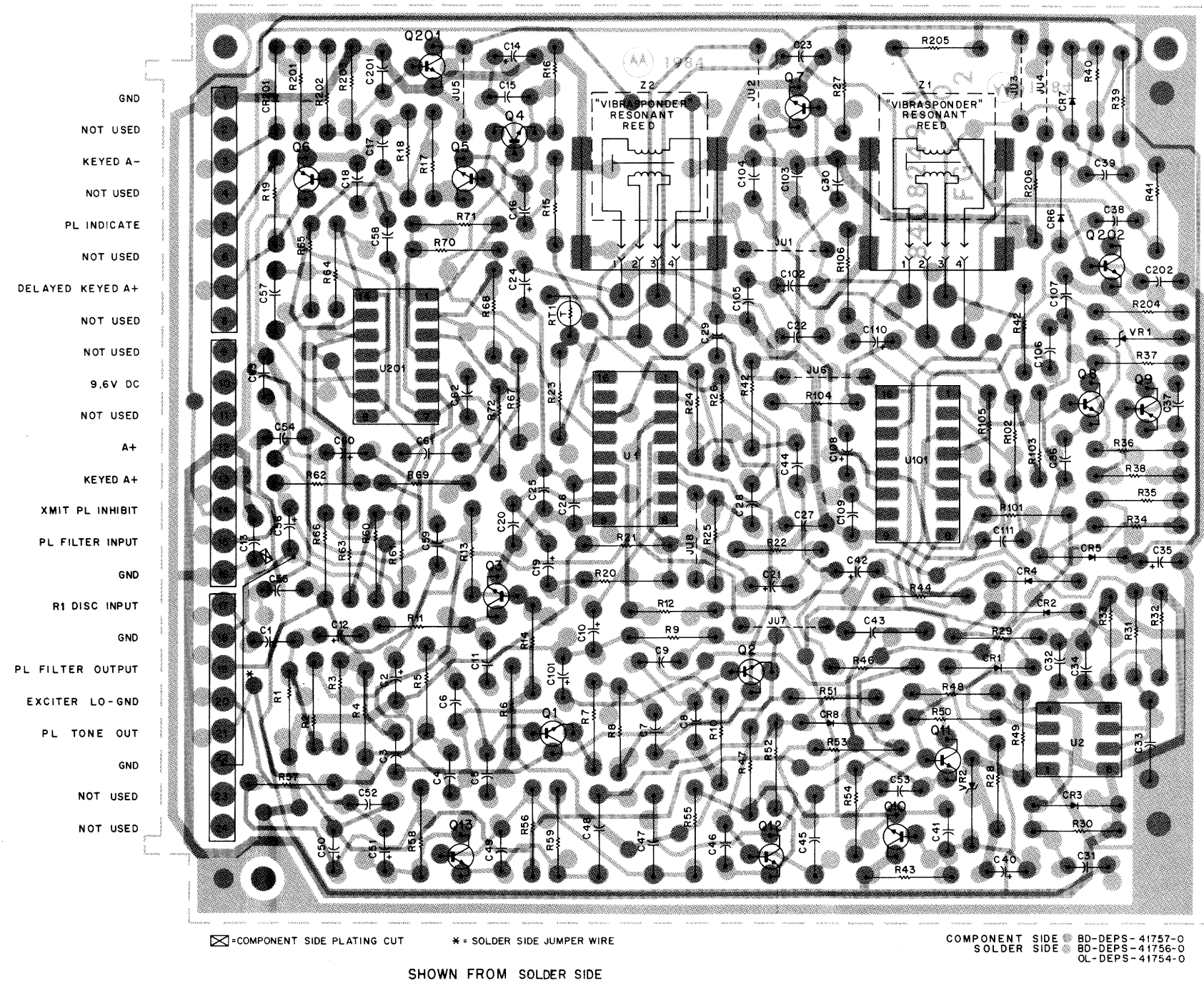
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TONE PRIVATE-LINE ENCODER-DECODER MODULES

MODELS TRN5073A, 74A, 75A



Functional Block Diagrams, Circuit Board Detail and Parts List
Motorola No. PEPS-34857-B
(Sheet 1 of 2)
11/1/85-UP



parts list

This parts list covers 3 models of the PL Encoder-Decoder Modules. Where differences exist, a letter code is added to the reference symbol to indicate the applicable unit.

TRN5073A PL Encoder-Decoder (Duplex TARB) Module
TRN5074A PL Encoder-Decoder (Simplex TARA) Module
TRN5075A PL Encoder-Decoder (Simplex TARB) Module

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
C1, 2	23-11019A20	capacitor, fixed: $\mu F \pm 10\%$; 50 V; unless otherwise stated
C3, 4	8-11017B08	10 $\pm 20\%$; 25 V
C5	8-11017B02	.0015
C6	21-11015B05	220 pF; 100 V
C7	8-11017B16	.068
C8	8-11017B09	.015
C9	21-11015B05	220 pF; 100 V
C10	23-11019A20	10 $\pm 20\%$; 25 V
C11	8-11017B08	.01
C12	8-11017B01	.001
C13	21-11015B05	220 pF; 100 V
C14	23-84612M09	1
C15, 16	21-11015B05	220 pF; 100 V
C17	8-11017B01	.001
C18	21-11015B05	220 pF; 100 V
C19	23-11019A09	1
C20	8-11017B06	.0047
C21	23-11019A20	10 $\pm 20\%$; 25 V
C22	8-11017B17	0.1
C23	21-11015B05	220 pF; 100 V
C24	23-11019A20	10 $\pm 20\%$; 25 V
C25	21-11015B05	220 pF; 100 V
C26, 27	8-11017B06	.0047
C28, 29, 30	21-11015B05	220 pF; 100 V
C31	23-11019A09	1
C32	8-11017B08	.01
C33	8-84637L15	0.27 $\pm 5\%$; 100 V
C34	8-11017B08	.01
C35	23-11019A20	10 $\pm 20\%$; 25 V
C36, 37, 38	21-11015B05	220 pF; 100 V
C39	23-84612M19	15; 25 V
C40	23-11019A20	10 $\pm 20\%$; 25 V
C41	21-11015B05	220 pF; 100 V
C42	23-11019A20	10 $\pm 20\%$; 25 V
C43	8-84637L22	0.22; 100 V
C44	8-11017B17	0.1
C45	8-84637L15	0.27 $\pm 5\%$; 100 V
C46	21-11015B05	220 pF; 100 V
C47, 48	8-84637L15	0.27 $\pm 5\%$; 100 V
C49	21-11015B05	220 pF; 100 V
C50, 51	23-11019A20	10 $\pm 20\%$; 25 V
C52	8-11017B06	.0047
C53	21-11015B05	220 pF
C54	8-11017A09	.015 $\pm 5\%$
C55	8-11017A11	.022 $\pm 5\%$
C56	23-11019A46	100 $\pm 20\%$; 25 V
C57	8-84637L36	.082 $\pm 5\%$; 100 V
C58	21-11015B05	220 pF; 100 V
C59	8-11017A17	0.1
C60	23-11019A46	100 $\pm 20\%$; 25 V
C61	8-84637L36	.082 $\pm 5\%$; 100 V
C62	21-11015B05	220 pF; 100 V
C63	8-11017B08	.01
C64 thru 100	NOT USED	
C101, 102 (A)	23-11019A20	10 $\pm 20\%$; 25 V
C103 (A)	8-11017B17	0.1
C104 (A)	21-11015B05	220 pF; 100 V
C105 (A)	8-11017B06	.0047
C106, 107 (A)	21-11015B05	220 pF; 100 V
C108 (A)	23-11019A09	1
C109 (A)	8-11017B06	.0047
C110 (A)	23-11019A20	10 $\pm 20\%$; 25 V
C111 (A)	8-11017B06	.0047
C112 thru 200	NOT USED	
C201 (C)	21-11015B05	220 pF; 100 V
C202 (B, C)	21-11015B05	220 pF; 100 V
CR1 thru 8	48-83654H01	diode (see note)
CR9 thru 200	NOT USED	
CR201 (C)	48-83654H01	silicon
JU1, 2 (B, C)	42-11060A01	jumper: 0 ohms
JU3 (B)	42-11060A01	0 ohms
JU4 (A, B)	42-11060A01	0 ohms
JU5 (A)	42-11060A01	0 ohms
JU6, 7 (B, C)	42-11060A01	0 ohms
JU8	42-11060A01	0 ohms
Q1, 2	48-134674	transistor: (see note)
Q3, 4, 5	48-869642	NPN; type M9642
Q6	48-869467	PNIP; type M9467
Q7, 8	48-869642	NPN; type M9642
Q9	48-869643	PNIP; type M9643
Q10 thru 13	48-869642	NPN; type M9642
Q14 thru 200	NOT USED	
Q201, 202 (C)	48-869642	NPN; type M9642
R1, 2	6-11009B02	150k
R3	6-11009A99	120k
R4, 5	6-11009A97	100k
R6	6-11009A89	47k
R7	6-11009A97	100k
R8	6-11009A78	16k
R9	6-11009A71	6.2k
R10	6-11009A55	1.8k
R11	6-11009A63	3.3k
R12	6-11009A97	100k
R13	6-11009A81	22k
R14	6-11009A57	2.2k
R15	6-11009A61	3.3k
R16	6-11009A49	1k
R17	6-11009A97	5.6k
R18	6-11009A73	10k
R19	6-11009A53	1.5k
R20	6-11009A57	2.2k
R21	6-11009A53	1.5k
R22	6-11009A57	2.2k
R23	6-11009A46	750
R24	6-11009A41	470
R25	6-11009A33	220
R26	6-11009A81	22k
R27	6-11009A85	38k
R28	6-11009A73	10k
R29	6-11009A53	1.5k
R30	6-11009A73	10k
R31	6-10621E60	549k $\pm 1\%$; 1/8 W
R32	6-10621B94	1k $\pm 1\%$; 1/8 W
R33	6-10621C25	2050 $\pm 1\%$; 1/8 W
R34	6-11009A89	47k
R35	6-11009A77	15k
R36, 37	6-11009A73	10k
R38	6-11009A77	15k
R39	6-11009A93	68k
R40	6-11009A61	3.3k
R41	6-11009A81	27k
R42	6-11009A47	820
R43	6-11009A37	330
R44	6-11009A80	3k
R45	6-11009A81	22k
R46	6-11009A67	5.6k
R47	6-11009A89	47k
R48	6-11009A73	10k
R49	6-11009A67	5.6k
R50	6-11009A89	47k
R51	6-11009A71	6.2k
R52	6-11009A44	620
R53, 54	6-11009A61	3.3k
R55	6-11009A99	120k
R56	6-11009A81	22k
R57	6-11009A57	2.2k
R58	6-11009A77	15k
R59	6-11009A55	1.8k
R60, 61	6-10621C91	10k $\pm 1\%$; 1/8 W
R62	6-11009A89	6.8k
R63, 64	6-10621C79	7.5k $\pm 1\%$; 1/8 W
R65	6-10621D09	15k $\pm 1\%$; 1/8 W
R66	6-11009A93	68k
R67, 68	6-10621C91	10k $\pm 1\%$; 1/8 W
R69	6-11009A69	6.8k
R70, 71	6-10621C79	7.5k $\pm 1\%$; 1/8 W
R72	6-10621D18	18.7k $\pm 1\%$; 1/8 W
R73 thru 100	NOT USED	
R101 (A)	6-11009A97	100k
R102 (A)	6-11009A43	560
R103 (A)	6-11009A81	22k
R104 (A)	6-11009A57	2.2k
R105 (A)	6-11009A53	1.5k
R106 (A)	6-11009A57	2.2k
R107 thru 200	NOT USED	
R201 (C)	6-11009A77	15k
R202 (C)	6-11009A73	10k
R203 (C)	6-11009A57	2.2k
R204 (B, C)	6-11009A89	47k
R205 (B, C)	6-11009A73	10k
R206 (C)	6-11009A85	33k
RT1	6-83241P01	thermistor: 300 Ω @ 25°C
U1	51-80074C02	PL driver & level detector
U2	51-84371K65	monolithic timer
U3	51-83629M06	op-amplifier
U4 thru 100	NOT USED	
U101 (A)	51-80074C02	PL driver & level detector

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
VR1	48-83696E07	voltage regulator: (see note)
VR2	48-82256C38	Zener type; 6.2 V
Z1	KLN6209A	Zener type; 9.1 V
Z2(A, C)	KLN6209A	Vibrasponder Resonant Reed
mechanical parts		
	3-84256M01	SCREW, tapping: 4-10 x 5/16"; 2 used unless otherwise stated
	5-84220B01	GROMMET, 2 used
	9-83497F01	RECEPTACLE, female; 8-contact; 3 used (circuit board edge connector)
	9-84910C01	SOCKET, reed; 2 used (TRN5073A, 75A)
	64-8285N01	PANEL, front

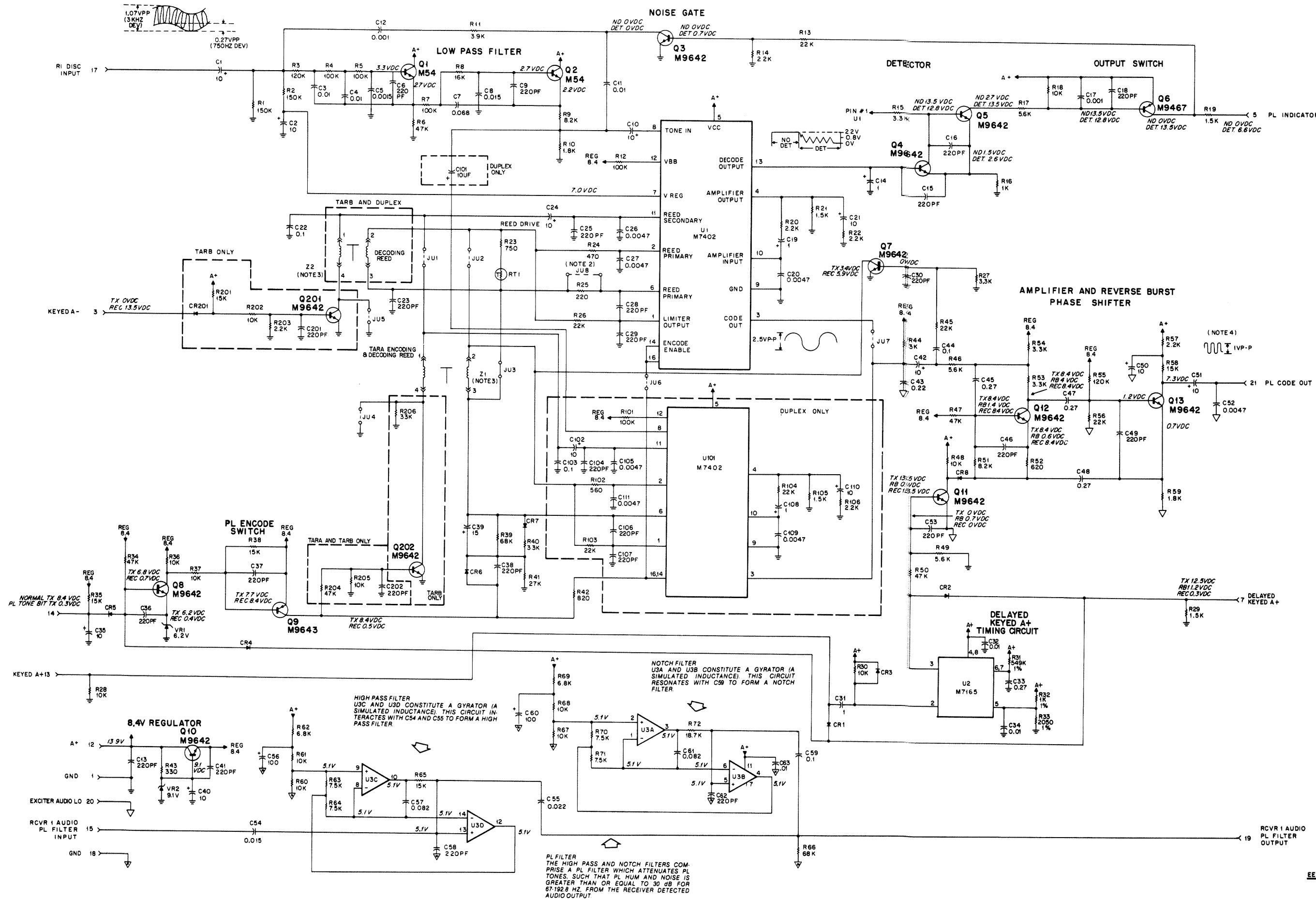
note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

COMPONENT SIDE
SOLDER SIDE

SHOWN FROM SOLDER SIDE

TONE PRIVATE-LINE ENCODER-DECODER MODULES

MODELS TRN5073A, 74A, 75A



NOTES:

- Unless otherwise indicated, resistors are in ohms, and capacitors are in microfarads.
- Jumper wire JU8 normally in. Out when using 67 Hz reed.
- For simplex TARA systems, Z1 encodes and decodes. For simplex TAR and duplex systems, Z1 encodes and Z2 decodes.
- Amplitude is 1 V p-p when PL module is connected to exciter.

Jumper Table

	Simplex Duplex		
	TARA	TARB	TARB
JU1	IN	IN	OUT
JU2	IN	IN	OUT
JU3	IN	OUT	OUT
JU4	IN	OUT	IN
JU5	OUT	OUT	IN
JU6	IN	IN	OUT
JU7	IN	IN	OUT
JU8	NOTE 2		

Schematic Diagram
Motorola No. PEPS-34857-B
(Sheet 2 of 2)
11/1/85-UP



Model Table

Model	Description
TRN5076A	Duplex T _A R _B
TRN5077A	Simplex T _A R _A
TRN5078A	Simplex T _A R _B

1. GENERAL

1.1 PHYSICAL DESCRIPTION

The TRN5076A, 77A, 78A *Digital Private-Line* (DPL) Encoder-Decoder Modules are plug-in modules designed for use with Motorola base and repeater stations. All components and circuitry are mounted on a sturdy circuit card with connecting terminals that mate with the backplane interconnect board of the station rf-control chassis.

1.2 FUNCTIONAL DESCRIPTION

Each of these modules can encode and decode subaudible *Digital Private-Line* codes. The encoder modulates the transmitter, and when the PTT signal is removed, the circuitry delays transmitter turn-off by approximately 180 ms to allow transmission of a receiver turn-off code. The decoder detects a received DPL code, and unmutes the receiver when the proper code is received.

2. DESCRIPTION OF OPERATION

Refer to the functional block and schematic diagrams attached to this instruction section.

2.1 SIMPLEX T_AR_A AND T_AR_B DPL MODULES

2.1.1 General

The TRN5077A Simplex T_AR_A Module incorporates one integrated circuit (U1) and one code plug (connected to J1) for both encoding and decoding. The TRN5078A Simplex T_AR_B Module also incorporates U1, but uses two code plugs (J250 and J251). The code plug designated J250 is used for the transmit code, and the code plug designated J251 is used for the receive code.

2.1.2 Decode Mode

In the decode (receive) mode, receiver audio is applied to the DPL module at pin 17, R1 DISC INPUT, and is routed through active low pass filter Q2-Q3, where frequencies above the DPL code range are attenuated. The output of the low pass filter is applied to phase-locked loop data conditioner U2, which squares the shape of the incoming code word. The output of the data conditioner is routed, via level shifter Q4, to the input of the decoder circuitry.

The decoder circuit consists of encoder-decoder U1, a 50 kHz clock (Y1, Q5), and the information stored in the code plug. When the proper code has been detected, the decoder provides a logic high at U1-7. This provides a logic high, via audio enable circuit Q15 & Q16, to pin 5, PL INDICATOR. This signal controls the audio mute gate on the station R1 audio and squelch module.

The logic high at U1-7 is also applied to sensitivity switch U3C, to disable the constant current source of U3D-U3E. With the constant current source disabled, the voltage at U2-8 is lowered, causing the sensitivity of U2 to increase. This provides additional immunity to audio interference and improved squaring of the incoming code word.

When the incoming (received) signal ceases, the sending transmitter produces a turn-off code. When the turn-off code is detected by the decoder, the detected output at U1-7 switches low. This decreases the sensitivity of the data conditioner and mutes receiver audio.

2.1.3 Encode Mode

When the station PTT signal is present, KEYED A+ is generated within the station. With KEYED A+ high, a high is generated at the collector of Q6, and is applied to encoder-decoder U1-9 (XMIT ENABLE). This causes U1 to switch to the encode mode. Encoder U1 then generates the transmit DPL code according to information stored in the code plug. The transmit DPL code signal is routed through the encoder low pass filter circuit (Q12 & Q13) to remove audio-frequency harmonics. The output

of the low pass filter is applied to the exciter via pin 21, DPL CODE OUT. During transmission, C22 is used in the circuit to shift the corner frequency of the filter. During the time when only turn-off code is transmitted, C22 is out of the circuit in order to unshift the corner frequency of the filter. When the PTT signal ceases, the loss of KEYED A+ triggers the delayed keyed A+ circuit (Q8, Q9, & Q10). This circuit provides DELAYED KEYED A+ to the station, via pin 7, for a period of approximately 180 ms, during which time the encoder sends the turn-off code to the exciter for transmission.

The transmit DPL code signal is inhibited during transmission (required for proper paging operation) by applying a low to pin 14, TRANSMIT PL INHIBIT. The low turns Q14 on, which shunts the junction of R17, R18, R20, and C20 to ac ground.

2.2 DUPLEX T_AR_B DPL MODULE

The TRN5076A Duplex T_AR_B Module is the same as the simplex versions, except that the module allows the station to decode (receive) and encode (transmit) simultaneously. This is accomplished by using separate, dedicated encoder and decoder integrated circuits and code plugs. In duplex operation, U1 is a decoder only, and U100 is an encoder only.

3. CIRCUIT DESCRIPTIONS

3.1 DELAYED KEYED A+ TIMING CIRCUIT

The delayed keyed A+ timing circuit is used to maintain transmitter turn-on long enough for the DPL encoder to send the turn-off code. This period is approximately 180 ms.

When pin 13, KEYED A+, goes low at the end of a transmission (loss of PTT), the negative side of C27 approaches A+. It should be noted that since the voltage

on C27 cannot change instantaneously, the voltage at the junction of R53, R54 & CR5 is increased. When this voltage is larger than the anode voltage of CR5, the diode does not conduct. Thus, the collector of Q9 swings low (approaches ground), the base of Q10 approaches A+, and the collector of Q10 swings low, which turns off Q10. Therefore, the delayed keyed A+ line switches low, which causes station transmission to cease.

3.2 TWO-CODE SWITCH CIRCUIT

The two-code switch circuit (Q250 & Q251) on simplex T_AR_B models is used to select and enable the proper code plug for transmit and receive modes. Code plug J250 is active in the transmit mode, and code plug J251 is active in the receive mode.

During the receive mode, the collector of keyed A+ switch Q6 is low. This low is inverted by Q250, and is applied as a high to code plug J250, to disable the transmit code. The high from Q250 is inverted by Q251, and applied as a low to code plug J251, to enable the receive code.

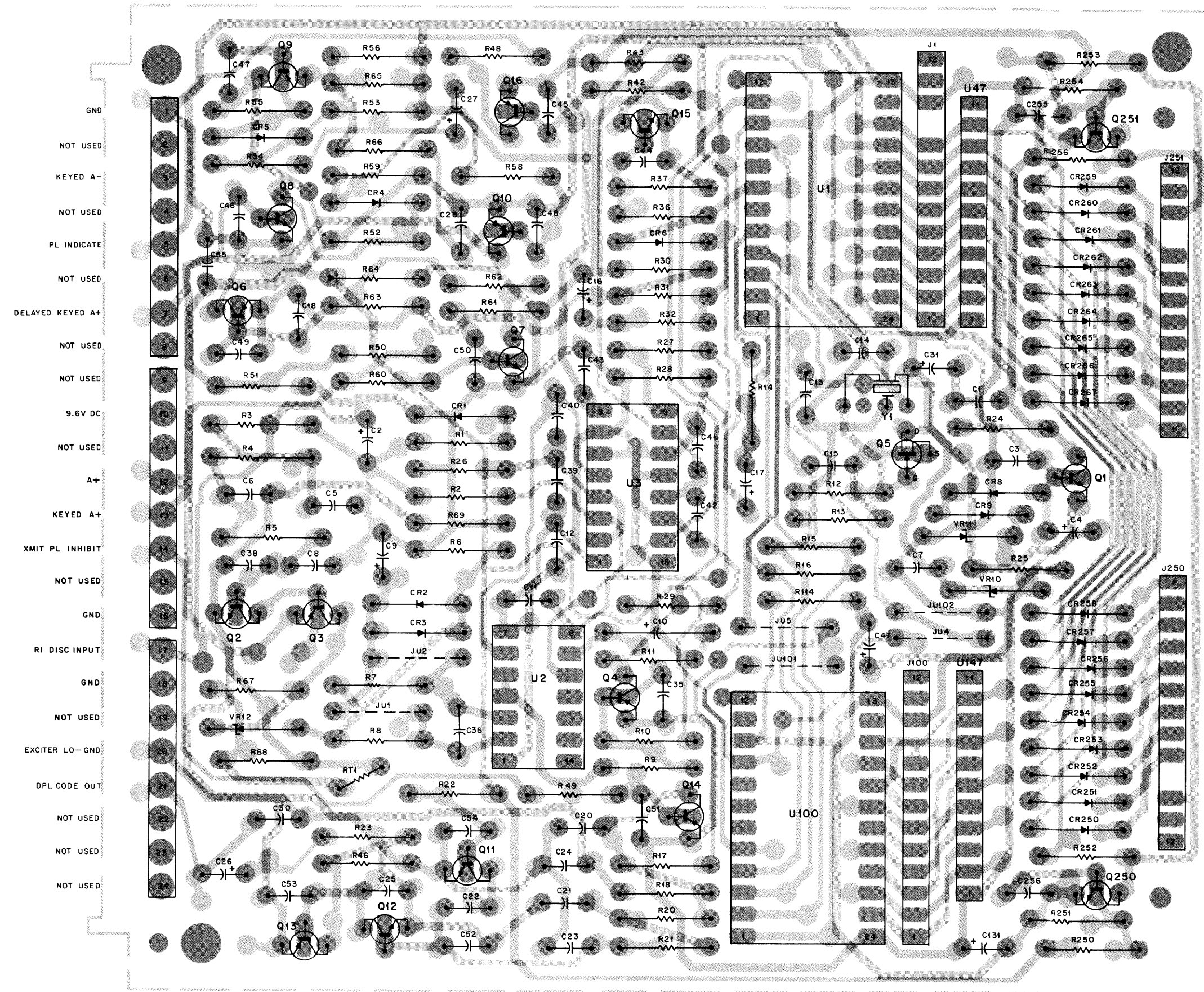
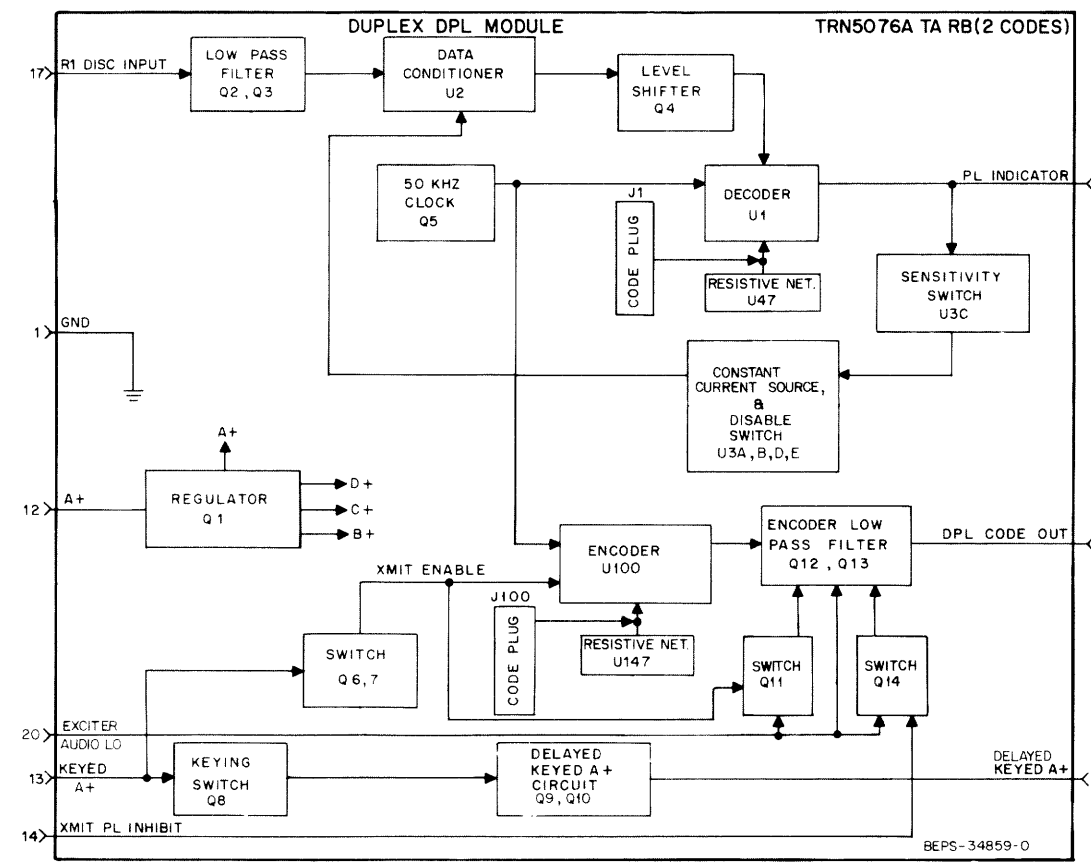
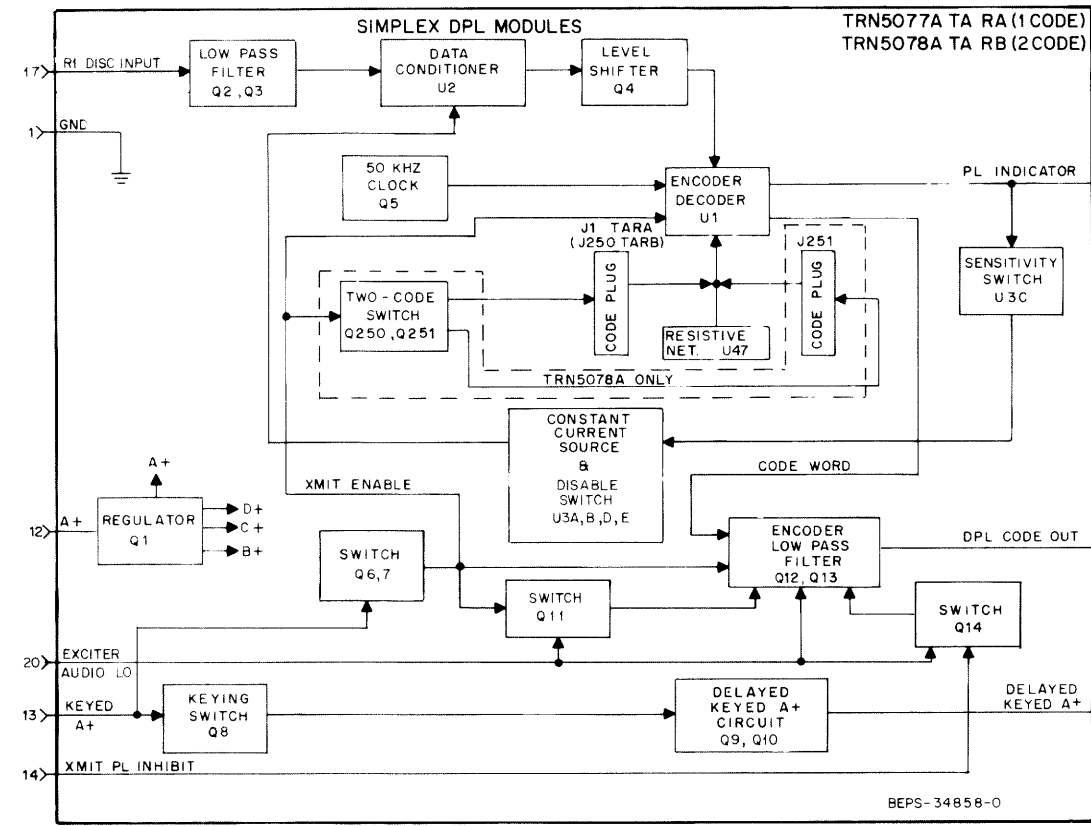
During the transmit mode, the collector of keyed A+ switch Q6 is high, which causes the transmit code from J250 to be enabled (inverted low by Q250), and the receive code from J251 to be disabled (inverted high by Q251).

3.3 REGULATOR CIRCUIT

Regulator Q1 provides three regulated dc voltages from station A+ (13.9 V). These voltages, in addition to A+, power all circuitry on the DPL board. The regulated voltages are 11.1 V (B+), 10.5 V (C+), and 6.2 V (D+).

DIGITAL PRIVATE-LINE ENCODER-DECODER MODULES

MODELS TRN5076A, 77A, 78A



SHOWN FROM SOLDER SIDE

parts list

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
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This parts list covers 3 models of the DPL Encoder-Decoder Modules. Where differences exist, a letter code is added to the reference symbol to indicate the applicable unit.

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
C1	21-11021F04	capacitor, fixed: uF ± 5%; 50 V;
C2	23-84612M20	01 ± 20%
C3	21-11021F04	47 ± 10%; 25 V
C4	23-84612M19	01 ± 20%
C5	8-11017A11	15 ± 10%; 25 V
C6	8-11017A16	0.22
C7	21-11021F04	0.1 ± 20%
C8	8-11017A18	0.039
C9	23-84612M18	10 ± 10%; 25 V
C10	23-82783B48	0.88; 35 V
C11, 12	21-11015B13	0.01 ± 10%; 100 V
C13	21-11022A55	100 pF
C14	21-11022A37	20 pF
C15	21-11021A21	0.047 ± 10%
C16	23-84612M17	6.8 ± 10%; 25 V
C17	23-11019A16	4.7 ± 20%; 35 V
C18	23-84612M17	6.8 ± 10%; 25 V
C19	—	NOT USED
C20	8-11017A14	0.047
C21	8-11017A13	0.33
C22	8-11017A19	0.056
C23	8-11017A05	0.033
C24	21-11021F04	0.1 ± 20%
C25	21-11015B13	0.01 ± 10%; 100 V
C26	23-84612M20	47 ± 10%; 25 V
C27	23-84612M18	10 ± 10%; 25 V
C28	21-11015B13	0.01 ± 10%; 100 V
C29	—	NOT USED
C30	8-11017B06	0.047
C31	23-11019A16	4.7 ± 20%; 35 V
C32, 33, 34	—	NOT USED
C35, 36	21-11015B05	220 pF ± 10%; 100 V
C37	—	NOT USED
C38 thru 54	21-11015B05	220 pF ± 10%; 100 V
C55 thru 116	—	NOT USED
C117 (A)	23-11019A16	4.7 ± 20%; 35 V
C118 thru 130	—	NOT USED
C131 (A)	23-11019A16	4.7 ± 20%; 35 V
C132 thru 254	—	NOT USED
C255, 256 (C)	21-11015B05	220 pF ± 10%; 100 V
CR1	48-83654H02	silicon
CR2, 3	48-84616A01	hot carrier
CR4, 5, 6	48-83654H01	silicon
CR7	—	NOT USED
CR8, 9	48-83654H01	silicon
CR10 thru 249	—	NOT USED
CR250 thru 267 (C)	48-83654H01	silicon
J1	9-82071K01	connector, receptacle: female; 12-contact (DPL plug)
J2 thru 99	—	NOT USED
J100 (A)	9-82071K01	female; 12-contact (DPL plug)
J101 thru 249	—	NOT USED
J250, 251 (C)	9-82071K01	female; 12-contact (DPL plug)
JU1 thru 4	42-11060A01	0 ohms
JU5 thru 100	—	NOT USED
JU101, 102 (A)	42-11060A01	0 ohms
Q1	48-869648	transistor: (see note) NPN; type M9648
Q2	48-869642	NPN; type M9642
Q3, 4	48-869643	PNP; type M9643
Q5	48-869653	field-effect; M9653
Q6	48-869643	PNP; type M9643
Q7, 8	48-869642	NPN; type M9642
Q9, 10	48-869643	PNP; type M9643
Q11, 12	48-869642	NPN; type M9642
Q13, 14	48-869643	PNP; type M9643
Q15	48-869642	NPN; type M9642
Q16	48-869643	PNP; type M9643
Q17 thru 249	—	NOT USED
Q250, 251 (C)	48-869642	NPN; type M9642
R1	6-11009A93	resistor, fixed: ± 5%; 1/4 W; unless otherwise stated
R2	6-11009A99	56k
R3, 4, 5	6-10621D64	120k
R6	6-11009A43	56.2k ± 1%
R7, 8	6-11009A73	10k
R9	6-11009A59	2.7k
R10	6-11009A73	10k
R11	6-11009A83	27k
R12	6-11009B08	270k
R13	6-11009A77	15k
R14	6-11009A97	100k
R15	6-11009B04	180k
R16	6-11009B14	470k
R17	6-11009A87	39k
R18	6-11009A99	120k
R19	—	NOT USED
R20, 21	6-11009A97	100k
R22	6-11009A75	12k
R23	6-11009A77	15k
R24, 25	6-11009A33	220
R26	6-11009A73	10k
R27	6-11009A89	47k
R28	6-11009A95	82k
R29	6-11009B14	470k
R30	6-11009A91	56k
R31	6-11009A99	120k
R32	6-11009A91	56k
R33, 34, 35	—	NOT USED
R36	6-11009A99	120k
R37	6-11009A95	82k
R38 thru 41	—	NOT USED
R42, 43	6-11009A89	47k
R44, 45	—	NOT USED
R46	6-11009A49	1k
R47	—	NOT USED
R48	6-11009A53	1.5k
R49	6-11009A97	100k
R50	6-11009A57	2.2k
R51	6-11009A49	1k
R52	6-11009A97	10k
R53	6-11009A83	27k
R54	6-11009A65	4.7k
R55	6-11009A75	12k
R56	6-11009A56	2k
R57	—	NOT USED
R58	6-11009A53	1.5k
R59	6-11009A57	2.2k
R60, 61	6-11009A89	47k
R62	6-11009A82	24k
R63	6-11009A73	10k
R64	6-11009A89	47k
R65	6-11009A56	2k
R66	6-11009A45	680
R67	6-11009A49	1k
R68	6-11009A45	680
R69	6-11009A53	1.5k
R70 thru 113	—	NOT USED
R114 (A)	6-11009A97	100k
R115 thru 249	—	NOT USED
R250 (C)	6-11009A73	10k
R251 (C)	6-11009A65	4.7k
R252, 253 (C)	6-11009A73	10k
R254 (C)	6-11009A65	4.7k
R255	—	NOT USED
R256 (C)	6-11009A73	10k
RT1	6-83241P01	thermistor: 300 @ 25°C
U1	51-80074C01	integrated circuit: (see note) encoder/decoder
U2	51-83629M01	phase loop lock
U3	51-83629M10	transistor array
U4 thru 46	—	NOT USED
U47	51-82142K02	resistor network
U48 thru 99	—	NOT USED
U100 (A)	51-80074C01	encoder/decoder
U101 thru 146	—	NOT USED
U147 (A)	51-82142K02	resistor network
VR10	48-83696E07	voltage regulator: (see note) Zener type; 6.2 V
VR11	48-82256C11	Zener type; 10 V
VR12	48-82256C26	Zener type; 3.3 V
Y1	48-82003K01	crystal: (see note) 50k

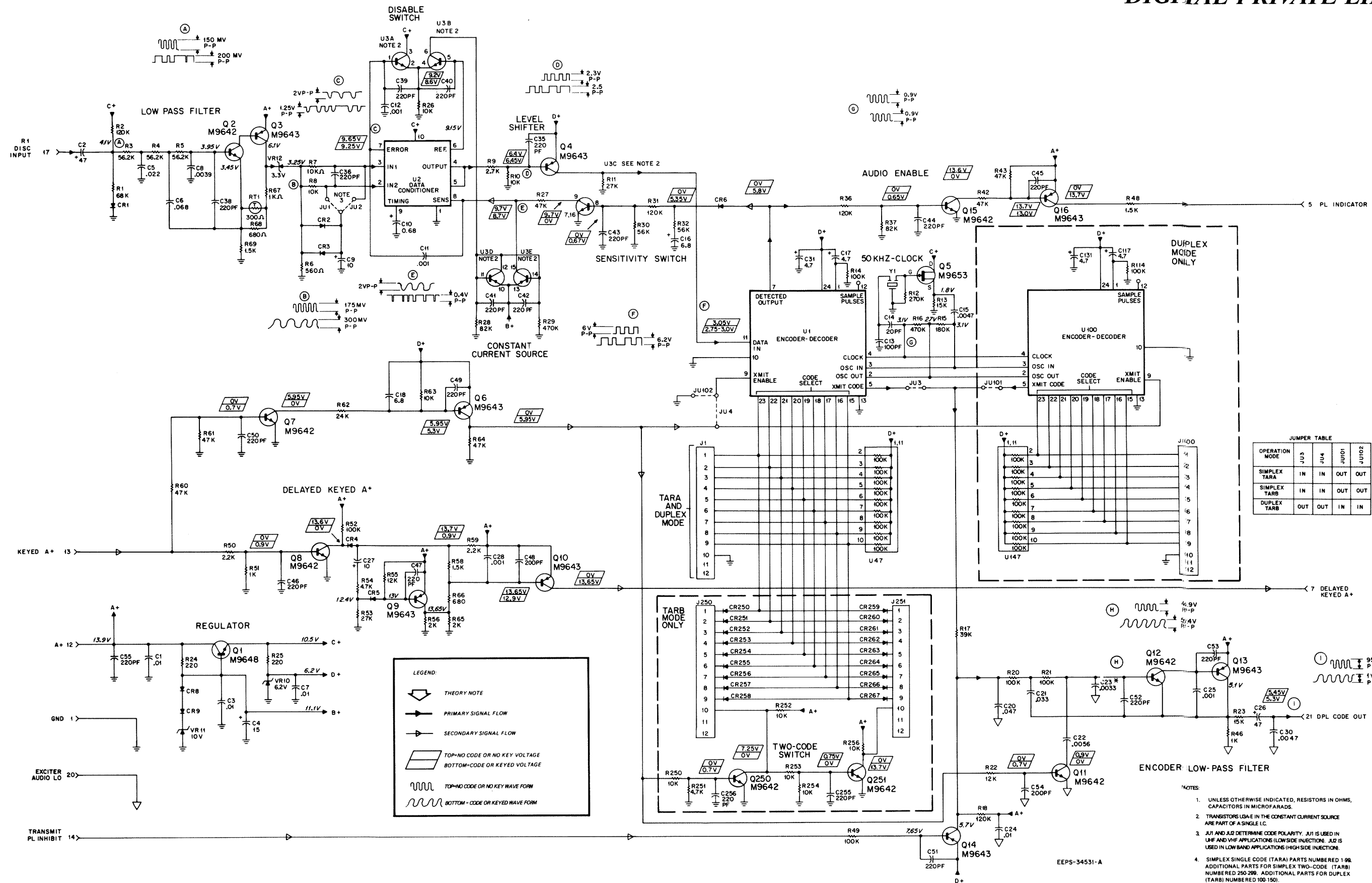
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
3-84256M01	—	SCREW, tapping; 4-10 x 5/16"; 2 used
5-8420B01	—	GNOMMET
9-83497F01	—	RECEPTACLE, female; 8-contact; 3 used (circuit board edge connector)
14-861196	—	INSULATOR, XTAL
64-83837N01	—	PANEL, front

note: For optimum performance, diodes, transistors, and integrated circuits must be ordered by Motorola part numbers.

Functional Block Diagrams, Circuit Board Detail, and Parts List Motorola No. PEPS-34860-B (Sheet 1 of 2) 11/1/85-UP

DIGITAL PRIVATE-LINE ENCODER-DECODER MODULES

MODELS TRN5076A, 77A, 78A



Schematic Diagram
Motorola No. PEPS-34860-B
(Sheet 2 of 2)
11/1/85- UP