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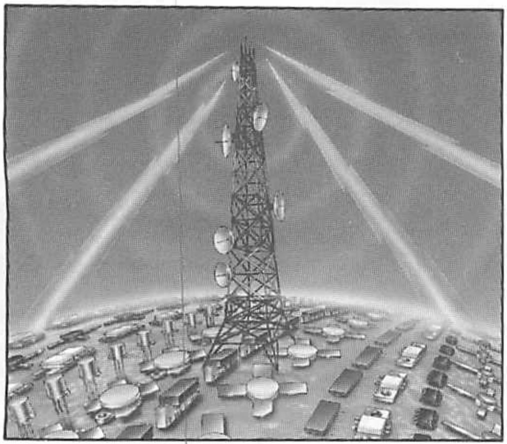
MOTOROLA

RF DEVICE DATA

VOLUME II



MOTOROLA
RF DEVICE DATA
Volume II

Prepared by
Technical Information Center

Extensive changes have been made to the sixth edition of the RF Data Manual. In March, 1988, Motorola acquired the RF Devices Division of TRW. The RF products manufactured by the acquired facilities were included for the first time in the fifth edition of the RF Data Book. During the past 2 years, a consolidation of products has taken place with the result being the deletion of a large number of products previously included in the fifth edition. However, an equally large number of new products has resulted in the data book remaining as a 2 volume set.

Once again, Volume 1 contains all Discrete Transistors (along with the Discrete portion of the RF Selection guide). All other devices, primarily amplifiers along with tuning diodes, are included in Volume 2. Also in Volume 2 is a greatly expanded section on Applications. The many diverse Application Notes from the TRW facilities in California and France have been integrated along with the previously available application notes from the RF facility in Arizona. This data forms one of the most comprehensive groups of RF application available in the industry today.

HOW TO USE THIS RF DATA BOOK:

Note that all devices in a given section — Discrete Transistors, Amplifiers and Tuning Diodes — are organized in conventional alphanumeric order.

If you know the part for which you desire technical data, simply turn to the appropriate page in Volume 1 or 2. If you are seeking a replacement for a competitor's part, then use the **Cross Reference** in Volume 2 to find the Motorola recommended replacement. If you have a requirement for a specified frequency band, then use the **Selector Guide** (in both Volumes 1 and 2) to find a suitable part with the desired voltage, output power, gain or other requisite characteristic.

Although information in these books has been carefully checked, no responsibility for inaccuracies can be assumed by Motorola. Please consult your nearest Motorola Semiconductor sales office for further assistance regarding any aspect of Motorola RF Products.

Sixth Edition
First Printing

Printed in U.S.A.

DATA CLASSIFICATION

Product Preview

Data sheets herein contain information on a product under development. Motorola reserves the right to change or discontinue these products without notice.

Advanced Information

Data sheets herein contain information on new products. Specifications and information are subject to change without notice.

Formal

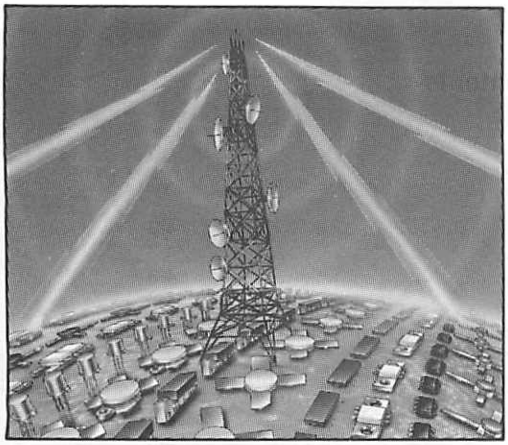
For a fully characterized device there must be devices in the warehouse and price authorization.

Designer's

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MASTER INDEX

AMPLIFIERS



Volume II

Selector Guide

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Table of Contents

RF Amplifiers

High Power

Complete amplifiers with 50 ohm in/out impedances are available for a variety of applications including land mobile radios, base stations, TV transmitters and other uses requiring large-signal amplification, both linear and Class C. Frequencies covered range from 1 MHz to 1000 MHz with power levels extending to 100 watts.

Land Mobile/Portable

The advantages of small size, reproducibility and overall lower cost become more pronounced with increasing frequency of operation. These amplifiers offer a wide range in power levels and gain, with guaranteed performance specifications for bandwidth, stability and ruggedness.

136–174 MHz, VHF BAND — Class C

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	Gp Power Gain dB Min	V_{CC} Supply Voltage Volts	Package/Style
MHW607-1	7	0.001	136–150	38.4	7.5	301K-02/3
MHW607-2	7	0.001	146–174	38.4	7.5	301K-02/3

400–512 MHz, UHF BAND — Class C

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	Gp Power Gain dB Min	V_{CC} Supply Voltage Volts	Package/Style
MHW707-1	7	0.001	403–440	38.4	7.5	301J-02/1
MHW707-2	7	0.001	440–470	38.4	7.5	301J-02/1
MHW709-1	7.5	0.1	400–440	18.8	12.5	700-03/1
MHW709-2	7.5	0.1	440–470	18.8	12.5	700-03/1
MHW709-3	7.5	0.1	470–512	18.8	12.5	700-03/1
MHW710-1	13	0.15	400–440	19.4	12.5	700-03/1
MHW710-2	13	0.15	440–470	19.4	12.5	700-03/1
MHW710-3	13	0.15	470–512	19.4	12.5	700-03/1
MHW720-1	20	0.15	400–440	21	12.5	700-03/1
MHW720-2	20	0.15	440–470	21	12.5	700-03/1
MHW720A1 (21)	20	0.15	400–440	21	12.5	700-03/1
MHW720A2 (21)	20	0.15	440–470	21	12.5	700-03/1
MHW721A2	20	0.15	450–460	21	12.5	700-03/1
MX20-1	20	0.15	400–440	21	12.5	830-01/1
MX20-2	20	0.15	440–470	21	12.5	830-01/1
MHW703	2.3	0.002	450–460	30.6	7.2	301J-02/1

806–960 MHz, UHF BAND — Class C

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	Gp Power Gain dB Min	V_{CC} Supply Voltage Volts	Package/Style
MHW801-1	1.6	0.001	820–850	32	6	413-01/1
MHW801-2	1.6	0.001	870–905	32	6	413-01/1
MHW801-3	2	0.001	890–915	33	6	413-01/1
MHW801-4	1.6	0.001	915–925	32	6	413-01/1
MHW803-1	2	0.001	820–850	33	7.5	301E-04/1
MHW803-2	2	0.001	806–870	33	7.5	301E-04/1
MHW803-3	2	0.001	870–905	33	7.5	301E-04/1
MHW806A1 (21)	6	0.03	820–850	23	12.5	301H-03/1
MHW806A2 (21)	6	0.03	806–870	23	12.5	301H-03/1
MHW806A3 (21)	6	0.04	890–915	21.7	12.5	301H-03/1
MHW806A4 (21)	6	0.04	870–950	21.7	12.5	301H-03/1
MHW807-1	6	0.001	820–850	38	12.5	301L-01/1
MHW807-2	6	0.001	870–905	38	12.5	301L-01/1
MHW812A3 (21)	12	0.1	870–950	20.8	13	301H-03/1
MHW820-3	18	0.35	870–950	17.1	12.5	301G-03/1
MHW820-1	20	0.25	806–870	19	12.5	301G-03/1
MHW820-2	20	0.25	806–890	19	12.5	301G-03/1
MHW851-1	1.6	0.001	820–850	32	6	301N-01/1
MHW851-2	1.6	0.001	870–905	32	6	301N-01/1
MHW851-3	2.0	0.001	890–915	33	6	301N-01/1
MHW851-4	1.6	0.001	915–925	32	6	301N-01/1
MHW857-1	6	0.001	820–850	37.8	12.5	301L-02/2
MHW857-2	6	0.001	870–905	37.8	12.5	301L-02/2

(21) Designed for Wide Range P_{out} Level Control

New introductions

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Base Station

The convenience of complete amplifiers for base station transmitters is offered for many two-way radio bands from VHF through the high-UHF cellular bands (806–960 MHz). Power levels to 120 W are available operating from 24 to 26 volt supplies. Class AB or Class A operation provides linear performance suitable in both analog and digital systems.

The AMR/ACR series can optionally be modified in frequency, power and mechanical outline. Please contact your local MOTOROLA field sales office.

145–225 MHz BAND — Class AB

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain dB Min	V_{CC} Supply Voltage Volts	Package/Style
AMR175-60	60	6	145–175	10	28	389K-01/1
AMR225-60	60	6	180–225	10	28	389K-01/1

400–512 MHz BAND — Class AB

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain dB Min	V_{CC} Supply Voltage Volts	Package/Style
AMR440-60	60	12	400–440	7	28	389L-01/1
AMR470-60	60	12	440–470	7	28	389L-01/1

806–960 MHz BAND — Class A and/or AB

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain dB Min	V_{CC} Supply Voltage Volts	Package/Style
AMR900-60A (22)	20	2.25	800–960	9.5	26	389B-02/1
ACR900-30E	30	0.48	890–960	18	25	389J-01/1
AMR900-60	60	12	800–960	7	24	389B-02/2
AMR900-80 (1)	80	16	865–900	7	26	389M-01/1
AMR960-80 (1)	80	16	935–960	7	26	389M-01/1
AMR960-100 (1)	100	20	860–960	7	26	389M-01/1

(1) To be introduced
(22) Class A device

New introductions

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TV Transmitters

These amplifiers are characterized for ultra-linear applications in Band IV and V TV transmitters.

Device	Frequency MHz	P_{ref} Watts	Gp (Min)/Freq. Power Gain dB/MHz	3 Tone (12) IMD 1 dB	3 Tone (24) IMD 2 dB	V_{CC} Volts	Package/ Style
ATV5030	470–860	20	7.5/860	−51	−54	26	389B-02/1
ATV5090B	470–860	90 (13)	7/860	—	—	28	389N-01/1
ATV6031	470–860	20	10.5/860	−50	−53	26.5	389B-02/1
ATV7050	470–860	30	8/860	−51	−54	25	389P-01/1
ATV7060	470–860	40	10/860	−51	−54	25.5	389H-01/1

PAM Series — Ultra Linear

PAM devices are class A and class AB linear amplifiers with medium and high output powers in the VHF and UHF frequency range. They feature a wide dynamic range and a high third order intercept point. These high quality amplifiers are offered in a heavy-duty machined housing and are ideal for applications in instrumentation, communications and electronic warfare.

VHF BAND — Class A

Device	Frequency MHz	P_o Min Watts	Gain Typ dB	V_{CC} Volts	3rd Order Intercept Typ dBm	Package/ Style
PAM225-42-10L	172–225	10	46	24	−58 (25)	389C-01/1
PAM225-42-10LA	172–225	10	46	28	−58 (25)	389C-01/1

VHF/UHF BAND — Class A

Device	Frequency MHz	P_o Min Watts	Gain Typ dB	V_{CC} Volts	3rd Order Intercept Typ dBm	Package/ Style
PAM0105-29-6L	100–500	6	31	24	+48.5	389C-01/1
PAM0105-29-6LA	100–500	6	31	28	+48.5	389C-01/1
PAM0105-7-25L	100–500	25	7.5	24	+53.5	389E-01/1
PAM0105-7-25LA	100–500	25	7.5	28	+53.5	389E-01/1
PAM0105-6-50L	100–500	50	7	24	+56.5	389D-01/1
PAM0105-6-50LA	100–500	50	7	28	+56.5	389D-01/1

UHF BAND — Class A

Device	Frequency MHz	P_o Min Watts	Gain Typ dB	V_{CC} Volts	3rd Order Intercept Typ dBm	Package/ Style
PAM0510-25-6L	500–1000	27	24	48.5	389C-01/1	
PAM0810-24-3L	800–1000	3	26	24	+45	389C-01/1
PAM0810-24-3LA	800–1000	3	26	28	+45	389C-01/1
PAM0810-24-5L	800–1000	5	26	24	+47.5	389C-01/1
PAM0810-24-5LA	800–1000	5	26	28	+47.5	389C-01/1
PAM0810-8-10L	800–1000	10	10	24	+50	389E-01/1
PAM0810-8-10LA	800–1000	10	10	28	+50	389E-01/1
PAM0810-7-25L	800–1000	25	8	24	+55	389E-01/1
PAM0810-7-25LA	800–1000	25	8	28	+55	389E-01/1
PAM0810-6-50L	800–1000	50	7	24	+56.5	389D-01/1
PAM0810-6-50LA	800–1000	50	7	28	+56.5	389D-01/1

(12) Vision Carrier = −8 dB; Sound Carrier = −7 dB; Sideband Carrier = −16 dB
(13) Output power at 1 dB compression, in Class AB
(17) Higher Voltage Version
(24) Vision Carrier = −8 dB; Sound Carrier = −10 dB; Sideband Carrier = −16 dB
(25) Composite Triple Beat in dB. Tones: −8, −11 and −16 dB

New introductions

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PAA Series — Ultra Linear Integrated Amplifier Assemblies

PAA and PAE integrated assemblies are class A amplifiers with internal power supply. Available in either 115 Vac or 220 Vac operation. They provide high-gain, excellent linearity and can withstand any load VSWR.

WIDE BAND, MEDIUM POWER — Class A

Device	Frequency MHz	P_O Min Watts	Gain Typ dB	V_{AC} Volts	3rd Order Intercept Typ dBm	Package/ Style
PAA0200-34-1.5L	1–200	1.5	36	115	+45	389R-01/1
PAA0200-34-3.1L	1–200	3.1	35	115	+48	389R-01/1
PAA0450-33-0.4L	30–450	0.4	34	115	+38	389R-01/1
PAA0500-17-1.0L	30–500	1	18	115	+42	389R-01/1
PAA0500-35-1.0L	30–500	1	36.5	115	+42	389R-01/1
PAA0500-17-2.0L	30–500	2	18	115	+33	389R-01/1
PAA1000-14-0.6L	10–1000	0.6	15	115	+42	389R-01/1
PAA1000-30-0.6L	10–1000	0.6	32	115	+42	389R-01/1
PAA1000-14-1.3L	10–1000	1.3	15	115	+44	389R-01/1
PAE0200-34-1.5L	1–200	1.5	36	220	+45	389R-01/1
PAE0200-34-3.1L	1–200	3.1	35	220	+48	389R-01/1
PAE0450-33-0.4L	30–450	0.4	34	220	+38	389R-01/1
PAE0500-17-1.0L	30–500	1	18	220	+42	389R-01/1
PAE0500-35-1.0L	30–500	1	36.5	220	+42	389R-01/1
PAE0500-17-2.0L	30–500	2	18	220	+33	389R-01/1
PAE1000-14-0.6L	10–1000	0.6	15	220	+42	389R-01/1
PAE1000-30-0.6L	10–1000	0.6	32	220	+42	389R-01/1
PAE1000-14-1.3L	10–1000	1.3	15	220	+44	389R-01/1

WIDE BAND, HIGH POWER — Class A

Device	Frequency MHz	P_O Min Watts	Gain Typ dB	V_{AC} Volts	3rd Order Intercept Typ dBm	Package/ Style
PAA1000-42-5L	25–1000	5	42	115	+46.5	389F-01/1
PAE1000-42-5L	25–1000	5	42	220	+46.5	389F-01/1

VHF BAND, HIGH POWER — Class A

Device	Frequency MHz	P_O Min Watts	Gain Typ dB	V_{AC} Volts	3rd Order Intercept Typ dBm	Package/ Style
PAA225-42-10L	172–225	10	46	115	−58 (25)	389F-01/1
PAE225-42-10L	172–225	10	46	220	−58 (25)	389F-01/1

VHF/UHF BAND, HIGH POWER — Class A

Device	Frequency MHz	P_O Min Watts	Gain Typ dB	V_{AC} Volts	3rd Order Intercept Typ dBm	Package/ Style
PAA0105-29-6L	100–500	6	31	115	+48.5	389F-01/1
PAA0105-45-25L	100–500	25	47	115	+53	389F-01/1
PAA0105-50-50LAS	100–500	50	52	115	+56.5	389G-01/1
PAE0105-29-6L	100–500	6	31	220	+48.5	389F-01/1
PAE0105-45-25L	100–500	25	47	220	+53	389F-01/1
PAE0105-50-50LAS	100–500	50	52	220	+56.5	389G-01/1

UHF BAND, HIGH POWER — Class A

Device	Frequency MHz	P_O Min Watts	Gain Typ dB	V_{AC} Volts	3rd Order Intercept Typ dBm	Package/ Style
PAA0510-25-6L	500–1000	6	27	115	48.5	389F-01/1
PAA0810-24-5L	800–1000	4.5	26	115	+47.5	389F-01/1
PAA0810-38-5LAS	800–1000	4.5	42	115	+47.5	389F-01/1
PAA0810-32-10L	800–1000	10	35	115	+50	389F-01/1
PAA0810-31-25L	800–1000	25	33	115	+55	389F-01/1
PAA0810-40-50L	800–1000	50	42	115	+56.5	389G-01/1
PAA0810-40-50LAM (26)	800–1000	50	42	115	+56	389G-01/1
PAA0810-54-50LAS	800–1000	50	56	115	+56.5	389G-01/1
PAA0810-54-50LSM (26)	800–1000	50	56	115	+56	389G-01/1
PAA0810-38-100AB	800–1000	100	38	115	—	389G-01/1
PAA0810-52-100AB	800–1000	100	52	115	—	389G-01
PAA0810-52-100AM (26)	800–1000	100	52	115	—	389G-01/1
PAE0810-24-5L	800–1000	4.5	26	220	+47.5	389F-01/1
PAE0810-38-5LAS	800–1000	4.5	42	220	+47.5	389F-01/1
PAE0810-32-10L	800–1000	10	35	220	+50	389F-01/1
PAE0810-31-25L	800–1000	25	33	220	+55	389F-01/1
PAE0810-40-50L	800–1000	50	42	220	+56.5	389G-01/1
PAE0810-40-50LAM (26)	800–1000	50	42	220	+56	389G-01/1
PAE0810-54-50LAS	800–1000	50	56	220	+56.5	389G-01/1
PAE0810-54-50LSM (26)	800–1000	50	56	220	+56	389G-01/1
PAE0810-38-100AB	800–1000	100	38	220	—	389G-01/1
PAE0810-52-100AM (26)	800–1000	100	52	220	—	389G-01/1

(25) Composite triple beat in dB. Tones: −8, −11 and −16 dB
(26) Includes directional wattmeter, filter and directional coupler

New introductions

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Low Power

The following categories describe a wide range of complete amplifier assemblies both hybrid and monolithic for use in CATV distribution systems, instrumentation, communications and military equipment. A variety of power levels and frequencies of operation are offered for many applications.

CATV Distribution

Motorola Hybrids are manufactured using fourth generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 77 channels.

HYBRIDS UP TO 60 CHANNELS AND 450 MHz

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test (28) dB	Composite Triple Beat dB 60 CH	Cross Modulation dB 60 CH	Noise Figure @ 450 MHz dB Max	Typ	Package/Style
MHW5122A	12	60	+46	−72	−58	−61	8	7	714-04/1
MHW5141A	14	60	+46	−72	−56	−59	7	—	714-04/1
MHW5142A	14	60	+46	−74	−61	−62	7	6	714-04/1
MHW5162A	16	60	+46	−72	−58	−61	7	6	714-04/1
MHW5171A	17	60	+46	−72	−58	−59	7	—	714-04/1
MHW5172A	17	60	+46	−74	−60	−62	7	6	714-04/1
MHW5181A	18	60	+46	−72	−57	−56	6.5	5.5	714-04/1
MHW5182A	18	60	+46	−72	−61	−59	6.5	5.5	714-04/1
MHW5222A	22	60	+46	−72	−60	−59	5	4.5	714-04/1
MHW5272A	27	60	+46	−72	−59	−60	6	—	714-04/1
MHW5342A	34	60	+46	−72	−59	−59	6	5	714-04/1
MHW5382A	38	60	+46	−70	−59	−59	5	4	714-04/1
MHW5332	33	60	+46	−70	−60	−59	6	5	714-04/1
CA7901	21	60	+46	−61	−58	−60	—	5.6	714F-01/1

(28) Channels 2 and M13 @ M22

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LOW POWER (continued)

HYBRIDS UP TO 77 CHANNELS AND 550 MHz

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test (29) dB	Composite Triple Beat dB	Cross Modulation dB	Noise Figure @ 550 MHz dB		Package/Style
					77 CH	77 CH	Max	Typ	
MHW6122	12	77	+44	−74	−56	−62	8.5	7	714-04/1
MHW6141	14	77	+44	−72	−56	−59	7.5		714-04/1
MHW6142	14	77	+44	−72	−59	−62	7.5		714-04/1
MHW6171	17	77	+44	−68	−56	−59	7		714-04/1
MHW6172	17	77	+44	−70	−59	−62	7		714-04/1
MHW6181	18	77	+44	−70	−56	−59	7		714-04/1
MHW6182	18	77	+44	−72	−58	−62	7		714-04/1
MHW6222	22	77	+44	−66	−57	−57	6		714-04/1
MHW6272	27	77	+44	−64	−57	−57	6.5	6	714-04/1
MHW6342	34	77	+44	−64	−57	−57	6.5	5.5	714-04/1

HYBRIDS UP TO 860 MHz

Device	Gain dB	Frequency MHz	V_{CC} Volts	2nd Order IMD dB @ V_{out} = 50 dBmV/ch	Composite Triple Beat dB @ V_{out}/Freq. (dBmV/MHz)	DIN45004B dBmV @ Freq. (MHz)	NF @ 860 MHz dB Max	Package/Style
CA901	17	40–860	24	−60		60 (860)	9	714P-01/2
CAB914	23	470–860	24		−51 (61/860)	62 (860)	8.5	830A-01/1

REVERSE AMPLIFIER HYBRIDS

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB (30)	Composite Triple Beat dB			Cross Modulation dB			Noise Figure @ 175 MHz dB	Package/Style
					12 CH	22 CH	26 CH	12 CH	22 CH	26 CH	Max	
MHW1134	13	22	+50	−72	—	−73	−71 (16)	—	−65	−65 (16)	7	714-04/1
MHW1184	18	22	+50	−72	—	−72	−70 (16)	—	−64	−64 (16)	5.5	714-04/1
MHW1224	22	22	+50	−72	—	−71	−68 (16)	—	−62	−62 (16)	5.5	714-04/1
MHW1244	24	22	+50	−72	—	−70	−68 (16)	—	−61	−61 (16)	5	714-04/1

(16) Typical
(29) Channels 2 and M30 @ M39
(30) Channels 2 and A @ 7

New introductions

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450/550 MHz POWER DOUBLING HYBRIDS

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 60 CH	Composite Triple Beat dB 77 CH	Cross Modulation dB 60 CH	Cross Modulation dB 77 CH	Noise Figure @ 450/550 MHz dB Max	Noise Figure Typ	Package/Style
MHW5185(36)	18	60	+46	−74 (28)	−65	—	−66	—	7	—	714-04/1
MHW6185(36)	18	77	+44	−71 (29)	—	−63	—	−63	7.5	—	714-04/1
MHW5225(36)	22	60	+46	−69(28)	−62	—	−60	—	6	5	714-04/1

450/550 MHz FEEDFORWARD HYBRIDS (Case 774-01/2)

Device	Hybrid Gain (Nominal) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 60 CH	Composite Triple Beat dB 77 CH	Cross Modulation dB 60 CH	Cross Modulation dB 77 CH	Noise Figure @ 450/550 MHz dB Max	Noise Figure Typ	Package/Style
FF124	24	60	+46	−84	−79	—	−75	—	10	—	825-02/1
FF124B	24	60	+46	−84	−79	—	−75	—	10	—	825A-01/1
FF224	24	77	+44	−86	—	−75	—	−70	11	—	825-02/1
FF224B	24	77	+44	−86	—	−75	—	−70	11	—	825A-01/1

General Purpose Wideband

A wide range of hybrid and silicon monolithic amplifiers is offered for low level signal amplification. Package type, gain, frequency of operation, output level and supply voltage combinations can be selected to fit the design engineer's specific requirements.

50 Ω HYBRIDS (Case 31A-03/2)

The MWA Series features excellent gain versus frequency flatness, temperature stability and are cascadable for high gain lineups. Construction techniques include thin film gold metal circuitry and hermetic TO-205AD package. MWA devices processed similarly to MIL-S-883, Method 5004.4, Class B, are available to special order.

Device	Frequency Range MHz	Gain dB Min/Typ	Supply Voltage Vdc	Output Level 1 dB Compression dBm	Noise Figure @ 250 MHz dB
MWA110	0.1–400	13/14	2.9	−2.5	4
MWA120	0.1–400	13/14	5	+8.2	5.5
MWA130	0.1–400	13/14	5.5	+18	7
MWA131	0–400	13/14	5.5	+20	5 (39)
MWA210	0.1–600	9/10	1.75	+1.5	6
MWA220	0.1–600	9/10	3.2	+10.5	6.5
MWA230	0.1–600	9/10	4.4	+18.5	7.5
MWA310	0.1–1000	7/8	1.6	+3.5	6.5
MWA320	0.1–1000	7/8	2.9	+11.5	6.7
MWA330	0.1–1000	—/6.2	4	+15.2	9

(28) Channels 2 and M13 @ M22
(29) Channels 2 and M30 @ M39
(36) Available in reverse voltage (−24 V) version (in Case 714C-04) by placing Suffix "R" after device number.
(39) NF @ f = 400 MHz

☐ New introductions

50 Ω–100 Ω HYBRIDS (Case 714-04/1)

The general purpose hybrid amplifiers listed are for broadband system applications requiring superior gain and current stability with temperature. The 50 to 100 ohm input and output impedances help simplify designs.

Device	Frequency Range MHz	Gain dB Min/Typ	Supply Voltage Vdc	Output Level 1 dB Compression mW/f (MHz)	Noise Figure @ 250 MHz dB
MHW591	1–250	34.5/36.5	13.6	700/100	5
MHW593	10–400	33/34.5	13.6	600/200	5
MHW590	10–400	31.5/34	24	800/200	5
MHW592	1–250	33.5/35	24	900/100	5

50 Ω MONOLITHIC

These monolithic amplifiers are fully cascadable and usable to frequencies over 3 GHz. External blocking capacitors are required along with an external bias resistor. Hermetic versions are available to special order in Case 303-01.

Device	Frequency Range MHz	Gain dB Typ @ 1 GHz	Recommended Operating Current mA	Output Level 1 dB Compression dBm Typ	Noise Figure @ 1500 MHz dB
Case 317-01/3					
MWA0204	DC–3000	11.5	25	7	6
MWA0304	DC–3000	11.5	35	12	6
Case 318A-05/4					
MWA0211L	DC–3000	11.5	25	7	6
MWA0311L	DC–3000	11.5	35	12	6
Case 303A-01/3					
MWA0270	DC–3000	12	25	7	6
MWA0370	DC–3000	12	35	12	6

4

STANDARD LINEAR HYBRIDS

The CA series of RF linear hybrid amplifiers consists of a family of medium power, broadband gain blocks in the CATV industry standard "CA" package. These amplifiers were designed for multi-purpose RF applications where linearity, dynamic range and wide bandwidth are of primary concern. Each amplifier is available in various package options. For hermetic package option add suffix "H" to part number except where noted (32). Four parts are available as indicated in a low profile package. Hermetic package parts are in Case 826-01/1 (for positive supply) or 826-01/2 (for negative supply).

Device	BW MHz	Gain Flatness ±dB	Gain/Freq. dB/MHz	P_{1dB} dBm	NF/Freq. dB/MHz	3rd Order Intercept Point/Freq. dBm/MHz	VSWR 50 Ω/75 Ω	V_S/I_S V/mA	Case/ Style
CA2800 (31)	10–400	1	17/50	29	8.5/300	44/300	2/1.3	24/200	714F-01/1
CA2810 (31)	10–350	1.5	33/50	29	8/300	43/300	2/1.3	24/300	714F-01/1
CA2813 (31)	40–300	1.25	34/50	22	5/300	40/300	2/1.3	15/160	714F-01/1
CA2818 (31)	1–200	1	18.5/50	29.5	5.5/150	47/150	2/1.3	24/205	714F-01/1
CA2820 (31)	1–520	1.5	30/100	26.5	8/500	37/500	2/	24/330	714M-01/2
CA2830 (31)	5–200	1	34.5/100	29	4.7/200	46/200	2/	24/300	714F-01/1
CA2833 (31)	5–200	1	34.5/100	29	4.7/200	46/200	2/	24/300	714G-01/1
CA2832 (31)	1–200	1	35.5/100	33	6/200	47/200	2/	28/435	714F-01/1
CA2842 (31)	30–300	1	22/100	30	5/100	46/300	1.5/	24/230	714F-01/1
CA2846 (31)	30–300	1	22/100	30	5/100	46/300	1.5/	24/230	714G-01/1
CA2850R (31)	40–100	0.2	17.5/100	25	4.5/70	40/70	1.3/	−19/125	714H-01/1
CA2851R (31)	40–100	0.2	17.5/100	25	4.5/70	40/70	1.3/	−19/125	714L-01/1
CA2870 (31)	20–400	1	34/100	27	7.5/400	45/300	2/	24/300	714M-01/1
CA2875R (31)	40–100	0.2	17.5/100	26	4.5/70	43/70	/1.07	−19/155	714H-01/1
CA2880R (31)	40–100	0.3	22/100	22	3/70	36/70	/1.2	−19/73	714L-01/1
CA2885 (32)	40–550	1	17.7/50	33	7/500	43/500	2/1.3	24/425	714F-01/1
CA4800 (31)	10–1000	0.5	17/100	26	7.5/1000	40/1000	2/	24/220	714P-01/2
CA4812 (31)	10–1000	0.5	17/100	26	7.5/1000	40/1000	2/	12/380	714P-01/3
CA4815 (31)	10–1000	0.5	17/100	26	7.5/1000	40/1000	2/	15/380	714P-01/3
CA5800 (31)	10–1000	0.5	15/100	30	8.5/1000	41/1000	2/	28/400	714P-01/2
CA5815 (31)	10–1000	0.5	16/100	30	8/1000	41/1000	2/	15/700	714P-01/3
CA5900	10–1200	0.5	15/100	30	8.5/1200	41/1200	2/	28/400	714P-01/2
CA5915	10–1200	0.5	15/100	30	8.5/1200	41/1200	2/	15/700	714P-01/3

(31) Available in Hi-Rel hermetic package manufactured compliant to MIL-A-28875. To order, insert an "R" in the part number following the prefix "CA" (Example, CAR2800).

(32) Not available in hermetic package

New introductions

4

SHP and DHP Linear

The SHP and DHP series of linear amplifiers consist of medium power, broadband, high gain amplifiers operating from 15 to 28 volt supplies. Both their wide dynamic and frequency ranges make them suitable for use in instrumentation, communications and military equipments.

SHP (Case 389A-01/1)

Device	BW (MHz)	Gain (dB)	VSWR 50 Ohms	DC Power	1 dB Compression W @ MHz	Third Order Intercept dBm @ MHz	Noise Figure dB @ MHz
SHP02-36-20	1–200	36	2:1	28 V/430 mA	2 @ 50 1.5 @ 200	+50 @ 50 +43 @ 200	5 @ 100 6 @ 200
SHP06-18-04	30–550	18	1.5:1	24 V/220 mA	0.8 @ 300 0.3 @ 550	+44 @ 300 +36 @ 550	6 @ 300 7.5 @ 550
SHP05-22-04	30–450	22	1.5:1	24 V/220 mA	0.8 @ 300 0.4 @ 450	+44 @ 300 +38 @ 450	5 @ 300 6 @ 450
SHP05-34-04	30–450	34	1.5:1	24 V/330 mA	0.8 @ 300 0.4 @ 450	+43 @ 300 +38 @ 450	5.5 @ 300 6 @ 450
SHP05-20-10	30–500	20	1.5:1	24 V/430 mA	2 @ 300 1 @ 500	+48 @ 300 +41 @ 500	5 @ 300 6 @ 500
SHP10-17-04	10–1000	17	2:1	24 V/220 mA	0.4 @ 500 0.4 @ 1000	+40 @ 500 +39 @ 1000	6.5 @ 500 7.5 @ 1000
SHP10-17-04-15	10–1000	17	2:1	15 V/400 mA	0.4 @ 500 0.4 @ 1000	+40 @ 500 +39 @ 1000	6.5 @ 500 7.5 @ 1000
SHP10-15-08	10–1000	15	2:1	28 V/400 mA	0.8 @ 500 0.7 @ 1000	+43 @ 500 +42 @ 1000	7.5 @ 500 8.5 @ 1000
SHP10-15-08-15	10–1000	15	2:1	15 V/700 mA	0.8 @ 500 0.7 @ 1000	+43 @ 500 +42 @ 1000	7.5 @ 500 8.5 @ 1000

DHP (Case 389-01/1)

Device	BW (MHz)	Gain (dB)	VSWR 50 Ohms	DC Power	1 dB Compression W @ MHz	Third Order Intercept dBm @ MHz	Noise Figure dB @ MHz
DHP02-36-40	1–200	36	2:1	28 V/870 mA	4 @ 50 3 @ 200	+53 @ 50 +46 @ 200	5.5 @ 100 6.5 @ 200
DHP05-36-10	30–500	36	1.5:1	24 V/600 mA	2 @ 300 1 @ 500	+48 @ 300 +41 @ 500	5 @ 300 6 @ 500
DHP05-18-20	30–500	18	1.5:1	24 V/830 mA	4 @ 300 2 @ 500	+51 @ 300 +44 @ 500	5.5 @ 300 6.5 @ 500
DHP10-14-15	10–1000	14	2:1	28 V/800 mA	1.5 @ 500 1.5 @ 1000	+45 @ 500 +44 @ 1000	8 @ 500 9 @ 1000
DHP10-32-08	10–1000	32	2:1	28 V/600 mA	0.8 @ 500 0.7 @ 1000	+43 @ 500 +42 @ 1000	6.5 @ 500 7.5 @ 1000

CRT Driver

These complete hybrid amplifiers are specifically designed for CRT driver applications requiring high frequency response and high voltage, such as high resolution color graphics video monitors. Gold metallized dice and substrates are used to insure high reliability and improved ruggedness.

Device	V_{CC} Volts	Gain (34) V/V	3 dB BW MHz	V_{out} (Max) Volts	Load	Package/Style
CR2424 (33)	60	12	145	50 P-P	6 to >20 pF	714G-01/1
CR2424R	−60	12	145	50 P-P	6 to >20 pF	714H-01/1
CAR2424H (35)	60	12	145	50 P-P	6 to >20 pF	826-01/1
CR2424H	60	12	145	50 P-P	6 to >20 pF	826-01/1
CR2425 (33)	60	12	145	50 P-P	6 to >20 pF	714F-01/1
CR3424	80	12	115	40 P-P	6 to >20 pF	714G-01/1
CR3424H	80	12	115	40 P-P	6 to >20 pF	826-01/1
CR3425	80	12	115	40 P-P	6 to >20 pF	714F-01/1
CR3424R	−80	12	115	40 P-P	6 to >20 pF	714H-01/1
CR3425R	−80	12	115	40 P-P	6 to >20 pF	714H-01/1

RF Transceiver Modules

These modules are designed for use in PC networks handling data rates up to 2 Mbps. Surface mount construction results in extremely small size — < 8 square inches of circuit board area. Each module provides high spectral purity and selectivity to prevent interference when used with other CATV signals on the cable interconnect system.

Device	Transmit P_O dBmV @ 75 Ohms Typ	Transmit Freq. MHz	Receive Freq. MHz	Input Level dBmV @ 75 Ohms Typ	Package/Style
MHW10000	54	50.75	219	8.5	817-01/1
MHW10001	54	56.75	249	8.5	817-01/1
MHW10002	54	62.75	255	8.5	817-01/1
MHW10003	54	50.75	243	8.5	817-01/1

(33) Text fixtures available. To order add "TF" suffix to device number
(34) Insertion gain; 50 ohm source
(35) Hi-Rel Hermetic packaged amplifier, manufactured compliant to MIL-A-28875

New introductions

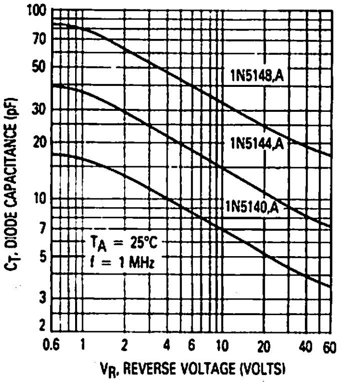
Tuning and Switching Diodes

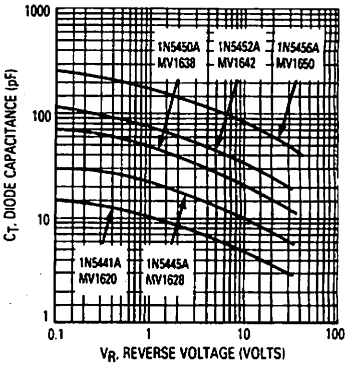
Tuning Diodes
Abrupt Junction

Voltage variable capacitance diodes for electronic tuning and control of RF circuits through UHF frequencies. Utilized for television tuning and AFC circuits.

TYPICAL CHARACTERISTICS

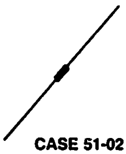
Diode Capacitance versus Reverse Voltage





4

General-Purpose
Glass



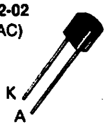
CASE 51-02
DO-204AA
(DO-7)

		• High Q • Capacitance TOL 10% — No Suffix 5% — Suffix A			• High Q • Controlled CR • Capacitance TOL 10% – A, 5% – B			• General-Purpose		
		Maximum Working Voltage								
		60 Volts			30 Volts			20 Volts		
		Cap Ratio C4/C60 Min	**Q @ 4 V 50 MHz Min**	**Device Type**	**Cap Ratio C2/C30 Min**	**Q @ 4 V 50 MHz Min**	**Device Type**	**Cap Ratio C2/C20 Min**	**Q @ 4 V 50 MHz Min**	**Device Type**
C_T Nominal Capacitance pF ±10% @ V_R = 4 V f = 1 MHz	**6.8**	2.7	350	1N5139,A	2.5	450	1N5441A	2	300	MV1620
	10	2.8	300	1N5140,A	2.6	400	1N5443A	2	300	MV1624
	12	2.8	300	1N5141,A	2.6	400	1N5444A	2	300	MV1626
	15	2.8	250	1N5142,A	2.6	450	1N5445A	2	250	MV1628
	18	2.8	250	1N5143,A	2.6	350	1N5446A	2	250	MV1630
	22	3.2	200	1N5144,A	2.6	350	1N5448A	2	250	MV1634
	27	3.1	200	1N5145,A	2.6	350	1N5449A	2	200	MV1636
	33	3.2	200	1N5146,A	2.6	350	1N5450A	2	200	MV1638
	39	3.	200	1N5147,A	2.6	300	1N5451A	2	200	MV1640
	47	3.2	200	1N5148,A	2.6	250	1N5452A	2	200	MV1642
	56				2.6	200	1N5453A	2	150	MV1644
	82				2.7	175	1N5455A	2	150	MV1648
	100				2.7	175	1N5456A	2	150	MV1650

General-Purpose

Plastic

CASE 182-02
(TO-226AC)



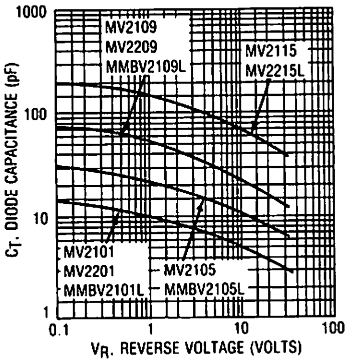
CASE 318-07
(TO-236AB)

	• Low-Cost • High Volume			• Low-Cost • High Volume		
	Maximum Working Voltage					
	30 Volts			30 Volts		
	CASE 182-02 2-Lead TO-92			CASE 318-07 TO-236AB		
C_T Nominal Capacitance pF ±10% @ V_R = 4 V f = 1 MHz	Cap Ratio C2/C30 Min	Q @ 4 V 50 MHz Min	Device Type	Cap Ratio C2/C30 Min	Q @ 4 V 50 MHz Min	Device Type
6.8	2.5	450	MV2101	2.5	400	MMBV2101L
10	2.5	400	MV2103	2.5	350	MMBV2103L
12	2.5	400	MV2104	2.5	350	MMBV2104L
15	2.5	400	MV2105	2.5	350	MMBV2105L
18	2.5	350	MV2106	2.5	300	MMBV2106L
22	2.5	350	MV2107	2.5	300	MMBV2107L
27	2.5	300	MV2108	2.5	250	MMBV2108L
33	2.5	200	MV2109	2.5	200	MMBV2109L
47	2.5	150	MV2111			
68	2.6	150	MV2113			
82	2.6	100	MV2114			
100				2.6	100	MV2115

4

TYPICAL CHARACTERISTICS

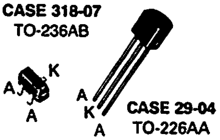
Diode Capacitance versus Reverse Voltage



High Capacitance

Dual Diodes

CASE 318-07
TO-236AB



CASE 29-04
TO-226AA
(TO-92)

- High Q
- Guaranteed Capacitance Range
- Monolithic Dual

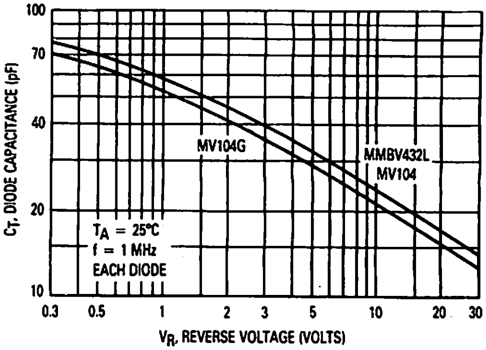
Maximum Working Voltage
32 Volts

C_T Capacitance			Cap Ratio C3/C30 Min	Q @ 3 V 50 MHz Min	Device Type
pF		@ V_R			
Min	Max	Volts			
34	39	3	2.5	100	MV104G(1)
37	42	3	2.5	100	MV104(1)
43	48.1	2	1.5*	100	MMBV432L(2)

(1) Case 29 (2) Case 318 *C2/C8

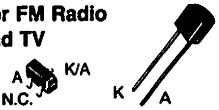
TYPICAL CHARACTERISTICS

Diode Capacitance versus Reverse Voltage



Tuning Diodes Hyper-Abrupt Junction

For FM Radio and TV



CASE 318-07 TO-236AB — CASE 182-02 TO-226AC

- High Q
- Guaranteed Capacitance Range

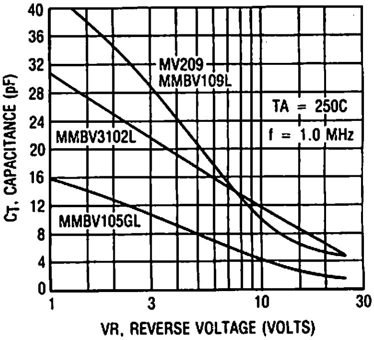
Maximum Working Voltage
30 Volts

C_T Capacitance			Cap Ratio C3/C25 Min	Q @ 3 V 50 MHz Typ	Device Type
pF		@ V_R			
Min	Max	Volts			
1.8	2.8	25	4	350	MMBV105G*
20	25	3	4.5	300	MMBV3102*
26	32	3	5	250	MMBV109*
26	32	3	5	250	MV209**

*Case 318 **Case 182

TYPICAL CHARACTERISTICS

Diode Capacitance versus Reverse Voltage

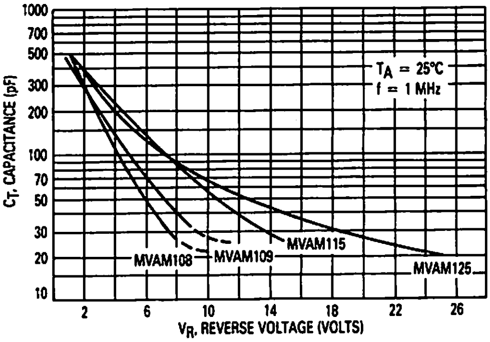


For AM Radio, Disc Drives

CASE 182-02 (TO-226AC)

- High Capacitance Ratio
- Guaranteed Diode Capacitance
- Close Matching

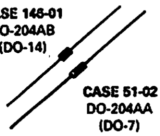
C_T		Q @ 1 Vdc, 1 MHz = 150 (Min)			
V_R = 1 V, f = 1 MHz pF		$V_{BR(R)}$ Min	Cap Ratio Min	@ V_R Volts	Device Type
Min	Max				
440	560	12	15	1/8	MVAM108
400	520	15	12	1/9	MVAM109
440	560	18	15	1/15	MVAM115
440	560	28	15	1/25	MVAM125



For High Capacitance and High Reliability Applications

100% Screening to High Rel electrical and environmental specifications, H suffix.

CASE 146-01 DO-204AB (DO-14)



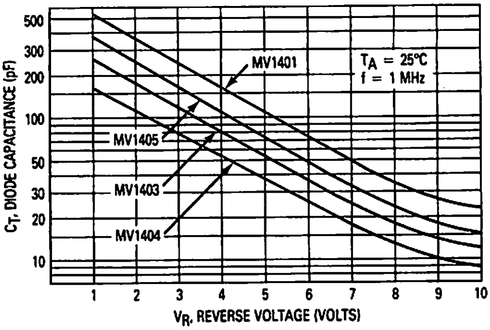
CASE 51-02 DO-204AA (DO-7)

- Hyper-Abrupt
- High Tuning Ratio
- High Rel — Suffix H

Maximum Working Voltage
12 Volts

C_T, Nominal Capacitance pF Nom ± 20%	@ V_R Volts	Cap Ratio C2/C10 Min	Q @ 2 V 1 MHz Min	Device Type Case 51	Device Type Case 146
120	2	10	200	MV1404,H	
175	2	10	200	MV1403,H	
250	2	10	200	MV1405,H	
550*	1	14(1)	200		MV1401,H

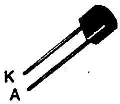
* ±15% (1)Cap Ratio @ C1/C10 V



4

Hot-Carrier (Schottky) Diodes

Hot-Carrier diodes are ideal for VHF and UHF mixer and detector applications as well as many higher frequency applications. They provide stable electrical characteristics by eliminating the point-contact diode presently used in many applications.



CASE 182-02

CASE 318-07

CASE 318-05

STYLE 8:
PIN 1. ANODE
2. N.C.
3. CATHODE

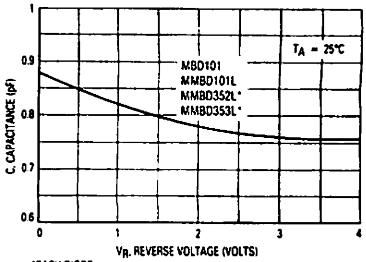
STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE/ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE/ANODE

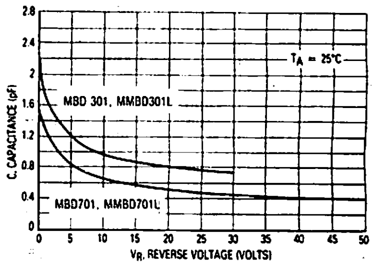
$V_{(BR)R}$ $I_R = 10\ \mu A$ Volts Min	C_T f = 1 MHz pF Max	@ V_R Volts	V_F $I_F = 10$ mA Volts Max	I_R nA Max	@ V_R Volts	Device Type
CASE 182, STYLE 1						
4	1	0	0.6	250	3	MBD101
30	1.5	15	0.6	200	25	MBD301
70	1	20	1.2	200	35	MBD701
CASE 318, STYLE 8						
4	1	0	0.6	250	3	MMBD101L
30	1.5	15	0.6	200	25	MMBD301L
70	1	20	1.2	200	35	MMBD701L
DUAL DIODES, CASE 318, STYLE 11*, STYLE 19**						
4	1	0	0.6	250	3	MMBD352L*
4	1	0	0.6	250	3	MMBD353L**

TYPICAL CHARACTERISTICS

Capacitance versus Reverse Voltage



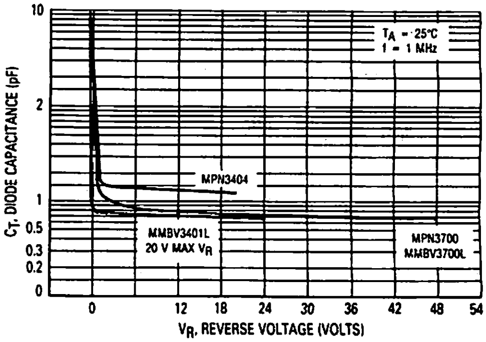
*EACH DIODE



PIN Switching Diodes

. . . designed for VHF band switching and general-purpose switching.

$V_{(BR)R}$ $I_R = 10\ \mu Adc$ Volts Min	R_S $I_F = 10$ mAdc f = 100 MHz Ohms Max	C_T $V_R = 20$ V f = 1 MHz pF Max	Device Type
CASE 182, STYLE 1			
20	0.85	2	MPN3404
200	1	1	MPN3700
CASE 318, STYLE 8			
35	0.7	1	MMBV3401L
200	1	1	MMBV3700L



4

RF Chips

Ordering and Shipping Information

Minimum Order Requirements:

In conjunction with Motorola corporate policy the minimum order, release or line/line shipment of standard product is $200.

The minimum order, release or line item shipment of non-standard product is **$2500 unless** otherwise stated at the time of quotation, order entry or acknowledgement.

Packaging:

Multi-Pak — Motorola supplies all discrete semiconductors in the industry standard multi-pak. (Waffle type carrier, Figure 1.) This is a 2 x 2 or 4 x 4 waffle type carrier with a separate hole for each die. Chips are 100% visually inspected with the rejects removed. There is no suffix associated with the multi-pak carrier.

Circle Pak (CP Suffix) (See Figure 2) — The wafer is placed on a sticky film before being sawed. Each wafer is completely sawed through with the back side against the PVC film. The die stick to the PVC film and maintain exact wafer orientation and spacing. This packaging method also offers the convenience of storage with original orientation and spacing even after a portion of the wafer is used. The evacuated plastic bag is thermally sealed holding the contents securely with no die movement. Die can be removed from the sticky film by a sharp ejector-pin pushing a die up and a vacuum needle manually picking it up. This package can also be handled by an automatic die loader with some minor adjustments. To order this package, the suffix CP must appear with the part number.

Wafer Pak (WP Suffix) (See Figure 3) — The pak contains a wafer that is 100% electrically tested. With the rejects inked, the wafer is left unsawed and is packaged with protective cardboard in a vacuum sealed plastic bag. The WP suffix must appear after the chip part number.

Heatspreader (See Figure 4) — Some chips (indicated by footnote in the preferred parts list) are also available mounted with eutectic bonding to copper heatspreaders that have been plated with nickel and gold. The use of heatspreaders increases thermal conductivity and allows solder reflow attachment of the die-heatspreader assembly.

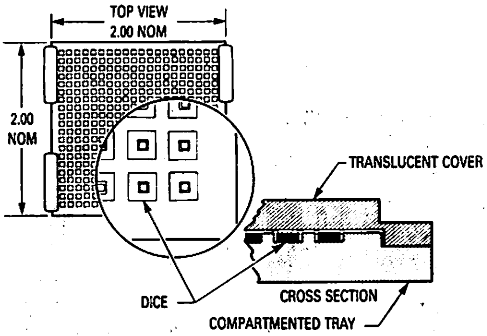


Figure 1. Multi-Pak (No Suffix)

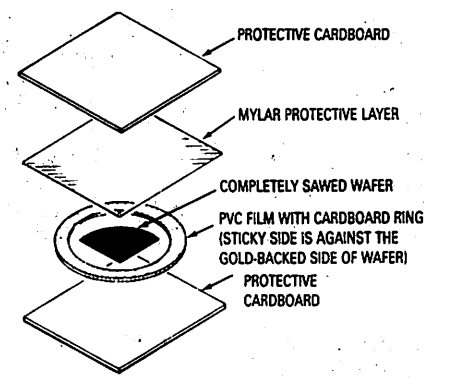


Figure 2. Circle Pak (CP Suffix)

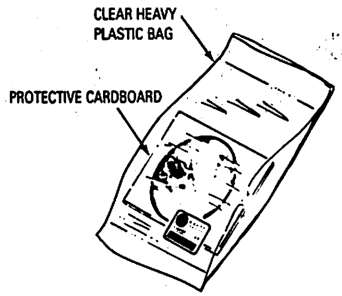


Figure 3. Wafer Pak (WP Suffix)

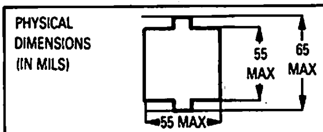
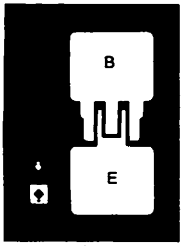


Figure 4. Heatspreader

Die Geometries

1



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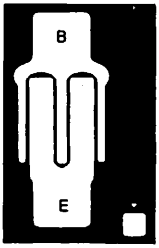

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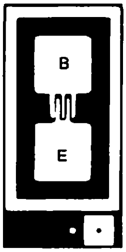

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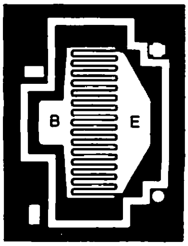

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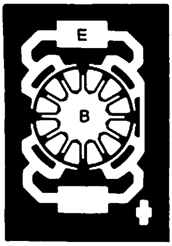

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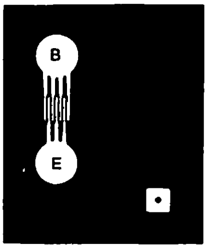

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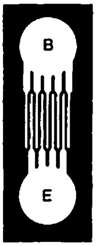

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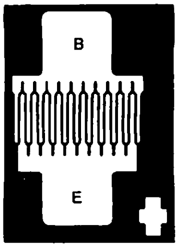

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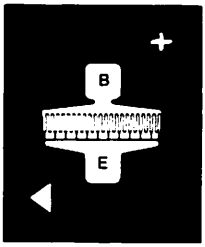

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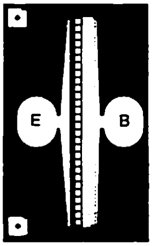

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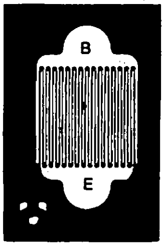

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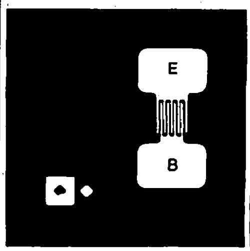

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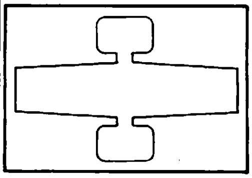

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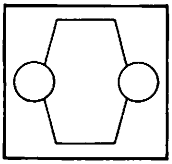

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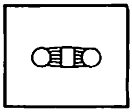


B = Base
E = Emitter

Preferred Parts List

Standard D.C. Parameters (at 25°C) — $V_{(BR)CBO}$, $V_{(BR)CEO}$, $V_{(BR)EBO}$, h_{FE} (d.c. current gain)
Special Request Parameters — I_{CEO}, I_{CES}, I_{CEX}, I_{EBO}, $V_{CE(sat)}$, $V_{BE(sat)}$, f_T, C_{CB}, C_{EB}, h_{FE} (ac), NF (Noise Figure), G_{PE}
Front Metallization Thickness — a minimum of 10,000 Å
Back Metallization Thickness — a minimum of 3,000 Å–24,000 Å

					Bond Pad Size		Metallization		Packaging			
Standard Part #	**Chip Part #**	**Die Geometry Reference #**	**Die Size Inches 1/1000**	**Die Thickness Inches 1/1000**	**Inches 1/1000 Base**	**Inches 1/1000 Emitter**	**Front**	**Back**	**Multi (none)**	**Wafer (WP)**	**Circle (CP)**	**Heat-spreader**
2N2857	2C2857	1	14x16	4–8	4.0x4.8	4.0x4.8	Al	Au	•	•	•	
2N3866	2C3866	2	15x22	4–8	4x4	4x4	Al	Au	•	•	•	
2N4957	2C4957	3	12x22	4–8	4x4	4x4	Al	Au	•	•	•	
2N5108	2C5108	11	12x17	4–8	2.5x2.1	2.5x2.1	Au	Au	•	•	•	
2N5160	2C5160	4	15x20	4–8	2.2x3.2	2.2x3.2	Al	Au	•	•	•	
2N5583	2C5583	4	15x20	4–8	2.2x3.2	2.2x3.2	Au	Au	•	•	•	
2N5943	2C5943	2	15x22	4–8	4x4	4x4	Al	Au	•	•	•	
BFR90	BFRC90	6	14x16	4–8	2.8 dia.	2.8 dia.	Au	Au	•	•	•	
BFR91	BFRC91	7	14x16	4–8	2.8 dia.	2.8 dia.	Au	Au	•	•	•	
BFR96	BFRC96	8	13x16	4–8	3.4x3.4	3.4x3.4	Au	Au	•	•	•	
LT1817	CD1880 (37)(38)	14	22x22	4–5	3.6 dia.	3.6 dia.	Au	Au	•			•
LT3005	CD3240 (37)(38)	13	16x25	4–5	2.75x3.75	2.75x3.75	Au	Au	•			•
LT4217	CD6150 (37)(38)	13	16x25	4–5	2.75x3.75	2.75x3.75	Au	Au	•			•
LT4700	CD3660 (37)(38)	15	17x17	4–5	1.5 dia.	1.5 dia.	Au	Au	•			•
LT5217	CD4880 (37)(38)	13	16x25	4–5	2.75x3.75	2.75x3.75	Au	Au	•			•
LT5817	CD5880 (37)(38)	14	22x22	4–5	3.6 dia.	3.6 dia.	Au	Au	•			•
MM4049	MMC4049	3	12x22	4–8	4x4	4x4	Al	Au	•	•	•	
MRF2369	MRFC2369	9	15x16	4–8	2.2x2.2	2.2x2.2	Au	Au	•	•	•	
MRF559	MRFC559	5	15x24	4–8	3.5 dia.	2.16x4	Au	Au	•	•	•	
MRF544	MRFC544	10	34x27	4–8	3x4	3x4	Au	Au	•	•	•	
MRF545	MRFC545	10	34x27	4–8	3x4	3x4	Au	Au	•	•	•	
MRF901	MRFC901	12	15x15	4–8	4.0x2.6	4.0x2.6	Au	Au	•	•	•	
MRF904	MRFC904	12	15x15	4–8	4.0x2.6	4.0x2.6	Au	Au	•	•	•	

Samples available upon request, contact the Motorola Sales Office. •Available Packaging

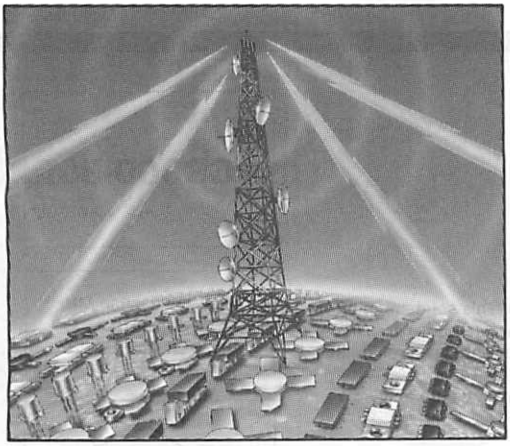
(37) To order CHIP mounted on a heatspreader, change prefix to "CH."
(38) To order high reliability chip with SEM qualifications and lot acceptance per MIL-STD-750 and 883, change prefix to "HD" or "HH" for die alone or die mounted on heatspreader respectively.

Storage and Handling Information

It is recommended that all Motorola die be stored at room temperature in an inert environment after removal of the seal from the original shipping package.

Special Electro-Static Discharge (ESD) precautions should be taken to avoid damaging the chips. Motorola recommends storage in the original ESD shipping package.

4



Volume II

Amplifier Data Sheets

5

ACR900-30E

Advance Information

The RF Line

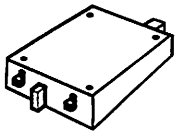
Linear Power Amplifier

**30 W — 890–960 MHz
LINEAR
POWER AMPLIFIER**

... specifically designed for cellular radio base station applications. This solid state, high power amplifier incorporates microstrip technology and utilizes discrete power transistors with gold metallization and diffused emitter ballast resistors for enhanced reliability and ruggedness.

Custom versions with modified electrical and mechanical specifications are available upon request.

- 890–960 MHz
- 30 W — P_{out}
- 25 V — V_{CC}
- 18 dB Gain
- Class AB



CASE 389J-02, STYLE 1
(ACR)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Voltage Supply	V_{CC}	30	Vdc
Operating Temperature Range (Note 1)	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 50°C, 50 Ω system, V_{CC} = 25 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth	BW	890	—	960	MHz
Power Gain (P_{out} = 30 W, f = 960 MHz)	G_p	18	—	—	dB
Supply Current (P_{out} = 30 W)	I_{CC}	—	3	—	A
Input Return Loss (P_{out} = 30 W)	IRL	15	20	—	dB
Efficiency (P_{out} = 30 W, f = 960 MHz)	η	—	40	—	%
Output Return Loss (P_{out} = 30 W)	ORL	15	20	—	dB
Load Mismatch (P_{out} = 30 W, f = 960 MHz, Load VSWR = 5:1, All Phase Angles)	ψ	No degradation in power output			

Note 1. Case Temperature is measured at base plate.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

AMR175-60

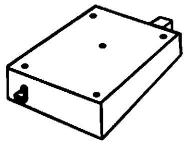
The RF Line
Linear Power Amplifier

... specifically designed for VHF land mobile base station applications. Microstrip design combined with the use of the most modern bipolar RF power transistor technology assures a reliable, cost effective complete power amplifier.

Custom versions with modified electrical and mechanical specifications are available upon request.

- 145–175 MHz
- 60 W — P_{out}
- 28 V — V_{CC}
- Class AB

60 W — 145–175 MHz
LINEAR
POWER AMPLIFIER



CASE 389K-01, STYLE 1
(AMR)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Voltage Supply	V_{CC}	30	Vdc
Operating Temperature Range (Note 1)	T_C	−20 to +70	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 70°C, 50 Ω system, V_{CC} = 28 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth	BW	145	—	175	MHz
Power Gain (P_{out} = 60 W, f = 175 MHz)	G_p	10	—	—	dB
Supply Current (P_{out} = 60 W)	I_{CC}	—	4.2	—	A
Input Return Loss (P_{out} = 60 W)	IRL	10	12	—	dB
Load Mismatch (P_{out} = 60 W, f = 175 MHz, Load VSWR = 20:1, All Phase Angles)	ψ	No degradation in power output			
Gain Flatness (P_{out} = 60 W, BW = 145–175 MHz)	G_F	—	—	±1	dB

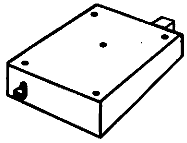
Note 1. Case Temperature is measured at base plate.

5

The RF Line
Linear Power Amplifier

AMR225-60

60 W — 180–225 MHz
LINEAR
POWER AMPLIFIER



CASE 389K-01, STYLE 1
(AMR)

. . . specifically designed for high VHF band land mobile base station applications. Microstrip design combined with the use of the most modern bipolar RF power transistor technology assures a reliable, cost effective complete power amplifier.

Custom versions with modified electrical and mechanical specifications are available upon request.

- 180–225 MHz
- 60 W — P_{out}
- 28 V — V_{CC}
- Class AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Voltage Supply	V_{CC}	30	Vdc
Operating Temperature Range (Note 1)	T_C	−20 to +90	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 70°C, 50 Ω system, V_{CC} = 28 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth	BW	180	—	225	MHz
Power Gain (P_{out} = 60 W, f = 225 MHz)	G_p	10	—	—	dB
Supply Current (P_{out} = 60 W)	I_{CC}	—	4.2	—	A
Input Return Loss (P_{out} = 60 W)	IRL	10	12	—	dB
Load Mismatch (P_{out} = 60 W, f = 225 MHz, Load VSWR = 20:1, All Phase Angles)	ψ	No degradation in power output			
Gain Flatness (P_{out} = 60 W, BW = 180–225 MHz)	G_F	—	—	±1.25	dB

Note 1. Case Temperature is measured at base plate.

5

AMR440-60

The RF Line

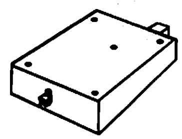
Linear Power Amplifier

... specifically designed for high UHF land mobile base station applications. Microstrip design combined with the use of the most modern bipolar RF power transistor technology assures a reliable, cost effective complete power amplifier.

Custom versions with modified electrical and mechanical specifications are available upon request.

- 400–440 MHz
- 60 W — P_{out}
- 28 V — V_{CC}
- Class AB

**60 W — 400–440 MHz
LINEAR
POWER AMPLIFIER**



CASE 389L-02, STYLE 1
(AMR)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Voltage Supply	V_{CC}	30	Vdc
Operating Temperature Range (Note 1)	T_C	−20 to +70	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 70°C, 50 Ω system, V_{CC} = 28 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth	BW	400	—	440	MHz
Power Gain (P_{out} = 60 W, f = 440 MHz)	G_p	7	—	—	dB
Supply Current (P_{out} = 60 W)	I_{CC}	—	4.5	—	A
Input Return Loss (P_{out} = 60 W)	IRL	10	12	—	dB
Load Mismatch (P_{out} = 60 W, f = 440 MHz, Load VSWR = 20:1, All Phase Angles)	ψ	No degradation in power output			
Gain Flatness (P_{out} = 60 W, BW = 400–440 MHz)	G_r	—	—	±0.5	dB

Note 1. Case Temperature is measured at base plate.

5

AMR470-60

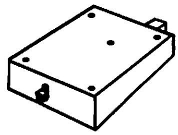
The RF Line
Linear Power Amplifier

... specifically designed for UHF land mobile base station applications. Microstrip design combined with the use of the most modern bipolar RF power transistor technology assures a reliable, cost effective complete power amplifier.

Custom versions with modified electrical and mechanical specifications are available upon request.

- 440–470 MHz
- 60 W — P_{out}
- 28 V — V_{CC}
- Class AB

**60 W — 440–470 MHz
LINEAR
POWER AMPLIFIER**



CASE 389L-02, STYLE 1
(AMR)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Voltage Supply	V_{CC}	30	Vdc
Operating Temperature Range (Note 1)	T_C	−20 to +70	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 70°C, 50 Ω system, V_{CC} = 28 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth	BW	440	—	470	MHz
Power Gain (P_{out} = 60 W, f = 470 MHz)	G_p	7	—	—	dB
Supply Current (P_{out} = 60 W)	I_{CC}	—	4.5	—	A
Input Return Loss (P_{out} = 60 W, BW = 440–470 MHz)	IRL	10	12	—	dB
Load Mismatch (P_{out} = 60 W, f = 470 MHz, Load VSWR = 20:1, All Phase Angles)	ψ	No degradation in power output			
Gain Flatness (P_{out} = 60 W, BW = 440–470 MHz)	G_r	—	—	±0.5	dB

Note 1. Case Temperature is measured at base plate.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

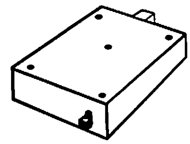
AMR900-60

The RF Line
Linear Power Amplifier

. . . designed for cellular radio base station applications in the 860–900 MHz frequency range. This solid state, Class B amplifier incorporates microstrip circuit technology and linear push-pull transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Wide Bandwidth 800–960 MHz (without retuning)
- 50 Ohm Input/Output Impedance
- Specified 24 Volt Characteristics:
  Output Power — 60 Watts
  Power Gain — 7 dB Typ
- Gold Metallized Push-Pull Transistors Give Broadband Performance and Excellent Reliability

60 W — 800–960 MHz
LINEAR
POWER AMPLIFIER



CASE 389B-02, STYLE 2
(AMR)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	25	Vdc
Supply Current	I_{CC}	6	Adc
Storage Temperature Range	T_{stg}	−40 to +100	°C
Operating Temperature Range	T_C	−20 to +70	°C

ELECTRICAL CHARACTERISTICS (T_C = 50°C, V_{CC} = 24 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 24 V, P_{out} = 50 W)	I_{CC}	—	4	—	mA
Power Gain (f = 800–960 MHz, P_{ref} = 50 W)	G_P	—	7	—	dB
Bandwidth (Continuous without retuning)	BW	800	—	960	MHz
Source/Load Return Loss	R_L	—	—	20	dB
Input/Output Return Loss (f = 800–960 MHz)	IRL/ORL	10	15	—	dB
Load Mismatch (P_{out} = 50 W, f = 960 MHz, Load VSWR = 5:1 Typ)	ψ	No Degradation in Performance			

Note 1. Case Temperature is measured at base plate.

5

TYPICAL CHARACTERISTICS

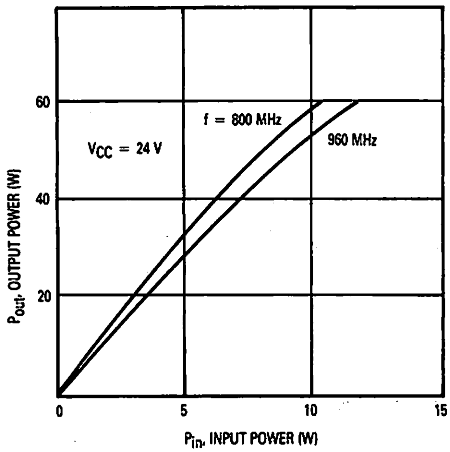


Figure 1. Output Power versus Input Power

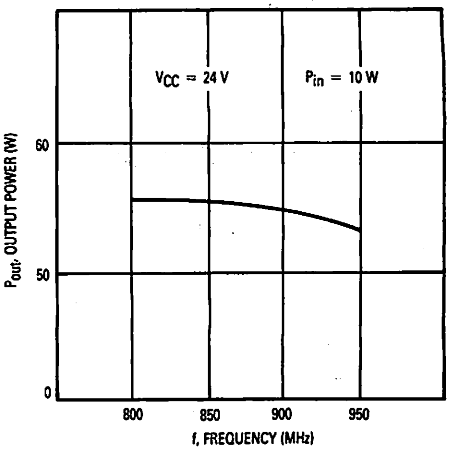


Figure 2. Output Power versus Frequency

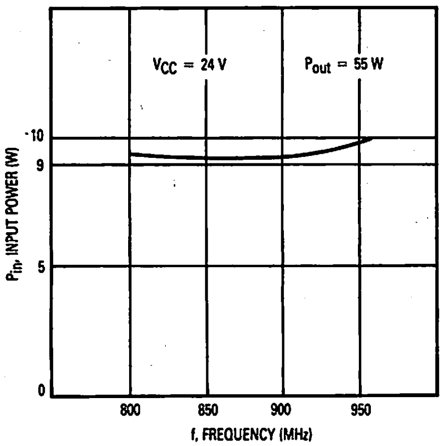


Figure 3. Input Power versus Frequency

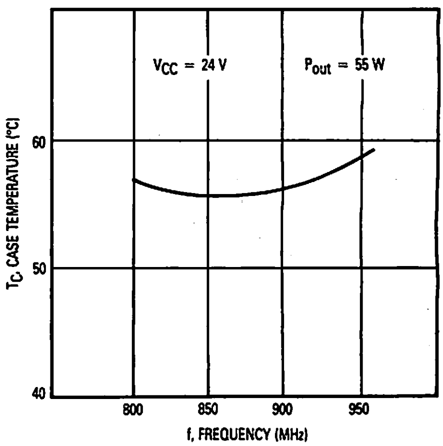


Figure 4. Case Temperature versus Frequency

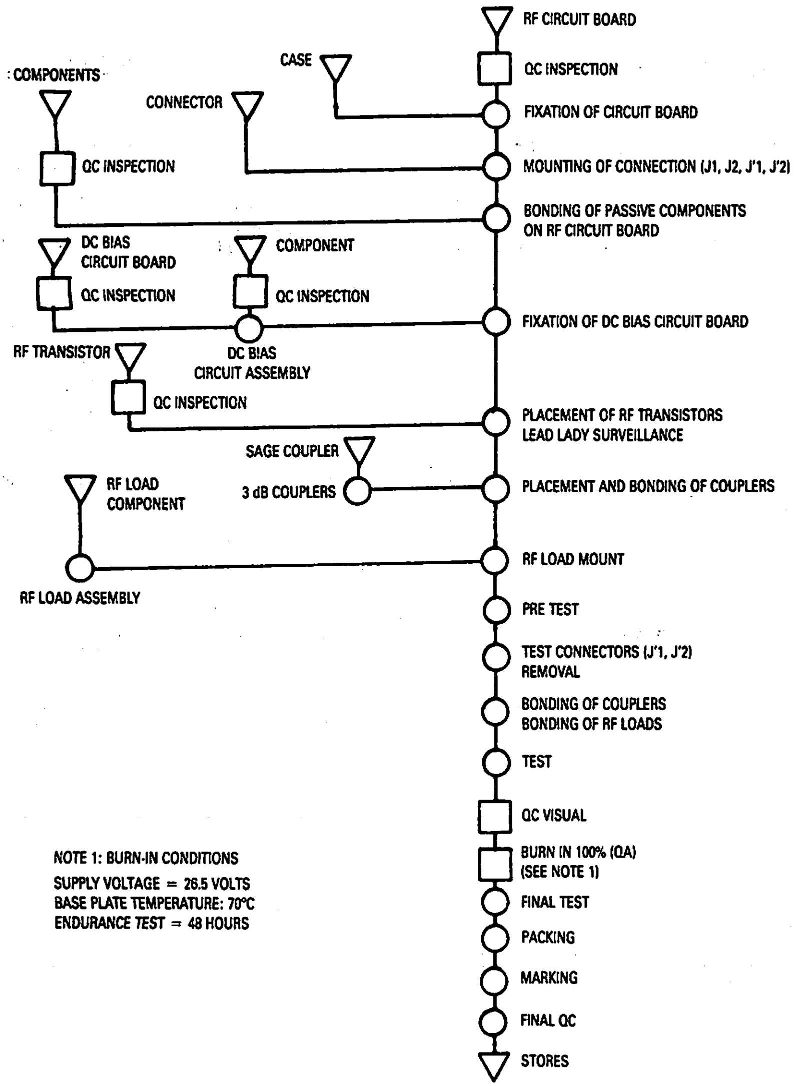


Figure 5. Manufacturing Flow Chart Operation

5

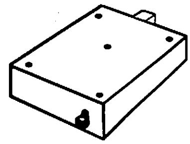
Advance Information

The RF Line

Linear Power Amplifier

AMR900-60A

**30 W — 800–960 MHz
LINEAR
POWER AMPLIFIER**



CASE 389B-02, STYLE 2
(AMR)

. . . specifically designed for cellular radio cell enhancer applications. This solid state, high power amplifier incorporates microstrip technology and utilizes discrete power transistors with gold metallization and diffused emitter ballast resistors for enhanced reliability and ruggedness.

Custom versions with modified electrical and mechanical specifications are available upon request.

- 800–960 MHz
- 30 W — P_{out}
- 26 V — V_{CC}
- 10 dB Gain, Class A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Voltage Supply	V_{CC}	27	Vdc
Operating Temperature Range (Note 1)	T_C	−20 to +70	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 50°C, 50 Ω system, V_{CC} = 26 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth	BW	800	—	960	MHz
Power Gain (P_{out} = 30 W, f = 960 MHz)	G_p	10	11	—	dB
Power Output @ 1 dB Gain Compression (Reference to P_{out} = 30 W, f = 960 MHz)	$P_{out(1\ dB)}$	25	28	—	W
Supply Current (P_{out} = 20 W)	I_{CC}	—	3.6	—	A
Input Return Loss (P_{out} = 30 W)	IRL	15	—	—	dB
Output Return Loss (P_{out} = 30 W)	ORL	15	—	—	dB
Load Mismatch (P_{out} = 20 W PEP, f = 960 MHz, Load VSWR = ∞:1, All Phase Angles)	ψ	No degradation in power output			
Intermodulation Distortion — 2 tones (P_{out} PEP = 27 W, f = 960 MHz, Δf = 1.6 MHz, I_C = 3.6 A)	IMD	—	—	−30	dB

Note 1. Case Temperature is measured at base plate.

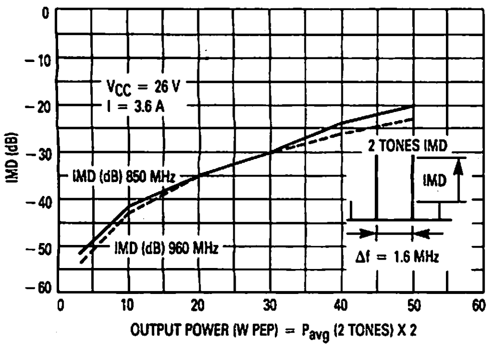


Figure 1. IMD versus Output Power

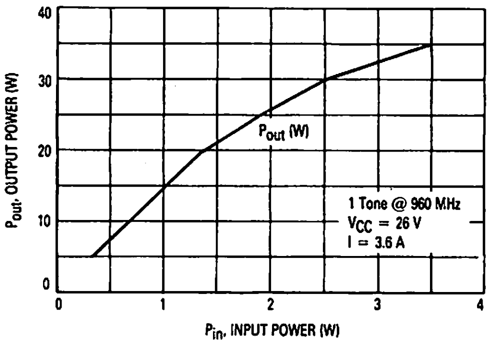


Figure 2. Output Power versus Input Power

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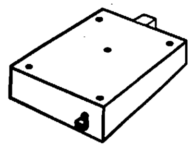
The RF Line
Linear Power Amplifier

ATV5030

**20 W — 470–860 MHz
LINEAR
POWER AMPLIFIER**

... a solid state Class A amplifier specifically designed for TV transposers and transmitters. This amplifier incorporates microstrip technology and discrete linear push-pull transistors with gold metallization and diffused emitter ballast resistors to enhance ruggedness and reliability.

- 470–860 MHz
- 20 W — P_{out}
- 26.5 V — V_{CC}
- 8.5 dB Typ Gain, Class A



CASE 389B-02, STYLE 1
(AMR)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Voltage Supply	V_{CC}	27	Vdc
Supply Current	I_{CC}	4	Adc
Operating Temperature Range (Note 1)	T_C	−20 to +70	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 50°C, 50 Ω system, V_{CC} = 26.5 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth	BW	470	—	860	MHz
Power Gain (P_{ref} = 20 W, 3 tones)	G_p	7.5	8.5	—	dB
Power Output @ 1 dB Gain Compression (Reference to P_{out} = 20 W)	$P_{out(1\ dB)}$	25	28	—	W
Supply Current (P_{out} = 20 W)	I_{CC}	—	3.8	—	A
Input Return Loss (P_{out} = 20 W)	IRL	15	—	—	dB
Output Return Loss (P_{out} = 20 W)	ORL	15	—	—	dB
Load Mismatch (P_{ref} = 20 W, 3 tones, f = 860 MHz, Load VSWR = ∞:1, All Phase Angles)	ψ	No degradation in power output			
Gain Flatness (P_{ref} = 20 W, 3 tones, BW = 470 to 860 MHz)	G_r	—	±0.5	±0.8	dB
Intermodulation Distortion — 3 tones (f = 860 MHz, V_{CE} = 25.5 V, P_{ref} = 20 W, Vision Carrier = −7 dB, Sound Carrier = −8 dB, Sideband Signal = −16 dB, Specification TV05001)	IMD_1	—	−52	−51	dB
Intermodulation Distortion (IDEM) (f = 860 MHz, V_{CE} = 25.5 V, P_{ref} = 20 W, Vision Carrier = −10 dB, Sound Carrier = −8 dB, Sideband Signal = −16 dB)	IMD_2	—	−55	−54	dB

Notes: 1. Case Temperature is measured at base plate.

TYPICAL CHARACTERISTICS

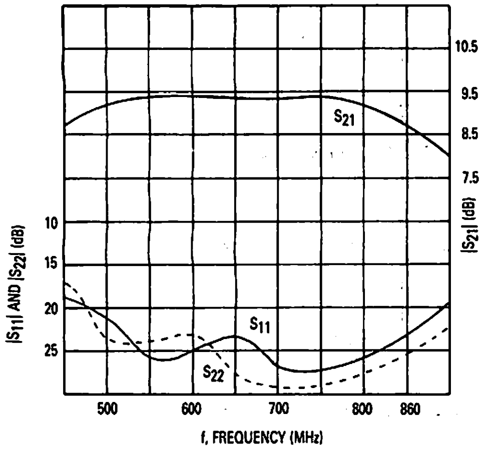


Figure 1. Small-Signal « S » Parameter Magnitude versus Frequency

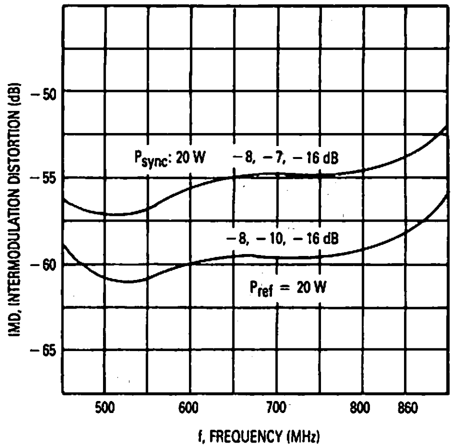


Figure 2. Intermodulation versus Frequency

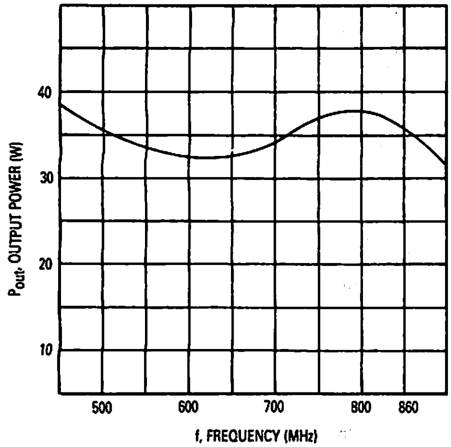


Figure 3. Output Power at 1 dB Gain Compression versus Frequency

* 3 tones test method:

IMD1: Vision carrier — 8 dB, sound carrier — 7 dB Sideband signal — 16 dB; Zero dB corresponds to peak sync level.

IMD2: Vision carrier — 8 dB, sound carrier — 10 dB Sideband signal — 16 dB; Zero corresponds to reference level.

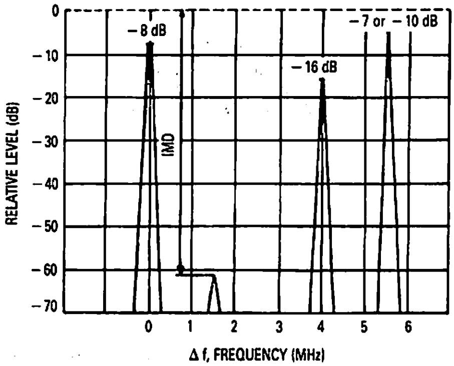


Figure 4. Relative Level versus Frequency

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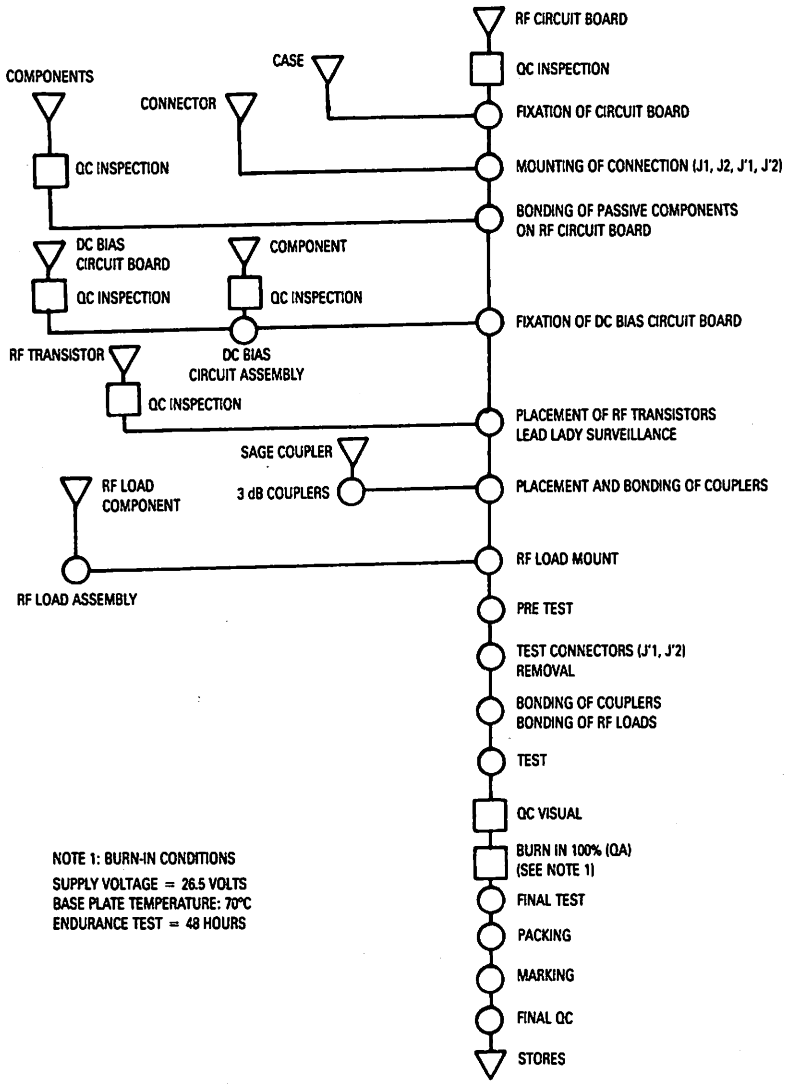


Figure 5. Manufacturing Flow Chart Operation

ATV5090B

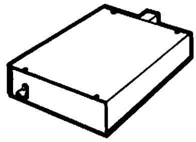
The RF Line

Linear Power Amplifier

. . . a solid state Class AB amplifier specifically designed for TV transposers and transmitters. This amplifier incorporates microstrip technology and discrete linear push-pull transistors with gold metallization and diffused emitter ballast resistors to enhance ruggedness and reliability.

- 470–860 MHz
- 90 W — P_{out}
- 28 V — V_{CC}
- 7 dB Min. Gain, Class AB

**90 W — 470–860 MHz
LINEAR
POWER AMPLIFIER**



CASE 389N-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Voltage Supply	V_{CC}	29	Vdc
Supply Current	I_{CC}	9	Adc
Source and Load VSWR (50 Ω REF.)	$VSWR_{S,L}$	1.20:1	—
Operating Temperature Range (Note 1)	T_C	−20 to +70	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, 50 Ω system, V_{CC} = 28 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth	BW	470	—	860	MHz
Power Gain (P_{out} = 90 W, CW)	G_p	7	—	—	dB
Efficiency	η	40	—	—	%
Power Output @ 1 dB Gain Compression	$P_{out(1\ dB)}$	90	—	—	W
Input Return Loss (P_{out} = 20 W)	IRL	15	—	—	dB
Load Mismatch (P_{ref} = 90 W, 3 tones, f = 860 MHz, Load VSWR = 3:1, All Phase Angles)	ψ	No degradation in power output			
Gain Ripple (P_{out} = 90 W, CW, BW = 470 to 860 MHz)	G_r	—	—	±1.5	dB

Note: 1. Case Temperature is measured at base plate — on RF transistor flange.

5

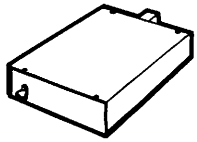
ATV6031

The RF Line
Linear Power Amplifier

**20 W — 470–860 MHz
LINEAR
POWER AMPLIFIER**

. . . a solid state Class A amplifier specifically designed for TV transposers and transmitters. This amplifier incorporates microstrip technology and discrete linear push-pull transistors with gold metallization and diffused emitter ballast resistors to enhance ruggedness and reliability.

- 470–860 MHz
- 20 W — P_{out}
- 26.5 V — V_{CC}
- 10.5 dB Min. Gain, Class A



CASE 389B-02, STYLE 1
(ATV)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Voltage Supply	V_{CC}	27	Vdc
Supply Current	I_{CC}	4	Adc
Source and Load VSWR (50 Ω REF.)	$VSWR_{S,L}$	1.2	
Operating Temperature Range (Note 1)	T_C	−20 to +70	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 50°C, 50 Ω system, V_{CC} = 26.5 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth	BW	470	—	860	MHz
Power Gain (P_{out} = 20 W, CW)	G_p	10.5	—	—	dB
Power Output @ 1 dB Gain Compression	$P_{out(1\ dB)}$	25	28	—	W
Supply Current (P_{out} = 20 W)	I_{CC}	—	—	3.6	A
Input Return Loss (P_{out} = 20 W)	IRL	15	—	—	dB
Load Mismatch (P_{out} = 20 W, CW, f = 860 MHz, Load VSWR = ∞:1, All Phase Angles)	ψ	No degradation in power output			
Gain Ripple (P_{out} = 20 W, CW, BW = 470 to 860 MHz)	G_r	—	±0.5	±1	dB
Intermodulation Distortion — 3 tones (f = 860 MHz, V_{CE} = 25.5 V, P_{ref} = 20 W, Vision Carrier = −8 dB, Sound Carrier = −7 dB, Sideband Signal = −16 dB, Specification TV05001)	IMD_1	—	—	−50	dB
Intermodulation Distortion (IDEM) (f = 860 MHz, V_{CE} = 25.5 V, P_{ref} = 20 W, Vision Carrier = −8 dB, Sound Carrier = −10 dB, Sideband Signal = −16 dB)	IMD_2	—	—	−53	dB

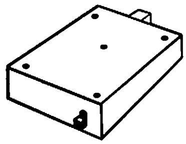
Note: 1. Case Temperature is measured at base plate — on RF transistor flange.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Advance Information
The RF Line
Linear Power Amplifier

ATV7050

30 W — 470–860 MHz
LINEAR
POWER AMPLIFIER



CASE 389B-02, STYLE 1
(ATV)

. . . a solid state Class A amplifier specifically designed for TV transposers and transmitters. This amplifier incorporates microstrip technology and discrete linear push-pull transistors with gold metallization and diffused emitter ballast resistors to enhance ruggedness and reliability.

- 470–860 MHz
- 30 W — P_{out}
- 25.5 V — V_{CC}
- 8 dB Min Gain, Class A

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Voltage Supply	V_{CC}	26.5	Vdc
Supply Current	I_{CC}	6.5	Adc
Operating Temperature Range (Note 1)	T_C	−20 to +60	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 50°C, 50 Ω system, V_{CC} = 25.5 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth	BW	470	—	860	MHz
Power Gain (P_{ref} = 30 W, 3 tones)	G_p	8	—	9.5	dB
Power Output @ 1 dB Gain Compression (Reference to P_{out} = 30 W)	$P_{out(1\ dB)}$	40	—	—	W
Input Return Loss (P_{out} = 30 W)	IRL	15	—	—	dB
Output Return Loss (P_{out} = 30 W)	ORL	15	—	—	dB
Load Mismatch (P_{ref} = 22 W, 3 tones, f = 860 MHz, Load VSWR = ∞:1, All Phase Angles)	ψ	No degradation in power output			
Gain Flatness (P_{ref} = 30 W, 3 tones, BW = 470 to 860 MHz)	G_r	—	±0.5	±0.7	dB
Intermodulation Distortion — 3 tones (f = 860 MHz, V_{CE} = 25.5 V, P_{ref} = 30 W, Vision Carrier = −8 dB, Sound Carrier = −7 dB, Sideband Signal = −16 dB, Specification TV05001)	IMD_1	—	−52	−51	dB
Intermodulation Distortion (IDEM) (f = 860 MHz, V_{CE} = 25.5 V, P_{ref} = 30 W, Vision Carrier = −8 dB, Sound Carrier = −10 dB, Sideband Signal = −16 dB)	IMD_2	—	−55	−54	dB

Notes: 1. Case Temperature is measured at base plate.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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TYPICAL CHARACTERISTICS

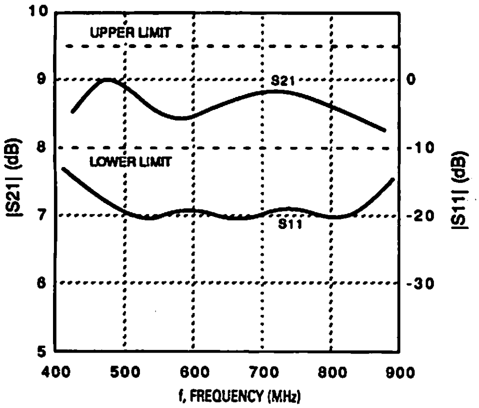


Figure 1. S Parameters versus Frequency

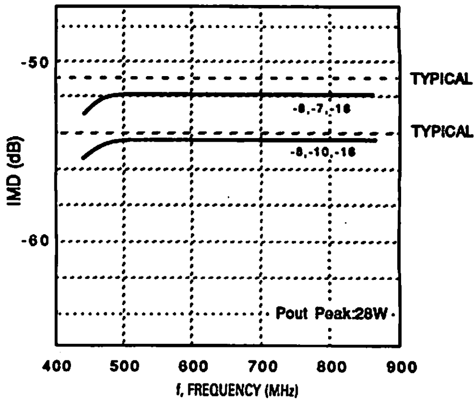


Figure 2. Intermodulation versus Frequency

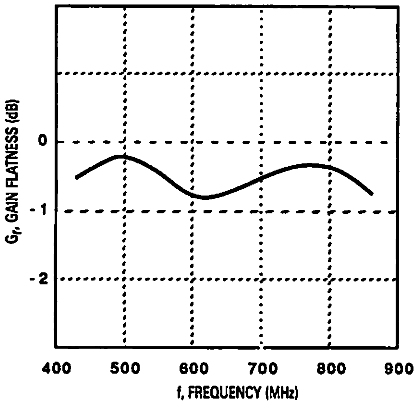
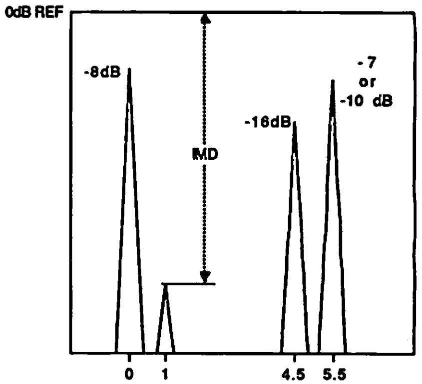


Figure 3. Compression Gain versus Frequency



3 TONES METHOD

IMD1 : Vision carrier -8 dB
Sound carrier -7 dB
Single band signal -16 dB

IMD2 : Vision carrier -8 dB
Sound carrier -10 dB
Single band signal -16 dB

0dB corresponds to Peak sync level

Figure 4. Peak Sync Level or Reference Level

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

ATV7060

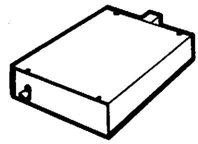
The RF Line

Linear Power Amplifier

40 W — 470–860 MHz
LINEAR
POWER AMPLIFIER

... a solid state Class A amplifier specifically designed for TV transposers and transmitters. This amplifier incorporates microstrip technology and discrete linear push-pull transistors with gold metallization and diffused emitter ballast resistors to enhance ruggedness and reliability.

- 470–860 MHz
- 40 W — P_{out}
- 26.5 V — V_{CC}
- 10 dB Min. Gain, Class A



CASE 389B-02, STYLE 1
(ATV)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector Voltage Supply	V_{CC}	26	Vdc
Supply Current	I_{CC}	9.4	Adc
Source and Load VSWR (50 Ω REF.)	$VSWR_{S,L}$	1.2	
Operating Temperature Range (Note 1)	T_C	−20 to +70	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 50°C, 50 Ω system, V_{CC} = 26.5 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Bandwidth	BW	470	—	860	MHz
Power Gain (P_{out} = 40 W)	G_p	10	—	—	dB
Power Output @ 1 dB Gain Compression	$P_{out(1\ dB)}$	55	—	—	W
Supply Current (P_{out} = 40 W)	I_{CC}	—	3.8	—	A
Input Return Loss (P_{out} = 40 W)	IRL	15	—	—	dB
Load Mismatch (P_{out} = 40 W, CW, f = 860 MHz, Load VSWR = ∞:1, All Phase Angles)	ψ	No degradation in power output			
Gain Flatness (P_{out} = 40 W, BW = 470 to 860 MHz)	G_F	—	—	1.0	dB
Intermodulation Distortion — 3 tones (f = 860 MHz, V_{CE} = 25.5 V, P_{ref} = 40 W, Vision Carrier = −8 dB, Sound Carrier = −7 dB, Sideband Signal = −16 dB, Specification TV05001)	IMD_1	—	—	−51	dB
Intermodulation Distortion (IDEM) (f = 860 MHz, V_{CE} = 25.5 V, P_{ref} = 40 W, Vision Carrier = −8 dB, Sound Carrier = −10 dB, Sideband Signal = −16 dB)	IMD_2	—	—	−54	dB

Note: 1. Case Temperature is measured at base plate — on RF transistor flange.

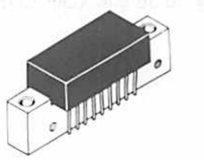
CA901

The RF Line
VHF/UHF CATV Amplifier

. . . designed for broadband applications requiring low-distortion amplification. Specifically intended for CATV/MATV market requirements. These amplifiers feature ion-implanted arsenic emitter transistors and an all gold metal system.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  Frequency Range — 40 to 860 MHz
  Power Gain — 17 dB Typ @ f = 40 MHz
  Noise Figure — 6.5 dB Typ @ f = 500 MHz
  120 dBμV DIN45004B
- All Gold Metallization for Improved Reliability
- Superior Gain, Return Loss and DC Current Stability with Temperature

17 dB
40–860 MHz
VHF/UHF
CATV/MATV
AMPLIFIER



CASE 714P-01, STYLE 2
(CA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+14	dBm
DC Supply Voltage	V_{CC}	26	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	860	MHz
Power Gain (f = 40 MHz)	P_G	16.5	17	17.5	dB
Slope (40–860 MHz)	S	0.2	0.8	1.4	dB
Gain Flatness	—	—	—	±0.3	dB
Return Loss — Input f = 40–100 MHz f = 100–800 MHz f = 800–860 MHz	IRL	20 15 10	— 17 12	— — —	dB
Return Loss — Output f = 40–100 MHz f = 100–860 MHz	ORL	20 15	— 18	— —	dB
Second Order Intermodulation Distortion (V_{out} = +50 dBmV per ch.)	IMD	—	—	−60	dB
DIN45004B (f = 40–860 MHz. See Figure 1) f = 40–400 MHz f = 400–860 MHz	DIN	121 120	— —	— —	dBμV
Noise Figure f = 500 MHz f = 860 MHz	NF	6.5 —	7.5 7.0	7.5 8.0	dB
DC Current	I_{DC}	—	235	255	mA

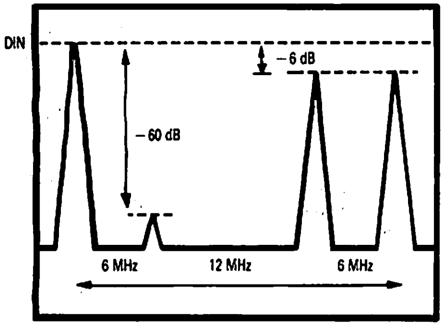


Figure 1. DIN45004B Test

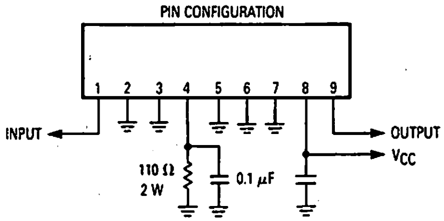
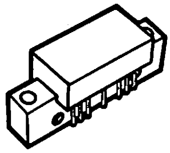


Figure 2. External Connections

CA2800

17 dB
10–400 MHz
800 mWATT
WIDEBAND
LINEAR AMPLIFIER



CASE 714F-01, STYLE 1
[CA (POS. SUPPLY)]
CA2800

The RF Line
Wideband Linear Amplifier

. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  Frequency Range — 10 to 400 MHz
  Output Power — 800 mW Typ @ 1 dB Compression, f = 200 MHz
  Power Gain — 17 dB Typ @ f = 50 MHz
  PEP — 400 mW Typ @ −32 dB IMD
  Noise Figure — 8.5 dB Typ @ f = 300 MHz
- All Gold Metallization for Improved Reliability

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+16	dBm
Operating Case Temperature Range	T_C	−20 to +90	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	400	MHz
Gain Flatness (f = 30–300 MHz) (f = 10–400 MHz)	—	— —	— —	±0.5 ±1	dB
Power Gain (f = 50 MHz)	P_G	16.25	17	17.75	dB
Noise Figure, Broadband (f = 60 MHz) (f = 300 MHz)	NF	— —	5 8.5	— —	dB
Power Output — 1 dB Compression (f = 200 MHz)	$P_{o1\,dB}$	800	—	—	mW
Third Order Intercept (See Figure 11, f_1 = 300 MHz)	ITO	—	44	—	dBm
Input/Output VSWR (f = 10–400 MHz)	VSWR	—	2:1	—	—
Second Harmonic Distortion (Tone at 10 mW, f_{2H} = 10–300 MHz)	d_{so}	—	−66	—	dB
Reverse Isolation (f = 10–400 MHz)	—	—	25	—	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 11) (f = 10–300 MHz @ −32 dB IMD)	PEP	—	400	—	mW
Supply Current	I_{CC}	—	—	220	mA

TYPICAL CHARACTERISTICS

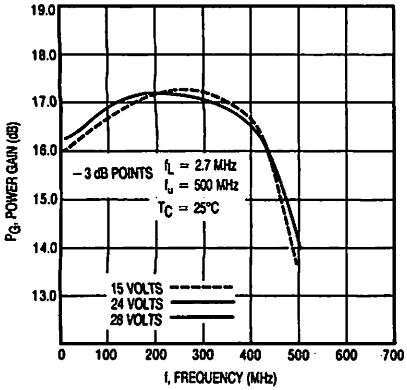


Figure 1. Power Gain versus Frequency

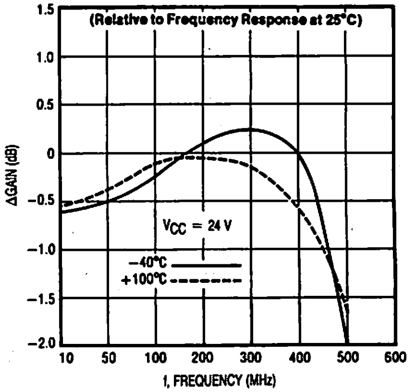


Figure 2. Relative Power Gain versus Temperature

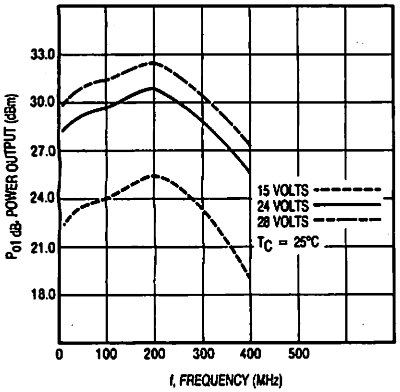


Figure 3. 1 dB Gain Compression versus Voltage

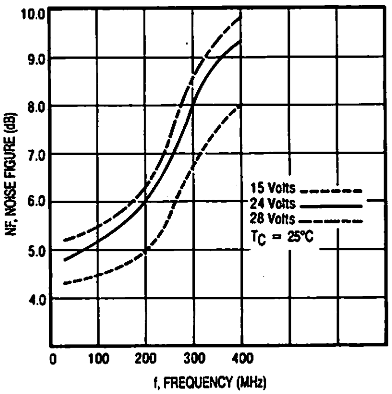


Figure 4. Noise Figure versus Voltage

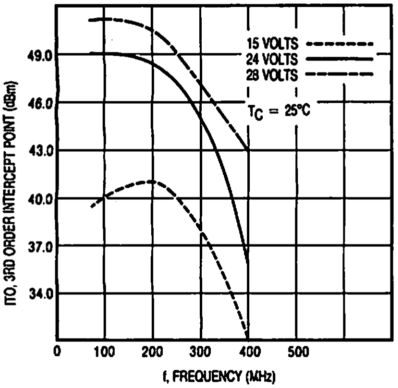


Figure 5. Third Order Intercept versus Voltage

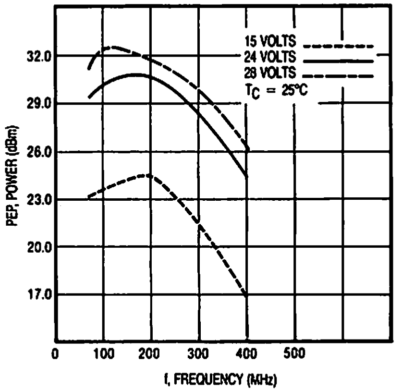


Figure 6. Peak Envelope Power versus Voltage

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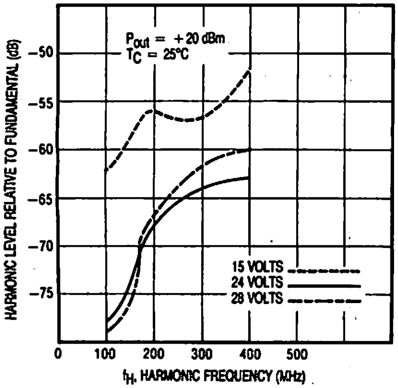


Figure 7. Second Harmonic Distortion versus Voltage

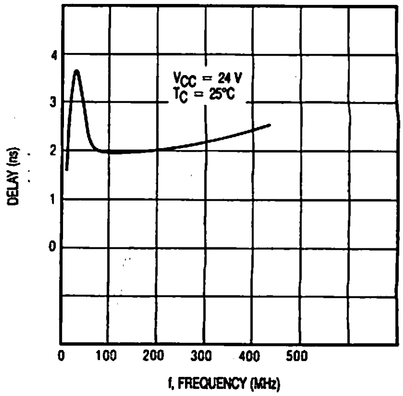


Figure 8. Group Delay versus Frequency

Biased at 24 Volts

T = 25°C Zo = 50Ω

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
10	-8.3	19.3	16.3	14.5	-24.2	-165	-9.7	36.5
100	-12.2	-21.0	16.8	-64.5	-23.8	135	-13.1	-29.3
200	-22.1	28.8	17.2	-136	-23.6	83	-22.0	30.0
300	-12.4	39.4	17.0	145	-24.6	27	-12.1	41.7
400	-11.0	17.6	16.2	63.1	-27.0	-34	-8.3	7.5

Magnitude in dB, Phase Angle in degrees.

Figure 9. S-Parameters

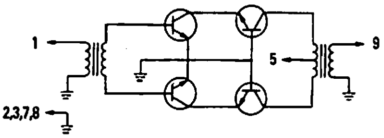
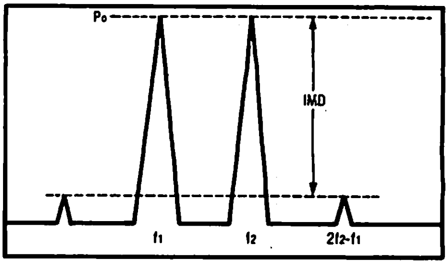


Figure 10. Functional Schematic



$I_{TO} = P_o + \frac{IMD}{2}$ @ IMD > 60dB

PEP = 4X Po @ IMD = −32dB

Figure 11. Intermodulation Test

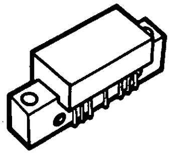
CA2810C
CA2810CH

The RF Line
Wideband Linear Amplifiers

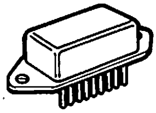
**33 dB
10–350 MHz
800 mWATT
WIDEBAND
LINEAR AMPLIFIERS**

... designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
- Frequency Range — 10 to 350 MHz
  Output Power — 800 mW Typ @ 1 dB Compression, f = 200 MHz
  Power Gain — 33 dB @ f = 50 MHz
  PEP — 400 mW Typ @ −32 dB IMD
  Noise Figure — 8 dB Max @ f = 300 MHz
- All Gold Metallization for Improved Reliability



CASE 714F-01, STYLE 1
(CA (POS. SUPPLY))
CA2810C



CASE 826-01, STYLE 1
(SIP)
CA2810CH

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+5	dBm
Operating Case Temperature Range	T_C	−20 to +90	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	350	MHz
Gain Flatness (f = 30–300 MHz) (f = 10–350 MHz)	—	— —	— —	±1 ±1.5	dB
Power Gain (f = 50 MHz)	P_G	32	33	34	dB
Noise Figure, Broadband (f = 60 MHz) (f = 300 MHz)	NF	— —	4.5 —	— 8	dB
Power Output — 1 dB Compression (f = 200 MHz)	$P_{o1\ dB}$	800	—	—	mW
Third Order Intercept (See Figure 11, f_1 = 300 MHz)	ITO	—	43	—	dBm
Input/Output VSWR (f = 10–350 MHz)	VSWR	—	2:1	—	—
Second Harmonic Distortion (Tone at 10 mW, f_{2H} = 10–300 MHz)	d_{so}	—	−66	—	dB
Reverse Isolation (f = 10–350 MHz)	—	—	40	—	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 11) (f = 10–300 MHz @ −32 dB IMD)	PEP	—	400	—	mW
Supply Current	I_{CC}	—	—	330	mA

TYPICAL CHARACTERISTICS

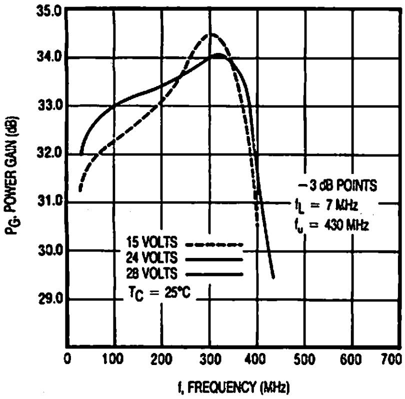


Figure 1. Power Gain versus Frequency

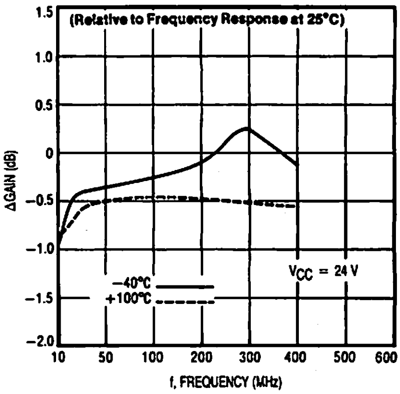


Figure 2. Relative Power Gain versus Temperature

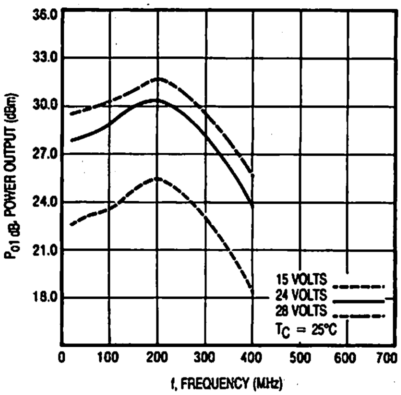


Figure 3. 1 dB Gain Compression versus Voltage

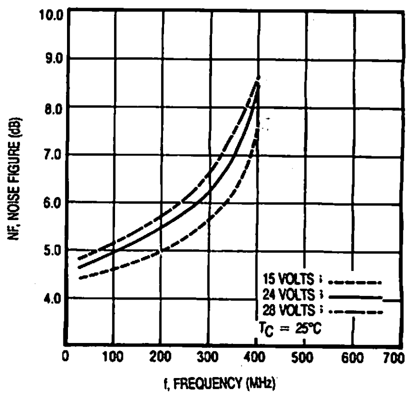


Figure 4. Noise Figure versus Voltage

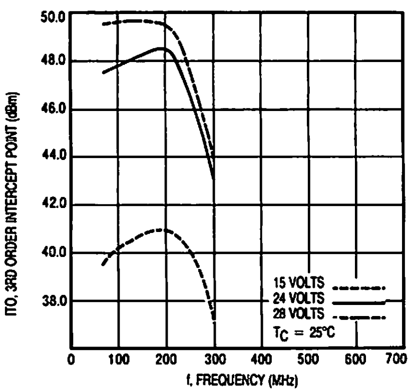


Figure 5. Third Order Intercept versus Voltage

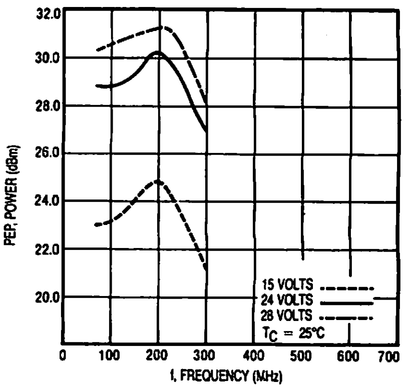


Figure 6. Peak Envelope Power versus Voltage

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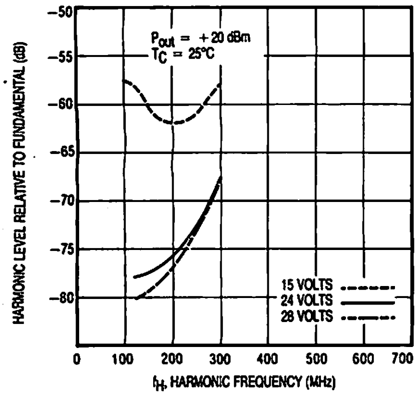


Figure 7. Second Harmonic Distortion versus Voltage

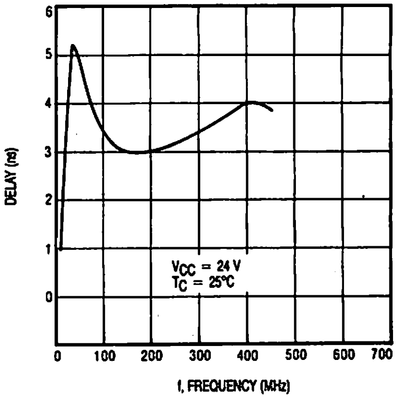


Figure 8. Group Delay versus Frequency

Biased at 24 Volts T = 25°C Zo = 50Ω

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
30	-13.7	-1.5	31.9	-10.5	-49.0	2.7	-14.2	10.5
50	-14.0	3.6	32.4	-39.9	-48.6	-16.6	-13.9	19.0
100	-13.3	5.8	32.9	-100	-48.4	-53.7	-11.8	11.3
200	-18.7	-3.7	33.4	147	-48.2	-123	-14.1	-1.7
300	-15.2	39.4	34.0	20.9	-47.7	154	-13.2	65.3

Magnitude in dB, Phase Angle in degrees.

Figure 9. S-Parameters

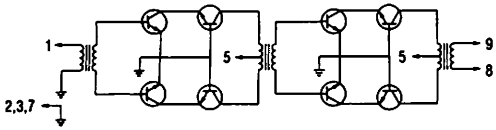
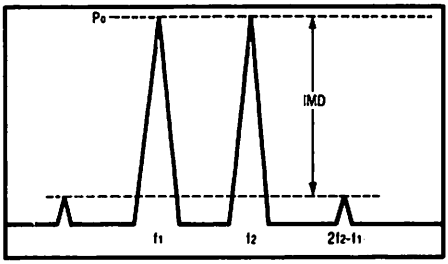


Figure 10. Functional Schematic



$I_{TO} = P_o + \frac{IMD}{2}$ @ IMD > 60dB

PEP = 4X Po @ IMD = -32dB

Figure 11. Intermodulation Test

CA2813C
CA2813CH

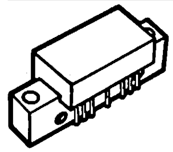
34 dB
40–300 MHz
160 mWATT
WIDEBAND
LINEAR AMPLIFIERS

The RF Line

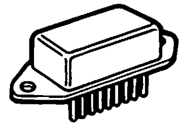
Wideband Linear Amplifiers

. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = 15 V, T_C = 25°C:
  Frequency Range — 40 to 300 MHz
  Output Power — 160 mW Typ @ 1 dB Compression, f = 300 MHz
  Power Gain — 34 dB Typ @ f = 50 MHz
  PEP — 150 mW Typ @ −32 dB IMD
  Noise Figure — 5 dB Typ @ f = 300 MHz
- All Gold Metallization for Improved Reliability
- Designed for 15 V Operation, Low Power Consumption
- Low VSWR for 75 Ohm System



CASE 714F-01, STYLE 1
[CA (POS. SUPPLY)]
CA2813C



CASE 826-01, STYLE 1
(SIP)
CA2813CH

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+5	dBm
Operating Case Temperature Range	T_C	−20 to +90	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 15 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	300	MHz
Gain Flatness (f = 40–300 MHz)	—	—	±0.75	±1.25	dB
Power Gain (f = 50 MHz)	P_G	33	34	35	dB
Noise Figure, Broadband (f = 50 MHz) (f = 300 MHz)	NF	— —	3.5 5	4.5 6	dB
Power Output — 1 dB Compression (f = 300 MHz)	$P_{o1\ dB}$	—	160	—	mW
Third Order Intercept (See Figure 11, f_1 = 300 MHz)	ITO	38	2.0:1	—	dBm
Input/Output VSWR (f = 40–300 MHz)	VSWR	—	1.2:1	—	—
Second Harmonic Distortion (Tone at 10 mW, f_{2H} = 300 MHz)	d_{so}	—	−50	—	dB
Reverse Isolation (f = 40–300 MHz)	—	—	40	—	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 11) (f = 40–300 MHz @ −32 dB IMD)	PEP	—	150	—	mW
Supply Current	I_{CC}	150	170	190	mA

TYPICAL CHARACTERISTICS

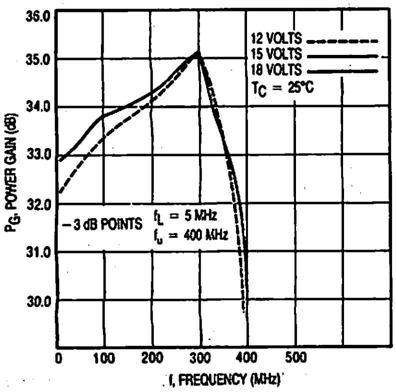


Figure 1. Power Gain versus Frequency

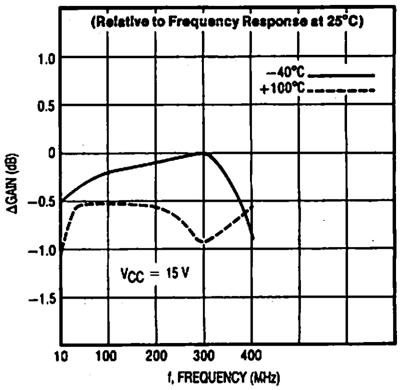


Figure 2. Relative Power Gain versus Temperature

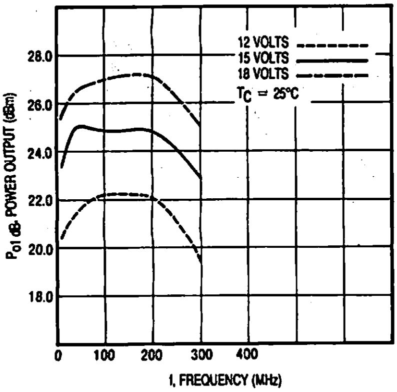


Figure 3. 1 dB Gain Compression versus Voltage

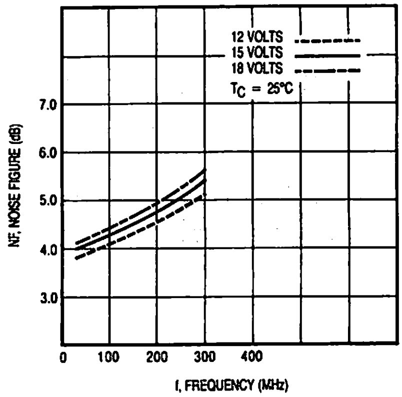


Figure 4. Noise Figure versus Voltage

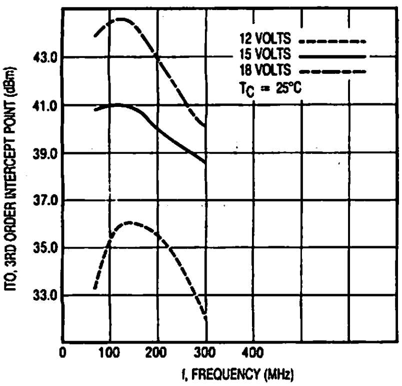


Figure 5. Third Order Intercept versus Voltage

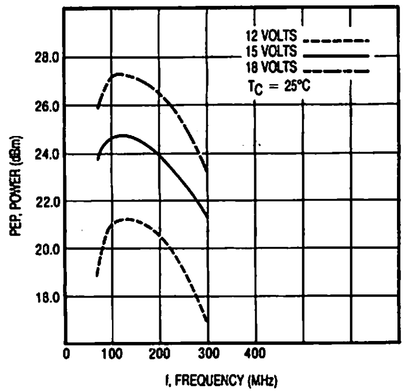


Figure 6. Peak Envelope Power versus Voltage

5

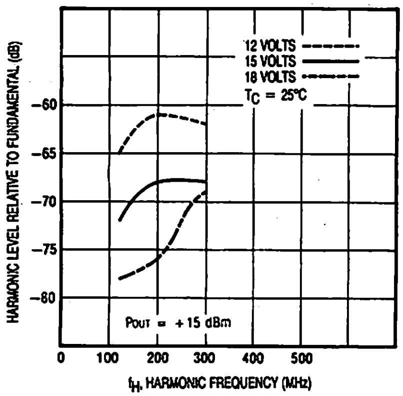


Figure 7. Second Harmonic Distortion versus Voltage

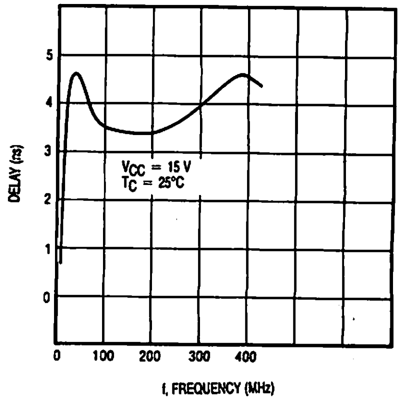


Figure 8. Group Delay versus Frequency

Biased at 15 Volts

T = 25°C Zo = 75Ω

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
10	-16.6	53.0	33.1	35.0	-48.1	39.1	-21.2	48.7
50	-32.3	-2.0	33.6	-44.9	-47.8	-21.0	-30.9	65.0
100	-41.4	119	34.2	-107	-47.7	-58.0	-30.3	22.6
200	-27.8	62.0	34.5	130	-48.6	-140	-38.5	-105
300	-26.1	-177	35.3	-10.2	-47.1	126	-23.3	84.5

Magnitude in dB, Phase Angle in degrees.

Figure 9. S-Parameters

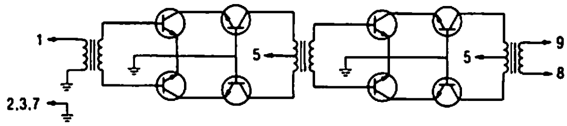
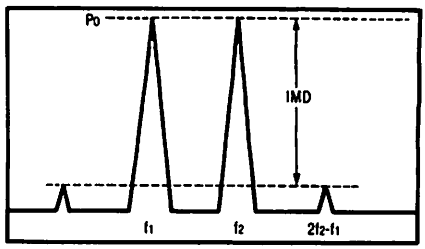


Figure 10. Functional Schematic



$I_{TO} = P_o + \frac{IMD}{2}$ @ IMD > 60dB

PEP = 4X P_o @ IMD = -32dB

Figure 11. Intermodulation Test

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

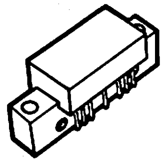
CA2818
CA2818H

The RF Line
Wideband Linear Amplifiers

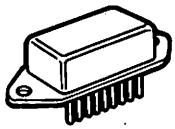
18.5 dB
1–200 MHz
900 mWATT
WIDEBAND
LINEAR AMPLIFIERS

... designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  Frequency Range — 1 to 200 MHz
  Output Power — 800 mW Typ @ 1 dB Compression, f = 200 MHz
  Power Gain — 18.5 dB Typ @ f = 50 MHz
  PEP — 800 mW Typ @ −32 dB IMD
  Noise Figure — 5.5 dB Typ @ f = 150 MHz
  ITO — 47 dBm Typ @ f = 150 MHz
- All Gold Metallization for Improved Reliability
- Refer to CATV Equivalent Model CA2418 for 75 Ohm Performance Data



CASE 714F-01, STYLE 1
(CA)
CA2818



CASE 826-01, STYLE 1
(SIP)
CA2818H

5

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+14	dBm
Operating Case Temperature Range	T_C	−40 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Gain Flatness f = 50–150 MHz f = 1–200 MHz	—	— —	±0.2 ±0.5	±0.5 ±1	dB
Frequency Range	BW	1	—	200	MHz
Power Gain (f = 50 MHz)	P_G	17.75	18.5	19.25	dB
Noise Figure, Broadband f = 30 MHz f = 150 MHz	NF	— —	4.5 5.5	6 7	dB
Power Output — 1 dB Compression (f = 150 MHz)	$P_{o\ 1dB}$	800	900	—	mW
Third Order Intercept (See Figure 11, f_1 = 150 MHz)	ITO	44	47	—	dBm
Input/Output VSWR (f = 1–200 MHz)	VSWR	—	1.7:1	2:1	—
Second Harmonic Distortion (Tone at 100 mW, f_{2H} = 1–200 MHz)	d_{so}	—	−60	−55	dB
Reverse Isolation (f = 1–200 MHz)	—	—	25	—	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 11) (f = 1–200 MHz @ −32 dB IMD)	PEP	600	800	—	mW
Supply Current	I_{CC}	190	205	220	mA

TYPICAL CHARACTERISTICS

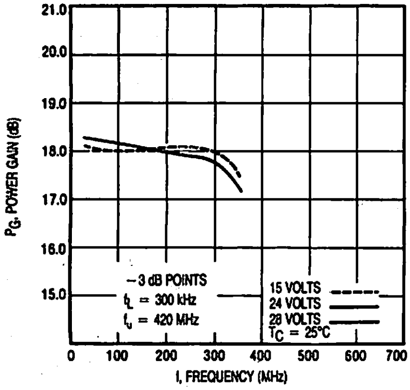


Figure 1. Power Gain versus Frequency

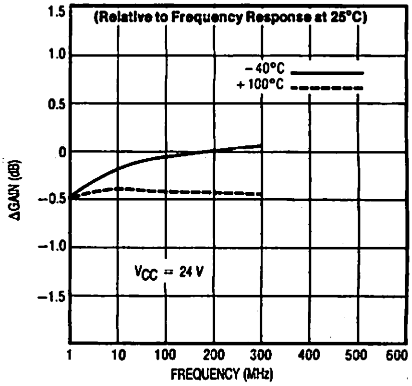


Figure 2. Relative Power Gain versus Temperature

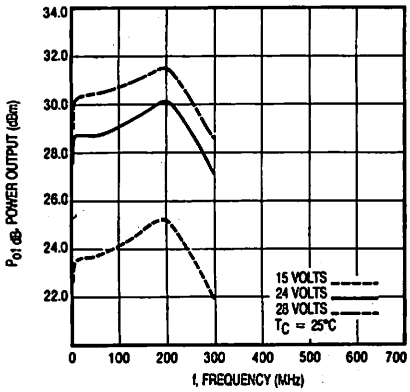


Figure 3. 1 dB Gain Compression versus Voltage

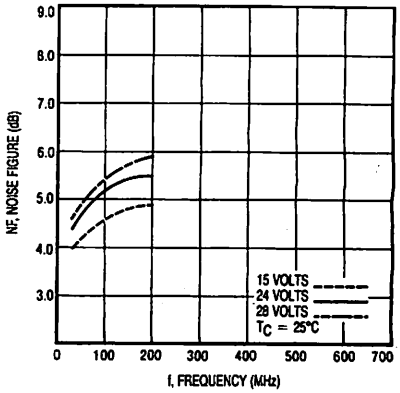


Figure 4. Noise Figure versus Voltage

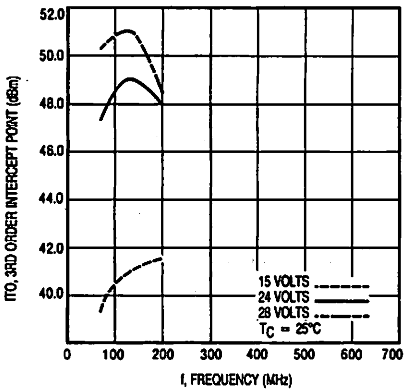


Figure 5. Third Order Intercept versus Voltage

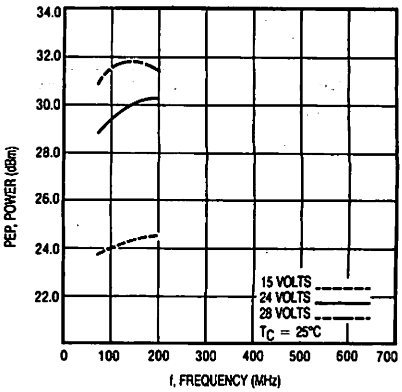


Figure 6. Peak Envelope Power versus Voltage

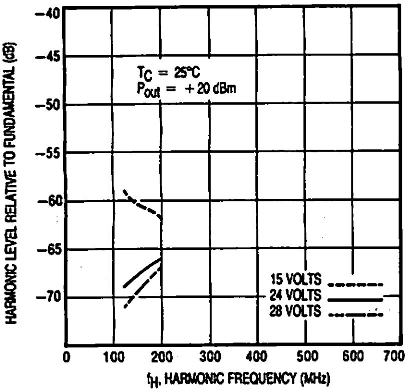


Figure 7. Second Harmonic Distortion versus Voltage

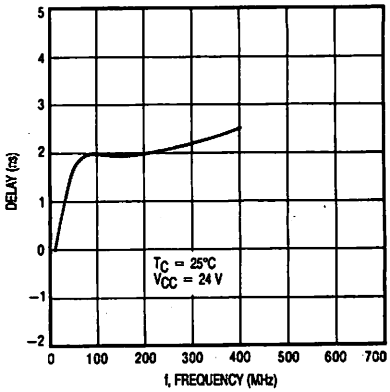


Figure 8. Group Delay versus Frequency

Biased at 24 Volts T = 25°C Zo = 50Ω

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
1	-11.6	23.5	17.8	9.7	-25.4	-167	-10.9	8.4
10	-11.1	0	18.2	-4.6	-24.9	-183	-11.0	0.4
50	-12.5	-14.2	18.2	-37.1	-25.0	154	-12.7	-9.6
100	-14.8	-18.0	18.2	-74.3	-24.9	128	-15.3	-24.0
200	-13.6	21.5	18.1	-147	-24.9	76.4	-22.7	43.0

Magnitude in dB, Phase Angle in degrees.

Figure 9. S-Parameters

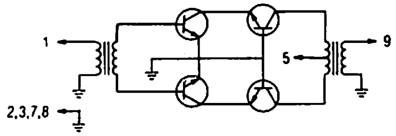
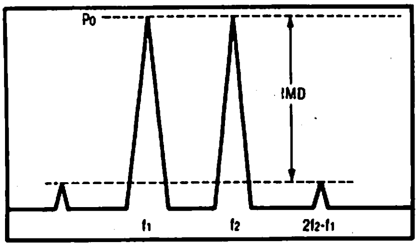


Figure 10. Functional Schematic



$I_{TO} = P_o + \frac{IMD}{2}$ @ IMD > 60dB

PEP = 4X P_o @ IMD = -32dB

Figure 11. Intermodulation Test

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

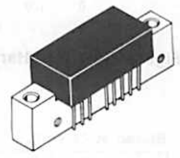
CA2820
CA2820H

The RF Line
Wideband Linear Amplifiers

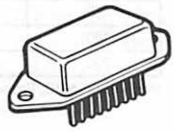
. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  Frequency Range — 1 to 520 MHz
  Output Power — 440 mW Typ @ 1 dB Compression, f = 1–520 MHz
  Power Gain — 30 dB Typ @ f = 100 MHz
  Noise Figure — 8.3 dB Typ @ f = 50 MHz
- All Gold Metallization for Improved Reliability
- Unconditional Stability Under All Mismatch Conditions

30 dB
1–520 MHz
440 mWATT
WIDEBAND
LINEAR AMPLIFIERS



CASE 714M-01, STYLE 2
(CA)
CA2820



CASE 826-01, STYLE 4
(SIP)
CA2820H

5

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+10	dBm
Operating Case Temperature Range	T_C	−40 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1	—	520	MHz
Gain Flatness (f = 1–520 MHz)	—	—	±0.8	±1.5	dB
Power Gain (f = 100 MHz)	P_G	29	30	31	dB
Noise Figure, Broadband f = 30 MHz f = 500 MHz	NF	— —	6 8.3	8 10	dB
Power Output — 1 dB Compression (f = 1–520 MHz)	$P_{o\ 1dB}$	400	440	—	mW
Third Order Intercept (See Figure 10, f_1 = 520 MHz)	ITO	35	37	—	dBm
Input/Output VSWR Input Output	VSWR	— —	1.5:1 1.8:1	2:1 2:1	—
Second Harmonic Distortion (Tone at 10 mW, f_{2H} = 1–520 MHz)	d_{so}	—	−55	−45	dB
Reverse Isolation (f = 1–520 MHz)	—	49	52	—	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 10) (f = 1–520 MHz @ −32 dB IMD)	PEP	300	400	—	mW
Supply Current	I_{CC}	300	330	360	mA

TYPICAL CHARACTERISTICS

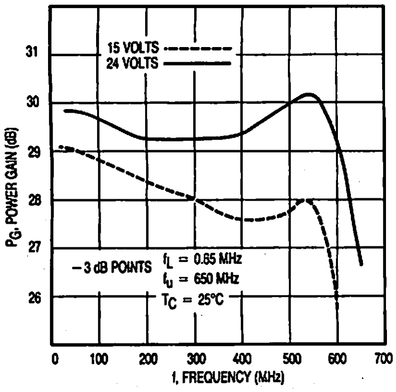


Figure 1. Power Gain versus Frequency

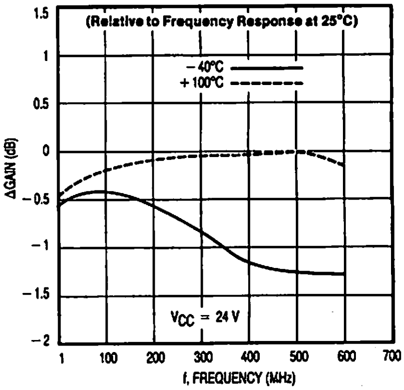


Figure 2. Relative Power Gain versus Temperature

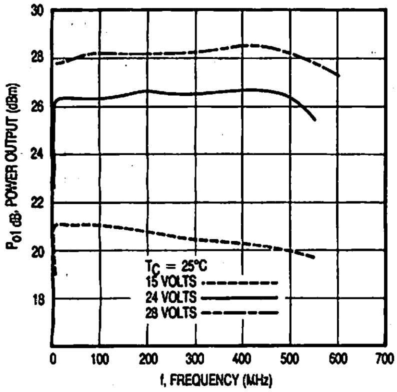


Figure 3. 1 dB Gain Compression versus Voltage

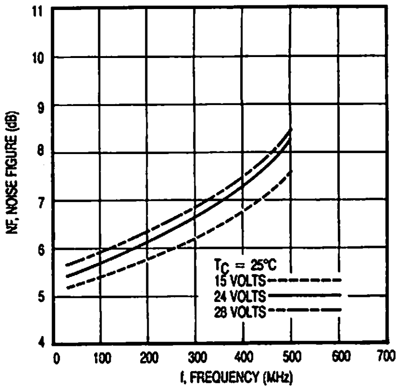


Figure 4. Noise Figure versus Voltage

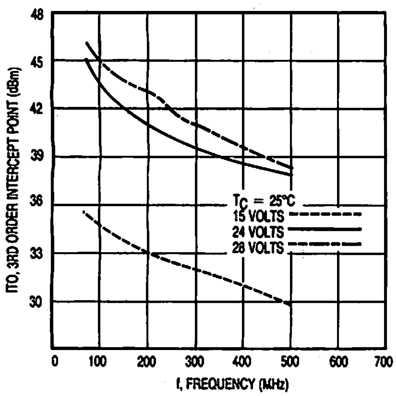


Figure 5. Third Order Intercept versus Voltage

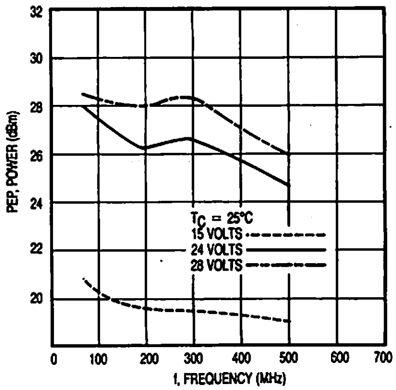


Figure 6. Peak Envelope Power versus Voltage

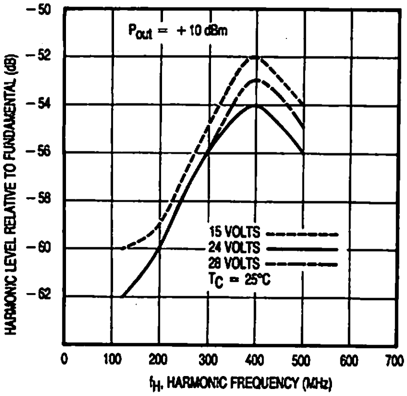


Figure 7. Second Harmonic Distortion versus Voltage

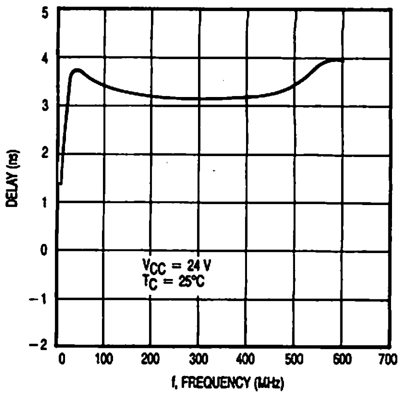


Figure 8. Group Delay versus Frequency

Biased at 24 Volts

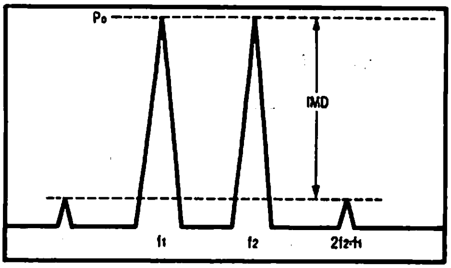
T = 25°C Zo = 50Ω

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
1	-12.5	-41.4	30.1	169	-52.8	150	-6.3	138
10	-25.4	-24.0	29.6	5.0	-53.8	5.0	-24.1	78
100	-27.5	5.6	29.6	-120	-55.3	-51.0	-39.3	-126
200	-21.4	3.6	29.3	120	-59.0	-118	-21.3	15.7
300	-17.1	-43	29.1	-1.6	-58.2	145	-16.0	-30
400	-15.5	-106	29.1	-123	-53.2	89.8	-10.4	-56.6
500	-16.5	-181	29.5	109	-50.3	36.0	-37.7	150
600	-17.3	129	28.7	-41.2	-55.4	14.8	-2.5	-14.2

Magnitude in dB, Phase Angle in degrees.

Figure 9. S-Parameters

5



$I_{TO} = P_o + \frac{IMD}{2}$ @ IMD > 60dB

PEP = 4X P_o @ IMD = -32dB

Figure 10. Intermodulation Test

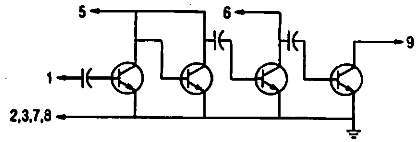


Figure 11. Functional Schematic

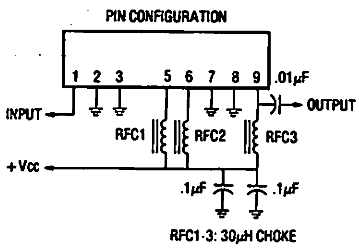


Figure 12. External Connections

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

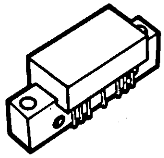
CA2830
CA2830H
CA2833

The RF Line
Wideband Linear Amplifiers

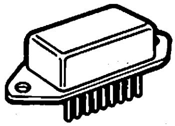
. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  - Frequency Range — 5 to 200 MHz
  - Output Power — 800 mW Typ @ 1 dB Compression, f = 200 MHz
  - Power Gain — 34.5 dB Typ @ f = 100 MHz
  - PEP — 800 mW Typ @ −32 dB IMD
  - Noise Figure — 4.7 dB Typ @ f = 200 MHz
  - ITO — 46 dBm @ f = 200 MHz
- All Gold Metallization for Improved Reliability
- Unconditional Stability Under All Load Conditions

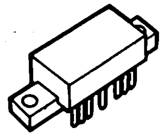
34.5 dB
5–200 MHz
800 mWATT
WIDEBAND
LINEAR AMPLIFIERS



CASE 714F-01, STYLE 1
(CA)
CA2830



CASE 826-01, STYLE 1
(SIP)
CA2830H



CASE 714G-01, STYLE 1
[CA, LOW PROFILE]
CA2833

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+5	dBm
Operating Case Temperature Range	T_C	−40 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	5	—	200	MHz
Gain Flatness (f = 5–200 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	33.5	34.5	35.5	dB
Noise Figure, Broadband (f = 200 MHz)	NF	—	4.7	5.5	dB
Power Output — 1 dB Compression (f = 5–200 MHz)	$P_{o\ 1dB}$	630	800	—	mW
Power Output — 1 dB Compression (f = 5–200 MHz, V_{CC} = 28 V)	$P_{o\ 1dB}$	1000	1260	—	mW
Third Order Intercept (See Figure 11, f_1 = 200 MHz)	ITO	44	46	—	dBm
Input/Output VSWR (f = 5–200 MHz)	VSWR	—	1.5:1	2:1	—
Second Harmonic Distortion (Tone at 100 mW, f_{2H} = 150 MHz)	d_{so}	—	−60	−50	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 11) (f = 5–200 MHz @ −32 dB IMD)	PEP	600	800	—	mW
Supply Current	I_{CC}	270	300	330	mA

5

TYPICAL CHARACTERISTICS

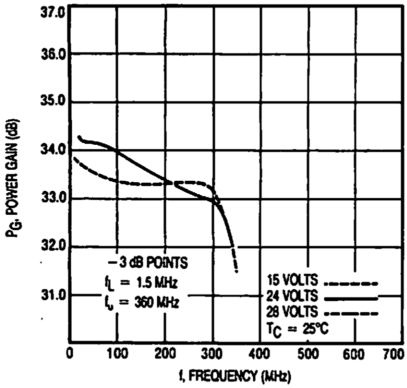


Figure 1. Power Gain versus Frequency

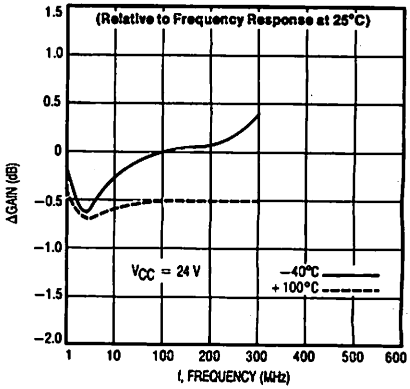


Figure 2. Relative Power Gain versus Temperature

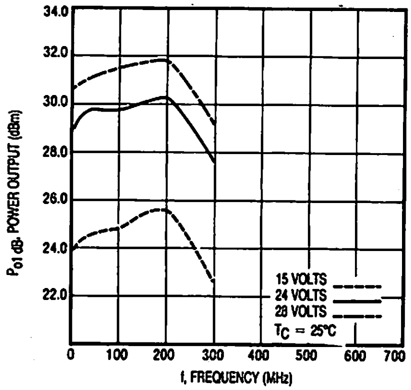


Figure 3. 1 dB Gain Compression versus Voltage

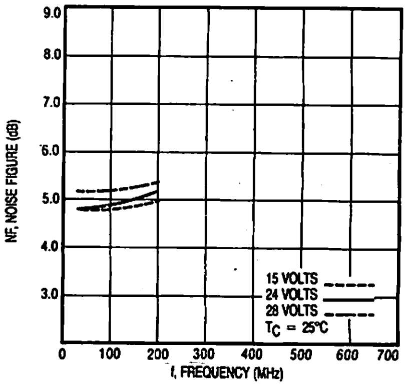


Figure 4. Noise Figure versus Voltage

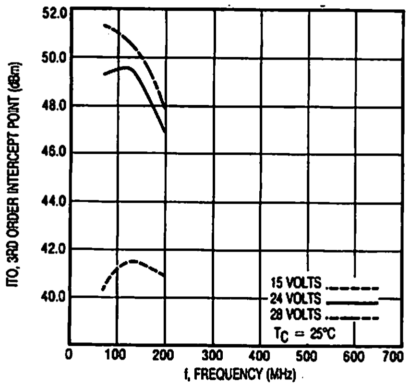


Figure 5. Third Order Intercept versus Voltage

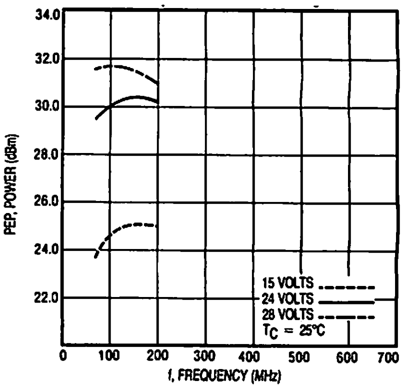


Figure 6. Peak Envelope Power versus Voltage

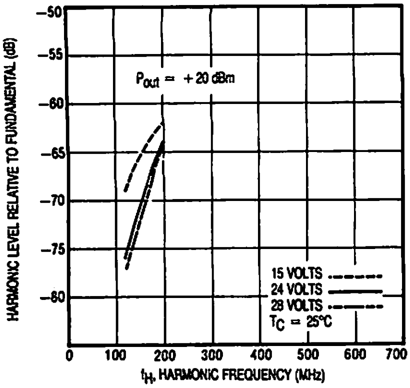


Figure 7. Second Harmonic Distortion versus Voltage

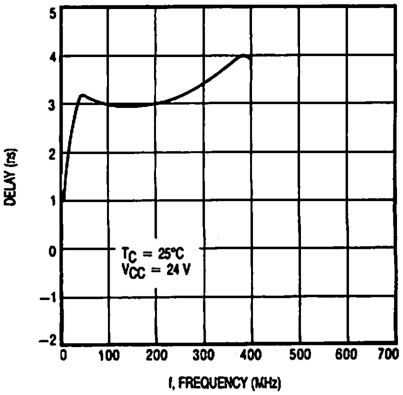


Figure 8. Group Delay versus Frequency

Biased at 24 Volts **T = 25°C Zo = 50Ω**

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
5	-18.3	66.2	34.6	15.2	-47.0	17.7	-9.8	87.4
10	-19.3	45.5	34.6	-0.6	-47.0	2.3	-14.5	76.8
50	-15.6	35.0	34.2	-56.7	-47.5	-30.3	-12.6	45.0
100	-13.2	34.4	33.9	-114	-47.9	-62.9	-10.8	10.7
200	-11.1	30.1	33.5	134	-48.3	-128	-14.9	-42.6

Magnitude in dB, Phase Angle in degrees.

Figure 9. S-Parameters

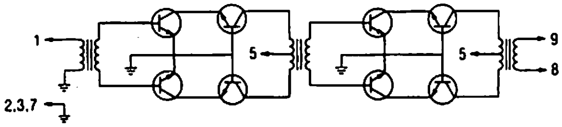
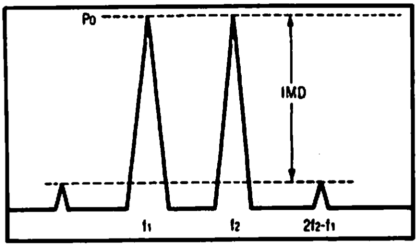


Figure 10. Functional Schematic



$ITO = P_o + \frac{IMD}{2}$ @ IMD > 60dB

PEP = 4X P_o @ IMD = -32dB

Figure 11. Intermodulation Test

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

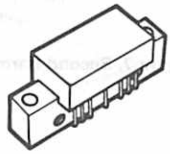
CA2832
CA2832H

35.5 dB
1–200 MHz
1.6 WATT
WIDEBAND
LINEAR AMPLIFIERS

The RF Line
Wideband Linear Amplifiers

. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = 28 V, T_C = 25°C:
  - Frequency Range — 1 to 200 MHz
  - Output Power — 1580 mW Typ @ 1 dB Compression, f = 200 MHz
  - Power Gain — 35.5 dB Typ @ f = 100 MHz
  - PEP — 900 mW Typ @ −32 dB IMD
  - Noise Figure — 6 dB Typ @ f = 200 MHz
  - ITO — 47 dBm @ f = 200 MHz
- All Gold Metallization for Improved Reliability
- Output Power — 2 W @ V_{CC} = 28 V
- Unconditional Stability Under All Load Conditions



CASE 714F-01, STYLE 1
(CA)
CA2832

CASE 826-01, STYLE 1
(SIP)
CA2832H

5

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	30	Vdc
RF Power Input	P_{in}	+5	dBm
Operating Case Temperature Range	T_C	−40 to +90	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 28 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1	—	200	MHz
Gain Flatness (f = 1–200 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	34	35.5	37	dB
Noise Figure, Broadband (f = 200 MHz)	NF	—	6	7	dB
Power Output — 1 dB Compression (f = 1–200 MHz)	$P_{o\ 1dB}$	1260	1580	—	mW
Power Output — 1 dB Compression (f = 150 MHz)	$P_{o\ 1dB}$	—	2000	—	mW
Third Order Intercept (See Figure 11, f_1 = 200 MHz)	ITO	45	47	—	dBm
Input/Output VSWR (f = 1–200 MHz)	VSWR	—	1.5:1	2:1	—
Second Harmonic Distortion (Tone at 100 mW, f_{2H} = 150 MHz)	d_{so}	—	−70	−60	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 11) (f = 1–200 MHz @ −32 dB IMD)	PEP	—	900	—	mW
Supply Current	I_{CC}	400	435	470	mA

TYPICAL CHARACTERISTICS

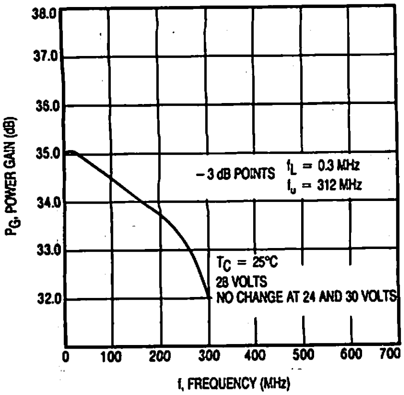


Figure 1. Power Gain versus Frequency

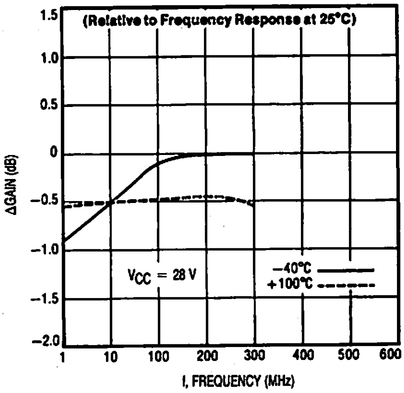


Figure 2. Relative Power Gain versus Temperature

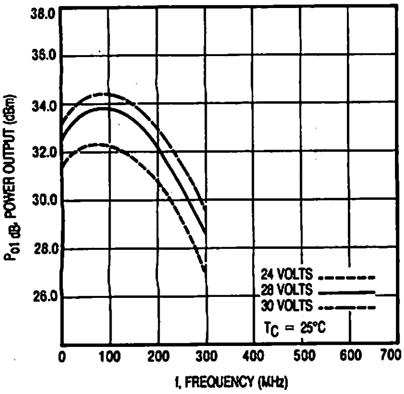


Figure 3. 1 dB Gain Compression versus Voltage

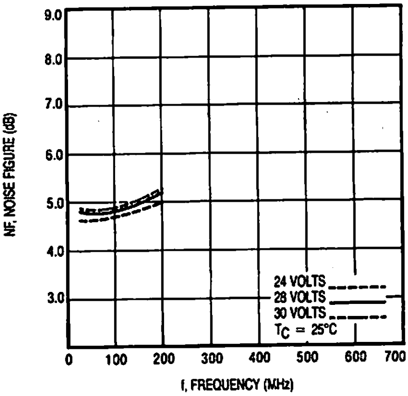


Figure 4. Noise Figure versus Voltage

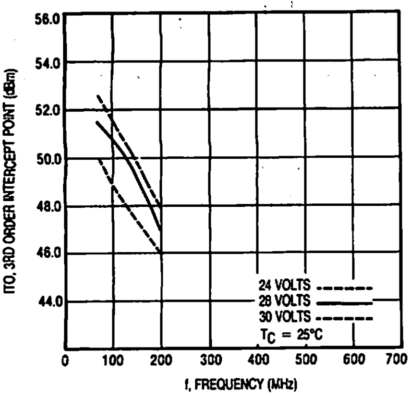


Figure 5. Third Order Intercept versus Voltage

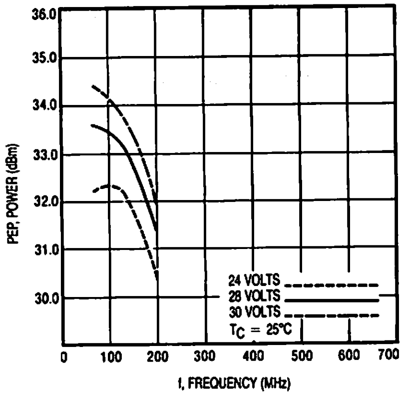


Figure 6. Peak Envelope Power versus Voltage

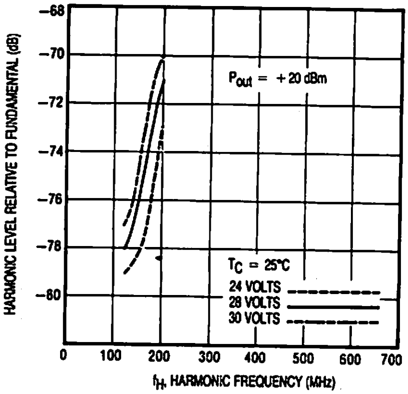


Figure 7. Second Harmonic Distortion versus Voltage

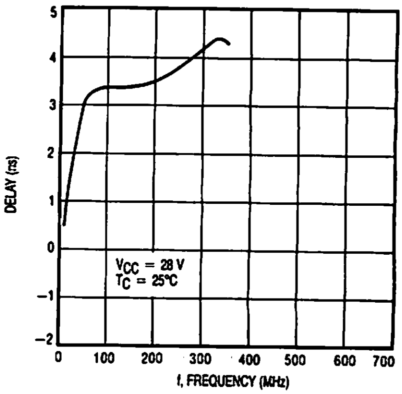


Figure 8. Group Delay versus Frequency

Biased at 28 Volts T = 25°C Zo = 50Ω

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
1	-17.6	79.3	35.2	23.5	-48.0	28.1	-12.6	60.5
10	-19.7	31.2	35.7	-9.1	-47.3	-4.9	-16.4	25.0
50	-16.0	30.6	35.5	-63.6	-48.0	-37.7	-11.8	9.8
100	-13.3	37.4	35.0	-126	-48.7	-75.0	-10.7	-34.2
200	-10.0	27.6	34.3	110	-50.5	-154	-9.8	-136

Magnitude in dB, Phase Angle in degrees.

Figure 9. S-Parameters

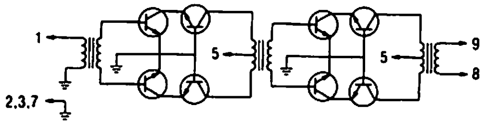
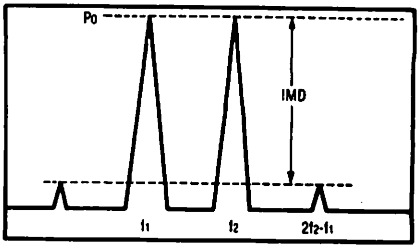


Figure 10. Functional Schematic



$I_{TO} = P_o + \frac{IMD}{2}$ @ IMD > 60dB

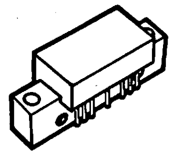
PEP = 4X P_o @ IMD = -32dB

Figure 11. Intermodulation Test

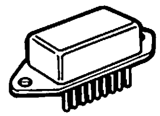
5

CA2842
CA2842H

22 dB
30–300 MHz
1.2 WATTS
WIDEBAND
LINEAR AMPLIFIERS



CASE 714F-01, STYLE 1
[CA (POS. SUPPLY)]
CA2842



CASE 826-01, STYLE 1
(SIP)
CA2842H

The RF Line
Wideband Linear Amplifiers

. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  Frequency Range — 30 to 300 MHz
  Output Power — 1580 mW Typ @ 1 dB Compression, f = 200 MHz, V_{CC} = 28 V
  Power Gain — 22 dB Typ @ f = 100 MHz
  PEP — 650 mW Typ @ −32 dB IMD
  Noise Figure — 5 dB Typ @ f = 100 MHz
  ITO — 46 dBm @ f = 300 MHz
- All Gold Metallization for Improved Reliability
- Unconditional Stability Under All Load Conditions

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+14	dBm
Operating Case Temperature Range	T_C	−40 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	30	—	300	MHz
Gain Flatness (f = 30–300 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	21	22	23	dB
Noise Figure, Broadband (f = 100 MHz)	NF	—	5	6	dB
Power Output — 1 dB Compression (f = 30–200 MHz, V_{CC} = 28 V)	$P_{o1\ dB}$	1260	1580	—	mW
Power Output — 1 dB Compression (f = 200–300 MHz, V_{CC} = 28 V)	$P_{o1\ dB}$	630	800	—	mW
Third Order Intercept (See Figure 10, f_1 = 30–300 MHz)	ITO	43	46	—	dBm
Input/Output VSWR (f = 30–200 MHz) (f = 200–300 MHz)	VSWR	— —	— —	1.3:1 1.5:1	—
Second Harmonic Distortion (Tone at 100 mW, f_{2H} = 300 MHz)	d_{so}	—	—	−50	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 10) (f = 200 MHz @ −32 dB IMD)	PEP	550	650	—	mW
Supply Current	I_{CC}	210	230	250	mA

TYPICAL CHARACTERISTICS

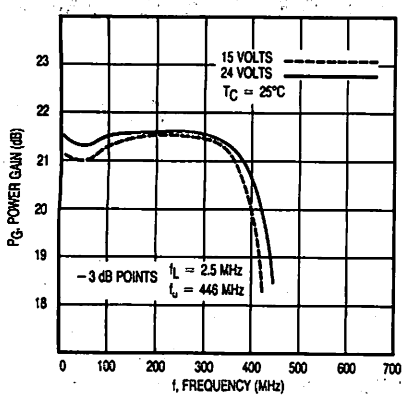


Figure 1. Power Gain versus Frequency

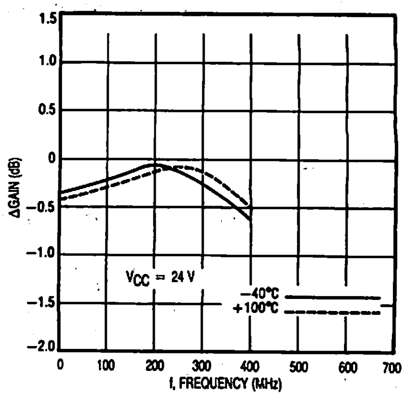


Figure 2. Relative Power Gain versus Temperature

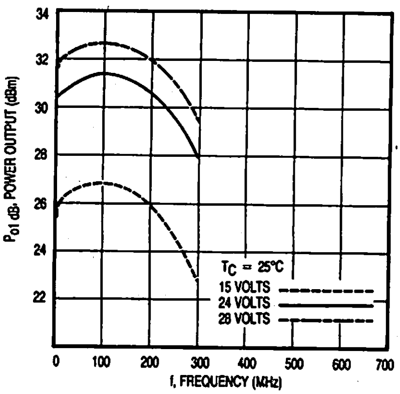


Figure 3. 1 dB Gain Compression versus Voltage

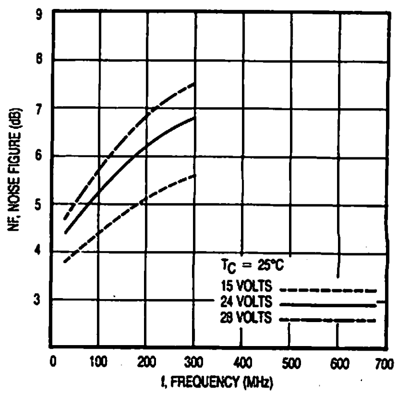


Figure 4. Noise Figure versus Voltage

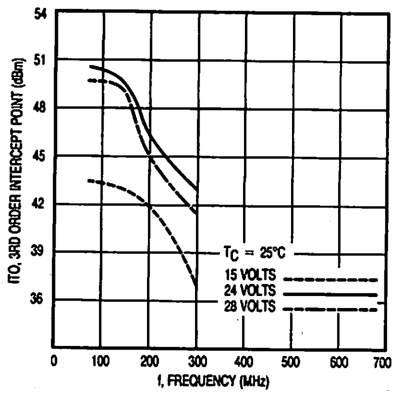


Figure 5. Third Order Intercept versus Voltage

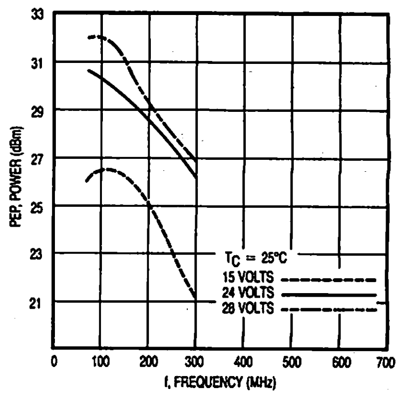


Figure 6. Peak Envelope Power versus Voltage

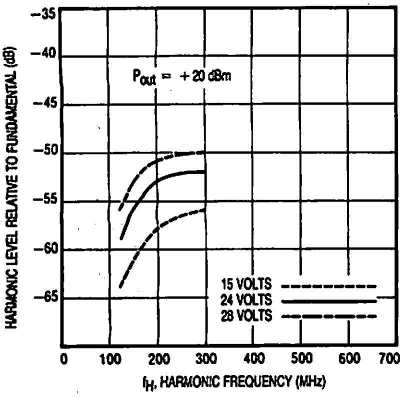


Figure 7. Second Harmonic Distortion versus Voltage

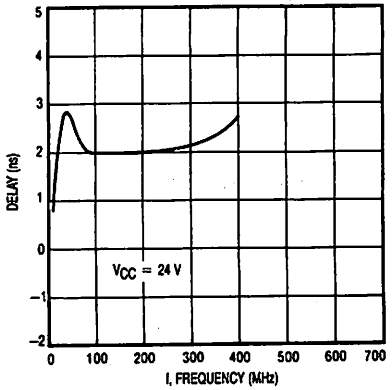


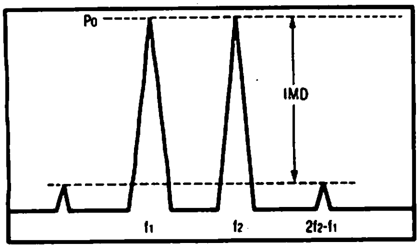
Figure 8. Group Delay versus Frequency

Biased at 24 Volts — T = 25°C Zo = 50Ω

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
10	-15.9	34.4	21.0	10.9	-26.3	-168	-18.9	39.0
50	-25.4	-11.8	21.2	-33.1	-26.5	157	-24.2	13.4
100	-32.8	7.6	21.4	-72.7	-26.5	128	-34.7	-63.0
200	-19.7	97.7	21.4	-148	-27.0	73.4	-19.4	85.0
300	-21.8	100	21.4	128	-28.7	12.5	-18.4	100

Magnitude in dB, Phase Angle in degrees.

Figure 9. S-Parameters



$$I_{TO} = P_o + \frac{IMD}{2} \text{ @ IMD} > 60\text{dB}$$

PEP = 4X Po @ IMD = -32dB

Figure 10. Intermodulation Test

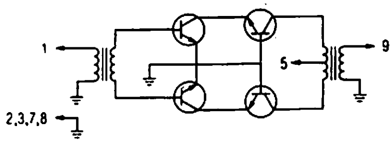


Figure 11. Functional Schematic

CA2850R
CA2851R

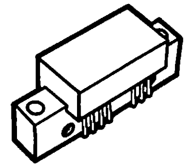
The RF Line

Wideband Linear Amplifiers

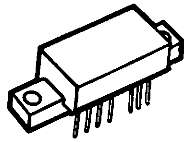
...designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = −19 V, T_C = 25°C:
  Frequency Range — 40 to 100 MHz
  Output Power — 320 mW Typ @ 1 dB Compression, f = 100 MHz
  Power Gain — 17.5 dB Typ @ f = 100 MHz
  PEP — 300 mW Typ @ −32 dB IMD
  Noise Figure — 4.5 dB Typ @ f = 70 MHz
- All Gold Metallization for Improved Reliability
- Low Power Consumption — I_{CC} = 125 mA Typ @ V_{CC} = −19 V

**17.5 dB
40–100 MHz
320 mWATT
WIDEBAND
LINEAR AMPLIFIERS**



CASE 714H-01, STYLE 1
(CA)
CA2850R



CASE 714L-01, STYLE 1
(CA, LOW PROFILE)
CA2851R

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	−28	Vdc
RF Power Input	P_{in}	+14	dBm
Operating Case Temperature Range	T_C	−40 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = −19 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	100	MHz
Gain Flatness (f = 40–100 MHz)	—	—	±0.1	±0.2	dB
Power Gain (f = 100 MHz)	P_G	17	17.5	18	dB
Noise Figure, Broadband (f = 70 MHz)	NF	—	4.5	5	dB
Power Output — 1 dB Compression (f = 40–100 MHz)	$P_{o\ 1dB}$	250	320	—	mW
Third Order Intercept (See Figure 10, f_1 = 70 MHz)	ITO	37	40	—	dBm
Input/Output VSWR (f = 40–100 MHz)	VSWR	—	1.2:1	1.3:1	—
Second Harmonic Distortion (Tone at 250 mW, f_{2H} = 100 MHz)	d_{so}	—	−40	—	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 10) (f = 40–100 MHz @ −32 dB IMD)	PEP	250	300	—	mW
Supply Current	I_{CC}	110	125	140	mA

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TYPICAL CHARACTERISTICS

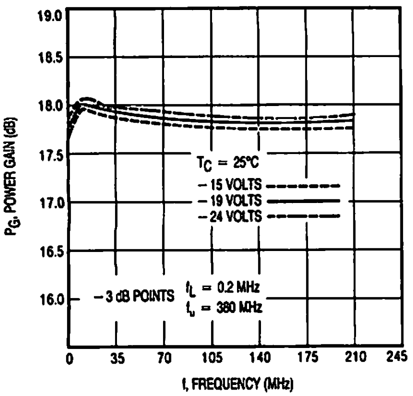

Figure 1. Power Gain versus Frequency

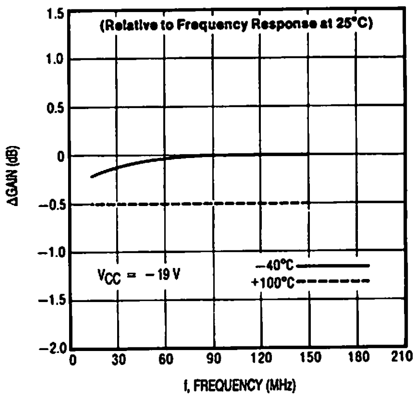

Figure 2. Relative Power Gain versus Temperature

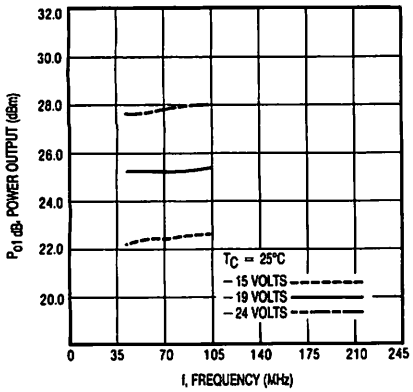

Figure 3. 1 dB Gain Compression versus Voltage

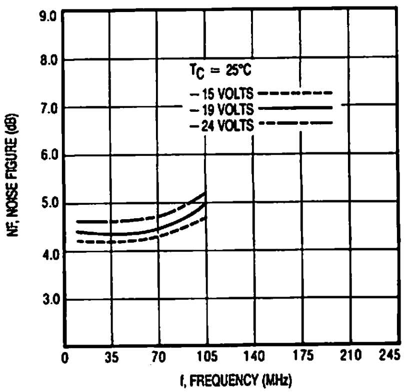

Figure 4. Noise Figure versus Voltage

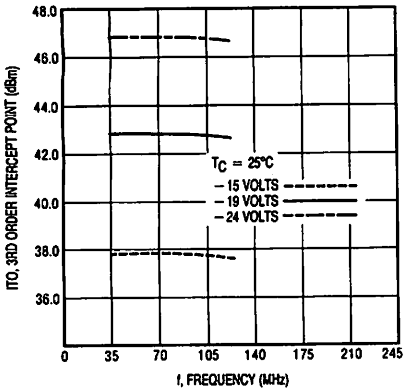

Figure 5. Third Order Intercept versus Voltage

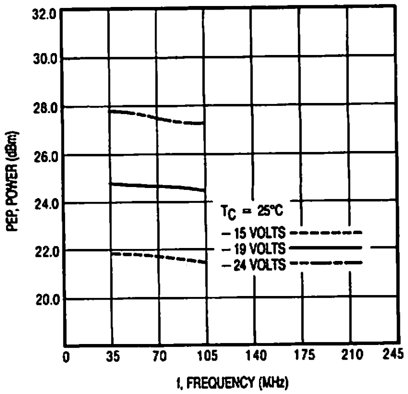

Figure 6. Peak Envelope Power versus Voltage

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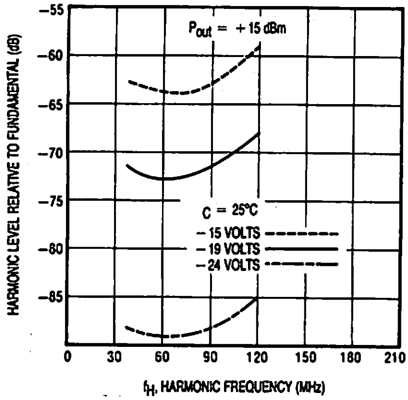


Figure 7. Second Harmonic Distortion versus Voltage

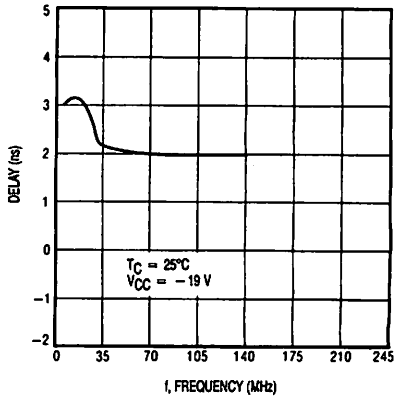


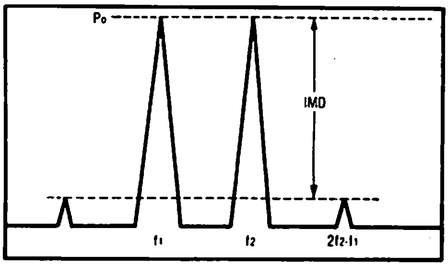
Figure 8. Group Delay versus Frequency

Biased at −19 Volts T = 25°C Zo = 50Ω

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
40	-33.7	-16.0	17.6	-28.2	-23.7	161	-23.6	4.2
50	-35.8	-8.8	17.6	-35.0	-23.8	158	-24.1	3.2
70	-38.9	+16.8	17.6	-49.1	-23.8	149	-25.5	-7.5
90	-38.0	53.2	17.6	-63.3	-23.8	141	-27.0	-24.8
100	-36.9	63.5	17.6	-70.2	-23.9	136	-27.4	-31.5

Magnitude in dB, Phase Angle in degrees.

Figure 9. S-Parameters



$$I_{TO} = P_o + \frac{IMD}{2} \text{ @ IMD} > 60\text{dB}$$

$$PEP = 4X\ P_o \text{ @ IMD} = -32\text{dB}$$

Figure 10. Intermodulation Test

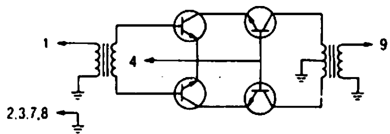


Figure 11. Functional Schematic

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

CA2870
CA2870H

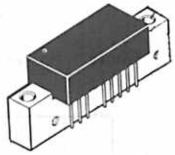
The RF Line
Wideband Linear Amplifiers

34 dB
20–400 MHz
500 mWATT
WIDEBAND
LINEAR AMPLIFIERS

... designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

Two B+ inputs, one for the preamplifier and one for the final stage, provide a convenient means of RF leveling by variation of the final stage B+ voltage. Although the uncorrected flatness of this module is superb (±0.5 dB typical), the leveling provisions provide convenient means of correcting for the frequency response of succeeding stages and injection of AM modulation.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  - Frequency Range — 20 to 400 MHz
  - Output Power — 500 mW Typ @ 1 dB Compression, f = 400 MHz
  - Power Gain — 34 dB Typ @ f = 100 MHz
  - PEP — 500 mW Typ @ −32 dB IMD
  - Noise Figure — 7.5 dB Typ @ f = 400 MHz
- All Gold Metallization for Improved Reliability
- Amplitude Leveling Provision



CASE 714M-01, STYLE 1
(CA)
CA2870

CASE 826-01, STYLE 3
(SIP)
CA2870H

5

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+5	dBm
Operating Case Temperature Range	T_C	−40 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	20	—	400	MHz
Gain Flatness (f = 20–400 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	32.5	34	35.5	dB
Noise Figure, Broadband f = 30 MHz f = 400 MHz	NF	— —	4.5 7.5	6 8.5	dB
Power Output — 1 dB Compression f = 225 MHz f = 400 MHz	$P_{o1\ dB}$	800 400	850 500	— —	mW
Third Order Intercept (See Figure 11, f_1 = 300 MHz)	ITO	42	45	—	dBm
Input/Output VSWR (f = 20–400 MHz) Input Output	VSWR	— —	1.5:1 1.8:1	2:1 2:1	—
Second Harmonic Distortion (Tone at 100 mW, f_{2H} = 20–400 MHz)	d_{so}	—	−52	−45	dB
Reverse Isolation (f = 20–400 MHz)	—	45	48	—	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 11) (f = 20–400 MHz @ −32 dB IMD)	PEP	400	500	—	mW
Supply Current	I_{CC}	270	300	330	mA

TYPICAL CHARACTERISTICS

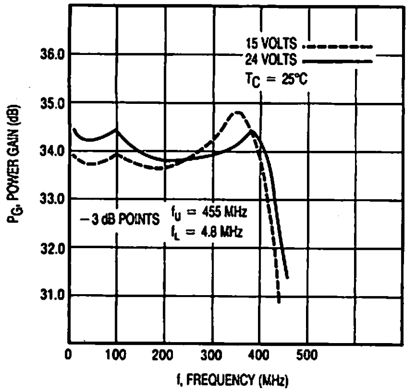


Figure 1. Power Gain versus Frequency

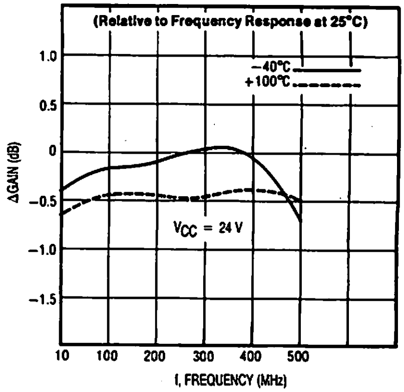


Figure 2. Relative Power Gain versus Temperature

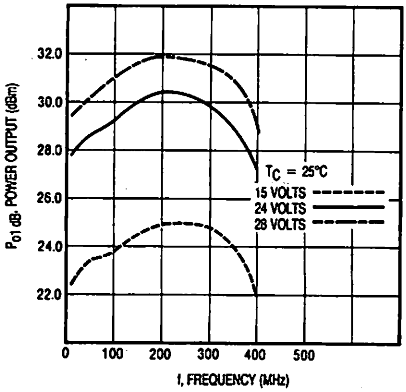


Figure 3. 1 dB Gain Compression versus Voltage

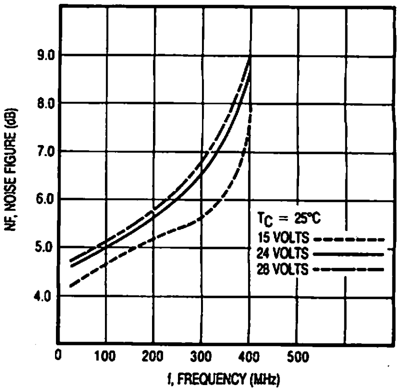


Figure 4. Noise Figure versus Voltage

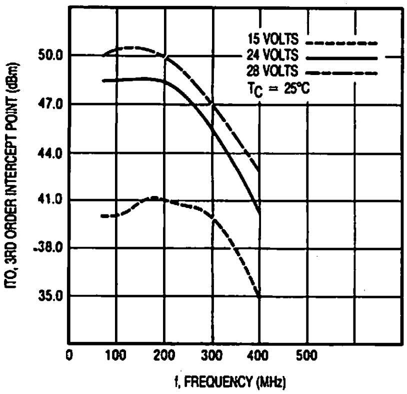


Figure 5. Third Order Intercept versus Voltage

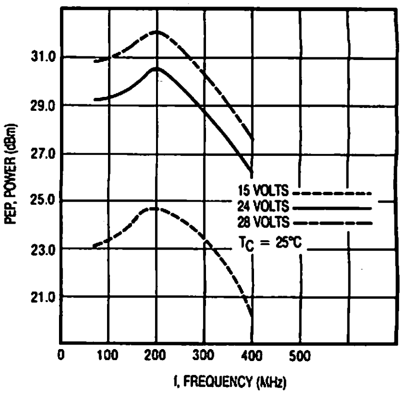


Figure 6. Peak Envelope Power versus Voltage

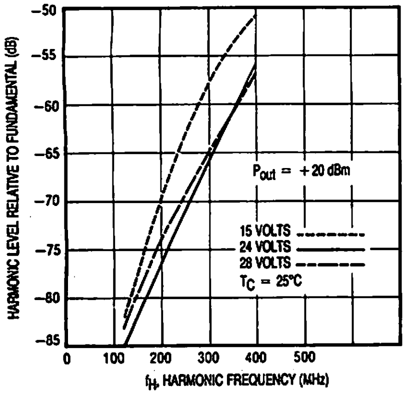


Figure 7. Second Harmonic Distortion versus Voltage

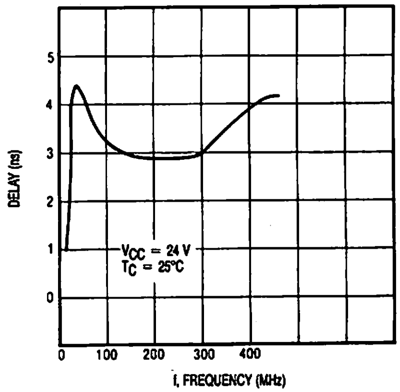


Figure 8. Group Delay versus Frequency

Biased at 24 Volts T = 25°C Zo = 50Ω

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
20	-29.0	99.8	34.0	-4.3	-47.9	6.0	-14.6	21.3
100	-18.0	76.2	34.3	-107	-47.6	-53.5	-12.3	-5.9
200	-16.1	61.8	33.8	143	-47.9	-115	-11.6	-35.3
300	-13.9	52.3	33.7	27.9	-47.9	172	-13.5	-89.0
400	-20.9	44.6	33.9	-110	-47.2	94.8	-18.5	95.2

Magnitude in dB, Phase Angle in degrees.

Figure 9. S-Parameters

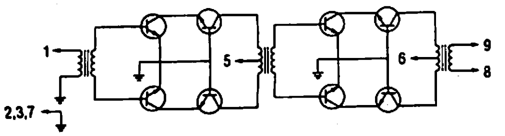
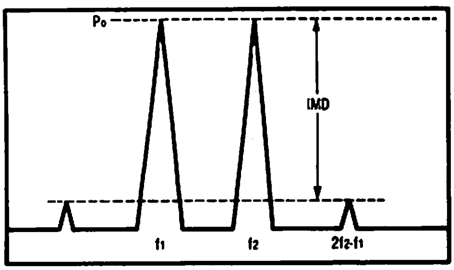


Figure 10. Functional Schematic



$I_{TO} = P_o + \frac{IMD}{2}$ @ IMD > 60dB

PEP = 4X Po @ IMD = -32dB

Figure 11. Intermodulation Test

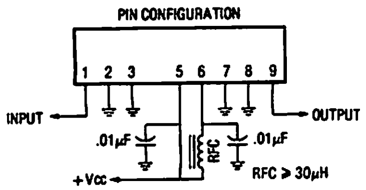


Figure 12. External Connections

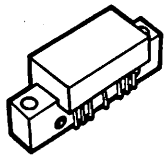
CA2875R

The RF Line
Wideband Linear Amplifier

17.5 dB
40–100 MHz
400 mWATT
WIDEBAND
LINEAR AMPLIFIER

. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = −19 V, T_C = 25°C:
  Frequency Range — 40 to 100 MHz
  Output Power — 400 mW Typ @ 1 dB Compression, f = 100 MHz
  Power Gain — 17.5 dB Typ @ f = 100 MHz
  PEP — 300 mW Typ @ −32 dB IMD
  Noise Figure — 4.5 dB Typ @ f = 70 MHz
  ITO — 43 dBm @ f = 70 MHz
- All Gold Metallization for Improved Reliability
- Specified for 75 Ohm Systems



CASE 714H-01, STYLE 1
(CA)
CA2875R

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	−28	Vdc
RF Power Input	P_{in}	+14	dBm
Operating Case Temperature Range	T_C	−40 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = −19 V, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	100	MHz
Gain Flatness (f = 40–100 MHz)	—	—	±0.1	±0.2	dB
Power Gain (f = 100 MHz)	P_G	17	17.5	18	dB
Noise Figure, Broadband (f = 70 MHz)	NF	—	4.5	5	dB
Power Output — 1 dB Compression (f = 40–100 MHz)	$P_{o\ 1dB}$	315	400	—	mW
Third Order Intercept (See Figure 11, f_1 = 70 MHz)	ITO	42	43	—	dBm
Input/Output VSWR (f = 40–100 MHz)	VSWR	—	—	1.1:1	—
Second Harmonic Distortion (Tone at 250 mW, f_{2H} = 100 MHz)	d_{so}	—	−40	—	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 11) (f = 40–100 MHz @ −32 dB IMD)	PEP	250	300	—	mW
Supply Current	I_{CC}	140	155	170	mA

TYPICAL CHARACTERISTICS

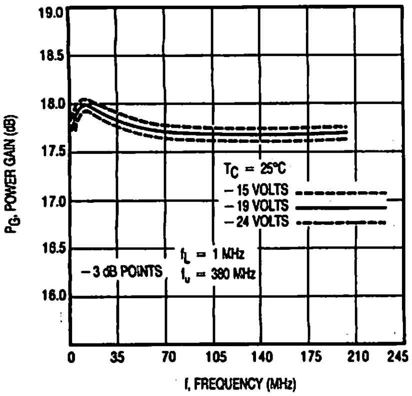


Figure 1. Power Gain versus Frequency

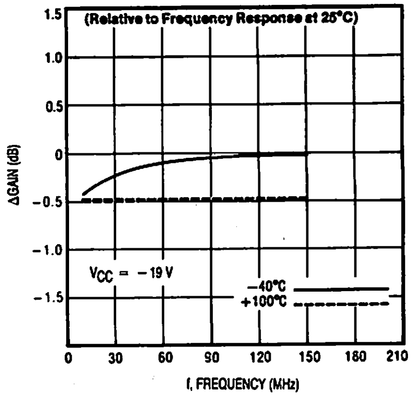


Figure 2. Relative Power Gain versus Temperature

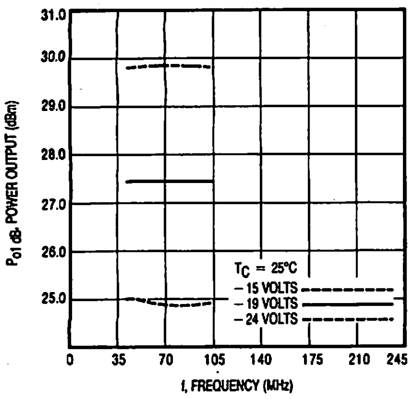


Figure 3. 1 dB Gain Compression versus Voltage

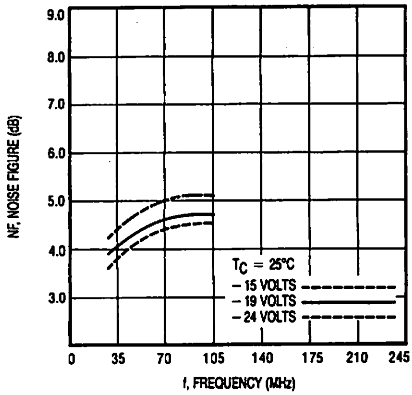


Figure 4. Noise Figure versus Voltage

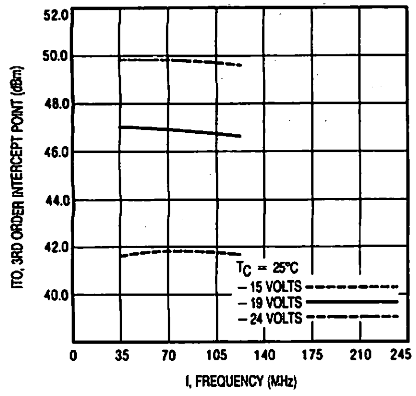


Figure 5. Third Order Intercept versus Voltage

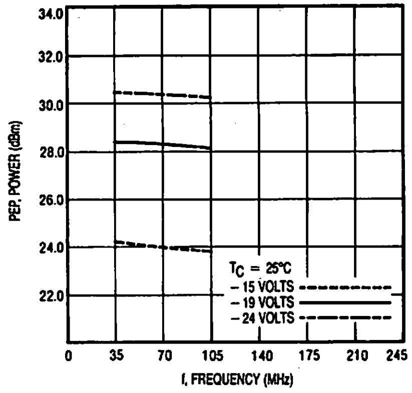


Figure 6. Peak Envelope Power versus Voltage

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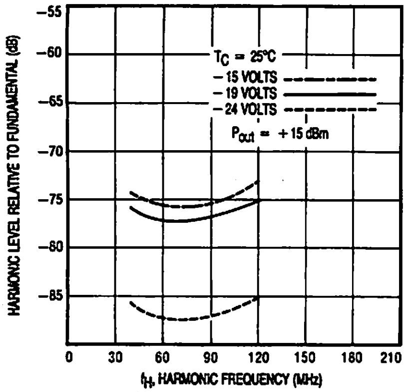


Figure 7. Second Harmonic Distortion versus Voltage

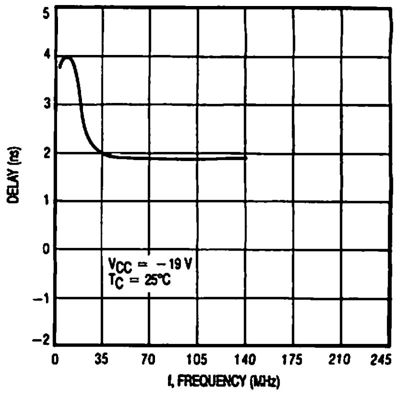


Figure 8. Group Delay versus Frequency

Biased at −19 Volts **T = 25°C Zo = 75Ω**

Frequency (MHz)	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
40	-32.1	14.8	17.6	-27.4	-24.2	161	-40.5	-31.1
50	-32.7	2.0	17.6	-34.3	-24.3	156	-39.4	-38.1
70	-33.4	-16.0	17.6	-48.1	-24.3	147	-36.0	-57.2
90	-32.8	-27.0	17.5	-60.9	-24.4	138	-32.4	-76.7
100	-32.6	-34.0	17.5	-68.0	-24.5	133	-30.3	-87.7

Magnitude in dB, Phase Angle in degrees.

Figure 9. S-Parameters

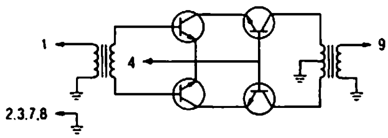
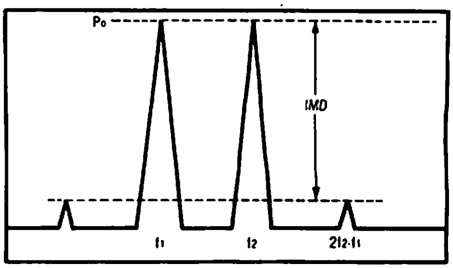


Figure 10. Functional Schematic



$I_{TO} = P_o + \frac{IMD}{2}$ @ IMD > 60dB

PEP = 4X P_o @ IMD = -32dB

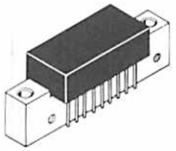
Figure 11. Intermodulation Test

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

CA4800
CA4800H

The RF Line
Wideband Linear Amplifiers

17 dB
10–1000 MHz
400 mWATT
WIDEBAND
LINEAR AMPLIFIERS



CASE 714P-01, STYLE 2
(CA)
CA4800

CASE 826-01, STYLE 6
(SIP)
CA4800H

. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  Frequency Range — 10 to 1000 MHz
  Output Power — 400 mW Typ @ 1 dB Compression, f = 500 MHz
  Power Gain — 17 dB Typ @ f = 100 MHz
  PEP — 320 mW Typ @ −32 dB IMD
  Noise Figure — 6.5 dB Typ @ f = 500 MHz
  ITO — 40 dBm Typ @ f = 1000 MHz
- All Gold Metallization for Improved Reliability

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	14	dBm
Operating Case Temperature Range	T_C	−55 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	1000	MHz
Gain Flatness (f = 10–1000 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	16	17	18	dB
Noise Figure, Broadband f = 500 MHz f = 1000 MHz	NF	— —	6.5 7.5	8 9	dB
Power Output — 1 dB Compression (f = 500 MHz)	$P_{o\ 1dB}$	300	400	—	mW
Third Order Intercept (See Figure 11, f_1 = 10–1000 MHz)	ITO	38	40	—	dBm
Input/Output VSWR f = 40–860 MHz f = 10–1000 MHz	VSWR	— —	— —	2:1 2.5:1	—
Second Harmonic Distortion (P_o = 100 mW, f_{2H} = 1000 MHz)	d_{so}	—	−50	−40	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 11) (f = 500 MHz @ −32 dB IMD)	PEP	—	320	—	mW
Supply Current	I_{CC}	200	220	240	mA
Intermodulation Distortion, 3 Tone (Vision Carrier = −8 dB, Sound Carrier = −10 dB, Sideband Signal = −17 dB. See Figure 12. f = 860 MHz, P_{SYNC} = 200 mW)	IMD	—	−60	—	dB

5

TYPICAL CHARACTERISTICS

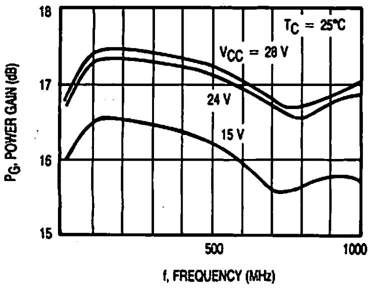


Figure 1. Frequency Response versus Voltage

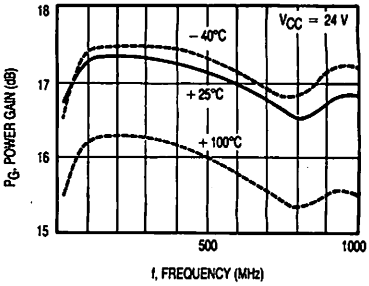


Figure 2. Frequency Response versus Temperature

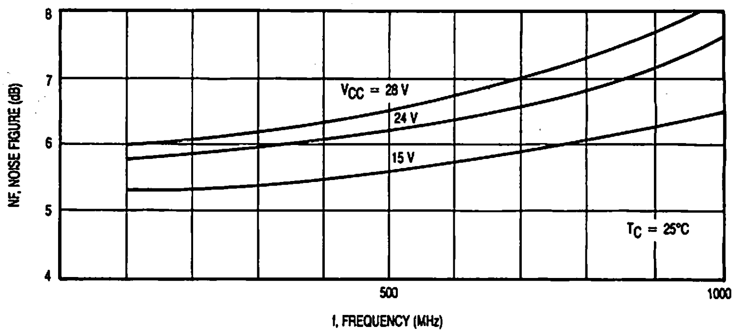


Figure 3. Noise Figure versus Frequency

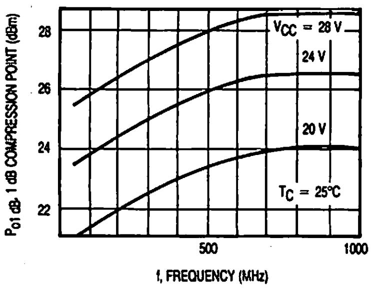


Figure 4. 1 dB Compression versus Frequency

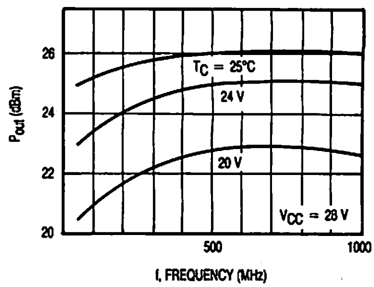


Figure 5. Peak Envelope Power versus Frequency

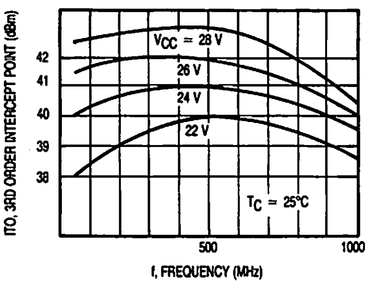


Figure 6. Third Order Intercept versus Frequency

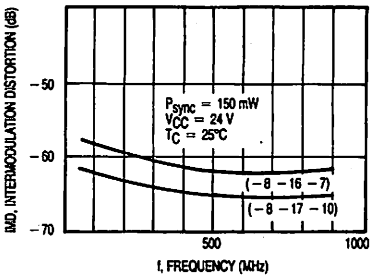


Figure 7. Intermodulation Distortion versus Frequency

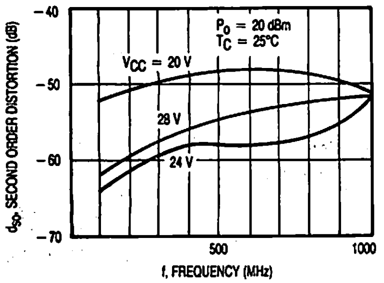


Figure 8. Second Harmonic Distortion versus Frequency

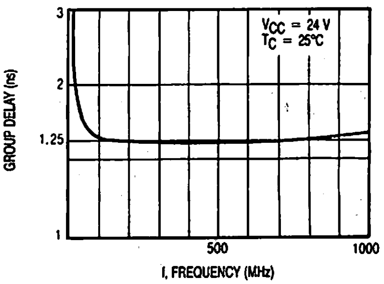


Figure 9. Group Delay versus Frequency

Biased at 24 Volts
220mA
Zo = 50 Ohms

Frequency (MHz)	S11		S21		S12		S22		k
10	−25.26	116.3	16.71	13.8	−43.08	−34.0	−12.00	95.3	9.766
110	−39.97	117.8	17.35	−47.1	−42.15	−8.6	−18.41	33.7	8.596
210	−31.20	130.0	17.35	−92.1	−41.04	−99.1	−17.27	22.1	7.534
310	−27.75	117.0	17.29	−138.1	−39.80	−18.4	−16.91	9.4	6.568
410	−27.26	114.0	17.24	177.3	−38.31	−28.4	−17.64	−4.2	5.588
510	−25.39	125.3	17.14	132.2	−36.36	−39.7	−18.85	−19.7	4.547
610	−21.39	125.2	16.87	88.3	−34.46	−56.3	−19.92	−43.8	3.784
710	−18.22	104.8	16.66	44.3	−32.66	−74.2	−20.26	−85.4	3.146
810	−16.08	71.8	16.50	1.4	−30.48	−94.0	−18.80	−137.1	2.488
910	−12.87	29.5	16.74	−42.7	−28.03	−117.4	−15.81	166.5	1.794
1010	−8.59	−20.8	16.79	−92.1	−25.74	−146.5	−12.71	104.8	1.253

Figure 10. S-Parameters

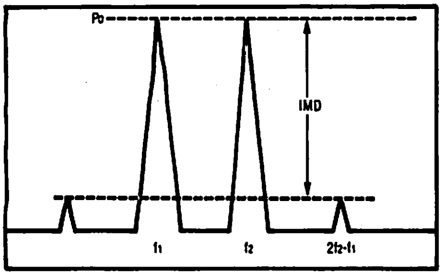


Figure 11. 2-Tone Intermodulation Test

$$I_{TO} = P_o + \frac{IMD}{2} \text{ @ IMD} > 60 \text{ dB}$$

$$PEP = 4 \times P_o \text{ @ IMD} = -32 \text{ dB}$$

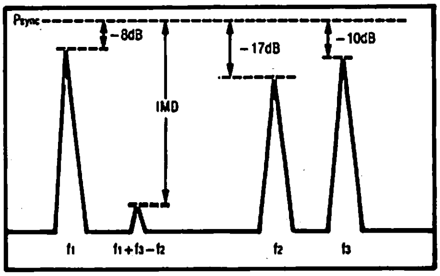


Figure 12. 3-Tone TV Intermodulation Test

f_1 = Video
f_2 = Sideband
f_3 = Sound

PIN CONFIGURATION

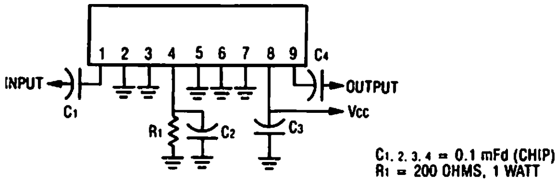


Figure 13. External Connections

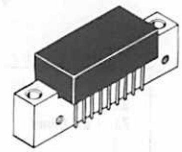
CA4812
CA4812H

The RF Line
Wideband Linear Amplifiers

. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = 12 V, T_C = 25°C:
  - Frequency Range — 10 to 1000 MHz
  - Output Power — 400 mW Typ @ 1 dB Compression, f = 500 MHz
  - PEP — 320 mW Typ @ −32 dB IMD
  - Noise Figure — 6.5 dB Typ @ f = 500 MHz
  - ITO — 40 dBm @ f = 1000 MHz
- All Gold Metallization for Improved Reliability
- Optimized for 12 Volt Operation

**17 dB
10–1000 MHz
400 mWATT
WIDEBAND
LINEAR AMPLIFIERS**



CASE 714P-01, STYLE 3
(CA)
CA4812

CASE 826-01, STYLE 7
(SIP)
CA4812H

5

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	14	Vdc
RF Power Input	P_{in}	+14	dBm
Operating Case Temperature Range	T_C	−40 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 12 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	1000	MHz
Gain Flatness (f = 10–1000 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	16	17	18	dB
Noise Figure, Broadband f = 500 MHz f = 1000 MHz	NF	— —	6.5 7.5	8 9	dB
Power Output — 1 dB Compression (f = 500 MHz)	$P_{o\ 1dB}$	300	400	—	mW
Third Order Intercept (See Figure 11, f_1 = 10–1000 MHz)	ITO	38	40	—	dBm
Input/Output VSWR f = 40–860 MHz f = 10–1000 MHz	VSWR	— —	— —	2:1 2.5:1	—
Second Harmonic Distortion (P_o = 100 mW, f_{2H} = 1000 MHz)	d_{so}	—	−50	−40	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 11) (f = 500 MHz @ −32 dB IMD)	PEP	—	320	—	mW
Supply Current	I_{CC}	360	380	400	mA
Intermodulation Distortion, 3 Tone (Vision Carrier = −8 dB, Sound Carrier = −10 dB, Sideband Signal = −17 dB. See Figure 12. f = 860 MHz, P_{sync} = 200 mW)	IMD	—	−60	—	dB

TYPICAL CHARACTERISTICS

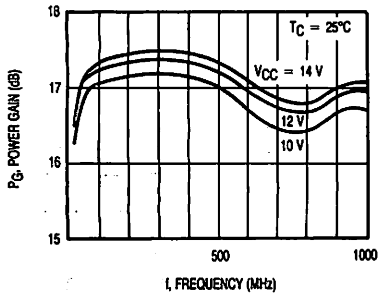


Figure 1. Frequency Response versus Voltage

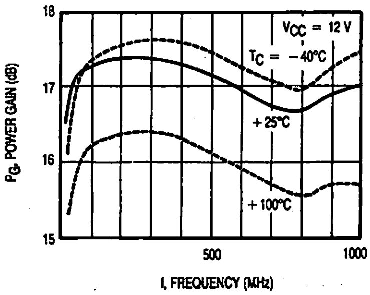


Figure 2. Frequency Response versus Temperature

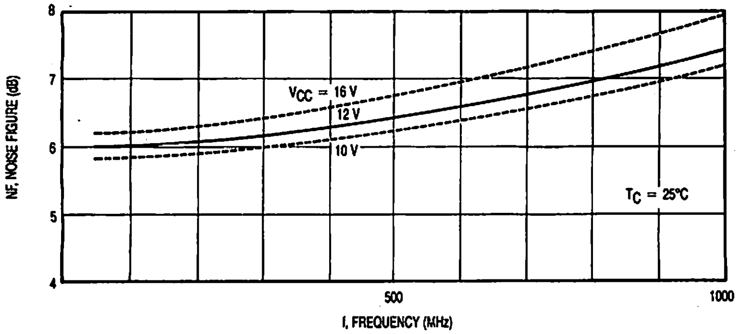


Figure 3. Noise Figure versus Voltage

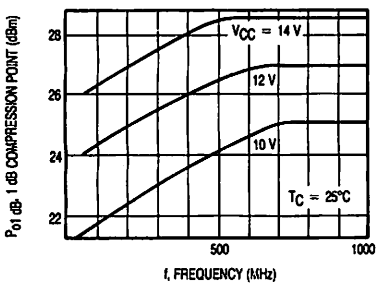


Figure 4. 1 dB Compression versus Voltage

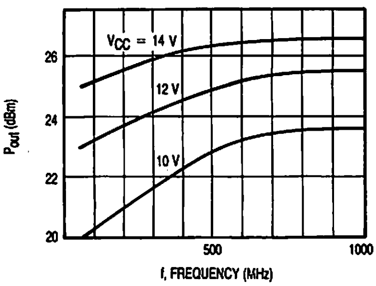


Figure 5. Peak Envelope Power versus Voltage

5

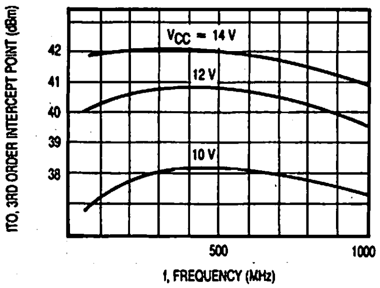


Figure 6. Third Order Intercept versus Voltage

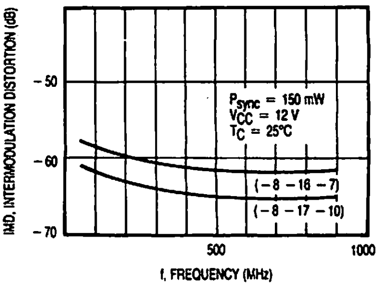


Figure 7. Intermodulation: TV Test

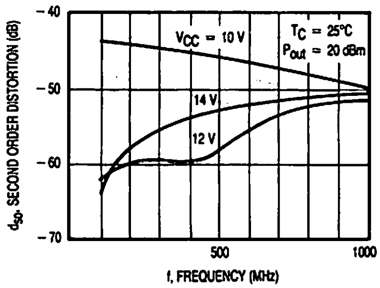


Figure 8. Second Harmonic Distortion versus Frequency

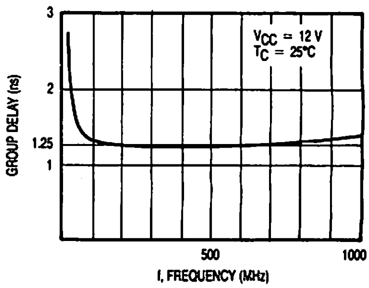


Figure 9. Group Delay versus Frequency

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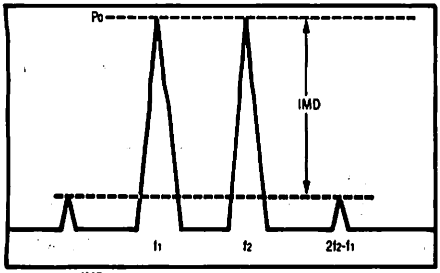
Biased at 12 Volts
378mA
Zo = 50 Ohms

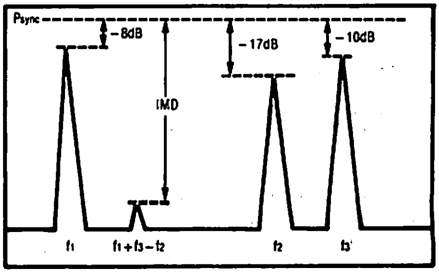
Frequency (MHz)	S11		S21		S12		S22		k
10	−26.45	120.1	16.50	14.2	−43.49	16.8	−11.58	98.1	10.425
110	−39.42	132.5	17.24	−47.2	−42.25	−0.5	−18.18	39.2	8.802
210	−31.22	133.7	17.15	−92.3	−41.15	−4.7	−16.72	29.3	7.787
310	−27.72	118.8	17.39	−138.6	−39.61	−13.4	−16.22	20.5	6.325
410	−27.24	119.2	17.33	176.2	−37.91	−24.1	−16.30	−13.6	5.249
510	−24.56	139.6	17.22	130.5	−36.08	−38.2	−16.64	−5.6	4.329
610	−19.41	136.4	16.97	86.1	−34.27	−55.2	−17.26	−6.6	3.622
710	−15.98	113.6	16.76	41.6	−32.16	−74.7	−19.19	−27.0	2.926
810	−14.04	76.9	16.66	−1.7	−30.01	−95.6	−25.19	−55.8	2.339
910	−11.66	31.1	16.93	−46.4	−27.63	−120.2	−25.82	119.3	1.728
1010	−7.98	−24.7	16.99	−97.3	−25.33	−150.7	−13.13	66.2	1.208

Figure 10. S-Parameters



$I_{TO} = P_O + \frac{IMD}{2}$ @ IMD > 60dB
PEP = 4X P_O @ IMD = −32dB

Figure 11. 2-Tone Intermodulation Test



f_1: video
f_2: sideband
f_3: sound

Figure 12. 3-Tone TV Intermodulation Test

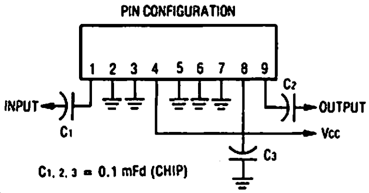
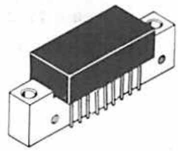


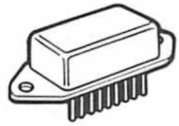
Figure 13. External Connections

CA4815
CA4815H

**17 dB
10–1000 MHz
400 mWATT
WIDEBAND
LINEAR AMPLIFIERS**



CASE 714P-01, STYLE 3
(CA)
CA4815



CASE 826-01, STYLE 7
(SIP)
CA4815H

The RF Line
Wideband Linear Amplifiers

. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

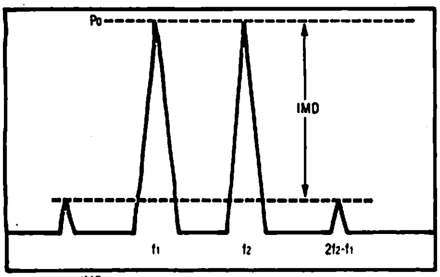
- Specified Characteristics at V_{CC} = 15 V, T_C = 25°C:
  Frequency Range — 10 to 1000 MHz
  Output Power — 400 mW Typ @ 1 dB Compression, f = 500 MHz
  Power Gain — 17 dB Typ @ f = 100 MHz
  PEP — 320 mW Typ @ −32 dB IMD
  Noise Figure — 6.5 dB Typ @ f = 500 MHz
  ITO — 40 dBm Typ @ f = 1000 MHz
- All Gold Metallization for Improved Reliability
- Optimized for 15 V Operation

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	18	Vdc
RF Power Input	P_{in}	+14	dBm
Operating Case Temperature Range	T_C	−40 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

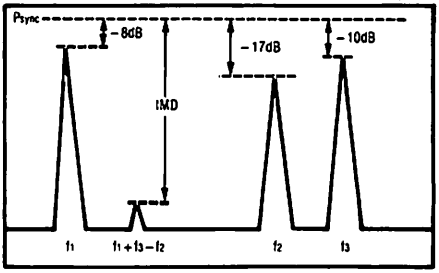
ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 15 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	1000	MHz
Gain Flatness (f = 10–1000 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	16	17	18	dB
Noise Figure, Broadband f = 500 MHz f = 1000 MHz	NF	— —	6.5 7.5	8 9	dB
Power Output — 1 dB Compression (f = 500 MHz)	$P_{o1\ dB}$	300	400	—	mW
Third Order Intercept (See Figure 1, f_1 = 10–1000 MHz)	ITO	38	40	—	dBm
Input/Output VSWR f = 40–860 MHz f = 10–1000 MHz	VSWR	— —	— —	2:1 2.5:1	—
Second Harmonic Distortion (P_o = 100 mW, f_{2H} = 1000 MHz)	d_{so}	—	−50	−40	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 1) (f = 500 MHz @ −32 dB IMD)	PEP	—	320	—	mW
Supply Current	I_{CC}	360	380	400	mA
Intermodulation Distortion, 3 Tone (Vision Carrier = −8 dB, Sound Carrier = −10 dB, Sideband Signal = −17 dB. See Figure 2. f = 860 MHz, P_{sync} = 200 mW)	IMD	—	−60	—	dB



$I_{TO} = P_O + \frac{IMD}{2}$ @ IMD > 60dB
PEP = 4X P_O @ IMD = −32dB

Figure 1. 2-Tone Intermodulation Test



f_1: video
f_2: sideband
f_3: sound

Figure 2. 3-Tone TV Intermodulation Test

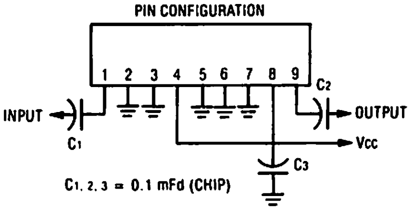


Figure 3. External Connections

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

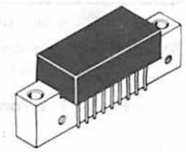
CA5800
CA5800H

The RF Line
Wideband Linear Amplifiers

. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = 28 V, T_C = 25°C:
  - Frequency Range — 10 to 1000 MHz
  - Output Power — 1 W Typ @ 1 dB Compression, f = 500 MHz
  - Power Gain — 15 dB Typ @ f = 100 MHz
  - PEP — 800 mW Typ @ −32 dB IMD
  - Noise Figure — 7.5 dB Type @ f = 500 MHz
  - ITO — 40.5 dBm @ f = 1000 MHZ
- All Gold Metallization for Improved Reliability
- Optimized for 28 V Operation

**15 dB
10–1000 MHz
800 mWATT
WIDEBAND
LINEAR AMPLIFIERS**



CASE 714P-01, STYLE 2
(CA)
CA5800

CASE 826-01, STYLE 6
(SIP)
CA5800H

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	32	Vdc
RF Power Input	P_{in}	+20	dBm
Operating Case Temperature Range	T_C	−40 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 28 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	1000	MHz
Gain Flatness (f = 10–1000 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	14	15	—	dB
Noise Figure, Broadband f = 500 MHz f = 1000 MHz	NF	— —	7.5 8.5	8.5 9.5	dB
Power Output — 1 dB Compression (f = 500 MHz)	$P_{o\ 1dB}$	630	1000	—	mW
Third Order Intercept (See Figure 9, f_1 = 47 MHz, f_2 = 658 MHz)	ITO	—	40.5	—	dBm
Input/Output VSWR f = 40–860 MHz f = 10–1000 MHz	VSWR	— —	— —	2:1 2.5:1	—
Second Harmonic Distortion (P_o = 100 mW, f_{2H} = 1000 MHz)	d_{so}	—	−55	−45	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 10) (f = 500 MHz @ −32 dB IMD)	PEP	—	800	—	mW
Supply Current	I_{CC}	360	400	440	mA
Intermodulation Distortion, 3 Tone (Vision Carrier = −8 dB, Sound Carrier = −10 dB, Sideband Signal = −17 dB. See Figure 11. f = 860 MHz, P_{sync} = 200 mW)	IMD	—	−58	—	dB
Second Order IMD (P_t = 2.75 dBm, f_1 = 373 MHz, f_2 = 450 MHz, See Fig. 9)	IM2		−65	−60	dB

5

TYPICAL CHARACTERISTICS

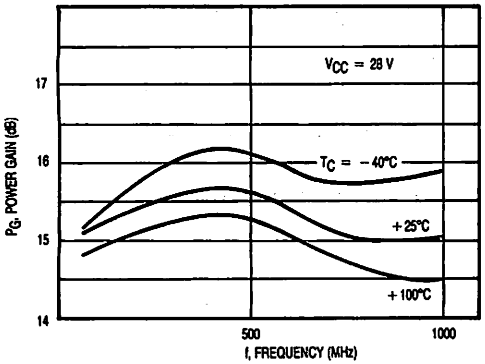


Figure 1. Frequency Response versus Temperature

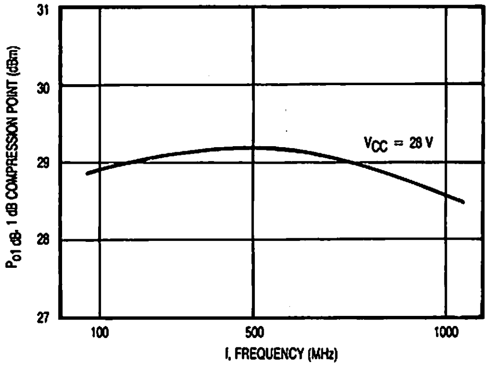


Figure 2. 1 dB Compression versus Frequency

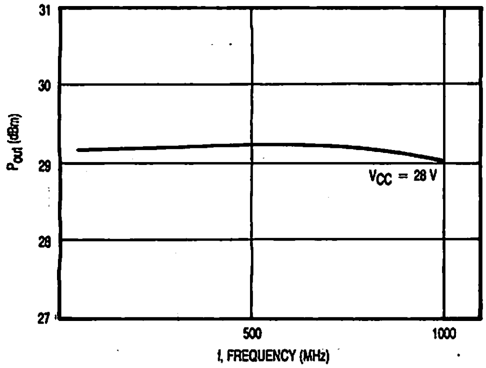


Figure 3. Peak Envelope Power versus Frequency

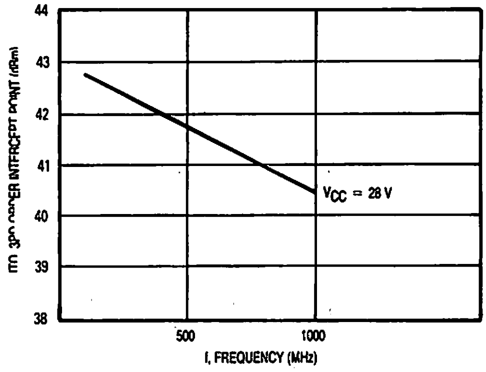


Figure 4. Third Order Intercept versus Frequency

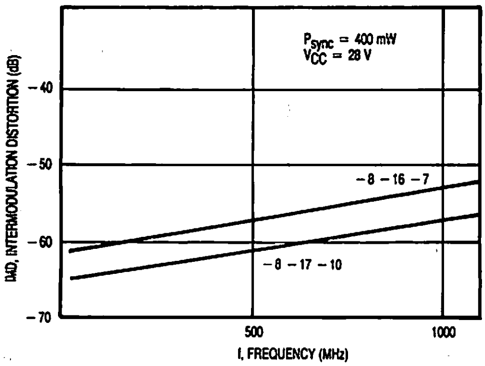


Figure 5. Intermodulation Distortion versus Frequency

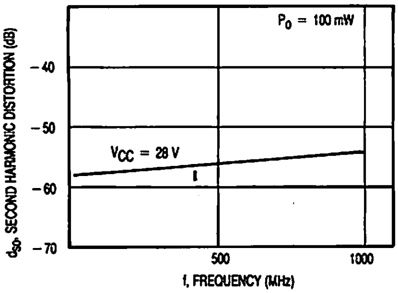


Figure 6. Second Harmonic Distortion versus Frequency

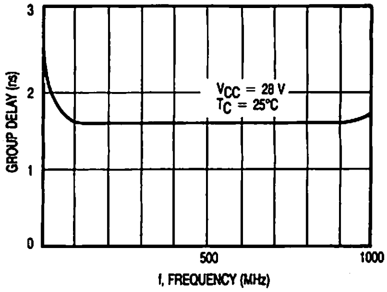


Figure 7. Group Delay versus Frequency

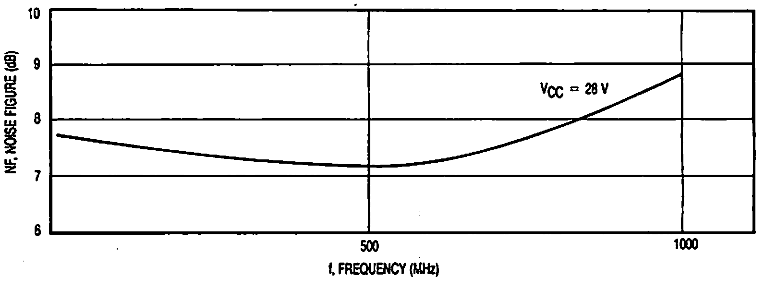
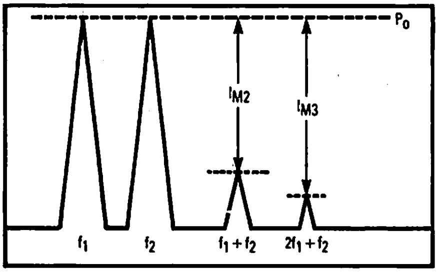
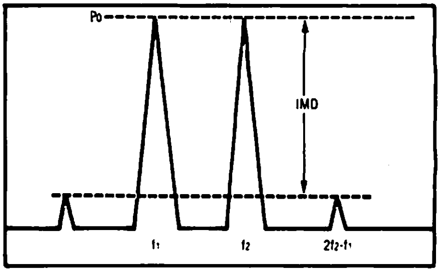


Figure 8. Noise Figure versus Frequency



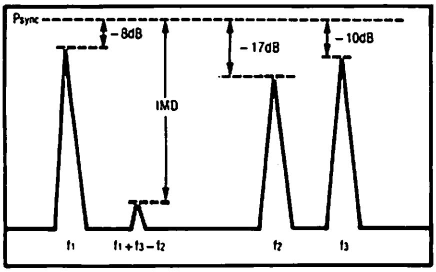
$ITO = P_O + \frac{IM3}{2}$ @ IM3 > 60 dB

Figure 9. 2-Tone Intermodulation, Test B



PEP = 4X Po @ IMD = −32dB

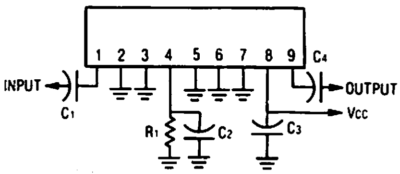
Figure 10. 2-Tone Intermodulation, Test A



f_1: video
f_2: sideband
f_3: sound

Figure 11. 3-Tone TV Intermodulation Test

PIN CONFIGURATION



$C_{1,2,3,4}$ = 0.1 mFd (CHIP)
R_1 = 90 OHMS, 2 WATTS

Figure 12. External Connections

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

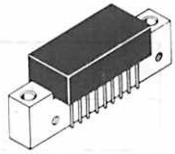
CA5815
CA5815H

The RF Line
Wideband Linear Amplifiers

. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = 15 V, T_C = 25°C:
  Frequency Range — 10 to 1000 MHz
  Output Power — 1 W Typ @ 1 dB Compression, f = 500 MHz
  Power Gain — 15 dB Typ @ f = 100 MHz
  PEP — 1 W Typ @ −32 dB IMD
  Noise Figure — 7.5 dB Typ @ f = 500 MHz
  ITO — 40.5 dBm Typ @ f = 1000 MHz
- All Gold Metallization for Improved Reliability
- Optimized for 15 Volt Operation

15 dB
10–1000 MHz
1 WATT
WIDEBAND
LINEAR AMPLIFIERS



CASE 714P-01, STYLE 3
(CA)
CA5815

CASE 826-01, STYLE 7
(SIP)
CA5815H

5

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	18	Vdc
RF Power Input	P_{in}	+20	dBm
Operating Case Temperature Range	T_C	−40 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 15 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	1000	MHz
Gain Flatness (f = 10–1000 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	14	15	—	dB
Noise Figure, Broadband f = 500 MHz f = 1000 MHz	NF	— —	7.5 8.5	8.5 9.5	dB
Power Output — 1 dB Compression (f = 500 MHz)	$P_{o\ 1dB}$	630	1000	—	mW
Third Order Intercept (See Figure 9, f_1 = 47 MHz; f_2 = 658 MHz)	ITO	—	40.5	—	dBm
Input/Output VSWR f = 40–860 MHz f = 10–1000 MHz	VSWR	— —	— —	2:1 2.5:1	—
Second Harmonic Distortion (P_o = 100 mW, f_{2H} = 1000 MHz)	d_{so}	—	−55	−45	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 10) (f = 500 MHz @ −32 dB IMD)	PEP	—	1000	—	mW
Supply Current	I_{CC}	660	700	800	mA
Intermodulation Distortion, 3 Tone (Vision Carrier = −8 dB, Sound Carrier = −10 dB, Sideband Signal = −17 dB. See Figure 11. f = 860 MHz, P_{sync} = 200 mW)	IMD	—	−60	—	dB
Second Order IMD (P_o = 2.75 dBm, f_1 = 373 mHz, f_2 = 450 MHz. See Figure 9.)	IM2	—	−65	−60	dB

TYPICAL CHARACTERISTICS

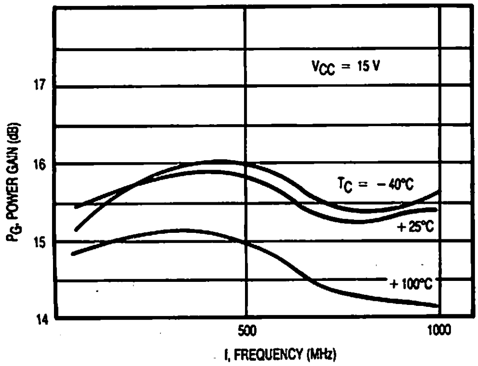


Figure 1. Frequency Response versus Temperature

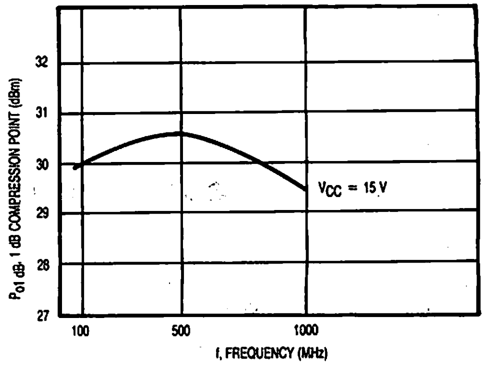


Figure 2. 1 dB Compression versus Frequency

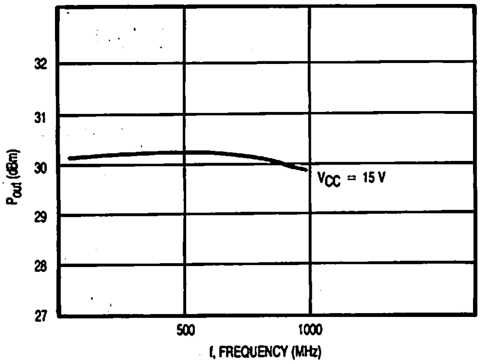


Figure 3. Peak Envelope Power versus Frequency

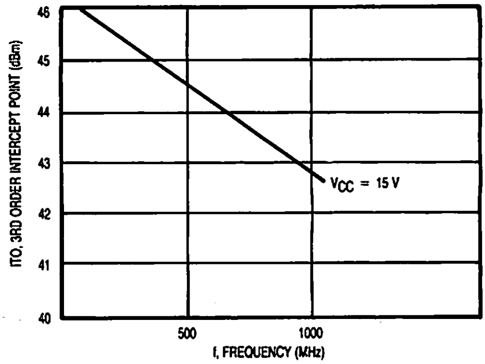


Figure 4. Third Order Intercept versus Frequency

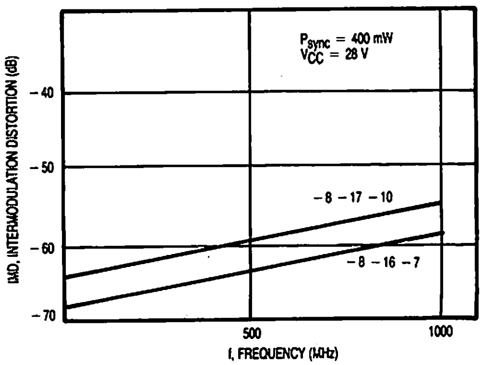


Figure 5. Intermodulation Distortion versus Frequency

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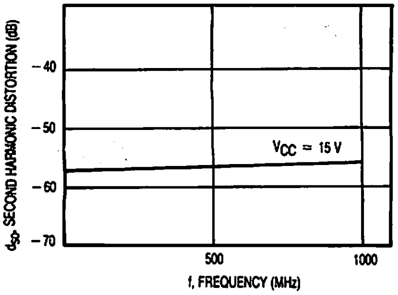


Figure 6. Second Harmonic Distortion versus Frequency

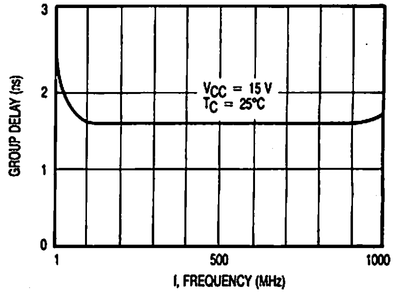


Figure 7. Group Delay versus Frequency

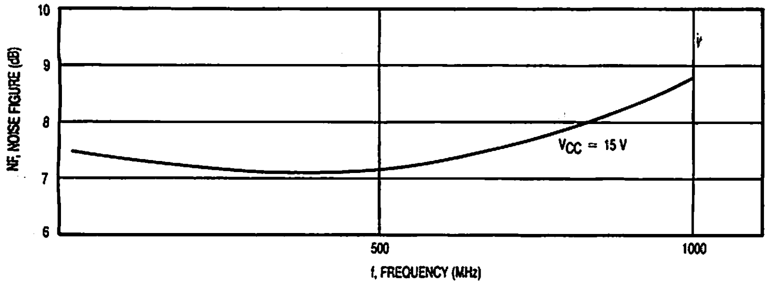
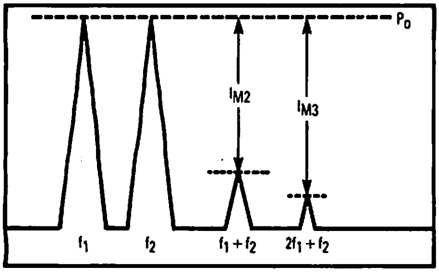
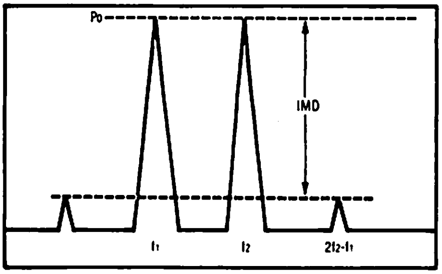


Figure 8. Noise Figure versus Frequency



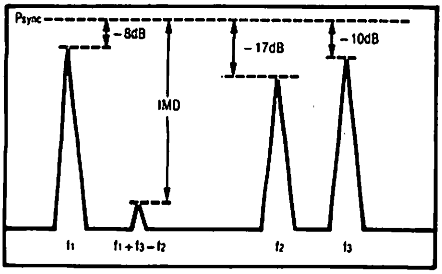
$$ITO = P_o + \frac{IM_3}{2} \text{ @ } IM_3 < 60 \text{ dB}$$

Figure 9. 2-Tone Intermodulation, Test B



PEP = 4X Po @ IMD = −32dB

Figure 10. 2-Tone Intermodulation, Test A



f1: video
f2: sideband
f3: sound

Figure 11. 3-Tone TV Intermodulation Test

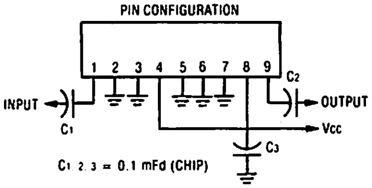


Figure 12. External Connections

Advance Information

The RF Line

Wideband Linear Amplifier

CA5900

15 dB
10–1200 MHz
800 mWATT
WIDEBAND
LINEAR AMPLIFIER

. . . designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = 28 V, T_C = 25°C:
  - Frequency Range — 10 to 1200 MHz
  - Output Power — 1.0 W Typ @ 1.0 dB Compression, f = 500 MHz
  - Power Gain — 15 dB Typ @ f = 100 MHz
  - PEP — 800 mW Typ @ −32 dB IMD
  - Noise Figure — 7.5 dB Typ @ f = 500 MHz
  - ITO — 41 dBm @ f = 752 MHz
- All Gold Metallization for Improved Reliability
- Optimized for 28 Volt Operation

CASE 714P-01
(CA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	32	Vdc
RF Power Input	P_{in}	+20	dBm
Operating Case Temperature Range	T_C	−40 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 28 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I_{CC}	360	400	440	mA
Frequency Range	BW	10	—	1200	MHz
Gain Flatness (f = 10–1200 MHz)	—	—	±0.5	±1.0	dB
Power Gain (f = 100 MHz)	P_G	14	15	—	dB
Noise Figure, Broadband f = 500 MHz f = 1200 MHz	NF	— —	7.5 8.5	8.5 9.5	dB
Power Output — 1.0 dB Compression (f = 500 MHz)	$P_{o\ 1dB}$	630	1000	—	mW
Third Order Intercept (See Figure 4, f_1 = 47 MHz, f_2 = 658 MHz)	ITO	—	41	—	dBm
Input/Output VSWR f = 40–1000 MHz f = 10–1200 MHz	VSWR	— —	— —	2:1 2.6:1	—
Second Harmonic Distortion (P_o = 100 mW, f_{2H} = 1200 MHz)	d_{so}	—	−50	−45	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 1) (f = 500 MHz @ −32 dB IMD)	PEP	—	800	—	mW
Intermodulation Distortion, 3 Tone (Vision Carrier = −8.0 dB, Sound Carrier = −10 dB, Sideband Signal = −17 dB. See Figure 2, f = 860 MHz, P_{sync} = 200 mW)	IMD	—	−58	—	dB
Second Order Intermodulation Distortion (P_o = 2.75 dBm, f_1 = 373 MHz, f_2 = 450 MHz, See Figure 4)	IM2	—	−65	−60	dB

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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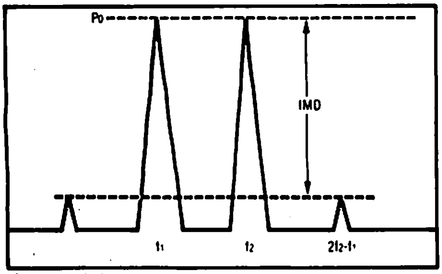
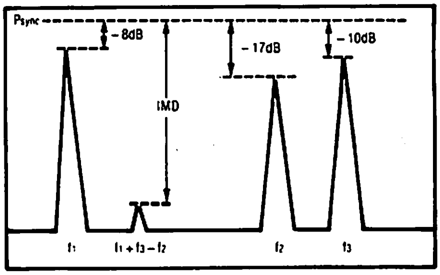


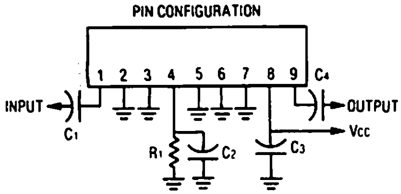
PEP = 4X Po @ IMD = −32dB

Figure 1. 2-Tone Intermodulation, Test A



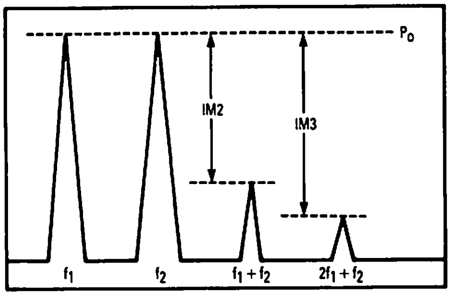
f_1: video
f_2: sideband
f_3: sound

Figure 2. 3-Tone TV Intermodulation Test



$C_{1,2,3,4}$ = 0.1 mFd (CHIP)
R_1 = 90 OHMS, 2 WATTS

Figure 3. External Connections



$ITO = P_0 + \frac{IM3}{2}$ @ IM3 > 60 dB

Figure 4. 2-Tone Intermodulation, Test B

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

CA5915

Advance Information

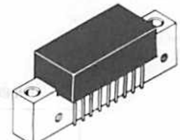
The RF Line

Wideband Linear Amplifier

15 dB
10–1200 MHz
1.0 WATT
WIDEBAND
LINEAR AMPLIFIER

... designed for amplifier applications in 50 to 100 ohm systems requiring wide bandwidth, low noise and low distortion. This hybrid provides excellent gain stability with temperature and linear amplification as a result of the push-pull circuit design.

- Specified Characteristics at V_{CC} = 15 V, T_C = 25°C:
  - Frequency Range — 10 to 1200 MHz
  - Output Power — 1.0 W Typ @ 1.0 dB Compression, f = 500 MHz
  - Power Gain — 15 dB Typ @ f = 100 MHz
  - PEP — 1.0 mW Typ @ −32 dB IMD
  - Noise Figure — 7.5 dB Typ @ f = 500 MHz
  - ITO — 41 dBm @ f = 752 MHz
- All Gold Metallization for Improved Reliability
- Optimized for 15 Volt Operation



CASE 714P-01
(CA)

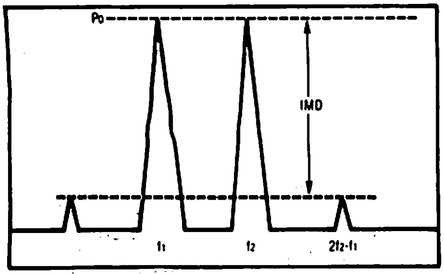
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	18	Vdc
RF Power Input	P_{in}	+20	dBm
Operating Case Temperature Range	T_C	−40 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 15 V, 50 Ω system unless otherwise noted)

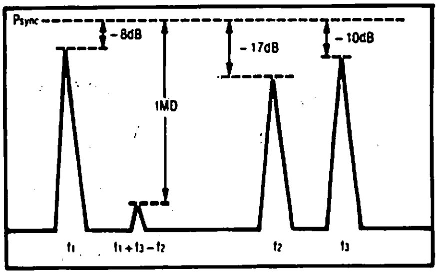
Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I_{CC}	660	700	800	mA
Frequency Range	BW	10	—	1200	MHz
Gain Flatness (f = 10–1200 MHz)	—	—	±0.5	±1.0	dB
Power Gain (f = 100 MHz)	P_G	14	15	—	dB
Noise Figure, Broadband f = 500 MHz f = 1200 MHz	NF	— —	7.5 8.5	8.5 9.5	dB
Power Output — 1.0 dB Compression (f = 500 MHz)	$P_{o\,1dB}$	630	1000	—	mW
Third Order Intercept (See Figure 4, f_1 = 47 MHz, f_2 = 658 MHz)	ITO	—	41	—	dBm
Input/Output VSWR f = 40–1000 MHz f = 10–1200 MHz	VSWR	— —	— —	2:1 2.6:1	—
Second Harmonic Distortion (P_o = 100 mW, f_{2H} = 1200 MHz)	d_{so}	—	−50	−45	dB
Peak Envelope Power (Two Tone Distortion Test — See Figure 1) (f = 500 MHz @ −32 dB IMD)	PEP	—	1000	—	mW
Intermodulation Distortion, 3 Tone (Vision Carrier = −8.0 dB, Sound Carrier = −10 dB, Sideband Signal = −17 dB. See Figure 2, f = 860 MHz, P_{sync} = 200 mW)	IMD	—	−60	—	dB
Second Order Intermodulation Distortion (P_o = 2.75 dBm, f_1 = 373 MHz, f_2 = 450 MHz, See Figure 4)	IM2	—	−65	−60	dB

This document contains information on a new product. Specifications and information herein are subject to change without notice.



PEP = 4X Po @ IMD = −32dB

Figure 1. 2-Tone Intermodulation, Test A



f1: video
f2: sideband
f3: sound

Figure 2. 3-Tone TV Intermodulation Test

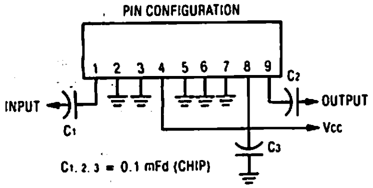
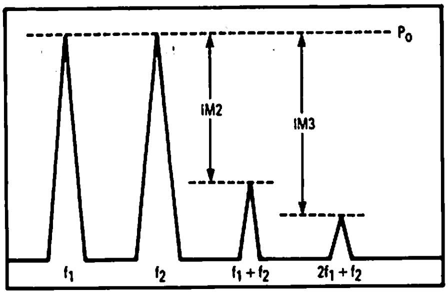


Figure 3. External Connections



$$ITO = P_o + \frac{IM3}{2} \text{ @ } IM3 > 60 \text{ dB}$$

Figure 4. 2-Tone Intermodulation, Test B

5

CA7901

The RF Line

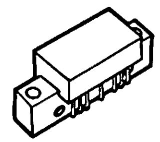
60-Channel (450 MHz) CATV Hi-Slope Trunk Amplifier

. . . increased gain slope versus frequency effectively reduces the need for equalization external to the amplifier in CATV systems.

Designed for broadband applications requiring low-distortion amplification. Specifically intended for CATV market requirements. These amplifiers feature ion-implanted arsenic emitter transistors and an all gold metallization system.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  - Frequency Range — 40 to 450 MHz
  - Power Gain — 15.4 dB Typ @ f = 50 MHz
  - — 20.5 dB Typ @ f = 450 MHz
  - Noise Figure — 5.5 dB Typ @ f = 450 MHz
  - CTB — −60 dB @ V_{out} = 48 dBmV with 5 dB cable slope.
- All Gold Metallization System for Improved Reliability

15–20 dB
40–450 MHz
60-CHANNEL
CATV
TRUNK AMPLIFIER



CASE 714F-01, STYLE 1
[CA (POS. SUPPLY)]

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	60	dBmV
DC Supply Voltage	V_{CC}	28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, T_C = 25°C, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	450	MHz
Power Gain — 50 MHz — 450 MHz	Gp	14.6 20	15.4 20.5	16.2 21	dB
Gain Slope	S	4.7	5.1	5.5	dB
Gain Flatness (Note 1)	—	—	—	±0.2	dB
Return Loss — Input/Output (f = 40–450 MHz)	IRL/ORL	18	20	—	dB
Composite Second Order Distortion (V_{out} = +48 dBmV @ 450 MHz, Ch. H22, 60-Channel @ 5.0 dB Cable Upslope)	CSO	—	−68	−61	dB
Cross Modulation Distortion (V_{out} = +48 dBmV @ 450 MHz, Ch. 2, 60-Channel @ 5.0 dB Cable Upslope)	XMD	—	−62	−60	dB
Composite Triple Beat (V_{out} = +48 dBmV @ 450 MHz, Ch. H22, 60-Channel @ 5.0 dB Cable Upslope)	CTB	—	−60	−58	dB
Noise Figure f = 50 MHz f = 450 MHz	NF	— —	4.6 5.5	6.0 7.0	dB
DC Current	I_{DC}	—	220	240	mA

Note: 1. Flatness calculation is based upon the following gain curve:

$$G_f = G_{50} + \Delta G\,[\alpha\,(f-50) + \beta\,(f-50)^2 + \gamma\,(f-50)^3]$$

where: G_{50} = Gain at 50 MHz
G_f = Gain at frequency f MHz
ΔG = Gain slope between 50 MHz and 450 MHz
$\alpha = 3.132\ 10^{-3}$
$\beta = 1.993\ 10^{-6}$
$\gamma = -8.934\ 10^{-9}$

5

CA97901

The RF Line

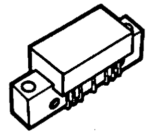
36-Channel (450 MHz) CATV Hi-Slope Input/Output Trunk Amplifier

... allows increased trunk length. Effectively reduces trunk distortion. 5.0 dB less output noise at low end.

Designed for broadband applications requiring low-distortion amplification. Specifically intended for CATV market requirements. These amplifiers feature ion-implanted arsenic emitter transistors and an all gold metallization system. The input amplifier is tuned for minimum noise figure while the output amplifier is tuned for minimum distortion..

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  - Frequency Range — 40 to 450 MHz
  - Power Gain — 15.6 dB Typ @ f = 50 MHz
    — 20.7 dB Typ @ f = 450 MHz
  - Noise Figure — 5.7 dB Typ @ f = 450 MHz
  - CTB — −66 dB @ V_{out} = 46 dBmV
- All Gold Metallization System for Improved Reliability

**15–20 dB
40–450 MHz
36-CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIER**



CASE 714F-01, STYLE 1
[CA (POS. SUPPLY)]

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	69	dBmV
DC Supply Voltage	V_{CC}	28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, T_C = 25°C, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	450	MHz
Power Gain — 50 MHz — 450 MHz	Gp	14.8 20.2	15.6 20.7	16.4 21.2	dB
Gain Slope	S	4.7	5.1	5.5	dB
Gain Flatness (Note 1)	—	—	—	±0.2	dB
Return Loss — Input/Output (f = 40 MHz) (f = 50–80 MHz) (f = 80–160 MHz) (f = 160–450 MHz)	IRL/ORL	22 20 19 18	26 24 22 20	— — — —	dB
Composite Second Order Distortion (V_{out} = +46 dBmV per ch., Ch. H20, 36-CH Flat) (Note 2)	CSO	—	−68	−65	dB
Cross Modulation Distortion (V_{out} = +46 dBmV per ch., Ch. 2, 36-CH Flat) (Note 2)	XMD	—	−66	−65	dB
Composite Triple Beat (V_{out} = +46 dBmV per ch., Ch. H20, 36-CH Flat) (Note 2)	CTB	—	−66	−65	dB
Noise Figure (f = 50 MHz) (f = 450 MHz)	NF	— —	4.6 5.5	6.0 6.8	dB
DC Current	I_{DC}	—	220	240	mA

Note 1 and Note 2 — See Next Page.

5

Note: 1. Flatness calculated is based upon the following gain curve:

$$G_f = G_{50} + \Delta G\,[\alpha\,(f-50) + \beta\,(f-50)^2 + \gamma\,(f-50)^3]$$

where: G_{50} = Gain at 50 MHz
G_f = Gain at frequency f MHz
ΔG = Gain slope between 50 MHz and 450 MHz
$\alpha = 3.132 \cdot 10^{-3}$
$\beta = 1.993 \cdot 10^{-6}$
$\gamma = -8.934 \cdot 10^{-9}$

Note 2: The following Channels are turned on for the CTB, XMOD and CSO measurement:

Channel #	Frequency (MHz)	Channel #	Frequency (MHz)	Channel #	Frequency (MHz)
1	55.25	13	235.25	25	325.25
2	61.25	14	247.25	26	337.25
3	133.25	15	253.25	27	349.25
4	139.25	16	259.25	28	361.25
5	145.25	17	265.25	29	367.25
6	151.25	18	271.25	30	373.25
7	163.25	19	283.25	31	385.25
8	175.25	20	289.25	32	391.25
9	187.25	21	295.25	33	409.25
10	205.25	22	301.25	34	415.25
11	217.25	23	313.25	35	421.25
12	229.25	24	319.25	36	433.25

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

CR820

Advance Information

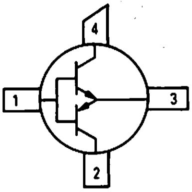
The RF Line

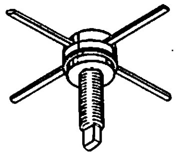
High Frequency Complementary Pair Transistor Array

HIGH FREQUENCY COMPLEMENTARY PAIR TRANSISTOR ARRAY NPN/PNP SILICON

... designed for use as an output device in very fast video amplifier circuits. The CR820 transistor array is a complementary pair of silicon bipolar transistors connected as emitter followers. Their primary application will be in black and white video monitors and other uses where discrete steps of brightness are required.

- High Voltage — $V_{(BR)CBO}$ = 70 V Min
- High Frequency — f_T = 1000 MHz
- Low Output Capacitance — C_{cb} = 2.5 pF Max @ V_{CB} = 15 V
- Gold Metallization
- Common-Base Common-Emitter Configuration





CASE 244D-01, STYLE 3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	65	V
Collector-Base Voltage	V_{CBO}	70	V
Collector Current — Continuous	I_C	400	mA
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1 mA, I_B = 0) (I_C = −1 mA, I_B = 0)	4-3 2-3	$V_{(BR)CEO1}$ $V_{(BR)CEO2}$	70 −65	— —	— —	V
Collector-Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0) (I_C = −0.1 mA, I_E = 0)	4-1 2-1	$V_{(BR)CBO1}$ $V_{(BR)CBO2}$	120 −80	— —	— —	V
ON CHARACTERISTICS						
DC Current Gain (I_C = 50 mA, V_{CE} = 5 V) (I_C = −50 mA, V_{CE} = −5 V)	4-1-3 2-1-3	H_{fe1} H_{fe2}	20 20	— —	60 60	—
Base-Emitter Forward Voltage (I_B = 1 mA, −1 mA)	1-3	$V_{(BR)CBO}$	—	+0.7, −0.7	—	V
DYNAMIC CHARACTERISTICS						
Collector-Base Capacitance (V_{CB} = 15 V) (V_{CB} = −15 V)	4-1 2-1	C_{cb1} C_{cb2}	— —	— —	2.5 2.5	pF
Cutoff Frequency (I_C = 50 mA, V_{CE} = 15 V) (I_C = 50 mA, V_{CE} = 15 V)	4-1-3 2-1-3	$F_{\tau 1}$ $F_{\tau 2}$	1.0 1.0	— —	— —	GHz

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

CR2424
CR2424H
CR2425

The RF Line

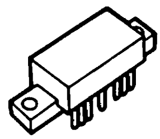
Video Driver Hybrid Amplifiers

... designed specifically for use as the video channel final stage in high resolution monitors.

- Typical 10–90% Transition Times are 2.5 ns
- 130 MHz Minimum Bandwidth at 40 Vp-p Output
- Low Power Consumption
- Excellent Grey-Scale Linearity
- Unconditional Stability
- All Gold (Monometallic) Metallization System for the Ultimate in Reliability
- Also Available In Reverse Polarity Version (−60 V Supply) For Grid Drive Applications. Part Numbers Are CR2424R And CR2425R.

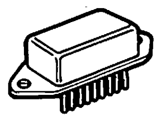
**2.5 ns
130 MHz
VIDEO DRIVER
HYBRID
AMPLIFIERS**

CR2424



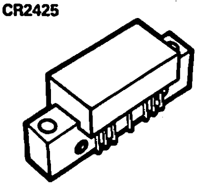
CASE 714G-01, STYLE 1
(CA LP)

CR2424H



CASE 826-01, STYLE 1
(SIP)

CR2425



CASE 714F-01, STYLE 1
(CA)

5

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	70	Vdc
Case Operating Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 60 V, T_C = 25°C, C_{Load} = 8.5 pF, 40 V Peak-to-Peak output swing with 30 Vdc offset; R_1 = 215 ohms, C_1 = 90 pF typ.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (With Input Open Circuited)	I_{CC}	39.5	43.5	47.5	mA
Input DC Voltage (With Input Open Circuited)	V_{inDC}	1.15	1.4	1.65	V
Output DC Voltage (With Input Open Circuited)	V_{outDC}	26	30	34	V
Voltage Gain (1) (2)	A_V	11.2	12.4	13.2	V/V
Transient Response (2) — Rise Time (10% to 90%)	t_r	—	2.5	2.9	ns
— Overshoot	$V_{os,r}$	—	8.0	15	%
— Fall Time (10% to 90%)	t_f	—	2.5	2.9	ns
— Overshoot	$V_{os,f}$	—	6.0	10	%
Operating Supply Current (V_{out} = 40 V Peak-to-Peak, 50 MHz Square Wave with 30 V offset) (3)	I_{CC}, max	—	—	100	mA
Linearity Error (V_{out} = +5.0 V to +55 V)	—	—	—	5.0	%

NOTES:
(1) $A_V = V_{out}/V_s$
(2) Input Signal is nominally a 62.5 kHz square wave of 3.25 V peak-to-peak with 1.4 Vdc offset. Input t_r, t_f < 1.0 ns.
(3) Output is not short circuit protected.

TYPICAL CHARACTERISTICS

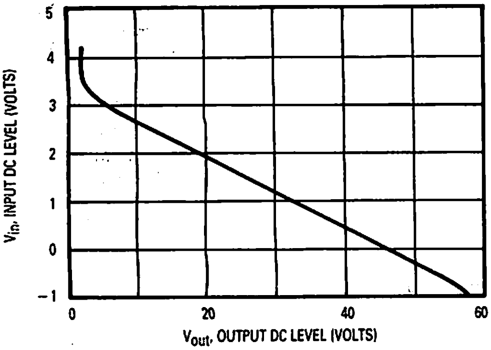


Figure 1. Voltage Ratio at RF Input Port

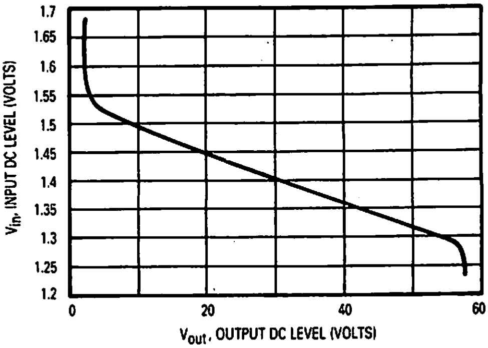


Figure 2. Voltage Ratio at Port 1

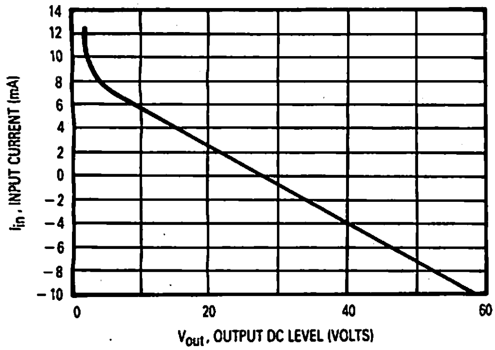


Figure 3. Output Voltage versus Input Current

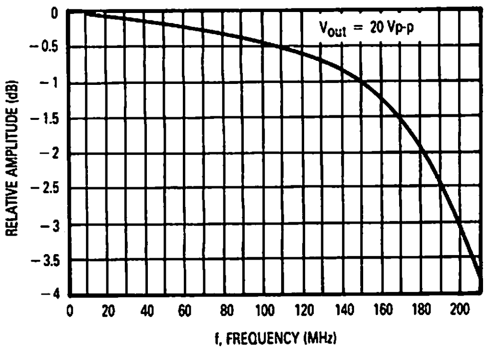


Figure 4. Frequency Response

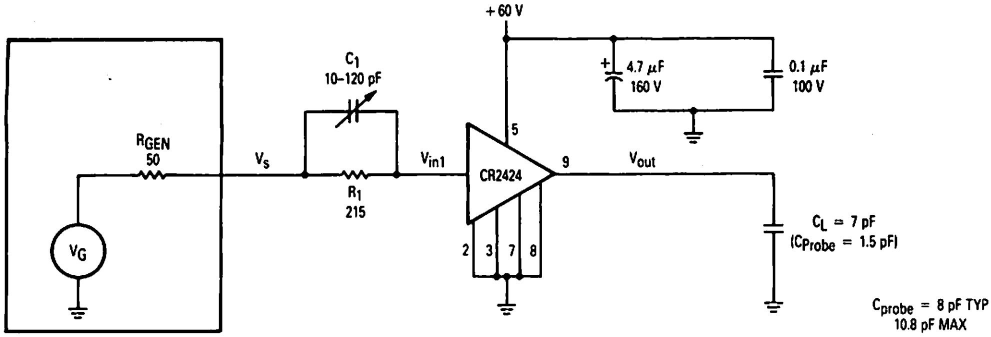


Figure 5. CRT Driver Test Circuit

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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

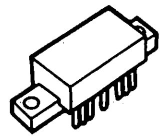
CR3424
CR3424H
CR3425

The RF Line
Video Driver Hybrid Amplifiers

2.7 ns
115 MHz
VIDEO DRIVER
HYBRID
AMPLIFIERS

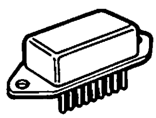
- Designed Specifically for use as the Video Channel Final Stage in High Resolution Monitors
- Low Power Consumption
- Typical 10–90% Transitions Times are 2.7 ns
- 115 MHz Minimum Bandwidth for 40 Vp-p Output Swing
- Excellent Grey Scale Linearity
- Unconditional Stability
- All Gold (Monometallic) Metallization System for the Ultimate in Reliability
- 80 Volt Supply Operation Provides Large DC Offset Range for Color Applications
- Also Available in Reverse Polarity Version (−80 V Supply) for Grid Drive Applications. Part Numbers are CR3424R and CR3425R.

CR3424



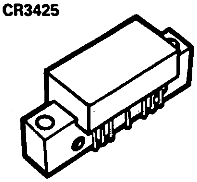
CASE 714G-01, STYLE 1
(CA LP)

CR3424H



CASE 826-01, STYLE 1
(SIP)

CR3425



CASE 714F-01, STYLE 1
(CA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	90	Vdc
Case Operating Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 80 Vdc, T_C = 25°C, C_{Load} = 10 pF, R_1 = 287 ohms, C_1 = 60 pF Typ., V_{out} = 40 V Peak-to-Peak with 40 Vdc offset). See Figure 4 for test circuit.

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (With Input Open Circuited)	I_{CC}	41	45	49	mA
DC Input Voltage (With Input Open Circuited)	V_{inDC}	1.3	1.55	1.8	Vdc
DC Output Voltage (With Input Open Circuited)	V_{outDC}	36	40	44	Vdc
Voltage Gain (1) (2)	A_V	11.5	12.7	13.5	V/V
Transient Response (2) — Rise Time (10% to 90%)	t_r	—	2.7	3.1	ns
— Overshoot	$V_{os,r}$	—	—	10	%
— Fall Time (90% to 10%)	t_f	—	2.7	3.1	ns
— Overshoot	$V_{os,f}$	—	—	10	%
Bandwidth (−3.0 dB Point)		115	—	—	MHz
Operating Supply Current (V_{out} = 40 V Peak-to-Peak, 50 MHz Square Wave with 40 V offset) (3)	I_{CC}, max	—	—	100	mA
Linearity Error (V_{out} = +5.0 V to +55 V)	—	—	—	5.0	%

NOTES:
(1) $A_V = V_{out}/V_s$
(2) Signal source output signal (V_s in Figure 1) is nominally a 62.5 kHz square wave of 3.25 V peak-to-peak with 1.4 Vdc offset
(3) Output is not short circuit protected

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TYPICAL CHARACTERISTICS

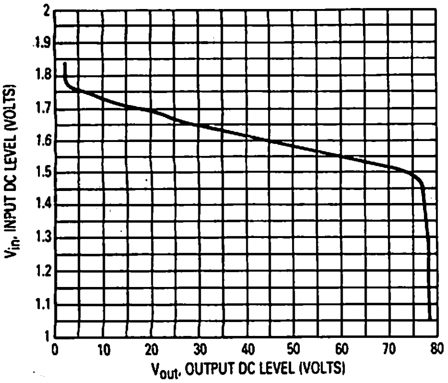

Figure 1. V_{in} versus V_{out}

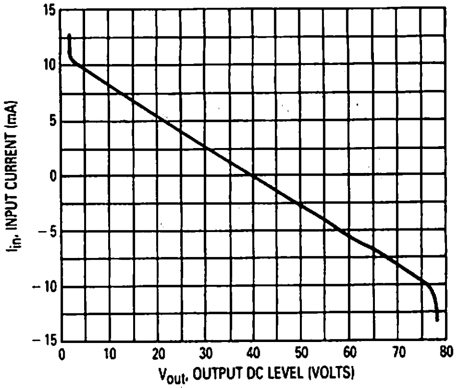

Figure 2. I_{in} versus V_{out}

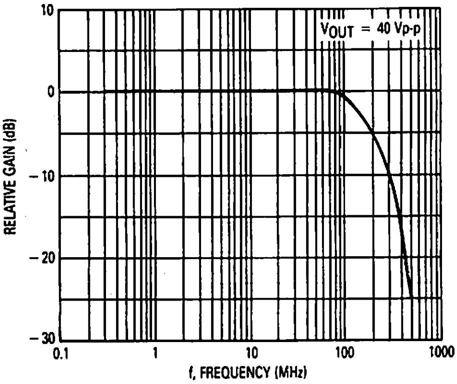

Figure 3. Frequency Response

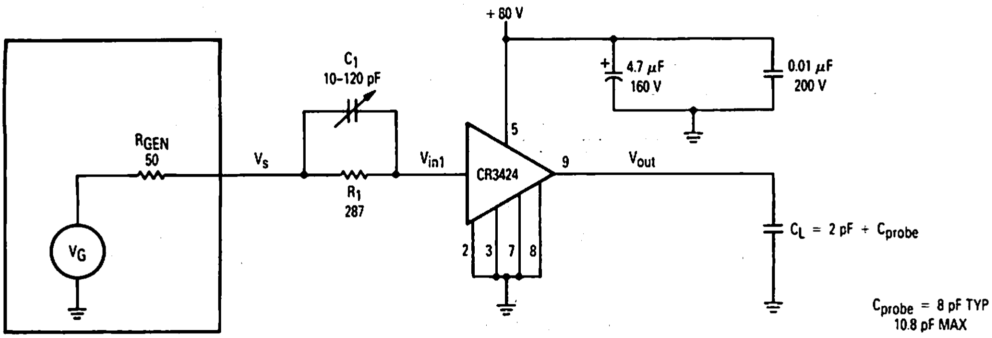

Figure 4. Hybrid Amplifier Test Circuit

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DHP02-36-40

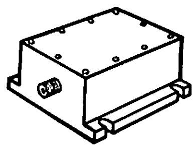
The RF Line

Linear Power Amplifier

. . . designed for wideband linear applications in the 1–200 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 28 volts.

- Specified V_{CC} = 28 Volt and T_C = 25°C Characteristics:
  Frequency Range — 1 to 200 MHz
  Output Power — 4 W Typ @ 1 dB Gain Compression, f = 100 MHz
  Power Gain — 35 dB Typ @ f = 100 MHz
  ITO — 53 dBm Typ @ f = 100 MHz
  Noise Figure — 6 dB Typ @ f = 200 MHz
- 500 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- Moisture Resistant, EMI Shielded Package

**4 WATTS
1 TO 200 MHz
LINEAR
POWER
AMPLIFIER**



DHP
CASE 389-01, STYLE 1

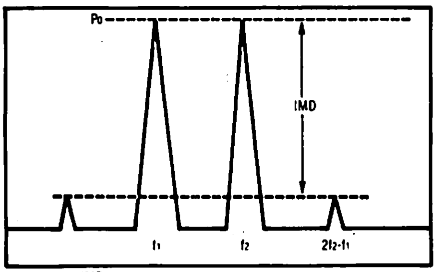
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	30	Vdc
RF Power Input	P_{in}	+5	dBm
Operating Case Temperature Range	T_C	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +100	°C

5

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 28 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1	—	200	MHz
Gain Flatness (Peak-to-Peak) (f = 1–200 MHz)	—	—	2	3	dB
Power Gain (f = 100 MHz)	P_G	33.5	35	36.5	dB
Noise Figure, Broadband f = 100 MHz f = 200 MHz	NF	— —	5 6	6.5 7.5	dB
Power Output — 1 dB Compression f = 100 MHz f = 200 MHz	$P_{o1\,dB}$	35 34	36 35	— —	dBm
Third Order Intercept f = 100 MHz (See Figure 1) f = 200 MHz	ITO	51 46	53 48	— —	dBm
Input/Output VSWR (f = 1–200 MHz)	VSWR	—	1.5:1	2:1	—
Supply Current	I_{CC}	800	870	940	mA



$I_{TO} = P_o + \frac{IMD}{2}$ @ IMD > 60dB   PEP = 4X Po @ IMD = −32dB

Figure 1. 2-Tone Intermodulation Test

DHP05-18-20

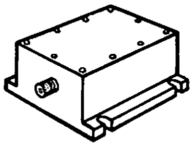
The RF Line

Linear Power Amplifier

...designed for wideband linear applications in the 30 to 500 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified Characteristics at V_{CC} = 24 V, T_C = 25°C:
  - Frequency Range — 30 to 500 MHz
  - Output Power — 2 W Typ @ 1 dB Gain Compression, f = 500 MHz
  - Power Gain — 18 dB Typ @ f = 50 MHz
  - ITO — 51 dBm Typ @ f = 300 MHz
  - Noise Figure — 5 dB Typ @ f = 300 MHz
- Designed for use in 50 Ohm Systems
- Moisture Resistant, EMI Shielded Package

**18 dB
30–500 MHz
2 WATTS
LINEAR POWER
AMPLIFIER**



DHP
CASE 389-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	18	dBm
Operating Case Temperature Range	T_C	−55 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +85	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 24 V)	I_{CC}	780	830	880	mA
Power Gain (f = 50 MHz)	Gp	17	18	19	dB
Bandwidth	BW	30	—	500	MHz
Gain Slope (f = 30–500 MHz)	S	0	0.7	1.6	dB
Gain Flatness (P-P around slope) (f = 30–500 MHz)	—	—	0.5	1	dB
Input/Output VSWR (f = 30–500 MHz)	—	—	1.2:1	1.5:1	—
Output Power @ 1 dB Gain Compression (f = 300 MHz) (f = 500 MHz)	$P_{o1\ dB}$	33 31	35 33	— —	dBm
Third Order Intercept Point (f = 300 MHz) (f = 500 MHz)	ITO	49 43	51 45	— —	dBm
Noise Figure (f = 300 MHz) (f = 500 MHz)	NF	— —	5 6.5	6 7.5	dB

DHP05-36-10

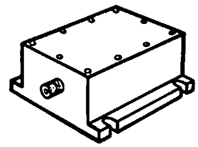
The RF Line

Linear Power Amplifier

. . . designed for wideband linear applications in the 30 to 500 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified V_{CC} = 24 Volt and T_C = 25°C Characteristics:
  Frequency Range — 30 to 500 MHz
  Output Power — 1 W Typ @ 1 dB Gain Compression, f = 300 MHz
  Power Gain — 38.5 dB Typ @ f = 50 MHz
  ITO — 42 dBm Typ @ f = 500 MHz
  Noise Figure — 6 dB Typ @ f = 500 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- Moisture Resistant, EMI Shielded Package

**1 WATT
30–500 MHz
LINEAR
POWER
AMPLIFIER**



DHP
CASE 389-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	−3	dBm
Storage Temperature Range	T_{stg}	−55 to +100	°C
Operating Temperature Range	T_C	−40 to +85	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 24 V)	I_{CC}	550	600	640	mA
Power Gain (f = 50 MHz)	Gp	35	36.5	38	dB
Bandwidth	BW	30	—	500	MHz
Gain Slope (f = 30–500 MHz)	S	0	1.5	3	dB
Gain Flatness (P-P around slope) (f = 30–500 MHz)	—	—	0.5	1	dB
Input/Output VSWR (f = 30–500 MHz)	—	—	1.2:1	1.5:1	—
Output Power @ 1 dB Gain Compression (f = 300 MHz) (f = 500 MHz)	$P_{o1\,dB}$	31 28	33 30	— —	dBm
Third Order Intercept Point (f = 300 MHz) (f = 500 MHz)	ITO	46 39	49 42	— —	dBm
Noise Figure (f = 300 MHz) (f = 500 MHz)	NF	— —	5 6	6 7	dB

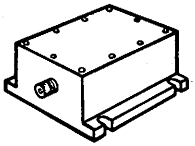
DHP10-14-15

The RF Line
Linear Power Amplifier

. . . designed for wideband linear applications in the 10 to 1000 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 28 volts.

- Specified Characteristics V_{CC} = 28 Volt and T_C = 25°C Characteristics:
  Frequency Range — 10 to 1000 MHz
  Output Power — 1.6 W Typ @ 1 dB Gain Compression, f = 500 MHz
  Power Gain — 15 dB Typ @ f = 100 MHz
  ITO — 44 dBm Typ @ f = 1000 MHz
  Noise Figure — 8 dB Typ @ f = 500 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- Moisture Resistant, EMI Shielded Package

**1.6 WATT
10–1000 MHz
LINEAR
POWER
AMPLIFIER**



DHP
CASE 389-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	32	Vdc
RF Power Input	P_{in}	23	dBm
Operating Case Temperature Range	T_C	−55 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +85	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 28 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 28 V)	I_{CC}	720	800	880	mA
Power Gain (f = 100 MHz)	Gp	14	15	16	dB
Bandwidth	BW	10	—	1000	MHz
Gain Flatness (P-P) (f = 10–1000 MHz)	—	—	±0.8	±1.5	dB
Input/Output VSWR (f = 40–900 MHz) (f = 10–1000 MHz)	—	— —	— 2:1	2:1 2.5:1	—
Output Power @ 1 dB Gain Compression (f = 500 MHz) (f = 1000 MHz)	$P_{o1\,dB}$	31 30	32 31	— —	dBm
Third Order Intercept Point (f = 500 MHz) (f = 1000 MHz)	ITO	43 42	45 44	— —	dBm
Noise Figure (f = 500 MHz) (f = 1000 MHz)	NF	— —	8 9	9 10	dB

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

DHP10-32-08

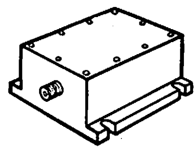
The RF Line

Linear Power Amplifier

. . . developed for medium power requirements in instrumentation, communications equipment and military applications; also cellular radio 900 MHz base stations. These packaged assemblies are in moisture resistant, EMI shielded cases and are matched for use in 50 ohm systems.

- Specified Characteristics at V_{CC} = 28 V, T_C = 25°C:
  - Frequency Range — 10 to 1000 MHz
  - Output Power — 630 mW Typ @ 1 dB Gain Compression, f = 1000 MHz
  - Power Gain — 32 dB Typ @ f = 100 MHz
  - ITO — 42 dBm Typ @ f = 1000 MHz
  - Noise Figure — 7.5 dB Typ @ f = 1000 MHz
- Designed for use in 50 Ohm Systems
- Moisture Resistant, EMI Shielded Package

32 dB
10–1000 MHz
630 mW
LINEAR POWER AMPLIFIER



DHP
CASE 389-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	32	Vdc
RF Power Input	P_{in}	3	dBm
Operating Case Temperature Range	T_C	−55 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +85	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 28 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 28 V)	I_{CC}	560	620	680	mA
Power Gain (f = 100 MHz)	G_P	30	32	34	dB
Bandwidth	BW	10	—	1000	MHz
Gain Flatness (P-P) (f = 10–1000 MHz)	—	—	±1	±1.5	dB
Input/Output VSWR (f = 40–900 MHz) (f = 10–1000 MHz)	—	— —	— 2:1	2:1 2.5:1	—
Output Power @ 1 dB Gain Compression (f = 500 MHz) (f = 1000 MHz)	$P_{o1\ dB}$	28 27	29 28	— —	dBm
Third Order Intercept Point (f = 500 MHz) (f = 1000 MHz)	ITO	41 40	43 42	— —	dBm
Noise Figure (f = 500 MHz) (f = 1000 MHz)	NF	— —	6.5 7.5	8 9	dB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

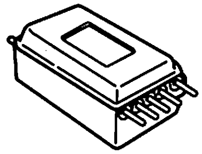
FF124
FF124B

The RF Line
450 MHz CATV Feedforward Amplifiers

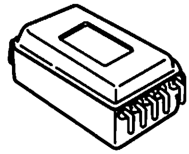
. . . designed for broadband applications requiring low-distortion amplification. Specifically intended for CATV market requirements. Two hybrid amplifiers along with couplers and delay lines are packaged together to provide extremely low distortion products at conventional CATV amplifier output levels.

- Specifically Designed to Provide Improved Performance in 450 MHz CATV Applications
- Distortion Components Reduced more than 20 dB from Conventional CATV Hybrid Amplifiers
- Specified for 60-Channel Performance
- Fully Shielded Metal Package
- Available in Bent Lead Option

24 dB
40–450 MHz
60-CHANNEL
CATV
FEEDFORWARD
AMPLIFIERS



CASE 825-03, STYLE 1
FF124



CASE 825A-02, STYLE 1
FF124B

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

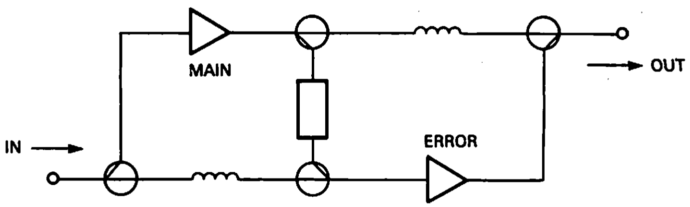
ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, T_C = 60°C, 75 Ω system unless otherwise noted)

Frequency Range	BW	40	—	550	MHz
Power Gain — 50 MHz	Gp	23.4	24	24.6	dB
Slope	S	+0.2	—	+1.4	dB
Gain Flatness	—	—	—	±0.2	dB
Return Loss — Input (f = 40–450 MHz)	IRL	18	—	—	dB
Return Loss — Output (f = 40–450 MHz)	ORL	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +50 dBmV per ch., ch. A, H2, H22)	IMD	—	—	−80	dB
Cross Modulation Distortion (V_{out} = 46 dBmV per ch., ch. 2, 60-channels) (V_{out} = 46 dBmV per ch., ch. 2, ---, H22)	XMD_{60}	 — —	 −80 —	 — −75	dB
Composite Triple Beat (V_{out} = 46 dBmV per ch., ch. 2, 60-channels) (V_{out} = 46 dBmV per ch., ch. 2, ---, H22)	CTB	 — —	 −85 —	 — −79	dB
Noise Figure (f = 50 MHz) (f = 450 MHz)	NF	— —	— —	9 10	dB
DC Current	I_{DC}	—	660	—	mA

PERFORMANCE DERATE versus TEMPERATURE (TYP)

Symbol	Characteristics	Test Conditions	−20 +80°C	−20 +100°C
G	Gain	50 MHz	±0.5 dB	±0.6 dB

CIRCUITRY BLOCK DIAGRAM



PERFORMANCE MEASUREMENT
Motorola test fixture: P/N FF124TF (For straight pins) and P/N FF124BTF (For bent pins) are necessary for accurate measurement.

FF224
FF224B

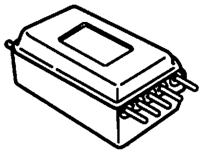
The RF Line

550 MHz CATV Feedforward Amplifiers

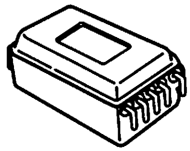
. . . designed for broadband applications requiring low-distortion amplification. Specifically intended for CATV market requirements. Two hybrid amplifiers along with couplers and delay lines are packaged together to provide extremely low distortion products at conventional CATV amplifier output levels.

- Specifically Designed to Provide Improved Performance in 550 MHz CATV Applications
- Distortion Components Reduced more than 20 dB from Conventional CATV Hybrid Amplifiers
- Specified for 77-Channel Performance
- Fully Shielded Metal Package
- Available in Bent Lead Option

**24 dB
40–550 MHz
77-CHANNEL
CATV
FEEDFORWARD
AMPLIFIERS**



CASE 825-03, STYLE 1
FF224



CASE 825A-02, STYLE 1
FF224B

5

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

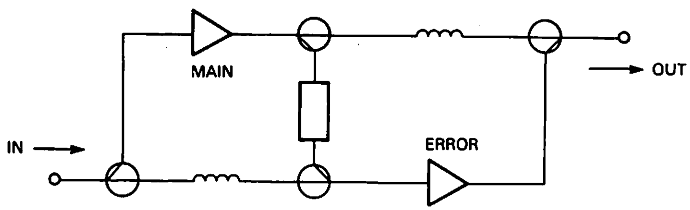
ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, T_C = 60°C, 75 Ω system unless otherwise noted)

Frequency Range	BW	40	—	550	MHz
Power Gain — 50 MHz	Gp	23.4	24	24.6	dB
Slope	S	+0.2	—	+1.8	dB
Gain Flatness	—	—	—	±0.25	dB
Return Loss — Input (f = 40–450 MHz) (f = 450–550 MHz)	IRL	18 16	— —	— —	dB
Return Loss — Output (f = 40–550 MHz)	ORL	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +50 dBmV per ch., ch. A, H2, H22)	IMD	—	—	−80	dB
Cross Modulation Distortion (V_{out} = 44 dBmV per ch., ch. 2, 77-channels) (V_{out} = 44 dBmV per ch., ch. 2, ---, H39)	XMD_{77}	 — —	 −80 —	 — −70	dB
Composite Triple Beat (V_{out} = 44 dBmV per ch., ch. 2, 77-channels) (V_{out} = 44 dBmV per ch., ch. 2, ---, H39)	CTB	 — —	 −85 —	 — −75	dB
Noise Figure (f = 50 MHz) (f = 550 MHz)	NF	— —	— —	9 11	dB
DC Current	I_{DC}	—	660	—	mA

PERFORMANCE DERATE versus TEMPERATURE (TYP)

Symbol	Characteristics	Test Conditions	−20 +80°C	−20 +100°C
G	Gain	50 MHz	±0.5 dB	±0.6 dB

CIRCUITRY BLOCK DIAGRAM



PERFORMANCE MEASUREMENT
Motorola test fixture: P/N FF124TF (For straight pins) and P/N FF124BTF (For bent pins) are necessary for accurate measurement.

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW590

The RF Line

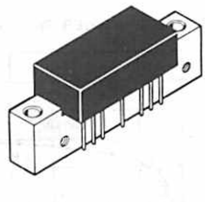
LOW DISTORTION WIDEBAND AMPLIFIER

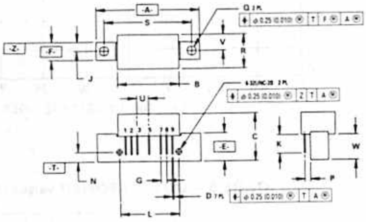
. . . low-noise, high-gain, ultra-linear, thin-film hybrid. Designed for multi-purpose broadband 50 to 100 ohm system applications requiring superior gain and current stability with temperature.

- Supply Voltage = 24 V Nominal
- Broadband Power Gain —
  G_p = 34 dB (Typ) @ f = 10-400 MHz
- Broadband Noise Figure —
  NF = 3.5 dB (Typ) @ f = 300 MHz
- *Ideal* for Low Level Wideband Linear Amplifiers and AM Modulators in VHF/UHF Communications Equipment and RF Instrumentation Applications

10–400 MHz

HIGH GAIN AMPLIFIER





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DC}	28	Vdc
Input Power	P_{in}	5.0	dBm
Operating Case Temperature Range	T_C	-20 to +90	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DC} = 24 Vdc, Z_o = 50 Ω, T_C = 25°C. All characteristics guaranteed over bandwidth listed under "Frequency Range", unless specified otherwise.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	400	MHz
Power Gain	G_p	31.5	34	35.5	dB
Gain Flatness	F	—	—	±1.5	dB
Voltage Standing Wave Ratio, In/Out	VSWR				
(f = 10-300 MHz)		—	1.5:1	—	
(f = 300-400 MHz)		—	2:1	—	
1 dB Compression	P1				mW
(f = 10 MHz)		—	800	—	
(f = 200 MHz)		700	800	—	
(f = 400 MHz)		—	300	—	
Reverse Isolation	P_{RI}	43	50	—	dB
2nd Harmonic (P_{out} = 10 mW)	d_{so}	—	-66	—	dB
Third Order Intercept	I_{TO}	—	43	—	dBm
Peak Envelope Power for -32 dB Distortion	PEP	—	500	—	mW
Noise Figure	NF				dB
(f = 60 MHz)		—	4.0	—	
(f = 300 MHz)		—	3.5	5.5	
DC Voltage	V_{DC}	—	24	28	V
DC Current	I_{DC}	—	300	340	mA

FIGURE 1 – POWER GAIN AND RETURN LOSS versus FREQUENCY

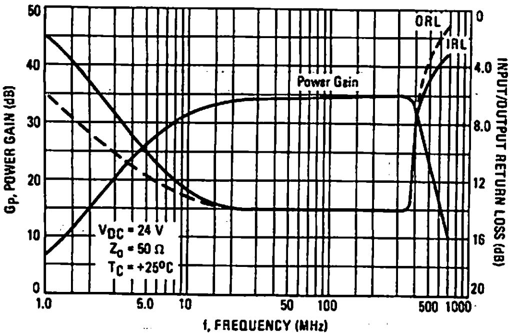


FIGURE 2 – POWER GAIN versus FREQUENCY

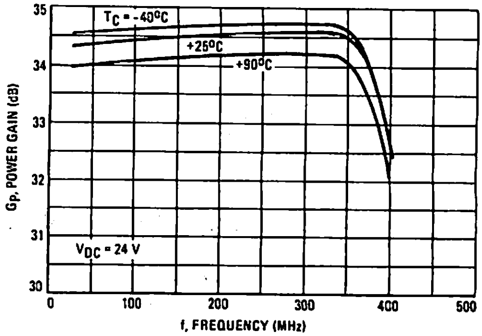


FIGURE 3 – POWER GAIN versus SUPPLY VOLTAGE

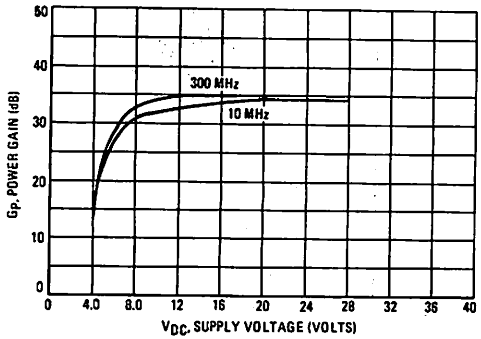


FIGURE 4 – NOISE FIGURE versus SUPPLY VOLTAGE

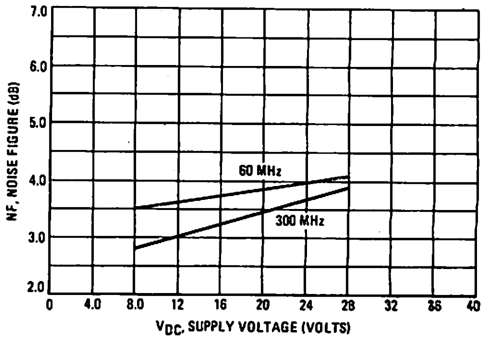


FIGURE 5 – OUTPUT POWER versus INPUT POWER

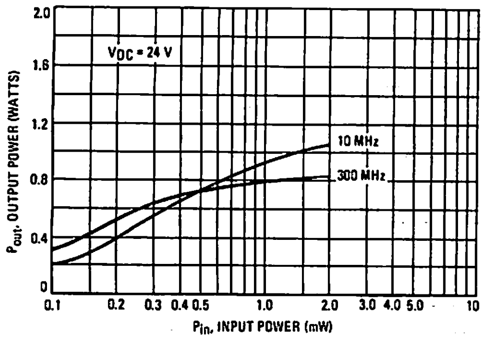


FIGURE 6 — OUTPUT POWER versus INPUT POWER

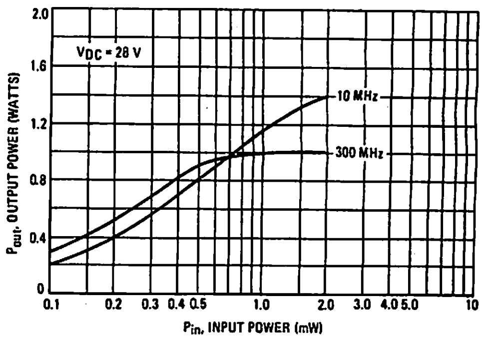


FIGURE 7 — INTERMODULATION DISTORTION — THIRD ORDER versus OUTPUT POWER

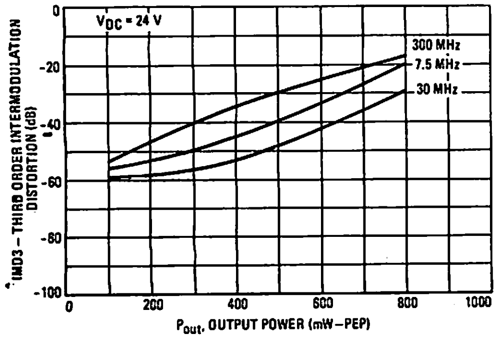


FIGURE 8 — INTERMODULATION DISTORTION — FIFTH ORDER versus OUTPUT POWER

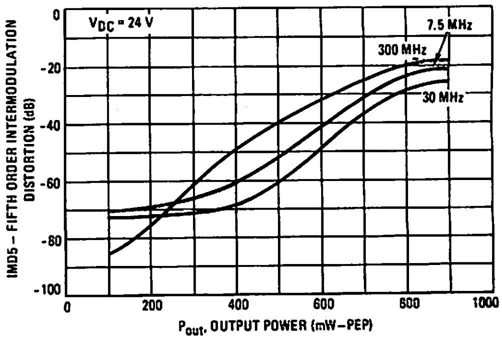


FIGURE 9 — INTERMODULATION DISTORTION — THIRD ORDER versus OUTPUT POWER

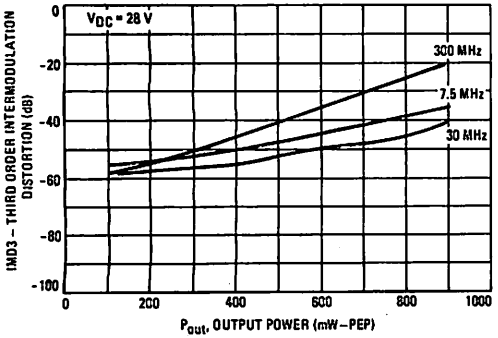


FIGURE 10 — INTERMODULATION DISTORTION — FIFTH ORDER versus OUTPUT POWER

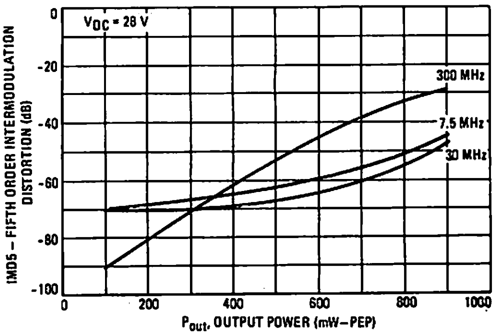


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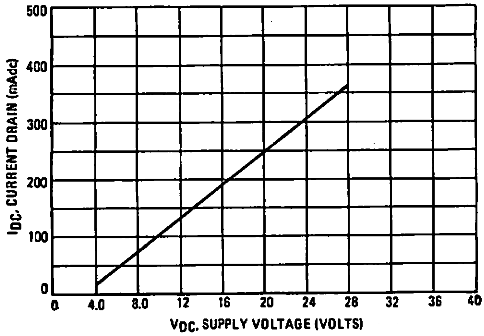
FIGURE 11 — DC CURRENT DRAIN versus SUPPLY VOLTAGE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW591

The RF Line

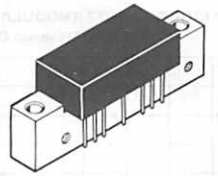
LOW DISTORTION WIDEBAND AMPLIFIER

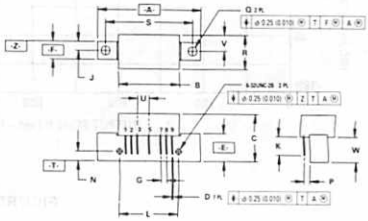
. . . low-noise, high-gain, ultra-linear, thin-film hybrid. Designed for multi-purpose broadband 50 to 100 ohm system applications requiring superior gain and current stability with temperature.

- Supply Voltage = 13.6 V Nominal
- Broadband Power Gain —
  G_p = 36.5 dB (Typ) @ f = 1-250 MHz
- Broadband Noise Figure —
  NF = 3.7 dB (Typ) @ f = 30 MHz
- Ideal for Low Level Wideband Linear Amplifiers and AM Modulators in HF/SSB, VHF Communications Equipment and RF Instrumentation Applications

1.0–250 MHz

HIGH GAIN AMPLIFIER





STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DC}	16	Vdc
Input Power	P_{in}	3.0	dBm
Operating Case Temperature Range	T_C	-20 to +90	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DC} = 13.6 Vdc, Z_o = 50 Ω, T_C = 25°C. All characteristics guaranteed over bandwidth listed under "Frequency Range", unless specified otherwise.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1.0	—	250	MHz
Power Gain	G_p	34.5	36.5	38	dB
Gain Flatness	F	—	—	±1.5	dB
Voltage Standing Wave Ratio, In/Out	VSWR				
(f = 1.0-30 MHz)		—	1.5:1	—	
(f = 30-250 MHz)		—	2:1	—	
1 dB Compression	P1				mW
(f = 30 MHz)		650	800	—	
(f = 100 MHz)		—	700	—	
(f = 250 MHz)		—	250	—	
Peak Envelope Power	PEP				mW
(IMD3 = -30 dB, f = 30 MHz)		700	850	—	
(IMD3 = -30 dB, f = 100 MHz)		—	600	—	
(IMD3 = -30 dB, f = 250 MHz)		—	300	—	
Noise Figure	NF				dB
(f = 30 MHz)		—	3.7	5.0	
(f = 100 MHz)		—	3.7	—	
(f = 250 MHz)		—	4.5	—	
DC Voltage	V_{DC}	—	13.6	16	V
DC Current	I_{DC}	—	300	340	mA

FIGURE 1 — POWER GAIN versus FREQUENCY

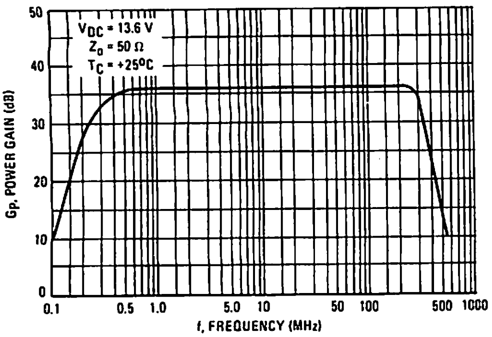


FIGURE 2 — POWER GAIN versus FREQUENCY

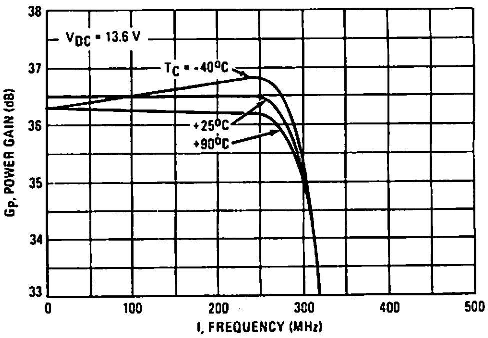


FIGURE 3 — POWER GAIN versus SUPPLY VOLTAGE

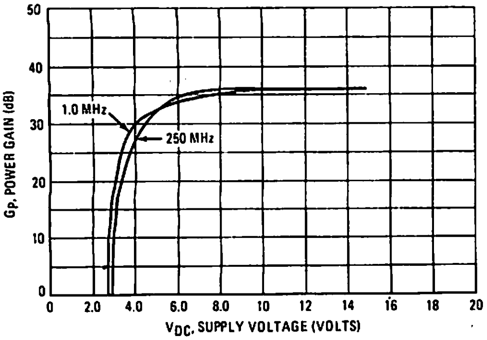


FIGURE 4 — NOISE FIGURE versus SUPPLY VOLTAGE

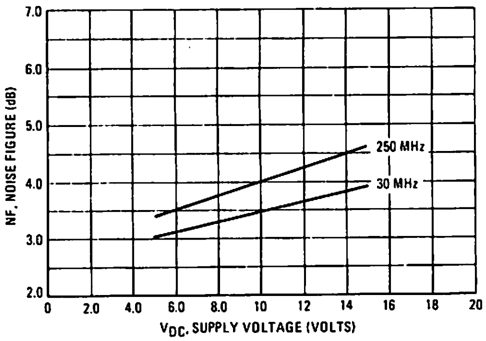


FIGURE 5 — OUTPUT POWER versus INPUT POWER

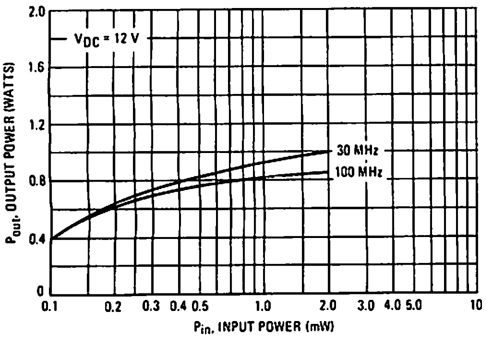


FIGURE 6 — OUTPUT POWER versus INPUT POWER

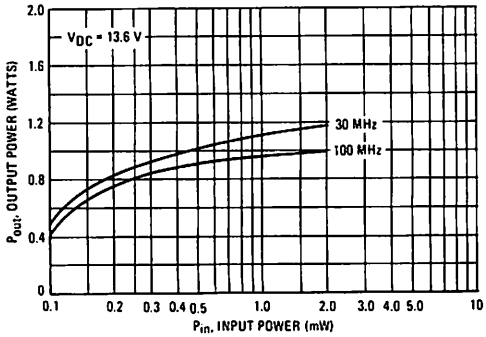


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FIGURE 7 — INTERMODULATION DISTORTION versus OUTPUT POWER

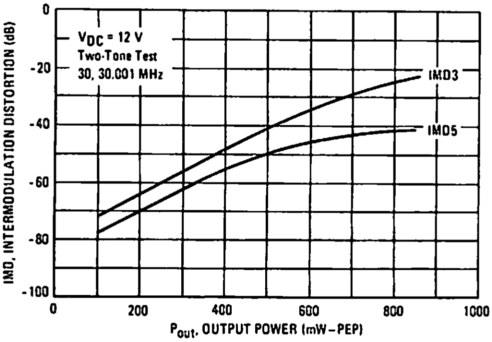


FIGURE 8 — INTERMODULATION DISTORTION versus OUTPUT POWER

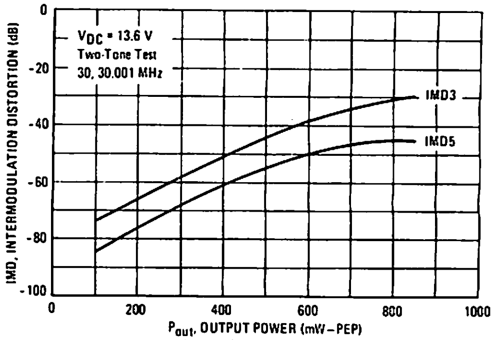
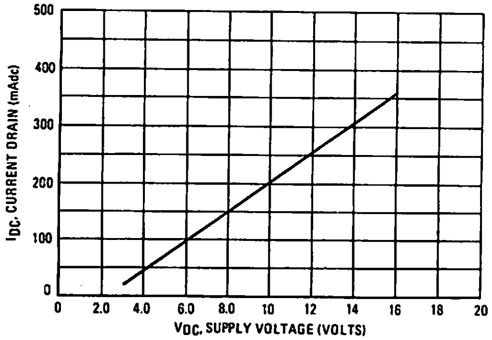


FIGURE 9 — DC CURRENT DRAIN versus SUPPLY VOLTAGE



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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW592

The RF Line

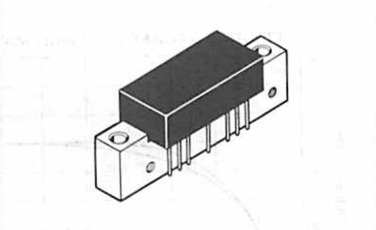
1.0–250 MHz

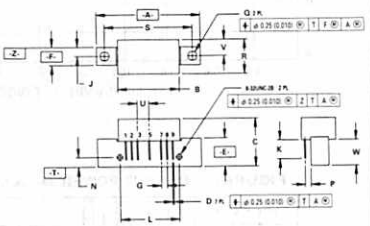
HIGH GAIN AMPLIFIER

LOW DISTORTION WIDEBAND AMPLIFIER

. . . low-noise, high-gain, ultra-linear, thin-film hybrid. Designed for multi-purpose broadband 50 to 100 ohm system applications requiring superior gain and current stability with temperature.

- Supply Voltage = 24 V Nominal
- Broadband Power Gain —
  G_p = 35 dB (Typ) @ f = 1-250 MHz
- Broadband Noise Figure —
  NF = 3.6 dB (Typ) @ f = 30 MHz
- Ideal for Low Level Wideband Linear Amplifiers and AM Modulators in HF/SSB, VHF Communications Equipment and RF Instrumentation Applications





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 1
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DC}	28	Vdc
Input Power	P_{in}	5.0	dBm
Operating Case Temperature Range	T_C	-20 to +90	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DC} = 24 Vdc, Z_o = 50 Ω, T_C = 25°C. All characteristics guaranteed over bandwidth listed under "Frequency Range", unless specified otherwise.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	1.0	—	250	MHz
Power Gain	G_p	33.5	35	36.5	dB
Gain Flatness	F	—	—	±1.0	dB
Voltage Standing Wave Ratio, In/Out	VSWR				
(f = 1.0-30 MHz)		—	1.5:1	—	
(f = 30-250 MHz)		—	2:1	—	
1 dB Compression	P1				mW
(f = 30 MHz)		750	900	—	
(f = 100 MHz)		—	900	—	
(f = 250 MHz)		—	750	—	
Peak Envelope Power	PEP				mW
(IMD3 = -30 dB, f = 30 MHz)		700	850	—	
(IMD3 = -30 dB, f = 100 MHz)		—	850	—	
(IMD3 = -30 dB, f = 250 MHz)		—	600	—	
Noise Figure	NF				dB
(f = 30 MHz)		—	3.6	5.0	
(f = 100 MHz)		—	3.7	—	
(f = 250 MHz)		—	3.9	—	
DC Voltage	V_{DC}	—	24	28	V
DC Current	I_{DC}	—	300	340	mA

FIGURE 1 — POWER GAIN versus FREQUENCY

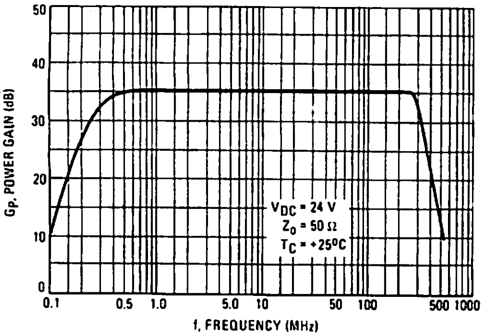


FIGURE 2 — POWER GAIN versus FREQUENCY

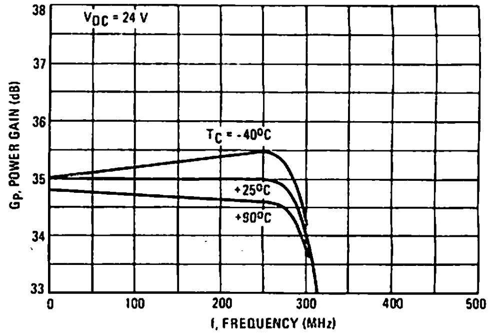


FIGURE 3 — POWER GAIN versus SUPPLY VOLTAGE

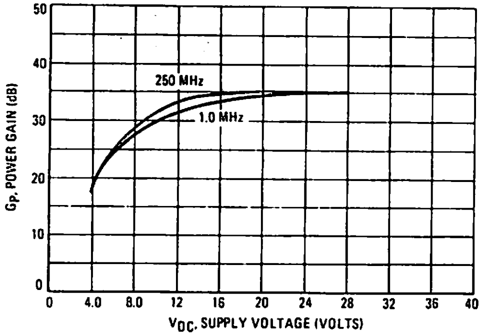


FIGURE 4 — NOISE FIGURE versus SUPPLY VOLTAGE

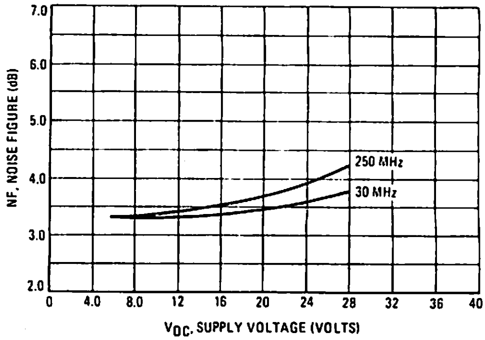


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FIGURE 5 — OUTPUT POWER versus INPUT POWER

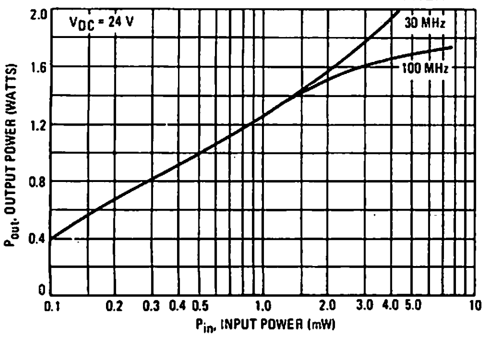


FIGURE 6 — OUTPUT POWER versus INPUT POWER

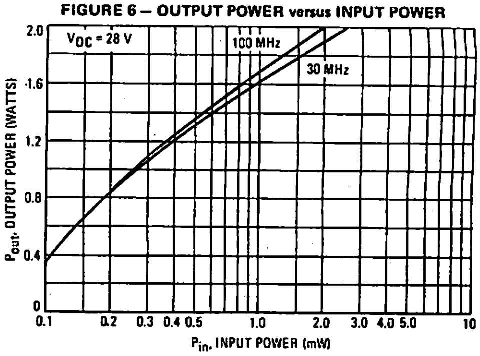


FIGURE 7 — INTERMODULATION DISTORTION versus OUTPUT POWER

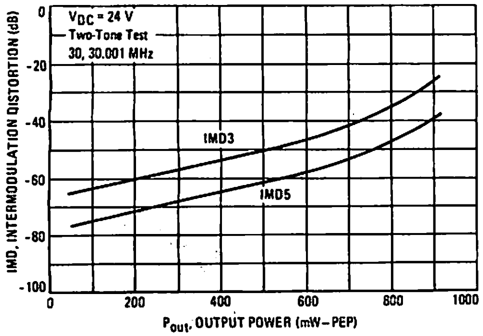


FIGURE 8 — INTERMODULATION DISTORTION versus OUTPUT POWER

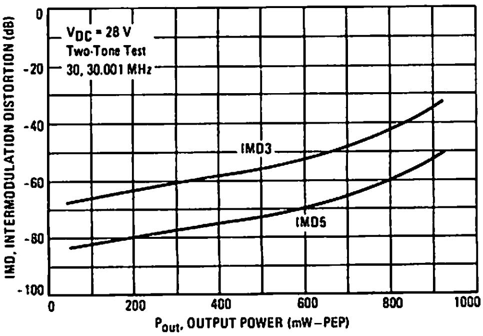
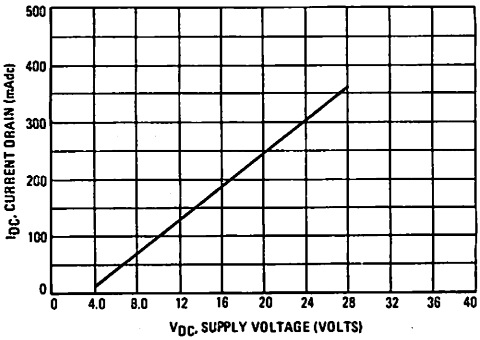


FIGURE 9 — DC CURRENT DRAIN versus SUPPLY VOLTAGE



5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW593

The RF Line

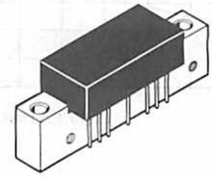
LOW DISTORTION WIDEBAND AMPLIFIER

. . . low-noise, high-gain, ultra-linear, thin-film hybrid. Designed for multi-purpose broadband 50 to 100 ohm system applications requiring superior gain and current stability with temperature.

- Supply Voltage = 13.6 V Nominal
- Broadband Power Gain —
  G_p = 34.5 dB (Typ) @ f = 10-400 MHz
- Broadband Noise Figure —
  NF = 4.0 dB (Typ) @ f = 300 MHz
- Ideal for Low Level Wideband Linear Amplifiers and AM Modulators in VHF/UHF Communications Equipment and RF Instrumentation Applications

10–400 MHz

HIGH GAIN AMPLIFIER

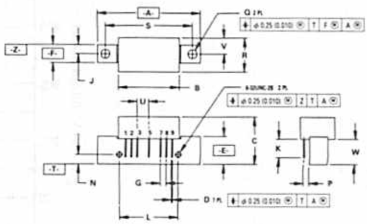


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DC}	16	Vdc
Input Power	P_{in}	3.0	dBm
Operating Case Temperature Range	T_C	-20 to +90	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DC} = 13.6 Vdc, Z_o = 50 Ω, T_C = 25°C. All characteristics guaranteed over bandwidth listed under "Frequency Range", unless specified otherwise.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	–	400	MHz
Power Gain	G_p	33	34.5	36	dB
Gain Flatness	F	–	–	±1.0	dB
Voltage Standing Wave Ratio, In/Out	VSWR				
(f = 10-300 MHz)		–	1.5:1	–	
(f = 300-400 MHz)		–	2:1	–	
1 dB Compression	P1				mW
(f = 10 MHz)		–	600	–	
(f = 200 MHz)		500	600	–	
(f = 400 MHz)		–	200	–	
Reverse Isolation	P_{RI}	45	50	–	dB
2nd Harmonic (P_{out} = 10 mW)	d_{so}	–	-55	–	dB
Third Order Intercept	I_{TO}	–	38	–	dBm
Peak Envelope Power for -32 dB Distortion	PEP	–	300	–	mW
Noise Figure	NF				dB
(f = 60 MHz)		–	3.7	–	
(f = 300 MHz)		–	4.0	5.5	
DC Voltage	V_{DC}	–	13.6	16	V
DC Current	I_{DC}	–	300	340	mA



STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

FIGURE 1 – POWER GAIN AND RETURN LOSS versus FREQUENCY

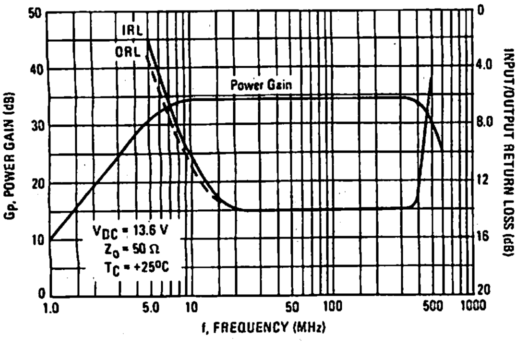


FIGURE 2 – POWER GAIN versus FREQUENCY

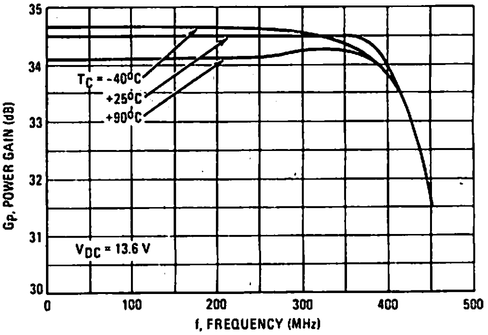


FIGURE 3 – POWER GAIN versus SUPPLY VOLTAGE

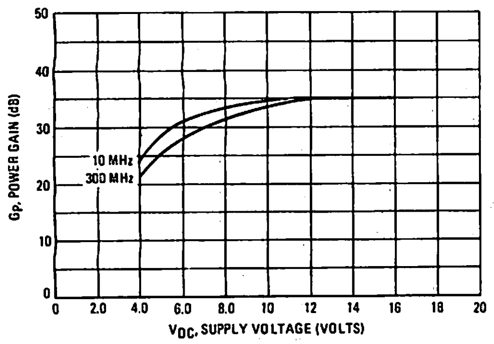


FIGURE 4 – NOISE FIGURE versus SUPPLY VOLTAGE

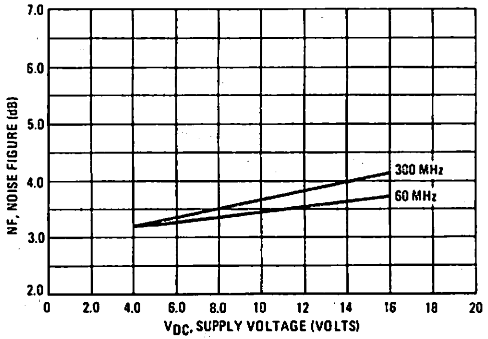


FIGURE 5 – OUTPUT POWER versus INPUT POWER

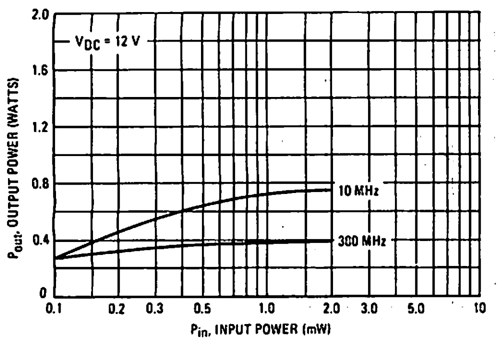


FIGURE 6 – OUTPUT POWER versus INPUT POWER

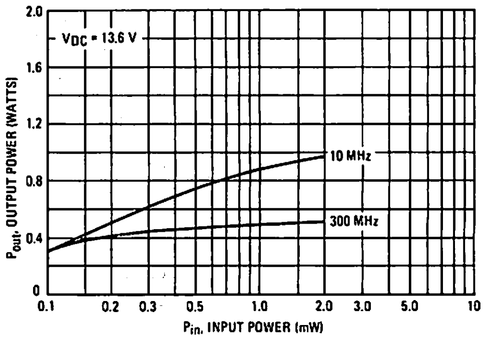


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FIGURE 7 — INTERMODULATION DISTORTION — THIRD ORDER versus OUTPUT POWER

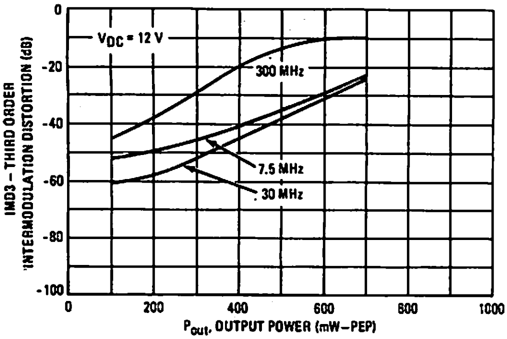


FIGURE 8 — INTERMODULATION DISTORTION — FIFTH ORDER versus OUTPUT POWER

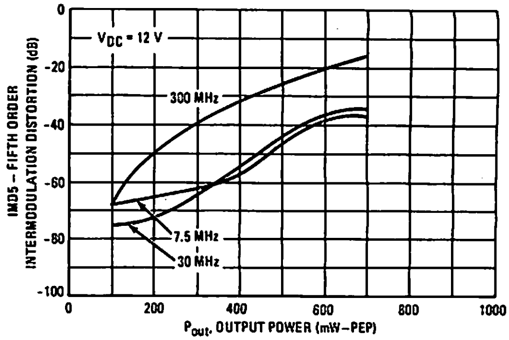


FIGURE 9 — INTERMODULATION DISTORTION — THIRD ORDER versus OUTPUT POWER

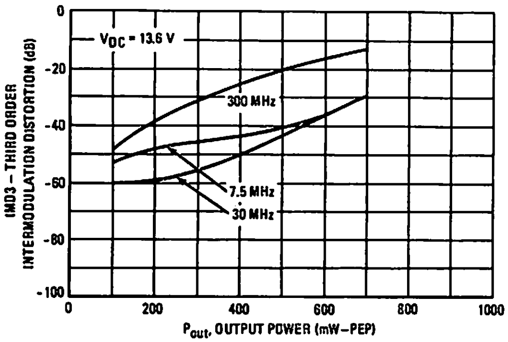


FIGURE 10 — INTERMODULATION DISTORTION — FIFTH ORDER versus OUTPUT POWER

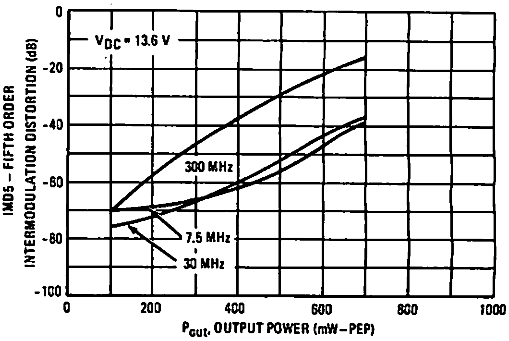
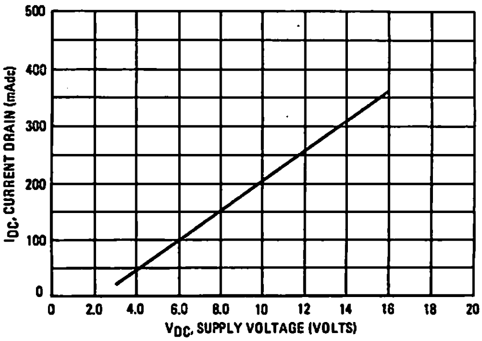


FIGURE 11 — DC CURRENT DRAIN versus SUPPLY VOLTAGE



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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

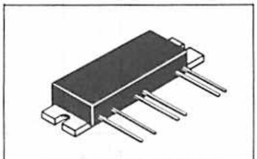
MHW607 Series

The RF Line
VHF Power Amplifiers

. . . designed for 7.5 volt VHF power amplifier applications in industrial and commercial equipment primarily hand portable radios.

- MHW607-1: 136–154 MHz
- MHW607-2: 146–174 MHz
- Specified 7.5 Volt Characteristics:
  - — RF Input Power = 1.0 mW (0 dBm)
  - — RF Output Power = 7.0 Watts
  - — Minimum Gain ($V_{Control}$ = 7.0 V) = 38.5 dB
  - — Harmonics = −40 dBc Max @ 2.0 f_o
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability

7.0 W — 136 to 174 MHz
VHF POWER AMPLIFIERS



CASE 301K-02, STYLE 2

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 2, 4, 5)	$V_{s1,2,3}$	9.0	Vdc
DC Control Voltage (Pin 3)	V_{Cont}	9.0	Vdc
RF Input Power	P_{in}	5.0	mW
RF Output Power ($V_{s1} = V_{s2} = V_{s3}$ = 9.0 V)	P_{out}	10	W
Operating Case Temperature Range	T_C	−30 to +100	°C
Storage Temperature Range	T_{stg}	−30 to +100	°C

ELECTRICAL CHARACTERISTICS $V_{s1} = V_{s2} = V_{s3}$ = 7.5 Vdc, (Pins 2, 4, 5), T_C = 25°C, 50 Ω System

Characteristic	Symbol	Min	Max	Unit
Frequency Range MHW607-1 MHW607-2	—	136 146	154 174	MHz
Control Voltage (P_{out} = 7.0 W, P_{in} = 1.0 mW)(1)	V_{Cont}	0	7.0	Vdc
Quiescent Current ($V_{s1} = V_{s2} = V_{s3}$ = 7.5 Vdc, V_{Cont} = 7.0 Vdc)	$I_{s1(q)} + I_{s2(q)}$	—	160	mA
Power Gain (P_{out} = 7.0 W, V_{Cont} = 7.0 Vdc)	G_p	38.5	—	dB
Efficiency (P_{out} = 7.0 W, P_{in} = 1.0 mW)(1)	η	40	—	%
Harmonics (P_{out} = 7.0 W)(1) 2 f_o (P_{in} = 1.0 mW) 3 f_o	—	— —	−40 −45	dBc
Input VSWR (P_{out} = 7.0 W, P_{in} = 1.0 mW), 50 Ω Ref. (1)	—	—	2.0:1	—
Load Mismatch ($V_{s1} = V_{s2} = V_{s3}$ = 9.0 Vdc) VSWR = 20:1, P_{out} = 10 W, P_{in} = 5.0 mW)(1)		No Degradation in Power Output		
Stability (P_{in} = 1.0–3.0 mW, $V_{s1} = V_{s2} = V_{s3}$ = 6.0–9.0 Vdc) P_{out} between 1.0 W and 10 W(1) Load VSWR = 8:1		All spurious outputs more than 60 dB below desired signal		

(1) Adjust V_{Cont} for specified P_{out}.

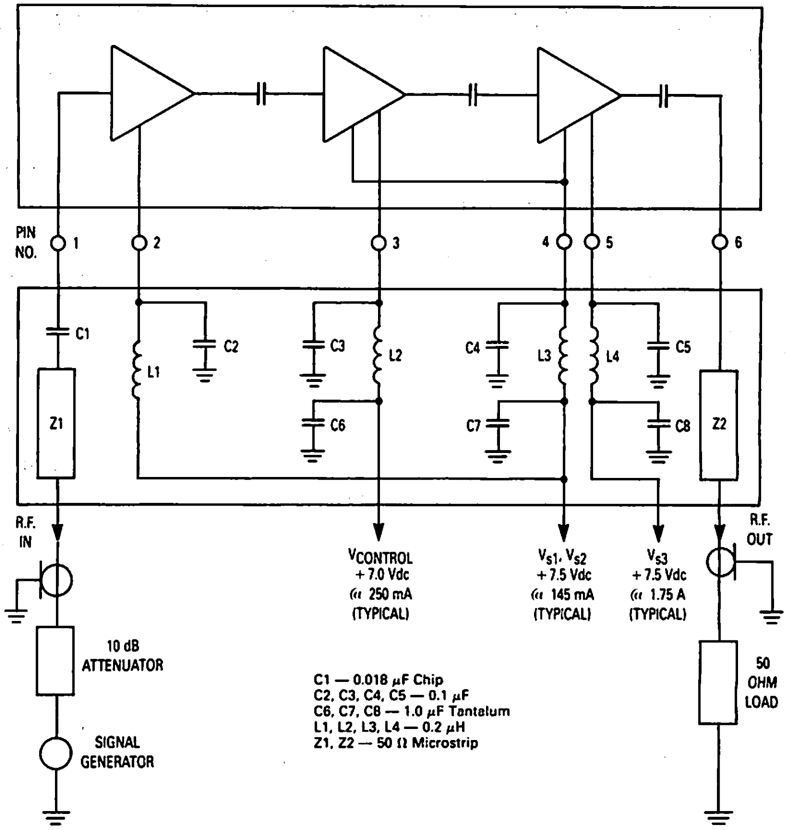


Figure 1. Power Module Test System Block Diagram

TYPICAL CHARACTERISTICS

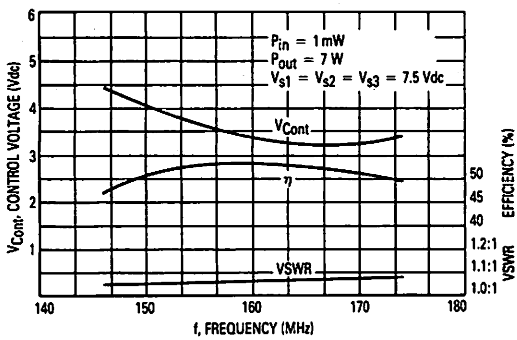


Figure 2. Control Voltage, Efficiency and VSWR versus Frequency

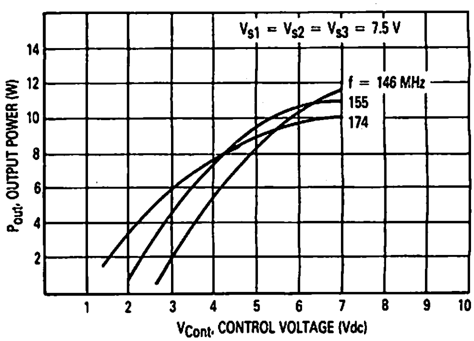


Figure 3. Output Power versus Control Voltage

TYPICAL CHARACTERISTICS

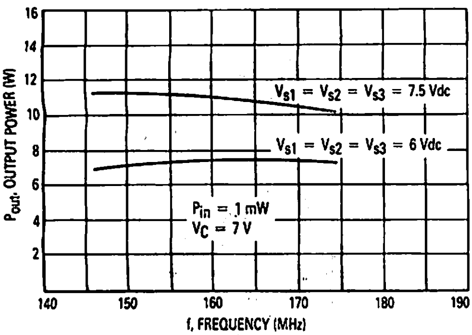


Figure 4. Output Power versus Frequency

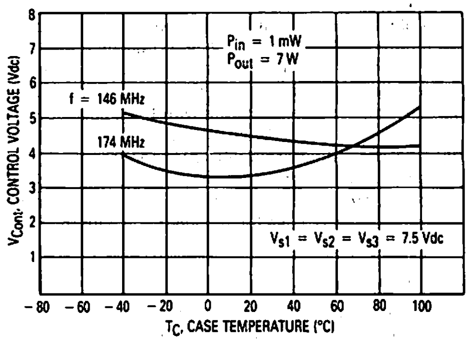


Figure 5. Control Voltage versus Case Temperature

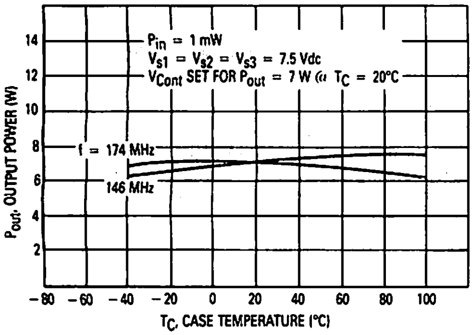


Figure 6. Output Power versus Case Temperature

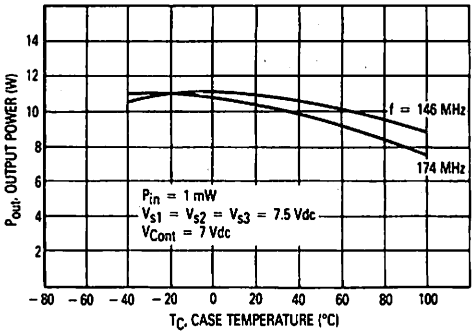


Figure 7. Output Power versus Case Temperature at Maximum Control Voltage

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APPLICATIONS INFORMATION

NOMINAL OPERATION

All electrical specifications are based on the nominal conditions of $V_{S1} = V_{S2} = V_{S3} = 7.5$ Vdc (Pins 2, 4, 5) and P_{out} equal to 7.0 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100°C case operating temperature is 165°C. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use have been made with the factory representative.

GAIN CONTROL

The module output should be limited to 7.0 watts. The preferred method of power output control is to fix $V_{S1} = V_{S2} = V_{S3} = 7.5$ Vdc (Pins 2, 4, 5), P_{in} (Pin 1) at 1.0 mW, and vary V_{Cont} (Pin 3) voltage.

DECOUPLING

Due to the high gain of the three stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3, 4 and 5 are internally bypassed with a 0.018 μF chip capacitor which is effective for frequencies from 5.0 MHz through 174 MHz. For bypassing frequencies below 5.0 MHz, networks equivalent to that shown in Figure 1 are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.

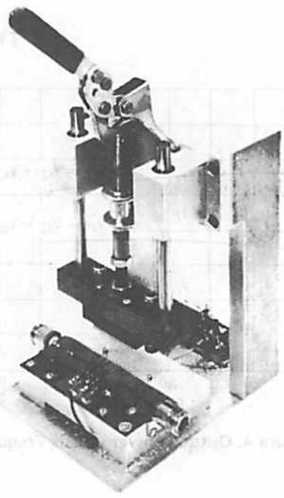

Figure 8. Test Fixture Assembly

LOAD MISMATCH

During final test, each module is load mismatch tested in a fixture having the identical decoupling networks described in Figure 1. Electrical conditions are $V_{S1} = V_{S2} = V_{S3}$ equal to 9.0 Vdc, VSWR equal to 20:1, and output power equal to 8.0 watts.

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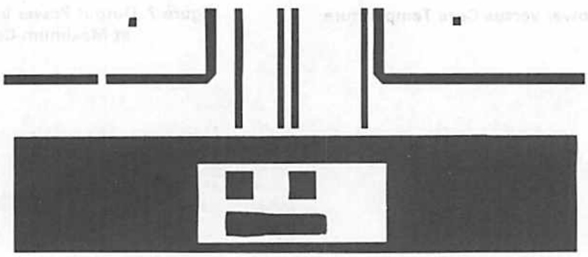


Note: The Printed Circuit Board shown is 75% of the original.

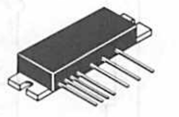
Figure 9. Photomaster For Test Fixture

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

The RF Line
UHF Power Amplifier

MHW703

2.3 W — 450 to 460 MHz
UHF POWER AMPLIFIER



CASE 301J-02, STYLE 2

. . . designed for 7.5 Volt UHF power amplifier applications in industrial and commercial equipment primarily hand portable radios.

- MHW703 450–460 MHz
- Specified 7.5 Volt Characteristics
  - RF Input Power = 2.0 mW (3.0 dBm)
  - RF Output Power = 2.3 Watts
  - Minimum Gain ($V_{Control}$ = 5.8 V) = 30.6 dB
  - Harmonics = −40 dBc Max @ 2 f_o
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pin 2)	V_{s1}	5.7	Vdc
DC Supply Voltage (Pins 4,5,6)	$V_{s2,3,4}$	9.0	Vdc
DC Control Voltage (Pin 3)	V_{Cont}	5.8	Vdc
RF Input Power	P_{in}	4.0	mW
RF Output Power (V_{s1} = 5.7 Vdc, V_{s2} = V_{s3} = V_{s4} = 9.0 Vdc)	P_{out}	3.0	W
Operating Case Temperature Range	T_C	−25 to +100	°C
Storage Temperature Range	T_{stg}	−25 to +100	°C

ELECTRICAL CHARACTERISTICS V_{s1} = 5.6 Vdc, (Pin 2), V_{s2} = V_{s3} = V_{s4} = 7.2 Vdc, (Pins 4,5,6), T_C = 25°C, 50 Ω System

Characteristic	Symbol	Min	Max	Unit
Frequency Range MHW703	—	450	460	MHz
Control Voltage (P_{out} = 2.3 W, P_{in} = 2.0 mW)(1)	V_{Cont}	0	5.8	Vdc
Leakage Current (V_{s1} = V_{s2} = V_{Cont} = 0, V_{s3} = V_{s4} = 9.0 Vdc, P_{in} = 0 mW)		—	0.2	mA
Power Gain (P_{out} = 2.3 W, V_{Cont} = 5.8 Vdc)	G_p	30.6	—	dB
Efficiency (P_{out} = 2.3 W, P_{in} = 2.0 mW)(1)	η	38	—	%
Harmonics (P_{out} = 2.3 W(1) 2 f_o (P_{in} = 2.0 mW)	—	—	−40	dBc
Input VSWR (P_{out} = 2.3 W, P_{in} = 2.0 mW), 50 Ω Ref.(1)	—	—	2.0:1	—
Control Current (V_{s1} = 5.7 Vdc, V_{s2} = V_{s3} = V_{s4} = 7.2 Vdc, P_{in} = 2.0 mW)(1)	—	—	65	mA
Load Mismatch (V_{s1} = 5.6 Vdc, V_{s2} = V_{s3} = V_{s4} = 9.0 Vdc) VSWR = ∞, P_{out} = 2.3 W, P_{in} = 3.0 mW(1)		No Degradation in Power Output		
Stability (P_{in} = 1.0–3.0 mW, V_{s1} = 5.0 Vdc, V_{s2} = V_{s3} = V_{s4} = 6.0–9.0 Vdc) P_{out} between 2.0 mW and 2.3 W(1) Load VSWR = 6:1, All Phase Angles		All spurious outputs more than 60 dB below desired signal		
Regulated Supply First Stage Quiescent Current (V_{s1} = 5.6 V)	$I_{SI(q)}$	—	40	mA

(1) Adjust V_{Cont} for specified P_{out}.

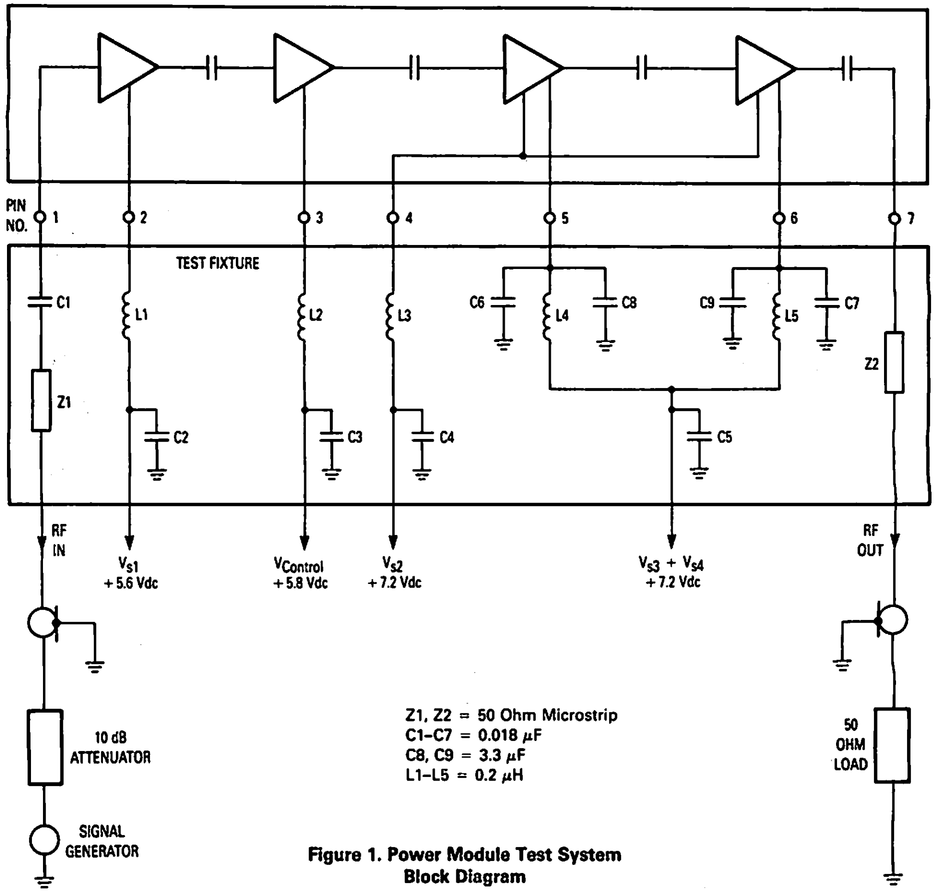


Figure 1. Power Module Test System Block Diagram

TYPICAL CHARACTERISTICS

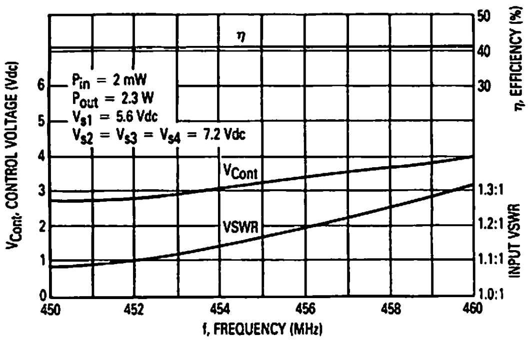


Figure 2. Control Voltage, Efficiency and VSWR versus Frequency

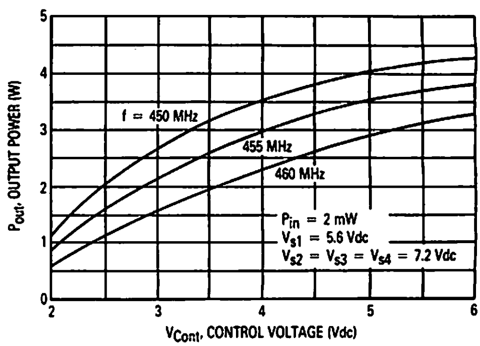


Figure 3. Output Power versus Control Voltage

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TYPICAL CHARACTERISTICS

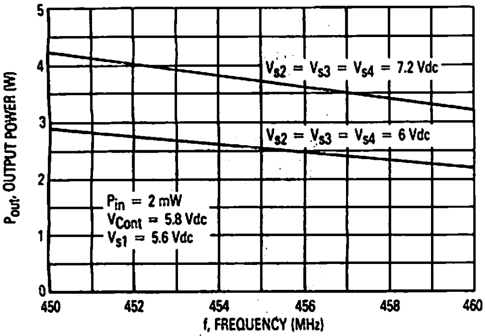

Figure 4. Output Power versus Frequency

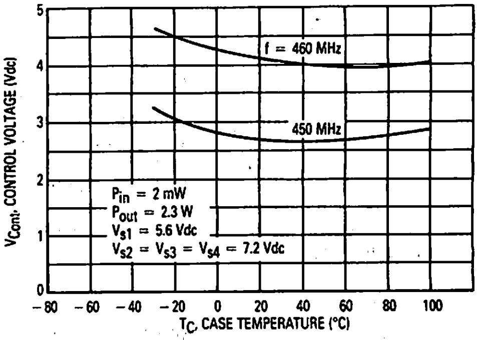

Figure 5. Control Voltage versus Case Temperature

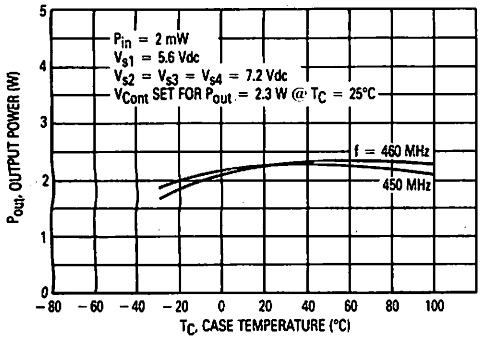

Figure 6. Output Power versus Case Temperature

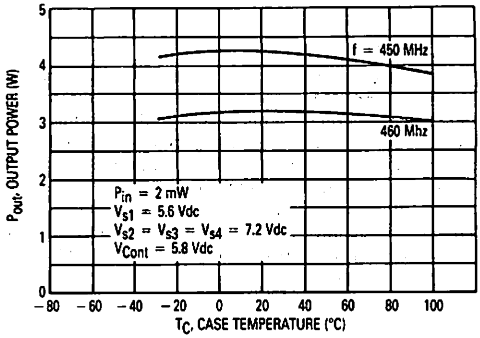

Figure 7. Output Power versus Case Temperature at Maximum Control Voltage

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APPLICATIONS INFORMATION

NOMINAL OPERATION

All electrical specifications are based on the nominal conditions of V_{s1} = 5.6 Vdc (Pin 2), $V_{s2} = V_{s3} = V_{s4}$ = 7.2 Vdc (Pins 4, 5, 6) and P_{out} equal to 2.3 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use have been made with the factory representative.

GAIN CONTROL

The module output should be limited to 2.3 watts. The preferred method of power output control is to fix V_{s1} = 5.6 Vdc (Pin 2), $V_{s2} = V_{s3} = V_{s4}$ = 7.2 Vdc (Pins 4, 5, 6), P_{in} (Pin 1) at 2.0 mW, and vary V_{cont} (Pin 3) voltage.

DECOUPLING

Due to the high gain of the four stages and the module size limitations, external decoupling networks require careful consideration. Pins 2, 3, 5 and 6 are internally bypassed with a 0.018 μF chip capacitor which is effective for frequencies from 5.0 MHz through 940 MHz. For bypassing frequencies below 5.0 MHz, networks equivalent to that shown in Figure 1 are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.

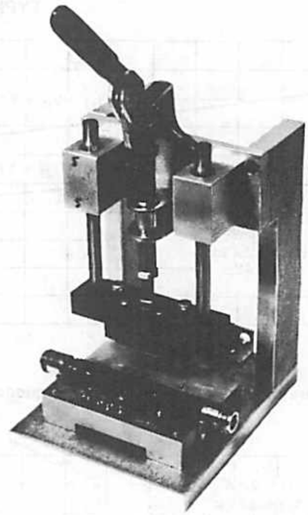


Figure 8. Test Fixture Assembly

LOAD MISMATCH

During final test, each module is load mismatch tested in a fixture having the identical decoupling networks described in Figure 1. Electrical conditions are V_{s1} = 5.6 Vdc, $V_{s2} = V_{s3} = V_{s4}$ equal to 9.0 Vdc, VSWR equal to ∞, and output power equal to 2.3 watts.

5

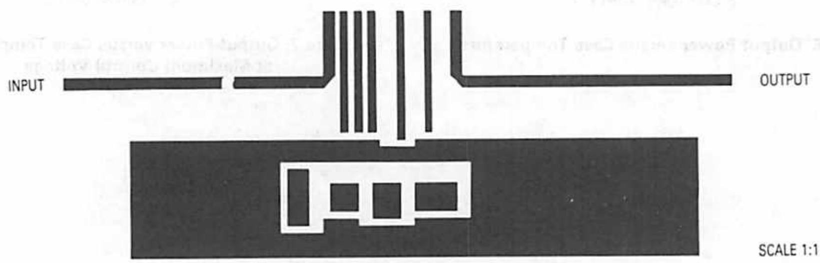


Figure 9. Photomaster For Test Fixture

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

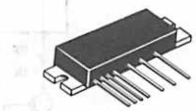
MHW707 Series

The RF Line
UHF Power Amplifiers

. . . designed for 7.5 Volt UHF power amplifier applications in industrial and commercial equipment primarily hand portable radios.

- MHW707-1 403–440 MHz
- MHW707-2 440–470 MHz
- Specified 7.5 Volt Characteristics
  - RF Input Power = 1.0 mW (0 dBm)
  - RF Output Power = 7.0 Watts
  - Minimum Gain ($V_{Control}$ = 7.0 V) = 38.5 dB
  - Harmonics = −40 dBc Max @ 2 f_o
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability

7.0 W — 403 to 470 MHz
UHF POWER
AMPLIFIERS



CASE 301J-02, STYLE 1

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 2,4,5,6)	$V_{s1,2,3,4}$	9.0	Vdc
DC Control Voltage (Pin 3)	V_{Cont}	7.0	Vdc
RF Input Power	P_{in}	3.0	mW
RF Output Power (V_{s1} = V_{s2} = V_{s3} = V_{s4} = 9.0 Vdc)	P_{out}	9.0	W
Operating Case Temperature Range	T_C	−30 to +80	°C
Storage Temperature Range	T_{stg}	−30 to +80	°C

ELECTRICAL CHARACTERISTICS V_{s1} = V_{s2} = V_{s3} = V_{s4} = 7.5 Vdc, (Pins 2,4,5,6), T_C = 25°C, 50 Ω System

Characteristic	Symbol	Min	Max	Unit
Frequency Range MHW707-1 MHW707-2	—	403 440	440 470	MHz
Control Voltage (P_{out} = 7.0 W, P_{in} = 1.0 mW)(1)	V_{Cont}	0	7.0	Vdc
Quiescent Current (V_{s1} = V_{s2} = V_{s3} = V_{s4} = 7.5 Vdc, P_{in} = 0 mW, V_{Cont} = 0 Vdc)		—	150	mA
Power Gain (P_{out} = 7.0 W, V_{Cont} = 7.0 Vdc)	G_p	38.5	—	dB
Efficiency (P_{out} = 7.0 W, P_{in} = 1.0 mW)(1)	η	40	—	%
Harmonics (P_{out} = 7.0 W)(1) 2 f_o (P_{in} = 1.0 mW)	—	—	−40	dBc
Input VSWR (P_{out} = 7.0 W, P_{in} = 1.0 mW), 50 Ω Ref.(1)	—	—	2.0:1	—
Control Current (V_{s1} = V_{s2} = V_{s3} = V_{s4} = 7.5 Vdc, P_{in} = 1.0 mW)(1)	—	—	95	mA
Load Mismatch (V_{s1} = V_{s2} = V_{s3} = V_{s4} = 9.0 Vdc) VSWR = 10:1, P_{out} = 9.0 W, P_{in} = 3.0 mW(1)		No Degradation in Power Output		
Stability (P_{in} = 1.0–3.0 mW, V_{s1} = V_{s2} = V_{s3} = V_{s4} = 6.0–9.0 Vdc) P_{out} between 1.0 W and 9.0 W(1) Load VSWR = 8:1, All Phase Angles		All spurious outputs more than 60 dB below desired signal		

(1) Adjust V_{Cont} for specified P_{out}.

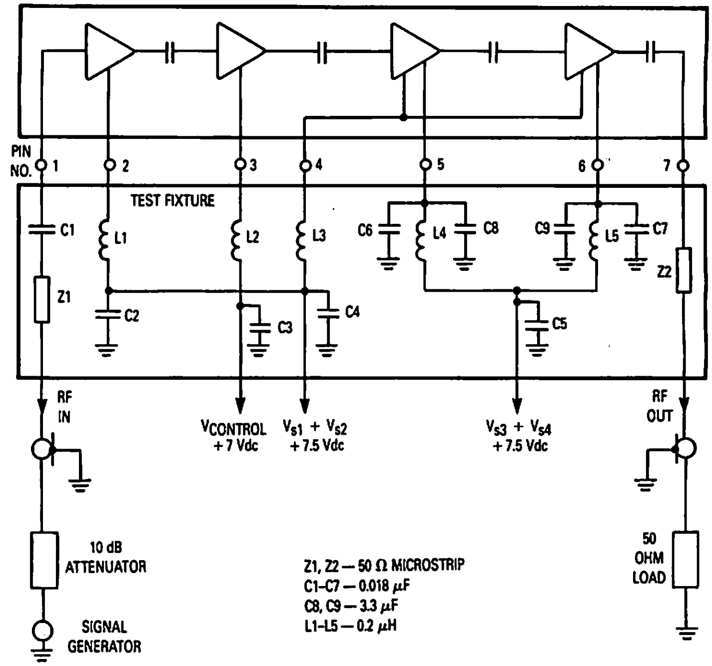


Figure 1. Power Module Test System Block Diagram

TYPICAL CHARACTERISTICS (MHW707-1)

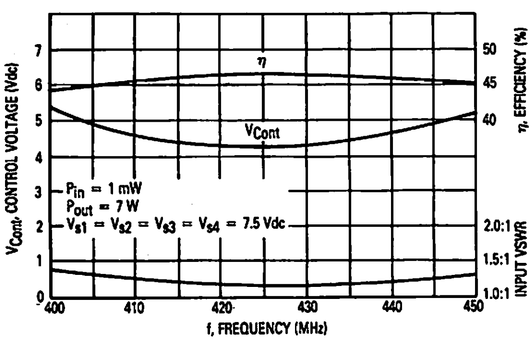


Figure 2. Control Voltage, Efficiency and VSWR versus Frequency

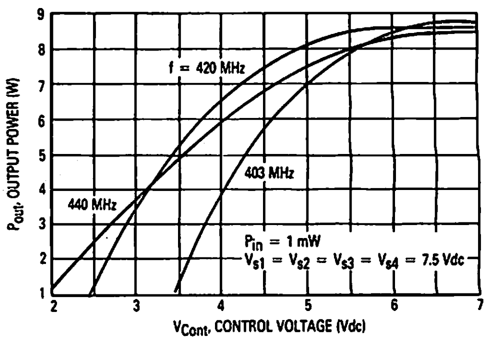


Figure 3. Output Power versus Control Voltage

TYPICAL CHARACTERISTICS
(MHW707-1)

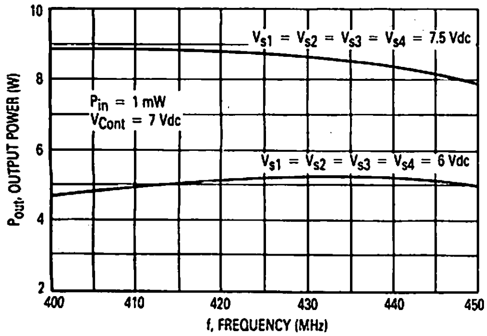


Figure 4. Output Power versus Frequency

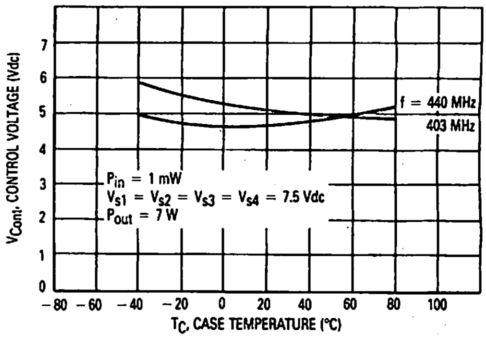


Figure 5. Control Voltage versus Case Temperature

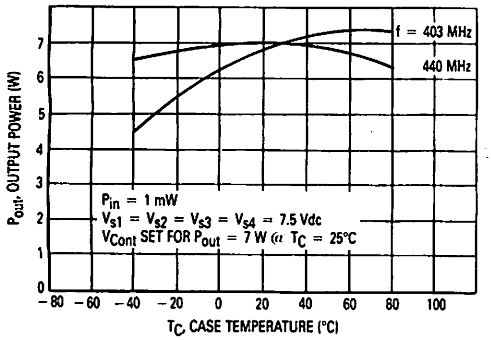


Figure 6. Output Power versus Case Temperature

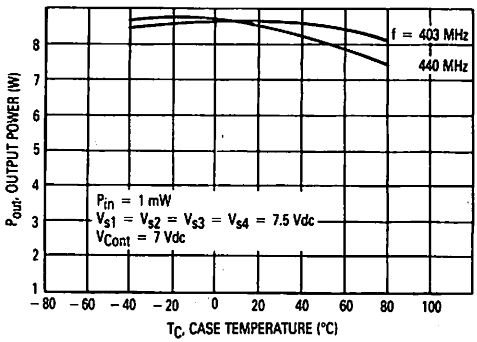


Figure 7. Output Power versus Case Temperature at Maximum Control Voltage

TYPICAL CHARACTERISTICS
(MHW707-2)

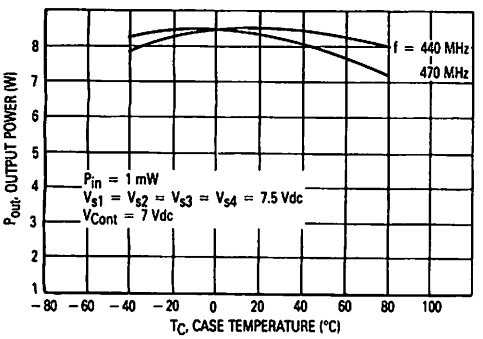


Figure 8. Output Power versus Case Temperature at Maximum Control Voltage

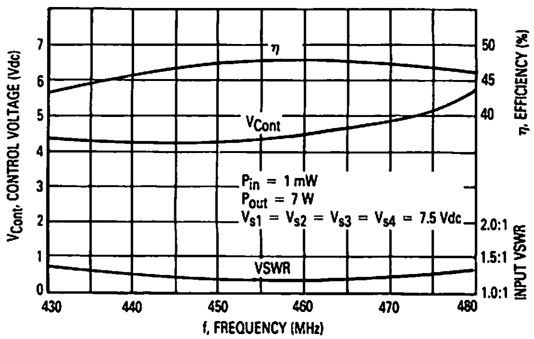


Figure 9. Control Voltage, Efficiency and VSWR versus Frequency

5

TYPICAL CHARACTERISTICS
(MHW707-2)

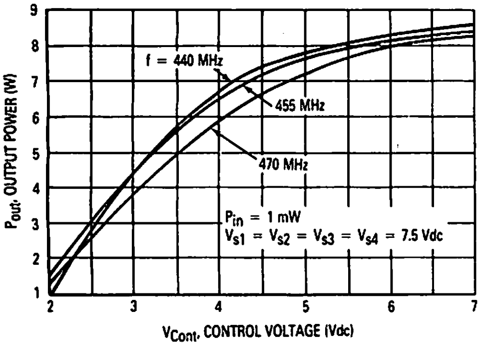


Figure 10. Output Power versus Control Voltage

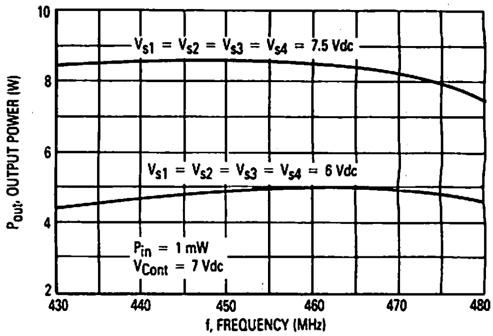


Figure 11. Output Power versus Frequency

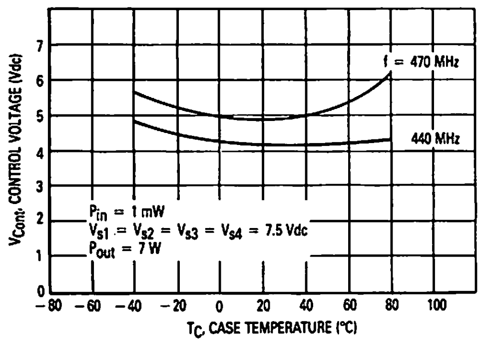


Figure 12. Control Voltage versus Case Temperature

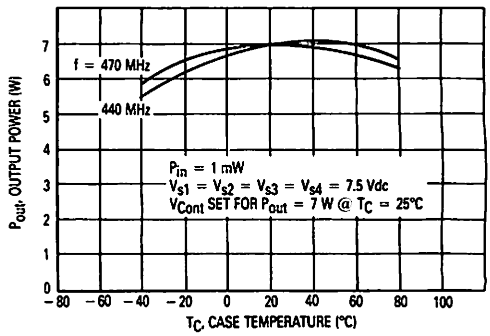


Figure 13. Output Power versus Case Temperature

5

APPLICATIONS INFORMATION

NOMINAL OPERATION

All electrical specifications are based on the nominal conditions of $V_{S1} = V_{S2} = V_{S3} = V_{S4}$ = 7.5 Vdc (Pins 2, 4, 5, 6) and P_{out} equal to 7.0 watts. With these conditions, maximum current density on any device is 1.5 x 10^5 A/cm^2. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use have been made with the factory representative.

GAIN CONTROL

The module output should be limited to 7.0 watts. The preferred method of power output control is to fix $V_{S1} = V_{S2} = V_{S3} = V_{S4}$ = 7.5 Vdc (Pins 2, 4, 5, 6), P_{in} (Pin 1) at 1.0 mW, and vary V_{cont} (Pin 3) voltage.

DECOUPLING

Due to the high gain of the four stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3, 5 and 6 are internally bypassed with a 0.018 μF chip capacitor which is effective for frequencies from 5.0 MHz through 940 MHz. For bypassing frequencies below 5.0 MHz, networks equivalent to that shown in Figure 1 are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.

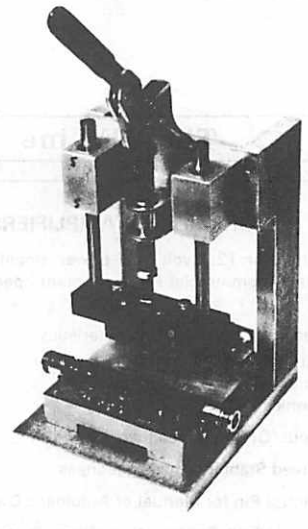
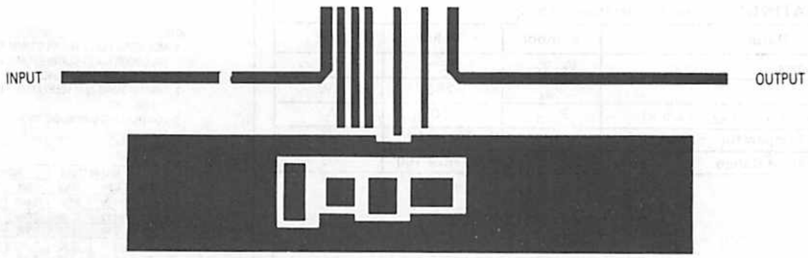


Figure 14. Test Fixture Assembly

LOAD MISMATCH

During final test, each module is load mismatch tested in a fixture having the identical decoupling networks described in Figure 1. Electrical conditions are $V_{S1} = V_{S2}$ $V_{S3} = V_{S4}$ equal to 9.0 Vdc, VSWR equal to 20:1, and output power equal to 8.0 watts.

5



Note: The Printed Circuit Board shown is 75% of the original.

Figure 15. Photomaster For Test Fixture

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW709-1
MHW709-2
MHW709-3

The RF Line

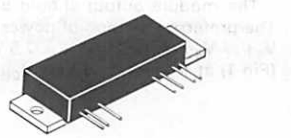
UHF POWER AMPLIFIERS

. . . designed for 12.5 volt UHF power amplifier applications in industrial and commercial FM equipment operating from 400 to 512 MHz.

- Specified 12.5 Volt, UHF Characteristics —
  Output Power = 7.5 Watts
  Minimum Gain = 18.8 dB
  Harmonics = 40 dB
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Gain Control Pin for Manual or Automatic Output Level Control
- Thin-Film Hybrid Construction Gives Consistent Performance and Reliability

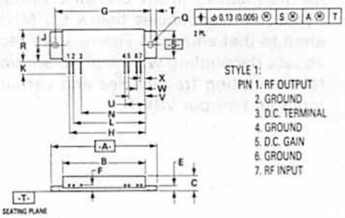
7.5 W — 400-512 MHz

RF POWER AMPLIFIERS



MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_S, V_{SC}	15.5	Vdc
RF Input Power	P_{in}	250	mW
RF Output Power(@ $V_S = V_{SC} = 12.5$ V)	P_{out}	10	W
Operating Case Temperature Range	T_C	-30 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C



STYLE 1:
PIN 1. RF OUTPUT
2. GROUND
3. D.C. TERMINAL
4. GROUND
5. D.C. GAIN
6. GROUND
7. RF INPUT

NOTES:
1. MOUNTING HOLES WITHIN 0.13MM (0.005) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH.

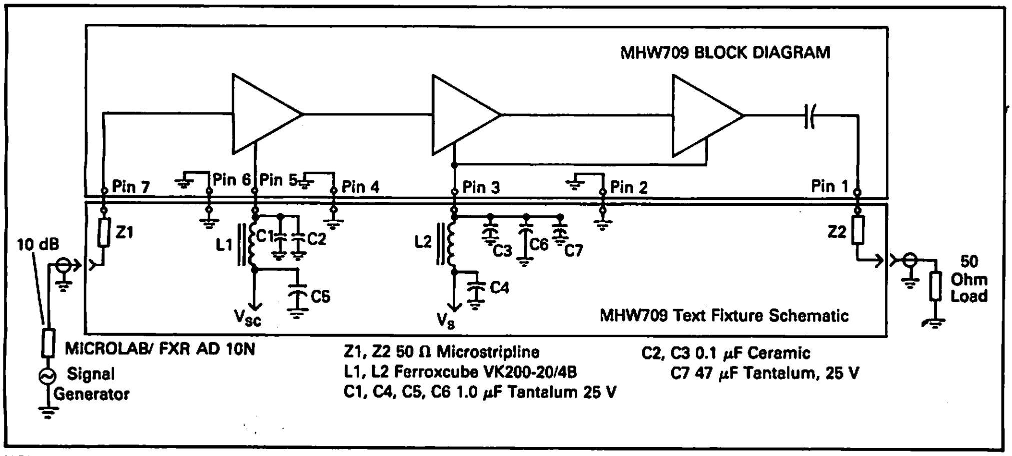
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	67.06	67.56	2.640	2.660
B	51.82	52.95	2.040	2.085
C	8.51	9.14	0.335	0.360
E	2.54	2.92	0.100	0.115
F	2.16	2.62	0.085	0.115
G	61.09 BSC		2.405 BSC	
H	47.88	48.64	1.885	1.915
J	10.16	11.18	0.400	0.440
K	5.85	7.62	0.230	0.300
L	45.34	46.10	1.785	1.815
N	40.26	41.02	1.585	1.615
Q	3.46	3.70	0.136	0.146
R	20.32	20.82	0.800	0.820
S	17.02	17.52	0.670	0.690
U	12.32	13.08	0.485	0.515
V	9.78	10.54	0.385	0.415
W	4.70	5.46	0.185	0.215
X	2.16	2.92	0.085	0.115

CASE 700-04

ELECTRICAL CHARACTERISTICS (V_s and V_{sc} set at 12.5 Vdc, T_A = 25°C, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range MHW709-1 MHW709-2 MHW709-3	—	400 440 470	440 470 512	MHz
Input Power (P_{out} = 7.5 W)	P_{in}	—	100	mW
Power Gain	G_p	18.8	—	dB
Efficiency (P_{out} = 7.5 W)	η	35	—	%
Harmonics (P_{out} = 7.5 W, Reference)	—	—	−40	dB
Input Impedance (P_{out} = 7.5 W, 50 Ω Reference)	Z_{in}	—	2:1	VSWR
Power Degradation (P_{out} = 7.5 W, T_C = 25°C, Reference) (T_C = 0°C to 60°C) (T_C = −30°C to 80°C)	—	 — —	 0.3 0.7	dB
Load Mismatch (VSWR = ∞, V_s = V_{sc} = 15.5 Vdc, P_{out} = 10 W)	—	No degradation in P_{out}		
Stability 1. (P_{in} = 30 to 150 mW, Load Mismatch = 2:1, 50 Ω Reference, V_s = V_{sc} = 3.0 to 15.5 Vdc) 2. (V_s = 12.5 Vdc, V_{sc} adjusted for P_{out} = 5.0 to 10 W, P_{in} = 100 mW, Load Mismatch = 4:1, 50 Ω Reference, note $V_{sc} \le V_s$)	—	All spurious outputs more than 70 dB below desired signal		
Standby Current (P_{in} = 0)	$I_{sc(q)}$	—	10	mA

FIGURE 1 — UHF POWER AMPLIFIER TEST SETUP



NOTE: No Internal D.C. blocking on input pin.

TYPICAL PERFORMANCE CURVES
(MHW709-2)

FIGURE 2 – INPUT POWER, EFFICIENCY, AND VSWR versus FREQUENCY

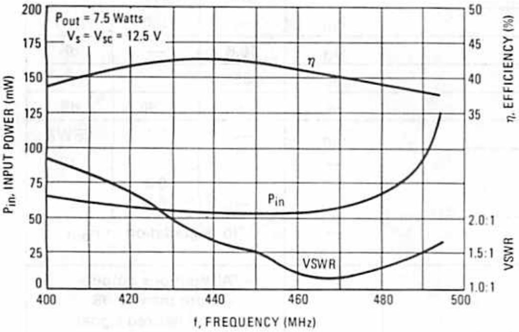


FIGURE 3 – OUTPUT POWER versus INPUT POWER

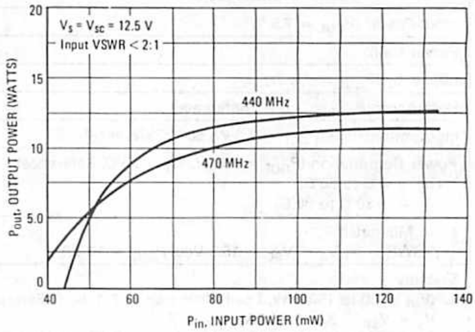


FIGURE 4 – OUTPUT POWER versus VOLTAGE

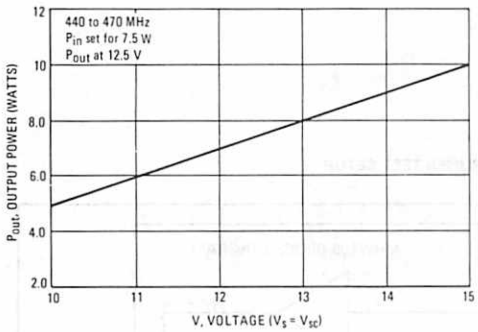


FIGURE 5 – OUTPUT POWER versus GAIN CONTROL VOLTAGE

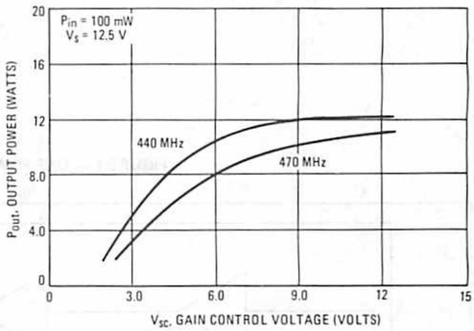


FIGURE 6 – GAIN CONTROL CURRENT versus VOLTAGE

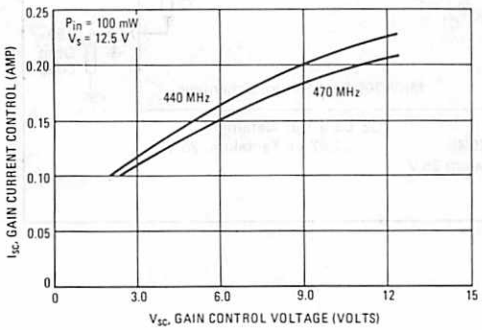
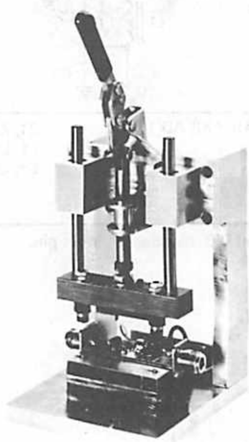


FIGURE 7 – TEST CIRCUIT



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APPLICATIONS INFORMATION

Nominal Operation

All electrical specifications are based on the nominal conditions of V_{SC} (Pin 5) and V_S (Pin 3) equal to 12.5 Vdc and with output power equaling 7.5 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100° base plate temperature is 165°. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use has been made with the factory representative.

Gain Control

The intent of these gain control methods is to set the nominal P_{out}. Do not use them for wide range gain control.

In general, the module output power should be limited to 10 watts. The preferred method of power output control is to fix both V_{SC} and V_S at 12.5 Vdc and vary the input RF drive level at Pin 7. The next method is to control V_{SC} through a stiff voltage source.

A third method of power output control is to control V_{SC} through a current source or voltage source with series resistance. This mode of control creates a region of negative slope on the power gain profile curve and aggravates output power slump with temperature.

Decoupling

Due to the high gain of the three stages and the module size limitation, external decoupling network requires careful consideration. Both Pins 3 and 5 are internally bypassed with a 0.018 μF chip capacitor effective for frequencies from 5 through 512 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in the test figure schematic are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR less than 3:1.

Load Pull

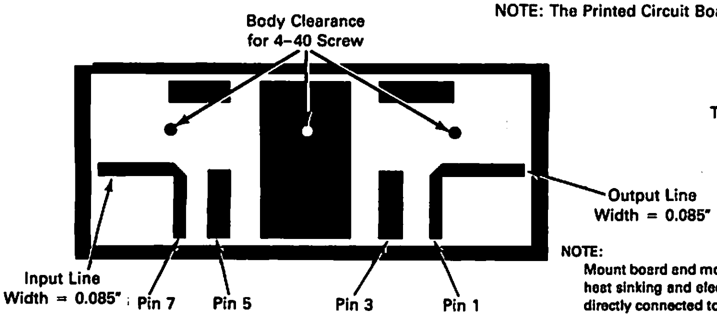
During final test, each module is "load pull" tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_S and V_{SC} equal 15.5 V output, VSWR infinite, output power equal to 10 watts.

Mounting Considerations

To insure optimum heat transfer from the flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.005 inch to prevent fracturing of ceramic substrate material. For more information on module mounting, see EB-107.

FIGURE 8 — UHF POWER AMPLIFIER TEST FIXTURE PRINTED CIRCUIT BOARD

NOTE: The Printed Circuit Board shown is 75% of the original.



NOTE:
Mount board and module on 1/2" thick aluminum block for heat sinking and electrical ground. Pins 2, 4 and 6 are not directly connected to ground in this test fixture. Ground is provided through module heat sink.

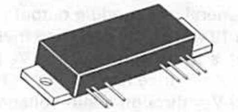
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW710-1
MHW710-2
MHW710-3

The RF Line

13 W 400–512 MHz

RF POWER AMPLIFIERS



UHF POWER AMPLIFIERS

. . . designed for 12.5 volt UHF power amplifier applications in industrial and commercial FM equipment operating from 400 to 512 MHz.

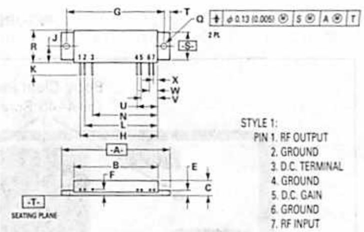
- Specified 12.5 Volt, UHF Characteristics —
  Output Power = 13 Watts
  Minimum Gain = 19.4 dB
  Harmonics = 40 dB
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Gain Control Pin for Manual or Automatic Output Level Control
- Thin Film Hybrid Construction Gives Consistent Performance and Reliability

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_s, V_{sc}	15.5	Vdc
RF Input Power	P_{in}	250	mW
RF Output Power (@ $V_s = V_{sc} = 12.5$ V)	P_{out}	15	W
Operating Case Temperature Range	T_C	−30 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS
(V_s and V_{sc} set at 12.5 Vdc, $T_A = 25°C$, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range MHW710-1 MHW710-2 MHW710-3	—	400 440 470	440 470 512	MHz
Input Power (P_{out} = 13 W)	P_{in}	—	150	mW
Power Gain	G_p	19.4	—	dB
Efficiency (P_{out} = 13 W)	η	35	—	%
Harmonics (P_{out} = 13 W, Reference)	—	—	−40	dB
Input Impedance (P_{out} = 13 W, 50 Ω Reference)	Z_{in}	—	2:1	VSWR
Power Degradation (P_{out} = 13 W, T_C = 25°C, Reference) (T_C = 0°C to 60°C) (T_C = −30°C to 80°C)	—	 — —	 0.3 0.7	dB
Load Mismatch (VSWR = ∞, V_s = 15.5 Vdc, P_{out} = 16.5 W)	—	No degradation in P_{out}		
Stability 1. (P_{in} = 50 to 200 mW, Load Mismatch = 4:1, 50 Ω reference, $V_s = V_{sc}$ = 8.0 to 15.5 Vdc) 2. (V_s = 12.5 Vdc, V_{sc} adjusted for P_{out} = 5.0 to 15 W, P_{in} = 150 mW, Load Mismatch = 4:1, 50 Ω reference, note $V_{sc} \leq V_s$)	—	All spurious outputs more than 70 dB below desired signal		



STYLE 1:
PIN 1. RF OUTPUT
2. GROUND
3. D.C. TERMINAL
4. GROUND
5. D.C. GAIN
6. GROUND
7. RF INPUT

NOTES:
1. MOUNTING HOLES WITHIN 0.13MM (0.005) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	67.06	67.56	2.640	2.660
B	51.82	52.95	2.040	2.085
C	8.51	9.14	0.335	0.360
E	2.54	2.92	0.100	0.115
F	2.16	2.62	0.085	0.115
G	61.09 BSC		2.405 BSC	
H	47.88	48.64	1.885	1.915
J	10.16	11.18	0.400	0.440
K	5.85	7.62	0.230	0.300
L	45.34	46.10	1.785	1.815
N	40.26	41.02	1.585	1.615
Q	3.46	3.70	0.136	0.146
R	20.32	20.82	0.800	0.820
S	17.02	17.52	0.670	0.690
U	12.32	13.08	0.485	0.515
V	9.78	10.54	0.385	0.415
W	4.70	5.46	0.185	0.215
X	2.16	2.92	0.085	0.115

CASE 700-04

5

APPLICATIONS INFORMATION

Nominal Operation

All electrical specifications are based on the nominal conditions of V_{SC} (Pin 5) and V_S (Pin 3) equal to 12.5 Vdc and with output power equaling 13 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100° base plate temperature is 165°. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use has been made with the factory representative.

Gain Control

The intent of these gain control methods is to set the nominal P_{out}. Do not use them for wide range gain control.

In general, the module output power should be limited to 10 watts. The preferred method of power output control is to fix both V_{SC} and V_S at 12.5 Vdc and vary the input RF drive level at Pin 7. The next method is to control V_{SC} through a stiff voltage source.

A third method of power output control is to control V_{SC} through a current source or voltage source with series resistance. This mode of control creates a region of negative slope on the power gain profile curve and aggravates output power slump with temperature.

Decoupling

Due to the high gain of the three stages and the module size limitation, external decoupling network requires careful consideration. Both Pins 3 and 5 are internally bypassed with a 0.018 μF chip capacitor effective for frequencies from 5 through 512 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in the test figure schematic are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR less than 3:1.

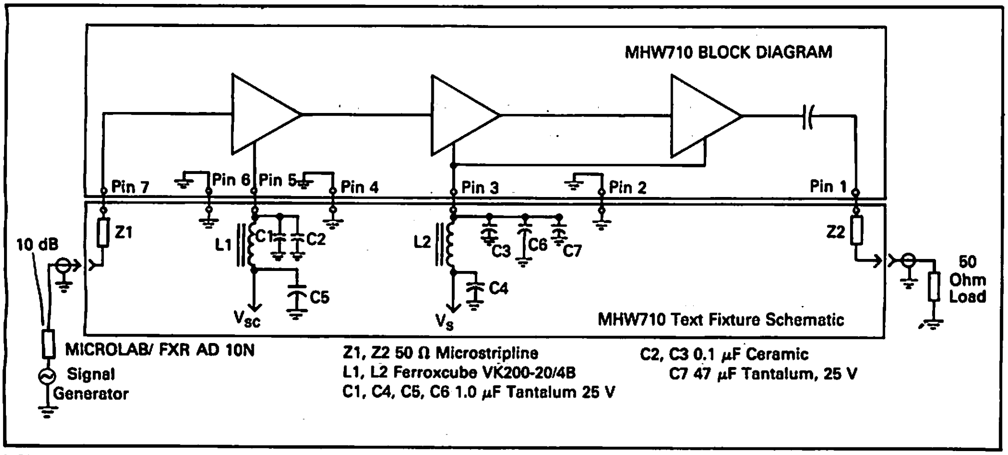
Load Pull

During final test, each module is "load pull" tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_S and V_{SC} equal 15.5 V output, VSWR infinite, output power equal to 16.5 watts.

Mounting Considerations

To insure optimum heat transfer from the flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.005 inch to prevent fracturing of ceramic substrate material. For more information on module mounting, see EB-107.

FIGURE 1 — UHF POWER AMPLIFIER TEST SETUP



NOTE: No Internal D.C. blocking on input pin.

TYPICAL PERFORMANCE CURVES
(MHW710-2)

FIGURE 2 — INPUT POWER, EFFICIENCY, AND VSWR versus FREQUENCY

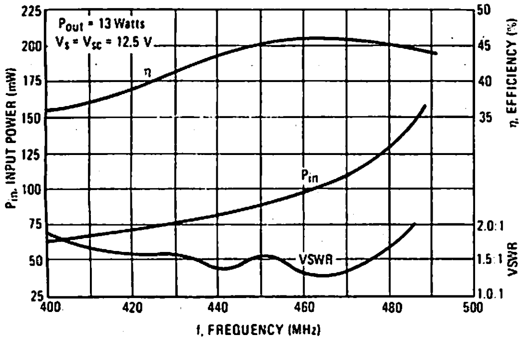


FIGURE 3 — OUTPUT POWER versus INPUT POWER

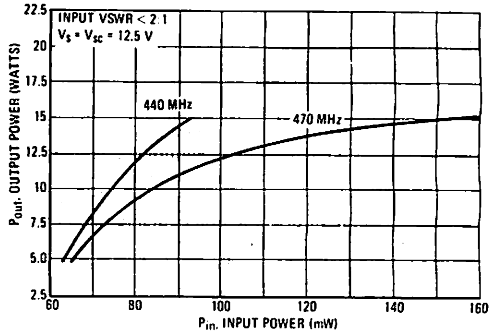


FIGURE 4 — OUTPUT POWER versus VOLTAGE

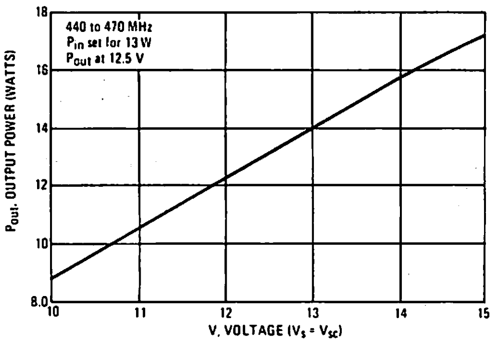


FIGURE 5 — OUTPUT POWER versus GAIN CONTROL VOLTAGE

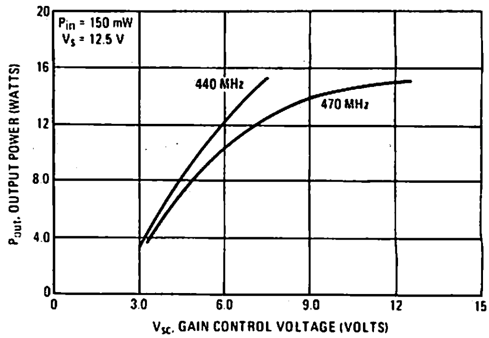


FIGURE 6 — GAIN CONTROL CURRENT versus VOLTAGE

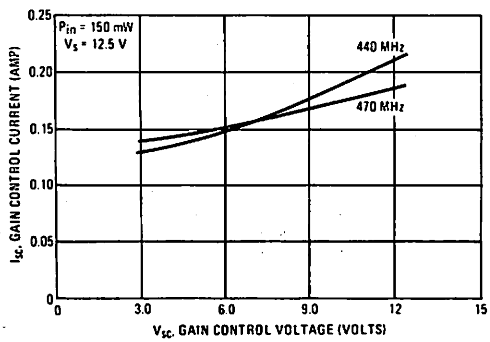


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FIGURE 7 — TEST CIRCUIT

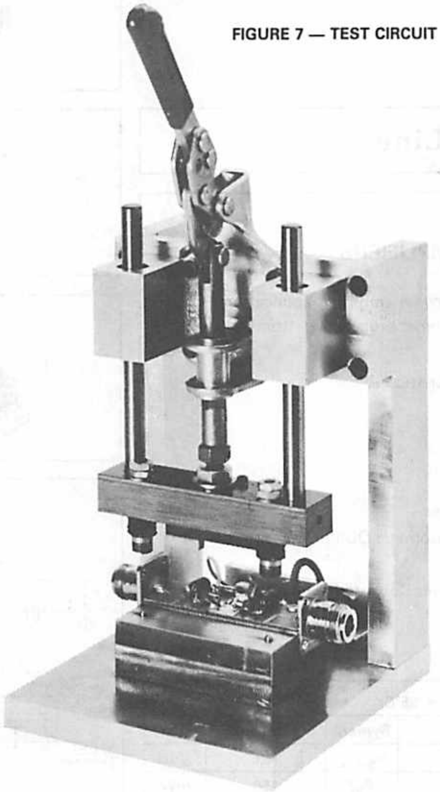
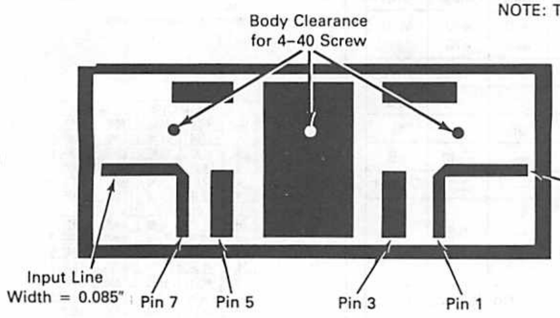


FIGURE 8 — UHF POWER AMPLIFIER TEST FIXTURE PRINTED CIRCUIT BOARD



NOTE: The Printed Circuit Board shown is 75% of the original.

Teflon Glass Board
t = 0.031"
ϵ_r = 2.56

NOTE:
Mount board and module on 1/2" thick aluminum block for heat sinking and electrical ground. Pins 2, 4 and 6 are not directly connected to ground in this test fixture. Ground is provided through module heat sink.

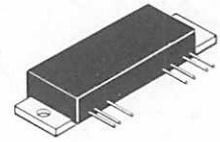
5

MHW720-1
MHW720-2

The RF Line

20 W 400–470 MHz

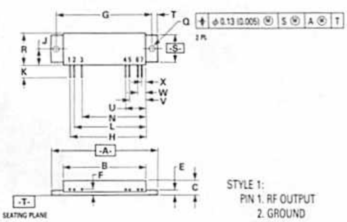
RF POWER
AMPLIFIERS



UHF POWER AMPLIFIERS

. . . designed for 12.5 volt UHF power amplifier applications in industrial and commercial FM equipment operating from 400 to 470 MHz.

- Specified 12.5 Volt, UHF Characteristics –
  Output Power = 20 Watts
  Minimum Gain = 21 dB
  Harmonics = 40 dB
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Gain Control Pin for Manual or Automatic Output Level Control
- Thin Film Hybrid Construction Gives Consistent Performance and Reliability



STYLE 1:
PIN 1. RF OUTPUT
2. GROUND
3. D.C. TERMINAL
4. GROUND
5. D.C. GAIN
6. GROUND
7. RF INPUT

NOTES:
1. MOUNTING HOLES WITHIN 0.13MM (0.005) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	67.06	67.56	2.640	2.660
B	51.82	52.95	2.040	2.085
C	8.51	9.14	0.335	0.360
E	2.54	2.92	0.100	0.115
F	2.16	2.62	0.085	0.115
G	61.09 BSC		2.405 BSC	
H	47.88	48.64	1.885	1.915
J	10.16	11.18	0.400	0.440
K	5.85	7.62	0.230	0.300
L	45.34	46.10	1.785	1.815
N	40.26	41.02	1.585	1.615
Q	3.46	3.70	0.136	0.146
R	20.32	20.82	0.800	0.820
S	17.02	17.52	0.670	0.690
U	12.32	13.08	0.485	0.515
V	9.78	10.54	0.385	0.415
W	4.70	5.46	0.185	0.215
X	2.16	2.92	0.085	0.115

CASE 700-04

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_S,V_{SC}	15.5	Vdc
RF Input Power	P_{in}	250	mW
RF Output Power (@ V_S = V_{SC} = 12.5 V)	P_{out}	25	W
Operating Case Temperature Range	T_C	−30 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS
(V_S and V_{SC} set at 12.5 Vdc, T_A = 25°C, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range MHW720-1 MHW720-2	—	400 440	440 470	MHz
Input Power (P_{out} = 20 W)	P_{in}	—	150	mW
Power Gain	G_p	21	—	dB
Efficiency (P_{out} = 20 W)	η	35	—	%
Harmonics (P_{out} = 20 W, Reference)	—	—	−40	dB
Input Impedance (P_{out} = 20 W, 50 Ω Reference)	Z_{in}	—	2:1	VSWR
Power Degradation (P_{out} = 20 W, T_C = 25°C, Reference) (T_C = 0°C to 60°C) (T_C = −30°C to 80°C)	—	 — —	 0.3 0.7	dB
Load Mismatch (VSWR = ∞, V_S = 15.5 Vdc, P_{out} = 30 W)	—	No degradation in P_{out}		
Stability 1. (P_{in} = 50 to 200 mW, Load Mismatch = 2:1, 50 Ω reference, V_S = V_{SC} = 8.0 to 15.5 Vdc) 2. (V_S = 12.5 Vdc, V_{SC} adjusted for P_{out} = 5.0 to 20 W, P_{in} = 150 mW, Load Mismatch = 2:1, 50 Ω reference, note $V_{SC} \leq V_S$)	—	All spurious outputs more than 70 dB below desired signal		

APPLICATIONS INFORMATION

Nominal Operation

All electrical specifications are based on the nominal conditions of V_{SC} (Pin 5) and V_S (Pin 3) equal to 12.5 Vdc and with output power equaling 20 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100° base plate temperature is 165°. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use has been made with the factory representative.

Gain Control

The intent of these gain control methods is to set the nominal P_{out}. Do not use them for wide range gain control.

In general, the module output power should be limited to 20 watts. The preferred method of power output control is to fix both V_{SC} and V_S at 12.5 Vdc and vary the input RF drive level at Pin 7. The next method is to control V_{SC} through a stiff voltage source.

A third method of power output control is to control V_{SC} through a current source or voltage source with series resistance. This mode of control creates a region of negative slope on the power gain profile curve and aggravates output power slump with temperature.

Decoupling

Due to the high gain of the three stages and the module size limitation, external decoupling network requires careful consideration. Both Pins 3 and 5 are internally bypassed with a 0.018 μF chip capacitor effective for frequencies from 5 through 512 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in the test figure schematic are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR less than 3:1.

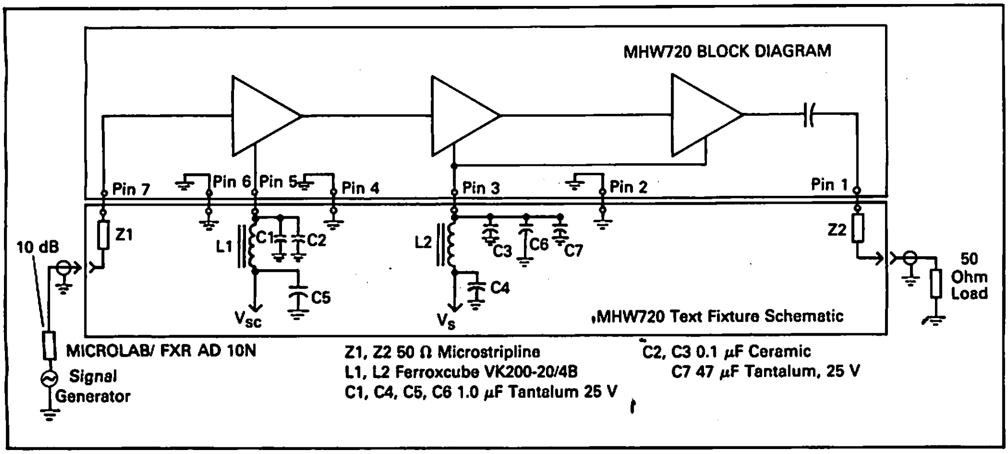
Load Pull

During final test, each module is "load pull" tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_S and V_{SC} equal 15.5 V output, VSWR infinite, output power equal to 30 watts.

Mounting Considerations

To insure optimum heat transfer from the flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.005 inch to prevent fracturing of ceramic substrate material. For more information on module mounting, see EB-107.

FIGURE 1 — UHF POWER AMPLIFIER TEST SETUP



NOTE: No Internal D.C. blocking on input pin.

TYPICAL PERFORMANCE CURVES
(MHW720-2)

FIGURE 2 — INPUT POWER, EFFICIENCY, AND VSWR versus FREQUENCY

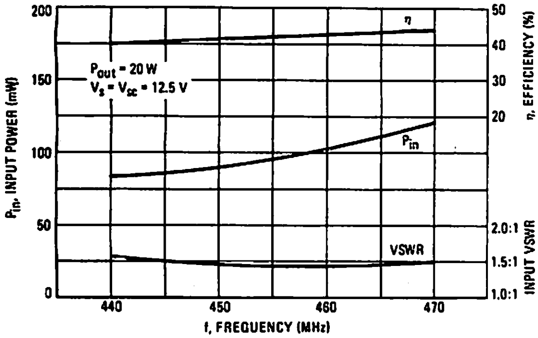


FIGURE 3 — OUTPUT POWER versus INPUT POWER

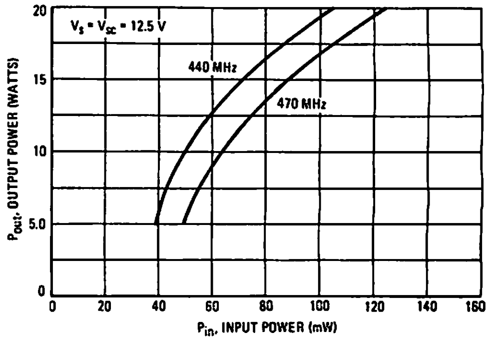


FIGURE 4 — OUTPUT POWER versus VOLTAGE

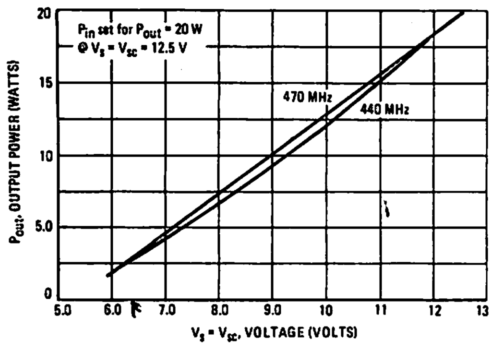


FIGURE 5 — OUTPUT POWER versus GAIN CONTROL VOLTAGE

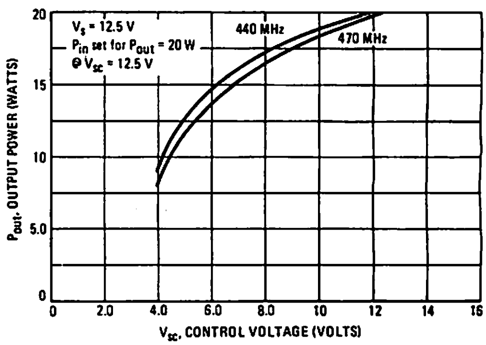


FIGURE 6 — GAIN CONTROL CURRENT versus VOLTAGE

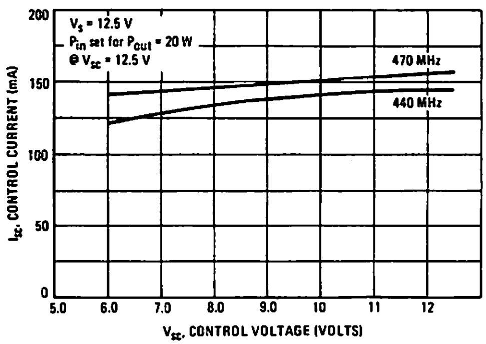


FIGURE 7 — TEST CIRCUIT

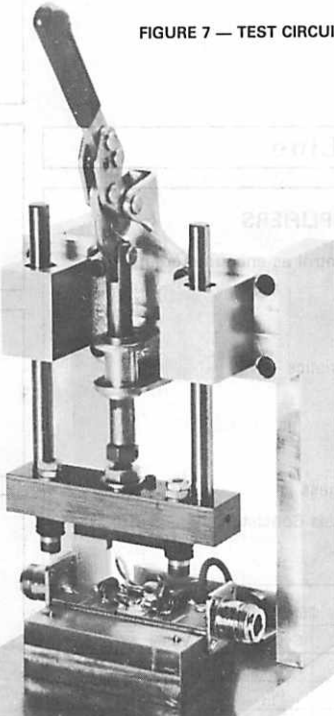
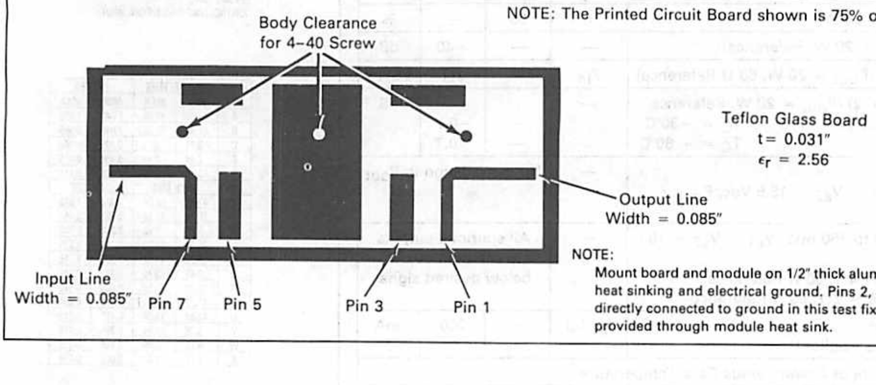


FIGURE 8 — UHF POWER AMPLIFIER TEST FIXTURE PRINTED CIRCUIT BOARD

NOTE: The Printed Circuit Board shown is 75% of the original.



NOTE:
Mount board and module on 1/2" thick aluminum block for heat sinking and electrical ground. Pins 2, 4 and 6 are not directly connected to ground in this test fixture. Ground is provided through module heat sink.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW720A1
MHW720A2

The RF Line

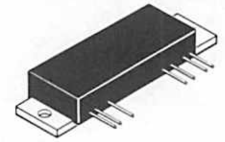
UHF POWER AMPLIFIERS

. . . capable of wide power range control as encountered in UHF cellular telephone applications.

- MHW720A1 400–440 MHz
- MHW720A2 440–470 MHz
- Specified 12.5 Volt, UHF Characteristics —
  Output Power = 20 Watts
  Minimum Gain = 21 dB
  Harmonics = −40 dB (Max)
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability

20 W 400–470 MHz

RF POWER AMPLIFIERS

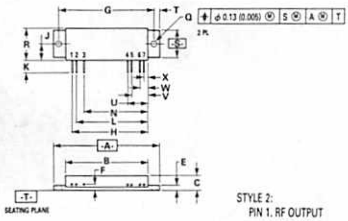


MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{s1}, V_{s2}	15.5	Vdc
RF Input Power	P_{in}	250	mW
RF Output Power (@ V_{s1} = V_{s2} = 12.5 V)	P_{out}	25	W
Operating Case Temperature Range	T_C	−30 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS
(V_{s1} and V_{s2} set at 12.5 Vdc, T_C = 25°C, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency Range MHW720A1 MHW720A2	—	400 440	440 470	MHz
Input Power (P_{out} = 20 W)	P_{in}	—	150	mW
Power Gain (P_{out} = 20 W)	G_p	21	—	dB
Efficiency (P_{out} = 20 W)	η	35	—	%
Harmonics (P_{out} = 20 W, Reference)	—	—	−40	dB
Input Impedance (P_{out} = 20 W, 50 Ω Reference)	Z_{in}	—	2:1	VSWR
Gain Degradation (2) (P_{out} = 20 W, Reference Gain @ T_C = +25°C) T_C = −30°C T_C = +80°C	—	— —	−0.7 −0.7	dB
Load Mismatch (VSWR = ∞, V_{s1} = V_{s2} = 15.5 Vdc, P_{out} = 30 W)	—	No degradation in P_{out}		
Stability (P_{in} = 0 to 250 mW, V_{s1} = V_{s2} = 10 to 15.5 Vdc) 1. Load VSWR = 4:1, 50 Ω Reference 2. Source VSWR = 2:1, 50 Ω Reference	—	All spurious outputs more than 60 dB below desired signal		
Quiescent Current (I_{s1} No RF Drive Applied)	I_{s1} (q)	—	200	mA
(2) See Figure 5, Input Power versus Case Temperature				



STYLE 2:
PIN 1. RF OUTPUT
2. GROUND
3. Vs 2
4. GROUND
5. Vs 1
6. GROUND
7. RF INPUT

NOTES:
1. MOUNTING HOLES WITHIN 0.13MM (0.005) DIA OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	67.06	67.56	2.640	2.660
B	51.82	52.95	2.040	2.085
C	8.51	9.14	0.335	0.360
E	2.54	2.92	0.100	0.115
F	2.16	2.62	0.085	0.115
G	61.09 BSC		2.405 BSC	
H	47.88	48.64	1.885	1.915
J	10.16	11.18	0.400	0.440
K	5.85	7.62	0.230	0.300
L	45.34	46.10	1.785	1.815
N	40.26	41.02	1.585	1.615
Q	3.46	3.70	0.136	0.146
R	20.32	20.82	0.800	0.820
S	17.02	17.52	0.670	0.690
U	12.32	13.08	0.485	0.515
V	9.78	10.54	0.385	0.415
W	4.70	5.46	0.185	0.215
X	2.16	2.92	0.085	0.115

CASE 700-04

APPLICATIONS INFORMATION

Nominal Operation

All electrical specifications are based on the nominal conditions of V_{S1} (Pin 5) and V_{S2} (Pin 3) equal to 12.5 Vdc and with output power equaling 20 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100° base plate temperature is 165°. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use has been made with the factory representative.

Gain Control

This module is designed for wide range P_{out} level control. The recommended method of power output control, as shown in Figure 3, is to fix V_{S1} and V_{S2} at 12.5 Vdc and vary the input RF drive level at Pin 7.

In all applications, the module output power should be limited to 20 watts.

Decoupling

Due to the high gain of the three stages and the module size limitation, the external decoupling network requires careful consideration. Both Pins 3 and 5 are internally bypassed with a 0.018 μF chip capacitor effective for frequencies from 5 through 470 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in the test fixture schematic are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR less than 4:1.

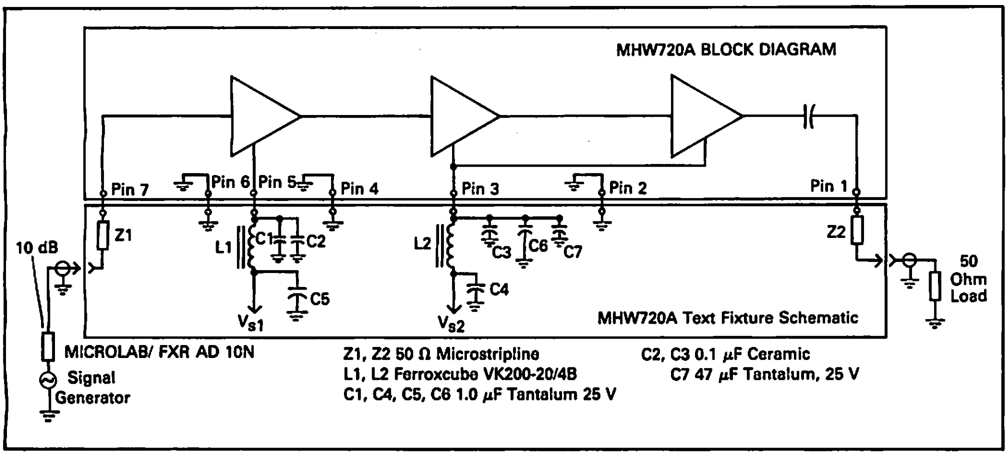
Load Mismatch

During final test, each module is load mismatch tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_{S1} and V_{S2} equal 15.5 V, load VSWR infinite, and output power equal to 30 watts.

Mounting Considerations

To insure optimum heat transfer from the flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.005 inch to prevent fracturing of ceramic substrate material. For more information on module mounting, see EB-107.

FIGURE 1 — UHF POWER AMPLIFIER TEST SETUP



NOTE: No Internal D.C. blocking on input pin.

FIGURE 2 — INPUT POWER, EFFICIENCY, AND VSWR versus FREQUENCY

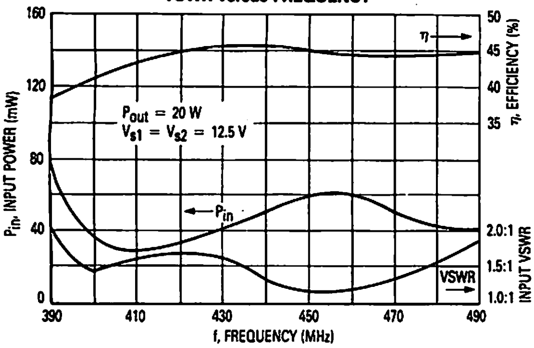


FIGURE 3 — OUTPUT POWER versus INPUT POWER

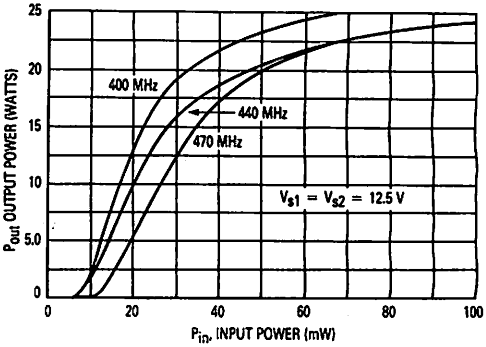


FIGURE 4 — OUTPUT POWER versus VOLTAGE

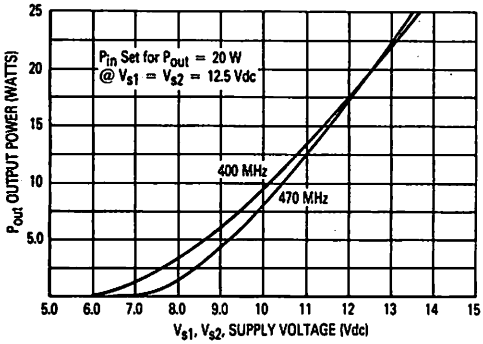


FIGURE 5 — INPUT POWER versus CASE TEMPERATURE

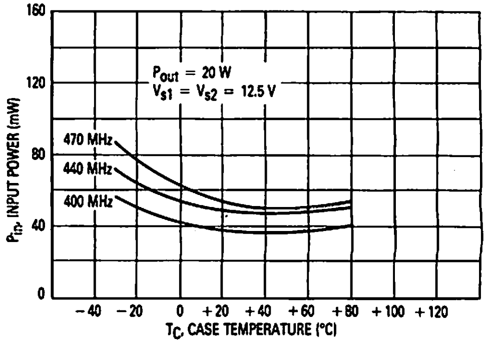


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FIGURE 6 — OUTPUT POWER versus CASE TEMPERATURE @ 10.8 V SUPPLY

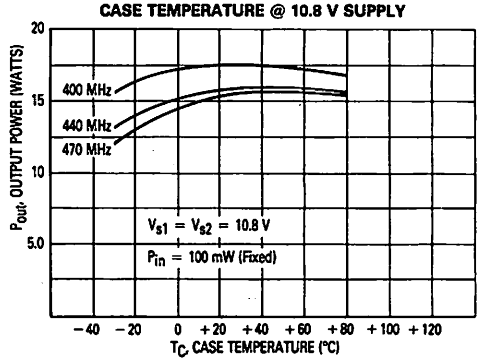


FIGURE 7 — TEST CIRCUIT

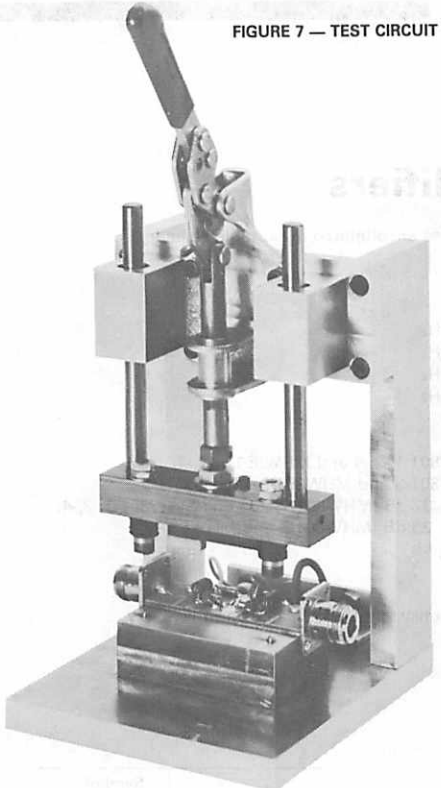
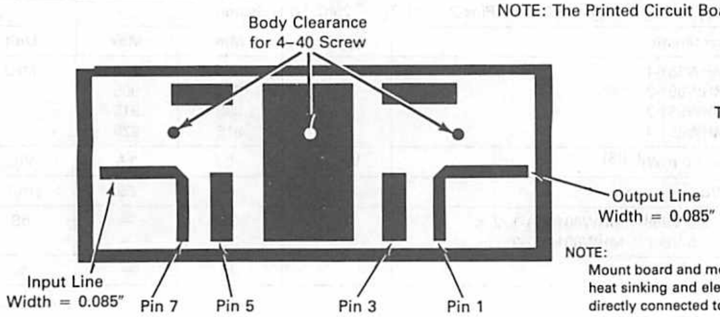


FIGURE 8 — UHF POWER AMPLIFIER TEST FIXTURE
PRINTED CIRCUIT BOARD

NOTE: The Printed Circuit Board shown is 75% of the original.



Teflon Glass Board
$t = 0.031''$
$\epsilon_r = 2.56$

NOTE:
Mount board and module on 1/2" thick aluminum block for heat sinking and electrical ground. Pins 2, 4 and 6 are not directly connected to ground in this test fixture. Ground is provided through module heat sink.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

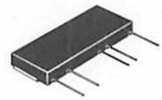
MHW801
MHW851
Series

The RF Line
UHF Power Amplifiers

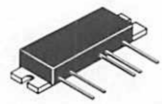
. . . capable of wide power range control as encountered in portable cellular radio applications (30 dB typical).

- High Efficiency
- Smallest Size in Industry
- MHW801-1 and MHW851-1 820–850 MHz
- MHW801-2 and MHW851-2 870–905 MHz
- MHW801-3 and MHW851-3 890–915 MHz
- MHW801-4 and MHW851-4 915–925 MHz
- Specified 6.0 Volt Characteristics
  RF Input Power = 1.0 mW (0 dBm)
  RF Output Power = 1.6 Watts (MHW801-1,-2,-4 and MHW851-1,-2,-4)
  = 2.0 Watts (MHW801-3 and MHW851-3)
  Minimum Gain ($V_{Control}$ = 3.5 V) = 32 dB (MHW801-1,-2,-4 and MHW851-1,-2,-4)
  ($V_{Control}$ = 3.5 V) = 33 dB (MHW801-3 and MHW851-3)
  Harmonics = −45 dBc Max @ 2.0 f_o
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability

1.6 W — 820–925 MHz
RF POWER
AMPLIFIERS



CASE 413-01, STYLE 1
MHW801 SERIES



CASE 301N-01, STYLE 1
MHW851 SERIES

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 2, 3, 4)	$V_{s1,2,3}$	7.5	Vdc
DC Control Voltage (Pin 1)	V_{Cont}	4.0	Vdc
RF Input Power	P_{in}	3.0	mW
RF Output Power (V_{s1} = V_{s2} = V_{s3} = 7.5 V)	P_{out}	3.0	W
Operating Case Temperature Range	T_C	−30 to +100	°C
Storage Temperature Range	T_{stg}	−30 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{s1} = V_{s2} = V_{s3} = 6.0 Vdc, (Pins 2, 3, 4), T_C = 25°C, 50 Ω System)

Characteristic	Symbol	Min	Max	Unit
Frequency Range MHW801-1 and MHW851-1 MHW801-2 and MHW851-2 MHW801-3 and MHW851-3 MHW801-4 and MHW851-4	—	820 870 890 915	850 905 915 925	MHz
Control Voltage (P_{out} = 1.6 W, P_{in} = 1.0 mW)(1)(3)	V_{Cont}	0	3.5	Vdc
Quiescent Current (V_{s1}, Pin 2 = 6.0 Vdc)(2)	$I_{s1(q)}$	—	65	mA
Power Gain (P_{out} = 1.6 W, V_{Cont} = 3.5 Vdc)(3) MHW801/851-1,-2,-4 (P_{out} = 2.0 W, V_{Cont} = 3.5 Vdc) MHW801/851-3	G_p	32 33	— —	dB
Efficiency (P_{out} = 1.6 W, P_{in} = 1.0 mW)(1)(3)	η	45	—	%

(1) Adjust V_{cont} for specified P_{out}.
(2) V_{Cont} = 0 Vdc.
(3) P_{out} = 2.0 watts for MHW801-3 and MHW851-3 only.

(continued)

ELECTRICAL CHARACTERISTICS — continued ($V_{s1} = V_{s2} = V_{s3}$ = 6.0 Vdc, (Pins 2, 3, 4), T_C = 25°C, 50 Ω System)

Characteristic	Symbol	Min	Max	Unit
Harmonics (P_{out} = 1.6 W)(1)(3) 2.0 f_o (P_{in} = 1.0 mW) 3.0 f_o	—	— —	−45 −55	dBc
Input VSWR (P_{out} = 1.6 W, P_{in} = 1.0 mW), 50 Ω Ref.(1)(3)	—	—	2.0:1	—
Noise Power 30 kHz Bandwidth, 45 MHz, above f_o (P_{out} = 1.6 W)(1)(3) T_C = +25°C (P_{in} = 1.0 mW) T_C = +100°C	—	 — —	 −85 −82	dBm
Load Mismatch ($V_{s1} = V_{s2} = V_{s3}$ = 7.5 Vdc) VSWR = 10:1, P_{out} = 3.0 W, P_{in} = 3.0 mW)(1)		No Degradation in Power Output		
Stability (P_{in} = 0.5–2.0 mW, $V_{s1} = V_{s2} = V_{s3}$ = 4.8–7.5 Vdc P_{out} between 0 mW and 1.6 W(1)(3) Load VSWR = 6:1, Source VSWR = 3:1)		All spurious outputs more than 60 dB below desired signal		

(1) Adjust V_{cont} for specified P_{out}.
(2) V_{Cont} = 0 Vdc.
(3) P_{out} = 2.0 watts for MHW801/851-3 only.

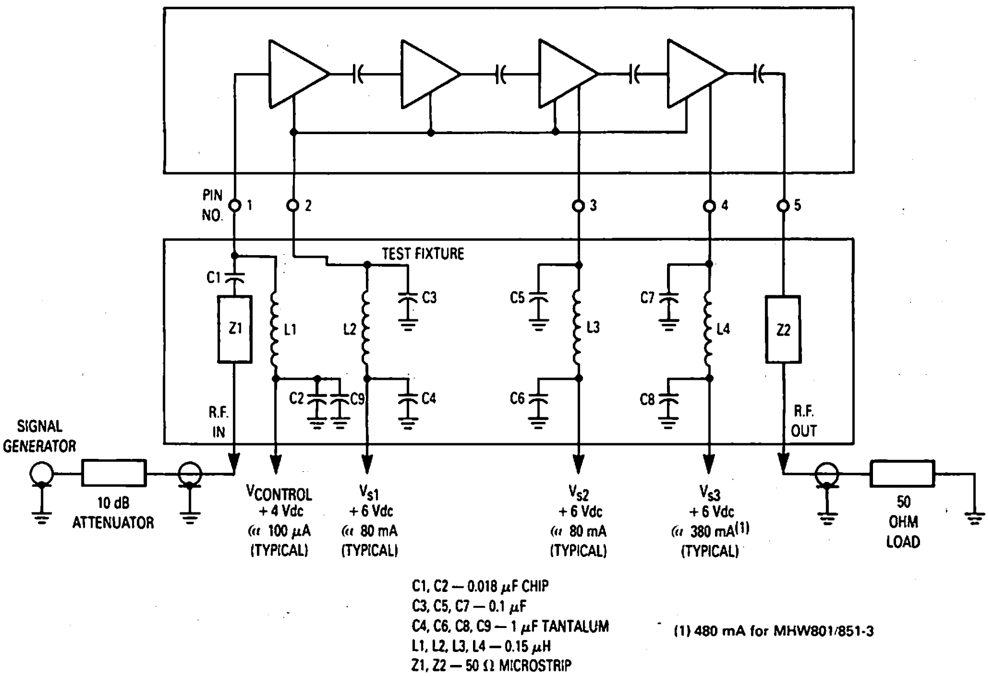


Figure 1. Power Module Test System Block Diagram

5

TYPICAL CHARACTERISTICS

MHW801/851-1 and MHW801/851-2

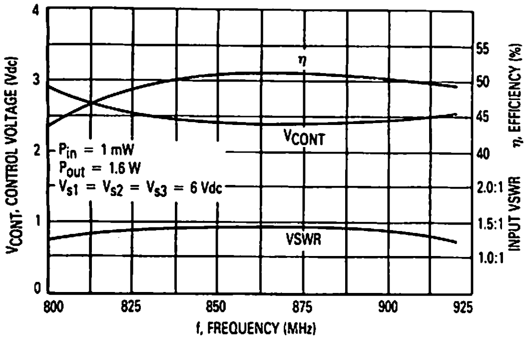


Figure 2. Control Voltage, Efficiency and Input VSWR versus Frequency

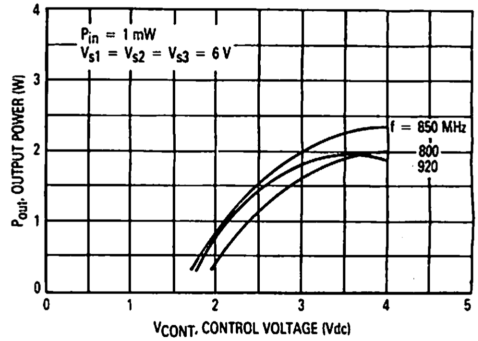


Figure 3. Output Power versus Control Voltage

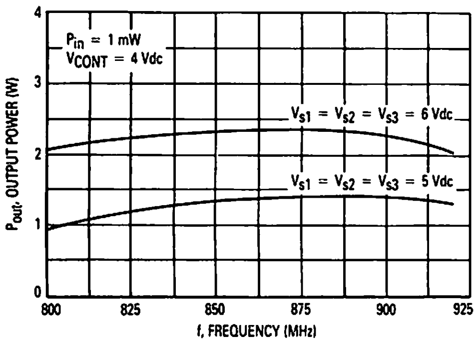


Figure 4. Output Power versus Frequency

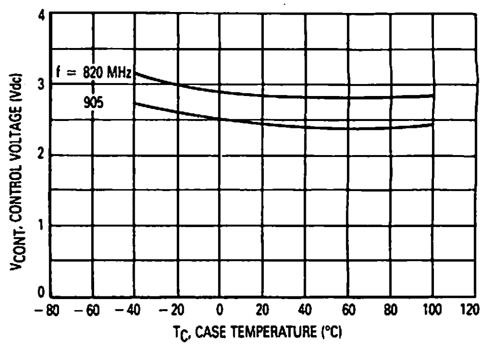


Figure 5. Control Voltage versus Case Temperature

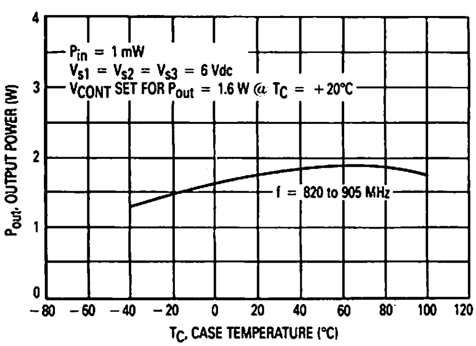


Figure 6. Output Power versus Case Temperature

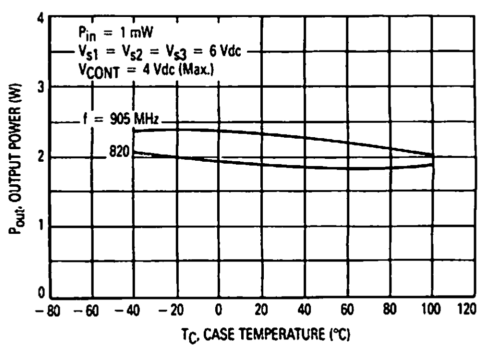


Figure 7. Output Power versus Case Temperature at Maximum Control Voltage

TYPICAL CHARACTERISTICS (continued)

MHW801/851-3 and MHW801/851-4

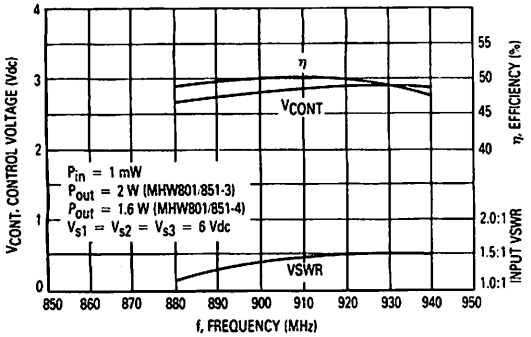


Figure 8. Control Voltage, Efficiency and VSWR versus Frequency

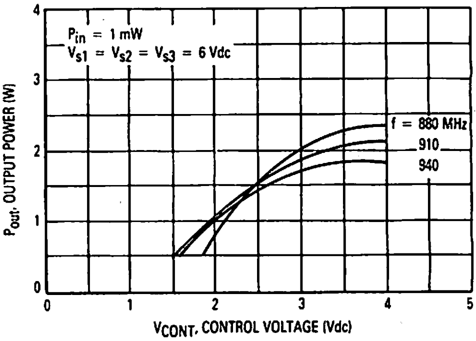


Figure 9. Output Power versus Control Voltage

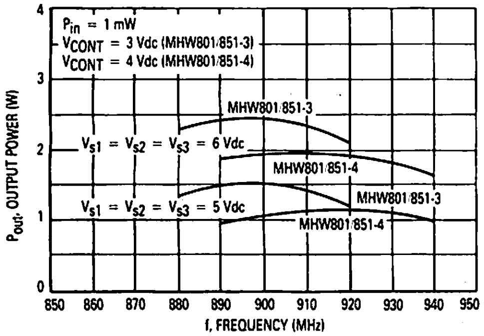


Figure 10. Output Power versus Frequency

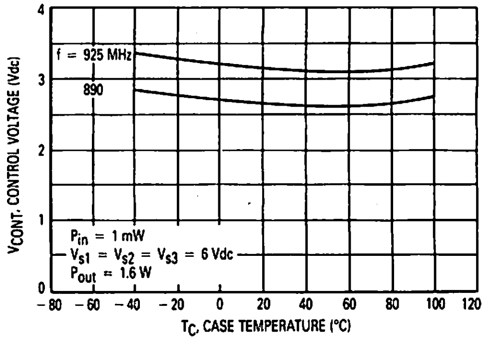


Figure 11. Control Voltage versus Case Temperature

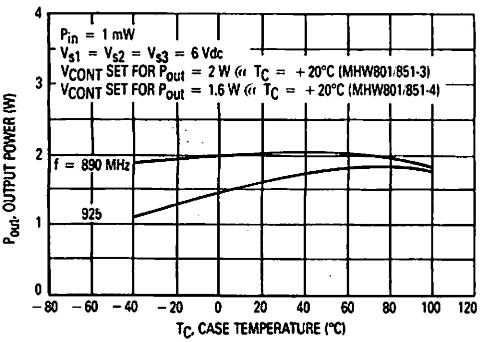


Figure 12. Output Power versus Case Temperature

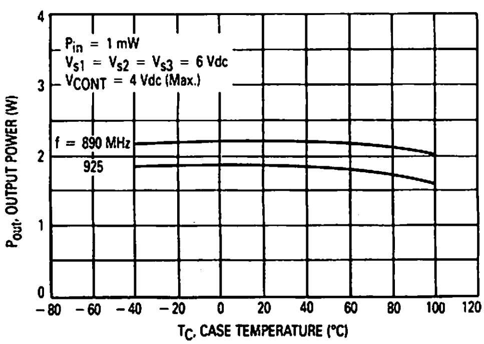


Figure 13. Output Power versus Case Temperature at Maximum Control Voltage

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APPLICATIONS INFORMATION

NOMINAL OPERATION

All electrical specifications are based on the nominal conditions of $V_{S1} = V_{S2} = V_{S3} = 6.0$ Vdc (Pins 2, 3, 4). With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100°C case operating temperature is 165°C. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use have been made with the factory representative.

GAIN CONTROL

The module output should be limited to specified value. The preferred method of power output control is to fix $V_{S1} = V_{S2} = V_{S3} = 6.0$ Vdc (Pins 2, 3, 4), P_{in} (Pin 1) at 1 mW, and vary V_{Cont} (Pin 1) voltage.

DECOUPLING

Due to the high gain of the three stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3 and 4 are internally bypassed with a 0.018 μF chip capacitor which is effective for frequencies from 5 MHz through 940 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in Figure 1 are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.

MOUNTING CONSIDERATIONS

For the MHW801 Series module, mounting is generally accomplished by soldering the flange to a suitable heat sink. This can be done with a low temperature solder such as 52% In, 48% Sn and type "R" Flux which liquifies below 150°C. Under no circumstances should the MHW801 Series modules be heated to a temperature greater than ≈165°C. Internal construction of the module has been achieved using 36% Tin, 62% lead, 2% silver solder which liquifies at 179–180°C.

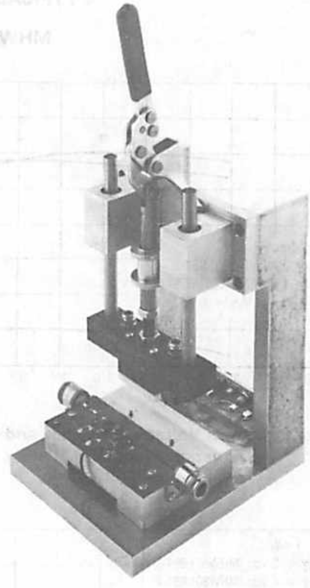


Figure 14. Test Fixture Assembly

Also remember that the modules are NOT hermetic. Do not immerse a module in a flux cleaning solution or other liquids under any circumstances.

LOAD MISMATCH

During final test, each module is load mismatch tested in a fixture having the identical decoupling networks described in Figure 1. Electrical conditions are $V_{S1} = V_{S2} = V_{S3}$ equal to 7.5 Vdc, VSWR equal to 10:1, and output power equal to 3 watts.

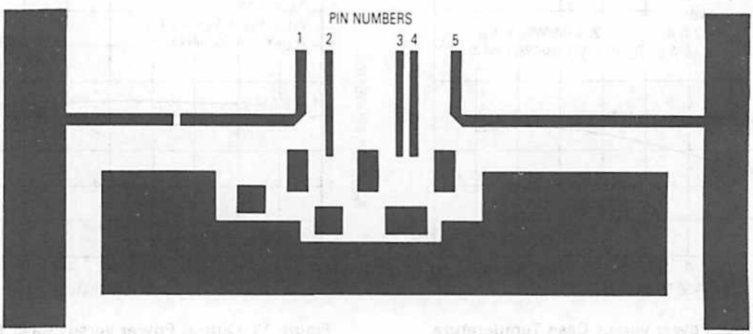


Figure 15. Photomaster For Test Fixture

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

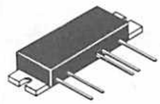
MHW803 Series

The RF Line
UHF Power Amplifiers

. . . capable of wide power range control as encountered in portable cellular radio applications (30 dB typical).

- MHW803-1 820–850 MHz
- MHW803-2 806–870 MHz
- MHW803-3 870–905 MHz
- Specified 7.5 Volt Characteristics
  RF Input Power = 1 mW (0 dBm)
  RF Output Power = 2 Watts
  Minimum Gain ($V_{Control}$ = 4 V) = 33 dB
  Harmonics = −45 dBc Max @ 2 f_o
- 50 Ω Input/Output Impedance
- Guaranteed Stability and Ruggedness
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability

2 W — 806 to 905 MHz UHF POWER AMPLIFIERS



CASE 301E-04, STYLE 1

MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 2,3,4)	$V_{s1,2,3}$	10	Vdc
DC Control Voltage (Pin 1)	V_{Cont}	4	Vdc
RF Input Power	P_{in}	3	mW
RF Output Power (V_{s1} = V_{s2} = V_{s3} = 10 V)	P_{out}	3	W
Operating Case Temperature Range	T_C	−30 to +100	°C
Storage Temperature Range	T_{stg}	−30 to +100	°C

ELECTRICAL CHARACTERISTICS V_{s1} = V_{s2} = V_{s3} = 7.5 Vdc, (Pins 2,3,4), T_C = 25°C, 50 Ω System

Characteristic	Symbol	Min	Max	Unit
Frequency Range MHW803-1 MHW803-2 MHW803-3	—	820 806 870	850 870 905	MHz
Control Voltage (P_{out} = 2 W, P_{in} = 1 mW)(1)	V_{Cont}	0	4	Vdc
Quiescent Current (V_{s1}, Pin 2 = 7.5 Vdc)(2)	$I_{s1(q)}$	—	65	mA
Power Gain (P_{out} = 2 W, V_{Cont} = 4 Vdc)	G_p	33	—	dB
Efficiency (P_{out} = 2 W, P_{in} = 1 mW)(1)	η	37	—	%
Harmonics (P_{out} = 2 W)(1) 2 f_o (P_{in} = 1 mW) 3 f_o	—	— —	−45 −55	dBc
Input VSWR (P_{out} = 2 W, P_{in} = 1 mW), 50 Ω Ref. (1)	—	—	2.0:1	—
Noise power 30 kHz Bandwidth, 45 MHz, above fo (P_{out} = 2 W)(1) T_C = +25°C (P_{in} = 1 mW) T_C = +100°C	— —	— —	−85 −82	dBm dBm
Load Mismatch (V_{s1} = V_{s2} = V_{s3} = 10 Vdc) VSWR = 10:1, P_{out} = 3 W, P_{in} = 3 mW)(1)		No Degradation in Power Output		
Stability (P_{in} = 0.5–2 mW, V_{s1} = V_{s2} = V_{s3} = 6–9 Vdc) P_{out} between 0 mW and 2 W(1) Load VSWR = 6:1, Source VSWR = 3:1)		All spurious outputs more than 60 dB below desired signal		

(1) Adjust V_{cont} for specified P_{out}.
(2) V_{Cont} = 0 Vdc.

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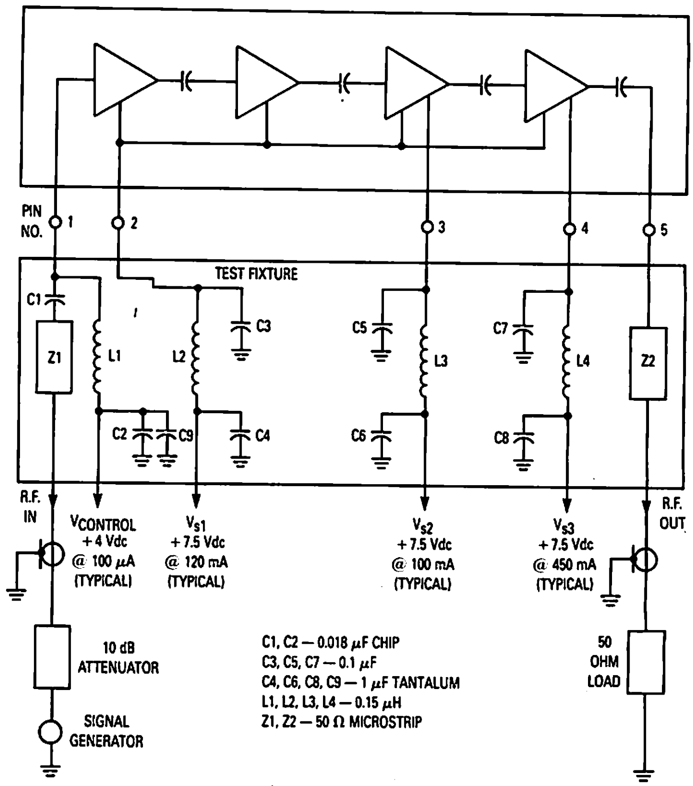

Figure 1. Power Module Test System Block Diagram

TYPICAL CHARACTERISTICS (MHW803-1,-2)

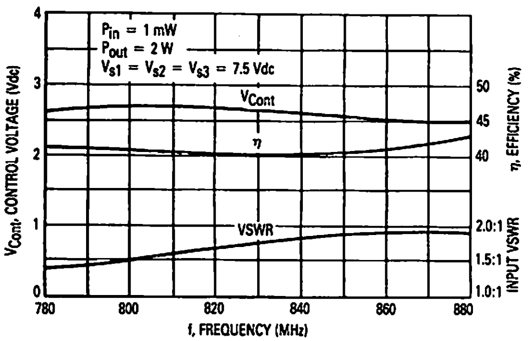

Figure 2. Control Voltage, Efficiency and VSWR versus Frequency

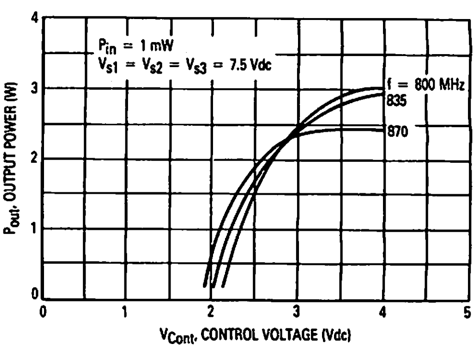

Figure 3. Output Power versus Control Voltage

TYPICAL CHARACTERISTICS
(MHW803-1,-2)

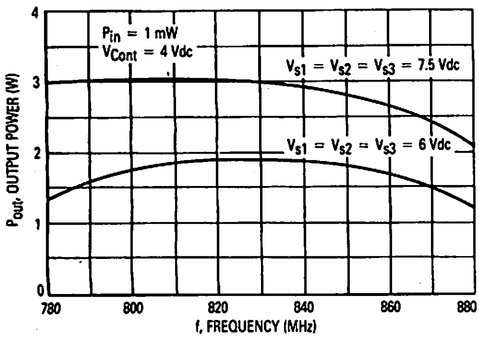

Figure 4. Output Power versus Frequency

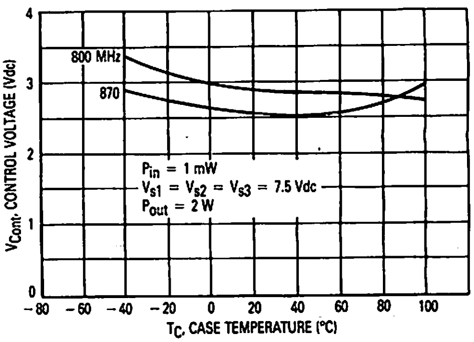

Figure 5. Control Voltage versus Case Temperature

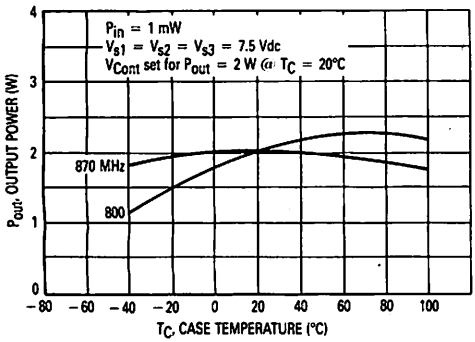

Figure 6. Output Power versus Case Temperature

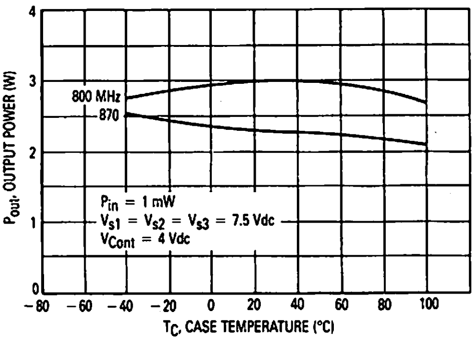

Figure 7. Output Power versus Case Temperature at Maximum Control Voltage

TYPICAL CHARACTERISTICS
(MHW803-3)

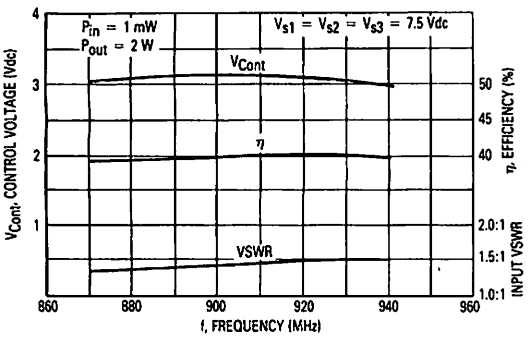

Figure 8. Control Voltage, Efficiency and VSWR versus Frequency

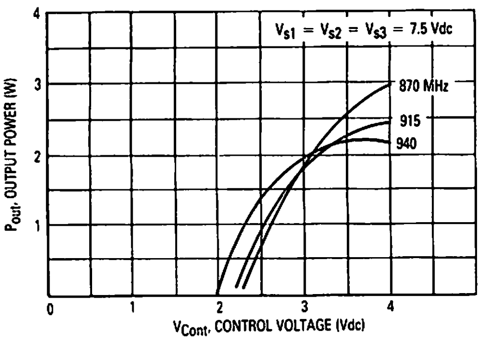

Figure 9. Output Power versus Control Voltage

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TYPICAL CHARACTERISTICS (MHW803-3)

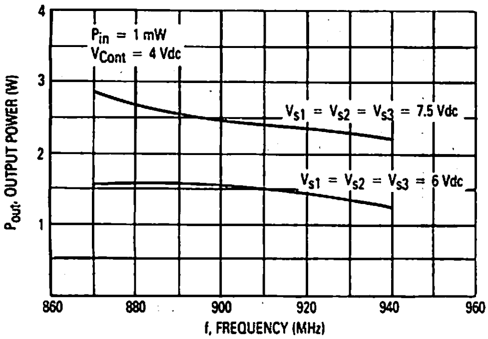

Figure 10. Output Power versus Frequency

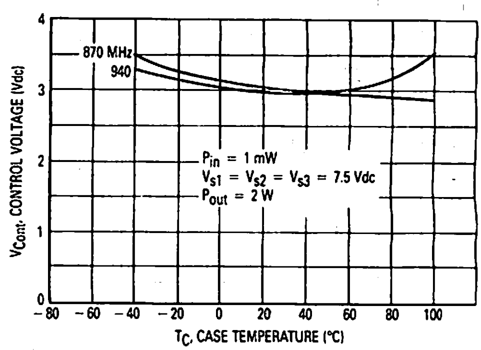

Figure 11. Control Voltage versus Case Temperature

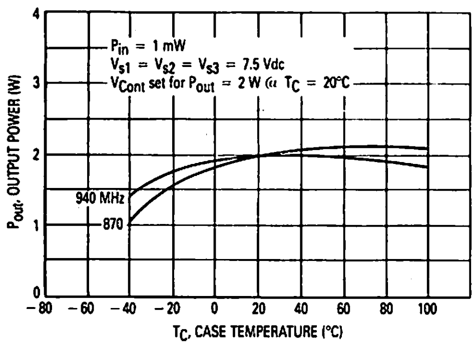

Figure 12. Output Power versus Case Temperature

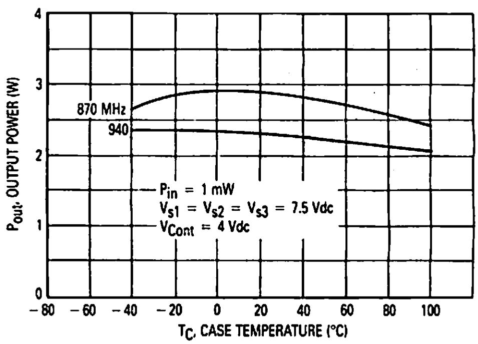

Figure 13. Output Power versus Case Temperature at Maximum Control Voltage

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APPLICATIONS INFORMATION

NOMINAL OPERATION

All electrical specifications are based on the nominal conditions of $V_{s1} = V_{s2} = V_{s3} = 7.5$ Vdc (Pins 2, 3, 4) and P_{out} equal to 2 watts. With these conditions, maximum current density on any device is 1.5×10^5 A/cm^2 and maximum die temperature with 100°C case operating temperature is 165°C. While the modules are designed to have excess gain margin with ruggedness, operation of these units outside the limits of published specifications is not recommended unless prior communications regarding intended use have been made with the factory representative.

GAIN CONTROL

The module output should be limited to 2 watts. The preferred method of power output control is to fix $V_{s1} = V_{s2} = V_{s3} = 7.5$ Vdc (Pins 2, 3, 4), P_{in} (Pin 1) at 1 mW, and vary V_{Cont} (Pin 1) voltage.

DECOUPLING

Due to the high gain of the three stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3 and 4 are internally bypassed with a 0.018 μF chip capacitor which is effective for frequencies from 5 MHz through 905 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in Figure 1 are recommended. Inadequate decoupling will result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.

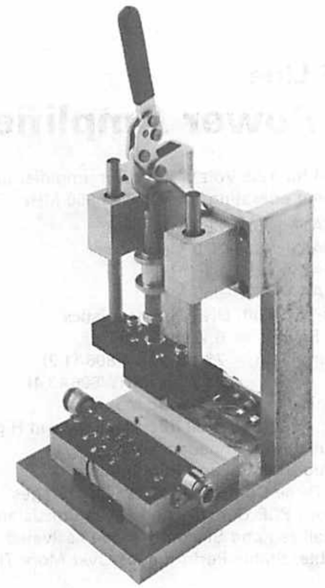

Figure 14. Test Fixture Assembly

LOAD MISMATCH

During final test, each module is load mismatch tested in a fixture having the identical decoupling networks described in Figure 1. Electrical conditions are $V_{s1} = V_{s2} = V_{s3}$ equal to 10 Vdc, VSWR equal to 10:1, and output power equal to 3 watts.

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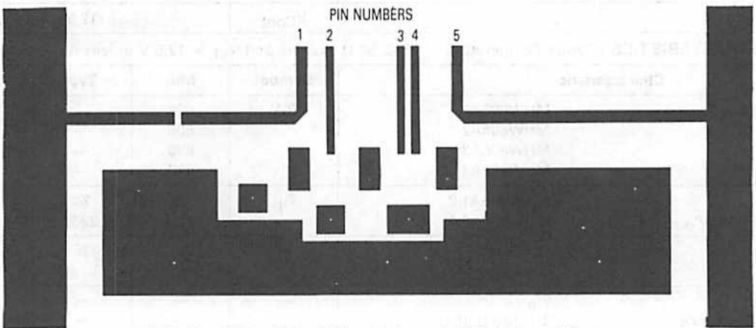


NOTE: The Printed Circuit Board shown is 75% of the original.

Figure 15. Photomaster For Test Fixture

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

5

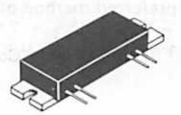
MHW806A SERIES

The RF Line
UHF Power Amplifiers

... designed for 12.5 Volt UHF power amplifier applications in industrial and commercial FM equipment operating from 806 to 950 MHz.

- MHW806A1 820–850 MHz
  MHW806A2 806–870 MHz
  MHW806A3 890–915 MHz
  MHW806A4 870–950 MHz
- Specified 12.5 Volt, UHF Characteristics
  Output Power = 6 Watts
  Minimum Gain = 23 dB (MHW806A1,2)
  = 21.7 dB (MHW806A3,4)
  Harmonics = −42 dBc Max ($2f_o$)
  = −60 dBc Max ($3f_o$ and Higher)
- 50 Ω Input/Output Impedances
- Guaranteed Stability and Ruggedness
- Features Three Common-Emitter Gain Stages
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability
- Gold-Metallized and Silicon Nitride-Passivated Transistor Chips
- Controllable, Stable Performance Over More Than 35 dB Range in Output Power

HIGH GAIN RF POWER AMPLIFIERS
6 WATTS
806–950 MHz



CASE 301H-03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{S1}	16	Vdc
RF Input Power	P_{in}	80	mW
RF Output Power	P_{out}	7.5	W
Storage Temperature Range	T_{stg}	−30 to +100	°C
Operating Case Temperature Range	T_C	−30 to +100	°C
DC Control Voltage	V_{Cont}	12.5	Vdc

ELECTRICAL CHARACTERISTICS (Flange Temperature = 25°C, 50 Ω system, and V_{S1} = 12.5 V unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range	MHW806A1 MHW806A2 MHW806A3 MHW806A4	BW	820 806 890 870	— — — —	850 870 915 950	MHz
Power Gain (V_{Cont} = 12.5 Vdc, P_{out} = 6 W)	MHW806A1,2 MHW806A3,4	G_p	23 21.7	24 22.7	— —	dB
Efficiency (1) (P_{out} = 6 W)		η	30	35	—	%
Harmonic Output (1) (P_{out} = 6 W Reference)	$2f_o$ $3f_o$ and Higher	—	— —	— —	−42 −60	dBc
Input VSWR (1) (P_{out} = 6 W, 50 Ω Reference, Reflected Signal Filtered to Eliminate Harmonic Content)		—	—	—	2:1	—

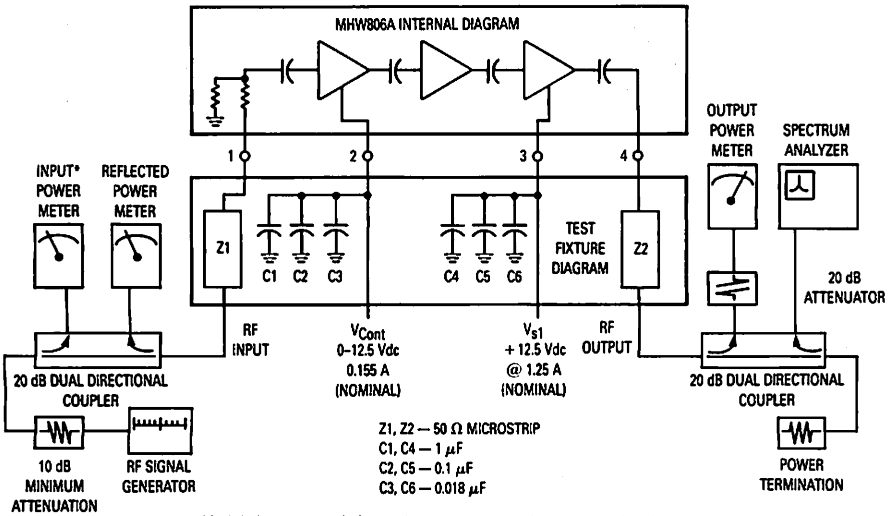
(1) P_{in} = 30 mW (MHW806A1,2) or P_{in} = 40 mW (MHW806A3,4), adjust V_{Cont} for specified P_{out}.

(continued)

ELECTRICAL CHARACTERISTICS — continued
(Flange Temperature = 25°C, 50 Ω system, and V_{S1} = 12.5 V unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Power Degradation (−30 to +80°C) (1) (Reference P_{out} = 6 W @ T_C = 25°C)		—	—	—	1.7	dB
Load Mismatch Stress (1) (V_{S1} = 16 Vdc, P_{out} = 7.5 W, VSWR = 30:1, all phase angles)		—	No degradation in Power Output			
Stability (P_{in} = 0 to 30 mW, [MHW806A1,2] or 0 to 40 mW [MHW806A3,4], V_{S1} = 10 to 16 Vdc, V_{Cont} = 0 to 12.5 Vdc, Load VSWR = 4:1, P_{out} Max = 7.5 W) (2)			All spurious outputs ≥70 dB below desired output signal level			
Quiescent Current @ V_{S1} = 12.5 V, V_{Cont} = 0 V (I_{Cont} with no RF drive applied)		$I_{S1(q)}$	—	—	1	mA
Control Voltage	P_{in} = 30 mW (MHW806A1,2), P_{in} = 40 mW (MHW806A3,4)	V_{Cont}	0	9	12.5	Vdc
Control Current	P_{out} = 6 W V_{Cont} = 12.5 V	I_{Cont}	0	155	225	mA

(1) P_{in} = 30 mW (MHW806A1,2) or P_{in} = 40 mW (MHW806A3,4) adjust V_{Cont} for specified P_{out}.
(2) Combination of P_{in}, V_{S1}, and V_{Cont} can not exceed max P_{out} = 7.5 W.



*Module input power is forward power as sampled by the directional coupler and read on the input power meter.

Figure 1. UHF Power Amplifier Test System Diagram

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MHW806A1, A2

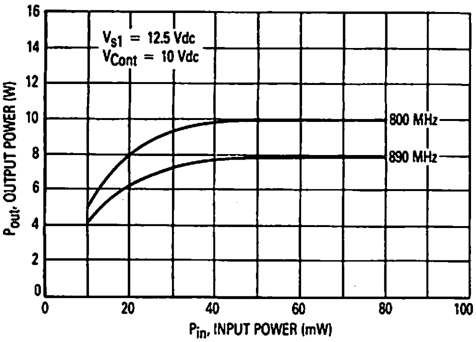

Figure 2. Output Power versus Input Power

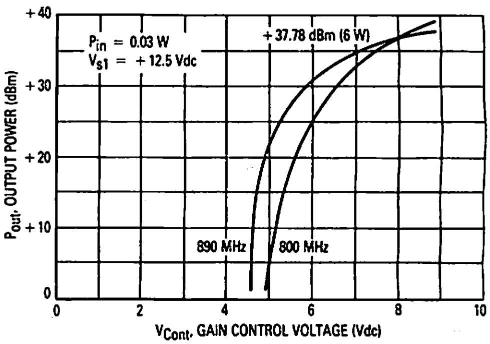

Figure 3. Output Power versus Gain Control Voltage

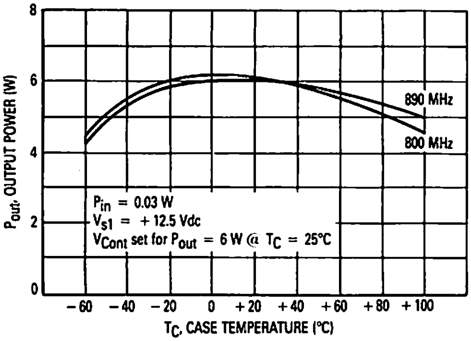

Figure 4. Output Power versus Case Temperature

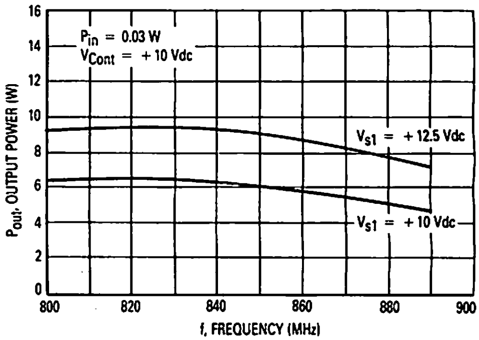

Figure 5. Output Power versus Frequency

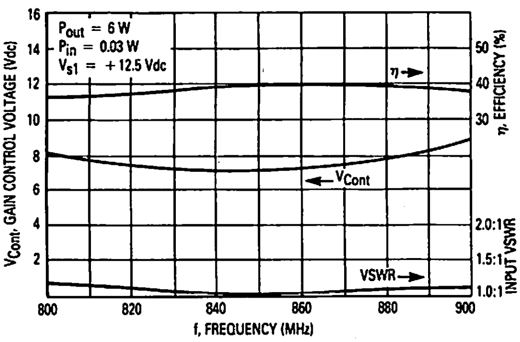

Figure 6. Gain Control Voltage, Input VSWR, Efficiency versus Frequency

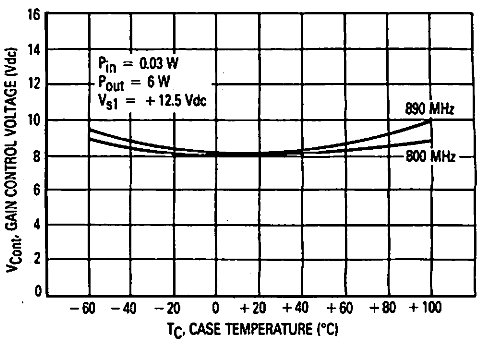

Figure 7. Gain Control Voltage versus Case Temperature

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MHW806A3, A4

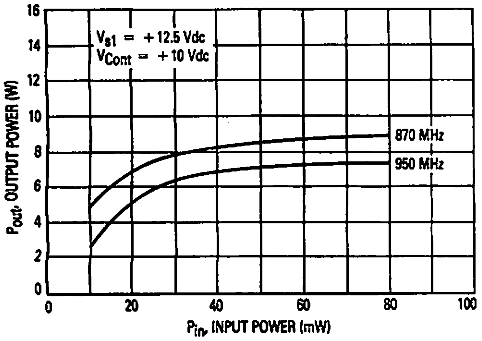


Figure 8. Output Power versus Input Power

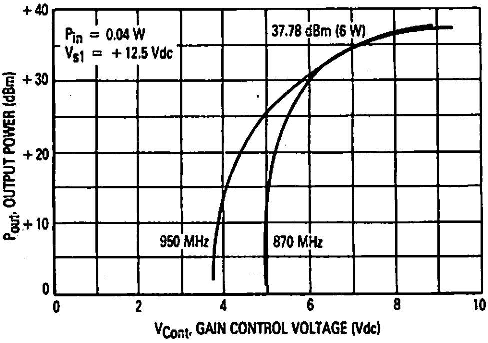


Figure 9. Output Power versus Gain Control Voltage

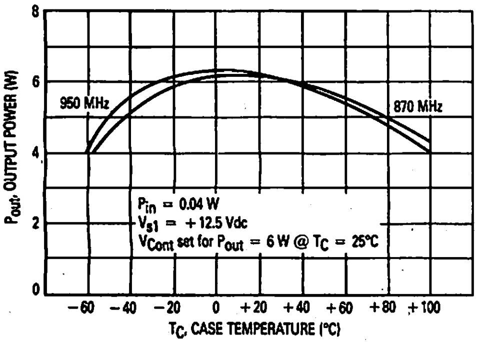


Figure 10. Output Power versus Case Temperature

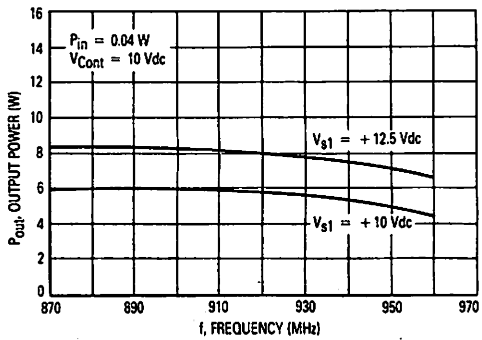


Figure 11. Output Power versus Frequency

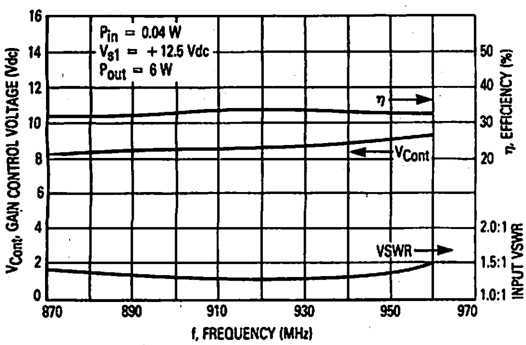


Figure 12. Gain Control Voltage, Input VSWR, Efficiency versus Frequency

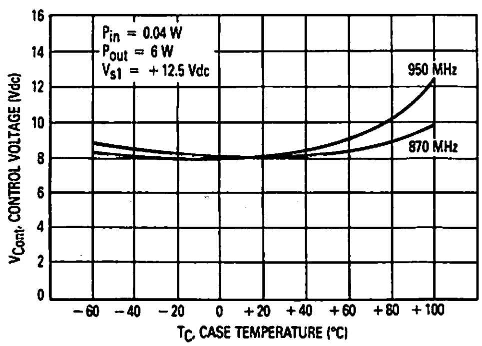


Figure 13. Gain Control Voltage versus Case Temperature

APPLICATIONS INFORMATION

Nominal Operation

All electrical specifications are based on the following nominal conditions: (P_{out} = 6 W, V_{S1} = 12.5 Vdc). This module is designed to have excess gain margin with ruggedness, but operation outside the limits of the published specifications is not recommended unless prior communications regarding the intended use have been made with a factory representative.

Gain Control

In general, the module output power should be limited to 7.5 watts. The preferred method of power output control is to fix V_{S1} at 12.5 volts, set RF drive level and vary the control voltage from 0 to 12.5 Volts. As designed, the module exhibits a gain control range greater than 35 dB using the method described above.

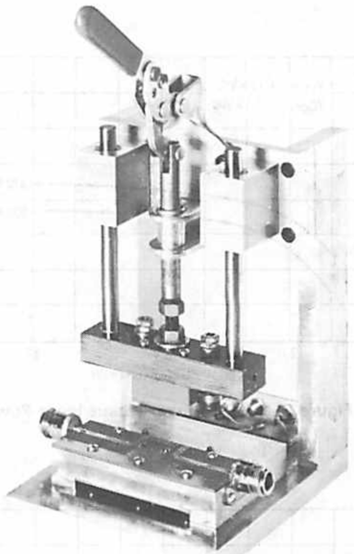
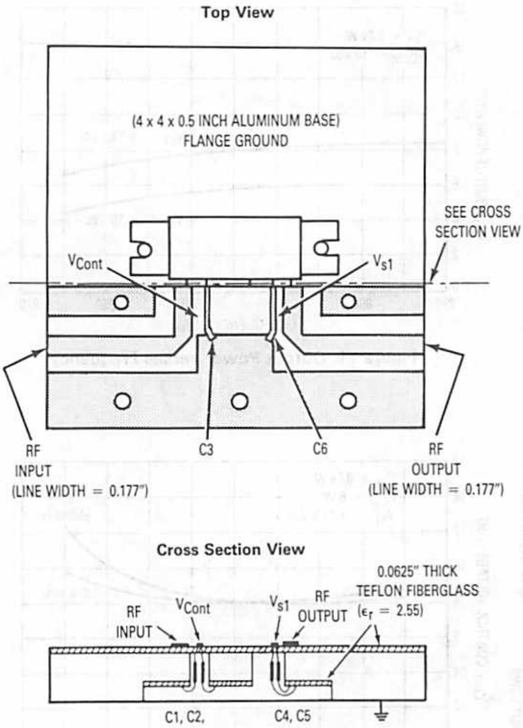


Figure 14. Test Fixture Assembly



Bring capacitor leads through fiberglass board and solder to V_{S1} and V_{Cont} lines as close to module as possible.

Figure 15. Test Fixture Construction

Decoupling

Due to the high gain of each of the three stages and the module size limitation, external decoupling networks require careful consideration. Both Pins 2 and 3 are internally bypassed with a 0.018 μF chip capacitor which is effective for frequencies from 5 MHz through 960 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in the test fixture schematic are recommended. Inadequate decoupling will result in spurious outputs at specific operating frequencies and phase angles of input and output VSWR.

Load Mismatch Stress

During final test, each module is load mismatch stress tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_{S1} equal to 16 volts, load VSWR 30:1 and output power equal to 7.5 watts.

Mounting Considerations

To insure optimum heat transfer from the flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicone thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.0015 inch. For more information on module mounting, see EB-107.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

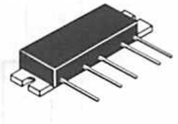
The RF Line
UHF Power Amplifiers

MHW807 Series

. . . designed specifically for mobile cellular radio applications. The MHW807 Series amplifiers are capable of wide power range control, operate from a 12 volt supply and require only 1.0 mW of RF input power.

- MHW807-1 820 to 850 MHz
  MHW807-2 870 to 905 MHz
- Specified 12.5 Volt Characteristics:
  RF Input Power — 1.0 mW (0 dBm)
  RF Output Power — 6.0 W
  Minimum Gain — 37.8 dB
  Harmonics — −25 dBc Max @ 2.0 f_o
  −45 dBc Max @ 3.0 f_o
- 50 Ohm Input/Output Impedances
- Guaranteed Stability and Ruggedness
- Controllable, Stable Performance Over More Than 35 dB Range in Output Power
- Gold-Metallized and Silicon Nitride-Passivated Transistor Chips

6.0 W — 820 to 905 MHz
HIGH GAIN
RF POWER AMPLIFIERS



CASE 301L-02, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{s1} V_{s3}	9.0 16	Vdc
RF Input Power	P_{in}	3.0	mW
RF Output Power	P_{out}	7.5	W
Operating Case Temperature Range	T_C	−30 to +100	°C
Storage Temperature Range	T_{stg}	−30 to +100	°C
DC Control Voltage	V_{Cont}	9.0	Vdc

ELECTRICAL CHARACTERISTICS (T_C = +25°C, 50 ohm system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range MHW807-1 MHW807-2	BW	820 870	— —	850 905	MHz
Power Gain (1) (V_{s1} = 8.0 Vdc; V_{s3} = 12.5 Vdc)	G_p	37.8	38.5	—	dB
Efficiency (1) (V_{s1} = 8.0 Vdc; V_{s3} = 12.5 Vdc; P_{out} = 6.0 W)	η	35	38	—	%
Harmonic Output (1) (P_{out} = 6.0 W Reference) 2.0 f_o 3.0 f_o	—	— —	— —	−25 −45	dBc
Input VSWR (1) (P_{out} = 6.0 W, Harmonics Filtered From P_{ref})	$VSWR_{in}$	—	—	2.5:1	—
Power Slump at Decreased Voltage (1) (T_C = 80°C) (V_{s1} = 8.0 Vdc, V_{s3} = 10 Vdc, V_{Cont} = 0 to 9.0 Vdc)	—	3.0	—	—	W
Load Mismatch Stress (1) (V_{s1} = 8.0 Vdc, V_{s3} = 16 Vdc, P_{out} = 7.0 W)	ψ	No Degradation in Output Power			
Stability (2) (V_{s1} = 8.0 Vdc, V_{s3} = 10 to 16 Vdc; P_{in} = 0.5 to 2.0 mW; P_{out} (Max) = 7.5 W; Load VSWR = 4:1, All Phase Angles	—	All spurious outputs more than 60 dB below desired signal			
Quiescent Current (I_{s3} With No Drive Applied) (V_{s3} = 12.5 Vdc; V_{s1} = V_{Cont} = 0 Vdc)	I_{s3}	—	—	1.0	mA
Control Voltage Slope (V_{s1} = 8.0 Vdc, V_{s3} = 12.5 Vdc, V_{Cont} = 0 to 9.0 Vdc, P_{in} = 1.0 mW)	—	—	—	5.0	mV/dB

(1) P_{in} = 1.0 mW. Adjust V_{Cont} for specified P_{out}.
(2) Combination of P_{in}, V_{s1} and V_{Cont} cannot exceed max P_{out} = 7.5 W.

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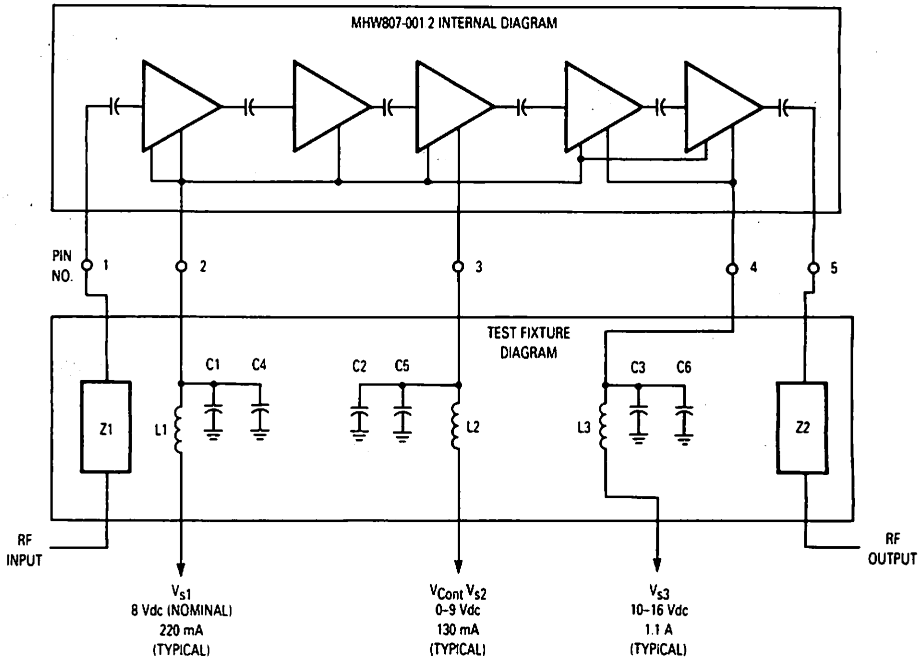

C1, C2, C3 = 0.018 μF CHIP
C4, C5, C6 = 2.2 μF TANTALUM
L1, L2 = 0.29 μH
L3 = 0.2 μH
Z1, Z2 = 50 Ω MICROSTRIP

Figure 1. UHF Power Module Test System Diagram

TYPICAL CHARACTERISTICS
(MHW807-1)

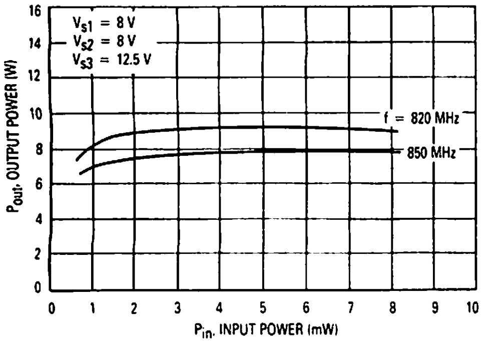

Figure 2. Output Power versus Input Power

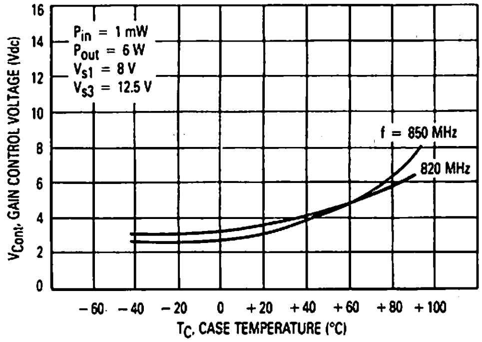

Figure 3. Gain Control Voltage versus Case Temperature

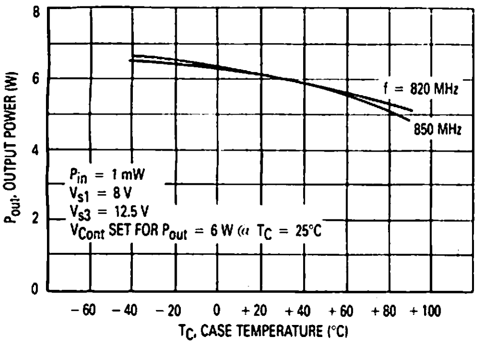

Figure 4. Output Power versus Case Temperature

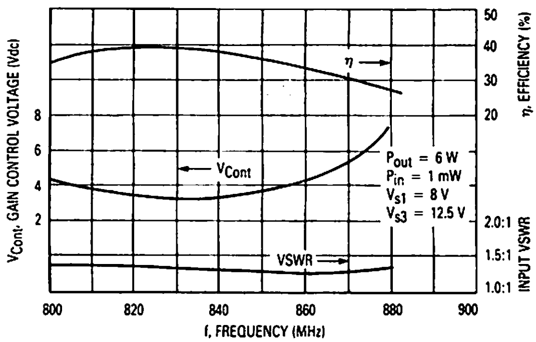

Figure 5. Gain Control Voltage, Input VSWR, Efficiency versus Frequency

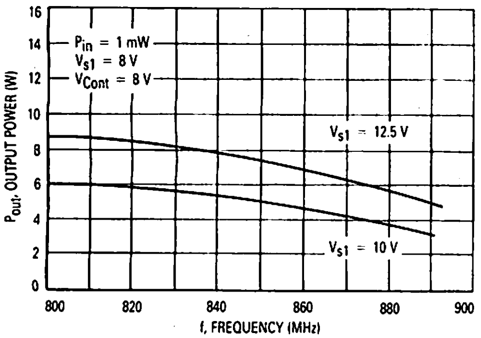

Figure 6. Output Power versus Frequency

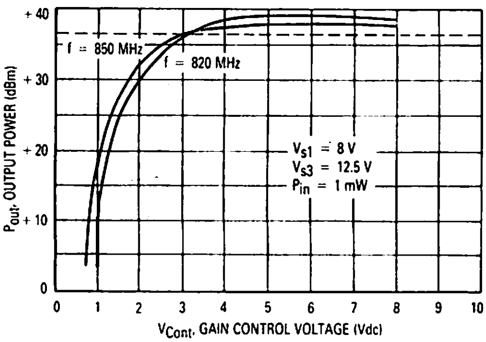

Figure 7. Output Power versus Gain Control Voltage

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TYPICAL CHARACTERISTICS
(MHW807-2)

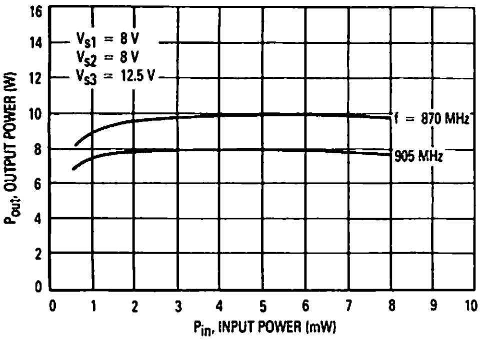

Figure 8. Output Power versus Input Power

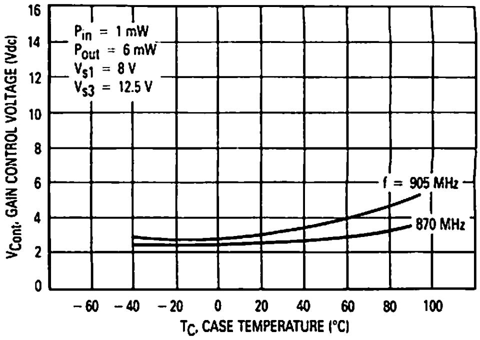

Figure 9. Gain Control Voltage versus Case Temperature

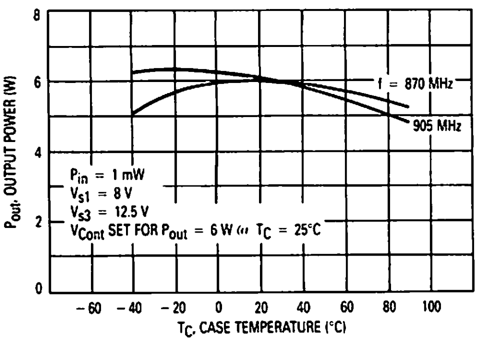

Figure 10. Output Power versus Case Temperature

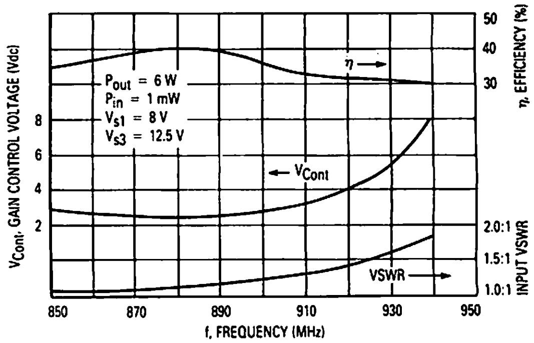

Figure 11. Gain Control Voltage, Input VSWR, Efficiency versus Frequency

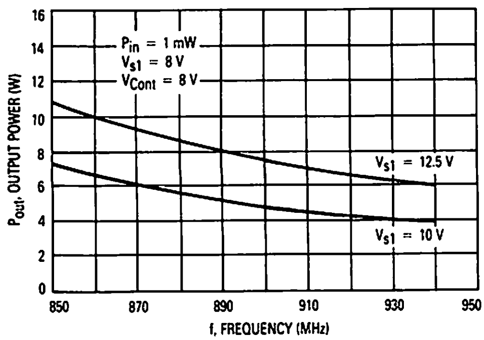

Figure 12. Output Power versus Frequency

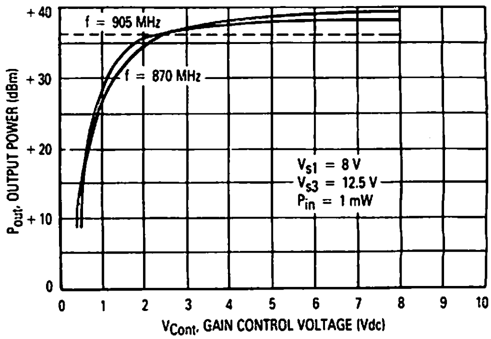

Figure 13. Output Power versus Gain Control Voltage

APPLICATIONS INFORMATION

NOMINAL OPERATION

All electrical specifications are based on the following nominal conditions: (P_{out} = 6.0 W, V_{S1} = 8.0 Vdc, V_{Cont} = 0–9.0 Vdc, V_{S3} = 12.5 Vdc, T_C = 25°C). This module is designed to have excess gain margin with ruggedness, but operation outside the limits of the published specifications is not recommended unless prior communications regarding the intended use have been made with a factory representative.

GAIN CONTROL

In general, the module output power should be limited to 7.5 watts. The preferred method of power output control is to fix V_{S3} at 12.5 Vdc, V_{S1} at 8.0 Vdc, set RF drive level to 0 dBm and vary the control voltage from 0 to 9.0 Volts. As designed, the module exhibits a gain control range greater than 35 dB using the method described above.

DECOUPLING

Due to the high gain of each of the five stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3 and 4 are internally bypassed with a 0.018 μF chip capacitor which is effective for frequencies from 5.0 MHz through 960 MHz. For bypassing frequencies below 5.0 MHz, networks equivalent to that shown in the test fixture schematic are recommended. Inadequate decoupling will result in spurious outputs at specific operating frequencies and phase angles of input and output VSWR.

LOAD MISMATCH STRESS

During final test, each module is load mismatch stress tested in a fixture having the identical decoupling networks described in Figure 1. Electrical conditions are V_{S3} = 16 volts, V_{S1} = 8.0 volts, output power equal to 7.0 watts, load VSWR greater than 30:1.

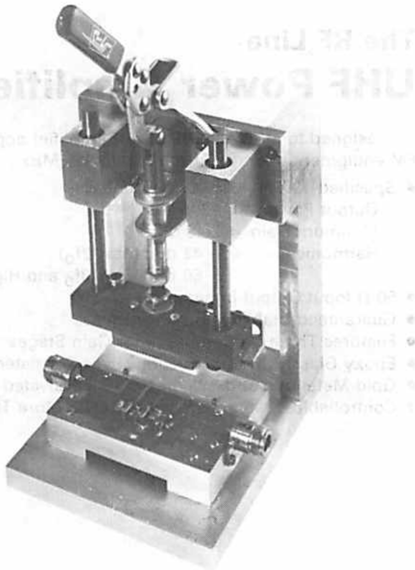

Figure 14. Test Fixture Assembly

MOUNTING CONSIDERATIONS

To insure optimum heat transfer from the flange to heatsink, use standard 4-40 mounting screws and an adequate quantity of silicone thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.0015 inch. For more information on module mounting, see EB107/D.

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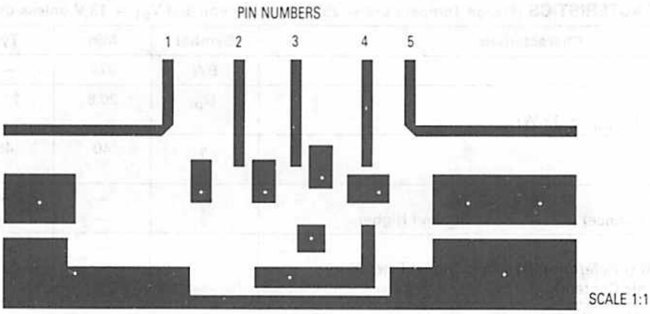


Figure 15. Photomaster For Test Fixture

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

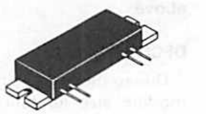
MHW812A3

The RF Line
UHF Power Amplifier

. . . designed for 13 Volt UHF power amplifier applications in industrial and commercial FM equipment operating from 890 to 915 MHz.

- Specified 13 Volt, UHF Characteristics
  - Output Power = 12 Watts
  - Minimum Gain = 20.8 dB
  - Harmonics = −42 dBc Max ($2f_o$)
  - −60 dBc Max ($3f_o$ and Higher)
- 50 Ω Input/Output Impedances
- Guaranteed Stability and Ruggedness
- Features Three Common-Emitter Gain Stages
- Epoxy Glass PCB Construction Gives Consistent Performance and Reliability
- Gold-Metallized and Silicon Nitride-Passivated Transistor Chips
- Controllable, Stable Performance Over More Than 35 dB Range in Output Power

HIGH GAIN RF POWER AMPLIFIERS
12 WATTS
890–915 MHz



CASE 301H-03, STYLE 2

5

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{S1}	16	Vdc
RF Input Power	P_{in}	200	mW
RF Output Power	P_{out}	15	W
Storage Temperature Range	T_{stg}	−30 to +100	°C
Operating Case Temperature Range	T_C	−30 to +100	°C
DC Control Voltage	V_{Cont}	12.5	Vdc

ELECTRICAL CHARACTERISTICS (Flange Temperature = 25°C, 50 Ω system, and V_{S1} = 13 V unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	870	—	950	MHz
Power Gain (V_{Cont} = 12.5 Vdc, P_{out} = 12 W)	G_p	20.8	21.5	—	dB
Efficiency (1) (P_{out} = 12 W)	η	40	45	—	%
Harmonic Output (1) (P_{out} = 12 W Reference) $2f_o$ / $3f_o$ and Higher	—	— / —	— / —	−42 / −60	dBc
Input VSWR (1) (P_{out} = 12 W, 50 Ω Reference, Reflected Signal Filtered to Eliminate Harmonic Content)	—	—	—	2:1	—

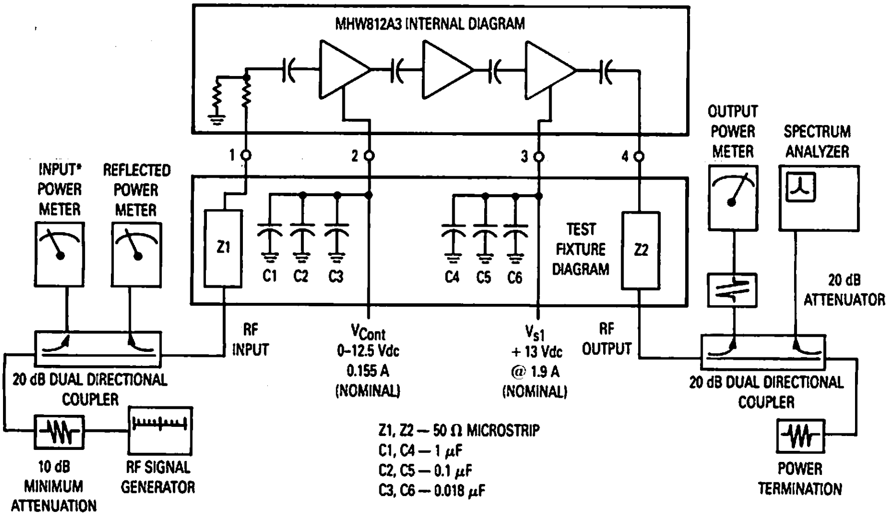
(1) P_{in} = 100 mW; adjust V_{Cont} for specified P_{out}.

(continued)

ELECTRICAL CHARACTERISTICS — continued
(Flange Temperature = 25°C, 50 Ω system, and V_{S1} = 13 V unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Power Degradation (−30 to +80°C) (1) (Reference P_{out} = 12 W @ T_C = 25°C)		—	—	—	1.7	dB
Load Mismatch Stress (1) (V_{S1} = 16 Vdc, P_{out} = 13 W, VSWR = 30:1, all phase angles)		—	No degradation in Power Output			
Stability (P_{in} = 0 to 200 mW, V_{S1} = 10 to 16 Vdc, V_{Cont} = 0 to 12.5 Vdc, Load VSWR = 4:1, P_{out} Max = 13 W) (2)			All spurious outputs ≥70 dB below desired output signal level			
Quiescent Current @ V_{Cont} = 12.5 V (I_{Cont} with no RF drive applied)		I_{Cont}	—	—	225	mA
Control Voltage	P_{in} = 100 mW	V_{Cont}	0	9	12.5	Vdc
Control Current	P_{out} = 12 W V_{Cont} = 12.5 V	I_{Cont}	0	155	225	mA

(1) P_{in} = 100 mW; adjust V_{Cont} for specified P_{out}.
(2) Combination of P_{in}, V_{S1}, and V_{Cont} can not exceed max P_{out} = 15 W.



*Module input power is forward power as sampled by the directional coupler and read on the input power meter.

Figure 1. UHF Power Amplifier Test System Diagram

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TYPICAL CHARACTERISTICS

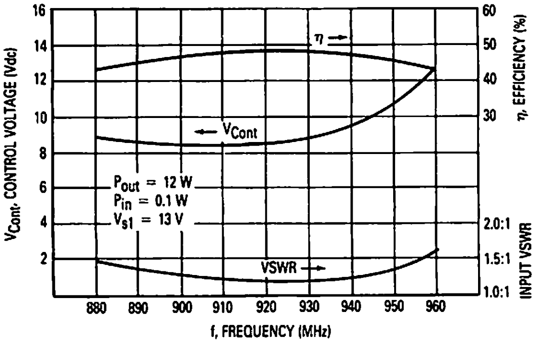


Figure 2. Control Voltage, Efficiency and VSWR versus Frequency

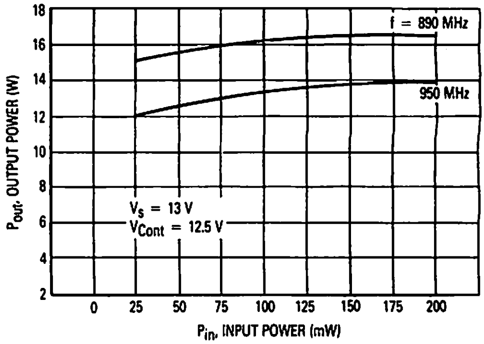


Figure 3. Output Power versus Input Power

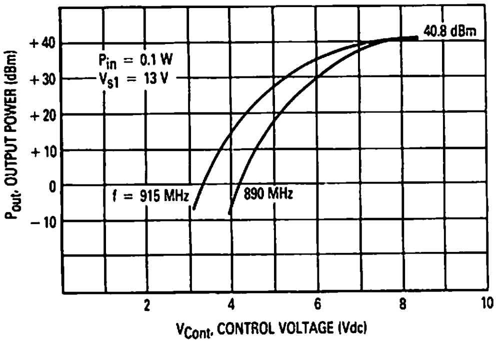


Figure 4. Output Power versus Control Voltage

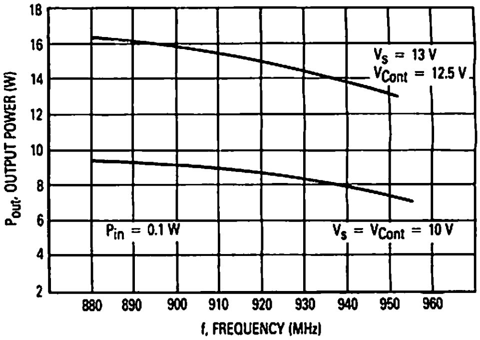


Figure 5. Output Power versus Frequency

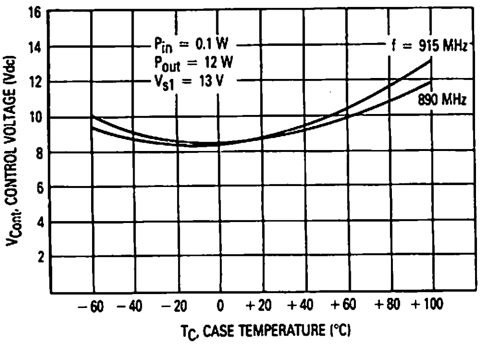


Figure 6. Control Voltage versus Case Temperature

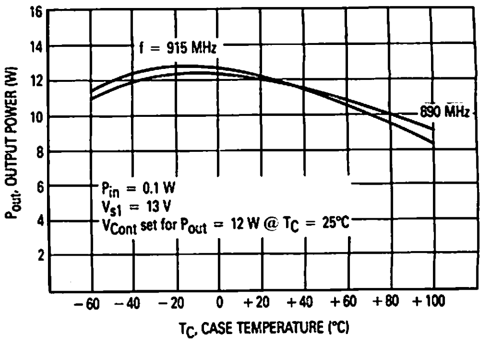


Figure 7. Output Power versus Case Temperature

5

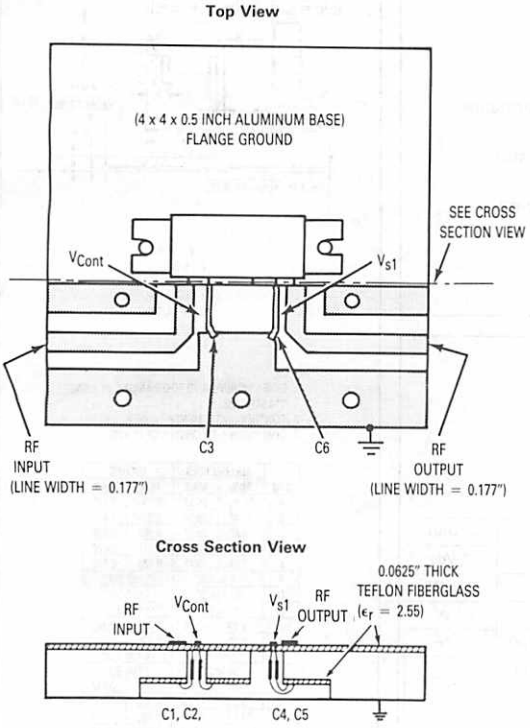
APPLICATIONS INFORMATION

Nominal Operation

All electrical specifications are based on the following nominal conditions: (P_{out} = 12 W, V_{S1} = 13 Vdc). This module is designed to have excess gain margin with ruggedness, but operation outside the limits of the published specifications is not recommended unless prior communications regarding the intended use have been made with a factory representative.

Gain Control

In general, the module output power should be limited to 13 watts. The preferred method of power output control is to fix V_{S1} at 13 volts, set RF drive level and vary the control voltage from 0 to 12.5 Volts. As designed, the module exhibits a gain control range greater than 35 dB using the method described above.



Bring capacitor leads through fiberglass board and solder to V_{S1} and V_{Cont} lines as close to module as possible.

Figure 9. Test Fixture Construction

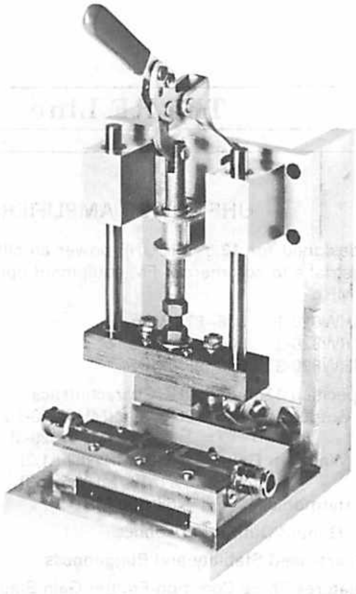


Figure 8. Test Fixture Assembly

Decoupling

Due to the high gain of each of the three stages and the module size limitation, external decoupling networks require careful consideration. Both Pins 2 and 3 are internally bypassed with a 0.018 μF chip capacitor which is effective for frequencies from 5 MHz through 960 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in the test fixture schematic are recommended. Inadequate decoupling will result in spurious outputs at specific operating frequencies and phase angles of input and output VSWR.

Load Mismatch Stress

During final test, each module is load mismatch stress tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_{S1} equal to 16 volts, load VSWR 30:1 and output power equal to 13 watts.

Mounting Considerations

To insure optimum heat transfer from the flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicone thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.0015 inch. For more information on module mounting, see EB-107.

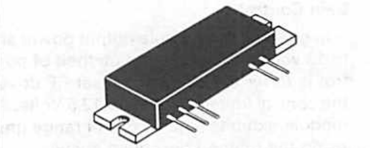
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW820-1
MHW820-2
MHW820-3

The RF Line

18/20 W — 806–950 MHz

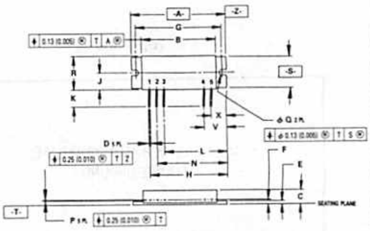
RF POWER AMPLIFIERS



UHF POWER AMPLIFIERS

. . . designed for 12.5 volt UHF power amplifier applications in industrial and commercial FM equipment operating from 806 to 950 MHz.

- MHW820-1 806–870 MHz
  MHW820-2 806–890 MHz
  MHW820-3 870–950 MHz
- Specified 12.5 Volt, UHF Characteristics
  Output Power = 20 Watts (MHW820-1,2)
  = 18 Watts (MHW820-3)
  Minimum Gain = 19 dB (MHW820-1,2)
  = 17.1 dB (MHW820-3)
  Harmonics = −58 dBc Max
- 50 Ω Input/Output Impedances
- Guaranteed Stability and Ruggedness
- Features Three Common-Emitter Gain Stages
- Thin-Film Hybrid Construction Gives Consistent Performance and Reliability
- Gold-Metallized and Silicon Nitride-Passivated Transistor Chips
- Controllable, Stable Performance Over More Than 30 dB Range in Output Power



STYLE 1:
PIN 1. RF INPUT
2. +DC
3. +DC
4. +DC
5. RF OUTPUT

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION F TO CENTER OF LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	55.63	56.13	2.190	2.210
B	35.44	35.94	1.395	1.415
C	8.89	9.55	0.350	0.376
D	0.46	0.55	0.018	0.022
E	3.05	3.42	0.120	0.135
F	4.06 BSC		0.160 BSC	
G	48.26 BSC		1.900 BSC	
H	40.64 BSC		1.600 BSC	
J	8.77	9.77	0.345	0.385
K	5.72	—	0.225	—
L	35.56 BSC		1.400 BSC	
N	38.10 BSC		1.500 BSC	
P	0.21	0.30	0.008	0.012
Q	3.81	4.06	0.150	0.160
R	17.53	19.55	0.690	0.770
S	15.12	15.49	0.595	0.610
V	17.78 BSC		0.700 BSC	
X	12.70 BSC		0.500 BSC	

CASE 301G-03

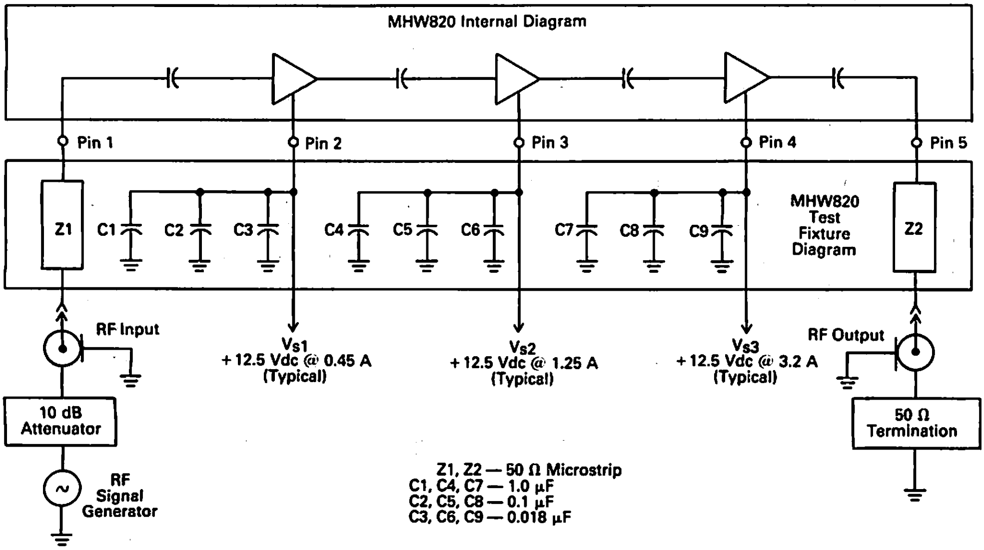
MAXIMUM RATINGS (Flange Temperature = 25°C)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{S1}, V_{S2}, V_{S3}	16	Vdc
RF Input Power ($P_{out} \leq 25$ W)	P_{in}	400	mW
RF Output Power ($P_{in} \leq 400$ mW)	P_{out}	25	W
Storage Temperature Range	T_{stg}	-30 to +100	°C
Operating Case Temperature Range	T_C	-40 to +100	°C

ELECTRICAL CHARACTERISTICS (Flange Temperature = 25°C, 50 Ω system, and $V_{S1} = V_{S2} = 12.5$ V unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range	MHW820-1 MHW820-2 MHW820-3	BW	806 806 870	— — —	870 890 950	MHz
Input Power (P_{out} = 20 W) (P_{out} = 18 W)	MHW820-1, 2 MHW820-3	P_{in}	— —	200 300	250 350	mW
Power Gain (P_{out} = 20 W) (P_{out} = 18 W)	MHW820-1, 2 MHW820-3	G_p	19 17.1	20 17.8	— —	dB
Efficiency (P_{out} = 20 W) (P_{out} = 18 W)	MHW820-1, 2 MHW820-3	η	28 26	32 30	—	%
Harmonic Output (P_{out} Reference = Rated P_{out})		—	—	—	−58	dBc
Input VSWR (P_{out} = Rated P_{out}, 50 Ω Reference)		—	—	—	2:1	—
Power Degradation (−30 to +80°C) (Reference P_{out} = Rated P_{out} @ T_C = 25°C)		—	—	1.2	1.7	dB
Load Mismatch Stress ($V_{S1} = V_{S2} = V_{S3}$ = 16 Vdc, P_{out} = 25 W, VSWR = 30:1, all phase angles)		—	No degradation in Power Output			
Stability (P_{in} = 0 to 250 mW, [MHW820-1, 2] or 350 mW [MHW820-3] consistent with max, P_{out} = 25 W, V_{S1} = V_{S2} = V_{S3} = 10 to 16 Vdc, Load VSWR = 4:1)		All non-harmonic related spurious outputs ≥ 70 dB below the desired output signal level				
Quiescent Current (I_{S1} with no RF drive applied)		$I_{S1(q)}$	—	—	125	mA

FIGURE 1 — 806-950 MHz TEST SYSTEM DIAGRAM



TYPICAL PERFORMANCE CURVES (MHW820-1, 2)

FIGURE 2 — INPUT POWER, EFFICIENCY AND VSWR versus FREQUENCY

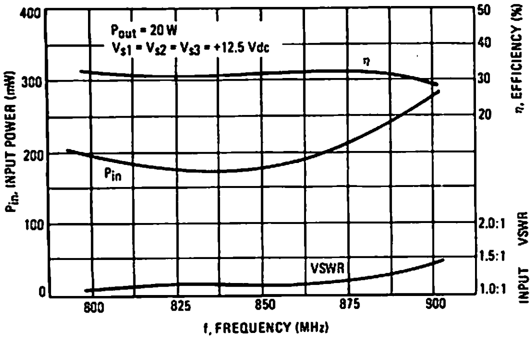


FIGURE 3 — OUTPUT POWER versus INPUT POWER

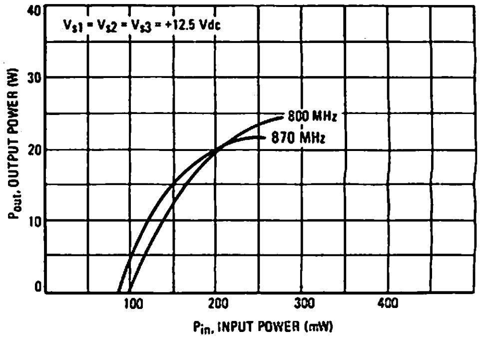


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE

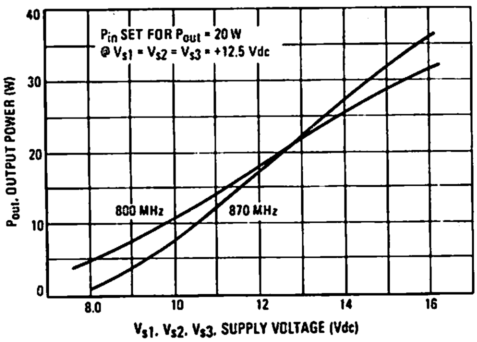


FIGURE 5 — EFFICIENCY versus SUPPLY VOLTAGE

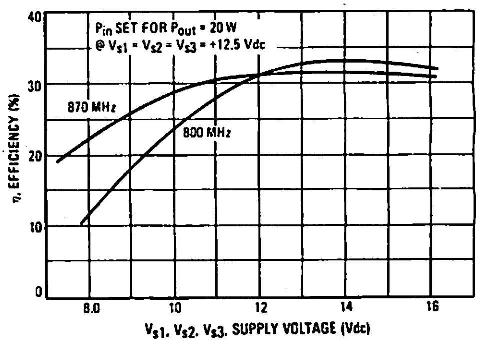


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FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE TO FIRST STAGE (V_{s1})

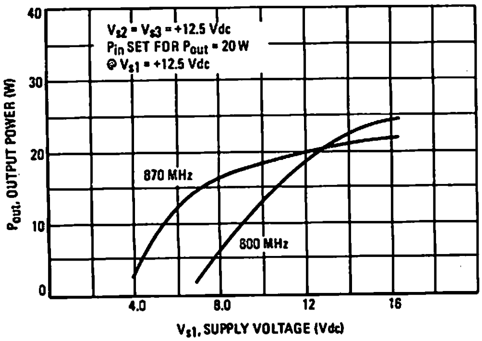
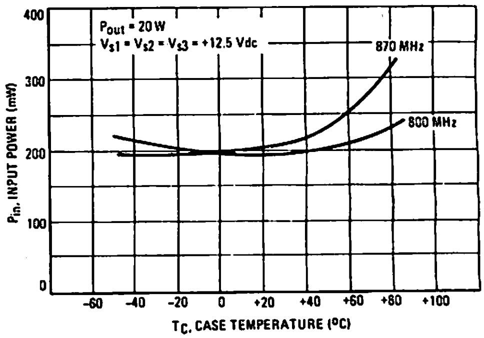


FIGURE 7 — INPUT POWER versus CASE TEMPERATURE



TYPICAL PERFORMANCE CURVES
(MHW820-3)

FIGURE 8 — INPUT POWER, EFFICIENCY AND VSWR versus FREQUENCY

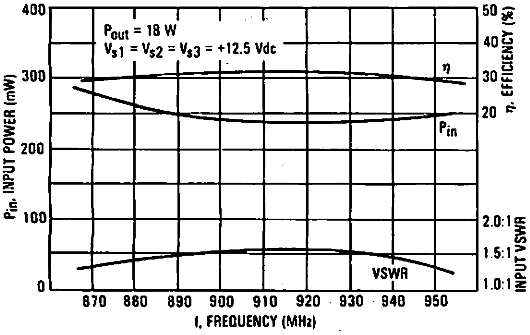


FIGURE 9 — OUTPUT POWER versus INPUT POWER

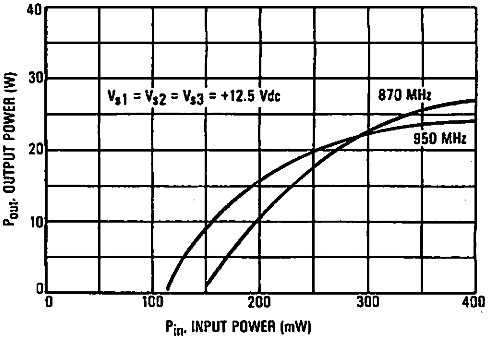


FIGURE 10 — OUTPUT POWER versus SUPPLY VOLTAGE

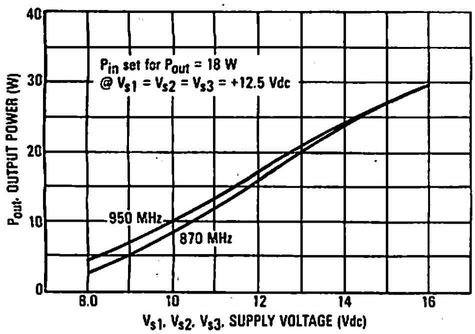
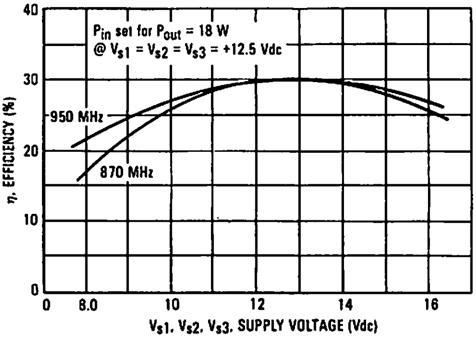


FIGURE 11 — EFFICIENCY versus SUPPLY VOLTAGE



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APPLICATIONS INFORMATION

Nominal Operation

All electrical specifications are based on the following nominal conditions: (P_{out} = Rated, $V_{S1} = V_{S2} = V_{S3}$ = 12.5 Vdc). This module is designed to have excess gain margin with ruggedness, but operation outside the limits of the published specifications is not recommended unless prior communications regarding the intended use has been made with a factory representative.

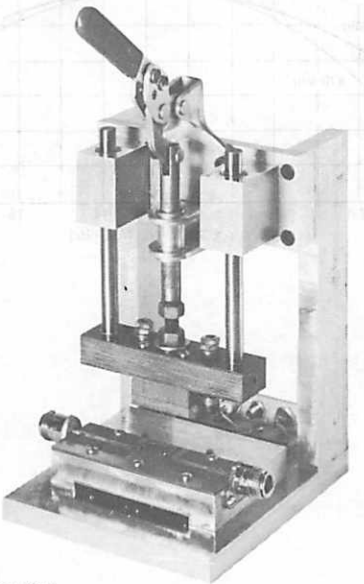
Gain Control

This module is designed for wide range P_{out} level control. The recommended method of power output control, as shown in Figure 3 and 9, is to fix V_{S1}, V_{S2}, and V_{S3} at 12.5 Vdc and vary the input RF drive level at Pin 1.

A second method of output control is to adjust the supply voltage (V_{S1} independently or V_{S1}, V_{S2}, and V_{S3} simultaneously). However, if any of these voltages fall out of the range from 10 to 16 volts module stability cannot be guaranteed. Typical ranges of power output control using this method are shown in Figures 4, 6, and 10.

In all applications, the module output power should be limited to 25 watts.

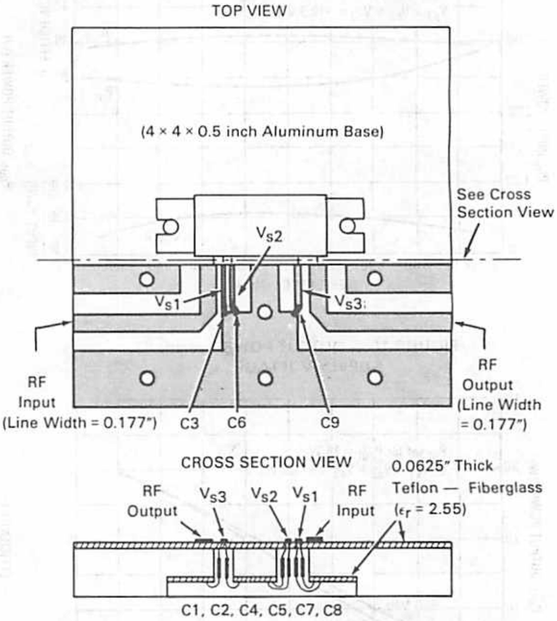
FIGURE 12 — TEST FIXTURE ASSEMBLY



Decoupling

Due to the high gain of each of the two stages and the module size limitation, external decoupling networks require careful consideration. Pins 2, 3 and 4 are internally bypassed with 0.018 μF chip capacitors which are effective for frequencies from 5 MHz through 950 MHz. For bypassing frequencies below 5 MHz, networks equivalent to that shown in the test fixture schematic are recommended. Inadequate decoupling will result in spurious outputs at specific operating frequencies and phase angles of input and output VSWR.

FIGURE 13 — TEST FIXTURE CONSTRUCTION



Bring capacitor leads through fiberglass board and solder to V_{S1}, V_{S2}, and V_{S3} lines as close to module as possible.
To insure optimum heat transfer from flange to heatsink, use standard 6-32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4-6 inch pounds.

Load Pull

During final test, each module is "load pull" tested in a fixture having the identical decoupling network described in Figure 1. Electrical conditions are V_{S1}, V_{S2} and V_{S3} equal to 16 volts output, VSWR 30:1 and output power equal to 25 watts.

Mounting Considerations

To insure optimum heat transfer from the flange to heatsink, use standard 6–32 mounting screws and an adequate quantity of silicon thermal compound (e.g., Dow Corning 340). With both mounting screws finger tight, alternately torque down the screws to 4–6 inch pounds. The heatsink mounting surface directly beneath the module flange should be flat to within 0.002 inch to prevent fracturing of ceramic substrate material. For more information on module mounting, see EB-107.

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW1134
MHW1184
MHW1224
MHW1244

The RF Line

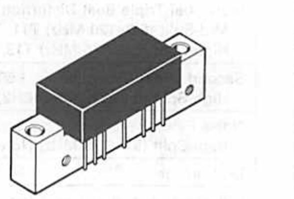
13.0 dB
18.5 dB
22.0 dB
24.0 dB

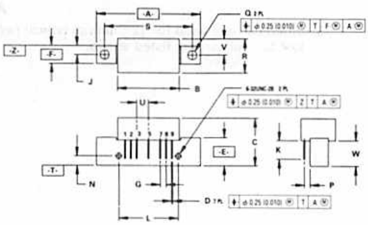
5.0–200 MHz
CATV HIGH-SPLIT
REVERSE AMPLIFIERS

LOW DISTORTION WIDEBAND AMPLIFIERS

. . . designed specifically for broadband applications requiring low distortion characteristics. Specified for use as return amplifiers for mid-split and high-split 2-way cable TV systems. Features all gold metallization system.

- Guaranteed Broadband Power Gain @ f = 5.0–200 MHz
- Guaranteed Broadband Noise Figure @ f = 5.0–175 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- All Ion-Implanted Arsenic Emitter Transistor Chips with 7.0 GHz f_T's
- Circuit Design Optimized for Good RF Stability Under High VSWR Load Conditions
- Transformers Designed to Insure Good Low Frequency Gain Stability versus Temperature





STYLE 1
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+65	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = + 30°C, 75 Ω system)

Characteristic	Symbol	MHW1134	MHW1184	MHW1224	MHW1244	Units
Power Gain @ 10 MHz	G_P	13.0±0.5	18.5±0.5	22.0±0.5	24.0±0.5	dB
Frequency Range (Response/Return Loss) Note 1	BW	5.0–200				MHz
Cable Slope Equivalent (5.0–200 MHz)	S	−0.2 Min/+0.8 Max				dB
Gain Flatness (5.0–200 MHz)	F	±0.2 Max				dB
Input/Output Return Loss (5.0–200 MHz) Note 1	IRL/ORL	18.0 Min				dB
Cross Modulation Distortion @ +50 dBmV per ch.						
12-Channel FLAT (5.0–120 MHz)	XM_{12}	−70 Typ	−68 Typ	−67 Typ	−66 Typ	dB
22-Channel FLAT (5.0–175 MHz) Notes 2 and 3	XM_{22}	−65 Max	−64 Max	−62 Max	−61 Max	dB
26-Channel FLAT (5.0–200 MHz)	XM_{26}	−65 Typ	−64 Typ	−62 Typ	−61 Typ	dB
Composite Triple Beat Distortion @ +50 dBmV per ch.						
22-Channel FLAT (5.0–175 MHz) Notes 2 and 3	CTB_{22}	−73 Max	−72 Max	−71 Max	−70 Max	dB
26-Channel FLAT (5.0–200 MHz) Notes 2 and 3	CTB_{26}	−71 Typ	−70 Typ	−68.5 Typ	−67.5 Typ	dB
Individual Triple Beat Distortion @ +50 dBmV per ch.						
Mid-Split (5.0–120 MHz) T11, T12 and CH2 @ 123.25 MHz	TB_3	−90 Typ	−88 Typ	−88 Typ	−87 Typ	dB
High-Split (5.0–175 MHz) T13, CH2 and CH5 @ 175.5 MHz	TB_3	−87 Typ	−85 Typ	−85 Typ	−84 Typ	dB
Second Order Distortion @ +50 dBmV per ch. High-Split (5.0–175 MHz) CH2, CHA @ 176.5 MHz	IMD	−72 Max	−72 Max	−72 Max	−72 Max	dB
Noise Figure High-Split (5.0–175 MHz) Note 2	NF	7.0 Max	5.5 Max	5.5 Max	5.0 Max	dB
DC Current	I_{DC}	210 Typ/240 Max				mAdc

1. Response and return loss characteristics are tested and guaranteed for the full 5.0–200 MHz frequency range.
2. Motorola 100% distortion and noise figure testing is performed over the 5.0–175 MHz frequency range. Cross modulation and composite triple beat testing are with 22-channel loading; Video carriers used are:

T7–T13	7.0–43.0 MHz	7-Channels
2–6	55.25–83.25 MHz	5-Channels
A–7	121.25–175.25 MHz	10-Channels

3. Video carriers used for 12-Channel typical performances are T7–6; For 26-Channel typical performance, Channels 8, 9, 10 and 11 are added to the 22-Channel carriers listed above.

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

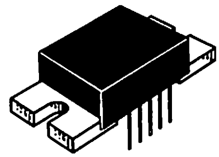
MHW2001-15

The RF Line
VHF Power Amplifier

. . . designed specifically for 15 volt Sonobouy applications in the frequency region of 135 to 175 MHz.

- Specified 15 Volt, VHF Characteristics:
  - Output Power — 1.0 Watt Min
  - Gain — 27 dB Min @ P_{in} = 2.0 mW
  - Harmonics — −38 dBc Max (2.0 f_o)
- 50 Ω Input/Output Impedances
- Guaranteed Stability and Ruggedness
- Automated Surface Mount Construction Gives Consistent Performance and Reliability
- Gain Control Pin for Manual or Automatic Output Level Control

27 dB
135–175 MHz
1.5 WATT
SONOBOUY
POWER AMPLIFIER



CASE 297C-02, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	18	Vdc
RF Input Power	P_{in}	8.0	mW
RF Output Power	P_{out}	2.0	W
Storage Temperature Range	T_{stg}	−40 to +80	°C
Operating Case Temperature	T_C	−20 to +80	°C

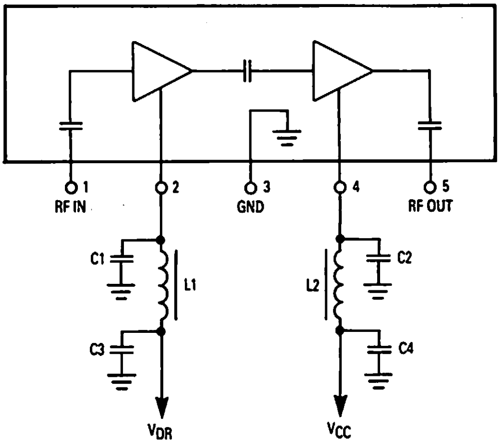
ELECTRICAL CHARACTERISTICS (V_{CC} = V_{DRIVE} = 15 V; Z_o = 50 Ω, T_C = 25°C. All characteristics guaranteed over bandwidth specified under "Frequency Range" unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	135	—	175	MHz
Gain @ P_{in} = 2.0 mW (Note 1)	G_p	27	29	33	dB
Input VSWR @ P_{in} = 2.0 mW	$VSWR_{in}$	—	—	2.5:1	—
Efficiency @ P_{in} = 2.0 mW	η	40	45	—	%
Harmonics @ P_o = 1.5 W	—	—	−45	−38	dBc
Stability @ P_{in} = 0 to 4.0 mW V_{CC} = V_{dr} = 12 to 16 V Source and Load VSWR = 4:1	—	All spurious outputs more than 60 dB below desired signal level			
Load Mismatch @ Load VSWR = 4:1 V_{CC} = V_{dr} = 16 V P_{out} = 1.5 W	—	No degradation in output power after return to initial operating conditions			
Standby Current @ P_{in} = 0 mW	I_s	—	47	55	mA

Note 1: Not designed for continuous operation. Duty cycle typical of Sonobuoy applications. Consult factory for other conditions of operation.

DECOUPLING

Pins 2 and 4 are internally bypassed with a 0.018 μF chip capacitor which is effective for frequencies from 5.0 MHz to 175 MHz. For bypassing frequencies below 5.0 MHz, networks equivalent to that shown in Figure 1 are recommended. Inadequate decoupling may result in spurious outputs at certain operating frequencies and certain phase angles of input and output VSWR.



L1 = L2 = 0.2 μH (ferrite loaded)
C1 = C2 = 0.1 μF
C3 = C4 = 1 μF Tantalum

Figure 1. Decoupling Networks

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

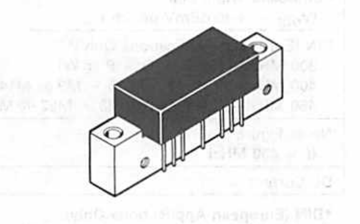
MHW5122A

The RF Line

12.5 dB GAIN

450 MHz

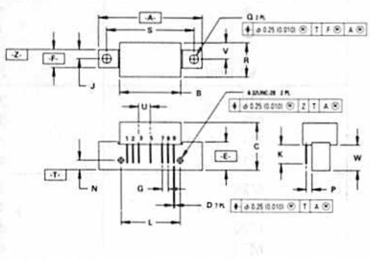
60-CHANNEL
CATV TRUNK AMPLIFIER



450 MHz CATV AMPLIFIER

. . . designed for broadband applications requiring low distortion characteristics. Specified for use as a CATV trunk-line amplifier. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T, and all an gold metallization system.

- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 12.5 dB (Typ)
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 12.5 dB (Typ)
- Broadband Noise Figure — @ f = 450 MHz
  NF = 7.0 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature



STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

5

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	12	12.5	13	dB
Slope		S	+0.2	+0.7	+1.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)			—	−78	—	
(V_{out} = +46 dBmV per ch., Ch2, M13, M22)			—	—	−72	
Cross Modulation Distortion	53-Channel FLAT	XMD_{53}	—	−63	—	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	XMD_{60}	—	−63	−61	
Composite Triple Beat	53-Channel FLAT	CTB_{53}	—	−63	—	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	CTB_{60}	—	−61	−58	
DIN (European Applications Only)*						dBμV**
300 MHz — (CH V + Q − P @ W)		DIN1	—	125	—	
400 MHz — (CH M8 + M15 − M9 @ M14)		DIN2	—	124	—	
450 MHz — (CH M20 + M23 − M22 @ M21)		DIN3	—	123	—	
Noise Figure (f = 450 MHz)		NF	—	7.0	8.0	dB
DC Current		I_{DC}	—	200	240	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ)	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+59	≤ −60
Q	259.25	+59	
V	289.25	+65	
W (Ref.)	295.25	+65	
M8	361.25	+58	≤ −60
M9	367.25	+58	
M14 (Ref.)	397.25	+64	
M15	403.25	+64	
M20	433.25	+63	≤ −60
M21 (Ref.)	439.25	+63	
M22	445.25	+57	
M23	451.25	+57	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW5141A
MHW5142A

The RF Line

450 MHz CATV AMPLIFIERS

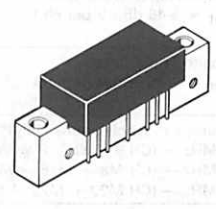
. . . designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

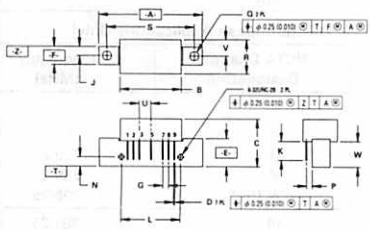
- Specified for 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 14 dB (Typ) @ 50 MHz
  14.5 dB (Min) @ 450 MHz
- Broadband Noise Figure @ 450 MHz
  NF = 7.0 dB (Max) MHW5141A
  7.0 dB (max) MHW5142A
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors

14 dB GAIN

450 MHz

60-CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIERS





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic	Symbol	MHW5141A Min	MHW5141A Typ	MHW5141A Max	MHW5142A Min	MHW5142A Typ	MHW5142A Max	Unit
Frequency Range	BW	40	—	450	40	—	450	MHz
Power Gain — 50 MHz	G_p	13.5	14	14.5	13.5	14	14.5	dB
Power Gain — 450 MHz	G_p	14.0	—	15.5	14.0	—	15.5	dB
Slope	S	0.2	—	1.5	0.2	—	1.5	dB
Gain Flatness (Peak To Valley)	—	—	0.2	0.4	—	0.2	0.4	dB
Return Loss — Input/Output 40–450 MHz (Z_o = 75 Ohms)	IRL/ORL	18	—	—	18	—	—	dB
Second Order Intermodulation Distortion	IMD							dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)		—	−78	—	—	−78	—	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)		—	—	−72	—	—	−74	
Cross Modulation Distortion								dB
(V_{out} = +46 dBmV per ch.) 53-Channel FLAT	XMD_{53}	—	−61	—	—	−63	—	
60-Channel FLAT	XMD_{60}	—	−60	−59	—	−63	−62	
Composite Triple Beat								dB
(V_{out} = +46 dBmV per ch.) 53-Channel FLAT	CTB_{53}	—	−61	—	—	−63	—	
60-Channel FLAT	CTB_{60}	—	−59	−58	—	−62	−61	
DIN (European Applications Only)*								dBμV**
300 MHz — (CH V + Q − P @ W)	DIN1	—	125	—	—	127	—	
400 MHz — (CH M8 + M15 − M9 @ M14)	DIN2	—	124	—	—	126	—	
450 MHz — (CH M20 + M23 − M22 @ M21)	DIN3	—	123	—	—	125	—	
Noise Figure (f = 450 MHz)	NF	—	—	7.0	—	6.0	7.0	dB
DC Current	I_{DC}	—	180	200	—	210	240	mA

*DIN (European Applications Only)

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ) MHW5181A	DIN Output Level (dBmV)**(Typ) MHW5182A	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+59	+61	≤ −60
Q	259.25	+59	+61	
V	289.25	+65	+67	
W (Ref.)	295.25	+65	+67	
M8	361.25	+58	+60	≤ −60
M9	367.25	+58	+60	
M14 (Ref.)	397.25	+64	+66	
M15	403.25	+64	+66	
M20	433.25	+63	+65	≤ −60
M21 (Ref.)	439.25	+63	+65	
M22	445.25	+57	+59	
M23	451.25	+57	+59	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW5162A

The RF Line

450 MHz CATV AMPLIFIER

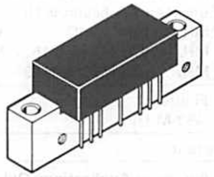
. . . designed for broadband applications requiring low-distortion characteristics. Specified for use as a CATV trunk-line amplifier. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

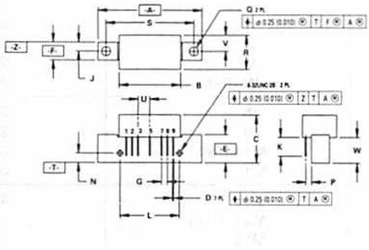
- *Specified for 53- and 60-Channel Performance*
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 16.4 dB (Typ)
- Broadband Noise Figure — @ f = 450 MHz
  NF = 6.5 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors

16.4 dB GAIN

450 MHz

60-CHANNEL CATV TRUNK AMPLIFIER





STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

5

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	15.9	16.4	16.9	dB
Slope		S	+0.2	+0.7	+1.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)			—	—	−74	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	—	−72	
Cross Modulation Distortion	53-Channel FLAT	XMD_{53}	—	−63	—	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	XMD_{60}	—	−63	−61	
Composite Triple Beat	53-Channel FLAT	CTB_{53}	—	−62	−61	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	CTB_{60}	—	−59	−58	
DIN (European Applications Only)*						dBμV**
300 MHz — (CH V + Q − P @ W)		DIN1	—	127	—	
400 MHz — (CH M8 + M15 − M9 @ M14)		DIN2	—	125	—	
450 MHz — (CH M20 + M23 − M22 @ M21)		DIN3	—	124	—	
Noise Figure (f = 450 MHz)		NF	—	6.0	7.0	dB
DC Current		I_{DC}	—	200	220	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ) MHW5162A	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	61	≤ −60
Q	259.25	61	
V	289.25	67	
W (Ref.)	295.25	67	
M8	361.25	59	≤ −60
M9	367.25	59	
M14 (Ref.)	397.25	65	
M15	403.25	65	
M20	433.25	64	≤ −60
M21 (Ref.)		64	
M22		58	
M23		58	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

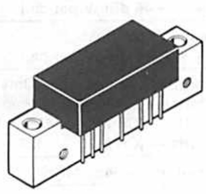
MHW5171A
MHW5172A

The RF Line

17 dB GAIN

450 MHz

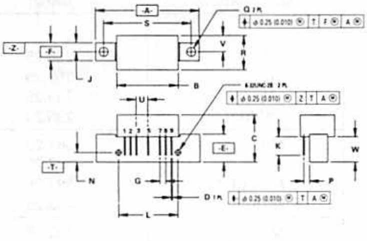
60-CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIERS



450 MHz CATV AMPLIFIERS

. . . designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 17.4 dB (Typ)
- Broadband Noise Figure
  NF = 7.0 dB (Max) MHW5171A
  7.0 dB (Max) MHW5172A
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	MHW5171A Min	MHW5171A Typ	MHW5171A Max	MHW5172A Min	MHW5172A Typ	MHW5172A Max	Unit
Frequency Range		BW	40	—	450	40	—	450	MHz
Power Gain — 50 MHz		G_p	16.8	17.4	17.8	16.8	17.4	17.8	dB
Power Gain — 450 MHz		G_p	17.4	18.4	19.0	17.4	18.4	19.0	dB
Slope		S	0.3	0.5	1.5	0.3	0.5	1.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.4	—	0.2	0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	18	—	—	dB
Second Order Intermodulation Distortion		IMD							dB
(V_{out} = +50 dBmV per ch., Ch 2, M6, M15)			—	−78	—	—	−78	—	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	—	−72	—	—	−74	
Cross Modulation Distortion	53-Channel FLAT	XMD_{53}	—	−60	—	—	−65	—	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	XMD_{60}	—	−60	−59	—	−64	−62	
Composite Triple Beat	53-Channel FLAT	CTB_{53}	—	−61	—	—	−63	—	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	CTB_{60}	—	−58	−58	—	−61	−60	
DIN (European Applications Only)*									dBμV**
300 MHz — (CH V + Q − P @ W)		DIN1	—	125	—	—	127	—	
400 MHz — (CH M8 + M15 − M9 @ M14)		DIN2	—	124	—	—	126	—	
450 MHz — (CH M20 + M23 − M22 @ M21)		DIN3	—	123	—	—	125	—	
Noise Figure (f = 450 MHz)		NF	—	—	7.0	—	6.0	7.0	dB
DC Current		I_{DC}	—	180	200	—	210	240	mA

*DIN (European Applications Only)

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ) MHW5171A	DIN Output Level (dBmV)**(Typ) MHW5172A	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+59	+61	≤ −60
Q	259.25	+59	+61	
V	289.25	+65	+67	
W (Ref.)	295.25	+65	+67	
M8	361.25	+58	+60	≤ −60
M9	367.25	+58	+60	
M14 (Ref.)	397.25	+64	+66	
M15	403.25	+64	+66	
M20	433.25	+63	+65	≤ −60
M21 (Ref.)	439.25	+63	+65	
M22	445.25	+57	+59	
M23	451.25	+57	+59	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

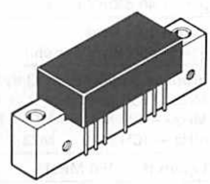
MHW5181A
MHW5182A

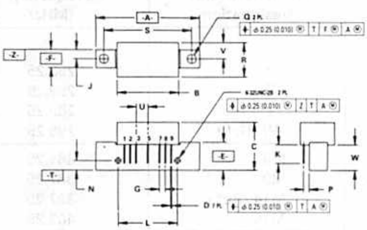
The RF Line

18 dB GAIN

450 MHz

60-CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIERS





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 1
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

450 MHz CATV AMPLIFIERS

... designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 18.2 dB (Typ) @ 50 MHz
  19.0 dB (Typ) @ 450 MHz
- Broadband Noise Figure
  NF = 6.0 dB (Max) MHW5181A
  6.5 dB (Max) MHW5182A
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	MHW5181A Min	MHW5181A Typ	MHW5181A Max	MHW5182A Min	MHW5182A Typ	MHW5182A Max	Unit
Frequency Range		BW	40	—	450	40	—	450	MHz
Power Gain — 50 MHz		G_p	17.8	18.2	18.8	17.8	18.2	18.8	dB
Power Gain — 450 MHz		G_p	18.5	19	20	18.5	19	20	dB
Slope		S	0.3	—	1.5	0.3	—	1.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.4	—	0.2	0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	18	—	—	dB
Second Order Intermodulation Distortion		IMD							dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)			—	−85	—	—	−85	—	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	−80	−72	—	−80	−72	
Cross Modulation Distortion	53-Channel FLAT	XMD_{53}	—	−59	—	—	−62	—	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	XMD_{60}	—	−58	−56	—	−61	−59	
Composite Triple Beat	53-Channel FLAT	CTB_{53}	—	−61	—	—	−64	—	dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	CTB_{60}	—	−58	−57	—	−62	−61	
DIN (European Applications Only)*									dBμV**
300 MHz — (CH V + Q − P @ W)		DIN1	—	124	—	—	126	—	
400 MHz — (CH M8 + M15 − M9 @ M14)		DIN2	—	124	—	—	126	—	
450 MHz — (CH M20 + M23 − M22 @ M21)		DIN3	—	123	—	—	125	—	
Noise Figure (f = 450 MHz)		NF	—	5.5	6.5	—	5.5	6.5	dB
DC Current		I_{DC}	—	180	200	—	210	240	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ) MHW5181A	DIN Output Level (dBmV)**(Typ) MHW5182A	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+58	+60	≤ −60
Q	259.25	+58	+60	
V	289.25	+64	+66	
W (Ref.)	295.25	+64	+66	
M8	361.25	+58	+60	≤ −60
M9	367.25	+58	+60	
M14 (Ref.)	397.25	+64	+66	
M15	403.25	+64	+66	
M20	433.25	+63	+65	≤ −60
M21 (Ref.)	439.25	+63	+65	
M22	445.25	+57	+59	
M23	451.25	+57	+59	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

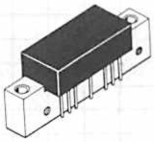
5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW5185
MHW6185

The RF Line
High Output Doubler 450/550 MHz CATV Amplifiers

18 dB GAIN
450/550 MHz
60/77-CHANNEL
CATV AMPLIFIERS



CASE 714-04, STYLE 1

. . . designed specifically for 450/550 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 6 to 8 GHz f_T and an all gold metallization system.

- 4th Generation Die Technology
- Specified for 60/77-Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 18.5 dB (Typ) @ 50 MHz
  19.0 dB (Typ) @ 450 MHz
  19.5 dB (Typ) @ 550 MHz
- Broadband Noise Figure
  NF = 5 dB (Typ) — MHW5185
  = 6 dB (Typ) — MHW6185
- Improvement in Distortion Over Conventional Hybrids
- Allows Higher Output Level Operation

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range	MHW5185 MHW6185	BW	40 40	— —	450 550	MHz
Power Gain	50 MHz 450 MHz 550 MHz	G_p	18 18.5 18.8	— — —	19 19.7 20.3	dB
Slope		S	0.5	—	2.0	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	8	dB
Second Order Intermodulation Distortion (V_{out} = +46 dBmV, Ch 2, M13, M22) (V_{out} = +46 dBmV, Ch 2, M30, M39)	 MHW5185 MHW6185	IMD	 — —	 — —	 −74 −71	dB
Cross Modulation Distortion (V_{out} = +46 dBmV) (V_{out} = +44 dBmV)	 60-Channel FLAT 77-Channel FLAT	 XMD_{60} XMD_{77}	 — —	 −68 −66	 −66 −63	dB
Composite Triple Beat (V_{out} = +46 dBmV) (V_{out} = +44 dBmV)	 60-Channel FLAT 77-Channel FLAT	 CTB_{60} CTB_{77}	 — —	 −67 −65	 −65 −63	dB
DIN (European Applications Only) 300 MHz — (CH V + Q − P @ W) 400 MHz — (CH M8 + M15 − M9 @ M14) 450 MHz — (CH M20 + M23 − M22 @ M21)	MHW5185	 DIN1 DIN2 DIN3	 — — —	 129 128 126	 — — —	dBμV
Noise Figure	450 MHz 550 MHz	NF	— —	5.0 6.0	7.0 7.5	dB
DC Current		I_{DC}	—	385	435	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ) MHW5185	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+63	≤ −60
Q	259.25	+63	
V	289.25	+69	
W (Ref.)	295.25	+69	
M8	361.25	+62	≤ −60
M9	367.25	+62	
M14 (Ref.)	397.25	+68	
M15	403.25	+68	
M20	433.25	+66	≤ −60
M21 (Ref.)	439.25	+66	
M22	445.25	+60	
M23	451.25	+60	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

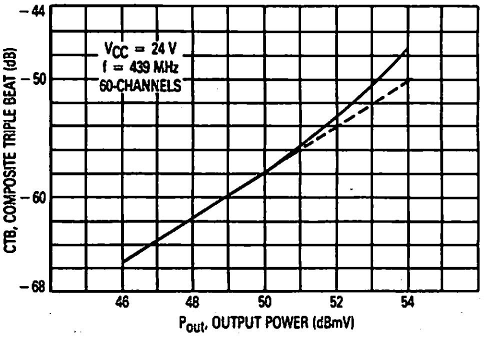


Figure 1. CTB versus Output Power

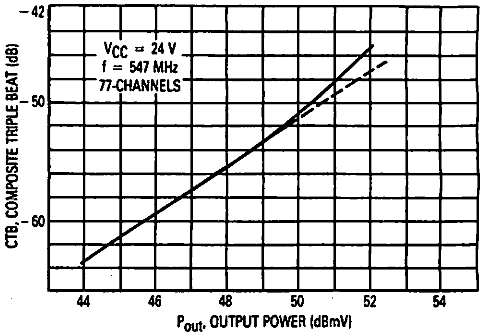


Figure 2. CTB versus Output Power

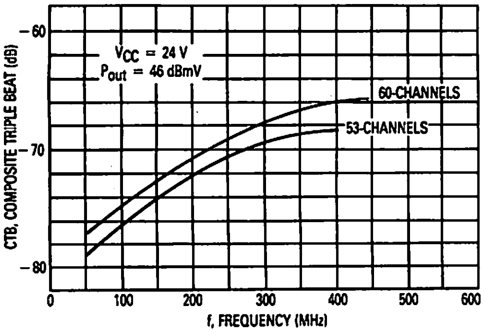


Figure 3. CTB versus Frequency/Channels

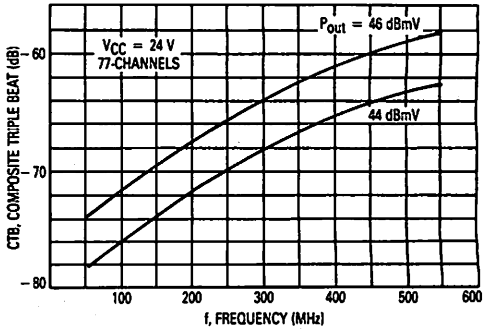


Figure 4. CTB versus Frequency/Output Power

5

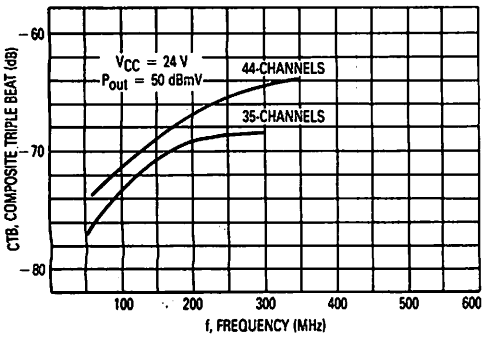


Figure 5. CTB versus Frequency/Channels

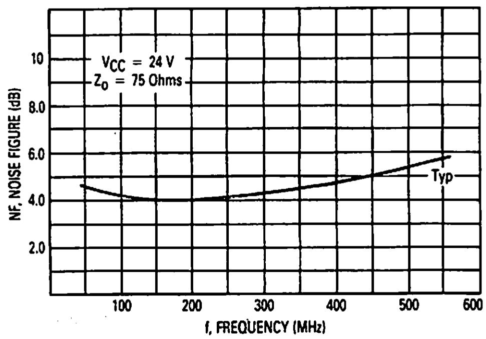


Figure 6. NF versus Frequency

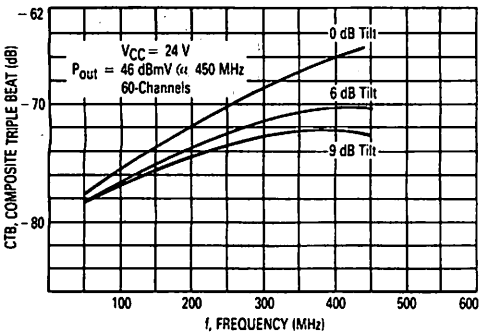


Figure 7. CTB versus Frequency/Tilt

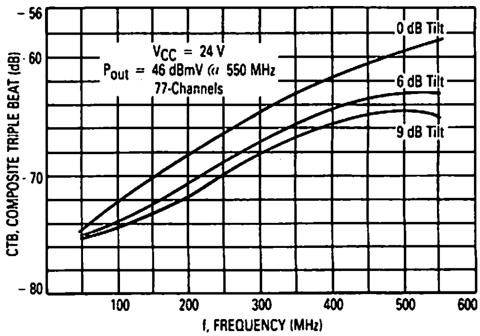


Figure 8. CTB versus Frequency/Tilt

5

Table 1. Functional Performance versus Temperature*

Parameter	Condition	Symbol	T1 −20°C	T2 35°C	T3 80°C	Units
Power Gain	50 MHz	G_{p1}	17.70	17.63	17.54	dB
Power Gain	450 MHz	G_{p2}	18.34	18.22	18.14	dB
Power Gain	550 MHz	G_{p3}	18.63	18.40	18.24	dB
Composite Triple Beat	V_{out} = +46 dBmV 60-Ch FLAT	CTB_{60}	−66.1	−64.9	−62.9	dB
Composite Triple Beat	V_{out} = +46 dBmV 77-Ch FLAT	CTB_{77}	−59.3	−57.7	−56.5	dB
DC Current	V_{DC} = 24 V	I_{DC}	370	401	419	mA

*Data in Table 1 is the average value of several parts and is only intended to show typical trends in performance as a function of temperature. Absolute values of specific parameters will comply with limits specified under "ELECTRICAL CHARACTERISTICS."

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW5222A

The RF Line

22 dB GAIN

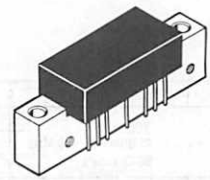
450 MHz

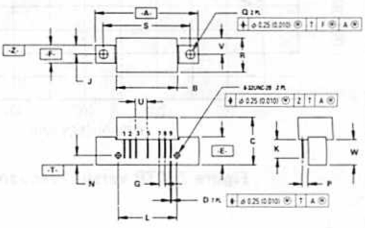
60-CHANNEL
CATV TRUNK AMPLIFIER

450 MHz CATV AMPLIFIER

. . . designed for broadband applications requiring low distortion characteristics. Specifically intended for CATV market requirements. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T, and all an gold metallization system.

- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 22 dB (Typ)
- Broadband Noise Figure — @ f = 450 MHz
  NF = 4.5 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

5

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	21.4	22	22.6	dB
Power Gain — 450 MHz		G_p	22.0	22.9	23.5	dB
Slope		S	0.2	0.5	1.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV, Ch 2, M6, M15)			—	−80	—	
(V_{out} = +44 dBmV, Ch 2, M13, M22)			—	−78	−72	
Cross Modulation Distortion (V_{out} = +46 dBmV)	53-Channel FLAT	XMD_{53}	—	−60	—	dB
	60-Channel FLAT	XMD_{60}		−60	−59	
Composite Triple Beat (V_{out} = +46 dBmV)	53-Channel FLAT	CTB_{53}	—	−63	—	dB
	60-Channel FLAT	CTB_{60}	—	−61	−60	
DIN (European Applications Only)						dBμV
300 MHz — (CH V + Q − P @ W)		DIN1	—	125.5	—	
400 MHz — (CH M8 + M15 − M9 @ M14)		DIN2	—	125	—	
450 MHz — (CH M20 + M23 − M22 @ M21)		DIN3	—	124	—	
Noise Figure (f = 450 MHz)		NF	—	4.5	5.0	dB
DC Current		I_{DC}	—	210	240	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ)	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+59.5	≤ −60
Q	259.25	+59.5	
V	289.25	+65.5	
W (Ref.)	295.25	+65.5	
M8	361.25	+59	≤ −60
M9	367.25	+59	
M14 (Ref.)	397.25	+65	
M15	403.25	+65	
M20	433.25	+64	≤ −60
M21 (Ref.)	439.25	+64	
M22	445.25	+58	
M23	451.25	+58	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

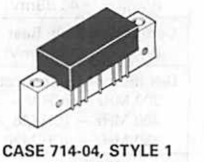
MHW5225
MHW5225R

The RF Line
High Output Doubler 450 MHz CATV Amplifiers

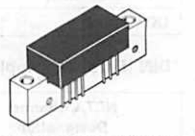
. . . designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 6.0 to 8.0 GHz f_T and an all gold metallization system.

- Both +24 V (MHW5225) and −24 V (MHW5225R) Supply Voltage
- 4th Generation Die Technology
- Specified for 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 22 dB (Typ) @ 50 MHz
  23 dB (Typ) @ 450 MHz
- Broadband Noise Figure
  NF = 4.5 dB (Typ)
- Improvement in Distortion Over Conventional Hybrids
- Allows Higher Output Level Operation

22 dB GAIN
450 MHz
60-CHANNEL
CATV AMPLIFIERS



CASE 714-04, STYLE 1
MHW5225



CASE 714C-04, STYLE 1
MHW5225R

ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
RF Voltage Input (Single Tone)		V_{in}	+70	dBmV
DC Supply Voltage	MHW5225 MHW5225R	V_{CC}	+28 −28	Vdc
Operating Case Temperature Range		T_C	−20 to +100	°C
Storage Temperature Range		T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc (MHW5225) or −24 V (MHW5225R), T_A = + 25°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain	50 MHz 450 MHz	G_p	21.4 22.3	22.0 23.0	22.6 23.7	dB
Slope		S	0.3	1.0	1.8	dB
Gain Flatness (Peak To Valley)		—	—	.25	.5	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +46 dBmV per ch., Ch 2, M13, M22)		IMD	—	−74	−69	dB
Cross Modulation Distortion (V_{out} = + 46 dBmV per ch.)	60-Channel FLAT	XMD_{60}	—	−67	−60	dB
Composite Triple Beat (V_{out} = + 46 dBmV per ch.)	60-Channel FLAT	CTB_{60}	—	−65	−62	dB
Noise Figure	450 MHz	NF	—	4.5	6.0	dB
DC Current	MHW5225 MHW5225R	I_{DC}	— —	415 415	440 440	mA

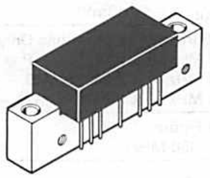
MHW5272A

The RF Line

27 dB GAIN

450 MHz

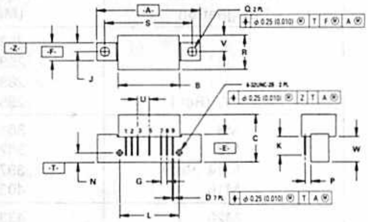
**60-CHANNEL
CATV LINE EXTENDER
AMPLIFIER**



450 MHz CATV AMPLIFIER

. . . designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 27 dB (Typ)
- Broadband Noise Figure
  NF = 5.0 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors



STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

5

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	26.2	27	27.8	dB
Power Gain — 450 MHz		G_p	27.0	28.0	29.0	dB
Slope		S	0	+1.0	+2.5	dB
Gain Flatness (Peak To Valley)		—	—	0.4	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M 6, M15)			—	−78	—	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	−76	−68	
Cross Modulation Distortion	53-Channel FLAT	XMD_{53}	—	−63	—	dB
(V_{out} = +46 dBmV)	60-Channel FLAT	XMD_{60}	—	−63	−60	
Composite Triple Beat	53-Channel FLAT	CTB_{53}	—	−63	—	dB
(V_{out} = +46 dBmV)	60-Channel FLAT	CTB_{60}	—	−61	−59	
DIN (European Applications Only)						dBμV
300 MHz — (CH V + Q − P @ W)		DIN1	—	126	—	
400 MHz — (CH M8 + M15 − M9 @ M14)		DIN2	—	125	—	
450 MHz — (CH M20 + M23 − M22 @ M21)		DIN3	—	124	—	
Noise Figure (f = 450 MHz)		NF	—	5.0	6.0	dB
DC Current		I_{DC}	—	310	340	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ)	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+60	≤ −60
Q	259.25	+60	
V	289.25	+66	
W (Ref.)	295.25	+66	
M8	361.25	+59	≤ −60
M9	367.25	+59	
M14 (Ref.)	397.25	+65	
M15	403.25	+65	
M20	433.25	+64	≤ −60
M21 (Ref.)	439.25	+64	
M22	445.25	+58	
M23	451.25	+58	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW5332A

The RF Line

450 MHz CATV AMPLIFIER

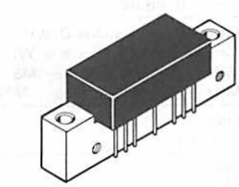
. . . designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

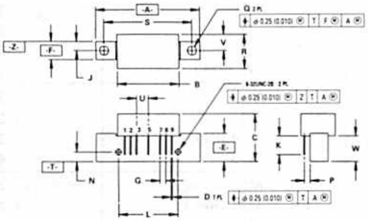
- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 33 dB (Typ)
- Broadband Noise Figure
  NF = 5.0 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors

33 dB GAIN

450 MHz

60-CHANNEL CATV LINE EXTENDER AMPLIFIER





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

5

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	450	MHz
Power Gain — 50 MHz	G_p	32	33	34	dB
Slope	S	0	+1.0	2.0	dB
Gain Flatness (Peak To Valley)	—	—	0.4	0.8	dB
Return Loss — Input/Output 40–450 MHz (Z_o = 75 Ohms)	IRL/ORL	20	—	—	dB
Second Order Intermodulation Distortion (V_{out} = +46 dBmV, Ch 2, M6, M15) (V_{out} = +46 dBmV, Ch 2, M13, M22)	IMD	 — —	 −80 −78	 — −70	dB
Cross Modulation Distortion 53-Channel FLAT (V_{out} = +46 dBmV) 60-Channel FLAT	XMD_{53} XMD_{60}	— —	−63 −61	— −59	dB
Composite Triple Beat 53-Channel FLAT (V_{out} = +46 dBmV) 60-Channel FLAT	CTB_{53} CTB_{60}	— —	−63 −61	— −60	dB
DIN (European Applications Only)* 300 MHz — (CH V + Q − P @ W) 400 MHz — (CH M8 + M15 − M9 @ M14) 450 MHz — (CH M20 + M23 − M22 @ M21)	 DIN1 DIN2 DIN3	 — — —	 126 125 124	 — — —	dBμV**
Noise Figure (f = 450 MHz)	NF	—	5.0	6.0	dB
DC Current	I_{DC}	—	310	340	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ)	DIN Beat Level dB Relative to Ref. Ch.
P Q V W (Ref.)	253.25 259.25 289.25 295.25	+60 +60 +66 +66	≤ −60
M8 M9 M14 (Ref.) M15	361.25 367.25 397.25 403.25	+59 +59 +65 +65	≤ −60
M20 M21 (Ref.) M22 M23	433.25 439.25 445.25 451.25	+64 +64 +58 +58	≤ −60

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW5342A

The RF Line

34 dB GAIN

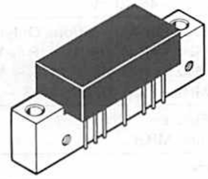
450 MHz

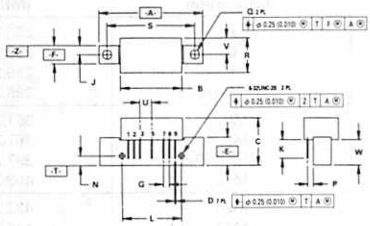
60-CHANNEL
CATV LINE EXTENDER
AMPLIFIER

450 MHz CATV AMPLIFIER

. . . designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 34 dB (Typ)
- Broadband Noise Figure
  NF = 5.0 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- *All Gold Metallization*
- 7.0 GHz Ion-Implanted Transistors





ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

5

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	33.5	34.5	35.5	dB
Power Gain — 450 MHz		G_p	34.5	35.5	37	dB
Slope		S	0	+1.0	+2.5	dB
Gain Flatness (Peak To Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)			—	−78	—	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	−74	−68	
Cross Modulation Distortion (V_{out} = +46 dBmV)	53-Channel FLAT	XMD_{53}	—	−63	—	dB
	60-Channel FLAT	XMD_{60}	—	−63	−59	
Composite Triple Beat (V_{out} = +46 dBmV)	53-Channel FLAT	CTB_{53}	—	−63	—	dB
	60-Channel FLAT	CTB_{60}	—	−62	−59	
DIN (European Applications Only)						dBμV
300 MHz — (CH V + Q − P @ W)		DIN1	—	126	—	
400 MHz — (CH M8 + M15 − M9 @ M14)		DIN2	—	125	—	
450 MHz — (CH M20 + M23 − M22 @ M21)		DIN3	—	124	—	
Noise Figure (f = 450 MHz)		NF	—	5.0	5.5	dB
DC Current		I_{DC}	—	310	340	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ)	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+60	≤ −60
Q	259.25	+60	
V	289.25	+66	
W (Ref.)	295.25	+66	
M8	361.25	+59	≤ −60
M9	367.25	+59	
M14 (Ref.)	397.25	+65	
M15	403.25	+65	
M20	433.25	+64	≤ −60
M21 (Ref.)	439.25	+64	
M22	445.25	+58	
M23	451.25	+58	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

5

MHW5382A

The RF Line

450 MHz CATV AMPLIFIER

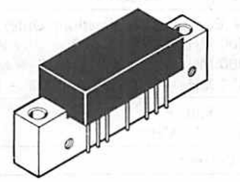
. . . designed specifically for 450 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

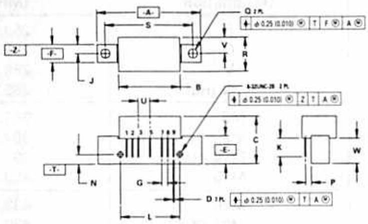
- Specified for 53- and 60-Channel Performance
- Broadband Power Gain — @ f = 40–450 MHz
  G_p = 38 dB (Typ)
- Broadband Noise Figure
  NF = 4.0 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors

38 dB GAIN

450 MHz

60-CHANNEL CATV LINE EXTENDER AMPLIFIER





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	450	MHz
Power Gain — 50 MHz		G_p	37	38	39.5	dB
Power Gain — 450 MHz		G_p	38.0	39.0	40.0	dB
Slope		S	0	+1.0	+2.5	dB
Gain Flatness (Peak To Valley)		—	—	0.3	0.6	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M6, M15)			—	−78	—	
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	−72	−64	
Cross Modulation Distortion (V_{out} = +46 dBmV)	53-Channel FLAT	XMD_{53}	—	−63	—	dB
	60-Channel FLAT	XMD_{60}	—	−61	−59	
Composite Triple Beat (V_{out} = +46 dBmV)	53-Channel FLAT	CTB_{53}	—	−63	—	dB
	60-Channel FLAT	CTB_{60}	—	−60	−59	
DIN (European Applications Only)						dBμV
300 MHz — (CH V + Q − P @ W)		DIN1	—	125	—	
400 MHz — (CH M8 + M15 − M9 @ M14)		DIN2	—	124	—	
450 MHz — (CH M20 + M23 − M22 @ M21)		DIN3	—	123	—	
Noise Figure (f = 450 MHz)		NF	—	4.0	5.0	dB
DC Current		I_{DC}	—	310	340	mA

***DIN (European Applications Only)**

NCTA Channel Designation	Frequency (MHz)	DIN Output Level (dBmV)**(Typ)	DIN Beat Level dB Relative to Ref. Ch.
P	253.25	+59	≤ −60
Q	259.25	+59	
V	289.25	+65	
W (Ref.)	295.25	+65	
M8	361.25	+58	≤ −60
M9	367.25	+58	
M14 (Ref.)	397.25	+64	
M15	403.25	+64	
M20	433.25	+57	≤ −60
M21 (Ref.)	439.25	+57	
M22	445.25	+63	
M23	451.25	+63	

**DIN (dBμV) = Reference Channel Level (dBmV) + 60 dB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW6122

The RF Line

12 dB GAIN

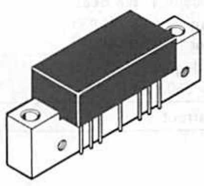
550 MHz

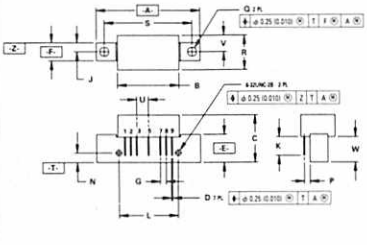
77-CHANNEL CATV INPUT/OUTPUT TRUNK AMPLIFIER

550 MHz CATV AMPLIFIER

. . . designed specifically for 550 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 77-Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 12.5 dB (Typ) @ 50 MHz
  13 dB (Min) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 8.5 dB (Max) MHW6122
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors





STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain — 50 MHz		G_p	12	12.5	13	dB
Power Gain — 550 MHz		G_p	12.5	—	—	dB
Slope		S	0.2	—	1.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV, Ch 2, M13, M22)			—	—	−72	
(V_{out} = +44 dBmV, Ch 2, M30, M39)			—	—	−72	
Cross Modulation Distortion						dB
(V_{out} = +46 dBmV)	60-Channel FLAT	XMD_{60}	—	−63	—	
(V_{out} = +44 dBmV)	77-Channel FLAT	XMD_{77}	—	−65	−62	
Composite Triple Beat						dB
(V_{out} = +46 dBmV)	60-Channel FLAT	CTB_{60}	—	−62	—	
(V_{out} = +44 dBmV)	77-Channel FLAT	CTB_{77}	—	−58	−56	
Noise Figure (f = 550 MHz)		NF	—	7.0	8.5	dB
DC Current		I_{DC}	—	210	240	mA

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW6141
MHW6142

The RF Line

550 MHz CATV AMPLIFIERS

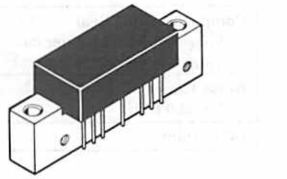
. . . designed specifically for 550 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for >77 Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 14 dB (Typ) @ 50 MHz
  14.5 dB (Min) @ 550 MHz
- Broadband Noise Figure
  NF = 7.5 dB (Max) MHW6141
  7.5 dB (Max) MHW6142
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors

14 dB GAIN

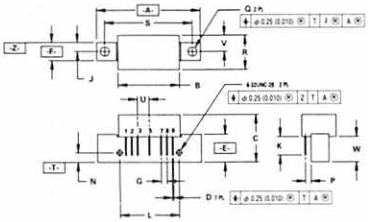
550 MHz

77-CHANNEL CATV INPUT/OUTPUT TRUNK AMPLIFIERS



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C



STYLE 1
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic	Symbol	MHW6141			MHW6142			Unit
		Min	Typ	Max	Min	Typ	Max	
Frequency Range	BW	40	—	550	40	—	550	MHz
Power Gain — 50 MHz	G_p	13.5	14	14.5	13.5	14	14.5	dB
Power Gain — 550 MHz	G_p	14.5	—	—	14.5	—	—	dB
Slope	S	0.2	—	1.5	0.2	—	1.5	dB
Gain Flatness (Peak To Valley)	—	—	0.2	0.4	—	0.2	0.4	dB
Return Loss — Input/Output 40–550 MHz (Z_o = 75 Ohms)	IRL/ORL	18	—	—	18	—	—	dB
Second Order Intermodulation Distortion	IMD							dB
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)		—	−75	—	—	−78	—	
(V_{out} = +44 dBmV per ch., Ch 2, M30, M39)		—	−73	−70	—	−75	−72	
Cross Modulation Distortion								dB
(V_{out} = +46 dBmV per ch.) 60-Channel FLAT	XMD_{60}	—	−61	—	—	−64	—	
(V_{out} = +44 dBmV per ch.) 77-Channel FLAT	XMD_{77}	—	−62	−59	—	−65	−62	
Composite Triple Beat								dB
(V_{out} = +46 dBmV per ch.) 60-Channel FLAT	CTB_{60}	—	−59	—	—	−62	—	
(V_{out} = +44 dBmV per ch.) 77-Channel FLAT	CTB_{77}	—	−58	−56	—	−65	−59	
Noise Figure (f = 550 MHz)	NF	—	—	7.5	—	6.5	7.5	dB
DC Current	I_{DC}	—	180	200	—	210	240	mA

5

MHW6171
MHW6172

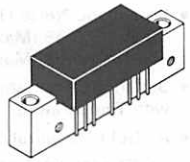
The RF Line

77-Channel (550 MHz) CATV Input/Output Trunk Amplifiers

**17 dB GAIN
550 MHz
77-CHANNEL
CATV AMPLIFIERS**

... designed specifically for 550 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7 GHz f_T and an all gold metallization system.

- Specified for 77-Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 17.2 dB (Typ)
- Broadband Noise Figure — @ f = 550 MHz
  NF = 6 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz Ion-Implanted Transistors



CASE 714-04, STYLE 1

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	MHW6171			MHW6172			Unit
			Min	Typ	Max	Min	Typ	Max	
Frequency Range		BW	40	—	550	40	—	550	MHz
Power Gain	50 MHz	G_p	16.8	17.2	17.8	16.8	17.2	17.8	dB
Slope		S	0	+0.5	+1.5	0	+0.5	+1.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.4	—	0.2	0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	18	—	—	dB
Second Order Intermodulation (V_{out} = +46 dBmV per ch., Ch 2, M13, M22) (V_{out} = +44 dBmV per ch., Ch 2, M30, M39)		IMD	 — —	 −80 −76	 — −68	 — —	 −80 −78	 — −70	dB
Cross Modulation Distortion (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 60-Channel FLAT 77-Channel FLAT	 XMD_{60} XMD_{77}	 — —	 −60 −62	 — −59	 — —	 −63 −65	 — −62	dB
Composite Triple Beat Noise (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 60-Channel FLAT 77-Channel FLAT	 CTB_{60} CTB_{77}	 — —	 −60 −58	 — −56	 — —	 −62 −60	 — −59	dB
Noise Figure	450 MHz 550 MHz	NF	— —	5.5 6	— 7	— —	5.5 6	— 7	dB
DC Current		I_{DC}	—	180	200	—	210	240	mA

MHW6181
MHW6182

The RF Line

550 MHz CATV AMPLIFIERS

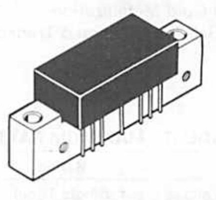
. . . designed specifically for 550 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

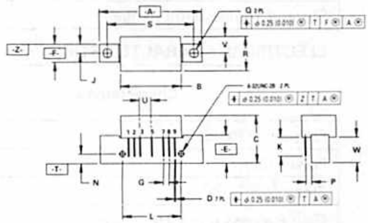
- Specified for >77 Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 18.2 dB (Typ) @ 50 MHz
  18.8 dB (Min) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 7.0 dB (Max) MHW6181
  7.0 dB (Max) MHW6182
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors

18 dB GAIN

550 MHz

77-CHANNEL
CATV INPUT/OUTPUT
TRUNK AMPLIFIERS





STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

CASE 714-04

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+70	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

5

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic	Symbol	MHW6181			MHW6182			Unit
		Min	Typ	Max	Min	Typ	Max	
Frequency Range	BW	40	—	550	40	—	550	MHz
Power Gain — 50 MHz	G_p	17.7	18.2	18.7	17.7	18.2	18.7	dB
Power Gain — 550 MHz	G_p	18.8	19.2	20	18.8	19.2	20	dB
Slope	S	0.5	—	2.0	0.5	—	2.0	dB
Gain Flatness (Peak To Valley)	—	—	0.2	0.4	—	0.2	0.4	dB
Return Loss — Input/Output 40–550 MHz (Z_o = 75 Ohms)	IRL/ORL	18	—	—	18	—	—	dB
Second Order Intermodulation Distortion	IMD							dB
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)		—	−83	—	—	−85	—	
(V_{out} = +44 dBmV per ch., Ch 2, M30, M39)		—	−78	−70	—	−80	−72	
Cross Modulation Distortion								dB
(V_{out} = +46 dBmV per ch.) 60-Channel FLAT	XMD_{60}	—	−58	—	—	−61	—	
(V_{out} = +44 dBmV per ch.) 77-Channel FLAT	XMD_{77}	—	−62	−59	—	−64	−62	
Composite Triple Beat								dB
(V_{out} = +46 dBmV per ch.) 60-Channel FLAT	CTB_{60}	—	−58	—	—	−62	—	
(V_{out} = +44 dBmV per ch.) 77-Channel FLAT	CTB_{77}	—	−58	−56	—	−60	−58	
Noise Figure (f = 550 MHz)	NF	—	—	7.0	—	—	7.0	dB
DC Current	I_{DC}	—	180	200	—	210	240	mA

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MHW6222

The RF Line

550 MHz CATV AMPLIFIER

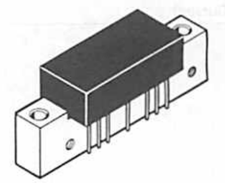
. . . designed specifically for 550 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7.0 GHz f_T and an all gold metallization system.

- Specified for 77-Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 22 dB (Typ) @ 50 MHz
  22 dB (Min) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 6.0 dB (Max)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7.0 GHz Ion-Implanted Transistors

22 dB GAIN

550 MHz

77-CHANNEL CATV INPUT/OUTPUT TRUNK AMPLIFIER



CASE 714-04

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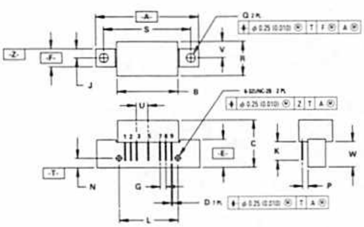

CASE 714-04

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+60	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain — 50 MHz		G_p	21.4	22	22.6	dB
Power Gain — 550 MHz		G_p	22	—	—	dB
Slope		S	0.2	—	1.5	dB
Gain Flatness (Peak To Valley)		—	—	0.2	0.4	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz	IRL/ORL	18	—	—	dB
Second Order Intermodulation Distortion		IMD				dB
(V_{out} = +46 dBmV per ch., Ch 2, M13, M22)			—	−80	—	
(V_{out} = +46 dBmV per ch., Ch 2, M30, M39)			—	−72	−66	
Cross Modulation Distortion						dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	XMD_{60}	—	−60	—	
(V_{out} = +44 dBmV per ch.)	77-Channel FLAT	XMD_{77}	—	−60	−57	
Composite Triple Beat						dB
(V_{out} = +46 dBmV per ch.)	60-Channel FLAT	CTB_{60}	—	−61	—	
(V_{out} = +44 dBmV per ch.)	77-Channel FLAT	CTB_{77}	—	−59	−57	
Noise Figure (f = 550 MHz)		NF	—	5.0	6.0	dB
DC Current		I_{DC}	—	210	240	mA

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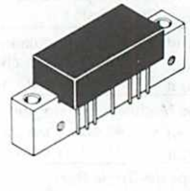
MHW6272

The RF Line

77-Channel (550 MHz) CATV Line Extender Amplifier

- Specified for 60- and 77-Channel Performance
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 27 dB (Typ)
- Broadband Noise Figure
  NF = 6 dB (Typ) @ 550 MHz
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz f_T Ion-Implanted Transistors

27 dB GAIN
550 MHz
77-CHANNEL
CATV AMPLIFIER



CASE 714-04, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain	50 MHz 550 MHz	G_p	26.2 27	27 —	27.8 29.2	dB
Slope		S	0	+1	2	dB
Gain Flatness (Peak To Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–450 MHz 450–550 MHz	IRL/ORL	18 16	— —	— —	dB
Second Order Intermodulation Distortion (V_{out} = +48 dBmV per ch., Ch 2, 13, R) (V_{out} = +46 dBmV per ch., Ch 2, M6, M15) (V_{out} = +46 dBmV per ch., Ch 2, M13, M22) (V_{out} = +44 dBmV per ch., Ch 2, M30, M39)		IMD	 — — — —	 −80 −78 −76 −69	 — — — −64	dB
Cross Modulation Distortion @ Ch 2 (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 53-Channel FLAT 60-Channel FLAT 70-Channel FLAT 77-Channel FLAT	 XMD_{53} XMD_{60} XMD_{70} XMD_{77}	 — — — —	 −63 −62 −61 −59	 — — — −57	dB
Composite Triple Beat (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	 53-Channel FLAT 60-Channel FLAT 70-Channel FLAT 77-Channel FLAT	 TB_{53} TB_{60} TB_{70} TB_{77}	 — — — —	 −63 −62 −61 −59	 — — — −57	dB
Noise Figure	550 MHz	NF	—	6.0	6.5	dB
DC Current		I_{DC}	—	310	340	mA

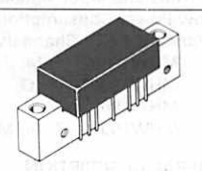
MHW6342

The RF Line
77-Channel (550 MHz) CATV Amplifier

. . . designed specifically for 550 MHz CATV applications. Features ion-implanted arsenic emitter transistors with 7 GHz f_T and an all gold metallization system.

- *Specified for 77-Channel Performance*
- Broadband Power Gain — @ f = 40–550 MHz
  G_p = 34.5 dB (Typ) @ 50 MHz
  35 dB (Min) @ 550 MHz
- Broadband Noise Figure @ 550 MHz
  NF = 6 dB (Typ)
- Superior Gain, Return Loss and DC Current Stability with Temperature
- All Gold Metallization
- 7 GHz Ion-Implanted Transistors

**34 dB GAIN
550 MHz
77-CHANNEL
CATV AMPLIFIER**



CASE 714-04, STYLE 1

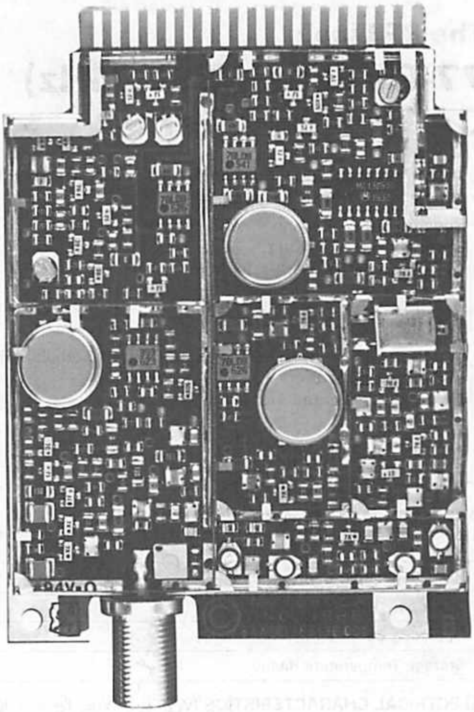
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+55	dBmV
DC Supply Voltage	V_{CC}	+28	Vdc
Operating Case Temperature Range	T_C	−20 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_C = +30°C, 75 Ω system unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	40	—	550	MHz
Power Gain	50 MHz	G_p	33.5	34.5	35.5	dB
Power Gain	550 MHz	G_p	35	—	—	dB
Slope		S	0	+1	2	dB
Gain Flatness (Peak To Valley)		—	—	0.4	0.8	dB
Return Loss — Input/Output (Z_o = 75 Ohms)	40–550 MHz 450–550 MHz	IRL/ORL	18 16	— —	— —	dB
Second Order Intermodulation Distortion (V_{out} = +46 dBmV per ch., Ch 2, M13, M22) (V_{out} = +44 dBmV per ch., Ch 2, M30, M39)		IMD	— —	−75 −70	— −64	dB
Cross Modulation Distortion (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	60-Channel FLAT 77-Channel FLAT	XMD_{60} XMD_{77}	— —	−61 −59	— −57	dB
Composite Triple Beat (V_{out} = +46 dBmV per ch.) (V_{out} = +44 dBmV per ch.)	60-Channel FLAT 77-Channel FLAT	CTB_{60} CTB_{77}	— —	−60 −58	— −57	dB
Noise Figure	550 MHz	NF	—	5.5	6.5	dB
DC Current		I_{DC}	—	310	340	mA

MHW10000 Series



Broadband RF Amplifier

For IBM PC Network and IEEE 802.7 Modem Applications

- IBM PC Network and Broadband LAN Compatible
- Extremely Small Size — <8 In^2
- 2 Mbps Data Rate
- High Selectivity
- High Spectral Purity
- RUGGED — Continuous operation into any load. Can withstand input signals to +65 dBmV
- Low Power Consumption (<300 mA @ 12 V)
- Standard CATV Channels
  - MHW10000 T-14, J
  - MHW10001 2′, O
  - MHW10002 3′, P
  - MHW10003 T-14, M

GENERAL DESCRIPTION

The MHW10000 Series RF Module is designed to provide the RF functions needed for implementation of a complete modem compatible with the IBM PC Network, and IEEE 802.7 broadband specifications. It is a full duplex, continuous phase frequency shift keyed (CPFSK) transceiver. The design is such that the module operation is completely compatible with a broadband coaxial cable environment such as a fully loaded 60 channel CATV distribution system. The transmitter occupied bandwidth and the receiver selectivity and overload characteristics have been controlled so that the module operation is completely transparent to the cable system operation.

The module transmitter operates at a carrier frequency of 50.75 to 62.75 MHz (See Table 1) with a total frequency deviation of 2 MHz. Transmitter occupied bandwidth is controlled by a SAW filter along with careful attention to the switching characteristics of the circuitry.

A companion receiver operates at a center frequency of 219 to 255 MHz (See Table 1). The circuitry is capable of operating with center frequency offsets up to ± 500 kHz. RF and IF selectivity in the receiver is sufficient to allow normal operation in the presence of a fully loaded cable environment with no performance degradation. The receiver RF selectivity is provided by a two resonator bandpass filter at the RF amplifier input and a two resonator filter between the RF amplifier and the mixer. Receiver noise bandwidth control and adjacent channel selectivity is provided by two cascaded SAW filters in the IF circuitry.

Transmitter output and receiver input circuitry along with an input transformer provide the necessary duplexing function in addition to control of the return loss presented to the cable network in both "on" and "off" conditions. The input transformer also provides protection against voltage surges sometimes found on large cable systems.

Conversion of the analog RF data to the digital data stream is provided by a Motorola MC13055 data IC. This IC provides the final IF amplification and limiting, the quadrature detector, data carrier detect (squelch) and data shaper functions. Careful design attention was paid to optimizing receiver performance in the presence of frequency offsets, transmitter frequency deviation variations, mark-space tilt, system noise and limit case data flag patterns.

Three on board voltage regulators stabilize the module operation in the presence of supply voltage variations and noise. Shielding is also provided to allow normal operation in strong RF fields as well as the electrically noisy environment sometimes found in computing equipment.

Surface mount construction is used to provide an automated, highly repeatable assembly process. The basic card occupies about 8 square inches (2.5 x 3 x 0.4 in.) excluding the "F" connector. Input power and data interface lines for the supporting modem circuitry are accessible thru an 18 pin edge connector. Block diagrams of both the receiver and transmitter functions are shown in Figures 1 and 2.

5

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

GENERAL

Characteristics	Specifications
RF Connector	F, Female
Characteristic Impedance, Nominal	75 Ohms
Return Loss Channel T-14 (Tx on) Channel T-14 (Tx off) Channel J Out-of-channel (10–890 MHz)	 ≥16 dB ≥14 dB ≥12 dB ≥6 dB
Spurious Output Levels Tx off (10–108 MHz) Tx on (10–108 MHz) Tx on/off (108–890 MHz)	 ≤ −26 dBmV ≤ −12 dBmV ≤ −18 dBmV
Load The RF modem is capable of operating continuously into a short or open circuit without damage, and is capable of withstanding input signal levels as high as 65 dBmV.	
Power	+12 Vdc, ±10%; 300 mA Max Max. ripple of 150 mV at frequencies of ≤50 kHz
Size (Nominal, exclusive of "F" conn.)	2.5" x 3" x 0.4"

TRANSMITTER

Center Frequency Range	f_c † ± 300 kHz
Mark Frequency, f_m, (nominal)	f_c + 1 MHz
Space Frequency, f_s, (nominal)	f_c − 1 MHz
Output Level @ 75 Ohms	54 dBmV ± 4 dB
Modulation Technique	Continuous Phase Frequency Shift Keying (CPFSK)
FSK Shift	2 MHz ± 150 kHz
Carrier-to-hum	>43 dB
Carrier-to-noise in 4.2 MHz bandwidth within f_c ± 8 MHz	>50 dB
Modulated Spectrum Shape* 3 dB Bandwidth (nominal) Down > 56 dB Down > 66 dB Down > 72 dB	 3 MHz ±3 MHz from f_c ±4 MHz from f_c ±6 MHz from f_c
Transmitter, Quiet (RTS Off)	≤ −30 dBmV
RTS Delay ("On" or "Off")	6 ± 1 micro-sec.

*TXD driven by pseudo-random NRZI data at 2 Mbps rate. RTS keyed on/off by 5.8 kHz, 10% duty cycle square wave.

† See Table 1.

ENVIRONMENTAL

Operating Temperature Range Storage Temperature Range Operating Humidity Range Storage Humidity Range	10°C to 50°C −40°C to 60°C 8% to 80% (non-condensing) 5% to 100% (non-condensing)

RECEIVER

Characteristics	Specifications
Center Frequency, f_c	†
Center Frequency Acceptance Range (Min.)	f_c ± 400 kHz
Bandwidth (3 dB, nominal)	4 MHz
Local Oscillator Frequency Stability	0.01% (after 10 min. warmup)
Selectivity (at 6 MHz)	≥50 dB
Input Level (nominal)	8.5 dBmV
Operating Level Range	−7 to 24 dBmV
Carrier Detect Threshold	−15 dBmV ± 4 dB
Carrier Detect Delay	<7 μs from application of input signal of −7 dBmV
Data Edge Jitter	≤ ± 150 nano-seconds
Data Symmetry	Better than ± 150 ns; −7 dBmV to +24 dBmV, f_c ± 400 kHz
Data Symmetry Settling Time	12 bits, 6 μs
Data Output Polarity	High Frequency Input = Mark
Data Output Level	TTL Compatible
Bit Error Rate	1E-9 or better with an input level of −7 dBmV and S/N of 33 dB (4.2 MHz bandwidth)

Table 1. Transmit/Receive Frequencies

Part Number	Transmitter Center Frequency	Receiver Center Frequency
MHW10000	50.75 MHz	219 MHz
MHW10001	56.75 MHz	249 MHz
MHW10002	62.75 MHz	255 MHz
MHW10003	50.75 MHz	243 MHz

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Figure 1. Transmitter Block Diagram

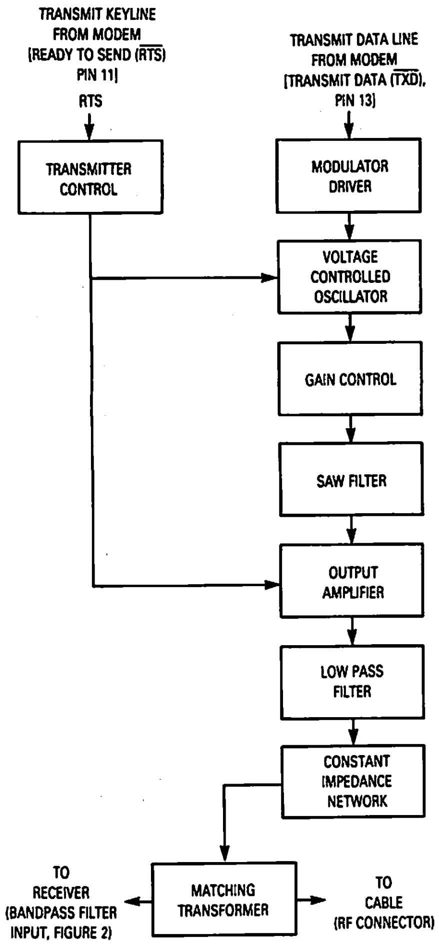
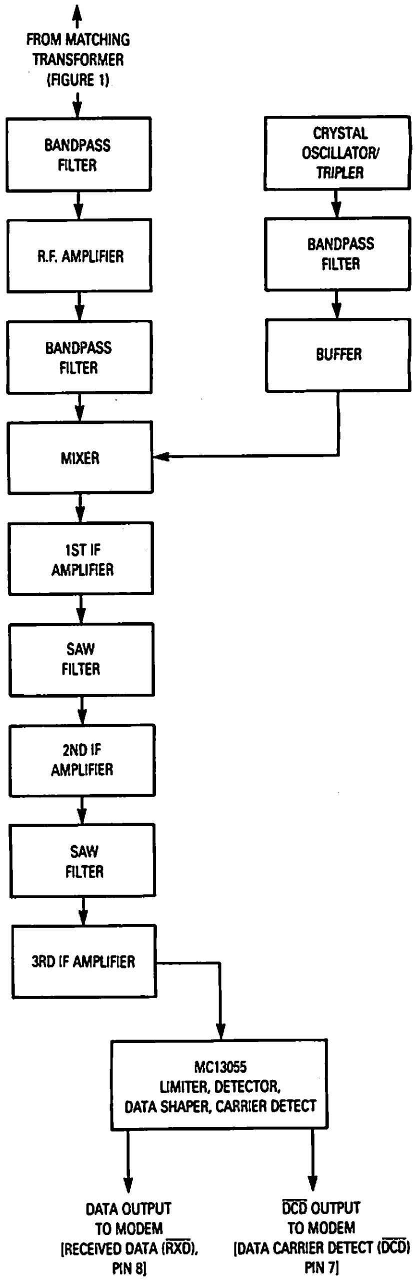


Figure 2. Receiver Block Diagram



Discontinued 10/93

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

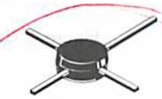
MWA0204
MWA0211L
MWA0270

Monolithic Microwave Integrated Circuit

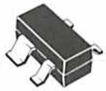
MONOLITHIC MICROWAVE INTEGRATED CIRCUIT

. . . designed for narrow or wideband IF and RF applications in industrial and commercial systems up to 3 GHz.

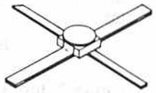
- 12 dB Gain at 1000 MHz (Typ)
- Fully Cascadable
- 50 Ω Input and Output Impedance
- Choice of Package Types
  - Low Cost
  - Surface Mount
  - Hermetic
- Tape and Reel Package Options
- 4.0 dBm P_O 1 dB, at 500 MHz (Typ)
- Unconditionally stable



CASE 317-01, STYLE 3
MWA0204



CASE 318A-05, STYLE 4
MWA0211L



CASE 303A-01, STYLE 3
MWA0270

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameters		Symbol	Ratings	Unit
Circuit Current		I_{CC}	40	mAdc
Input Power, RF		P_{in}	+16	dBm
Bias Voltage		V_{CC}	6	Vdc
Storage Temperature	0204/0211L 0270	T_{stg}	−65 to +150 −65 to +200	°C

RECOMMENDED OPERATING CONDITIONS

Parameters	Symbol	Ratings	Unit
Operating Current	I_{CC}	25	mA
Source Impedance	Z_S	50 to 75	Ω
Load Impedance	Z_L	50 to 75	Ω

THERMAL CHARACTERISTICS

Characteristic	Device	Symbol	Value	Unit
Thermal Resistance, Die to Case	MWA0204 MWA0211L MWA0270	$R_{\theta JC}$	150 200 130	°C/W

DEVICE MARKING

MWA0211,L = 06

ELECTRICAL CHARACTERISTICS (T_A = 25°C, I_{CC} = 25 mA, Z_S = Z_L = 50 Ω, unless specified otherwise)

Characteristic		Symbol	Min	Typ	Max	Unit
Gain (f = 1000 MHz) (f = 100 MHz)	MWA0204/0211L MWA0270	G_T	10 11.5	12 12.5	— 13.5	dB dB
Gain Flatness (f = DC to 800 MHz — MWA0204/0211L) (f = DC to 1500 MHz — MWA0270)			 — —	 1 1	 — —	dB
Noise Figure (f = 100–1600 MHz)		NF	—	5.5 6.5	—	dB
Third Order Intercept Output Power (f_1 = 480 MHz) (f_2 = 500 MHz) (f_1 = 980 MHz) (f_2 = 1000 MHz)		ITO_1 ITO_2 ITO_3 ITO_4	— — — —	16 16 16 16	— — — —	dBm
Second Order Intercept Output Power (f_1 = 480 MHz) (f_2 = 500 MHz) (f_1 = 980 MHz) (f_2 = 1000 MHz)		ISO_1 ISO_2 ISO_3 ISO_4	— — — —	20 20 19 19	— — — —	dBm

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TYPICAL CHARACTERISTICS

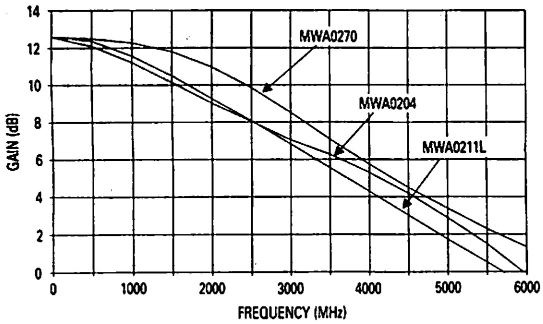

Figure 1. Gain versus Frequency

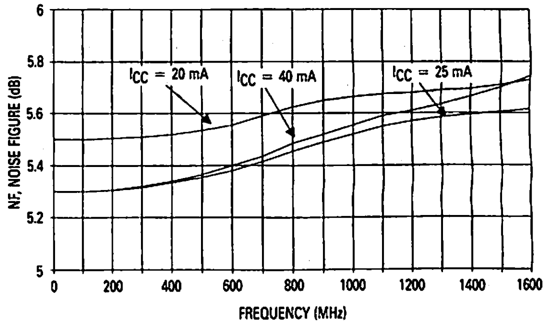

Figure 2. Noise Figure versus Frequency

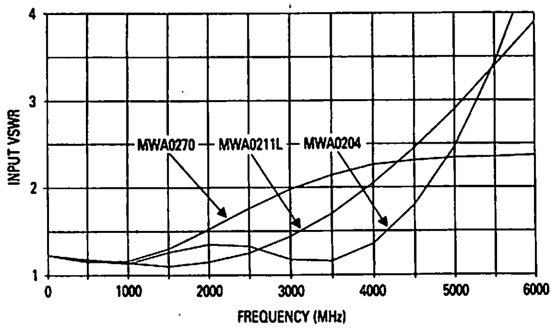

Figure 3. Input VSWR versus Frequency

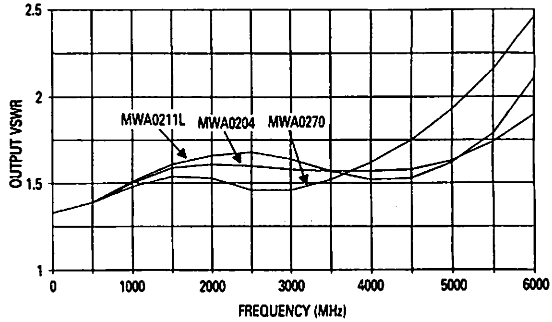

Figure 4. Output VSWR versus Frequency

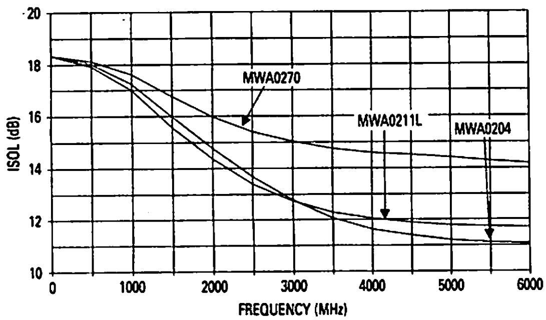

Figure 5. Reverse Isolation versus Frequency

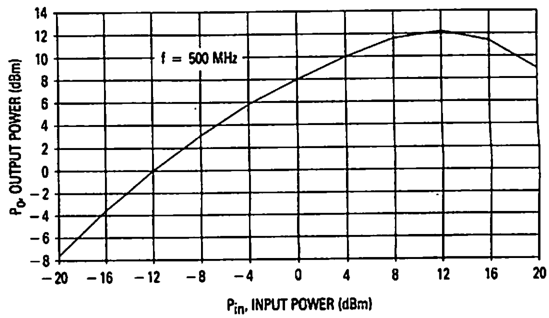

Figure 6. Output Power versus Power

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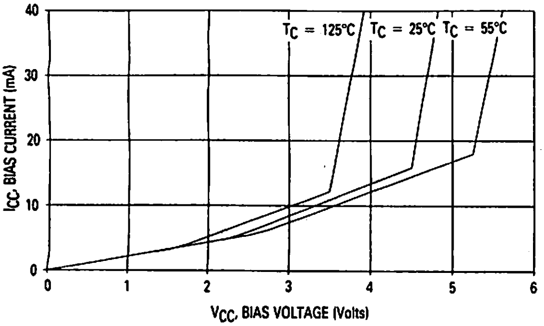

Figure 7. Bias Currrent versus Bias Voltage

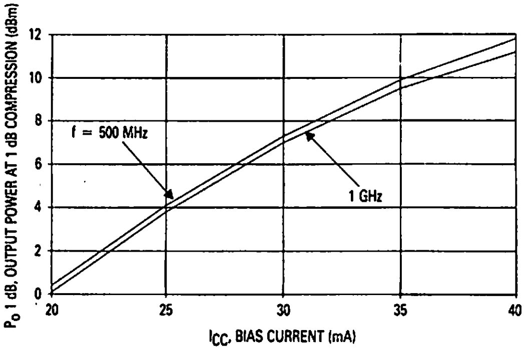

Figure 8. Output power at 1 dB Gain Compression versus Bias Current

Table 1 — Typical S-Parameters and Stability Factor K
MWA0204

I_{CC} (mA)	f (MHz)	S_{11}		S_{21}			S_{12}		S_{22}		
		$\lvert S_{11}\rvert$	∠φ	S_{21} (dB)	$\lvert S_{21}\rvert$	∠φ	$\lvert S_{12}\rvert$	∠φ	$\lvert S_{22}\rvert$	∠φ	K
25	100	0.106	174.2	12.48	4.21	173.1	0.121	2.3	0.132	−13.5	1.195
	200	0.107	164.4	12.46	4.2	166.5	0.121	3.6	0.131	−23.3	1.196
	400	0.093	149.5	12.25	4.1	153.7	0.124	5.8	0.149	−41.1	1.199
	600	0.07	126.3	11.98	3.97	141.2	0.127	9.9	0.168	−56.4	1.208
	800	0.051	88.2	11.63	3.81	129.4	0.134	11.1	0.19	−66.9	1.2
	1000	0.052	41.2	11.23	3.64	118	0.139	13.3	0.201	−74	1.208
	1500	0.116	−20.3	10.15	3.22	92.3	0.16	15.2	0.228	−85.1	1.19
	2000	0.156	−45.7	9.04	2.83	69.3	0.182	14	0.235	−95.8	1.177
	2500	0.145	−64.4	8.05	2.53	48.7	0.207	9.9	0.23	−107.8	1.17
	3000	0.083	−89.6	7.06	2.25	28.8	0.229	5.4	0.225	−123.3	1.179
	3500	0.043	143.7	6.29	2.06	10.3	0.249	−0.9	0.224	−143.5	1.17
	4000	0.153	96.5	5.31	1.84	−8.1	0.262	−7.6	0.221	−160.7	1.181
	5000	0.421	66.5	2.89	1.39	−41.5	0.278	−18.8	0.238	162	1.163
	6000	0.644	49.2	−0.14	0.98	−68.6	0.277	−29.8	0.318	123.8	1.096

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Table 2 — Typical S-Parameters and Stability Factor K
MWA0211L

I_{CC} (mA)	f (MHz)	S_{11}		S_{21}			S_{12}		S_{22}		K
		$\|S_{11}\|$	$\angle\phi$	S_{21} (dB)	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$	
25	100	0.093	172.7	12.7	4.31	173.8	0.121	1.4	0.142	−11.7	1.179
	200	0.093	167.3	12.66	4.3	167	0.122	3.6	0.144	−23.2	1.178
	400	0.083	151.7	12.48	4.21	153.8	0.125	7.2	0.158	−47.7	1.196
	600	0.082	142.5	12.26	4.1	141.4	0.128	10.1	0.171	−69.6	1.178
	800	0.071	137.1	11.97	3.97	129.5	0.136	13	0.186	−86.4	1.161
	1000	0.066	127.2	11.57	3.79	117.4	0.141	12.9	0.206	−103.3	1.163
	1500	0.036	140.1	10.52	3.36	90.7	0.166	16.3	0.233	−127.8	1.126
	2000	0.069	151.9	9.28	2.91	66.6	0.191	14.8	0.248	−153.8	1.116
	2500	0.11	173.4	8.08	2.54	57.3	0.214	20.8	0.265	−156.4	1.105
	3000	0.179	153.5	6.84	2.2	37.9	0.231	15.3	0.228	−167	1.142
	3500	0.289	146	5.56	1.9	20.1	0.237	7.9	0.224	−173.6	1.155
	4000	0.342	132.4	4.37	1.65	4.6	0.252	2.6	0.194	−171.1	1.183
	5000	0.487	107.5	1.86	1.24	−22.8	0.259	−6.2	0.237	177	1.205
	6000	0.573	89.7	−0.74	0.92	−44.5	0.26	−14.8	0.356	159.2	1.222

Table 3 — Typical S-Parameters and Stability Factor K
MWA0270

I_{CC} (mA)	f (MHz)	S_{11}		S_{21}			S_{12}		S_{22}		K
		$\|S_{11}\|$	$\angle\phi$	S_{21} (dB)	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$	
25	100	0.111	179	12.6	4.27	175.2	0.121	1.3	0.146	−10.6	1.178
	200	0.1	177.4	12.56	4.25	170.4	0.122	2	0.147	−19.6	1.18
	400	0.087	176.4	12.49	4.21	161.2	0.122	3.7	0.154	−36.9	1.187
	600	0.072	179.7	12.46	4.2	152	0.125	5.6	0.171	−54.3	1.172
	800	0.065	−171	12.36	4.15	142.7	0.128	7.1	0.183	−66.3	1.161
	1000	0.061	−151.1	12.28	4.11	133.5	0.132	8.2	0.195	−77.6	1.145
	1500	0.116	−119.9	11.82	3.9	109.9	0.145	10	0.211	−99	1.093
	2000	0.205	−126.9	10.99	3.55	86.8	0.159	8.7	0.208	−111	1.057
	2500	0.276	−141.9	9.86	3.11	65.6	0.17	5.7	0.186	−118.7	1.063
	3000	0.33	−157.6	8.53	2.67	47.3	0.177	2.1	0.188	−116.5	1.096
	3500	0.364	−171.1	7.11	2.27	31.1	0.183	−0.4	0.206	−116.1	1.154
	4000	0.382	176.8	5.76	1.94	17.5	0.186	−3.7	0.237	−120.5	1.229
	5000	0.401	156	3.39	1.48	−5	0.19	−8	0.321	−135.4	1.373
	6000	0.407	138.1	1.35	1.17	−23.6	0.196	−11.7	0.422	−149.2	1.456

TYPICAL CHARACTERISTICS (MWA0270 ONLY)

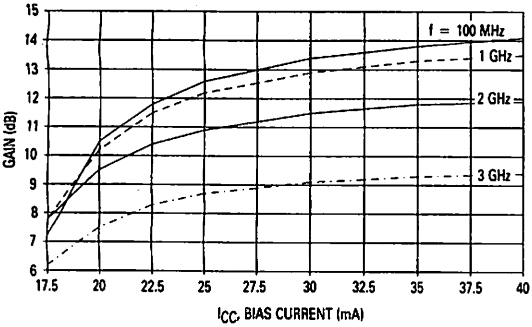

Figure 9. Gain versus Bias Current

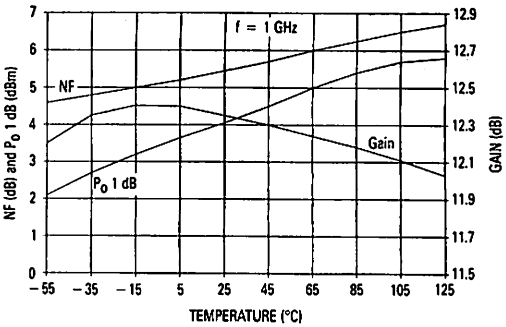

Figure 10. Output Power at 1 dB Gain Compression Noise Figure and Gain versus Temperature

MMIC AMPLIFIER APPLICATIONS INFORMATION

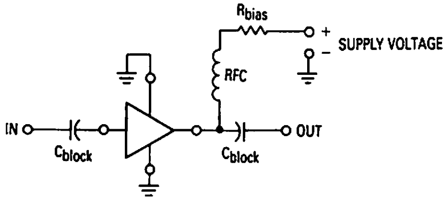

Figure 11. Typical Biasing Configuration

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Operation

Operation of the Monolithic Microwave Integrated Circuit as an amplifier is achieved by simply connecting it to 50 ohm driving source and load impedances with dc blocking capacitors at both input and output.

DC Bias

A positive current must be supplied to the device output terminal. Power supply decoupling elements must include resistive current limiting. Device output voltage at the recommended operating current of 25 mA is typically 5 Vdc, see Fig. 7, R_{bias} (Figure 9) is selected to permit the device to draw 25 mA. For example, when operating with a 12 Vdc supply:

$$R_{bias} = \frac{(12-5)}{0.025} = 280 \text{ ohms}$$

The nearest standard value of 270 ohms would suffice.

External Decoupling Impedance

In all cases the external bias (decoupling elements) must present an impedance which is large compared to the 50 Ω load impedance to minimize RF gain reduction. The loss in gain due to the decoupling impedance is given by the equation:

$$\text{Loss} = -20 \text{ Log } \frac{Z_D}{Z_D + 25} \text{ dB}$$

where Z_D = decoupling impedance in ohms. For example, if Z_D = 1 kΩ, Loss = 0.214 dB.

The RF choke is not mandatory, but including it improves gain by raising the dc supply voltage decoubling impedance. 4 turns of #26 AWG enameled wire wound on a ferrite bead is suggested for the choke.

Low Frequency Response

The value of the blocking capacitors determines the low frequency response of the amplifier. The following expression is used to determine the blocking capacitor value to yield a desired 3 dB low frequency corner (f_{LFC}).

$$C_{Block}(\text{Farads}) = \frac{1}{100\ \pi\ f_{LFC}(\text{Hz})}$$

Discontinued
10/93

MWA0304
MWA0311L
MWA0370

Monolithic Microwave Integrated Circuit

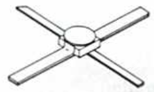
. . . designed for narrow or wideband IF and RF applications in industrial and commercial systems up to 3 GHz.

- 12 dB Gain at 500 MHz (Typ)
- Fully Cascadable
- 50 Ω Input and Output Impedance
- Choice of Package Types
  - Low Cost
  - Surface Mount
  - Hermetic
- Available In Both Standard Profile (MWA0311) and Low Profile (MWA0311L)
- Tape and Reel Packaging Options
- 10.5 dBm P_O 1 dB at 500 MHz (Typ)
- Unconditionally Stable

MONOLITHIC
MICROWAVE
INTEGRATED
CIRCUIT

CASE 317-01, STYLE 3
MWA0304

CASE 318A-05, STYLE 4
MWA0311L



CASE 303A-01, STYLE 3
MWA0370

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameters		Symbol	Ratings	Unit
Circuit Current (Note 1)		I_{CC}	40	mAdc
Input Power, RF		P_{in}	+16	dBm
Bias Voltage		V_{CC}	6	Vdc
Storage Temperature	0304/0311L 0370	T_{stg}	−65 to +150 −65 to +200	°C
Junction Temperature	0304/0311L 0370	T_J	150 200	°C

RECOMMENDED OPERATING CONDITIONS

Parameters	Symbol	Ratings	Unit
Operating Current	I_{CC}	35	mA
Source Impedance	Z_S	50 to 75	Ω
Load Impedance	Z_L	50 to 75	Ω

THERMAL CHARACTERISTICS

Thermal Resistance, Die to Case	MWA0304 MWA0311L MWA0370	$R_{\theta JC}$	150 200 130	°C/W

DEVICE MARKING

MWA0311L = 14

ELECTRICAL CHARACTERISTICS (T_A = 25°C, I_{CC} = 35 mA, Z_S = Z_L = 50 Ω, unless specified otherwise)

Characteristic	Symbol	Min	Typ	Max	Unit
Gain (f = 500 MHz)	G_T	10	12	—	dB
Gain Flatness (f = DC to 800 MHz — MWA0304/0311L) (f = DC to 1600 MHz — MWA0370)	—	 — —	 1 1	 — —	dB
Noise Figure (f = 100–1500 MHz)	NF	—	5.5	—	dB
Third Order Intercept Output Power (f_1 = 480 MHz, f_2 = 500 MHz)	ITO_1	—	24	—	dBm
Third Order Intercept Output Power (f_1 = 980 MHz, f_2 = 1000 MHz)	ITO_2	—	22	—	dBm
Second Order Intercept Output Power (F_1 = 480 MHz, f_2 = 500 MHz)	ISO_1	—	32.5	—	dBm
Second Order Intercept Output Power (f_1 = 980 MHz, f_2 = 1000 MHz)	ISO_2	—	29.5	—	dBm

Note 1: Based on maximum junction temperature and assumed MTBF of at least 10 years.

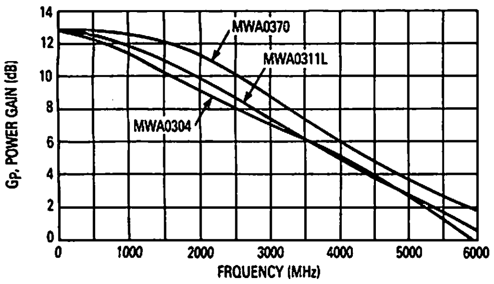


Figure 1. Gain versus Frequency

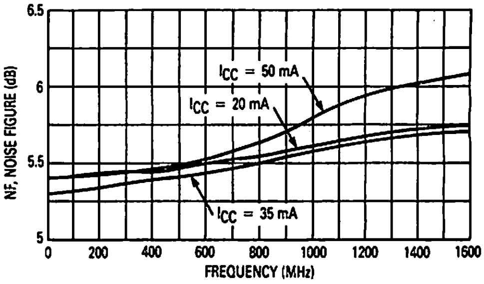


Figure 2. Noise Figure versus Frequency

MWA0304

Frequency (MHz)	S_{11} (mag)	S_{11} (ang)	S_{21} (dB)	S_{21} (mag)	S_{21} (ang)	S_{12} (mag)	S_{12} (ang)	S_{22} (mag)	S_{22} (ang)	K
100	0.059	168.5	12.61	4.27	172.9	0.123	3.2	0.169	−10.3	1.18
200	0.052	156.9	12.57	4.25	166.3	0.124	2.9	0.173	−18.8	1.18
400	0.044	125.1	12.35	4.15	153.3	0.124	6.1	0.183	−35.6	1.19
600	0.034	72.6	12.11	4.03	140.7	0.131	9.2	0.199	−49	1.18
800	0.052	19.1	11.75	3.87	128.5	0.134	11.5	0.21	−58.2	1.19
1000	0.08	−4.8	11.37	3.7	116.9	0.144	13.2	0.219	−66.9	1.17
1500	0.155	−41.1	10.23	3.25	90.3	0.162	14.8	0.243	−78	1.16
2000	0.185	−61.7	9.08	2.84	67.2	0.185	13	0.244	−87.9	1.16
2500	0.153	−83	8.03	2.52	45.9	0.207	10.1	0.235	−100.1	1.16
3000	0.085	−122	7.03	2.25	25.9	0.229	5.4	0.23	−114.1	1.17
3500	0.077	140.5	6.09	2.01	7.25	0.243	−1	0.231	−133	1.19
4000	0.186	93.7	5.08	1.79	−11	0.258	−6.7	0.23	−149.4	1.19
5000	0.443	62.4	2.7	1.36	−43.7	0.279	−17.4	0.236	173.2	1.14
6000	0.648	44.6	−0.22	0.97	−70.7	0.287	−31	0.274	127.6	1.09

Figure 3. Typical S S-Parameters and Stability Factor K

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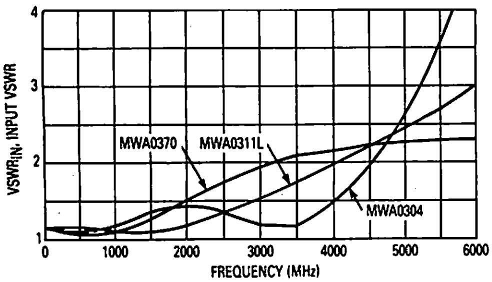

Figure 4. Input VSWR versus Frequency

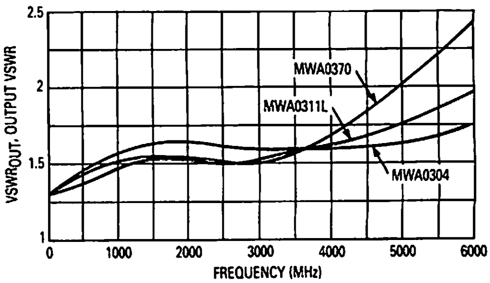

Figure 5. Output VSWR versus Frequency

MWA0311L

Frequency (MHz)	S_{11} (mag)	S_{11} (ang)	S_{21} (dB)	S_{21} (mag)	S_{21} (ang)	S_{12} (mag)	S_{12} (ang)	S_{22} (mag)	S_{22} (ang)	K
100	0.092	173.7	12.8	4.37	174.3	0.119	1.5	0.134	−12.8	1.19
200	0.089	166.7	12.77	4.35	168.8	0.119	5	0.139	−21.3	1.19
400	0.078	155.4	12.62	4.27	158.3	0.127	7.3	0.149	−42	1.16
600	0.074	143.6	12.47	4.2	147.9	0.129	13.4	0.165	−58.5	1.16
800	0.06	135.7	12.19	4.07	137.9	0.132	16.6	0.176	−72	1.17
1000	0.05	133.2	11.85	3.91	128.5	0.139	19.1	0.192	−84.9	1.16
1500	0.035	176.3	10.97	3.53	105.4	0.162	24.1	0.221	−107.3	1.12
2000	0.083	−159.1	9.88	3.12	84.4	0.184	25.9	0.209	−127	1.1
2500	0.15	−171.1	8.64	2.7	66.3	0.198	26	0.199	−139.8	1.12
3000	0.214	173.4	7.38	2.34	50.2	0.22	23.5	0.215	−146.9	1.11
3500	0.276	161.7	6.1	2.02	36.8	0.233	22.7	0.226	−148.7	1.13
4000	0.334	150.7	4.9	1.76	24.7	0.238	22.3	0.234	−145.3	1.16
5000	0.414	131.5	2.64	1.36	5.24	0.259	19.6	0.277	−140.5	1.17
6000	0.5	113.2	0.56	1.07	−10.5	0.284	17.3	0.327	−151.2	1.14

Figure 6. Typical S-Parameters and Stability Factor K

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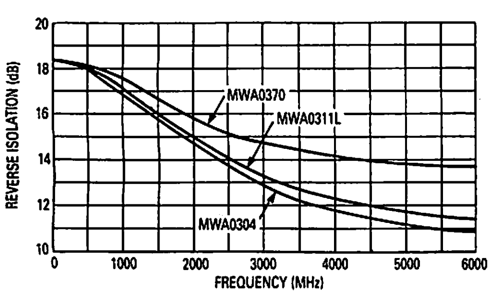

Figure 7. Reverse Isolation versus Frequency

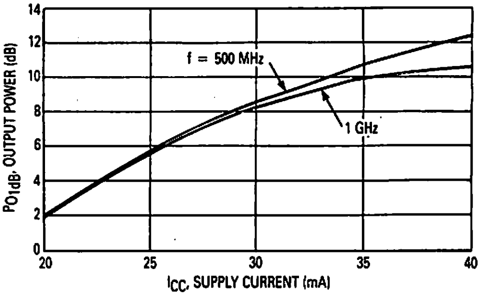

Figure 8. Output Power At 1 dB Gain Compression versus Bias Current

MWA0370

Frequency (MHz)	S_{11} (mag)	S_{11} (ang)	S_{21} (dB)	S_{21} (mag)	S_{21} (ang)	S_{12} (mag)	S_{12} (ang)	S_{22} (mag)	S_{22} (ang)	K
100	0.046	−178.6	12.84	4.39	175.2	0.12	1.1	0.181	−8.8	1.17
200	0.045	−178.4	12.84	4.38	170.5	0.121	2.2	0.178	−15.6	1.17
400	0.037	−174.5	12.8	4.37	161.3	0.122	4.6	0.185	−29.7	1.17
600	0.028	−156.5	12.76	4.34	151.9	0.125	6.7	0.191	−44	1.15
800	0.031	−125.5	12.68	4.31	142.7	0.129	8.4	0.198	−56.9	1.14
1000	0.047	−104.5	12.59	4.26	133.2	0.133	10.4	0.205	−68.5	1.12
1500	0.122	−99.6	12.11	4.03	109.5	0.147	12.1	0.216	−92.8	1.07
2000	0.201	−114.8	11.24	3.65	86.8	0.162	11	0.213	109.7	1.04
2500	0.27	−134	10.09	3.2	65.5	0.176	8.4	0.203	−117.5	1.03
3000	0.32	−151.4	8.73	2.73	47.4	0.185	5.3	0.2	−117.6	1.06
3500	0.354	−166.1	7.34	2.33	31.2	0.19	1.9	0.221	−116.8	1.11
4000	0.366	−179.6	6.02	2	18.2	0.196	−0.4	0.256	−118.1	1.16
5000	0.389	158.3	3.68	1.53	−3.4	0.205	−5.1	0.335	−126.2	1.26
6000	0.394	137.8	1.73	1.22	−21.9	0.214	−9.2	0.414	−137.1	1.33

Figure 9. Typical S-Parameters and Stability Factor K

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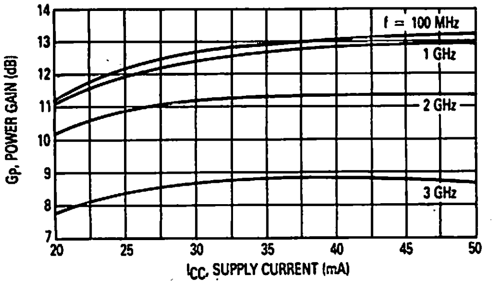

Figure 10. Power Gain versus Bias Current

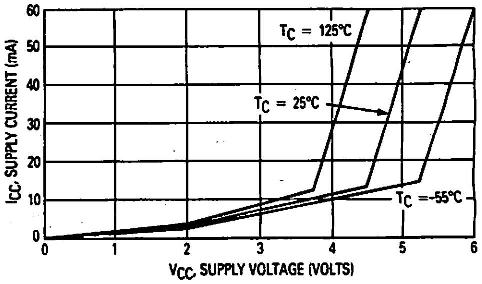

Figure 11. Bias Current versus Bias Voltage

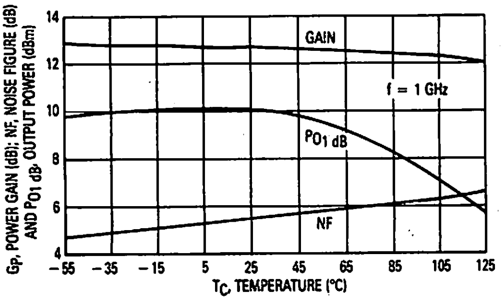

Figure 12. Output Power at 1 dB Gain Compression, Noise Figure and Gain versus Temperature

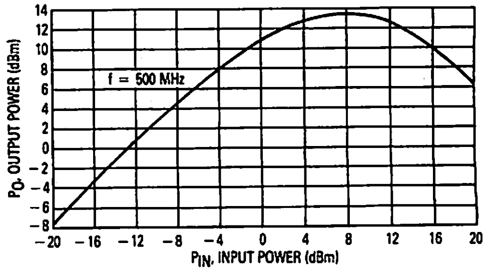

Figure 13. Output Power versus Input Power

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MMIC AMPLIFIER APPLICATIONS INFORMATION

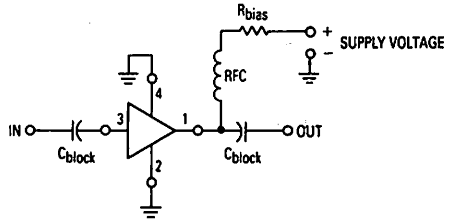

Figure 14. Typical Biasing Configuration

Operation

Operation of the Monolithic Microwave Integrated Circuit as an amplifier is achieved by simply connecting it to 50 ohm driving source and load impedances with dc blocking capacitors at both input and output.

DC Bias

A positive current must be supplied to the device output terminal. Power supply decoupling elements must include resistive current limiting. Device output voltage at the recommended operating current of 35 mA is typically 5 Vdc (see Fig. 11) R_{bias} (Figure 9) is selected to permit the device to draw 35 mA. For example, when operating with a 12 Vdc supply:

$$R_{bias} = \frac{(12-5)}{0.035} = 200 \text{ ohms}$$

External Decoupling Impedance

In all cases the external bias (decoupling elements) must present an impedance which is large compared to the 50 Ω load impedance to minimize RF gain reduction. The loss in gain due to the decoupling impedance is given by the equation:

$$\text{Loss} = -20 \text{ Log } \frac{Z_D}{Z_D + 25} \text{ dB}$$

Where Z_D = decoupling impedance in ohms. For example, if Z_D = 1 kΩ, Loss = 0.214 dB.

The RF choke is not mandatory, but including it improves gain by raising the dc supply voltage decoupling impedance. 4 turns of #26 AWG enameled wire would on a ferrite bead is suggested for the choke.

Low Frequency Response

The value of the blocking capacitors determines the low frequency response of the amplifier. The following expression is used to determine the blocking capacitor value to yield a desired 3 dB low frequency corner (f_{LFC}).

$$C_{Block}(\text{Farads}) = \frac{1}{100\ \tau\ f_{LFC}(\text{Hz})}$$

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MWA110
MWA120
MWA130

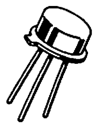
The RF Line

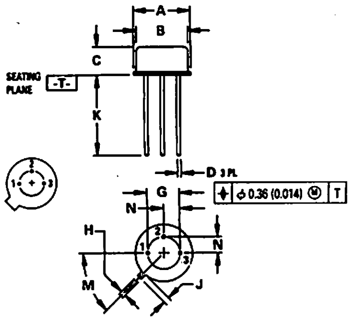
WIDEBAND HYBRID AMPLIFIERS

. . . single stage amplifiers designed for broadband linear applications up to 400 MHz.

- Low-Cost TO-39 Type Package
- Gain 14 dB Typ
- 50 Ω Input and Output Impedance
- Fully Cascadable for Any Gain
- Thin Film Construction
- Hermetic Package
- Guaranteed Performance from -25°C to +125°C

DC-400 MHz WIDEBAND GENERAL-PURPOSE HYBRID AMPLIFIERS





STYLE 2:
PIN 1. INPUT
2. OUTPUT
3. GROUND

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.50	0.305	0.335
C	3.81	4.57	0.165	0.185
D	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	—	0.500	—
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	

CASE 31A-03

MAXIMUM RATINGS

Rating	Symbol	Value MWA110	Value MWA120	Value MWA130	Unit
RF Input Power	P_{in}	←	100	→	mW
DC Supply Current	I_D	25	55	100	mA
Maximum Case Temperature	T_C	←	125	→	°C
Storage Temperature Range	T_{stg}	←	−65 to +200	→	°C

OPERATING CONDITIONS

Device Voltage	V_D	2.9	5.0	5.5	Vdc
Device Current	I_D	10	25	60	mAdc
Decoupling Impedance	Z_D	620	620	240	Ω

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	110	°C/W

ELECTRICAL CHARACTERISTICS (T_C = -25 to +125°C, 50 Ω system and specified operating conditions)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	0.1	–	400	MHz
Power Gain (f = 100 MHz)		G_p	13	14	–	dB
Response Flatness		F	–	0	±1.0	dB
Input VSWR	MWA110/120	–	–	–	2.5:1	–
	MWA130	–	–	–	3:1	–
Output VSWR	MWA110/120/130	–	–	–	2.5:1	–
Output @ 1 dB Gain Compression						dBm
	MWA110		–	-2.5	–	
	MWA120		–	+8.2	–	
	MWA130		–	+18	–	
Noise Figure		NF				dB
	MWA110		–	4.0	–	
	MWA120		–	5.5	–	
	MWA130		–	7.0	–	
Reverse Isolation		P_{RI}				dB
	MWA110		–	18.8	–	
	MWA120		–	19.2	–	
	MWA130		–	16.8	–	
Harmonic Output		d_{so}				dB
	MWA110 (P_{out} = -9 dBm)		–	-24	–	
	MWA120 (P_{out} = 0 dBm)		–	-34	–	
	MWA130 (P_{out} = +10 dBm)		–	-35	–	

FIGURE 1 — DEVICE VOLTAGE versus DEVICE CURRENT

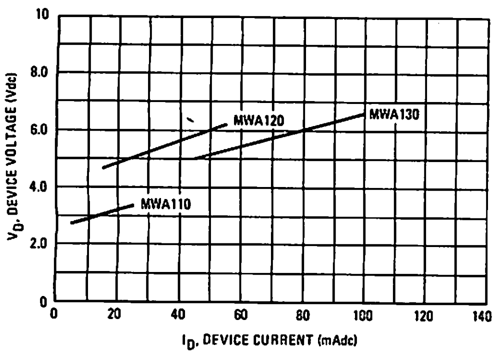


FIGURE 2 — DEVICE CURRENT versus CASE TEMPERATURE

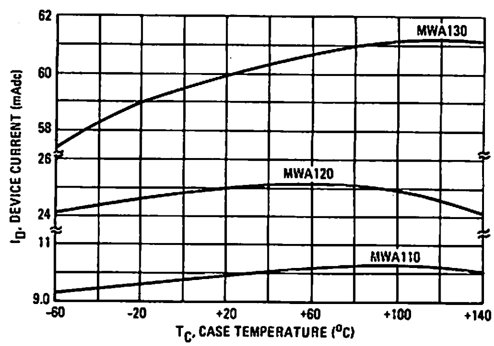


FIGURE 3 — POWER GAIN versus FREQUENCY

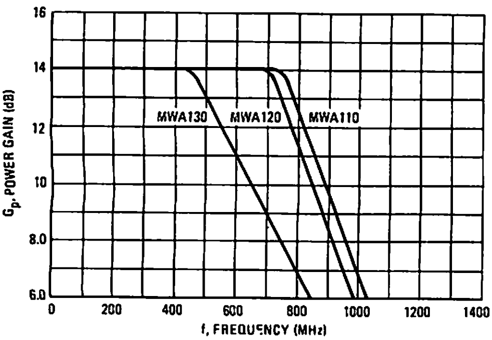


FIGURE 4 — POWER GAIN versus DEVICE CURRENT
f = 400 MHz

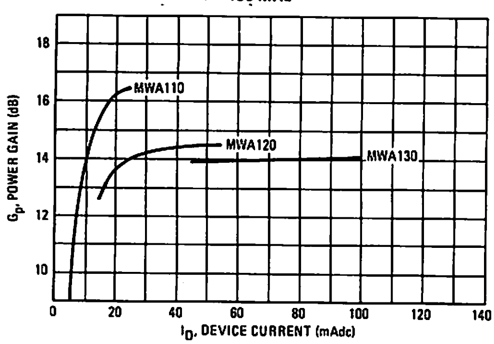


FIGURE 5 — POWER GAIN versus CASE TEMPERATURE
f = 100 MHz

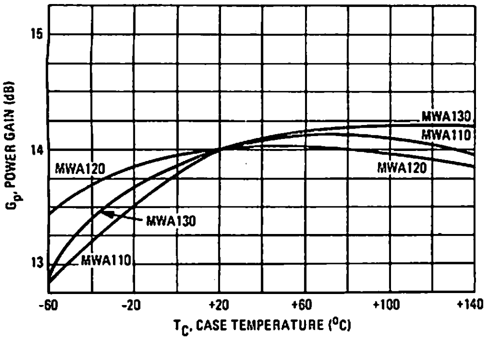


FIGURE 6 — POWER GAIN versus CASE TEMPERATURE
f = 400 MHz

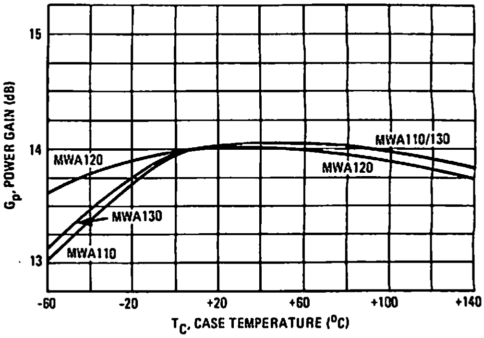


FIGURE 7 — VSWR versus FREQUENCY
MWA110

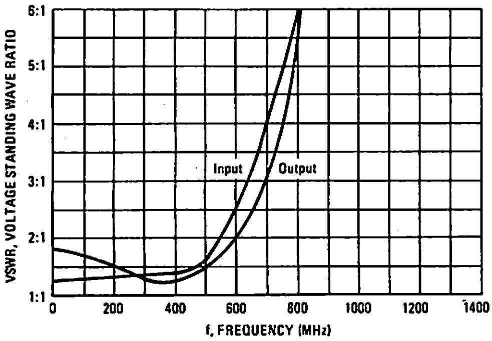


FIGURE 8 — VSWR versus FREQUENCY
MWA120

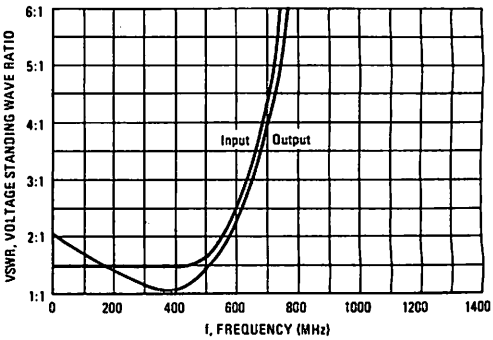


FIGURE 9 — VSWR versus FREQUENCY
MWA130

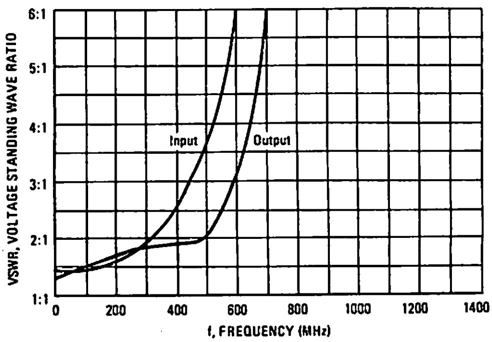
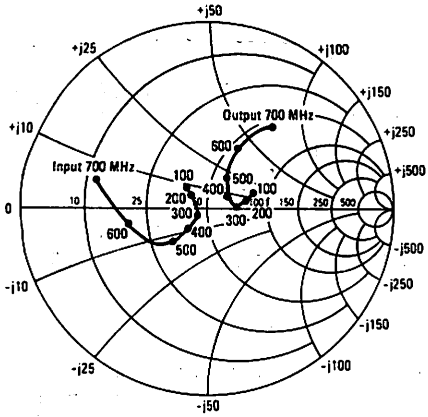
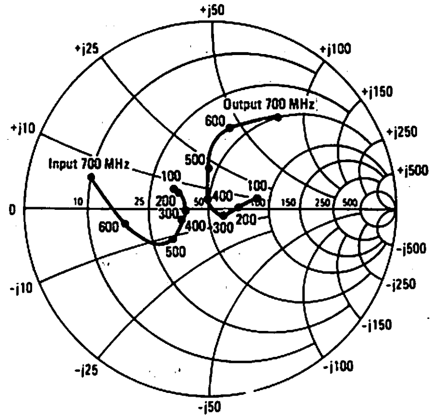


FIGURE 10 — INPUT AND OUTPUT IMPEDANCE versus FREQUENCY MWA110



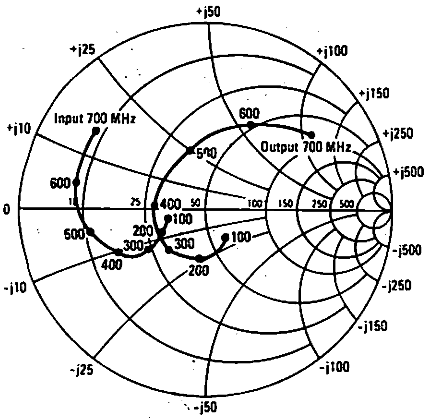
Coordinates in Ohms

FIGURE 11 — INPUT AND OUTPUT IMPEDANCE versus FREQUENCY MWA120



Coordinates in Ohms

FIGURE 12 — INPUT AND OUTPUT IMPEDANCE versus FREQUENCY MWA130



Coordinates in Ohms

FIGURE 13 — 1.0 dB GAIN COMPRESSION versus FREQUENCY

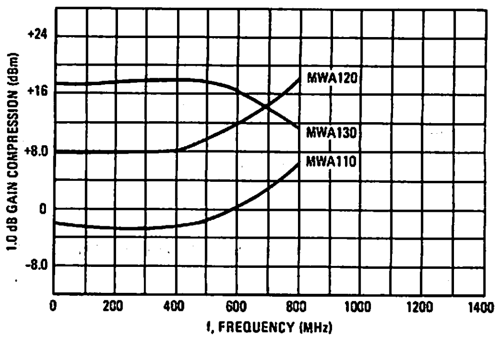


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FIGURE 14 – 1.0 dB GAIN COMPRESSION versus DEVICE CURRENT f = 400 MHz

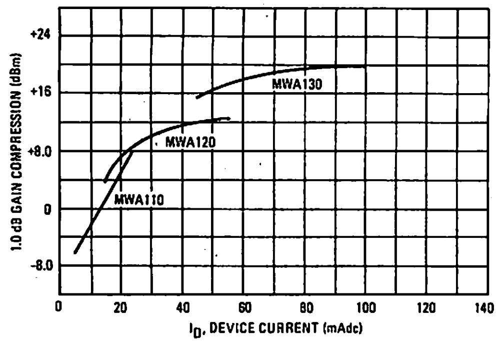

FIGURE 15 – 1.0 dB GAIN COMPRESSION versus CASE TEMPERATURE f = 400 MHz

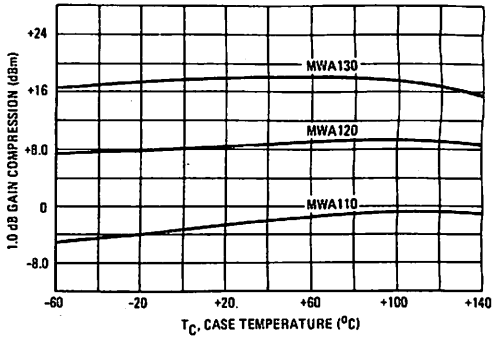

FIGURE 16 – NOISE FIGURE versus FREQUENCY

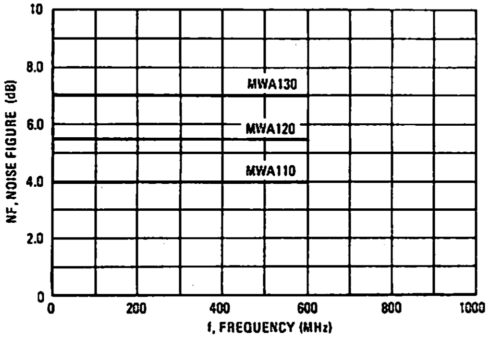

FIGURE 17 – REVERSE ISOLATION versus FREQUENCY

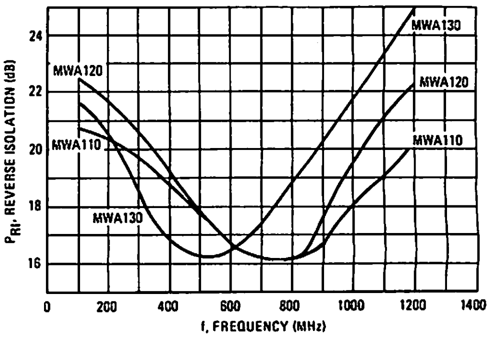

FIGURE 18 – SECOND HARMONIC OUTPUT versus FREQUENCY

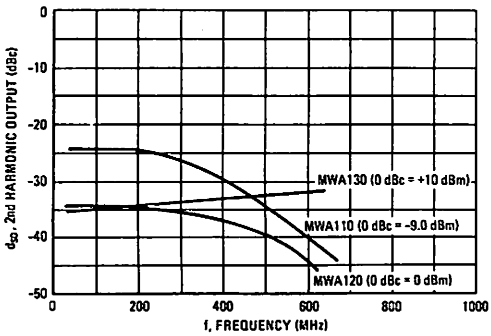

FIGURE 19 – SECOND AND THIRD ORDER INTERCEPT MWA110

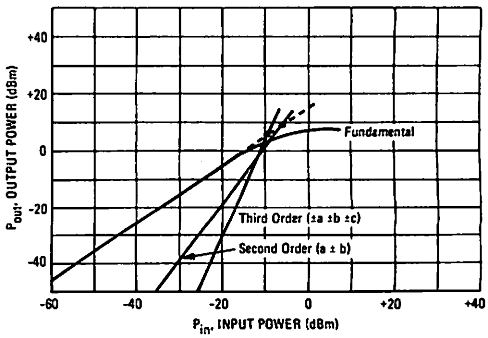

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FIGURE 20 — SECOND AND THIRD ORDER INTERCEPT
MWA120

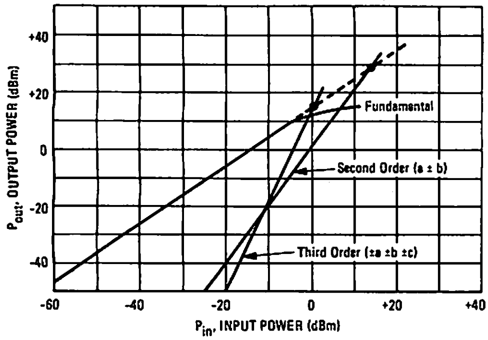

FIGURE 21 — SECOND AND THIRD ORDER INTERCEPT
MWA130

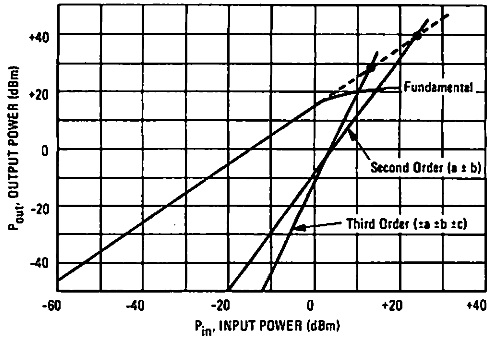

FIGURE 22 — INTERMODULATION DISTORTION
versus POWER OUTPUT
MWA110

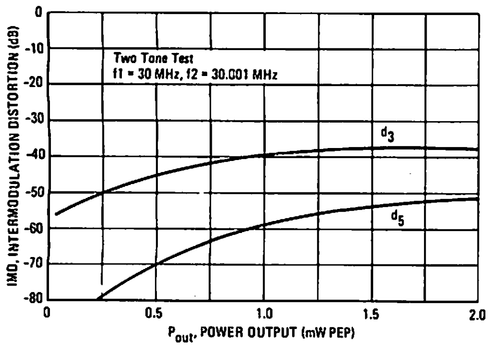

FIGURE 23 — INTERMODULATION DISTORTION
versus POWER OUTPUT
MWA120

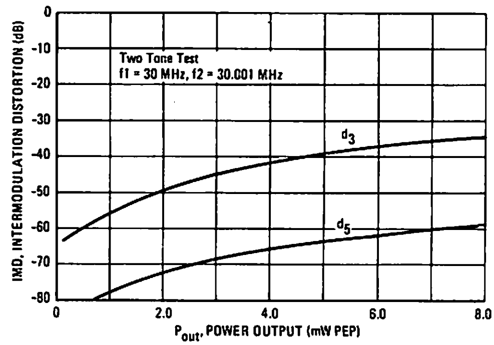

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FIGURE 24 — INTERMODULATION DISTORTION
versus POWER OUTPUT
MWA130

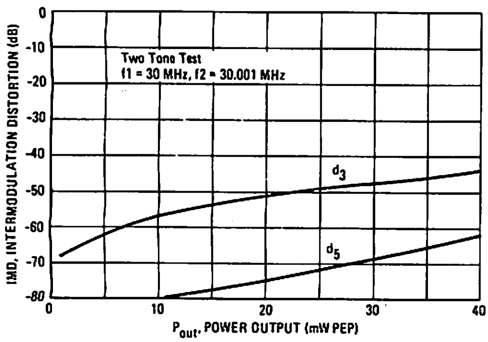
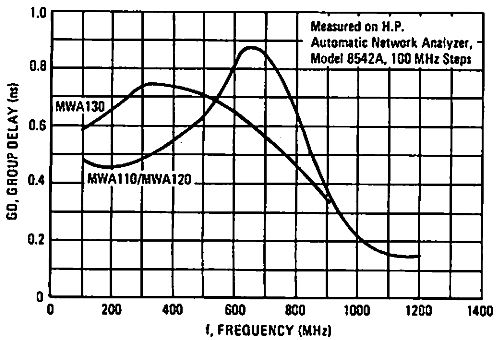


FIGURE 25 — GROUP DELAY versus FREQUENCY



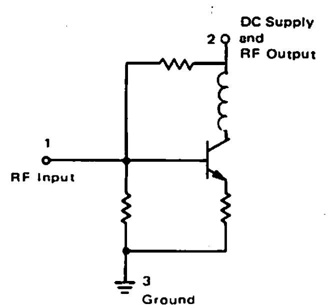
MWA SERIES HYBRID AMPLIFIER APPLICATIONS INFORMATION

The MWA series hybrid amplifiers are designed for wideband general purpose applications in 50 Ω systems. Fully cascadable for any gain combination, operable at voltages as low as 3 Vdc, and external control of the low frequency corner make the MWA amplifiers extremely versatile gain blocks.

Basic Circuit Configuration

Figure 26 shows the basic internal circuit. It is important to note that the specified operating conditions of voltage, current, and external decoupling impedance must be applied to the units in order to achieve the published electrical characteristics.

FIGURE 26 – INTERNAL CIRCUIT



Amplifier Application

The circuit schematic for a simple amplifier design is shown in Figure 27. External to the MWA hybrid amplifier the only components required are:

Decoupling elements – Bypass Capacitor
Decoupling Impedance
(resistor/inductor)
DC Blocking Capacitors at the RF input and output.

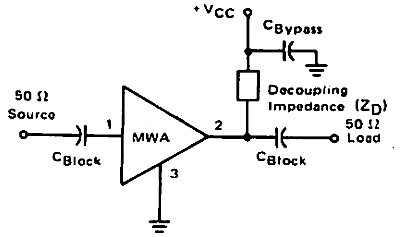
External Decoupling Impedance

In all cases the external bias (decoupling elements) must present an impedance which is large compared to the 50 Ω load impedance to minimize RF gain reduction. The loss in gain due to the decoupling impedance is given by the equation:

$$\text{Loss} = 20 \text{ Log } \frac{Z_D}{Z_D + 25} \text{ dB}$$

where Z_D = decoupling impedance in ohms. For example, if Z_D = 1 kΩ, Loss = 0.214 dB.

FIGURE 27 – AMPLIFIER SCHEMATIC DIAGRAM



Supply Voltage

The value of the external decoupling resistive impedance (R_D) determines the supply voltage ($+V_{CC}$) and is determined by the following equation:

$$V_{CC} = R_D \times I_D + V_D$$

where I_D and V_D are the device current and voltage stated in the data sheet. For example, for MWA110,

$$I_D = 10 \text{ mA}$$
$$V_D = 2.9 \text{ V}$$

and, if R_D = 330 Ω, then

$$V_{CC} = 6.2 \text{ V}$$

More commonly V_{CC} is predetermined and R_D may be calculated from:

$$R_D = \frac{V_{CC} - V_D}{I_D}$$

An RF choke is not recommended for use as a decoupling impedance without also using a resistor having an appropriate value.

Low Frequency Response

The value of the blocking capacitors determines the low frequency response of the amplifier. The following expression is used to determine the blocking capacitor value to yield a desired 3 dB low frequency corner (f_{LFC}).

$$C_{Block}(\text{Farads}) = \frac{1}{100\,\pi\, f_{LFC}(\text{Hz})}$$

Bypass Capacitor

The reactive impedance of the bypass capacitor should be small compared to the impedance of the decoupling element at the lowest frequency of operation.

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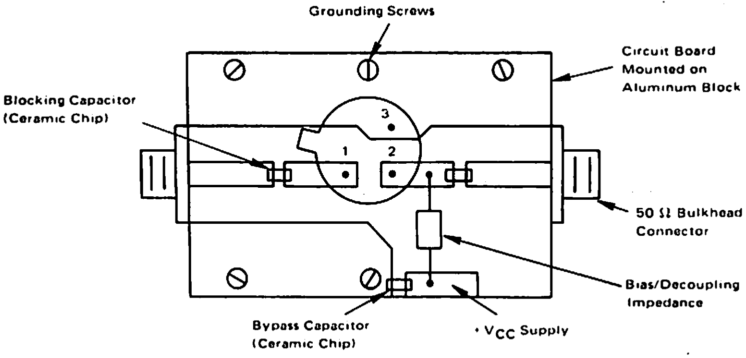
FIGURE 28 — TEST FIXTURE



Note: The circuitry indicated is on the underside of the printed circuit board with sockets for the amplifier pins. The case of the amplifier should contact the printed circuit board top surface to ensure effective RF grounding.

Text Fixture

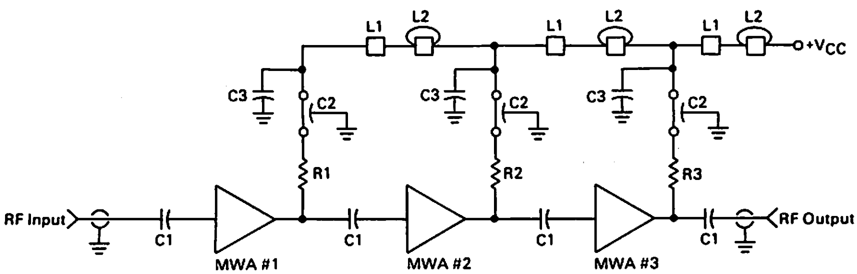
The 50 Ω input/output impedance levels of the MWA hybrids are most easily preserved on a circuit board by using 50 Ω microstrip transmission lines. Figure 28 is an example of a circuit board layout which utilizes microstrip transmission lines in conjunction with other sound RF construction techniques.

The characteristic impedance and corresponding line width of the microstrip are a function of the circuit board dielectric constant and thickness. The table lists appropriate line widths for 50 Ω microstrip lines on commonly used circuit board materials.

MATERIAL TYPE	DIELECTRIC CONSTANT	DIELECTRIC THICKNESS INCHES	LINE WIDTH INCHES
Teflon-Fiberglass	2.5	0.03125 0.0625	0.090 0.180
Fiberglass Epoxy	5.0	0.0625	0.100

As in all good RF circuit designs, care should be taken to minimize parasitic lead inductances and to provide adequate grounding.

FIGURE 29 — TYPICAL CASCADE



The dc isolation components shown are critical in maintaining good stability in multi-stage designs. Keep Pin #3 (Ground) as short as possible preferably soldering the case to the ground plane for best gain flatness to 1000 MHz.

C1 — For operation to 400 MHz, 1000 pF, 50 mil Chip Capacitor - ATC 50 mil Case (5.0 MHz L.F.)
C1 — For operation to 1000 MHz, 0.018 mF, Chip Capacitor for 0.25 MHz L.F. Cut-Off
C2 — Feedthru Capacitor Centralab SFT-102, 1000 pF or Metuchen 54-794002-681M, 680 pF
C3 — 0.1 μF Sprague 3CZ5U104X0050C5 - 50 Volt
L1 — Ferroxcube Shielding Bead 56-590-65/4A - Single Wire
L2 — Ferroxcube Shielding Bead 56-590-65/4A - 2 Turns #26 AWG

Cascading

The inherent stability of the MWA hybrid modules makes possible the cascading of two or more units with no oscillatory problems. Figure 29 shows a typical 3 hybrid cascade with measured data for 400 MHz and 1000 MHz hybrids.

	Cascade 1	Cascade 2
Frequency Range	0.25 to 400 MHz	5.0 to 1000 MHz
Gain	43.5 dB	20.5 dB
Gain Flatness	± 1.0 dB	± 0.75 dB
Input VSWR	2.0:1	2.4:1
Output VSWR	1.2:1	2.1:1
V_{CC} Supply	12 Vdc	33 Vdc
I Supply	44 mAdc	150 mAdc
MWA #1	MWA110	MWA320
MWA #2	MWA110	MWA330
MWA #3	MWA120	MWA330
R1	1000 Ω	1000 Ω
R2	1000 Ω	500 Ω
R3	300 Ω	500 Ω

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

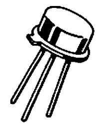
MWA131

The RF Line
Wideband Hybrid Amplifier

. . . single stage amplifiers designed for broadband linear applications up to 400 MHz.

- Low-Cost TO-39 Type Package
- Gain 15 dB Typ @ f = 100 MHz
- 50 Ω Input and Output Impedance
- Fully Cascadable for Any Gain
- Thin Film Construction
- Hermetic Package
- Guaranteed Performance from −25°C to +125°C
- 20 dBm P_O 1.0 dB Typ (100 MHz)

DC-400 MHz WIDEBAND GENERAL-PURPOSE HYBRID AMPLIFIER



CASE 31A-03, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Input Power	P_{in}	100	mW
DC Supply Current	I_D	120	mA
Maximum Case Temperature	T_C	125	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

OPERATING CONDITIONS

Device Voltage	V_D	5.5	Vdc
Device Current	I_D	90	mAdc
Decoupling Impedance	Z_D	240	Ω

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_C = −25 to +125°C, 50 Ω system and specified operating conditions)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	0.1	—	400	MHz
Power Gain (f = 100 MHz)	G_p	13	14	—	dB
Response Flatness	F	—	0	±1.0	dB
Input VSWR (f = 400 MHz)	—	—	—	3:1	—
Output VSWR (f = 400 MHz)	—	—	—	2:1	—
Output @ 1.0 dB Gain Compression (f = 100 MHz) (f = 400 MHz)		— —	20 19	— —	dBm
Noise Figure (f = 400 MHz)	NF	—	5.0	—	dB
Reverse Isolation (f = 400 MHz)	P_{RI}	—	18	—	dB
Harmonic Output — 2nd Order (f = 400 MHz, P_{out} = +10 dBm)	d_{so}	—	−35	—	dBc
Second Order Intercept P_o (f_1 = 380 MHz, f_2 = 400 MHz)	ISO	—	50	—	dBm
Third Order Intercept P_o (f_1 = 380 MHz, f_2 = 400 MHz)	ITO	—	30	—	dBm

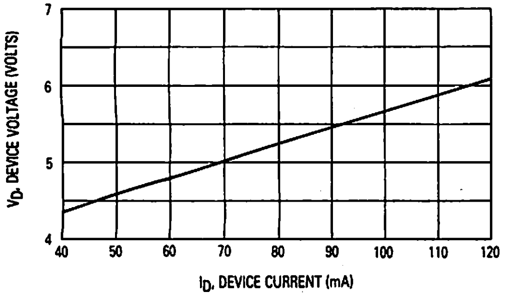


Figure 1. Device Voltage versus Device Current

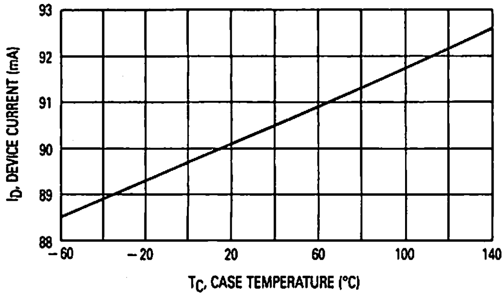


Figure 2. Device Current versus Case Temperature

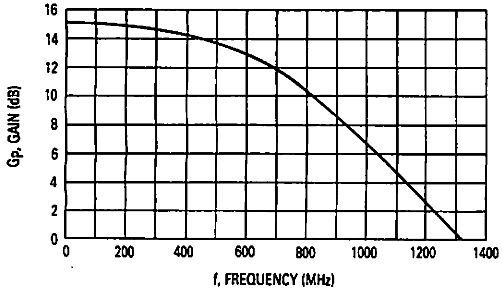


Figure 3. Power Gain versus Frequency

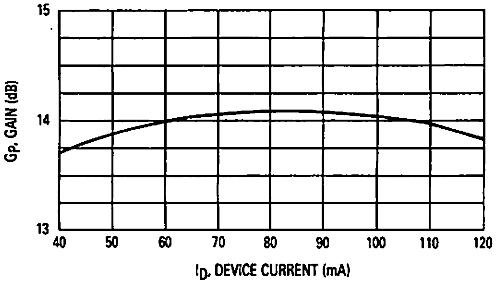


Figure 4. Power Gain versus Device Current
f = 400 MHz

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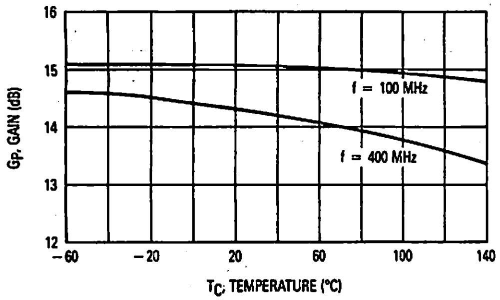

Figure 5. Power Gain versus Case Temperature

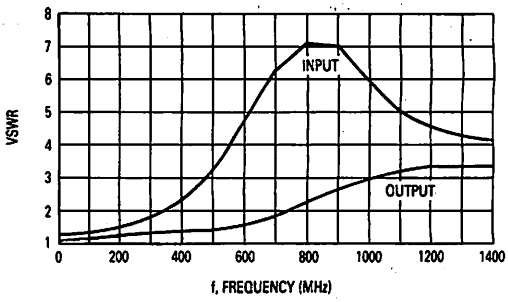

Figure 6. VSWR versus Frequency

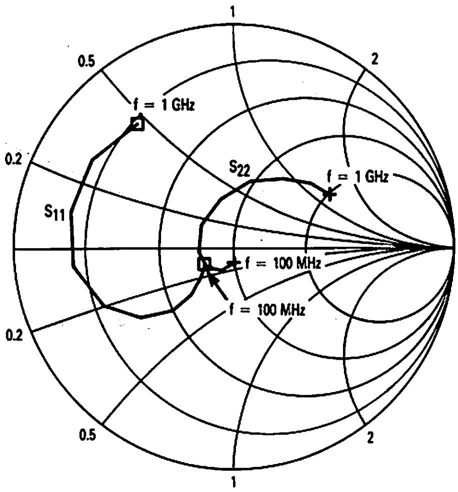

Figure 7. S_{11} and S_{22} versus Frequency

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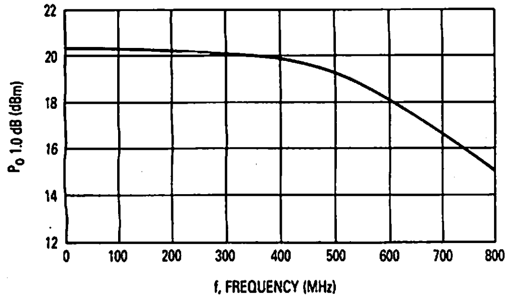

Figure 8. Output Power at 1.0 dB Gain Compression versus Frequency

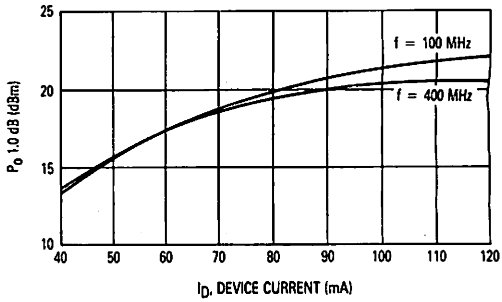

Figure 9. Output Power at 1.0 dB Gain Compression versus Device Current

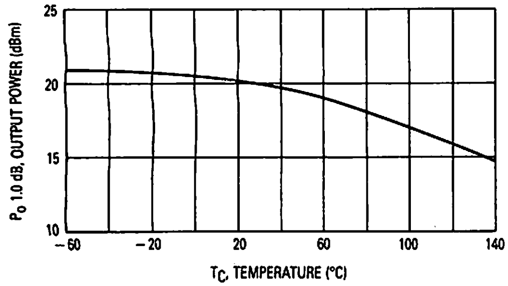

Figure 10. Output Power at 1.0 dB Gain Compression versus Case Temperature f = 400 MHz

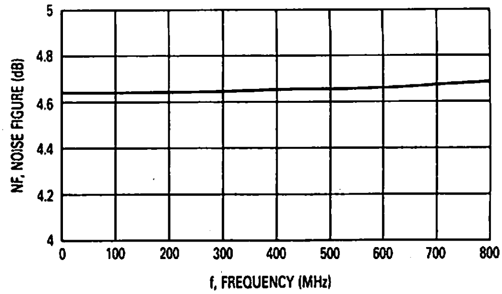

Figure 11. Noise Figure versus Frequency

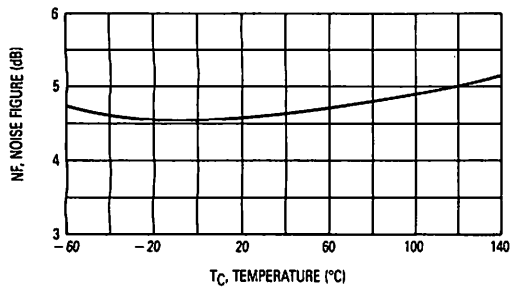

Figure 12. Noise Figure versus Temperature f = 400 MHz

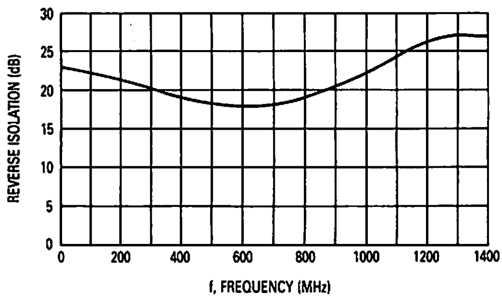

Figure 13. Reverse Isolation versus Frequency

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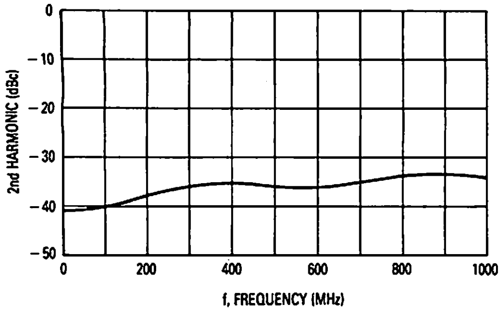


Figure 14. Second Harmonic Output versus Frequency
0 dBc = +10 dBm

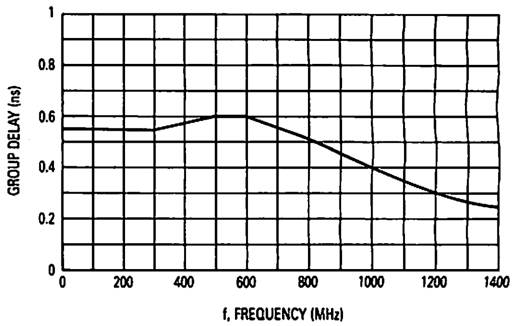


Figure 15. Group Delay versus Frequency

Frequency (MHz)	S_{11} (mag)	S_{11} (ang)	S_{21} (dB)	S_{21} (mag)	S_{21} (ang)	S_{12} (mag)	S_{12} (ang)	S_{22} (mag)	S_{22} (ang)	K
100	0.146	−152.1	15.07	5.67	160.0	0.077	8.90	0.071	−86.20	1.33
200	0.202	−137.9	14.88	5.55	140.2	0.085	13.6	0.121	−116.9	1.22
300	0.292	−132.4	14.62	5.38	120.3	0.098	15.2	0.149	−142.1	1.09
400	0.403	−134.6	14.29	5.18	100.4	0.112	12.9	0.163	−173.1	0.96
500	0.527	−142.9	13.83	4.91	79.5	0.122	6.60	0.178	146.4	0.87
600	0.649	−156.5	13.06	4.50	57.8	0.129	−1.50	0.224	106.2	0.81
700	0.733	−173.3	11.93	3.95	36.5	0.125	−11.6	0.305	75.9	0.79
800	0.759	167.9	10.41	3.32	16.7	0.112	−19.3	0.384	54.3	0.88
900	0.753	148.3	8.64	2.70	−1.60	0.096	−26.4	0.453	39.8	1.07
1000	0.711	127.8	6.71	2.17	−17.7	0.079	−29.7	0.498	28.2	1.50
1100	0.668	107.4	4.71	1.72	−32.2	0.060	−27.6	0.525	20.1	2.34
1200	0.641	89.3	2.54	1.34	−44.9	0.051	−20.3	0.542	12.8	3.43
1300	0.620	72.3	0.43	1.05	−55.5	0.043	−7.40	0.543	5.9	5.08
1400	0.611	57.8	−1.67	0.83	−65.9	0.044	5.40	0.543	−1.4	6.31
1500	0.605	45.2	−3.79	0.65	−74.6	0.049	15.9	0.551	−10.5	7.05

Table 1. S-Parameters

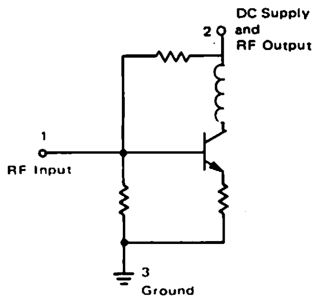
MWA SERIES HYBRID AMPLIFIER APPLICATIONS INFORMATION

The MWA series hybrid amplifiers are designed for wideband general purpose applications in 50 Ω systems. Fully cascadable for any gain combination, operable at voltages as low as 3 Vdc, and external control of the low frequency corner make the MWA amplifiers extremely versatile gain blocks.

Basic Circuit Configuration

Figure 26 shows the basic internal circuit. It is important to note that the specified operating conditions of voltage, current, and external decoupling impedance must be applied to the units in order to achieve the published electrical characteristics.

FIGURE 26 – INTERNAL CIRCUIT



Amplifier Application

The circuit schematic for a simple amplifier design is shown in Figure 27. External to the MWA hybrid amplifier the only components required are:

Decoupling elements – Bypass Capacitor
Decoupling Impedance
(resistor/inductor)
DC Blocking Capacitors at the RF input and output.

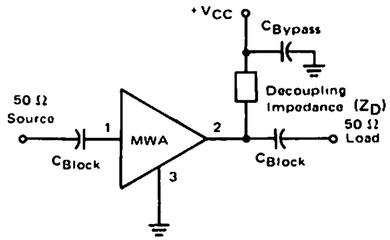
External Decoupling Impedance

In all cases the external bias (decoupling elements) must present an impedance which is large compared to the 50 Ω load impedance to minimize RF gain reduction. The loss in gain due to the decoupling impedance is given by the equation:

$$\text{Loss} = -20 \text{ Log } \frac{Z_D}{Z_D + 25} \text{ dB.}$$

where Z_D = decoupling impedance in ohms. For example, if Z_D = 1 kΩ, Loss = 0.214 dB.

FIGURE 27 – AMPLIFIER SCHEMATIC DIAGRAM



Supply Voltage

The value of the external decoupling resistive impedance (R_D) determines the supply voltage ($+V_{CC}$) and is determined by the following equation:

$$V_{CC} = R_D \times I_D + V_D$$

where I_D and V_D are the device current and voltage stated in the data sheet. For example, for MWA110,

$$I_D = 10 \text{ mA}$$
$$V_D = 2.9 \text{ V}$$

and, if R_D = 330 Ω, then

$$V_{CC} \doteq 6.2 \text{ V}$$

More commonly V_{CC} is predetermined and R_D may be calculated from:

$$R_D = \frac{V_{CC} - V_D}{I_D}$$

Low Frequency Response

The value of the blocking capacitors determines the low frequency response of the amplifier. The following expression is used to determine the blocking capacitor value to yield a desired 3 dB low frequency corner (f_{LFC}).

$$C_{Block}(\text{Farads}) = \frac{1}{100\,\pi\, f_{LFC}(\text{Hz})}$$

Bypass Capacitor

The reactive impedance of the bypass capacitor should be small compared to the impedance of the decoupling element at the lowest frequency of operation.

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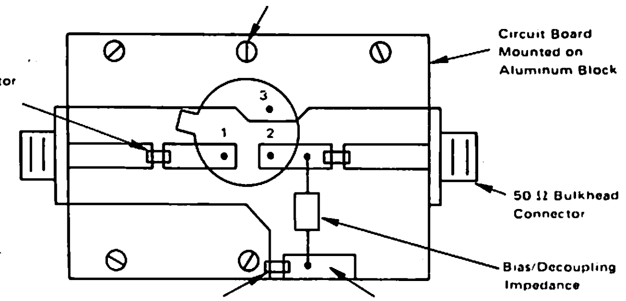
FIGURE 28 — TEST FIXTURE



Note: The circuitry indicated is on the underside of the printed circuit board with sockets for the amplifier pins. The case of the amplifier should contact the printed circuit board top surface to ensure effective RF grounding.

Text Fixture

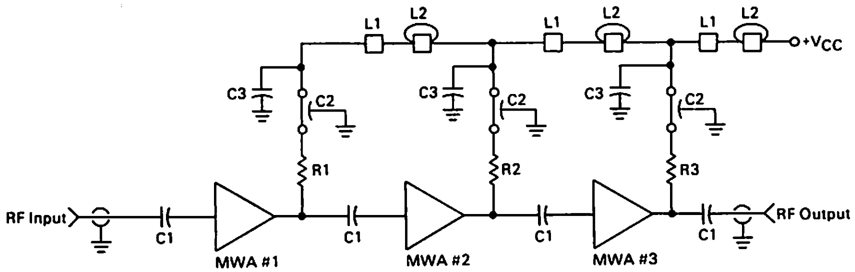
The 50 Ω input/output impedance levels of the MWA hybrids are most easily preserved on a circuit board by using 50 Ω microstrip transmission lines. Figure 28 is an example of a circuit board layout which utilizes microstrip transmission lines in conjunction with other sound RF construction techniques.

The characteristic impedance and corresponding line width of the microstrip are a function of the circuit board dielectric constant and thickness. The table lists appropriate line widths for 50 Ω microstrip lines on commonly used circuit board materials.

MATERIAL TYPE	DIELECTRIC CONSTANT	DIELECTRIC THICKNESS INCHES	LINE WIDTH INCHES
Teflon-Fiberglass	2.5	0.03125 0.0625	0.090 0.180
Fiberglass Epoxy	5.0	0.0625	0.100

As in all good RF circuit designs, care should be taken to minimize parasitic lead inductances and to provide adequate grounding.

FIGURE 29 — TYPICAL CASCADE



The dc isolation components shown are critical in maintaining good stability in multi-stage designs. Keep Pin #3 (Ground) as short as possible preferably soldering the case to the ground plane for best gain flatness to 1000 MHz.

C1 — For operation to 400 MHz, 1000 pF, 50 mil Chip Capacitor - ATC 50 mil Case (5.0 MHz L.F.)
C1 — For operation to 1000 MHz, 0.018 mF, Chip Capacitor for 0.25 MHz L.F. Cut-Off
C2 — Feedthru Capacitor Centralab SFT-102, 1000 pF or Metuchen 54-794002-681M, 680 pF
C3 — 0.1 μF Sprague 3CZ5U104X0050C5 - 50 Volt
L1 — Ferroxcube Shielding Bead 56-590-65/4A - Single Wire
L2 — Ferroxcube Shielding Bead 56-590-65/4A - 2 Turns #26 AWG

	Cascade 1	Cascade 2
Frequency Range	0.25 to 400 MHz	5.0 to 1000 MHz
Gain	43.5 dB	20.5 dB
Gain Flatness	± 1.0 dB	± 0.75 dB
Input VSWR	2.0:1	2.4:1
Output VSWR	1.2:1	2.1:1
V_{CC} Supply	12 Vdc	33 Vdc
I Supply	44 mAdc	150 mAdc
MWA #1	MWA110	MWA320
MWA #2	MWA110	MWA330
MWA #3	MWA120	MWA330
R1	1000 Ω	1000 Ω
R2	1000 Ω	500 Ω
R3	300 Ω	500 Ω

Cascading

The inherent stability of the MWA hybrid modules makes possible the cascading of two or more units with no oscillatory problems. Figure 29 shows a typical 3 hybrid cascade with measured data for 400 MHz and 1000 MHz hybrids.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MWA210
MWA220
MWA230

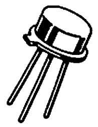
The RF Line

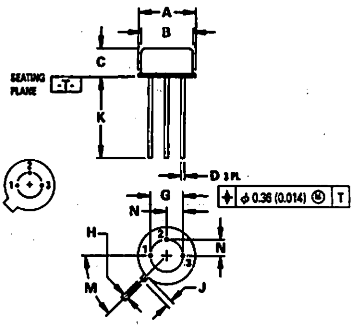
WIDEBAND HYBRID AMPLIFIERS

. . . single stage amplifiers designed for broadband linear applications up to 600 MHz.

- Low-Cost TO-39 Type Package
- Gain 10 dB Typ
- 50 Ω Input and Output Impedance
- Fully Cascadable for Any Gain
- Thin Film Construction
- Hermetic Package
- Guaranteed Performance from −25°C to +100°C

DC-600 MHz WIDEBAND GENERAL-PURPOSE HYBRID AMPLIFIERS





STYLE 2:
PIN 1. INPUT
2. OUTPUT
3. GROUND

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.50	0.305	0.335
C	3.81	4.57	0.165	0.185
D	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	—	0.500	—
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	

CASE 31A-03

MAXIMUM RATINGS

Rating	Symbol	Value MWA210	Value MWA220	Value MWA230	Unit
RF Input Power	P_{in}	← 100 →			mW
DC Supply Current	I_D	25	55	100	mA
Maximum Case Temperature	T_C	← 125 →			°C
Storage Temperature Range	T_{stg}	← −65 to +200 →			°C

OPERATING CONDITIONS

Device Voltage	V_D	1.75	3.2	4.4	Vdc
Device Current	I_D	10	25	60	mAdc
Decoupling Impedance	Z_D	620	620	240	Ω

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	110	°C/W

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ELECTRICAL CHARACTERISTICS (T_C = –25 to +100°C, 50 Ω system and specified operating conditions)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	0.1	–	600	MHz
Power Gain (f = 100 MHz)		G_p	9.0	10	–	dB
Response Flatness		F	–	0	±1.0	dB
Input VSWR	MWA210/220	–	–	–	2.5:1	–
	MWA230	–	–	–	3:1	–
Output VSWR	MWA210/220/230	–	–	–	2.5:1	–
Output @ 1 dB Gain Compression						dBm
	MWA210		–	+1.5	–	
	MWA220		–	+10.5	–	
	MWA230		–	+18.5	–	
Noise Figure		NF				dB
	MWA210		–	6.0	–	
	MWA220		–	6.5	–	
	MWA230		–	7.5	–	
Reverse Isolation		P_{RI}				dB
	MWA210		–	13.5	–	
	MWA220		–	14.5	–	
	MWA230		–	12.9	–	
Harmonic Output		d_{so}				dB
	MWA210 (P_{out} = -9.0 dBm)		–	-29	–	
	MWA220 (P_{out} = 0 dBm)		–	-36	–	
	MWA230 (P_{out} = +10 dBm)		–	-36	–	

FIGURE 1 — DEVICE VOLTAGE versus DEVICE CURRENT

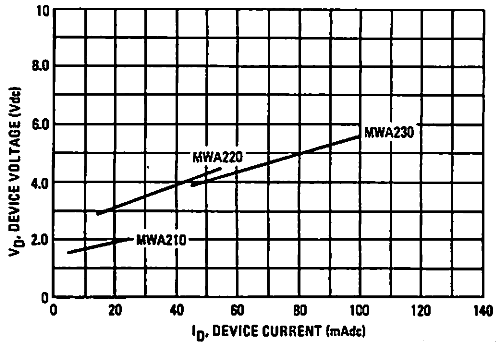

FIGURE 2 — DEVICE CURRENT versus CASE TEMPERATURE

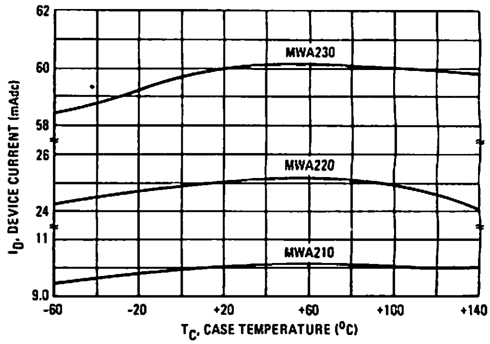

FIGURE 3 — POWER GAIN versus FREQUENCY

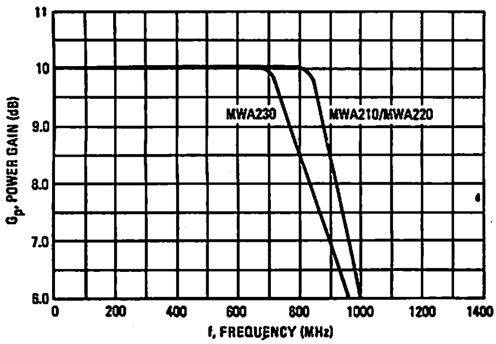

FIGURE 4 — POWER GAIN versus DEVICE CURRENT
f = 600 MHz

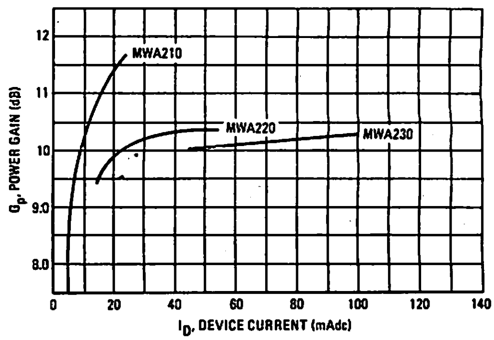

FIGURE 5 – POWER GAIN versus CASE TEMPERATURE
f = 100 MHz

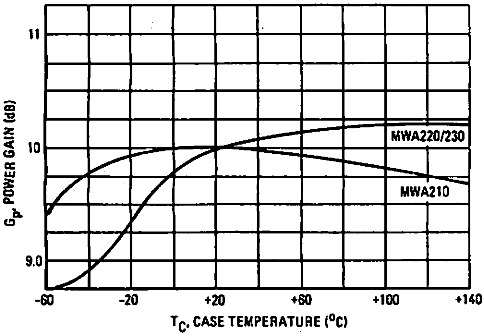

FIGURE 6 – POWER GAIN versus CASE TEMPERATURE
f = 600 MHz

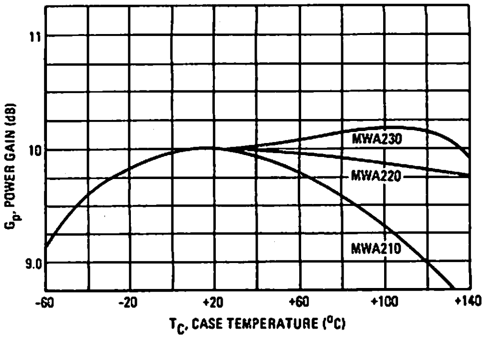

FIGURE 7 – VSWR versus FREQUENCY
MWA210

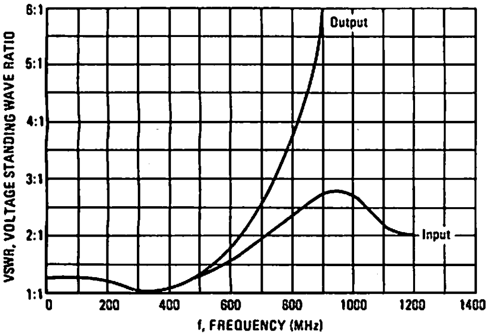

FIGURE 8 – VSWR versus FREQUENCY
MWA220

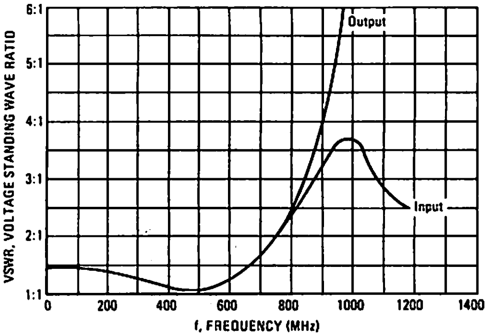

FIGURE 9 – VSWR versus FREQUENCY
MWA230

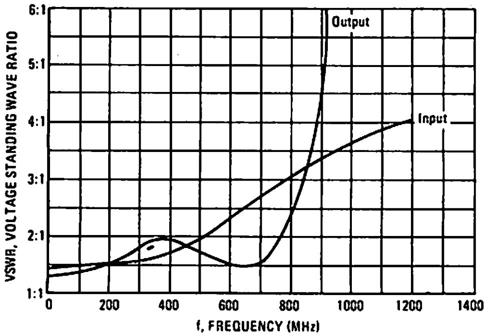

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FIGURE 10 — INPUT AND OUTPUT IMPEDANCE versus FREQUENCY MWA210

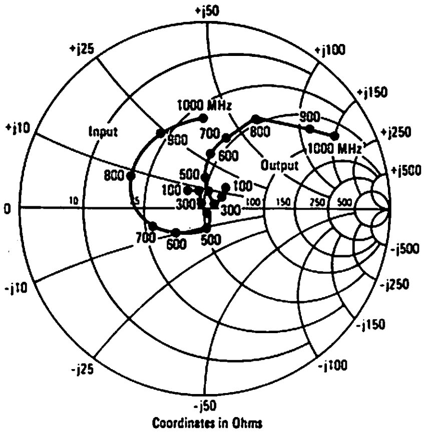


FIGURE 11 — INPUT AND OUTPUT IMPEDANCE versus FREQUENCY MWA220

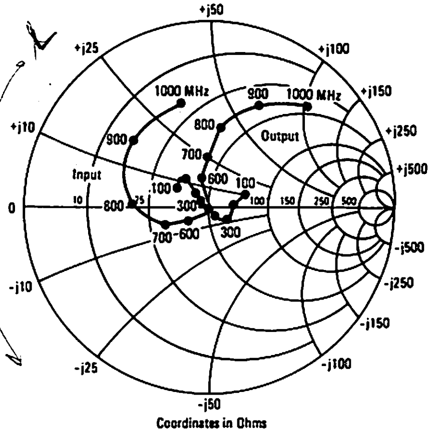


FIGURE 12 — INPUT AND OUTPUT IMPEDANCE versus FREQUENCY MWA230

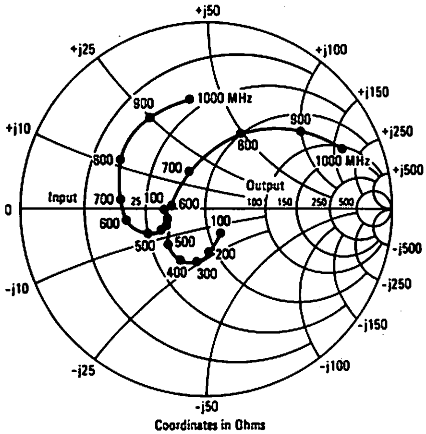


FIGURE 13 — 1.0 dB GAIN COMPRESSION versus FREQUENCY

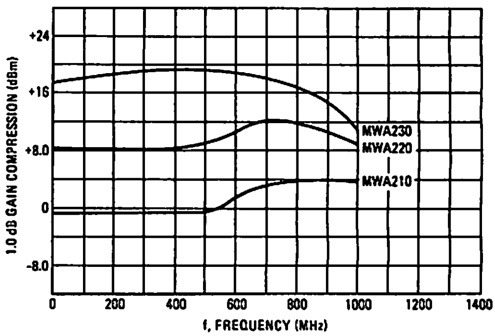


FIGURE 14 — 1.0 dB GAIN COMPRESSION versus DEVICE CURRENT f = 600 MHz

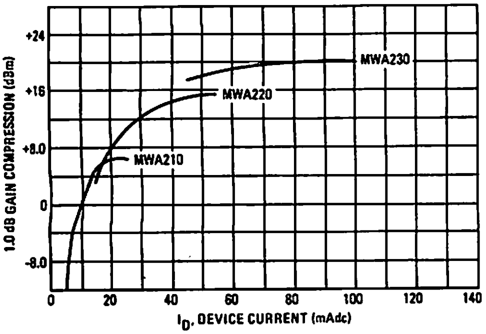


FIGURE 15 — 1.0 dB GAIN COMPRESSION versus CASE TEMPERATURE f = 600 MHz

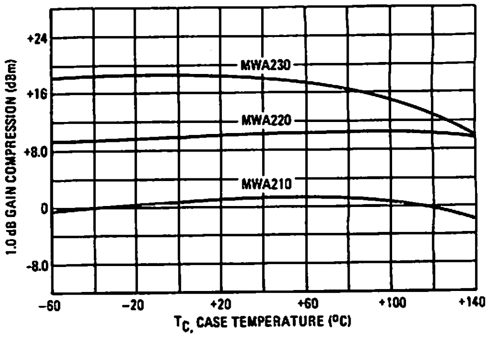


FIGURE 16 — NOISE FIGURE versus FREQUENCY

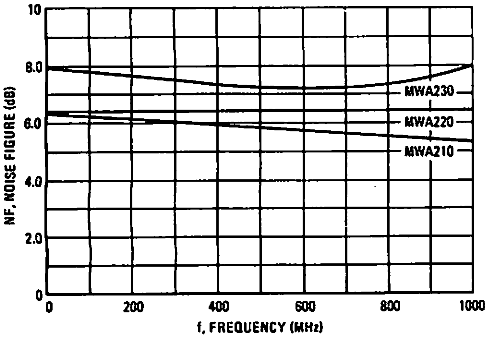


FIGURE 17 — REVERSE ISOLATION versus FREQUENCY

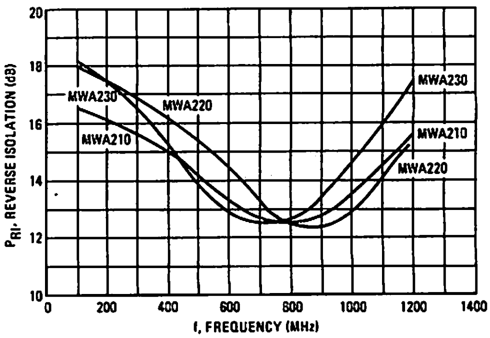


FIGURE 18 — SECOND HARMONIC OUTPUT versus FREQUENCY

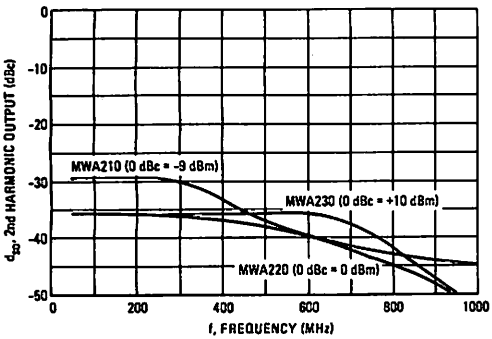


FIGURE 19 — SECOND AND THIRD ORDER INTERCEPT MWA210

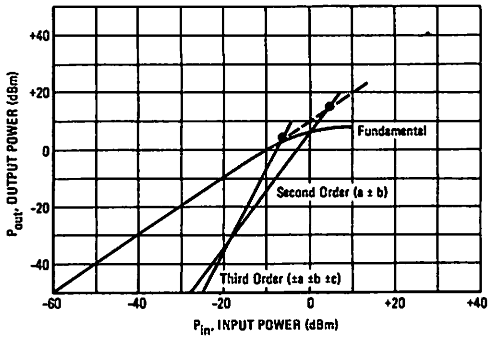


FIGURE 20 – SECOND AND THIRD ORDER INTERCEPT MWA220

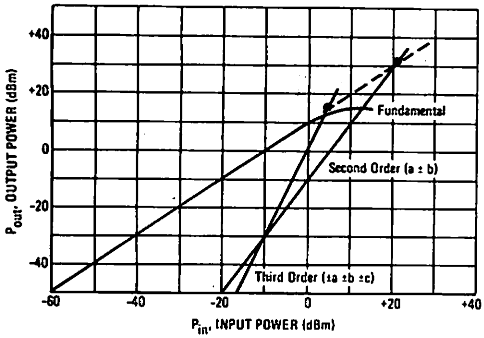


FIGURE 21 – SECOND AND THIRD ORDER INTERCEPT MWA230

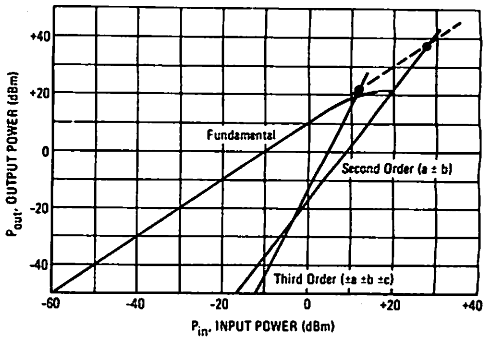


FIGURE 22 – INTERMODULATION DISTORTION versus POWER OUTPUT MWA210

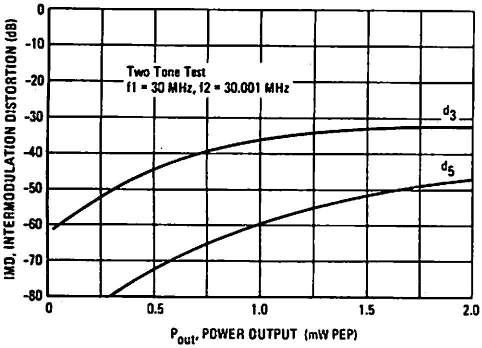


FIGURE 23 – INTERMODULATION DISTORTION versus POWER OUTPUT MWA220

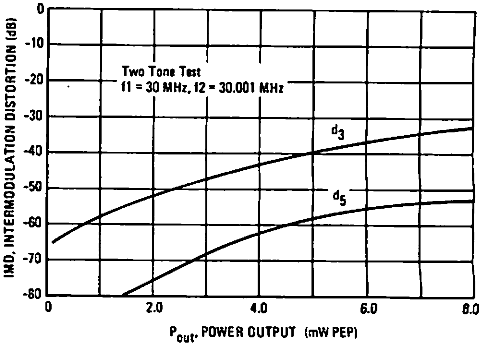


FIGURE 24 – INTERMODULATION DISTORTION versus POWER OUTPUT MWA230

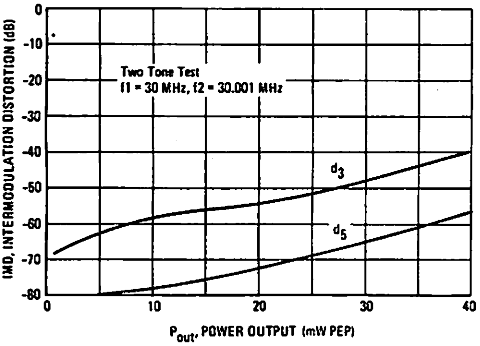
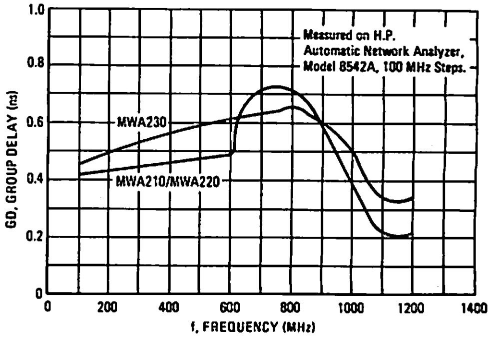


FIGURE 25 – GROUP DELAY versus FREQUENCY



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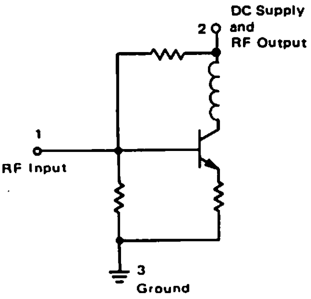


Amplifier Application

The circuit schematic for a simple amplifier design is shown in Figure 27. External to the MWA hybrid amplifier the only components required are:

Decoupling elements — Bypass Capacitor
Decoupling Impedance
(resistor/inductor)
DC Blocking Capacitors at the RF input and output.

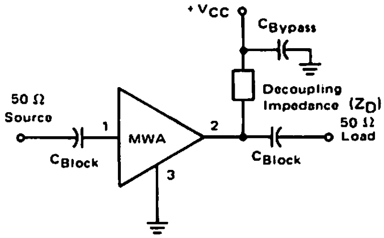
External Decoupling Impedance

In all cases the external bias (decoupling elements) must present an impedance which is large compared to the 50 Ω load impedance to minimize RF gain reduction. The loss in gain due to the decoupling impedance is given by the equation:

$$\text{Loss} = 20 \text{ Log } \frac{Z_D}{Z_D + 25} \text{ dB}$$

where Z_D = decoupling impedance in ohms. For example, if Z_D = 1 kΩ, Loss = 0.214 dB.

FIGURE 27 — AMPLIFIER SCHEMATIC DIAGRAM



Supply Voltage

The value of the external decoupling resistive impedance (R_D) determines the supply voltage ($+V_{CC}$) and is determined by the following equation:

$$V_{CC} = R_D \times I_D + V_D$$

where I_D and V_D are the device current and voltage stated in the data sheet. For example, for MWA110,

$$I_D = 10 \text{ mA}$$
$$V_D = 2.9 \text{ V}$$

and, if R_D = 330 Ω, then

$$V_{CC} = 6.2 \text{ V}$$

More commonly V_{CC} is predetermined and R_D may be calculated from:

$$R_D = \frac{V_{CC} - V_D}{I_D}$$

An RF choke is not recommended for use as a decoupling impedance without also using a resistor having an appropriate value.

Low Frequency Response

The value of the blocking capacitors determines the low frequency response of the amplifier. The following expression is used to determine the blocking capacitor value to yield a desired 3 dB low frequency corner (f_{LFC}).

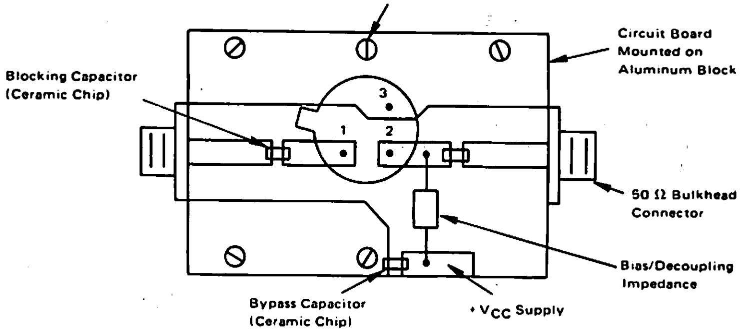
$$C_{Block}(\text{Farads}) = \frac{1}{100 \pi f_{LFC}(\text{Hz})}$$

Bypass Capacitor

The reactive impedance of the bypass capacitor should be small compared to the impedance of the decoupling element at the lowest frequency of operation.

5

FIGURE 28 — TEST FIXTURE



Note: The circuitry indicated is on the underside of the printed circuit board with sockets for the amplifier pins. The case of the amplifier should contact the printed circuit board top surface to ensure effective RF grounding.

Text Fixture

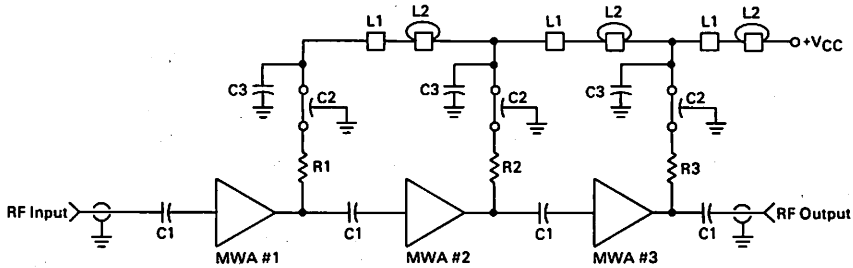
The 50 Ω input/output impedance levels of the MWA hybrids are most easily preserved on a circuit board by using 50 Ω microstrip transmission lines. Figure 28 is an example of a circuit board layout which utilizes microstrip transmission lines in conjunction with other sound RF construction techniques.

The characteristic impedance and corresponding line width of the microstrip are a function of the circuit board dielectric constant and thickness. The table lists appropriate line widths for 50 Ω microstrip lines on commonly used circuit board materials.

MATERIAL TYPE	DIELECTRIC CONSTANT	DIELECTRIC THICKNESS INCHES	LINE WIDTH INCHES
Teflon-Fiberglass	2.5	0.03125 0.0625	0.090 0.180

As in all good RF circuit designs, care should be taken to minimize parasitic lead inductances and to provide adequate grounding.

FIGURE 29 — TYPICAL CASCADE



The dc isolation components shown are critical in maintaining good stability in multi-stage designs. Keep Pin #3 (Ground) as short as possible preferably soldering the case to the ground plane for best gain flatness to 1000 MHz.

C1 — For operation to 400 MHz, 1000 pF, 50 mil Chip Capacitor - ATC 50 mil Case (5.0 MHz L.F.)
C1 — For operation to 1000 MHz, 0.018 mF, Chip Capacitor for 0.25 MHz L.F. Cut-Off
C2 — Feedthru Capacitor Centralab SFT-102, 1000 pF or Metuchen 54-794002-681M, 680 pF
C3 — 0.1 μF Sprague 3CZ5U104X0050C5 - 50 Volt
L1 — Ferroxcube Shielding Bead 56-590-65/4A - Single Wire
L2 — Ferroxcube Shielding Bead 56-590-65/4A - 2 Turns #26 AWG

Cascading

The inherent stability of the MWA hybrid modules makes possible the cascading of two or more units with no oscillatory problems. Figure 29 shows a typical 3 hybrid cascade with measured data for 400 MHz and 1000 MHz hybrids.

	Cascade 1	Cascade 2
Frequency Range	0.25 to 400 MHz	5.0 to 1000 MHz
Gain	43.5 dB	20.5 dB
Gain Flatness	±1.0 dB	±0.75 dB
Input VSWR	2.0:1	2.4:1
Output VSWR	1.2:1	2.1:1
V_{CC} Supply	12 Vdc	33 Vdc
I Supply	44 mAdc	150 mAdc
MWA #1	MWA110	MWA320
MWA #2	MWA110	MWA330
MWA #3	MWA120	MWA330
R1	1000 Ω	1000 Ω
R2	1000 Ω	500 Ω
R3	300 Ω	500 Ω

MWA310
MWA320
MWA330

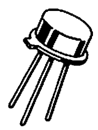
The RF Line

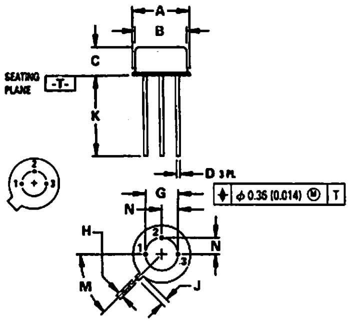
WIDEBAND HYBRID AMPLIFIERS

... single stage amplifiers designed for broadband linear applications up to 1000 MHz.

- Low-Cost TO-39 Type Package
- Gain – 8.0 dB Typ MWA310/320
  – 6.2 dB Typ MWA330
- 50 Ω Input and Output Impedance
- Fully Cascadable for Any Gain
- Thin Film Construction
- Hermetic Package
- Guaranteed Performance from -25°C to +80°C

DC-1000 MHz WIDEBAND GENERAL-PURPOSE HYBRID AMPLIFIERS





STYLE 2:
PIN 1. INPUT
2. OUTPUT
3. GROUND

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.50	0.305	0.335
C	3.81	4.57	0.165	0.185
D	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	—	0.500	—
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	

CASE 31A-03

MAXIMUM RATINGS

Rating	Symbol	Value MWA310	Value MWA320	Value MWA330	Unit
RF Input Power	P_{in}	← 100 →			mW
DC Supply Current	I_D	25	55	100	mA
Maximum Case Temperature	T_C	← 125 →			°C
Storage Temperature Range	T_{stg}	← −65 to +200 →			°C

OPERATING CONDITIONS

Device Voltage	V_D	1.6	2.9	4.0	Vdc
Device Current	I_D	10	25	60	mAdc
Decoupling Impedance	Z_D	620	620	240	Ω

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	110	°C/W

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ELECTRICAL CHARACTERISTICS (T_C = -25 to +80°C, 50 Ω system and specified operating conditions)

Characteristic		Symbol	Min	Typ	Max	Unit
Frequency Range		BW	0.1	–	1000	MHz
Power Gain	MWA310/320	G_p	7.0	8.0	–	dB
	MWA330		–	6.2	–	
Response Flatness		F	–	0	±1.0	dB
Input VSWR		–	–	–	3:1	–
Output VSWR		–	–	–	3:1	–
Output @ 1 dB Gain Compression						dBm
	MWA310		–	+3.5	–	
	MWA320		–	+11.5	–	
	MWA330		–	+15.2	–	
Noise Figure		NF				dB
	MWA310		–	6.5	–	
	MWA320		–	6.7	–	
	MWA330		–	9.0	–	
Reverse Isolation		P_{RI}				dB
	MWA310		–	10.4	–	
	MWA320		–	10.4	–	
	MWA330		–	9.0	–	
Harmonic Output		d_{so}				dB
	MWA310 (P_{out} = -9 dBm)		–	-30	–	
	MWA320 (P_{out} = 0 dBm)		–	-38	–	
	MWA330 (P_{out} = +10 dBm)		–	-35	–	

FIGURE 1 – DEVICE VOLTAGE versus DEVICE CURRENT

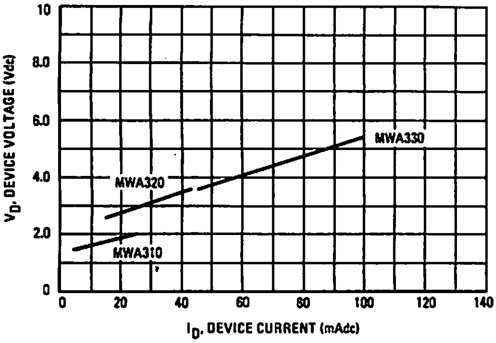

FIGURE 2 – DEVICE CURRENT versus CASE TEMPERATURE

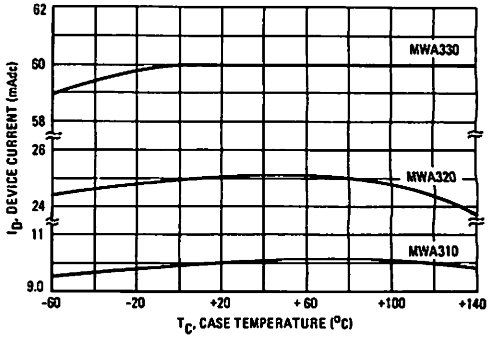

FIGURE 3 – POWER GAIN versus FREQUENCY

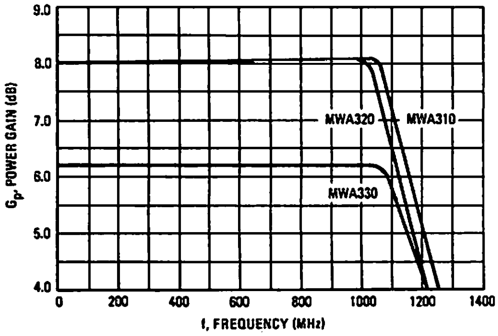

FIGURE 4 – POWER GAIN versus DEVICE CURRENT
f = 1000 MHz

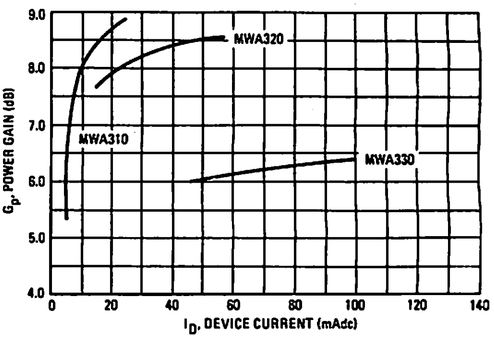

FIGURE 5 — POWER GAIN versus CASE TEMPERATURE
f = 100 MHz

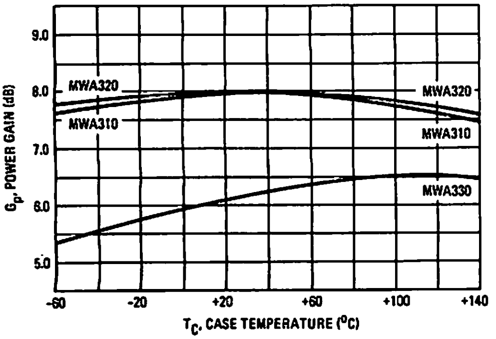

FIGURE 6 — POWER GAIN versus CASE TEMPERATURE
f = 1000 MHz

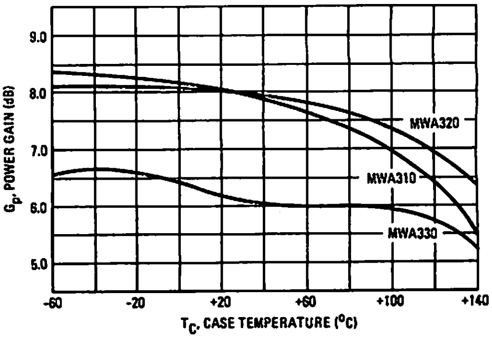

FIGURE 7 — VSWR versus FREQUENCY
MWA310

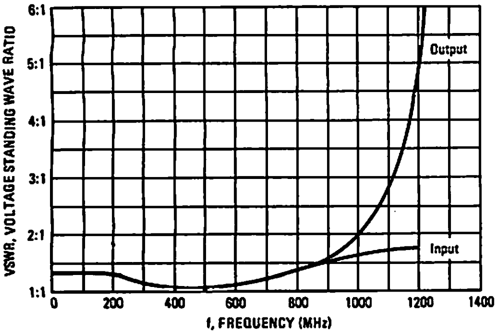

FIGURE 8 — VSWR versus FREQUENCY
MWA320

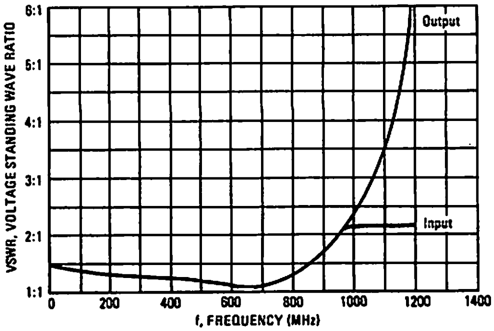

FIGURE 9 — VSWR versus FREQUENCY
MWA330

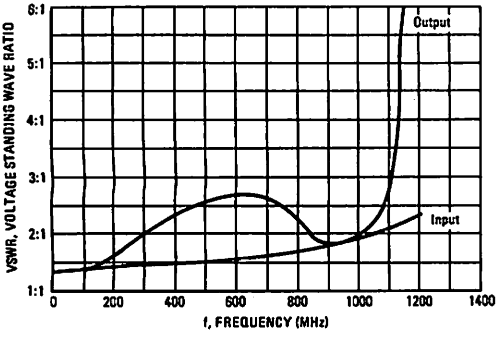

FIGURE 10 — INPUT IMPEDANCE versus FREQUENCY
MWA310

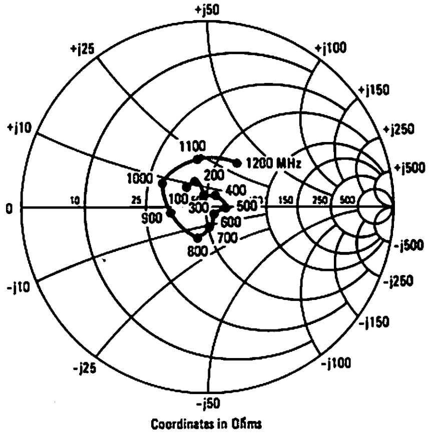

FIGURE 11 — OUTPUT IMPEDANCE versus FREQUENCY MWA310

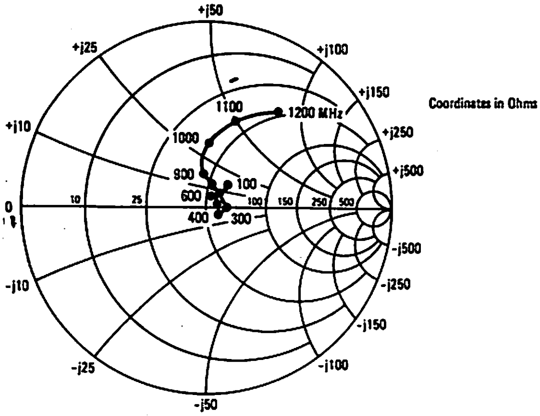

FIGURE 12 — INPUT IMPEDANCE versus FREQUENCY MWA320

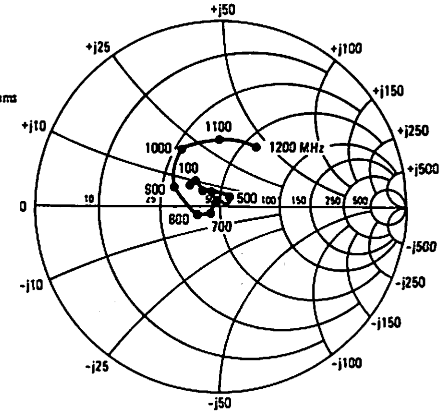

FIGURE 13 — OUTPUT IMPEDANCE versus FREQUENCY MWA320

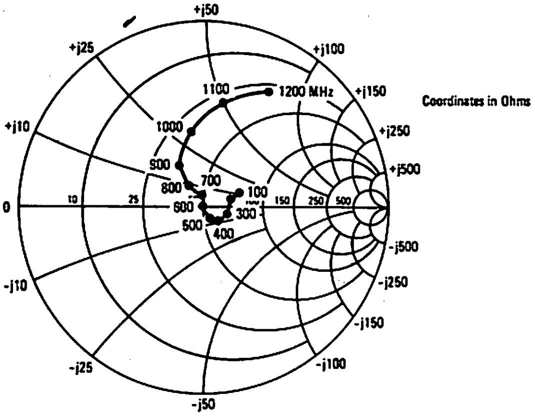

FIGURE 14 — INPUT IMPEDANCE versus FREQUENCY MWA330

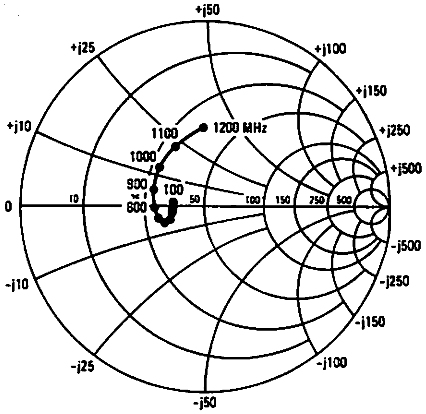

FIGURE 15 — OUTPUT IMPEDANCE versus FREQUENCY MWA330

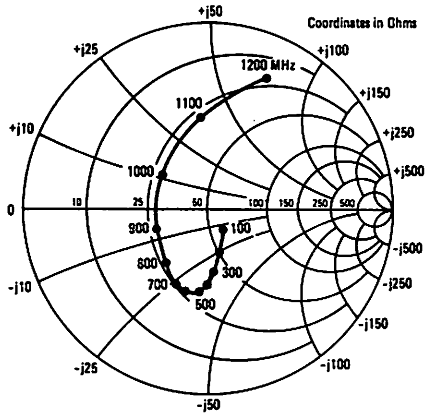

FIGURE 16 — 1.0 dB GAIN COMPRESSION versus FREQUENCY

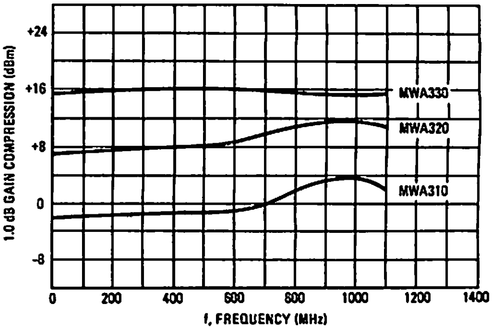

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FIGURE 17 – 1.0 dB GAIN COMPRESSION
versus DEVICE CURRENT
f = 1000 MHz

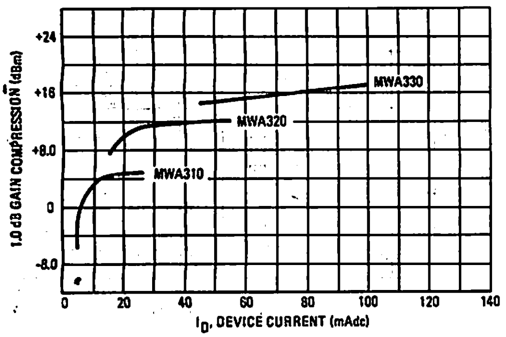

FIGURE 18 – 1.0 dB GAIN COMPRESSION
versus CASE TEMPERATURE
f = 1000 MHz

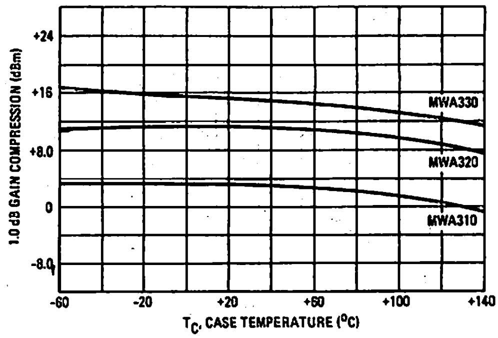

FIGURE 19 – NOISE FIGURE versus FREQUENCY

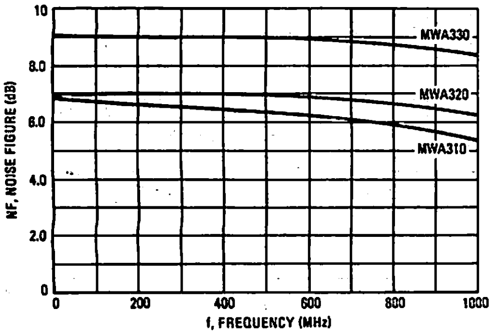

FIGURE 20 – REVERSE ISOLATION versus FREQUENCY

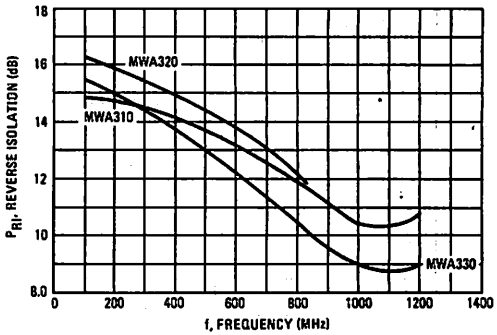

FIGURE 21 – SECOND HARMONIC OUTPUT versus FREQUENCY

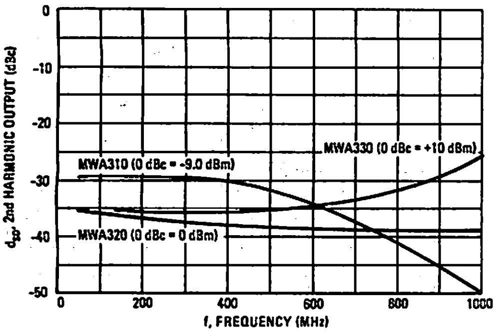

FIGURE 22 – SECOND AND THIRD ORDER INTERCEPT
MWA310

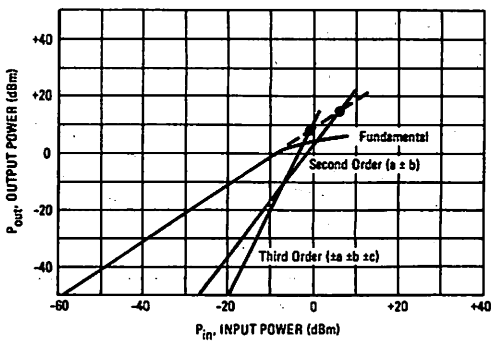

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FIGURE 23 — SECOND AND THIRD ORDER INTERCEPT
MWA320

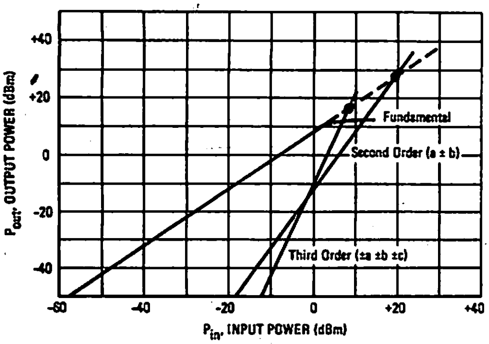


FIGURE 24 — SECOND AND THIRD ORDER INTERCEPT
MWA330

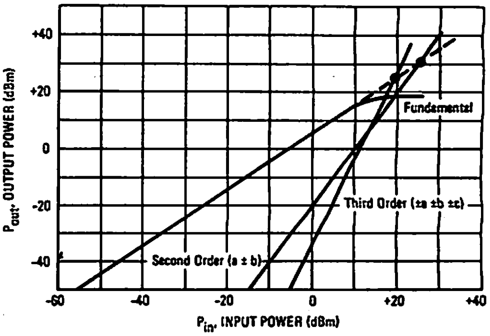


FIGURE 25 — INTERMODULATION DISTORTION versus POWER OUTPUT
MWA310

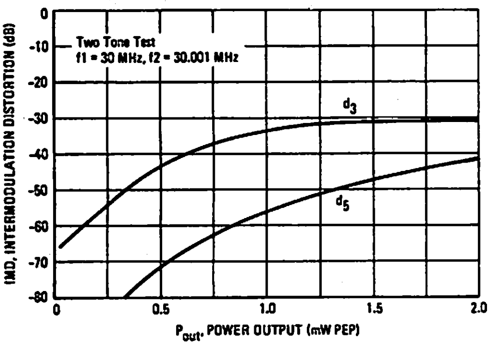


FIGURE 26 — INTERMODULATION DISTORTION versus POWER OUTPUT
MWA320

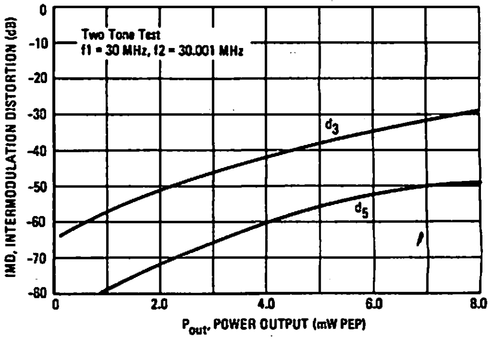


FIGURE 27 — INTERMODULATION DISTORTION versus POWER OUTPUT
MWA330

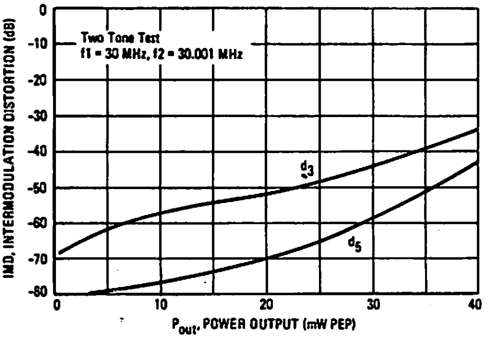
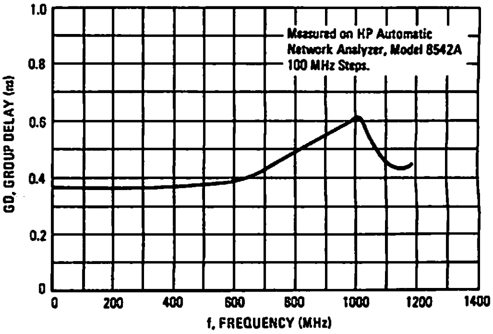


FIGURE 28 — GROUP DELAY versus FREQUENCY
MWA310/MWA320/MWA330



5

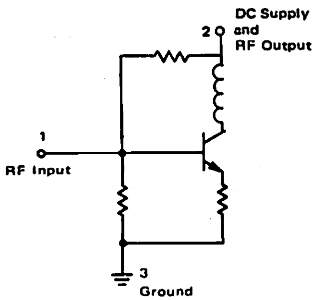
MWA SERIES HYBRID AMPLIFIER APPLICATIONS INFORMATION

The MWA series hybrid amplifiers are designed for wideband general purpose applications in 50 Ω systems. Fully cascadable for any gain combination, operable at voltages as low as 3 Vdc, and external control of the low frequency corner make the MWA amplifiers extremely versatile gain blocks.

Basic Circuit Configuration

Figure 29 shows the basic internal circuit. It is important to note that the specified operating conditions of voltage, current, and external decoupling impedance must be applied to the units in order to achieve the published electrical characteristics.

FIGURE 29 — INTERNAL CIRCUIT



Amplifier Application

The circuit schematic for a simple amplifier design is shown in Figure 30. External to the MWA hybrid amplifier the only components required are:

Decoupling elements — Bypass Capacitor
Decoupling Impedance
(resistor/inductor)

DC Blocking Capacitors at the RF input and output.

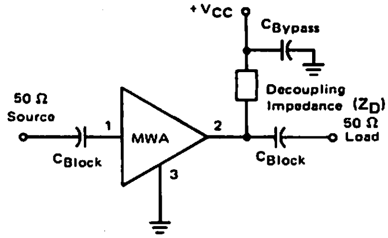
External Decoupling Impedance

In all cases the external bias (decoupling elements) must present an impedance which is large compared to the 50 Ω load impedance to minimize RF gain reduction. The loss in gain due to the decoupling impedance is given by the equation:

$$\text{Loss} = 20 \text{ Log } \frac{Z_D}{Z_D + 25} \text{ dB}$$

where Z_D = decoupling impedance in ohms. For example, if Z_D = 1 kΩ, Loss = 0.214 dB.

FIGURE 30 — AMPLIFIER SCHEMATIC DIAGRAM



Supply Voltage

The value of the external decoupling resistive impedance (R_D) determines the supply voltage ($+V_{CC}$) and is determined by the following equation:

$$V_{CC} = R_D \times I_D + V_D$$

where I_D and V_D are the device current and voltage stated in the data sheet. For example, for MWA110,

$$I_D = 10 \text{ mA}$$
$$V_D = 2.9 \text{ V}$$

and, if R_D = 330 Ω, then

$$V_{CC} = 6.2 \text{ V}$$

More commonly V_{CC} is predetermined and R_D may be calculated from:

$$R_D = \frac{V_{CC} - V_D}{I_D}$$

An RF choke is not recommended for use as a decoupling impedance without also using a resistor having an appropriate value.

Low Frequency Response

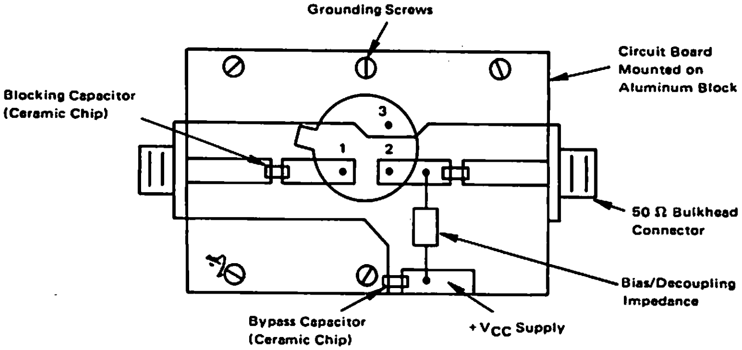
The value of the blocking capacitors determines the low frequency response of the amplifier. The following expression is used to determine the blocking capacitor value to yield a desired 3 dB low frequency corner (f_{LFC}).

$$C_{Block}(\text{Farads}) = \frac{1}{100 \pi f_{LFC}(\text{Hz})}$$

Bypass Capacitor

The reactive impedance of the bypass capacitor should be small compared to the impedance of the decoupling element at the lowest frequency of operation.

FIGURE 31 – TEST FIXTURE



Note: The circuitry indicated is on the underside of the printed circuit board with sockets for the amplifier pins. The case of the amplifier should contact the printed circuit board top surface to ensure effective RF grounding.

Text Fixture

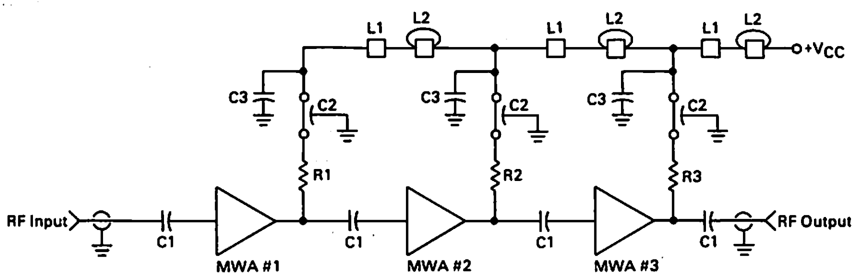
The 50 Ω input/output impedance levels of the MWA hybrids are most easily preserved on a circuit board by using 50 Ω microstrip transmission lines. Figure 31 is an example of a circuit board layout which utilizes microstrip transmission lines in conjunction with other sound RF construction techniques.

The characteristic impedance and corresponding line width of the microstrip are a function of the circuit board dielectric constant and thickness. The table lists appropriate line widths for 50 Ω microstrip lines on commonly used circuit board materials.

MATERIAL TYPE	DIELECTRIC CONSTANT	DIELECTRIC THICKNESS INCHES	LINE WIDTH INCHES
Teflon-Fiberglass	2.5	0.03125 0.0625	0.090 0.180

As in all good RF circuit designs, care should be taken to minimize parasitic lead inductances and to provide adequate grounding.

FIGURE 32 — TYPICAL CASCADE



The dc isolation components shown are critical in maintaining good stability in multi-stage designs. Keep Pin #3 (Ground) as short as possible preferably soldering the case to the ground plane for best gain flatness to 1000 MHz.

C1 — For operation to 400 MHz, 1000 pF, 50 mil Chip Capacitor - ATC 50 mil Case (5.0 MHz L.F.)
C1 — For operation to 1000 MHz, 0.018 mF, Chip Capacitor for 0.25 MHz L.F. Cut-Off
C2 — Feedthru Capacitor Centralab SFT-102, 1000 pF or Metuchen 54-794002-681M, 680 pF
C3 — 0.1 μF Sprague 3CZ5U104X0050C5 - 50 Volt
L1 — Ferroxcube Shielding Bead 56-590-65/4A - Single Wire
L2 — Ferroxcube Shielding Bead 56-590-65/4A - 2 Turns #26 AWG

	Cascade 1	Cascade 2
Frequency Range	0.25 to 400 MHz	5.0 to 1000 MHz
Gain	43.5 dB	20.5 dB
Gain Flatness	± 1.0 dB	± 0.75 dB
Input VSWR	2.0:1	2.4:1
Output VSWR	1.2:1	2.1:1
V_{CC} Supply	12 Vdc	33 Vdc
I Supply	44 mAdc	150 mAdc
MWA #1	MWA110	MWA320
MWA #2	MWA110	MWA330
MWA #3	MWA120	MWA330
R1	1000 Ω	1000 Ω
R2	1000 Ω	500 Ω
R3	300 Ω	500 Ω

Cascading

The inherent stability of the MWA hybrid modules makes possible the cascading of two or more units with no oscillatory problems. Figure 32 shows a typical 3 hybrid cascade with measured data for 400 MHz and 1000 MHz hybrids.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MX20-1
MX20-2

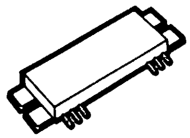
The RF Line

UHF Power Amplifiers

. . . designed for wide power range control as encountered in UHF cellular radio applications.

- MX20-1 400–440 MHz
  MX20-2 440–470 MHz
- Specified 12.5 V, UHF Characteristics —
  Output Power — 20 W
  Minimum Gain — 21 dB
  Harmonics — −40 dBc Max
- 50 Ohm Input/Output Impedances
- Guaranteed Stability and Ruggedness

20 WATTS
400–470 MHz
RF POWER AMPLIFIERS



CASE 830-01, STYLE 1
(MVM)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{CC1}, V_{CC2}	15.6	Vdc
Operating Case Temperature Range	T_C	−30 to +100	°C
Storage Temperature Range	T_{stg}	−40 to +100	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Unit
Thermal Resistance, Junction to Flange	$R_{\theta JF}$	4	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC1} and V_{CC2} set at 12.5 Vdc, T_A = 25°C, 50 Ω system unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range MX20-1 MX20-2	—	400 440	— —	440 470	MHz
Input Power (P_o = 20 W)	P_{in}	—	—	150	mW
Power Gain (P_o = 20 W)	G_P	21	—	—	dB
Efficiency (P_o = 20 W)	η	35	40	—	%
Harmonics (P_o = 20 W, Reference)	—	—	—	−40	dBc
Input Return Loss	Γ_{IN}	10	—	—	dB
Power Derating (P_o = 20 W, T_C = 25°C Ref.) −30°C to +70°C	—	—	—	1	dB
Load Mismatch (V_{CC} = 15.6 V, $P_o \leq$ 30 W, $P_{in} \leq$ 200 mW, Load VSWR 20:1, All Phase Angles)	ψ	No change in P_{out} Before and After Test			
Stability (P_{in} — 0 to 200 mW; Load Mismatch 4:1; V_{CC2} = 0 to 15.6 Vdc; V_{CC1} adjusted to keep $P_o \leq$ 20 W)	—	All spurious outputs more than 70 dB below desired signal			
Gain Control Range	—	30	—	—	dB

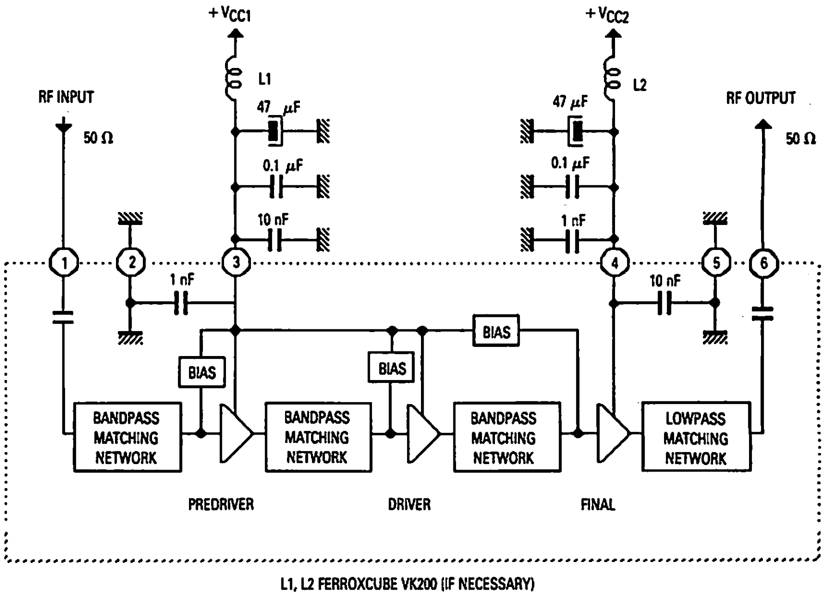


Figure 1. UHF Module Test Setup

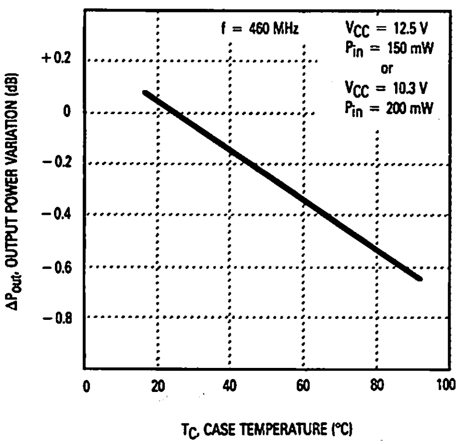


Figure 2. Output Power Variation versus Temperature

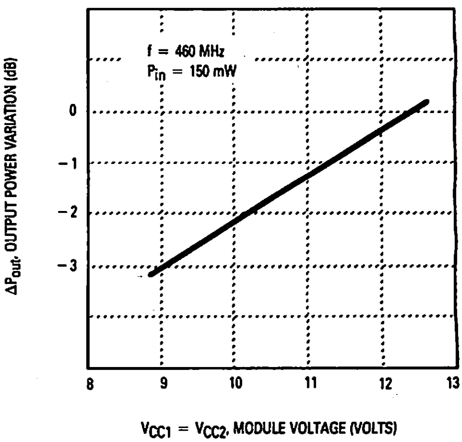


Figure 3. Output Power Variation versus Voltage

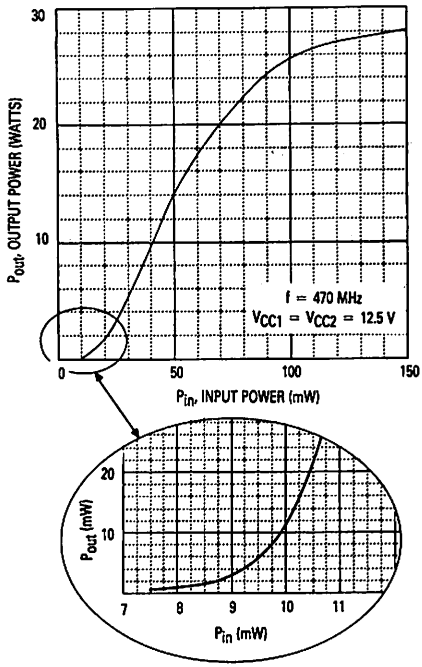


Figure 4. Output Power versus Input Power

5

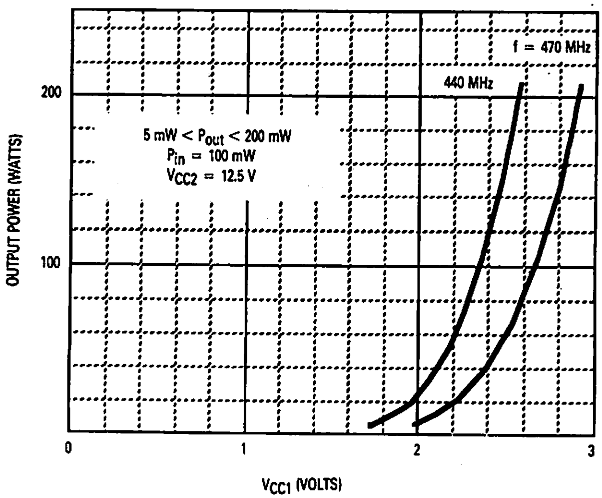


Figure 5. Output Power versus Control Voltage

PAA0105-29-6L

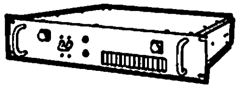
The RF Line

Integrated VHF-UHF Linear Power Amplifier

... designed for wideband linear applications in the 100 to 500 MHz frequency range. Motorola class A high-power transistors provide excellent ITOs, high gain, and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 100 to 500 MHz
- Output Power — 6.0 Watts Minimum
- Gain — 31 dB
- Linearity — +48.5 dBm Typ ITO
- Noise Figure — 6.0 dB Typ @ f = 500 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling

**6.0 WATT
100–500 MHz
LINEAR POWER
AMPLIFIER ASSEMBLY**



CASE 389F-01

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ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SSG	Small Signal Gain	f = 100–500 MHz	29	31		dB
f_r	Frequency Response	f = 100–500 MHz, P_o = 6.0 W		±1.5	±2.0	dB
P_o	Power Output	f = 100–500 MHz	6.0	8.0		W
NF	Noise Figure	f = 100–500 MHz		6.0	7.0	dB
ITO	Third Order Intercept Point	f = 100–500 MHz	+47.5	+48.5		dBm
DSO	Second Harmonic Attenuation	f = 200–1000 MHz	−15	−20		dB
P_{sat}	Saturated Power	f = 100–500 MHz	8.0	10		W
VSWR	Input (Ref = 50 Ω) Output (Ref = 50 Ω)	f = 100–500 MHz f = 100–500 MHz		3.0:1 2.0:1	3.5:1 3.0:1	
VSWR Load	VSWR Survival	P_o = 6.0 W CW f = 100–500 MHz			∞:1	
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz		85	100	W

PAA0105-45-25L

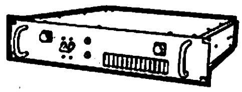
The RF Line

Integrated VHF-UHF Linear Power Amplifier

**25 WATT
100–500 MHz
LINEAR POWER
AMPLIFIER ASSEMBLY**

. . . designed for wideband linear applications in the 100 to 500 MHz frequency range. Motorola class A high-power transistors provide excellent ITOs, high gain, and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 100 to 500 MHz
- Output Power — 25 Watts Minimum
- Gain — 47 dB
- Linearity — +53 dBm Typ ITO
- Noise Figure — 5.0 dB Typ @ f = 500 MHz
- 50 Ohm Input/Output Impedance
- *Heavy Duty* Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling



CASE 389F-01

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SSG	Small Signal Gain	f = 100–500 MHz	45	47		dB
f_r	Frequency Response	f = 100–500 MHz		±2.0	±2.5	dB
P_o	Power Output	f = 100–500 MHz	25	30		W
NF	Noise Figure	f = 100–500 MHz		5.0	6.5	dB
ITO	Third Order Intercept Point	f = 100–500 MHz	+52	+53		dBm
dso	Second Harmonic Attenuation	f = 0.2–1.0 GHz	20	33		dB
VSWR	Input (Ref = 50 Ω) Output (Ref = 50 Ω)	f = 100–500 MHz f = 100–500 MHz		1.5:1 3.0:1	2.0:1	
VSWR Load	VSWR Survival	P_o = 25 W CW f = 100–500 MHz			∞:1	
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz		270	325	W

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PAA0105-50-50LAS

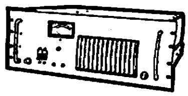
The RF Line

Integrated VHF-UHF Linear Power Amplifier

**50 WATT
100–500 MHz
LINEAR POWER
AMPLIFIER**

... designed for wideband linear applications in the 100 to 500 MHz frequency range. Motorola class A high-power transistors provide excellent ITOs, high gain, and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 100 to 500 MHz
- Output Power — 50 Watts Minimum
- Gain — 52 dB
- Linearity — +56.5 dBm Typ ITO
- Noise Figure — 7.5 dB Typ @ f = 500 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling
- Built-In System DC Voltmeter



CASE 389G-01

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SSG	Small Signal Gain	f = 100–500 MHz	50	52		dB
f_r	Frequency Response	f = 100–500 MHz		±2.0	±2.5	dB
P_o	Power Output	f = 100–500 MHz	50	60		W
NF	Noise Figure	f = 100–500 MHz		7.5	8.5	dB
ITO	Third Order Intercept Point	f = 100–500 MHz	+55	+56.5		dBm
DSO	Second Harmonic Attenuation	f = 0.2–1.0 GHz	35	45		dB
VSWR	Input (Ref = 50 Ω) Output (Ref = 50 Ω)	f = 100–500 MHz f = 100–500 MHz		1.25:1 1.35:1	1.5:1 1.75:1	
VSWR Load	VSWR Survival	P_o = 50 W CW f = 100–500 MHz			∞:1	
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz		700	750	W

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PAA0200-34-1.5L

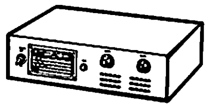
The RF Line

Integrated Power Amplifier

... designed for wideband linear applications in the 1.0 to 200 MHz frequency range. Contains an all hybrid amplifier module — Motorola's own proven reliable circuitry, used in millions of operating units over twenty years — utilizing Motorola's class A transistors. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 1.0 to 200 MHz
- Output Power — 1.5 Watts Minimum
- Gain — 36 dB Typ
- Linearity — +51 dBm Typ ITO
- Noise Figure — 4.5 dB Typ @ f = 100 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Forced Air Cooling
- Thermally Protected
- 220 Vac Model Available, P/N PAE0200-34-1.5L

**2.0 WATTS
1.0–200 MHz
LINEAR POWER
AMPLIFIER**



CASE 389R-01, STYLE 1

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
P_g	Power Gain	f = 100 MHz	34	36	37	dB
f_r	Frequency Response	f = 1.0–200 MHz	—	±0.5	±1.25	dB
P_{o1dB}	Power Output, 1.0 dB Compression	f = 100 MHz f = 200 MHz	1.5 1.3	2.0 1.5	— —	W
NF	Noise Figure	f = 100 MHz f = 200 MHz	— —	4.5 5.5	6.0 7.0	dB
ITO	Third Order Intercept Point	f = 100 MHz f = 200 MHz	+49 +44	+51 +55	— —	dBm
VSWR	Input (Ref. = 50 Ω) Output (Ref. = 50 Ω)	f = 1.0–200 MHz f = 1.0–200 MHz	— —	1.5:1 1.5:1	2.0:1 2.0:1	—
VSWR Load	VSWR Survival	P_o = 1.5 W f = 1.0–200 MHz	—	—	30:1	—
P_{in}	AC Input	V_{in} = 115 Vac, 1.0φ, 60 Hz	—	27	37	W

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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

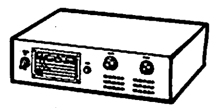
PAA0200-34-3.1L

The RF Line
Integrated Power Amplifier

4.0 WATTS
1.0–200 MHz
LINEAR POWER AMPLIFIER

... designed for wideband linear applications in the 1.0 to 200 MHz frequency range. Contains an all hybrid amplifier module — Motorola's own proven reliable circuitry, used in millions of operating units over twenty years — utilizing Motorola's class A transistors. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 1.0 to 200 MHz
- Output Power — 3.1 Watts Minimum
- Gain — 35 dB Typ
- Linearity — +53 dBm Typ ITO
- Noise Figure — 5.0 dB Typ @ f = 100 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Forced Air Cooling
- Thermally Protected
- 220 Vac Model Available, P/N PAE0200-34-3.1L



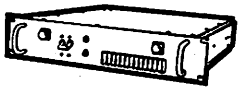
CASE 389R-01, STYLE 1

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
P_g	Power Gain	f = 100 MHz	33.5	35	36.5	dB
f_r	Frequency Response	f = 1.0–200 MHz	—	±1.0	±1.5	dB
P_{o1dB}	Power Output, 1.0 dB Compression	f = 100 MHz f = 200 MHz	3.1 2.5	4.0 3.1	— —	W
NF	Noise Figure	f = 100 MHz f = 200 MHz	— —	5.0 6.0	6.5 7.5	dB
ITO	Third Order Intercept Point	f = 100 MHz f = 200 MHz	+51 +46	+53 +48	— —	dBm
VSWR	Input (Ref. = 50 Ω) Output (Ref. = 50 Ω)	f = 1.0–200 MHz f = 1.0–200 MHz	— —	1.5:1 1.5:1	2.0:1 2.0:1	—
VSWR Load	VSWR Survival	P_o = 3.0 W f = 1.0–200 MHz	—	—	30:1	—
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz	—	50	60	W

PAA225-42-10L

**10 WATT
172–225 MHz
LINEAR POWER
AMPLIFIER ASSEMBLY**



CASE 389F-01

The RF Line

Integrated VHF Linear Power Amplifier

. . . designed for television service applications in the 172 to 225 MHz frequency range. Motorola class A high-power transistors provide low noise, high gain, and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 172 to 225 MHz
- Output Power — 10 Watts, Peak Sync.
- Gain — 45 dB
- Linearity — −58 dB, 3 Tone IMD
- Noise Figure — 5.0 dB Typ @ f = 225 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
RF Power Input	P_{in}	+5.0	dBm
Operating Base Plate Temperature Range	T_C	−40 to +90	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS

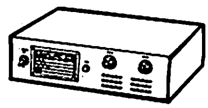
Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SSG	Small Signal Gain	f = 172–225 MHz	42	46	51	dB
f_r	Frequency Response	f = 172–225 MHz		±0.5	±1.0	dB
$P_{o(1)}$	IMD 3 Tone = −58 dB Vision Carrier = −8.0 dB Reference Sound Carrier = −10 dB Reference Sideband Carrier = −16 dB Reference	f = 172–225 MHz	10			W
$P_{o(2)}$	IMD 3 Tone = −55 dB Vision Carrier = −8.0 dB Reference Sound Carrier = −7.0 dB Reference Sideband Carrier = −16 dB Reference	f = 172–225 MHz	10			W
NF	Noise Figure	f = 172–225 MHz		5.0		dB
VSWR	Input (50 Ω) Output (50 Ω)	f = 172–225 MHz f = 172–225 MHz		1.5:1 2.0:1	2.0:1 2.5:1	N/A N/A
VSWR Load	VSWR Survival	P_o = 10 W CW f = 172 MHz			∞:1	N/A
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz		135	150	W

The RF Line

Integrated Power Amplifier

PAA0450-33-0.4L

**1.0 WATT
30–450 MHz
LINEAR POWER
AMPLIFIER**



CASE 389R-01, STYLE 1

. . . designed for wideband linear applications in the 30 to 450 MHz frequency range. Contains an all hybrid amplifier module — Motorola's own proven reliable circuitry, used in millions of operating units over twenty years — utilizing Motorola's class A transistors. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 30 to 450 MHz
- Output Power — 0.6 Watts Minimum
- Gain — 34 dB Typ
- Linearity — +45 dBm Typ ITO
- Noise Figure — 5.0 dB Typ @ f = 300 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Forced Air Cooling
- Thermally Protected
- 220 Vac Model Available, P/N PAE0450-33-0.4L

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
P_g	Power Gain	f = 50 MHz	33	34	35	dB
f_r	Frequency Response	f = 30–450 MHz	—	±0.75	±1.5	dB
P_{o1dB}	Power Output, 1.0 dB Compression	f = 300 MHz f = 450 MHz	0.6 0.25	1.0 0.4	— —	W
NF	Noise Figure	f = 300 MHz f = 450 MHz	— —	5.0 6.0	6.0 7.0	dB
ITO	Third Order Intercept Point	f = 300 MHz f = 450 MHz	+42 +36	+45 +38	— —	dBm
VSWR	Input (Ref. = 50 Ω) Output (Ref. = 50 Ω)	f = 30–450 MHz f = 30–450 MHz	— —	1.2:1 1.2:1	1.5:1 1.5:1	—
VSWR Load	VSWR Survival	P_o = 0.4 W f = 30–450 MHz	—	—	30:1	—
P_{in}	AC Input	V_{in} = 115 Vac, 1.0φ, 60 Hz	—	19	30	W

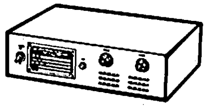
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PAA0500-17-1.0L

The RF Line

Integrated Power Amplifier

2.0 WATTS
30–500 MHz
LINEAR POWER AMPLIFIER



CASE 389R-01, STYLE 1

. . . designed for wideband linear applications in the 30 to 500 MHz frequency range. Contains an all hybrid amplifier module — Motorola's own proven reliable circuitry, used in millions of operating units over twenty years — utilizing Motorola's class A transistors. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 30 to 500 MHz
- Output Power — 1.25 Watts Minimum
- Gain — 18 dB Typ
- Linearity — +49 dBm Typ ITO
- Noise Figure — 4.5 dB Typ @ f = 300 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Forced Air Cooling
- Thermally Protected
- 220 Vac Model Available, P/N PAE0500-17-1.0L

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
P_g	Power Gain	f = 50 MHz	17	18	21	dB
f_r	Frequency Response	f = 30–500 MHz	—	±0.75	±1.5	dB
P_{o1dB}	Power Output, 1.0 dB Compression	f = 300 MHz f = 500 MHz	1.25 0.6	2.0 1.0	— —	W
NF	Noise Figure	f = 300 MHz f = 500 MHz	— —	4.5 6.0	5.5 7.0	dB
ITO	Third Order Intercept Point	f = 300 MHz f = 500 MHz	+47 +40	+49 +42	— —	dBm
VSWR	Input (Ref. = 50 Ω) Output (Ref. = 50 Ω)	f = 30–500 MHz f = 30–500 MHz	— —	1.2:1 1.2:1	1.5:1 1.5:1	—
VSWR Load	VSWR Survival	P_o = 1.0 W f = 30–500 MHz	—	—	30:1	—
P_{in}	AC Input	V_{in} = 115 Vac, 1.0φ, 60 Hz	—	23	33	W

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PAA0500-17-2.0L

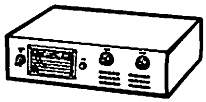
The RF Line

Integrated Power Amplifier

**3.1 WATTS
30–500 MHz
LINEAR POWER
AMPLIFIER**

. . . designed for wideband linear applications in the 30 to 500 MHz frequency range. Contains an all hybrid amplifier module — Motorola's own proven reliable circuitry, used in millions of operating units over twenty years — utilizing Motorola's class A transistors. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 30 to 500 MHz
- Output Power — 2.0 Watts Minimum
- Gain — 18 dB Typ
- Linearity — +51 dBm Typ ITO
- Noise Figure — 5.0 dB Typ @ f = 300 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Forced Air Cooling
- Thermally Protected
- 220 Vac Model Available, P/N PAE0500-17-2.0L



CASE 389R-01, STYLE 1

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
P_g	Power Gain	f = 50 MHz	17	18	19	dB
f_r	Frequency Response	f = 30–500 MHz	—	±0.75	±1.5	dB
P_{o1dB}	Power Output, 1.0 dB Compression	f = 300 MHz f = 500 MHz	2.0 1.3	3.1 2.0	— —	W
NF	Noise Figure	f = 300 MHz f = 500 MHz	— —	5.0 6.5	6.0 7.5	dB
ITO	Third Order Intercept Point	f = 300 MHz f = 500 MHz	+49 +31	+51 +33	— —	dBm
VSWR	Input (Ref. = 50 Ω) Output (Ref. = 50 Ω)	f = 30–500 MHz f = 30–500 MHz	— —	1.2:1 1.2:1	1.5:1 1.5:1	—
VSWR Load	VSWR Survival	P_o = 2.0 W f = 30–500 MHz	—	—	30:1	—
P_{in}	AC Input	V_{in} = 115 Vac, 1.0φ, 60 Hz	—	40	50	W

PAA0500-35-1.0L

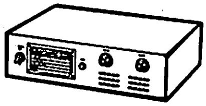
The RF Line

Integrated Power Amplifier

2.0 WATTS
30–500 MHz
LINEAR POWER
AMPLIFIER

. . . designed for wideband linear applications in the 30 to 500 MHz frequency range. Contains an all hybrid amplifier module — Motorola's own proven reliable circuitry, used in millions of operating units over twenty years — utilizing Motorola's class A transistors. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 30 to 500 MHz
- Output Power — 1.25 Watts Minimum
- Gain — 36.5 dB Typ
- Linearity — +49 dBm Typ ITO
- Noise Figure — 5.0 dB Typ @ f = 300 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Forced Air Cooling
- Thermally Protected
- 220 Vac Model Available, P/N PAE0500-35-1.0L



CASE 389R-01, STYLE 1

ELECTRICAL CHARACTERISTICS

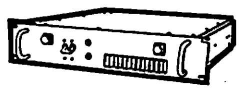
Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
P_g	Power Gain	f = 50 MHz	35	36.5	38	dB
f_r	Frequency Response	f = 30–500 MHz	—	±1.0	±2.0	dB
P_{o1dB}	Power Output, 1.0 dB Compression	f = 300 MHz f = 500 MHz	1.25 0.6	2.0 1.0	— —	W
NF	Noise Figure	f = 300 MHz f = 500 MHz	— —	5.0 6.0	6.0 7.0	dB
ITO	Third Order Intercept Point	f = 300 MHz f = 500 MHz	+46 +39	+49 +42	— —	dBm
VSWR	Input (Ref. = 50 Ω) Output (Ref. = 50 Ω)	f = 30–500 MHz f = 30–500 MHz	— —	1.2:1 1.2:1	1.5:1 1.5:1	—
VSWR Load	VSWR Survival	P_o = 1.0 W f = 30–500 MHz	—	—	30:1	—
P_{in}	AC Input	V_{in} = 115 Vac, 1.0φ, 60 Hz	—	30	40	W

The RF Line

Integrated UHF Linear Power Amplifier

PAA0510-25-6L

**6.0 WATTS
500–1000 MHz
LINEAR POWER
AMPLIFIER ASSEMBLY**



CASE 389F-01, STYLE 1

. . . designed for wideband linear applications in the 500 to 1000 MHz frequency range. Motorola class A high-power transistors provide excellent ITOs, high gain, and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 500 to 1000 MHz
- Output Power — 7.0 Watts Typical
- Gain — 27 dB
- Linearity — +48.5 dBm Typ ITO
- Noise Figure — 8.0 dB Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling

5

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SSG	Small Signal Gain	f = 500–1000 MHz	25	27		dB
f_r	Frequency Response	f = 500–1000 MHz		±1.0	±1.5	dB
P_O	Power Output	f = 500–1000 MHz	6.0	7.0		W
NF	Noise Figure	f = 500–1000 MHz		8.0	9.5	dB
ITO	Third Order Intercept Point	f = 500–1000 MHz	+47.5	+48.5		dBm
dso	Second Harmonic Attenuation	f = 1.0–2.0 GHz	25	35		dB
VSWR	Input (Ref = 50 Ω) Output (Ref = 50 Ω)	f = 500–1000 MHz f = 500–1000 MHz		2.0:1 2.5:1	2.5:1	
VSWR Load	VSWR Survival	P_O = 6.0 W CW f = 500–1000 MHz			30:1	
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz		85	100	W

PAA0810-24-5L

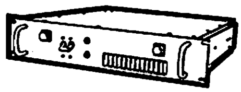
The RF Line

Integrated UHF Linear Power Amplifier

. . . designed for wideband linear applications in the 800 to 1000 MHz frequency range. Motorola class A high-power transistors provide excellent ITOs, high gain, and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 800 to 1000 MHz
- Output Power — 5.0 Watts Typical
- Gain — 26 dB
- Linearity — +47.5 dBm Typ ITO
- Noise Figure — 8.0 dB Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling

**5.0 WATT
800–1000 MHz
LINEAR POWER
AMPLIFIER ASSEMBLY**



CASE 389F-01, STYLE 1

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SSG	Small Signal Gain	f = 800–1000 MHz	24	26		dB
f_r	Frequency Response	f = 800–1000 MHz		±0.5	±1.0	dB
P_o	Power Output	f = 800–1000 MHz	4.5	5.0		W
NF	Noise Figure	f = 800–1000 MHz		8.0	9.5	dB
ITO	Third Order Intercept Point	f = 800–1000 MHz	+46.5	+47.5		dBm
dso	Second Harmonic Attenuation	f = 1.6–2.0 GHz	25	35		dB
VSWR	Input (Ref = 50 Ω) Output (Ref = 50 Ω)	f = 800–1000 MHz f = 800–1000 MHz		2.0:1 2.5:1	2.5:1	
VSWR Load	VSWR Survival	P_o = 5.0 W CW f = 800–1000 MHz			∞:1	
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz		85	100	W

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PAA0810-31-25L

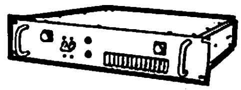
The RF Line

Integrated UHF Linear Power Amplifier

. . . designed for wideband linear applications in the 800 to 1000 MHz frequency range. Motorola class A high-power transistors provide excellent ITOs, high gain, and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 800 to 1000 MHz
- Output Power — 25 Watts Minimum
- Gain — 33 dB
- Linearity — +55 dBm Typ ITO
- Noise Figure — 8.0 dB Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling

**25 WATT
800–1000 MHz
LINEAR POWER
AMPLIFIER ASSEMBLY**



CASE 389F-01, STYLE 1

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SSG	Small Signal Gain	f = 800–1000 MHz	31	33		dB
f_r	Frequency Response	f = 800–1000 MHz		±0.75	±1.0	dB
P_o	Power Output	f = 800–1000 MHz	25	30		W
NF	Noise Figure	f = 800–1000 MHz		8.0	9.0	dB
ITO	Third Order Intercept Point	f = 800–1000 MHz	+54	+55		dBm
dso	Second Harmonic Attenuation	f = 1.6–2.0 GHz	35	40		dB
VSWR	Input (Ref = 50 Ω) Output (Ref = 50 Ω)	f = 800–1000 MHz f = 800–1000 MHz		2.0:1 1.5:1	2.5:1 2.0:1	
VSWR Load	VSWR Survival	P_o = 25 W CW f = 800–1000 MHz			∞:1	
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz		270	300	W

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PAA0810-32-10L

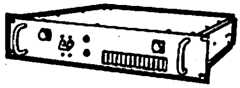
The RF Line

Integrated UHF Linear Power Amplifier

**10 WATT
800–1000 MHz
LINEAR POWER
AMPLIFIER ASSEMBLY**

. . . designed for wideband linear applications in the 800 to 1000 MHz frequency range. Motorola class A high-power transistors provide excellent ITOs, high gain, and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 800 to 1000 MHz
- Output Power — 10 Watts Minimum
- Gain — 35 dB
- Linearity — +56 dBm Typ ITO
- Noise Figure — 8.0 dB Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling



CASE 389F-01, STYLE 1

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SSG	Small Signal Gain	f = 800–1000 MHz	32	35		dB
f_r	Frequency Response	f = 800–1000 MHz		±0.75	±1.0	dB
P_o	Power Output	f = 800–1000 MHz	10	12		W
NF	Noise Figure	f = 800–1000 MHz		8.0	9.0	dB
ITO	Third Order Intercept Point	f = 800–1000 MHz	+48.5	+50		dBm
dso	Second Harmonic Attenuation	f = 1.6–2.0 GHz	35	40		dB
VSWR	Input (Ref = 50 Ω) Output (Ref = 50 Ω)	f = 800–1000 MHz f = 800–1000 MHz		1.5:1 1.5:1	2.0:1 2.0:1	
VSWR Load	VSWR Survival	P_o = 10 W CW f = 800–1000 MHz			∞:1	
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz		180	200	W

5

PAA0810-38-5LAS

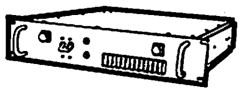
The RF Line

Integrated UHF Linear Power Amplifier

... designed for wideband linear applications in the 800 to 1000 MHz frequency range. Motorola class A high-power transistors provide excellent ITOs, high gain, and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 800 to 1000 MHz
- Output Power — 5.0 Watts Typical
- Gain — 42 dB
- Linearity — +47.5 dBm Typ ITO
- Noise Figure — 8.0 dB Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling

**5.0 WATT
800–1000 MHz
LINEAR POWER
AMPLIFIER ASSEMBLY**



CASE 389F-01, STYLE 1

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ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SSG	Small Signal Gain	f = 800–1000 MHz	38	42		dB
f_r	Frequency Response	f = 800–1000 MHz		±0.75	±1.0	dB
P_o	Power Output	f = 800–1000 MHz	4.5	5.0		W
NF	Noise Figure	f = 800–1000 MHz		8.0	9.0	dB
ITO	Third Order Intercept Point	f = 800–1000 MHz	+46.5	+47.5		dBm
dso	Second Harmonic Attenuation	f = 1.6–2.0 GHz	25	35		dB
VSWR	Input (Ref = 50 Ω) Output (Ref = 50 Ω)	f = 800–1000 MHz f = 800–1000 MHz		2.0:1 2.5:1	2.5:1	
VSWR Load	VSWR Survival	P_o = 5.0 W CW f = 800–1000 MHz			∞:1	
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz		100	125	W

PAA0810-38-100AB

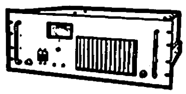
**100 WATTS
800–1000 MHz
LINEAR POWER
AMPLIFIER**

The RF Line

Integrated UHF Linear Power Amplifier

. . . designed for wideband linear applications in the 800 to 1000 MHz frequency range. Motorola high-power transistors provide high gain and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A" Driver Stages, Class "AB" Final Amplifier
- Operates from 115 Vac Power Source
- Frequency Range — 800 to 1000 MHz
- Output Power — 100 Watts Minimum
- Gain — 38 dB Typ
- Infinite VSWR Load Capability, Circulator Protected
- Noise Figure — 8.0 dB Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling
- Built-In System DC Voltmeter
- 220 Vac Model Available, P/N PAE0810-38-100AB



CASE 389G-01

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
P_g	Power Gain	f = 800–1000 MHz, P_o = 100 W	37	38	—	dB
f_r	Frequency Response	f = 800–1000 MHz	—	±1.0	±1.25	dB
P_o	Power Output	f = 800–1000 MHz	100	120	—	W
NF	Noise Figure	f = 800–1000 MHz	—	8.0	9.5	dB
dso	Second Harmonic Attenuation	f = 1.6–2.0 GHz	25	40	—	dB
VSWR	Input (Ref. = 50 Ω) Output (Ref. = 50 Ω)	f = 800–1000 MHz f = 800–1000 MHz	— —	2.0:1 1.25:1	2.5:1 1.5:1	—
VSWR Load	VSWR Survival	P_o = 100 W CW f = 800–1000 MHz	—	—	∞:1	—
$P_{AC\text{-}IN}$	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz	—	700	825	W

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PAA0810-40-50L

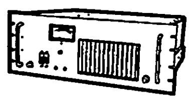
The RF Line

Integrated UHF Linear Power Amplifier

**50 WATT
800–1000 MHz
LINEAR POWER
AMPLIFIER**

. . . designed for wideband linear applications in the 800 to 1000 MHz frequency range. Motorola class A high-power transistors provide excellent ITOs, high gain, and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 800 to 1000 MHz
- Output Power — 50 Watts Minimum
- Gain — 42 dB
- Linearity — +56 dBm Typ ITO
- Noise Figure — 8.0 dB Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling
- Built-In System DC Voltmeter



CASE 389G-01, STYLE 1

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SSG	Small Signal Gain	f = 800–1000 MHz	40	42		dB
f_r	Frequency Response	f = 800–1000 MHz		±0.75	±1.0	dB
P_o	Power Output	f = 800–1000 MHz	50	55		W
NF	Noise Figure	f = 800–1000 MHz		8.0	9.0	dB
ITO	Third Order Intercept Point	f = 800–1000 MHz	+55	+56.5		dBm
dso	Second Harmonic Attenuation	f = 1.6–2.0 GHz	40	50		dB
VSWR	Input (Ref = 50 Ω) Output (Ref = 50 Ω)	f = 800–1000 MHz f = 800–1000 MHz		2.0:1 1.25:1	2.5:1 1.5:1	
VSWR Load	VSWR Survival	P_o = 50 W CW f = 800–1000 MHz			∞:1	
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz		560	600	W

5

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

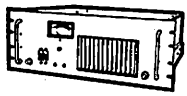
PAA0810-40-50LAM

The RF Line
Integrated UHF Linear Power Amplifier

50 WATT
800–1000 MHz
LINEAR POWER
AMPLIFIER

. . . designed for wideband linear applications in the 800 to 1000 MHz frequency range. Motorola class A high-power transistors provide excellent ITOs, high gain, and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 800 to 1000 MHz
- Output Power — 50 Watts Minimum
- Gain — 42 dB
- Linearity — +56 dBm Typ ITO
- Noise Figure — 8.0 dB Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling
- Built-In RF Wattmeter
- Built-In Low Pass Filter and Directional Coupler



CASE 388G-01, STYLE 1

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SSG	Small Signal Gain	f = 800–1000 MHz	40	42		dB
f_r	Frequency Response	f = 800–1000 MHz		±0.75	±1.0	dB
P_O	Power Output	f = 800–1000 MHz	50	55		W
NF	Noise Figure	f = 800–1000 MHz		8.0	9.0	dB
ITO	Third Order Intercept Point	f = 800–1000 MHz	+55	+56		dBm
dso	Second Harmonic Attenuation	f = 1.6–2.0 GHz	40	50		dB
VSWR	Input (Ref = 50 Ω) Output (Ref = 50 Ω)	f = 800–1000 MHz f = 800–1000 MHz		2.0:1 1.25:1	2.5:1 1.5:1	
VSWR Load	VSWR Survival	P_O = 50 W CW f = 800–1000 MHz			∞:1	
Sample Level	Directional Coupler Output	f = 800–1000 MHz		−30		dBc
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz		560	600	W
P_O Scale	RF Wattmeter Range Power Output	f = 800–1000 MHz			100	W
P_r	RF Wattmeter Range Reflected Power	f = 800–1000 MHz			25	W

5

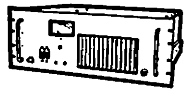
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PAA0810-52-100AB

The RF Line

Integrated UHF Linear Power Amplifier

100 WATTS
800–1000 MHz
LINEAR POWER
AMPLIFIER



CASE 389G-01

. . . designed for wideband linear applications in the 800 to 1000 MHz frequency range. Motorola high-power transistors provide high gain and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A" Driver Stages, Class "AB" Final Amplifier
- Operates from 115 Vac Power Source
- Frequency Range — 800 to 1000 MHz
- Output Power — 100 Watts Minimum
- Gain — 52 dB Typ
- Infinite VSWR Load Capability, Circulator Protected
- Noise Figure — 9.0 dB Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling
- Built-In System DC Voltmeter
- 220 Vac Model Available, P/N PAE0810-52-100AB

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ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
P_g	Power Gain	f = 800–1000 MHz, P_O = 100 W	50	52	—	dB
f_r	Frequency Response	f = 800–1000 MHz	—	±1.0	±1.25	dB
P_O	Power Output	f = 800–1000 MHz	100	120	—	W
NF	Noise Figure	f = 800–1000 MHz	—	9.0	10	dB
dso	Second Harmonic Attenuation	f = 1.6–2.0 GHz	25	40	—	dB
VSWR	Input (Ref. = 50 Ω) Output (Ref. = 50 Ω)	f = 800–1000 MHz f = 800–1000 MHz	— —	2.0:1 1.25:1	2.5:1 1.5:1	—
VSWR Load	VSWR Survival	P_O = 100 W CW f = 800–1000 MHz	—	—	∞:1	—
$P_{AC\text{-}IN}$	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz	—	700	825	W

PAA0810-52-100AM

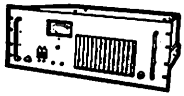
The RF Line

Integrated UHF Linear Power Amplifier

100 WATTS
80–1000 MHz
LINEAR POWER
AMPLIFIER

. . . designed for wideband linear applications in the 800 to 1000 MHz frequency range. Motorola high-power transistors provide high gain and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A" Driver Stages, Class "AB" Final Amplifier
- Operates from 115 Vac Power Source
- Frequency Range — 800 to 1000 MHz
- Output Power — 100 Watts Minimum
- Gain — 52 dB
- Infinite VSWR Load Capability, Circulator Protected
- Noise Figure — 8.0 dB Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling
- Built-In RF Wattmeter and Directional Coupler
- 220 Vac Model Available, P/N PAE0810-52-100AM



CASE 389G-01

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
P_g	Power Gain	f = 800–1000 MHz, P_o = 100 W	51	52	—	dB
f_r	Frequency Response	f = 800–1000 MHz	—	±1.0	±1.25	dB
P_o	Power Output	f = 800–1000 MHz	100	120	—	W
NF	Noise Figure	f = 800–1000 MHz	—	8.0	9.5	dB
dso	Second Harmonic Attenuation	f = 1.6–2.0 GHz	25	40	—	dB
VSWR	Input (Ref. = 50 Ω) Output (Ref. = 50 Ω)	f = 800–1000 MHz f = 800–1000 MHz	— —	2.0:1 1.25:1	2.5:1 1.5:1	—
VSWR Load	VSWR Survival	P_o = 100 W CW f = 800–1000 MHz	—	—	∞:1	—
$P_{AC\text{-}IN}$	AC Input	V_{in} = 115 Vac, 1φ, 60 Hz	—	700	825	W
Sample Level	Directional Coupler Output	f = 800–1000 MHz	—	−30	—	dBc
P_o Scale	RF Wattmeter Range Power Output	f = 800–1000 MHz	—	—	250	W
P_r	RF Wattmeter Range Reflected Power	f = 800–1000 MHz	—	—	50	W

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PAA0810-54-50LAS

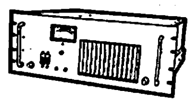
The RF Line

Integrated UHF Linear Power Amplifier

. . . designed for wideband linear applications in the 800 to 1000 MHz frequency range. Motorola class A high-power transistors provide excellent ITOs, high gain, and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 800 to 1000 MHz
- Output Power — 50 Watts Minimum
- Gain — 56 dB
- Linearity — +56 dBm Typ ITO
- Noise Figure — 8.0 dB Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housings with Dip Brazed Plenum Assembly
- Forced Air Cooling
- Built-In System DC Voltmeter

**50 WATT
800–1000 MHz
LINEAR POWER
AMPLIFIER**



CASE 389G-01, STYLE 1

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SSG	Small Signal Gain	f = 800–1000 MHz	54	56		dB
f_r	Frequency Response	f = 800–1000 MHz		±0.75	±1.0	dB
P_o	Power Output	f = 800–1000 MHz	50	55		W
NF	Noise Figure	f = 800–1000 MHz		8.0	9.0	dB
ITO	Third Order Intercept Point	f = 800–1000 MHz	+55	+56.5		dBm
dso	Second Harmonic Attenuation	f = 1.6–2.0 GHz	40	50		dB
VSWR	Input (Ref = 50 Ω) Output (Ref = 50 Ω)	f = 800–1000 MHz f = 800–1000 MHz		2.0:1 1.25:1	2.5:1 1.5:1	
VSWR Load	VSWR Survival	P_o = 50 W CW f = 800–1000 MHz			∞:1	
P_{in}	AC Input	V_{in} = 115 Vac, 1.0φ, 60 Hz		560	600	W

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PAA0810-54-50LSM

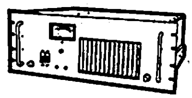
The RF Line

Integrated UHF Linear Power Amplifier

... designed for wideband linear applications in the 800 to 1000 MHz frequency range. Motorola class A high-power transistors provide excellent ITOs, high gain, and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 800 to 1000 MHz
- Output Power — 50 Watts Minimum
- Gain — 56 dB
- Linearity — +56 dBm Typ ITO
- Noise Figure — 8.0 dB Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling
- Built-In RF Wattmeter
- Built-In Low Pass Filter and Directional Coupler

**50 WATT
800–1000 MHz
LINEAR POWER
AMPLIFIER**



CASE 389G-01, STYLE 1

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SSG	Small Signal Gain	f = 800–1000 MHz	54	56		dB
f_r	Frequency Response	f = 800–1000 MHz		±0.75	±1.0	dB
P_o	Power Output	f = 800–1000 MHz	50	55		W
NF	Noise Figure	f = 800–1000 MHz		8.0	9.0	dB
ITO	Third Order Intercept Point	f = 800–1000 MHz	+55	+56		dBm
dso	Second Harmonic Attenuation	f = 1.6–2.0 GHz	40	50		dB
VSWR	Input (Ref = 50 Ω) Output (Ref = 50 Ω)	f = 800–1000 MHz f = 800–1000 MHz		2.0:1 1.25:1	2.5:1 1.5:1	
VSWR Load	VSWR Survival	P_o = 50 W CW f = 800–1000 MHz			∞:1	
Sample Level	Directional Coupler Output	f = 800–1000 MHz		−30		dBc
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz		560	600	W
P_o Scale	RF Wattmeter Range Power Output	f = 800–1000 MHz			100	W
P_r	RF Wattmeter Range Reflected Power	f = 800–1000 MHz			25	W

PAA1000-14-0.6L

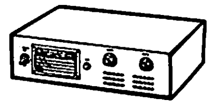
The RF Line

Integrated Power Amplifier

**0.8 WATT
10–1000 MHz
LINEAR POWER
AMPLIFIER**

. . . designed for wideband linear applications in the 10 to 1000 MHz frequency range. Contains an all hybrid amplifier module — Motorola's own proven reliable circuitry, used in millions of operating units over twenty years — utilizing Motorola's class A transistors. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 10 to 1000 MHz
- Output Power — 0.6 Watt Minimum
- Gain — 15 dB Typ
- Linearity — +43 dBm Typ ITO
- Noise Figure — 7.5 dB Typ @ f = 500 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Forced Air Cooling
- Thermally Protected
- 220 Vac Model Available, P/N PAE1000-14-0.6L



CASE 389R-01, STYLE 1

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
P_g	Power Gain	f = 100 MHz	14	15	16	dB
f_r	Frequency Response	f = 10–1000 MHz	—	±0.5	±1.0	dB
P_{o1dB}	Power Output, 1.0 dB Compression	f = 500 MHz f = 1000 MHz	0.6 0.5	0.8 0.6	— —	W
NF	Noise Figure	f = 500 MHz f = 1000 MHz	— —	7.5 8.5	8.5 9.5	dB
ITO	Third Order Intercept Point	f = 500 MHz f = 1000 MHz	+41 +40	+43 +42	— —	dBm
VSWR	Input (Ref. = 50 Ω) Output (Ref. = 50 Ω)	f = 10–1000 MHz f = 10–1000 MHz	— —	2.0:1 2.0:1	2.5:1 2.5:1	—
VSWR Load	VSWR Survival	P_o = 0.6 W f = 10–1000 MHz	—	—	30:1	—
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz	—	25	35	W

PAA1000-14-1.3L

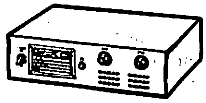
The RF Line

Integrated Power Amplifier

1.6 WATTS
10–1000 MHz
LINEAR POWER
AMPLIFIER

... designed for wideband linear applications in the 10 to 1000 MHz frequency range. Contains an all hybrid amplifier module — Motorola's own proven reliable circuitry, used in millions of operating units over twenty years — utilizing Motorola's class A transistors. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 10 to 1000 MHz
- Output Power — 1.3 Watts Minimum
- Gain — 15 dB Typ
- Linearity — +45 dBm Typ ITO
- Noise Figure — 8.0 dB Typ @ f = 500 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Forced Air Cooling
- Thermally Protected
- 220 Vac Model Available, P/N PAE1000-14-1.3L



CASE 389R-01, STYLE 1

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
P_g	Power Gain	f = 100 MHz	14	15	16	dB
f_r	Frequency Response	f = 10–1000 MHz	—	±0.8	±1.5	dB
P_{o1dB}	Power Output, 1.0 dB Compression	f = 500 MHz f = 1000 MHz	1.3 1.0	1.6 1.3	— —	W
NF	Noise Figure	f = 500 MHz f = 1000 MHz	— —	8.0 9.0	9.0 10	dB
ITO	Third Order Intercept Point	f = 500 MHz f = 1000 MHz	+43 +42	+45 +44	— —	dBm
VSWR	Input (Ref. = 50 Ω) Output (Ref. = 50 Ω)	f = 10–1000 MHz f = 10–1000 MHz	— —	2.0:1 2.0:1	2.5:1 2.5:1	—
VSWR Load	VSWR Survival	P_o = 1.3 W f = 10–1000 MHz	—	—	30:1	—
P_{in}	AC Input	V_{in} = 115 Vac, 1.0φ, 60 Hz	—	45	55	W

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PAA1000-30-0.6L

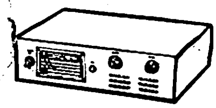
The RF Line

Integrated Power Amplifier

0.8 WATT
10–1000 MHz
LINEAR POWER AMPLIFIER

. . . designed for wideband linear applications in the 10 to 1000 MHz frequency range. Contains an all hybrid amplifier module — Motorola's own proven reliable circuitry, used in millions of operating units over twenty years — utilizing Motorola's class A transistors. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- All Class "A"
- Operates from 115 Vac Power Source
- Frequency Range — 10 to 1000 MHz
- Output Power — 0.6 Watt Minimum
- Gain — 32 dB Typ
- Linearity — +43 dBm Typ ITO
- Noise Figure — 6.5 dB Typ @ f = 500 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Forced Air Cooling
- Thermally Protected
- 220 Vac Model Available, P/N PAE1000-30-0.6L



CASE 389R-01, STYLE 1

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
P_g	Power Gain	f = 100 MHz	30	32	34	dB
f_r	Frequency Response	f = 10–1000 MHz	—	±1.0	±1.5	dB
P_{o1dB}	Power Output, 1.0 dB Compression	f = 500 MHz f = 1000 MHz	0.6 0.5	0.8 0.6	— —	W
NF	Noise Figure	f = 500 MHz f = 1000 MHz	— —	6.5 7.5	8.0 9.0	dB
ITO	Third Order Intercept Point	f = 500 MHz f = 1000 MHz	+41 +40	+43 +42	— —	dBm
VSWR	Input (Ref. = 50 Ω) Output (Ref. = 50 Ω)	f = 10–1000 MHz f = 10–1000 MHz	— —	2.0:1 2.0:1	2.5:1 2.5:1	—
VSWR Load	VSWR Survival	P_o = 0.6 W f = 10–1000 MHz	—	—	30:1	—
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz	—	35	45	W

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

PAA1000-42-5L

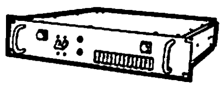
The RF Line

Ultrawide Band Linear Power Amplifier

. . . designed for wideband linear applications in the 25 to 1000 MHz frequency range. Motorola class A hybrid amplifiers provide excellent ITOs, high gain, and wide dynamic range. Designed for high reliability with such standard features as a high-quality power supply, EMI/RFI filter, stainless steel hardware and many MIL-STD heavy duty components. Each unit undergoes 24-hour burn-in prior to final test and Q/A.

- *All Class "A"*
- All Hybrid RF Amplifier Circuitry
- Operates from 115 Vac Power Source
- Frequency Range — 25 to 1000 MHz
- Output Power — 5.0 Watts Minimum
- Gain — 42 dB
- Linearity — +46.5 dBm Typ ITO
- Noise Figure — 7.5 dB Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing with Dip Brazed Plenum Assembly
- Forced Air Cooling
- 220 Vac Model Available, P/N PAE1000-42-5L

**5.0 WATTS
25–1000 MHz
LINEAR POWER
AMPLIFIER ASSEMBLY**



CASE 389F-01, STYLE 1

ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
SSG	Small Signal Gain	f = 25–1000 MHz	40	42	—	dB
f_r	Frequency Response	f = 25–1000 MHz	—	±1.5	±2.5	dB
P_o	Power Output	f = 25–1000 MHz	5.0	6.0	—	W
NF	Noise Figure	f = 25–1000 MHz	—	7.5	8.5	dB
ITO	Third Order Intercept Point	f = 25 –1000 MHz	+45.5	+46.5	—	dBm
dso	Second Harmonic Attenuation	f = 0.05–2.0 GHz	25	35	—	dB
VSWR	Input (Ref. = 50 Ω) Output (Ref. = 50 Ω)	f = 25–1000 MHz f = 25–1000 MHz	— —	2.0:1 1.5:1	2.5:1 2.5:1	—
VSWR Load	VSWR Survival	P_o = 5.0 W CW f = 25–1000 MHz	—	—	∞:1	—
P_{in}	AC Input	V_{in} = 115 Vac, 1.0ϕ, 60 Hz	—	200	225	W

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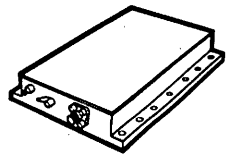
PAM0105-6-50L

The RF Line
Linear Power Amplifier

. . . designed for wideband linear applications in the 100–500 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified V_{CC} = 24 Volt and T_C = 25°C Characteristics:
  Frequency Range — 100 to 500 MHz
  Output Power — 55 W (Typ), 100–500 MHz
  Power Gain — 7.0 dB Typ @ f = 500 MHz
  ITO — 56.5 dBm Typ @ f = 500 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- 28 V_{CC} Model Available, P/N PAM0105-6-50LA

**55 WATTS
100–500 MHz
LINEAR
RF POWER
AMPLIFIER**



CASE 389C-01, STYLE 1
(PAM)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	25	Vdc
RF Power Input	P_{in}	25	W
Storage Temperature Range	T_{stg}	−55 to +125	°C
Operating Temperature Range	T_C	−40 to +70	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 24 V)	I_{CC}	—	12	—	A
Power Gain (f = 100–500 MHz)	P_G	6.0	7.0	—	dB
Bandwidth	BW	100	—	500	MHz
Gain Flatness (f = 100–500 MHz)	—	—	±1.0	±1.5	dB
Input VSWR (f = 100–500 MHz)	$VSWR_{in}$	—	1.35:1	1.75:1	—
Output VSWR (f = 100–500 MHz)	$VSWR_{out}$	—	1.35:1	1.75:1	—
Third Order Intercept Point (f = 100–500 MHz) (See Figure 1)	ITO	+55	+56.5	—	dBm
Load Mismatch (P_o = 50 W, f = 100 MHz, Load VSWR = ∞:1)	ψ	No Damage or Degradation in Performance			
Saturated Output Power (Single Tone) (f = 100–500 MHz)	P_{sat}	60	70	—	W
Power Output	P_{out}	50	55	—	W
Second Harmonic Suppression (P_{out} = 50 W, CW, f_{2h} = 200 MHz)	d_{so}	25	35	—	dB

$$ITO = P_o + \frac{IMD}{2} \text{ @ IMD} > 60 \text{ dB}$$

$$PEP = 4 \times P_o \text{ @ IMD} = -32 \text{ dB}$$

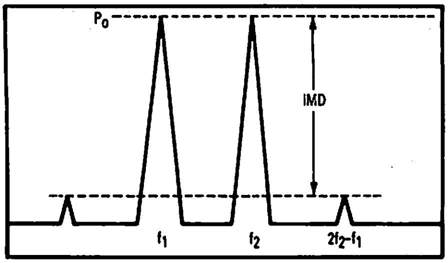


Figure 1. 2-Tone Intermodulation Test

PAM0105-7-25L

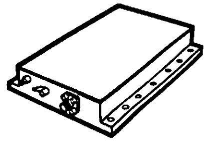
The RF Line

Linear Power Amplifier

. . . designed for wideband linear applications in the 100–500 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified V_{CC} = 24 Volt and T_C = 25°C Characteristics:
  Frequency Range — 100 to 500 MHz
  Output Power — 30 W (Typ), 100–500 MHz
  Power Gain — 7.5 dB Typ @ f = 500 MHz
  ITO — 53.5 dBm Typ @ f = 500 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- 28 V_{CC} Model Available, P/N PAM0105-7-25LA

**30 WATTS
100–500 MHz
LINEAR
RF POWER
AMPLIFIER**



CASE 389E-01, STYLE 1
(PAM)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	25	Vdc
RF Power Input	P_{in}	12	W
Storage Temperature Range	T_{stg}	−55 to +125	°C
Operating Temperature Range	T_C	−40 to +70	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 24 V)	I_{CC}	—	6.0	—	A
Power Gain (f = 100–500 MHz)	P_G	6.0	7.5	—	dB
Bandwidth	BW	100	—	500	MHz
Gain Flatness (f = 100–500 MHz)	—	—	±1.5	±1.75	dB
Input VSWR (f = 100–500 MHz)	$VSWR_{in}$	—	3.0:1	—	—
Output VSWR (f = 100–500 MHz)	$VSWR_{out}$	—	3.0:1	—	—
Third Order Intercept Point (f = 100–500 MHz) (See Figure 1)	ITO	+52.5	+53.5	—	dBm
Noise Figure (f = 100–500 MHz)	NF	—	10	11.5	dB
Load Mismatch (P_o = 25 W, f = 100 MHz, Load VSWR = ∞:1)	ψ	No Damage or Degradation in Performance			
Saturated Output Power (Single Tone) (f = 100–500 MHz)	P_{sat}	30	35	—	W
Power Output	P_{out}	25	30	—	W
Second Harmonic Suppression (P_{out} = 25 W, CW, f_{2h} = 0.2–1.0 GHz)	d_{so}	20	33	—	dB

$$ITO = P_0 + \frac{IMD}{2} @ IMD > 60\ dB$$

$$PEP = 4 \times P_0 @ IMD = -32\ dB$$

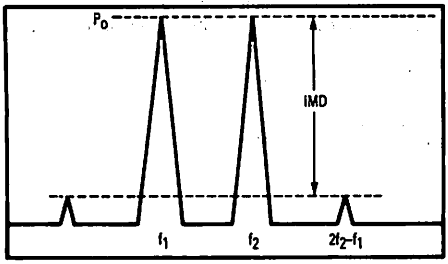


Figure 1. 2-Tone Intermodulation Test

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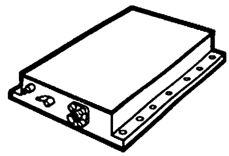
PAM0105-29-6L

The RF Line
Linear Power Amplifier

... designed for wideband linear applications in the 100–500 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified V_{CC} = 24 Volt and T_C = 25°C Characteristics:
  Frequency Range — 100 to 500 MHz
  Output Power — 8.0 W (Typ), 100–500 MHz
  Power Gain, Small-Signal — 31 dB Typ @ f = 500 MHz
  ITO — 48.5 dBm Typ @ f = 500 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- 28 V_{CC} Model Available, P/N PAM0105-29-6LA

**8.0 WATTS
100–500 MHz
LINEAR
RF POWER
AMPLIFIER**



CASE 389C-01, STYLE 1
(PAM)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	26	Vdc
RF Power Input	P_{in}	15	dBm
Storage Temperature Range	T_{stg}	−55 to +125	°C
Operating Temperature Range	T_C	−40 to +90	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 24 V)	I_{CC}	—	1800	1950	mAdc
Small-Signal Gain (f = 100–500 MHz)	G_{SS}	29	31	—	dB
Bandwidth	BW	100	—	500	MHz
Gain Flatness (f = 100–500 MHz)	—	—	±1.5	±2.0	dB
Input VSWR (f = 100–500 MHz)	$VSWR_{in}$	—	3.0:1	3.5:1	—
Output VSWR (f = 100–500 MHz)	$VSWR_{out}$	—	2.0:1	3.0:1	—
Third Order Intercept Point (f = 100–500 MHz) (See Figure 1)	ITO	+47.5	+48.5	—	dBm
Noise Figure (f = 100–500 MHz)	NF	—	6.5	7.5	dB
Load Mismatch (P_o = 6.0 W, f = 100 MHz, Load VSWR = ∞:1)	ψ	No Damage or Degradation in Performance			
Saturated Output Power (Single Tone) (f = 100–500 MHz)	P_{sat}	8.0	10	—	W
Power Output	P_{out}	6.0	8.0	—	W
Second Harmonic Suppression (P_{out} = 6.0 W CW, f_{2h} = 200 MHz)	d_{so}	15	20	—	dB

$$ITO = P_O + \frac{IMD}{2} @ IMD > 60\ dB$$

$$PEP = 4 \times P_O @ IMD = -32\ dB$$

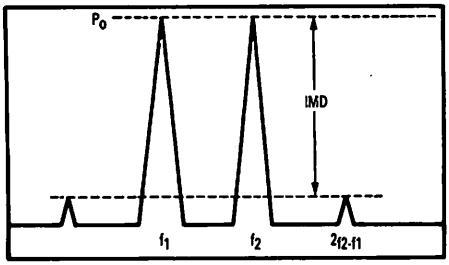


Figure 1. 2-Tone Intermodulation Test

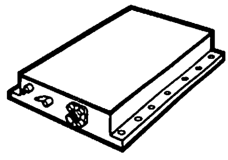
PAM225-42-10LA

The RF Line
Linear Power Amplifier

. . . designed for wideband linear applications in the VHF frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 28 volts.

- Specified V_{CC} = 28 Volt and T_C = 25°C Characteristics:
  Frequency Range — 172 to 225 MHz
  Output Power — 10 W Peak Sync Output
  Power Gain, Small-Signal — 46 dB Typ @ f = 225 MHz
  Noise Figure — 5.0 dB Typ @ f = 225 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability

**10 WATTS
172–225 MHz
LINEAR
RF POWER
AMPLIFIER**



CASE 389C-01
(PAM)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	29	Vdc
RF Power Input	P_{in}	5.0	dBm
Storage Temperature Range	T_{stg}	−55 to +125	°C
Operating Temperature Range	T_C	−40 to +90	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 28 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 28 V)	I_{CC}	—	3.4	—	Adc
Small-Signal Gain (f = 172–225 MHz)	G_{SS}	42	46	51	dB
Bandwidth	BW	172	—	225	MHz
Gain Flatness (f = 172–225 MHz)	—	—	±0.5	±1.0	dB
Input VSWR (f = 172–225 MHz)	$VSWR_{in}$	—	1.5:1	2.0:1	—
Output VSWR (f = 172–225 MHz)	$VSWR_{out}$	—	2.0:1	2.5:1	—
Noise Figure (f = 172–225 MHz)	NF	5.0	5.0	—	dB
Load Mismatch (P_o = 10 W, f = 172 MHz, Load VSWR = ∞:1)	ψ	No Damage or Degradation in Performance			
Power Output (See Figure 1) @ IMD 3-Tone = −58 dB, Vision Carrier = −8.0 dB Reference, Sound Carrier = −10 dB Reference, Sideband Carrier = −16 dB Reference	$P_{out(1)}$	10	—	—	W
Power Output @ IMD 3-Tone = −55 dB, Vision Carrier = −8.0 dB Reference, Sound Carrier = −7.0 dB Reference, Sideband Carrier = −16 dB Reference	$P_{out(2)}$	10	—	—	W

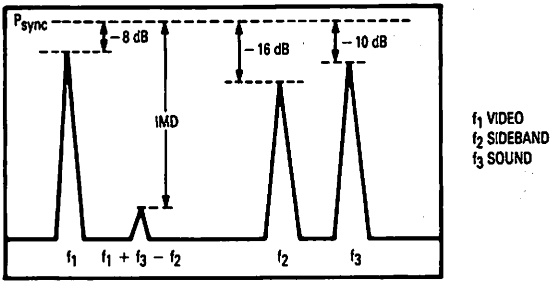


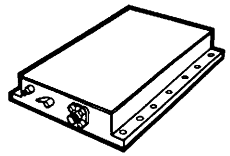
Figure 1. 3-Tone TV Intermodulation Test

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

The RF Line
Linear Power Amplifier

PAM0510-25-6L

6.0 WATTS
500–1000 MHz
LINEAR
RF POWER
AMPLIFIER



CASE 389C-01, STYLE 1
(PAM)

... designed for wideband linear applications in the 500–1000 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified V_{CC} = 24 Volt and T_C = 25°C Characteristics:
  Frequency Range — 500 to 1000 MHz
  Output Power — 7.0 W (Typ)
  Gain, Small-Signal — 27 dB Typ @ f = 1000 MHz
  ITO — +48.5 dBm Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- 28 V_{CC} Model Available, P/N PAM0510-25-6LA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	25	Vdc
RF Power Input	P_{in}	+20	dBm
Storage Temperature Range	T_{stg}	−55 to +125	°C
Operating Temperature Range	T_C	−40 to +70	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 24 V)	I_{CC}	—	1600	1750	mAdc
Small-Signal Gain (f = 500–1000 MHz)	G_{SS}	25	27	—	dB
Bandwidth	BW	500	—	1000	MHz
Gain Flatness (f = 500–1000 MHz)	—	—	±1.0	±1.5	dB
Input VSWR (f = 500–1000 MHz)	$VSWR_{in}$	—	—	2.5:1	—
Output VSWR (f = 500–1000 MHz)	$VSWR_{out}$	—	2.5:1	—	—
Third Order Intercept Point (f = 500–1000 MHz) (See Figure 1)	ITO	+47.5	+48.5	—	dBm
Noise Figure (f = 500–1000 MHz)	NF	—	8.0	9.5	dB
Load Mismatch (P_o = 6.0 W, f = 500 MHz, Load VSWR = ∞:1)	ψ	No Damage or Degradation in Performance			
Saturated Output Power (Single Tone) (f = 500–1000 MHz)	P_{sat}	7.0	8.0	—	W
Power Output (f = 500–1000 MHz)	P_o	6.0	7.0	—	W
Second Harmonic Suppression (P_{out} = 6.0 W CW, f_{2h} = 1.0 GHz)	d_{so}	25	35	—	dB

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$$ITO = P_O + \frac{IMD}{2} \text{ @ } IMD > 60 \text{ dB}$$

$$PEP = 4 \times P_O \text{ @ } IMD = -32 \text{ dB}$$

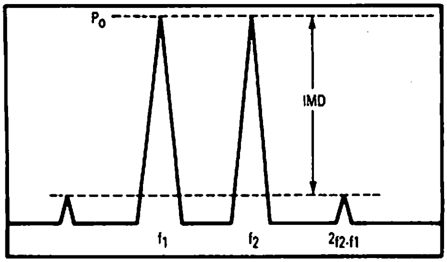
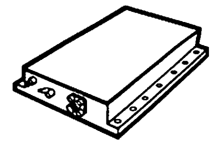


Figure 1. 2-Tone Intermodulation Test

The RF Line
Linear Power Amplifier

PAM0810-6-50L

**60 WATTS
800–1000 MHz
LINEAR
RF POWER
AMPLIFIER**



CASE 389D-01, STYLE 1
(PAM)

. . . designed for wideband linear applications in the 800–1000 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified V_{CC} = 24 Volt and T_C = 25°C Characteristics:
  Frequency Range — 800 to 1000 MHz
  Output Power — 50 W (Typ), 800–1000 MHz
  Power Gain — 7.0 dB Typ @ f = 1000 MHz
  ITO — 56.5 dBm Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- 28 V_{CC} Model Available, P/N PAM0810-6-50LA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	25	Vdc
RF Power Input	P_{in}	20	W
Storage Temperature Range	T_{stg}	−55 to +125	°C
Operating Temperature Range	T_C	−40 to +70	°C

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ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 28 V)	I_{CC}	—	9.6	—	Adc
Power Gain (f = 800–1000 MHz)	G_P	6.0	7.0	—	dB
Bandwidth	BW	800	—	1000	MHz
Gain Flatness (f = 800–1000 MHz)	—	—	±0.5	±0.75	dB
Input VSWR (f = 800–1000 MHz)	$VSWR_{in}$	—	—	1.5:1	—
Output VSWR (f = 800–1000 MHz)	$VSWR_{out}$	—	—	1.5:1	—
Third Order Intercept Point (f = 800–1000 MHz) (See Figure 1)	ITO	56	56.5	—	dBm
Load Mismatch (P_o = 50 W, f = 800 MHz, Load VSWR = ∞:1)	ψ	No Damage or Degradation in Performance			
Saturated Output Power (Single Tone) (f = 800–1000 MHz)	P_{sat}	60	70	—	W
Power Output	P_{out}	50	60	—	W
Second Harmonic Suppression (P_{out} = 50 W CW, f_{2h} = 1.6 GHz)	d_{so}	35	45	—	dB

$$ITO = P_o + \frac{IMD}{2} \text{ @ } IMD > 60 \text{ dB}$$

$$PEP = 4 \times P_o \text{ @ } IMD = -32 \text{ dB}$$

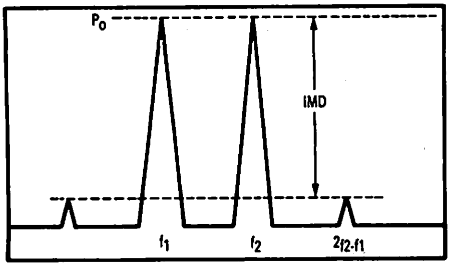

Figure 1. 2-Tone Intermodulation Test

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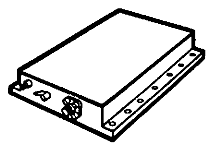
PAM0810-7-25L

The RF Line
Linear Power Amplifier

... designed for wideband linear applications in the 800–1000 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified V_{CC} = 24 Volt and T_C = 25°C Characteristics:
  Frequency Range — 800 to 1000 MHz
  Output Power — 30 W (Typ) @ 1.0 dB Compression
  Power Gain, Small-Signal — 8.0 dB Typ @ f = 1000 MHz
  ITO — 55 dBm Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- 28 V_{CC} Model Available, P/N PAM0810-7-25LA

**30 WATTS
800–1000 MHz
LINEAR
RF POWER
AMPLIFIER**



CASE 389E-01, STYLE 1
(PAM)

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	25	Vdc
RF Power Input	P_{in}	10	W
Storage Temperature Range	T_{stg}	−55 to +125	°C
Operating Temperature Range	T_C	−40 to +70	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 24 V)	I_{CC}	—	4.8	—	Adc
Small-Signal Gain (f = 800–1000 MHz)	G_{SS}	7.0	8.0	—	dB
Bandwidth	BW	800	—	1000	MHz
Gain Flatness (f = 800–1000 MHz)	—	—	±0.5	±0.75	dB
Input VSWR (f = 800–1000 MHz)	$VSWR_{in}$	—	1.5:1	2.0:1	—
Output VSWR (f = 800–1000 MHz)	$VSWR_{out}$	—	1.5:1	2.0:1	—
Third Order Intercept Point (f = 800–1000 MHz) (See Figure 1)	ITO	54	55	—	dBm
Noise Figure (f = 800–1000 MHz)	NF	—	11	12.5	dB
Load Mismatch (P_o = 25 W, f = 800 MHz, Load VSWR = ∞:1)	ψ	No Damage or Degradation in Performance			
Saturated Output Power (Single Tone) (f = 800–1000 MHz)	P_{sat}	35	40	—	W
Power Output @ 1.0 dB Compression Point	$P_{1\ dB}$	25	30	—	W
Second Harmonic Suppression (P_{out} = 25 W CW, f_{2h} = −2.0 GHz)	d_{so}	35	45	—	dB

$$ITO = P_o + \frac{IMD}{2} \text{ @ } IMD > 60\text{ dB}$$

$$PEP = 4 \times P_o \text{ @ } IMD = -32\text{ dB}$$

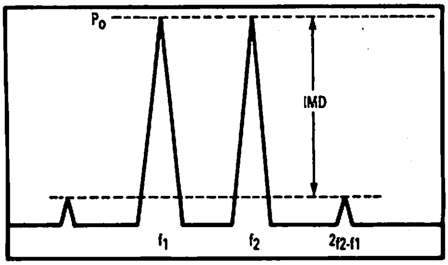

Figure 1. 2-Tone Intermodulation Test

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PAM0810-8-10L

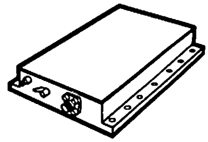
The RF Line

Linear Power Amplifier

... designed for wideband linear applications in the 800–1000 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified V_{CC} = 24 Volt and T_C = 25°C Characteristics:
  Frequency Range — 800 to 1000 MHz
  Output Power — 12 W (Typ), 800–1000 MHz
  Power Gain, Small-Signal — 10 dB Typ @ f = 1000 MHz
  ITO — 50 dBm Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- 28 V_{CC} Model Available, P/N PAM0810-8-10LA

**12 WATTS
800–1000 MHz
LINEAR
RF POWER
AMPLIFIER**



CASE 389E-01, STYLE 1
(PAM)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	25	Vdc
RF Power Input	P_{in}	6.0	W
Storage Temperature Range	T_{stg}	−55 to +125	°C
Operating Temperature Range	T_C	−40 to +70	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 24 V)	I_{CC}	—	2.4	—	A
Small-Signal Gain (f = 800–1000 MHz)	G_{SS}	8.0	10	—	dB
Bandwidth	BW	800	—	1000	MHz
Gain Flatness (f = 800–1000 MHz)	—	—	±0.5	±0.75	dB
Input VSWR (f = 800–1000 MHz)	$VSWR_{in}$	—	1.5:1	2.0:1	—
Output VSWR (f = 800–1000 MHz)	$VSWR_{out}$	—	1.5:1	2.0:1	—
Third Order Intercept Point (f = 800–1000 MHz) (See Figure 1)	ITO	+48.5	+50	—	dBm
Noise Figure (f = 800–1000 MHz)	NF	—	10	11.5	dB
Load Mismatch (P_o = 10 W, f = 800 MHz, Load VSWR = ∞:1)	ψ	No Damage or Degradation in Performance			
Saturated Output Power (Single Tone) (f = 800–1000 MHz)	P_{sat}	12	15	—	W
Power Output	P_{out}	10	12	—	W
Second Harmonic Suppression (P_{out} = 10 W, CW, f_{2h} = 1.6–2.0 GHz)	d_{so}	35	45	—	dB

$$ITO = P_0 + \frac{IMD}{2} \text{ @ } IMD > 60\ dB$$

$$PEP = 4 \times P_0 \text{ @ } IMD = -32\ dB$$

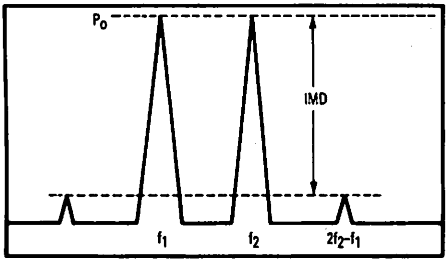


Figure 1. 2-Tone Intermodulation Test

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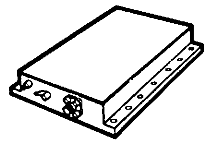
PAM0810-24-3L

The RF Line

Linear Power Amplifier

**3.2 WATTS
800–1000 MHz
LINEAR
RF POWER
AMPLIFIER**



CASE 389C-01, STYLE 1
(PAM)

. . . designed for wideband linear applications in the 800 to 1000 MHz frequency range. This solid state, class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified V_{CC} = 24 Volts and T_C = 25°C Characteristics:
  Frequency Range — 800 to 1000 MHz
  Output Power — 3.2 W (Typ) @ −32 dB IMD
  Power Gain, Small-Signal — 26 dB Typ @ f = 1000 MHz
  ITO — 45 dBm Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- 28 V_{CC} Model Available, P/N PAM0810-24-3LA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	26	Vdc
RF Power Input	P_{in}	20	dBm
Storage Temperature Range	T_{stg}	−55 to +125	°C
Operating Temperature Range	T_C	−40 to +70	°C

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ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 24 V)	I_{CC}	—	950	1050	mAdc
Small-Signal Gain (f = 800–1000 MHz)	G_{SS}	24	26	—	dB
Bandwidth	BW	800	—	1000	MHz
Gain Flatness (f = 800–1000 MHz)	—	—	±0.5	±1.0	dB
Input VSWR (f = 800–1000 MHz)	$VSWR_{in}$	—	—	2.5:1	—
Output VSWR (f = 800–1000 MHz)	$VSWR_{out}$	—	2.0:1	—	—
Third Order Intercept Point (f = 800–1000 MHz) (See Figure 1)	ITO	44.5	45	—	dBm
Noise Figure (f = 800–1000 MHz)	NF	—	8.0	9.5	dB
Load Mismatch (P_o = 3.0 W, f = 800 MHz, Load VSWR = ∞:1)	ψ	No Damage or Degradation in Performance			
Saturated Output Power (Single Tone) (f = 800–1000 MHz)	P_{sat}	4.0	5.0	—	W
Peak Envelope Power for Two Tone Distortion Test (f = 800–1000 MHz @ −32 dB IMD) (See Figure 1)	P_{out}	2.8	3.2	—	W
Second Harmonic Suppression (P_{out} = 3.0 W CW, f_{2h} = 1.6 GHz)	dso	25	35	—	dB

$$ITO = P_O + \frac{IMD}{2} \text{ @ } IMD > 60 \text{ dB}$$

$$PEP = 4 \times P_O \text{ @ } IMD = -32 \text{ dB}$$

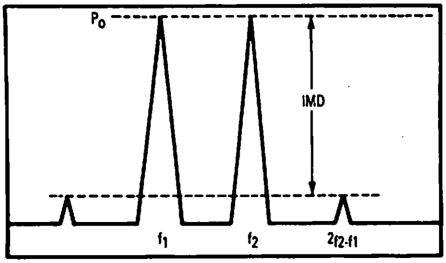


Figure 1. 2-Tone Intermodulation Test

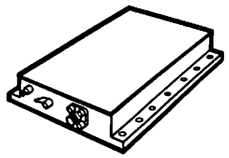
PAM0810-24-5LA

The RF Line
Linear Power Amplifier

... designed for wideband linear applications in the 800–1000 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 28 volts.

- Specified V_{CC} = 28 Volt and T_C = 25°C Characteristics:
  Frequency Range — 800 to 1000 MHz
  Output Power — 5.0 W (Typ) @ −30 dB IMD
  Power Gain, Small-Signal — 26 dB Typ @ f = 1000 MHz
  ITO — 47.5 dBm Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- 24 V_{CC} Model Available, P/N PAM0810-24-5L

**5.0 WATTS
800–1000 MHz
LINEAR
RF POWER
AMPLIFIER**



CASE 389C-01, STYLE 1
(PAM)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	29	Vdc
RF Power Input	P_{in}	20	dBm
Storage Temperature Range	T_{stg}	−55 to +125	°C
Operating Temperature Range	T_C	−40 to +70	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 28 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 28 V)	I_{CC}	—	1600	1750	mAdc
Small-Signal Gain (f = 800–1000 MHz)	G_{SS}	24	26	—	dB
Bandwidth	BW	800	—	1000	MHz
Gain Flatness (f = 800–1000 MHz)	—	—	±0.5	±1.0	dB
Input VSWR (f = 800–1000 MHz)	$VSWR_{in}$	—	—	2.5:1	—
Output VSWR (f = 800–1000 MHz)	$VSWR_{out}$	—	2.5:1	—	—
Third Order Intercept Point (f = 800–1000 MHz) (See Figure 1)	ITO	46.5	47.5	—	dBm
Noise Figure (f = 800–1000 MHz)	NF	—	8.0	9.5	dB
Load Mismatch (P_o = 5.0 W, f = 800 MHz, Load VSWR = ∞:1)	ψ	No Damage or Degradation in Performance			
Saturated Output Power (Single Tone) (f = 800–1000 MHz)	P_{sat}	7.0	8.0	—	W
Power Output (−30 dB IMD, Two Tone)	P_{out}	4.5	5.0	—	W
Second Harmonic Suppression (P_{out} = 5.0 W CW, f_{2h} = 1.6 GHz)	d_{so}	25	35	—	dB

$$ITO = P_0 + \frac{IMD}{2} @ IMD > 60\ dB$$

$$PEP = 4 \times P_0 @ IMD = -32\ dB$$

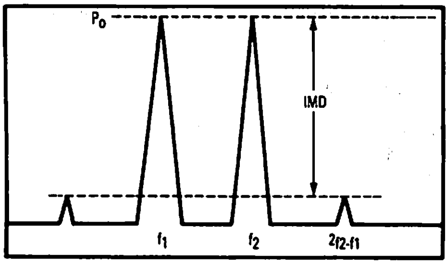


Figure 1. 2-Tone Intermodulation Test

SHP02-36-20

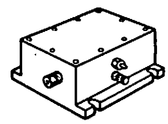
The RF Line

Linear Power Amplifier

. . . designed for wideband linear applications in the 1 to 200 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 28 volts.

- Specified V_{CC} = 28 Volt and T_C = 25°C Characteristics:
  - Frequency Range — 1 to 200 MHz
  - Output Power — 2 W Typ @ 1 dB Gain Compression, f = 100 MHz
  - Power Gain — 36 dB Typ @ f = 100 MHz
  - ITO — 51 dBm Typ @ f = 100 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability

**2 WATTS
1–200 MHz
LINEAR
POWER
AMPLIFIER**



SHP
CASE 389A-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	30	Vdc
RF Power Input	P_{in}	5	dBm
Storage Temperature Range	T_{stg}	−55 to +100	°C
Operating Temperature Range	T_C	−40 to +65	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 28 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 28 V)	I_{CC}	400	435	470	mA
Power Gain (f = 100 MHz)	G_P	34	36	37	dB
Bandwidth	BW	1	—	200	MHz
Gain Flatness (P-P) (f = 1–200 MHz)	—	—	1	2.5	dB
Input/Output VSWR (f = 1–200 MHz)	—	—	1.5:1	2:1	—
Output Power @ 1 dB Gain Compression (f = 100 MHz) (f = 200 MHz)	$P_{o\ 1dB}$	32 31	33 32	— —	dBm
Third Order Intercept Point (f = 100 MHz) (f = 200 MHz)	ITO	49 44	51 45	— —	dBm
Noise Figure (f = 100 MHz) (f = 200 MHz)	NF	— —	4.5 5.5	6 7	dB

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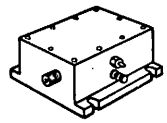
SHP05-20-10

The RF Line
Linear Power Amplifier

... *designed for wideband* linear applications in the 30 to 500 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified V_{CC} = 24 Volt and T_C = 25°C Characteristics:
  - Frequency Range — 30 to 500 MHz
  - Output Power — 1 W Typ @ 1 dB Gain Compression, f = 100 MHz
  - Power Gain — 20 dB Typ @ f = 50 MHz
  - ITO — 49 dBm Typ @ f = 300 MHz
  - Noise Figure — 6 dB Typ @ f = 500 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- Moisture Resistant, EMI Shielded Package

**1 WATT
30–500 MHz
LINEAR
POWER
AMPLIFIER**



SHP
CASE 389A-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	15	dBm
Storage Temperature Range	T_{stg}	−55 to +100	°C
Operating Temperature Range	T_C	−40 to +85	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 24 V)	I_{CC}	390	415	440	mA
Power Gain (f = 50 MHz)	G_P	19	20	21	dB
Bandwidth	BW	30	—	500	MHz
Gain Slope (f = 30–500 MHz)	S	0	0.6	1.6	dB
Gain Flatness (P-P around slope) (f = 30–500 MHz)	—	—	0.5	1	dB
Input/Output VSWR (f = 30–500 MHz)	—	—	1.2:1	1.5:1	—
Output Power @ 1 dB Gain Compression (f = 300 MHz) (f = 500 MHz)	$P_{o\ 1dB}$	31 28	33 30	— —	dBm
Third Order Intercept Point (f = 300 MHz) (f = 500 MHz)	ITO	47 40	49 42	— —	dBm
Noise Figure (f = 300 MHz) (f = 500 MHz)	NF	— —	4.5 6	5.5 7	dB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

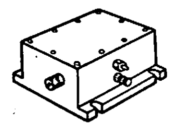
SHP05-22-04

The RF Line
Linear Power Amplifier

... designed for wideband linear applications in the 30–450 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified V_{CC} = 24 Volt and T_C = 25°C Characteristics:
  Frequency Range — 30 to 450 MHz
  Output Power — 1.2 W Typ @ 1 dB Gain Compression, f = 300 MHz
  Power Gain — 22 dB Typ @ f = 50 MHz
  ITO — 39 dBm Typ @ f = 450 MHz
  Noise Figure — 6 dB Typ @ f = 450 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- Moisture Resistant, EMI Shielded Package

1.2 WATT
30 TO 450 MHz
LINEAR
POWER
AMPLIFIER



SHP
CASE 389A-01, STYLE 1

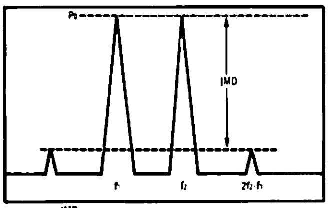
5

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+15	dBm
Operating Case Temperature Range	T_C	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	30	—	450	MHz
Gain Flatness (Peak-to-Peak) (f = 30–450 MHz)	—	—	0.5	1	dB
Power Gain (f = 50 MHz)	P_G	21.2	21.9	22.4	dB
Noise Figure, Broadband (f = 300 MHz) (f = 450 MHz)	NF	— —	5 6	6 7	dB
Power Output — 1 dB Compression (f = 300 MHz) (f = 450 MHz)	$P_{o\ 1dB}$	30 26	31 27	— —	dBm
Third Order Intercept (f = 300 MHz) (See Figure 1) (f = 450 MHz)	ITO	42 37	44 39	— —	dBm
Input/Output VSWR (f = 30–450 MHz)	VSWR	—	1.2:1	1.5:1	—
Supply Current	I_{CC}	175	220	250	mA
Gain Slope (f = 30–450 MHz)	S	0	1	2	dB



$ITO = P_o + \frac{IMD}{2}$ @ IMD > 60dB
PEP = 4X Po @ IMD = −32dB

Figure 1. Tone Intermodulation Test

SHP05-34-04

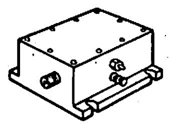
The RF Line

Linear Power Amplifier

. . . designed for wideband linear applications in the 30 to 450 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified V_{CC} = 24 Volt and T_C = 25°C Characteristics:
  Frequency Range — 30 to 450 MHz
  Output Power — 1 W Typ @ 1 dB Gain Compression, f = 300 MHz
  Power Gain — 34 dB Typ @ f = 50 MHz
  ITO — 38 dBm Typ @ f = 450 MHz
  Noise Figure — 6 dB Typ @ f = 450 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- Moisture Resistant, EMI Shielded Package

**1 WATT
30–450 MHz
LINEAR
POWER
AMPLIFIER**



SHP
CASE 389A-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	0	dBm
Storage Temperature Range	T_{stg}	−55 to +100	°C
Operating Temperature Range	T_C	−40 to +85	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 24 V)	I_{CC}	280	315	345	mA
Power Gain (f = 50 MHz)	G_P	33	34	35	dB
Bandwidth	BW	30	—	450	MHz
Gain Slope (f = 30–450 MHz)	S	0	1	2	dB
Gain Flatness (P-P around slope) (f = 30–450 MHz)	—	0	0.5	1	dB
Input/Output VSWR (f = 30–450 MHz)	—	—	1.2:1	1.5:1	—
Output Power @ 1 dB Gain Compression (f = 300 MHz) (f = 450 MHz)	$P_{o\ 1dB}$	28 24	30 26	— —	dBm
Third Order Intercept Point (f = 300 MHz) (f = 450 MHz)	ITO	42 36	45 38	— —	dBm
Noise Figure (f = 300 MHz) (f = 450 MHz)	NF	— —	5 6	6 7	dB

5

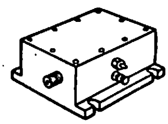
SHP06-18-04

The RF Line
Linear Power Amplifier

... designed for wideband linear applications in the 30–550 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified V_{CC} = 24 Volt and T_C = 25°C Characteristics:
  Frequency Range — 30 to 550 MHz
  Output Power — 1.2 W Typ @ 1 dB Gain Compression, f = 300 MHz
  Power Gain — 18 dB Typ @ f = 50 MHz
  ITO — 45 dBm Typ @ f = 300 MHz
  Noise Figure — 7.5 dB Typ @ f = 550 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- Moisture Resistant, EMI Shielded Package

**1.2 WATT
30 TO 550 MHz
LINEAR
POWER
AMPLIFIER**



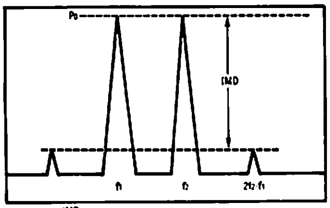
SHP
CASE 389A-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+15	dBm
Operating Case Temperature Range	T_C	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	30	—	550	MHz
Gain Flatness (Peak-to-Peak) (f = 30–550 MHz)	—	—	0.5	1	dB
Power Gain (f = 50 MHz)	P_G	17.5	18	18.5	dB
Noise Figure, Broadband (f = 300 MHz) (f = 550 MHz)	NF	— —	6 7.5	7 8.5	dB
Power Output — 1 dB Compression (f = 300 MHz) (f = 550 MHz)	$P_{o\ 1dB}$	29 26	31 28	— —	dBm
Third Order Intercept (f = 300 MHz) (See Figure 1) (f = 550 MHz)	ITO	43 38	45 40	— —	dBm
Input/Output VSWR (f = 30–550 MHz)	VSWR	—	1.2:1	1.5:1	—
Supply Current	I_{CC}	180	220	250	mA
Gain Slope (f = 30–550 MHz)	S	0	1	2	dB



$ITO = P_o + \frac{IMD}{2}$ @ IMD > 60dB
PEP = 4X Po @ IMD = −32dB

Figure 1. Tone Intermodulation Test

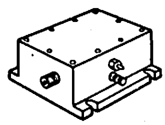
SHP10-15-08

The RF Line
Linear Power Amplifier

... designed for wideband linear applications in the 10 to 1000 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 28 volts.

- Specified V_{CC} = 28 Volt and T_C = 25°C Characteristics:
  Frequency Range — 10 to 1000 MHz
  Output Power — 0.8 W Typ @ 1 dB Gain Compression, f = 500 MHz
  Power Gain — 15 dB Typ @ f = 100 MHz
  ITO — 42 dBm Typ @ f = 1000 MHz
  Noise Figure — 8.5 dB Typ @ f = 1000 MHz
- *50 Ohm Input/Output Impedance*
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- Moisture Resistant, EMI Shielded Package

**0.8 WATT
10–1000 MHz
LINEAR
POWER
AMPLIFIER**



SHP
CASE 389A-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	32	Vdc
RF Power Input	P_{in}	20	dBm
Storage Temperature Range	T_{stg}	−55 to +100	°C
Operating Temperature Range	T_C	−40 to +85	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 28 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (V_{CC} = 28 V)	I_{CC}	360	400	440	mA
Power Gain (f = 100 MHz)	Gp	14	15	16	dB
Bandwidth	BW	10	—	1000	MHz
Gain Flatness (P-P) (f = 10–1000 MHz)	—	—	±0.5	±1	dB
Input/Output VSWR (f = 40–900 MHz) (f = 10–1000 MHz)	—	— —	— 2:1	2:1 2.5:1	—
Output Power @ 1 dB Gain Compression (f = 500 MHz) (f = 1000 MHz)	$P_{o\ 1dB}$	28 27	29 28	— —	dBm
Third Order Intercept Point (f = 500 MHz) (f = 1000 MHz)	ITO	41 40	43 42	— —	dBm
Noise Figure (f = 500 MHz) (f = 1000 MHz)	NF	— —	7.5 8.5	8.5 9.5	dB

5

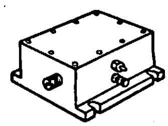
SHP10-15-08-15

The RF Line
Linear Power Amplifier

...designed for wideband linear applications in the 10–1000 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 15 volts.

- Specified V_{CC} = 15 Volt and T_C = 25°C Characteristics:
  Frequency Range — 10 to 1000 MHz
  Output Power — 800 mW Typ @ 1 dB Gain Compression, f = 500 MHz
  Power Gain — 15 dB Typ @ f = 100 MHz
  ITO — 43 dBm Typ @ f = 500 MHz
  Noise Figure — 8.5 dB Typ @ f = 1000 MHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- Moisture Resistant, EMI Shielded Package

**0.8 WATT
10 TO 1000 MHz
LINEAR
POWER
AMPLIFIER**



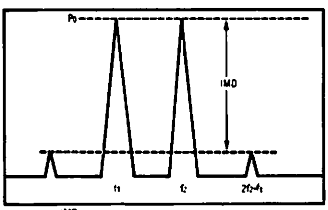
**SHP
CASE 389A-01, STYLE 1**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	18	Vdc
RF Power Input	P_{in}	+20	dBm
Operating Case Temperature Range	T_C	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 15 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	1000	MHz
Gain Flatness (Peak-to-Peak) (f = 10–1000 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	14	15	16	dB
Noise Figure, Broadband (f = 500 MHz) (f = 1000 MHz)	NF	— —	7.5 8.5	8.5 9.5	dB
Power Output — 1 dB Compression (f = 500 MHz) (f = 1000 MHz)	$P_{o\ 1dB}$	28 27	29 28	— —	dBm
Third Order Intercept (f = 500 MHz) (See Figure 1) (f = 1000 MHz)	ITO	41 40	43 42	— —	dBm
Input/Output VSWR (f = 40–900 MHz) (f = 10–1000 MHz)	VSWR	— —	— 2:1	2:1 2.5:1	—
Supply Current	I_{CC}	640	700	810	mA



$ITO = P_o + \frac{IMD}{2}$ @ IMD > 60dB
PEP = 4X Po @ IMD = −32dB

Figure 1. Tone Intermodulation Test

SHP10-17-04

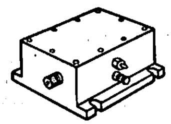
The RF Line

Linear Power Amplifier

... designed for wideband linear applications in the 10–1000 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 24 volts.

- Specified V_{CC} = 24 Volt and T_C = 25°C Characteristics:
  - Frequency Range — 10 to 1000 MHz
  - Output Power — 400 mW Typ @ 1 dB Gain Compression, f = 1 GHz
  - Power Gain — 17 dB Typ @ f = 100 MHz
  - ITO — 40 dBm Typ @ f = 500 MHz
  - Noise Figure — 7.5 dB Typ @ f = 1 GHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- Moisture Resistant, EMI Shielded Package

**0.4 WATT
10 TO 1000 MHz
LINEAR
POWER
AMPLIFIER**



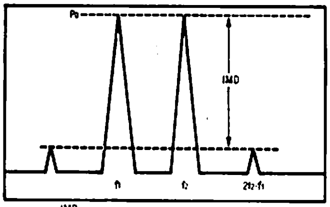
SHP
CASE 389A-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	28	Vdc
RF Power Input	P_{in}	+20	dBm
Operating Case Temperature Range	T_C	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +100	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 24 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	1000	MHz
Gain Flatness (Peak-to-Peak) (f = 10–1000 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	15.9	17	18.1	dB
Noise Figure, Broadband (f = 500 MHz) (f = 1000 MHz)	NF	— —	6.5 7.5	7.5 8.5	dB
Power Output — 1 dB Compression (f = 500 MHz) (f = 1000 MHz)	$P_{o\ 1dB}$	25 25	26 26	— —	dBm
Third Order Intercept (f = 500 MHz) (See Figure 1) (f = 1000 MHz)	ITO	38 37	40 39	— —	dBm
Input/Output VSWR (f = 40–900 MHz) (f = 10–1000 MHz)	VSWR	— —	— 2:1	2:1 2.5:1	—
Supply Current	I_{CC}	190	220	245	mA



$ITO = P_O + \frac{IMD}{2}$ @ IMD > 60dB
PEP = 4X P_O @ IMD = −32dB

Figure 1. Tone Intermodulation Test

SHP10-17-04-15

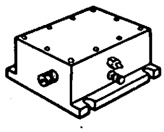
The RF Line

Linear Power Amplifier

. . . designed for wideband linear applications in the 10–1000 MHz frequency range. This solid state, Class A amplifier incorporates microstrip circuit technology and high performance, gold metallized transistors to provide a complete broadband, linear amplifier operating from a supply voltage of 15 volts.

- Specified V_{CC} = 15 Volt and T_C = 25°C Characteristics:
  Frequency Range — 10 to 1000 MHz
  Output Power — 400 mW Typ @ 1 dB Gain Compression, f = 1 GHz
  Power Gain — 17 dB Typ @ f = 100 MHz
  ITO — 40 dBm Typ @ f = 500 MHz
  Noise Figure — 7.5 dB Typ @ f = 1 GHz
- 50 Ohm Input/Output Impedance
- Heavy Duty Machined Housing
- Gold Metallized Transistors for Improved Reliability
- Moisture Resistant, EMI Shielded Package

**0.4 WATT
10 TO 1000 MHz
LINEAR
POWER
AMPLIFIER**



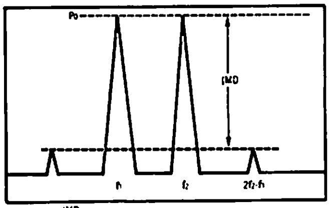
SHP
CASE 389A-01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	18	Vdc
RF Power Input	P_{in}	+20	dBm
Operating Case Temperature Range	T_C	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +100	°C

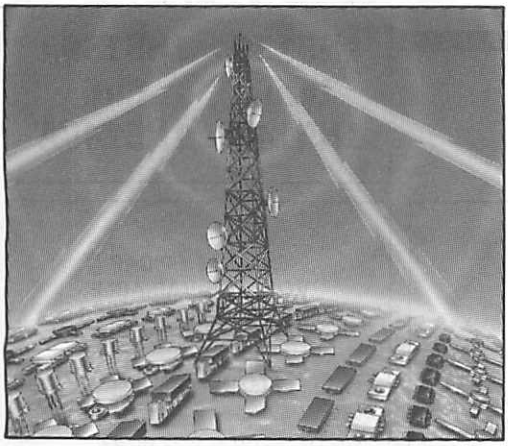
ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{CC} = 15 V, 50 Ω system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	10	—	1000	MHz
Gain Flatness (Peak-to-Peak) (f = 10–1000 MHz)	—	—	±0.5	±1	dB
Power Gain (f = 100 MHz)	P_G	15.9	17	18.1	dB
Noise Figure, Broadband (f = 500 MHz) (f = 1000 MHz)	NF	— —	6.5 7.5	7.5 8.5	dB
Power Output — 1 dB Compression (f = 500 MHz) (f = 1000 MHz)	$P_{o\ 1dB}$	25 25	26 26	— —	dBm
Third Order Intercept (f = 500 MHz) (See Figure 1) (f = 1000 MHz)	ITO	38 37	40 39	— —	dBm
Input/Output VSWR (f = 40–900 MHz) (f = 10–1000 MHz)	VSWR	— —	— 2:1	2:1 2.5:1	—
Supply Current	I_{CC}	340	400	420	mA



$ITO = P_o + \frac{IMD}{2}$ @ IMD > 60dB
PEP = 4X Po @ IMD = −32dB

Figure 1. Tone Intermodulation Test



Volume II

Tuning, Hot Carrier and PIN Diode Data Sheets

6

1N5139 thru 1N5148 / 1N5139A thru 1N5148A

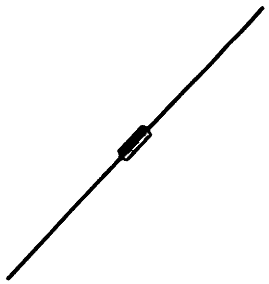
6.8-47 pF EPICAP VOLTAGE-VARIABLE CAPACITANCE DIODES

SILICON EPITAXIAL PASSIVATED

SILICON EPICAP DIODES

. . . designed for electronic tuning and harmonic-generation applications, and providing solid-state reliability to replace mechanical tuning methods.

- Guaranteed High-Frequency Q
- Guaranteed Wide Tuning Range
- Guaranteed Temperature Coefficient
- Standard 10% Capacitance Tolerance
- Complete Typical Design Curves

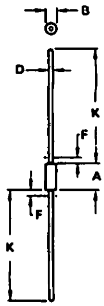


MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	60	Volts
Forward Current	I_F	250	mA
RF Power Input†	P_{in}	5	Watts
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Device Dissipation @ T_C = 25°C Derate above 25°C	P_C	2.0 13.3	Watts mW/°C
Junction Temperature	T_J	+175	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

†The RF power input rating assumes that an adequate heat sink is provided.

NOTES:
1. PACKAGE CONTOUR OPTIONAL WITHIN DIA B AND LENGTH A. HEAT SLUGS, IF ANY, SHALL BE INCLUDED WITHIN THIS CYLINDER, BUT SHALL NOT BE SUBJECT TO THE MIN LIMIT OF DIA B.
2. LEAD DIA NOT CONTROLLED IN ZONES F, TO ALLOW FOR FLASH, LEAD FINISH BUILDUP, AND MINOR IRREGULARITIES OTHER THAN HEAT SLUGS.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	38.10	1.000	1.500

All JEDEC dimensions and notes apply

CASE 51-02
DO-204AA

6

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic — All Types	Test Conditions	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 10 μAdc	BV_R	60	70	—	Vdc
Reverse Voltage Leakage Current	V_R = 55 Vdc, T_A = 25°C V_R = 55 Vdc, T_A = 150°C	I_R	— —	— —	0.02 20	μAdc
Series Inductance	f = 250 MHz, L ≈ 1/16"	L_S	—	4	—	nH
Case Capacitance	f = 1 MHz, L ≈ 1/16"	C_C	—	0.17	—	pF
Diode Capacitance Temperature Coefficient	V_R = 4 Vdc, f = 1 MHz	TC_C	—	200	—	ppm/°C

	C_T, Diode Capacitance V_R = 4 Vdc, f = 1 MHz pF			Q, Figure of Merit V_R = 4 Vdc, f = 50 MHz	α V_R = 4 Vdc, f = 1 MHz		TR, Tuning Ratio C_4/C_{60} f = 1 MHz	
Device	Min	Typ	Max	Min	Min	Typ	Min	Typ
1N5139	6.1	6.8	7.5	350	0.37	0.40	2.7	2.9
1N5139A	6.5	6.8	7.1	350	0.37	0.40	2.7	2.9
1N5140	9.0	10.0	11.0	300	0.38	0.41	2.8	3.0
1N5140A	9.5	10.0	10.5	300	0.38	0.41	2.8	3.0
1N5141	10.8	12.0	13.2	300	0.38	0.41	2.8	3.0
1N5141A	11.4	12.0	12.6	300	0.38	0.41	2.8	3.0
1N5142	13.5	15.0	16.5	250	0.38	0.41	2.8	3.0
1N5142A	14.3	15.0	15.7	250	0.38	0.41	2.8	3.0
1N5143	16.2	18.0	19.8	250	0.38	0.41	2.8	3.0
1N5143A	17.1	18.0	18.9	250	0.38	0.41	2.8	3.0
1N5144	19.8	22.0	24.2	200	0.43	0.45	3.2	3.4
1N5144A	20.9	22.0	23.1	200	0.43	0.45	3.2	3.4
1N5145	24.3	27.0	29.7	200	0.43	0.45	3.2	3.4
1N5145A	25.7	27.0	28.3	200	0.43	0.45	3.2	3.4
1N5146	29.7	33.0	36.3	200	0.43	0.45	3.2	3.4
1N5146A	31.4	33.0	34.6	200	0.43	0.45	3.2	3.4
1N5147	36.1	39.0	42.9	200	0.43	0.45	3.2	3.4
1N5147A	37.1	39.0	40.9	200	0.43	0.45	3.2	3.4
1N5148	42.3	47.0	51.7	200	0.43	0.45	3.2	3.4
1N5148A	44.7	47.0	49.3	200	0.43	0.45	3.2	3.4

PARAMETER TEST METHODS

1. L_S, SERIES INDUCTANCE

L_S is measured on a shorted package at 250 MHz using an impedance bridge (Boonton Radio Model 250A RX Meter). L = lead length.

2. C_C, CASE CAPACITANCE

C_C is measured on an open package at 1 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

3. C_T, DIODE CAPACITANCE

($C_T = C_C + C_J$). C_T is measured at 1 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

4. TR, TUNING RATIO

TR is the ratio of C_T measured at 4 Vdc divided by C_T measured at 60 Vdc.

5. Q, FIGURE OF MERIT

Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equations:

$$Q = \frac{2\pi fC}{G}$$

(Boonton Electronics Model 33AS8).

6. α, DIODE CAPACITANCE REVERSE VOLTAGE SLOPE

The diode capacitance, C_T (as measured at V_R = 4 Vdc, f = 1 MHz) is compared to C_T (as measured at V_R = 60 Vdc, f = 1 MHz) by the following equation which defines α.

$$\alpha = \frac{\log C_T(4) - \log C_T(60)}{\log 60 - \log 4}$$

Note that a C_T versus V_R law is assumed as shown in the following equation where C_C is included.

$$C_T = \frac{K}{V^{\alpha}}$$

7. TC_C, DIODE CAPACITANCE TEMPERATURE COEFFICIENT

TC_C is guaranteed by comparing C_T at V_R = 4 Vdc, f = 1 MHz, T_A = −65°C with C_T at V_R = 4 Vdc, f = 1 MHz, T_A = +85°C in the following equation which defines TC_C:

$$TC_C = \left| \frac{C_T(+85°C) - C_T(-65°C)}{85 + 65} \right| \cdot \frac{10^6}{C_T(25°C)}$$

6

FIGURE 1 — DIODE CAPACITANCE versus REVERSE VOLTAGE

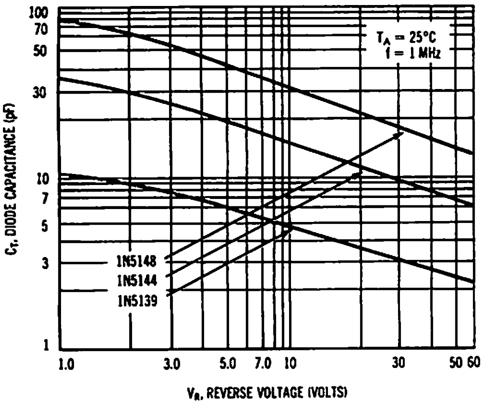


FIGURE 2 — FIGURE OF MERIT versus REVERSE VOLTAGE

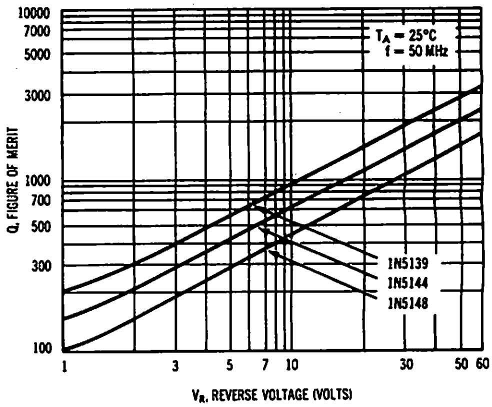


FIGURE 3 — NORMALIZED DIODE CAPACITANCE versus JUNCTION TEMPERATURE

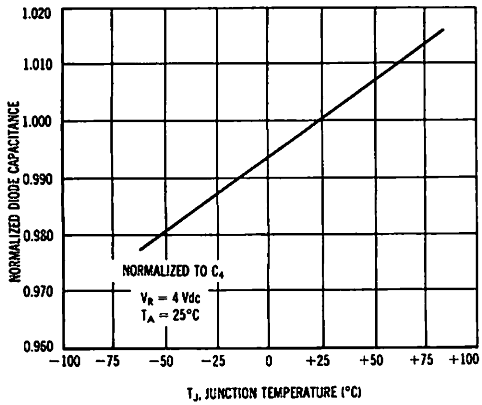


FIGURE 4 — NORMALIZED FIGURE OF MERIT versus JUNCTION TEMPERATURE

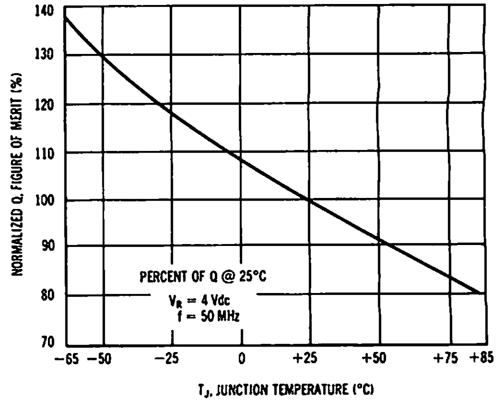


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FIGURE 5 — REVERSE CURRENT versus REVERSE BIAS VOLTAGE

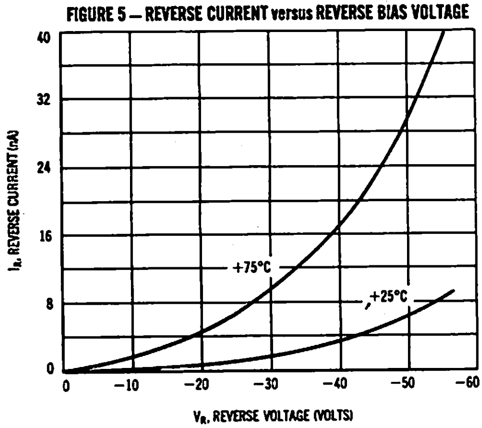
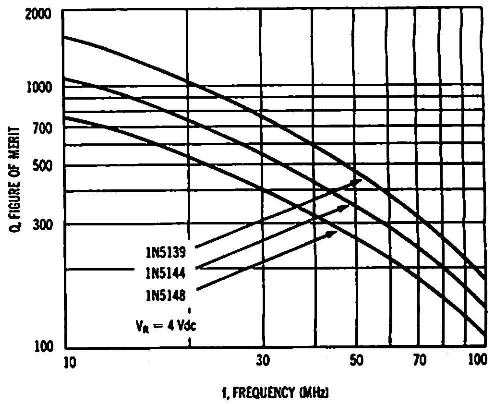


FIGURE 6 — FIGURE OF MERIT versus FREQUENCY



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

1N5441A,B thru 1N5456A,B

VVC

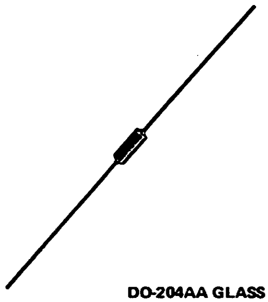
VOLTAGE-VARIABLE CAPACITANCE DIODES

6.8 – 100 pF
30 VOLTS

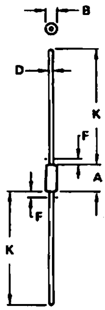
SILICON EPICAP DIODES

. . . epitaxial passivated abrupt junction tuning diodes designed for electronic tuning, FM, AFC and harmonic-generation applications in AM through UHF ranges, providing solid-state reliability to replace mechanical tuning methods.

- Excellent Q Factor at High Frequencies
- Guaranteed Capacitance Change — 2.0 to 30 V
- Guaranteed Temperature Coefficient
- Capacitance Tolerance — 10% and 5.0%
- Complete Typical Design Curves



DO-204AA GLASS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	38.10	1.000	1.500

All JEDEC dimensions and notes apply

CASE 51-02
DO-204AA

*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Operating Junction Temperature Range	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

6

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic — All Types	Test Conditions	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 10 μAdc	$V_{(BR)R}$	30	—	—	Vdc
Reverse Voltage Leakage Current	V_R = 25 Vdc, T_A = 25°C V_R = 25 Vdc, T_A = 150°C	I_R	— —	— —	0.02 20	μAdc
Series Inductance	f = 250 MHz, lead length ≈ 1/16"	L_S	—	4.0	—	nH
Case Capacitance	f = 1.0 MHz, lead length ≈ 1/16"	C_C	—	0.17	—	pF
Diode Capacitance Temperature Coefficient (Note 6)	V_R = 4.0 Vdc, f = 1.0 MHz	TC_c	—	300	—	ppm/°C

Device	C_T, Diode Capacitance (1) V_R = 4.0 Vdc, f = 1.0 MHz pF			TR, Tuning Ratio C_2/C_{30} f = 1.0 MHz		Q, Figure of Merit V_R = 4.0 Vdc f = 50 MHz
	Min (Nom −10%)	Nom	Max (Nom +10%)	Min	Max	Min
1N5441A	6.1	6.8	7.5	2.5	3.2	450
1N5443A	9.0	10.0	11.0	2.6	3.2	400
1N5444A	10.8	12.0	13.2	2.6	3.2	400
1N5445A	13.5	15.0	16.5	2.6	3.2	400
1N5446A	16.2	18.0	19.8	2.6	3.2	350
1N5448A	19.8	22.0	24.2	2.6	3.2	350
1N5449A	24.3	27.0	29.7	2.6	3.2	350
1N5450A	29.7	33.0	36.3	2.6	3.2	350
1N5451A	35.1	39.0	42.9	2.6	3.2	300
1N5452A	42.3	47.0	51.7	2.6	3.2	250
1N5453A	50.4	56.0	61.6	2.6	3.3	200
1N5455A	73.8	82.0	90.2	2.7	3.3	175
1N5456A	90.0	100.0	110.0	2.7	3.3	175

(1) To order devices with C_T Nom ±5.0% add Suffix B.
*Indicates JEDEC Registered Data.

PARAMETER TEST METHODS

1. **L_S, Series Inductance**
   L_S is measured on a shorted package at 250 MHz using an impedance bridge (Boonton Radio Model 250A RX Meter or equivalent).
2. **C_C, Case Capacitance**
   C_C is measured on an open package at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
3. **C_T, Diode Capacitance**
   (C_T = C_C + C_J). C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
4. **TR, Tuning Ratio**
   TR is the ratio of C_T measured at 2.0 Vdc divided by C_T measured at 30 Vdc.
5. **Q, Figure of Merit**
   Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equations:

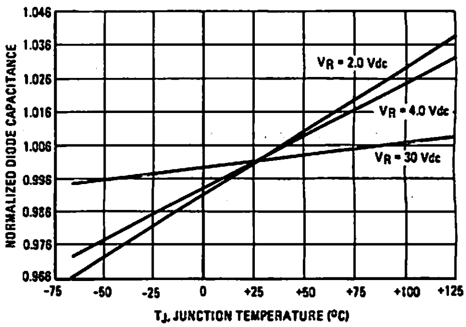
$$Q = \frac{2\pi fC}{G}$$

   (Boonton Electronics Model 33AS8 or equivalent).
6. **TC_c, Diode Capacitance Temperature Coefficient**
   TC_c is guaranteed by comparing C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = -65°C with C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = +85°C in the following equation, which defines TC_c:

$$TC_c = \left|\frac{C_T(+85^\circ C) - C_T(-65^\circ C)}{85 + 65}\right| \frac{10^6}{C_T(25^\circ C)}$$

   Accuracy limited by C_T measurement to ±0.1 pF.

FIGURE 1 — NORMALIZED DIODE CAPACITANCE versus JUNCTION TEMPERATURE



6

TYPICAL DEVICE PERFORMANCE

FIGURE 2 – DIODE CAPACITANCE versus REVERSE VOLTAGE

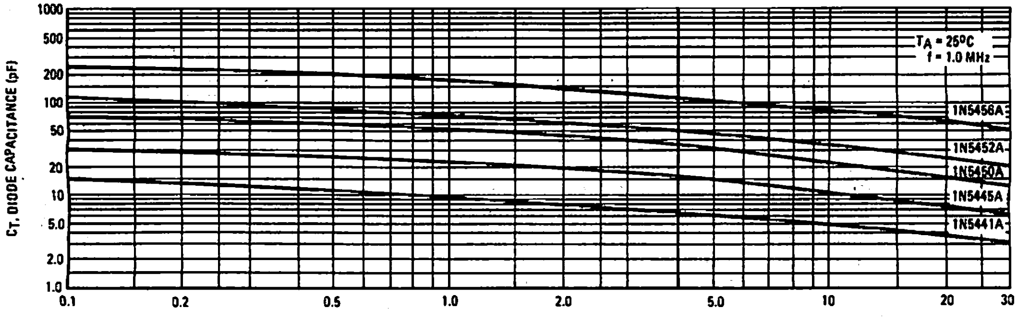


FIGURE 3 – FIGURE OF MERIT versus REVERSE VOLTAGE

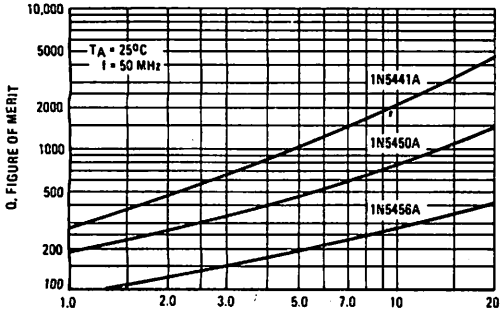


FIGURE 4 – FIGURE OF MERIT versus FREQUENCY

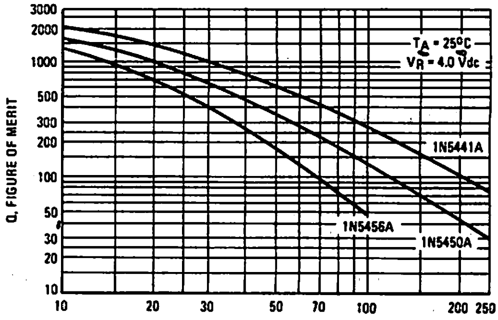


FIGURE 5 – REVERSE CURRENT versus REVERSE BIAS VOLTAGE

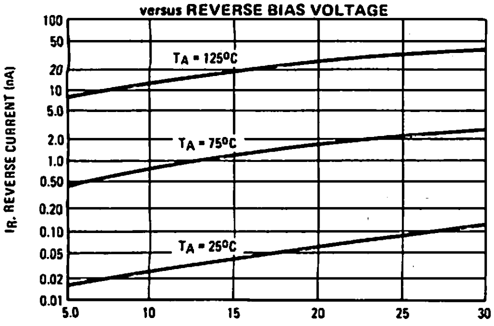
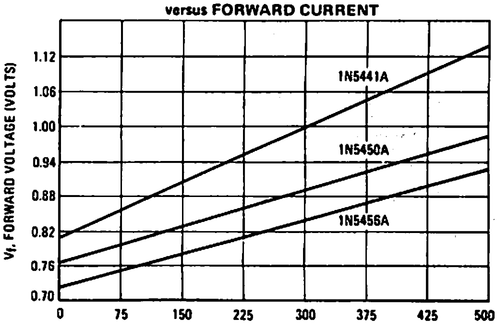


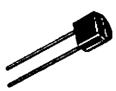
FIGURE 6 – FORWARD VOLTAGE versus FORWARD CURRENT



6

MBD101
MMBD101L

SILICON HOT-CARRIER UHF MIXER DIODES



CASE 182-02
TO-226AC
MBD101

CASE 318-07
TO-236AB
SOT-23
MMBD101L

SILICON HOT-CARRIER DIODES (SCHOTTKY BARRIER DIODES)

. . . designed primarily for UHF mixer applications but suitable also for use in detector and ultra-fast switching circuits. Supplied in an inexpensive plastic package for low-cost, high-volume consumer requirements. Also available in Surface Mount package.

- The Rugged Schottky Barrier Construction Provides Stable Characteristics by Eliminating the "Cat-Whisker" Contact
- Low Noise Figure — 6.0 dB Typ @ 1.0 GHz
- Very Low Capacitance — Less Than 1.0 pF @ Zero Volts
- High Forward Conductance — 0.50 Volts (Typ) @ I_F = 10 mA

MAXIMUM RATINGS

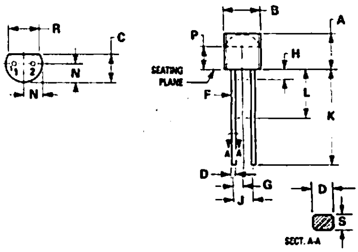
Rating	Symbol	MBD101 Value	MMBD101L Value	Unit
Reverse Voltage	V_R	4.0		Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	280 2.8	200 2.0	mW mW/°C
Junction Temperature	T_J	+125		°C
Storage Temperature Range	T_{stg}	−55 to +150		°C

DEVICE MARKING

MMBD101 = 4M

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

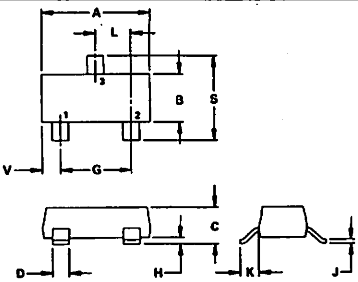
Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	4.0	5.0	–	Volts
Diode Capacitance (V_R = 0, f = 1.0 MHz, Note 1)	C_T	–	0.88	1.0	pF
Forward Voltage (1) (I_F = 10 mA)	V_F	–	0.50	0.60	Volts
Noise Figure (f = 1.0 GHz, Note 2)	NF	–	6.0	—	dB
Reverse Leakage (V_R = 3.0 V)	I_R	–	0.02	0.25	μA



STYLE 1:
PIN 1. ANODE
2. CATHODE

CASE 182-02
TO-226AC

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016



STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

CASE 318-07
TO-236AB
SOT-23

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.0350	0.0440
D	0.37	0.50	0.0150	0.0200
G	1.78	2.04	0.0701	0.0807
H	0.013	0.100	0.0005	0.0040
J	0.085	0.177	0.0034	0.0070
K	0.45	0.60	0.0180	0.0236
L	0.89	1.02	0.0350	0.0401
S	2.10	2.50	0.0830	0.0984
V	0.45	0.60	0.0177	0.0236

6

TYPICAL CHARACTERISTICS
(T_A = 25°C unless noted)

FIGURE 1 – REVERSE LEAKAGE

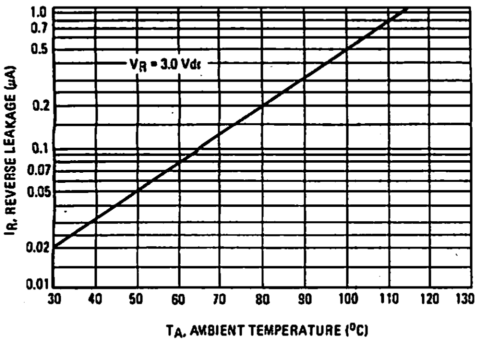


FIGURE 2 – FORWARD VOLTAGE

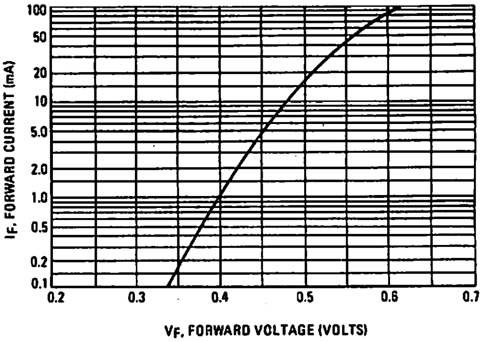


FIGURE 3 – CAPACITANCE

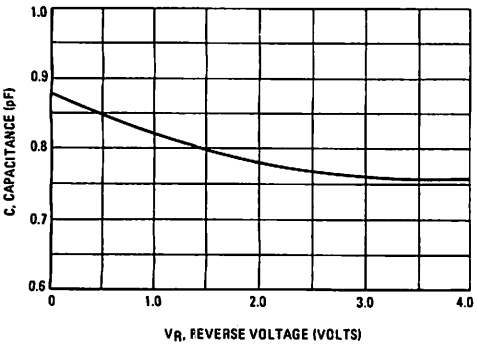


FIGURE 4 – NOISE FIGURE

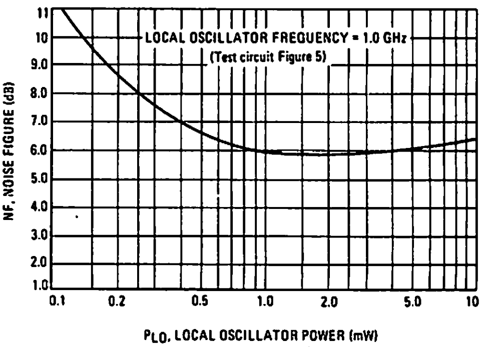
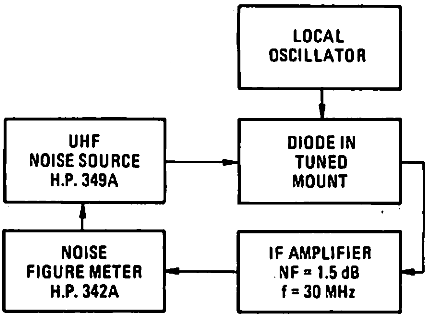


FIGURE 5 – NOISE FIGURE TEST CIRCUIT



NOTES ON TESTING AND SPECIFICATIONS

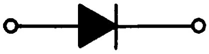
Note 1 – C_C and C_T are measured using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

Note 2 – Noise figure measured with diode under test in tuned diode mount using UHF noise source and local oscillator (LO) frequency of 1.0 GHz. The LO power is adjusted for 1.0 mW. IF amplifier NF = 1.5 dB, f = 30 MHz, see Figure 5.

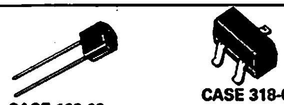
Note 3 – L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).

6

MBD301
MMBD301L



SILICON HOT-CARRIER DETECTOR AND SWITCHING DIODES
30 VOLTS



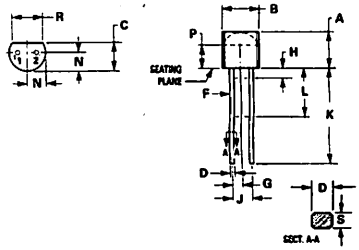
CASE 182-02
TO-226AC
MBD301

CASE 318-07
TO-236AB
SOT-23
MMBD301L

SILICON HOT-CARRIER DIODES (SCHOTTKY BARRIER DIODES)

. . . designed primarily for high-efficiency UHF and VHF detector applications. Readily adaptable to many other fast switching RF and digital applications. Supplied in an inexpensive plastic package for low-cost, high-volume consumer and industrial/commercial requirements. Also available in Surface Mount package.

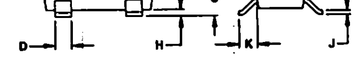
- The Schottky Barrier Construction Provides Ultra-Stable Characteristics By Eliminating the "Cat-Whisker" or "S-Bend" Contact
- Extremely Low Minority Carrier Lifetime — 15 ps (Typ)
- Very Low Capacitance — 1.5 pF (Max) @ V_R = 15 V
- Low Reverse Leakage — I_R = 13 nAdc (Typ) MBD301, MMBD301L



STYLE 1:
PIN 1. ANODE
2. CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	—	1.27	—	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

CASE 182-02
TO-226AC



STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.0350	0.0440
D	0.37	0.50	0.0150	0.0200
G	1.78	2.04	0.0701	0.0807
H	0.013	0.100	0.0005	0.0040
J	0.085	0.177	0.0034	0.0070
K	0.45	0.60	0.0180	0.0236
L	0.89	1.02	0.0350	0.0401
S	2.10	2.50	0.0830	0.0984
V	0.45	0.60	0.0177	0.0236

CASE 318-07
TO-236AB
SOT-23

MAXIMUM RATINGS (T_J = 125°C unless otherwise noted)

Rating	Symbol	Value MBD301	Value MMBD301L	Unit
Reverse Voltage MBD301, MMBD301L	V_R	30		Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	280 2.8	200 2.0	mW mW/°C
Operating Junction Temperature Range	T_J	−55 to +125		°C
Storage Temperature Range	T_{stg}	−55 to +150		°C

DEVICE MARKING

MMBD301L = 4T

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc) MBD301, MMBD301L	$V_{(BR)R}$	30	—	—	Volts
Total Capacitance, Figure 1 (V_R = 15 Volts, f = 1.0 MHz)	C_T	—	0.9	1.5	pF
Minority Carrier Lifetime, Figure 2 (I_F = 5.0 mA, Krakauer Method)	τ	—	15	—	ps
Reverse Leakage, Figure 3 (V_R = 25 V) MBD301, MMBD301L	I_R	—	13	200	nAdc
Forward Voltage, Figure 4 (I_F = 10 mAdc)	V_F	—	0.5	0.6	Vdc

6

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – TOTAL CAPACITANCE

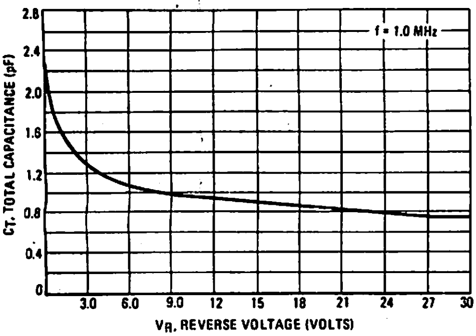


FIGURE 2 – MINORITY CARRIER LIFETIME

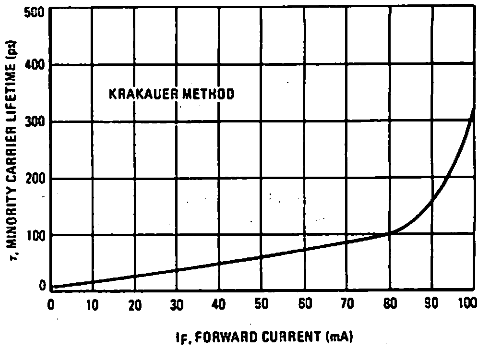


FIGURE 3 – REVERSE LEAKAGE

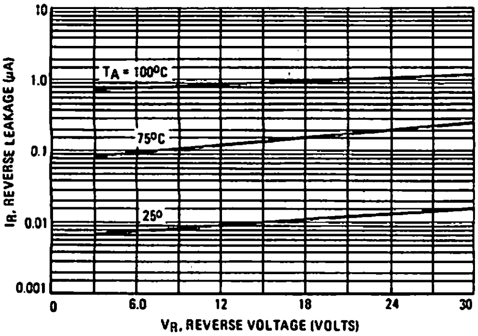
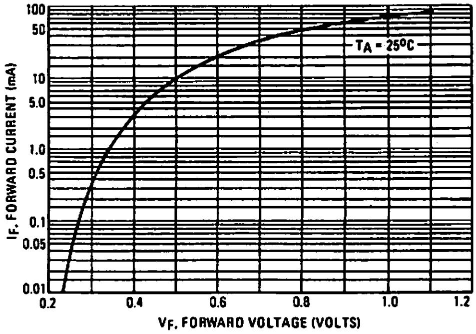
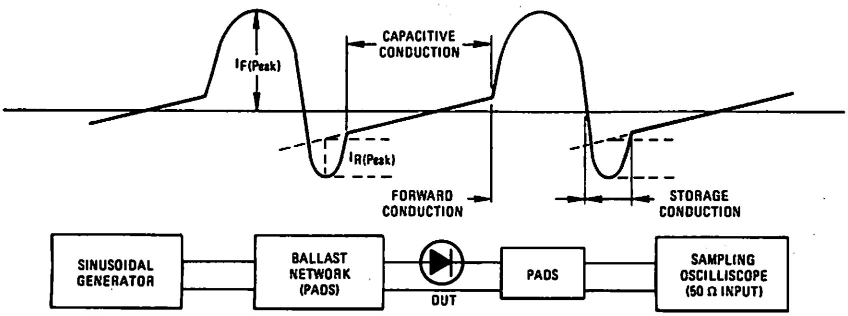


FIGURE 4 – FORWARD VOLTAGE



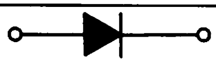
KRAKAUER METHOD OF MEASURING LIFE TIME



6

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MBD701
MMBD701L

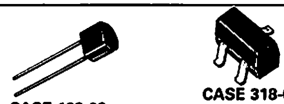


SILICON HOT-CARRIER DIODES (SCHOTTKY BARRIER DIODES)

. . . designed primarily for high-efficiency UHF and VHF detector applications. Readily adaptable to many other fast switching RF and digital applications. Supplied in an inexpensive plastic package for low-cost, high-volume consumer and industrial/commercial requirements. Also available in Surface Mount package.

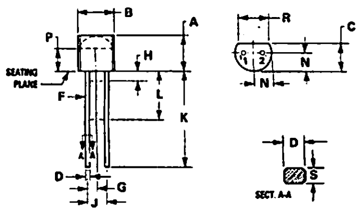
- The Schottky Barrier Construction Provides Ultra-Stable Characteristics by Eliminating the "Cat-Whisker" or "S-Bend" Contact
- Extremely Low Minority Carrier Lifetime — 15 ps (Typ)
- Very Low Capacitance — 1.0 pF @ V_R = 20 V
- High Reverse Voltage — to 70 Volts
- Low Reverse Leakage — 200 nA (Max)

HIGH-VOLTAGE SILICON HOT-CARRIER DETECTOR AND SWITCHING DIODES
70 VOLTS



CASE 182-02
TO-226AC
MBD701

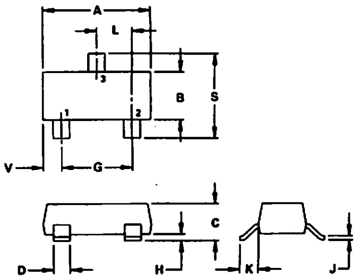
CASE 318-07
TO-236AB
SOT-23
MMBD701L



STYLE 1:
PIN 1. ANODE
2. CATHODE

CASE 182-02
TO-226AC

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	—	1.27	—	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016



STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

CASE 318-07
TO-236AB
SOT-23

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.0350	0.0440
D	0.37	0.50	0.0150	0.0200
G	1.78	2.04	0.0701	0.0807
H	0.013	0.100	0.0005	0.0040
J	0.085	0.177	0.0034	0.0070
K	0.45	0.60	0.0180	0.0236
L	0.89	1.02	0.0350	0.0401
S	2.10	2.50	0.0830	0.0984
V	0.45	0.60	0.0177	0.0236

6

MAXIMUM RATINGS (T_J = 125°C unless otherwise noted)

Rating	Symbol	Value MBD701	Value MMBD701L	Unit
Reverse Voltage MBD701, MMBD701L	V_R	70		Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	280 2.8	200 2.0	mW mW/°C
Operating Junction Temperature Range	T_J	−55 to +125		°C
Storage Temperature Range	T_{stg}	−55 to +150		°C

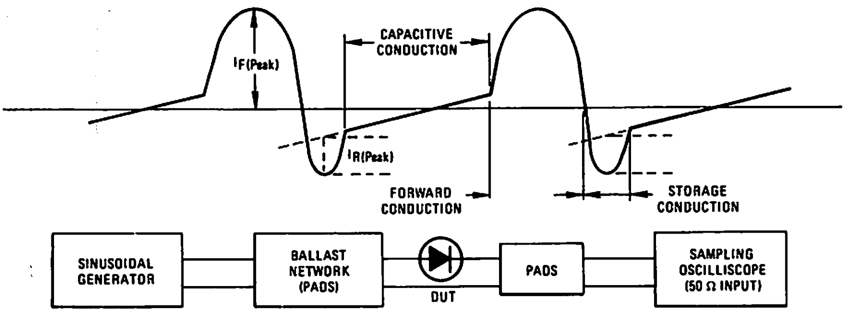
DEVICE MARKING

MMBD701L = 5H

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc) MBD701, MMBD701L	$V_{(BR)R}$	70	—	—	Volts
Total Capacitance, Figure 1 (V_R = 20 Volts, f = 1.0 MHz)	C_T	—	0.5	1.0	pF
Minority Carrier Lifetime, Figure 2 (I_F = 5.0 mA, Krakauer Method)	τ	—	15	—	ps
Reverse Leakage, Figure 3 (V_R = 35 V) MBD701, MMBD701L	I_R	—	9.0	200	nAdc
Forward Voltage, Figure 4 (I_F = 10 mAdc)	V_F	—	1.0	1.2	Vdc

KRAKAUER METHOD OF MEASURING LIFE TIME



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – TOTAL CAPACITANCE

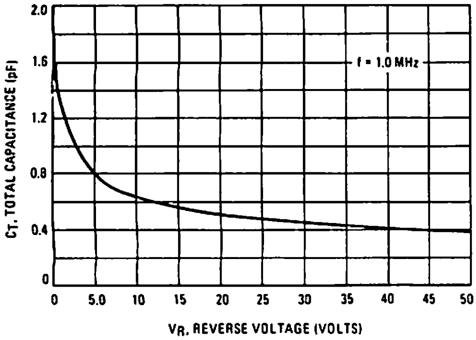


FIGURE 2 – MINORITY CARRIER LIFETIME

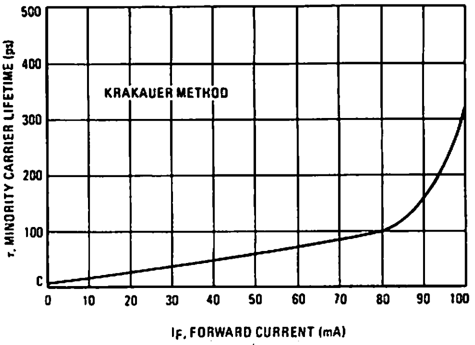


FIGURE 3 – REVERSE LEAKAGE

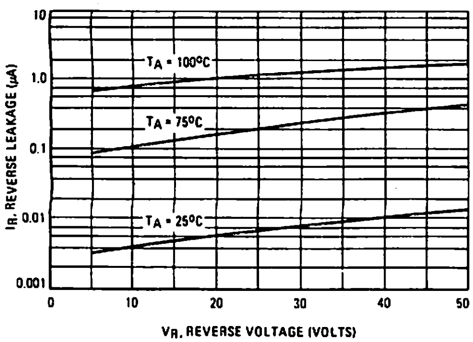
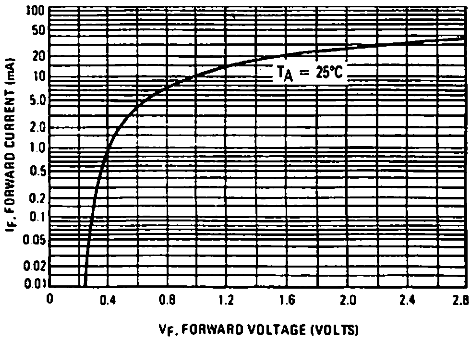


FIGURE 4 – FORWARD VOLTAGE



6

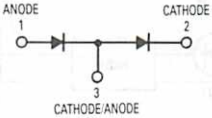
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Dual Hot Carrier Mixer Diodes

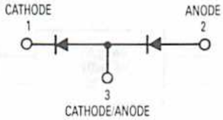
MMBD352L
MMBD353L

DUAL HOT CARRIER MIXER DIODES

MMBD352L (STYLE 11)



MMBD353L (STYLE 9)



CASE 318-07
SOT-23
(TO-236AB)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Continuous Reverse Voltage	V_R	4.0	V_{CC}

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board,* $T_A = 25°C$	P_D	225	mW
Derate above 25°C		1.8	mW/°C
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate,** $T_A = 25°C$	P_D	300	mW
Derate above 25°C		2.4	mW/°C
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

*FR-5 = 1.0 x 0.75 x 0.062 in.
**Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina.

DEVICE MARKING

MMBD352L = M5G; MMBD353L = M4F

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Forward Voltage (I_F = 10 mA)	V_F	—	0.6	V
Reverse Voltage Leakage Current	I_R			μA
(V_R = 3 V)		—	0.25	
(V_R = 4 V)		—	10	
Capacitance (V_R = 0 V, f = 1 MHz)	C	—	1	pF

6

MMBV105GL

VVC

VOLTAGE VARIABLE CAPACITANCE DIODE

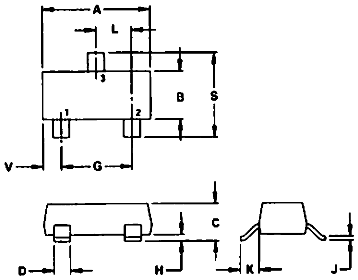
30 VOLTS

CASE 318-07
TO-236AB

SILICON EPICAP DIODE

. . . designed in the Surface Mount package for general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

- Controlled and Uniform Tuning Ratio



STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.0350	0.0440
D	0.37	0.50	0.0150	0.0200
G	1.78	2.04	0.0701	0.0807
H	0.013	0.100	0.0005	0.0040
J	0.085	0.177	0.0034	0.0070
K	0.45	0.60	0.0180	0.0236
L	0.89	1.02	0.0350	0.0401
S	2.10	2.50	0.0830	0.0984
V	0.45	0.60	0.0177	0.0236

CASE 318-07
TO-236AB
SOT-23

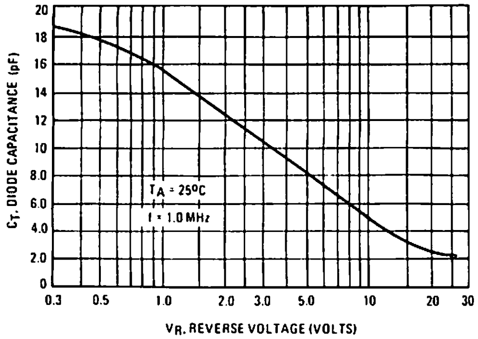
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Forward Current	I_F	200	mA
Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	200 2.0	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

DEVICE MARKING

MMBV105GL = M4E

FIGURE 1 – DIODE CAPACITANCE



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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic-All Types	Symbol	Min	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	30	–	Vdc
Reverse Voltage Leakage Current (VR = 28 V)	I_R	–	50.0	nAdc

Device Type	C_T V_R = 25 Vdc pF		Q f = 100 MHz V_R = 3.0V	C_3/C_{25}	
	Min	Max	Typ	Min	Max
MMBV105GL	1.8	2.8	150	4.0	6

FIGURE 2 – FIGURE OF MERIT

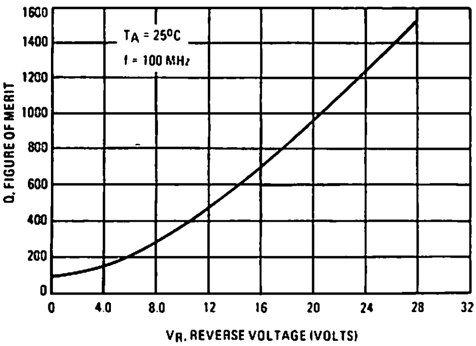
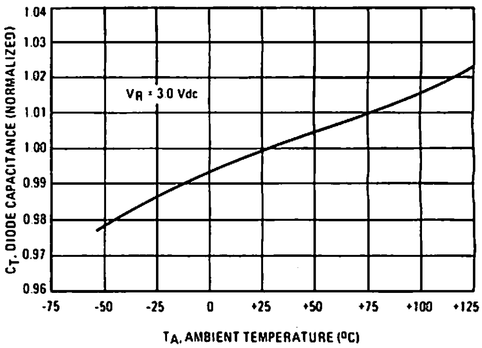


FIGURE 3 – DIODE CAPACITANCE



6

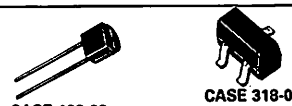
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MMBV109L
MV209

VVC

VOLTAGE VARIABLE CAPACITANCE DIODES

26–32 pF



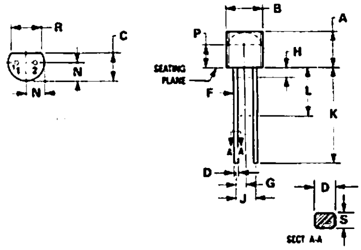
CASE 182-02
TO-226AC
MV209

CASE 318-07
TO-236AB
SOT-23
MMBV109L

SILICON EPICAP DIODES

. . . designed for general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

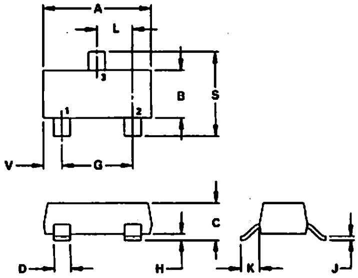
- High Q with Guaranteed Minimum Values at VHF Frequencies
- Controlled and Uniform Tuning Ratio
- Available in Surface Mount Package



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	—	1.27	—	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

STYLE 1:
PIN 1. ANODE
2. CATHODE

CASE 182-02
TO-226AC



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.0350	0.0440
D	0.37	0.50	0.0150	0.0200
G	1.78	2.04	0.0701	0.0807
H	0.013	0.100	0.0005	0.0040
J	0.085	0.177	0.0034	0.0070
K	0.45	0.60	0.0180	0.0236
L	0.89	1.02	0.0350	0.0401
S	2.10	2.50	0.0830	0.0984
V	0.45	0.60	0.0177	0.0236

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

CASE 318-07
TO-236AB
SOT-23

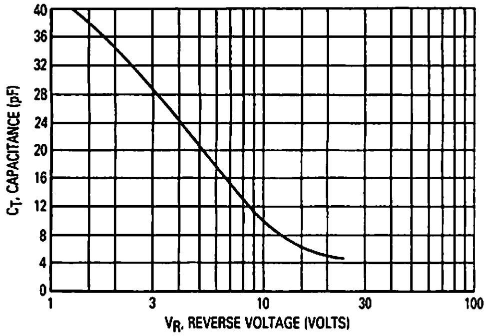
MAXIMUM RATINGS

Rating	Symbol	Value MV209	Value MMBV109L	Unit
Reverse Voltage	V_R	30		Volts
Forward Current	I_F	200		mA
Forward Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	280 2.8	200 2.0	mW mW/°C
Junction Temperature	T_J	+125		°C
Storage Temperature Range	T_{stg}	−55 to +150		°C

DEVICE MARKING

MMBV109L = M4A

FIGURE 1 — DIODE CAPACITANCE



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic — All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	30	—	—	Vdc
Reverse Voltage Leakage Current (V_R = 25 Vdc)	I_R	—	—	0.1	μAdc
Diode Capacitance Temperature Coefficient (V_R = 3.0 Vdc, f = 1.0 MHz)	TC_C	—	300	—	ppm/°C

Device	C_t, Diode Capacitance V_R = 3.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 3.0 Vdc f = 50 MHz (Note 1)	C_R, Capacitance Ratio C_3/C_{25} f = 1.0 MHz (Note 2)	
	Min	Nom	Max	Min	Min	Max
MMBV109L, MV209	26	29	32	200	5.0	6.5

FIGURE 2 — FIGURE OF MERIT

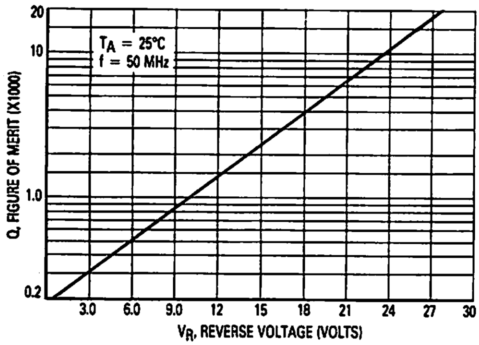


FIGURE 3 — LEAKAGE CURRENT

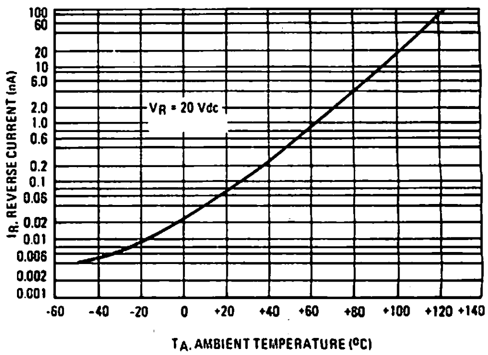
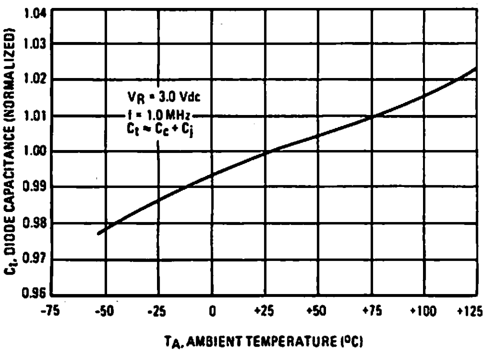


FIGURE 4 — DIODE CAPACITANCE



NOTES ON TESTING AND SPECIFICATIONS

1. Q is calculated by taking the G and C readings of an admittance bridge, such as Boonton Electronics Model 33AS8, at the specified frequency and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

2. C_R is the ratio of C_t measured at 3.0 Vdc divided by C_t measured at 25 Vdc.

6

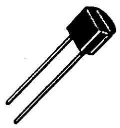
MMBV409L
MV409

Silicon Epicap Diodes

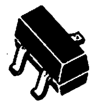
. . . designed for general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

- High Q with Guaranteed Minimum Values at VHF Frequencies
- Controlled and Uniform Tuning Ratio
- Available in Surface Mount Package

VOLTAGE VARIABLE CAPACITANCE DIODES
26–32 pF



CASE 182-02, STYLE 1
(TO-226AC)
MV409



CASE 318-07, STYLE 8
(TO-236AB)
SOT-23
MMBV409L

MAXIMUM RATINGS

Rating	Symbol	MV409	MMBV409L	Unit
		Value		
Reverse Voltage	V_R	20		Volts
Forward Current	I_F	200		mA
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	280 2.8	225* 1.8	mW mW/°C
Junction Temperature	T_J	+125		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

*FR5 Board 1.0 x 0.75 x 0.62 in.

DEVICE MARKING

MMBV409L = X5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic — All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	20	—	—	Vdc
Reverse Voltage Leakage Current (V_R = 15 Vdc)	I_R	—	—	0.1	μAdc
Diode Capacitance Temperature Coefficient (V_R = 3.0 Vdc, f = 1.0 MHz)	TC_C	—	300	—	ppm/°C

6

Device	C_t, Diode Capacitance V_R = 3 Vdc, f = 1 MHz pF Min	Nom	Max	Q, Figure of Merit V_R = 3 Vdc f = 50 MHz (Note 1) Min	C_R, Capacitance Ratio C_3/C_8 f = 1 MHz (Note 2) Min	Max
MMBV409L/MV409	26	29	32	200	1.5	1.9

NOTES ON TESTING AND SPECIFICATIONS

(1) Q is calculated by taking the G and C readings of an admittance bridge, such as Boonton Electronics Model 33AS8, at the specified frequency and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

(2) C_R is the ratio of C_t measured at 3 Vdc divided by C_t measured at 8 Vdc.

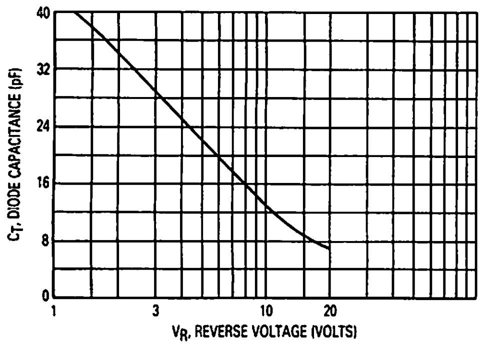


Figure 1. Diode Capacitance

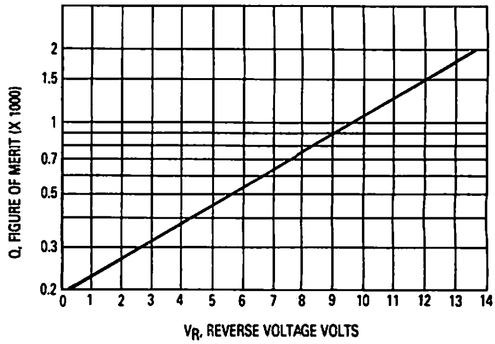


Figure 2. Figure of Merit

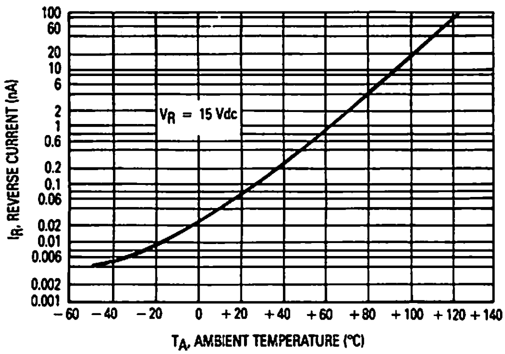


Figure 3. Leakage Current

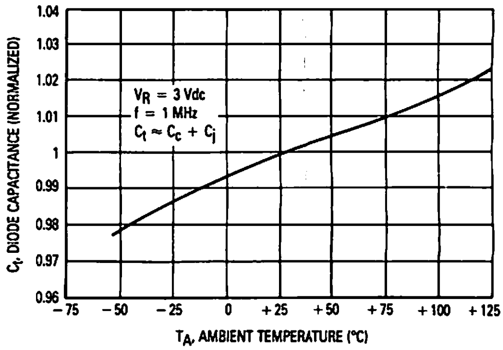


Figure 4. Diode Capacitance

6

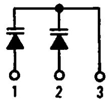
Silicon Epicap Diode

MMBV432L

DUAL VOLTAGE-VARIABLE CAPACITANCE DIODE

. . . designed for FM tuning, general frequency control and tuning, or any top-of-the-line application requiring back-to-back diode configuration for minimum signal distortion and detuning. This device is supplied in the SOT-23 plastic package for high volume, pick and place assembly requirements.

- High Figure of Merit — Q = 150 (Typ) @ V_R = 2 Vdc, f = 50 MHz
- Guaranteed Capacitance Range
- Dual Diodes — Save Space and Reduce Cost
- Surface Mount Package
- Available in 8 mm Tape and Reel
- Monolithic Chip Provides Improved Matching — Guaranteed ±1% (Max) Over Specified Tuning Range



CASE 318-07, STYLE 9
(TO-236AB)

MAXIMUM RATINGS (Each Diode)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	14	Volts
Forward Current	I_F	200	mA
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

DEVICE MARKING

MMBV432L = M4B

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	14	—	—	Vdc
Reverse Voltage Leakage Current (V_R = 9 Vdc)	I_R	—	—	100	nAdc
Diode Capacitance (V_R = 2 Vdc, f = 1 MHz)	C_T	43	—	48.1	pF
Capacitance Ratio C2/C8 (f = 1 MHz)	C_R	1.5	—	2	—
Figure of Merit* (V_R = 2 Vdc, f = 50 MHz)	Q	100	150	—	—

* $Q = \dfrac{1}{2\pi f C_T R_S}$

TYPICAL CHARACTERISTICS

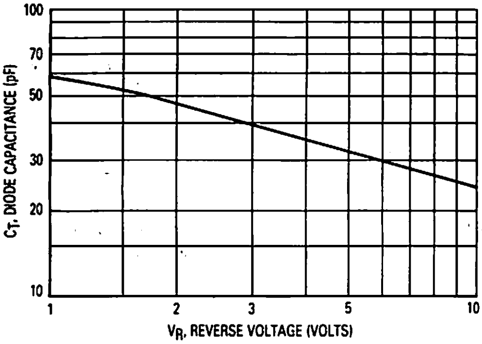


Figure 1. Diode Capacitance

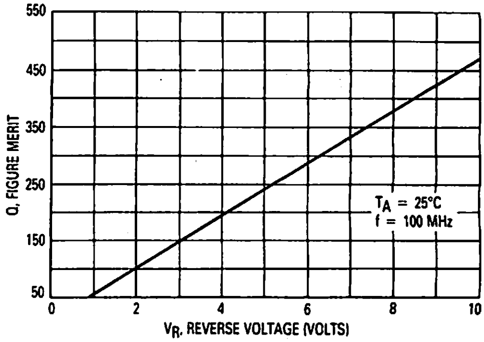


Figure 2. Figure of Merit versus Voltage

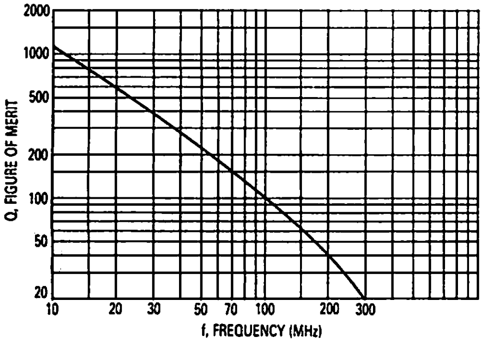


Figure 3. Figure of Merit versus Frequency

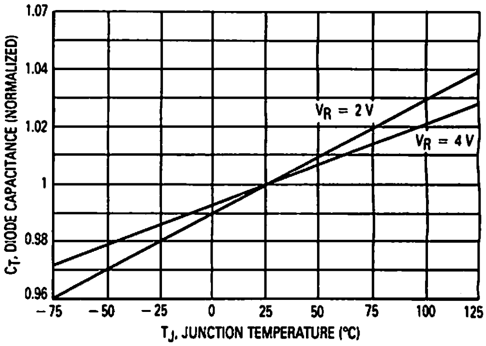


Figure 4. Diode Capacitance versus Temperature

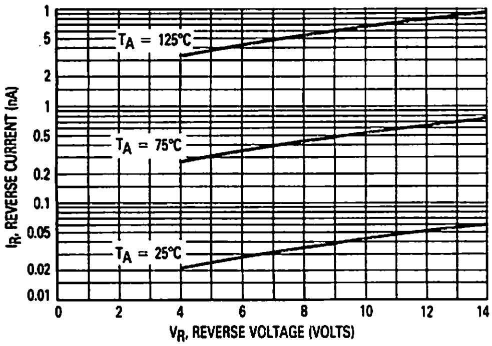


Figure 5. Reverse Current versus Reverse Voltage

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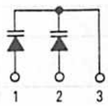
Silicon Epicap Diode

MMBV609L

. . . designed for FM tuning, general frequency control and tuning, or any top-of-the-line application requiring back-to-back diode configuration for minimum signal distortion and detuning. This device is supplied in the SOT-23 plastic package for high volume, pick and place assembly requirements.

- High Figure of Merit — Q = 350 (Typ) @ V_R = 3.0 Vdc, f = 50 MHz
- Guaranteed Capacitance Range
- *Dual Diodes* — Save Space and Reduce Cost
- Surface Mount Package
- Available in 8 mm Tape and Reel
- Monolithic Chip Provides Improved Matching
- Hyper Abrupt Junction Process Provides High Tuning Ratio

DUAL VOLTAGE-VARIABLE CAPACITANCE DIODE



CASE 318-07, STYLE 9
(TO-236AB)
SOT-23

DEVICE MARKING = 5L

MAXIMUM RATINGS (Each Diode)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	20	Volts
Forward Current	I_F	100	mA
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	20	—	—	Vdc
Reverse Voltage Leakage Current (V_R = 15 Vdc)	I_R	—	—	10	nAdc
Diode Capacitance (V_R = 3.0 Vdc, f = 1.0 MHz)	C_T	26	—	32	pF
Capacitance Ratio C3/C8 (f = 1.0 MHz)	C_R	1.8	—	2.4	—
Figure of Merit (V_R = 3.0 Vdc, f = 50 MHz)	Q	250	350	—	—

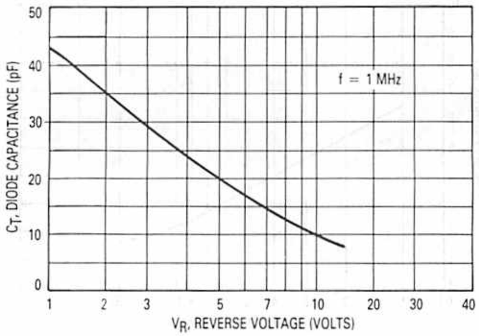


Figure 1. Diode Capacitance

6

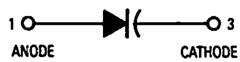
MMBV809L

Silicon Epicap Diode

... designed for 900 MHz frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

- Controlled and Uniform Tuning Ratio
- Available in Surface Mount Package
- Available in 8 mm Tape and Reel

VOLTAGE VARIABLE
CAPACITANCE DIODE
4.5–6.1 pF



CASE 318-07, STYLE 8
TO-236AB
SOT-23

DEVICE MARKING: 5K

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	20	Volts
Forward Current	I_F	20	mA
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	225* 1.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

*FR5 Board 1.0 x 0.75 x 0.62 in.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic — All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	20	—	—	Vdc
Reverse Voltage Leakage Current (V_R = 15 Vdc)	I_R	—	—	50	nAdc

	C_t, Diode Capacitance V_R = 2.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 3.0 Vdc f = 50 MHz (Note 1)	C_R, Capacitance Ratio C_2/C_8 f = 1.0 MHz (Note 2)	
Device	Min	Typ	Max	Min	Min	Max
MMBV809L	4.5	5.3	6.1	300	1.8	2.6

NOTES ON TESTING AND SPECIFICATIONS

(1) Q is calculated by taking the G and C readings of an admittance bridge, such as Boonton Electronics Model 33AS8, at the specified frequency and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

(2) C_R is the ratio of C_t measured at 2.0 Vdc divided by C_t measured at 8.0 Vdc.

6

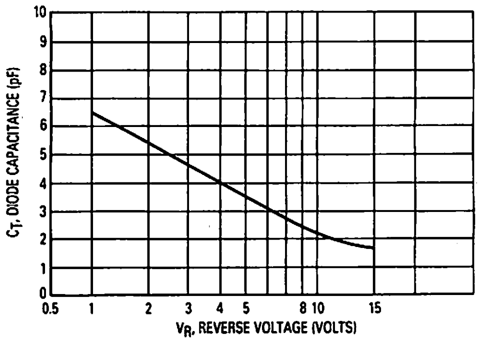
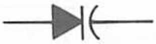


Figure 1. Diode Capacitance

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MMBV2101L thru MMBV2109L
MV2101 thru MV2115

VVC 

VOLTAGE-VARIABLE CAPACITANCE DIODES
6.8–100 pF
30 VOLTS

SILICON EPICAP DIODES

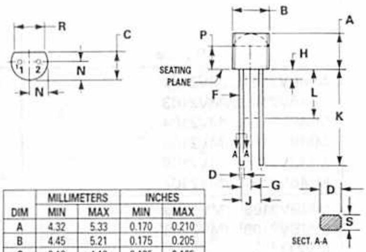
. . . designed in the popular PLASTIC PACKAGE for high volume requirements of FM Radio and TV tuning and AFC, general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

Also available in Surface Mount package up to 33 pF.

- High Q with Guaranteed Minimum Values
- Controlled and Uniform Tuning Ratio
- Standard Capacitance Tolerance — 10%
- Complete Typical Design Curves

CASE 182-02
MV2101 thru MV2115

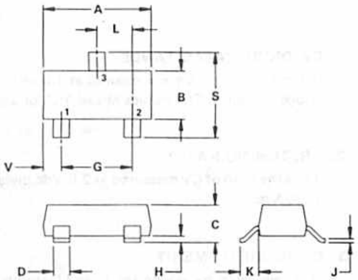
CASE 318-07
TO-236AB
SOT-23
MMBV2101L thru MMBV2109L



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	—	1.27	—	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

STYLE 1:
PIN 1. ANODE
2. CATHODE

CASE 182-02



STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.0350	0.0440
D	0.37	0.50	0.0150	0.0200
G	1.78	2.04	0.0701	0.0807
H	0.013	0.100	0.0005	0.0040
J	0.085	0.177	0.0034	0.0070
K	0.45	0.60	0.0180	0.0236
L	0.89	1.02	0.0350	0.0401
S	2.10	2.50	0.0830	0.0984
V	0.45	0.60	0.0177	0.0236

CASE 318-07
TO-236AB
SOT-23

MAXIMUM RATINGS

Rating	Symbol	Value MV2101 thru MV2115	Value MMBV2101L thru MMBV2109L	Unit
Reverse Voltage	V_R	30		Volts
Forward Current	I_F	200		mA
Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	280 2.8	200 2.0	mW mW/°C
Junction Temperature	T_J	+125		°C
Storage Temperature Range	T_{stg}	−55 to +150		°C

DEVICE MARKING

MMBV2101L = M4G
MMBV2103L = 4H
MMBV2104L = 4Z
MMBV2105L = 4U
MMBV2106L = 4V
MMBV2107L = 4W
MMBV2108L = 4X
MMBV2109L = 4J

6

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic — All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	30	—	—	Vdc
Reverse Voltage Leakage Current (V_R = 25 Vdc, T_A = 25°C)	I_R	—	—	0.1	μAdc
Diode Capacitance Temperature Coefficient (V_R = 4.0 Vdc, f = 1.0 MHz)	TC_C	—	280	—	ppm/°C

Device	C_T, Diode Capacitance V_R = 4.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 4.0 Vdc, f = 50 MHz	TR, Tuning Ratio C_2/C_{30} f = 1.0 MHz		
	Min	Nom	Max	Typ	Min	Typ	Max
MMBV2101L /MV2101	6.1	6.8	7.5	450	2.5	2.7	3.2
MMBV2103L /MV2103	9.0	10.0	11.0	400	2.5	2.9	3.2
MMBV2104L /MV2104	10.8	12.0	13.2	400	2.5	2.9	3.2
MMBV2105L /MV2105	13.5	15.0	16.5	400	2.5	2.9	3.2
MMBV2106L /MV2106	16.2	18.0	19.8	350	2.5	2.9	3.2
MMBV2107L /MV2107	19.8	22.0	24.2	350	2.5	2.9	3.2
MMBV2108L /MV2108	24.3	27.0	29.7	300	2.5	3.0	3.2
MMBV2109L /MV2109	29.7	33.0	36.3	200	2.5	3.0	3.2
MV2111	42.3	47.0	51.7	150	2.5	3.0	3.2
MV2113	61.2	68.0	74.8	150	2.6	3.0	3.3
MV2114	73.8	82.0	90.2	100	2.6	3.0	3.3
MV2115	90.0	100.0	110.0	100	2.6	3.0	3.3

PARAMETER TEST METHODS

6

1. **C_T, DIODE CAPACITANCE**
   (C_T = C_C + C_J). C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

2. **TR, TUNING RATIO**
   TR is the ratio of C_T measured at 2.0 Vdc divided by C_T measured at 30 Vdc.

3. **Q, FIGURE OF MERIT**
   Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equations:

$$Q = \frac{2\pi fC}{G}$$

   (Boonton Electronics Model 33AS8). Use Lead Length ≈1/16".

4. **TC_C, DIODE CAPACITANCE TEMPERATURE COEFFICIENT**
   TC_C is guaranteed by comparing C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = -65°C with C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = +85°C in the following equation which defines TC_C:

$$TC_C = \frac{C_T(+85^\circ C) - C_T(-65^\circ C)}{85 + 65} \cdot \frac{10^6}{C_R(25^\circ C)}$$

   Accuracy limited by measurement of C_T to ± 0.1 pF.

TYPICAL DEVICE PERFORMANCE

FIGURE 1 – DIODE CAPACITANCE versus REVERSE VOLTAGE

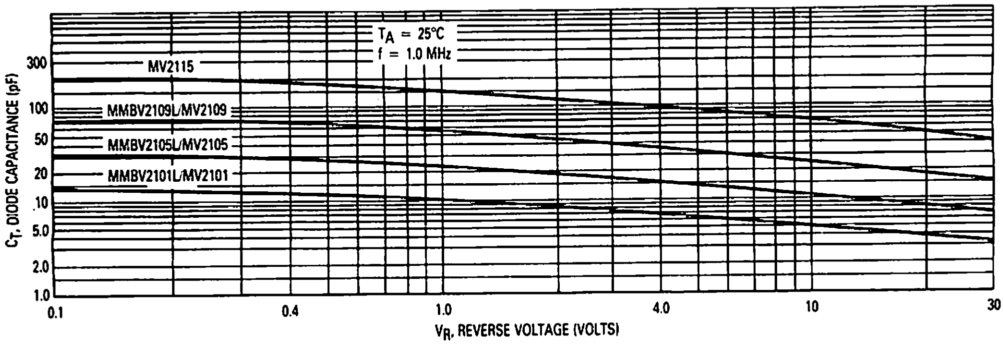


FIGURE 2 – NORMALIZED DIODE CAPACITANCE versus JUNCTION TEMPERATURE

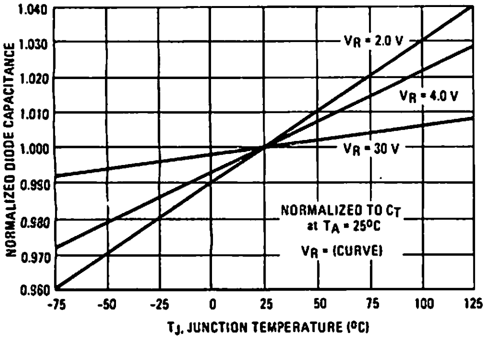


FIGURE 3 – REVERSE CURRENT versus REVERSE BIAS VOLTAGE

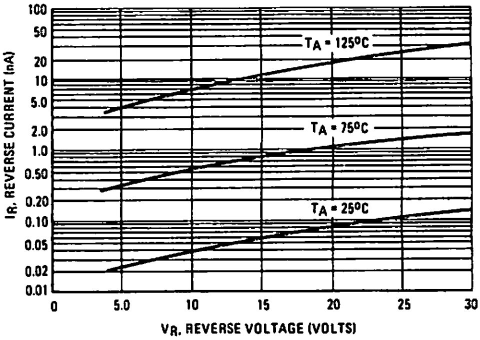


FIGURE 4 – FIGURE OF MERIT versus REVERSE VOLTAGE

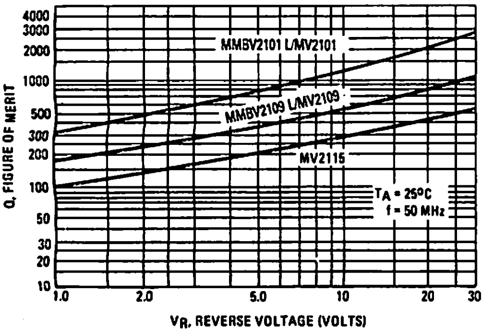
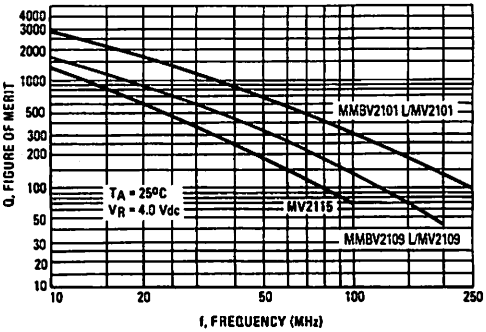


FIGURE 5 – FIGURE OF MERIT versus FREQUENCY



6

MMBV3102L

VVC 

SILICON EPICAP DIODE

. . . designed in the Surface Mount package for general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

- High Q with Guaranteed Minimum Values at VHF Frequencies
- Controlled and Uniform Tuning Ratio

VOLTAGE VARIABLE CAPACITANCE DIODE

22 pF (Nominal)
30 VOLTS

CASE 318-07
TO-236AB

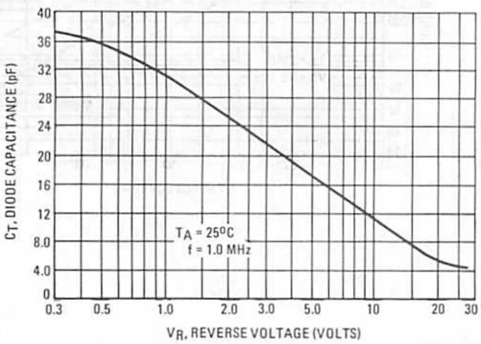
MAXIMUM RATINGS

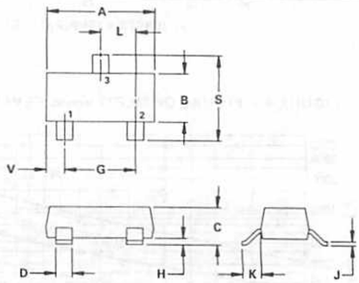
Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Forward Current	I_F	200	mA
Device Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	200 2.0	mW $mW/^oC$
Junction Temperature	T_J	+125	^oC
Storage Temperature Range	T_{stg}	−55 to +150	^oC

DEVICE MARKING

MMBV3102L = M4C

FIGURE 1 – DIODE CAPACITANCE





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.0350	0.0440
D	0.37	0.50	0.0150	0.0200
G	1.78	2.04	0.0701	0.0807
H	0.013	0.100	0.0005	0.0040
J	0.085	0.177	0.0034	0.0070
K	0.45	0.60	0.0180	0.0236
L	0.89	1.02	0.0350	0.0401
S	2.10	2.50	0.0830	0.0984
V	0.45	0.60	0.0177	0.0236

CASE 318-07
TO-236AB

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic—All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	30	—	—	Vdc
Reverse Voltage Leakage Current (V_R = 25 Vdc, T_A = 25°C)	I_R	—	—	0.1	μAdc
Diode Capacitance Temperature Coefficient (V_R = 3.0 Vdc, f = 1.0 MHz)	TC_C	—	300	—	ppm/°C

	C_T, Diode Capacitance V_R = 3.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 3.0 Vdc f = 50 MHz	C_R, Capacitance Ratio C_3/C_{25} f = 1.0 MHz	
Device	Min	Nom	Max	Min	Min	Typ
MMBV3102L	20	22	25	200	4.5	4.8

FIGURE 2 — FIGURE OF MERIT

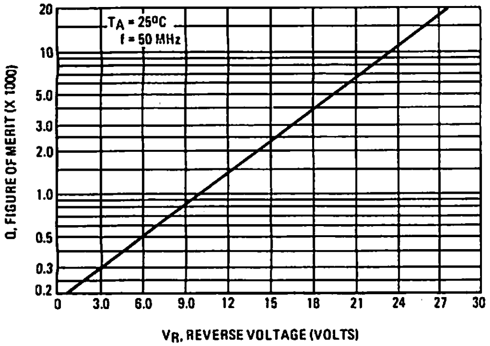


FIGURE 3 — LEAKAGE CURRENT

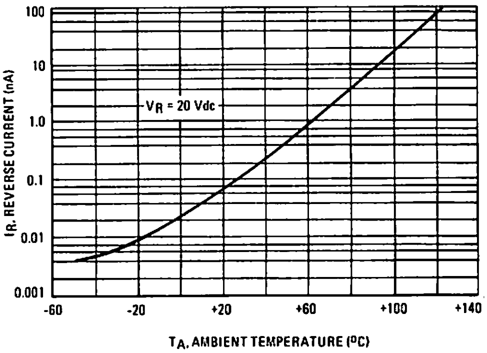
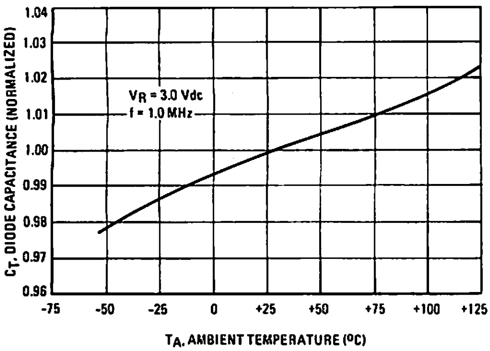


FIGURE 4 — DIODE CAPACITANCE



NOTES ON TESTING AND SPECIFICATIONS

1. L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).
2. C_C is measured on a package without a die, using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
3. Q is calculated by taking the G and C readings of an admittance bridge, such as Boonton Electronics Model 33AS8, at the specified frequency and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

4. C_R is the ratio of C_T measured at 3.0 Vdc divided by C_T measured at 25 Vdc.

6

MMBV3401L

SILICON PIN SWITCHING DIODE

SILICON PIN DIODE

. . . designed primarily for VHF band switching applications but also suitable for use in general-purpose switching and attenuator circuits. Supplied in a Surface Mount package.

- Rugged PIN Structure Coupled with Wirebond Construction for Optimum Reliability
- Low Capacitance — 0.7 pF Typ at V_R = 20 V
- Very Low Series Resistance at 100 MHz — 0.34 Ohms (Typ) @ I_F = 10 mAdc

CASE 318-07
TO-236AB

MAXIMUM RATINGS

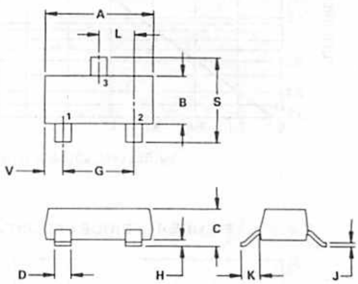
Rating	Symbol	Value	Unit
Reverse Voltage	V_R	20	Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	200 2.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

DEVICE MARKING

MMBV3401L = 4D

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	35	—	—	Volts
Diode Capacitance V_R = 20 V	C_T	—	—	1.0	pF
Series Resistance (Figure 5) (I_F = 10 mA) f = 100 MHz	R_S	—	—	0.7	Ohms
Reverse Leakage Current (V_R = 25 V)	I_R	—	—	0.1	μA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.0350	0.0440
D	0.37	0.50	0.0150	0.0200
G	1.78	2.04	0.0701	0.0807
H	0.013	0.100	0.0005	0.0040
J	0.085	0.177	0.0034	0.0070
K	0.45	0.60	0.0180	0.0236
L	0.89	1.02	0.0350	0.0401
S	2.10	2.50	0.0830	0.0984
V	0.45	0.60	0.0177	0.0236

CASE 318-07
TO-236AB

6

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – SERIES RESISTANCE

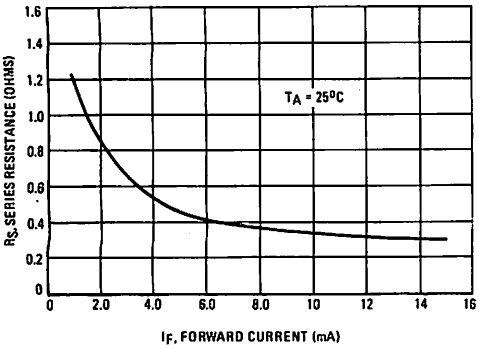


FIGURE 2 – FORWARD VOLTAGE

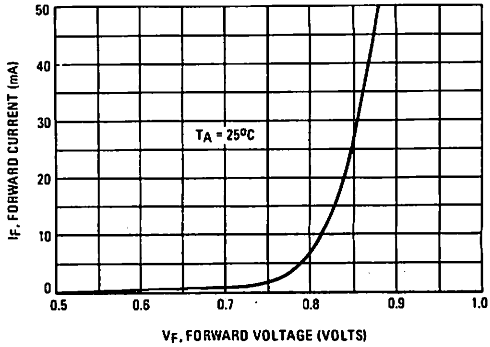


FIGURE 3 – DIODE CAPACITANCE

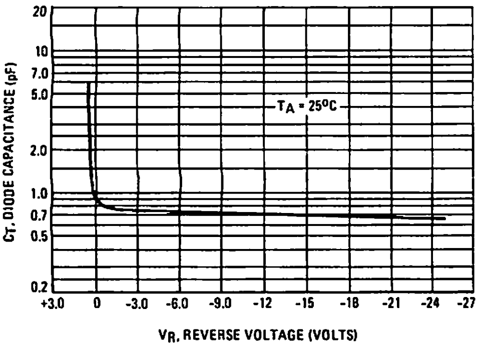


FIGURE 4 – LEAKAGE CURRENT

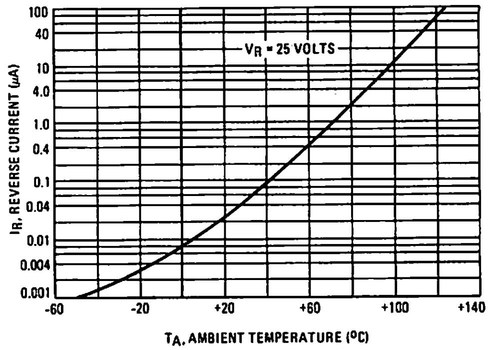
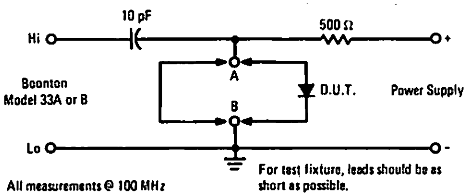


FIGURE 5 – FORWARD SERIES RESISTANCE TEST METHOD



To measure series resistance, a 10 pF capacitor is used to reduce the forward capacitance of the circuit and to prevent shorting of the external power supply through the bridge. The small signal from the bridge is prevented from shorting through the power supply by the 500-ohm resistor. The resistance of the 10 pF capacitor can be considered negligible for this measurement.

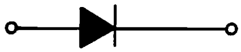
1. The RF Admittance Bridge (Boonton 33A or B) must be initially balanced, with the test circuit connected to the bridge test terminals. The conductance scale will be set at zero and the capacitance scale will be set at 120 pF, as required when using the 100 MHz test coil.
2. Use a short length of wire to short the test circuit from point "A" to "B". Then connect the power supply providing 10 mA of bias current to the test circuit.
3. Adjust the capacitance scale arm of the bridge and the "G" zero control for a minimum null on the "null meter". The null occurs at approximately 130 pF.
4. Replace the wire short with the device to be tested. Bias the device to a forward conductance state of 10 mA.
5. Obtain a minimum null on the "null meter", with the capacitance and conductance scale adjustment arms.
6. Read conductance (G) direct from the scale. Now read the capacitance value from the scale (≈ 130 pF) and subtract 120 pF which yields capacitance (C). The forward resistance (R_S) can now be calculated from:

$$R_S = \frac{2.533\,G}{C^2}$$

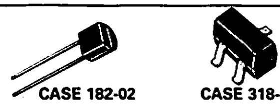
Where:
G – in micromhos,
C – in pF,
R_S – in ohms

6

MMBV3700L
MPN3700



SILICON PIN SWITCHING DIODES



CASE 182-02	CASE 318-07
TO-226AC	TO-236AB
TO-92	SOT-23
MPN3700	MMBV3700L

HIGH VOLTAGE SILICON PIN DIODES

. . . designed primarily for VHF band switching applications but also suitable for use in general-purpose switching and attenuator circuits. Supplied in a cost effective plastic package for economical, high-volume consumer and industrial requirements.

- Long Reverse Recovery Time
  t_{rr} = 300 ns (Typ)
- Rugged PIN Structure Coupled with Wirebond Construction for Optimum Reliability
- Low Series Resistance @ 100 MHz —
  R_S = 0.7 Ohms (Typ) @ I_F = 10 mAdc
- Reverse Breakdown Voltage = 200 V (Min)

6

MAXIMUM RATINGS

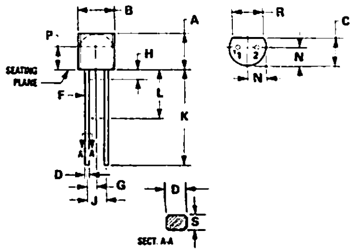
Rating	Symbol	Value MPN3700	Value MMBV3700L	Unit
Reverse Voltage	V_R	200		Volts
Total Device Dissipation @ T_A = 25°C	P_D	280	200	mW
Derate above 25°C		2.8	2.0	mW/°C
Junction Temperature	T_J	+125		°C
Storage Temperature Range	T_{stg}	−55 to +150		°C

DEVICE MARKING

MMBV3700L = 4R

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

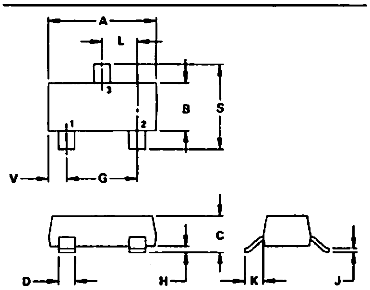
Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	200	—	—	Volts
Diode Capacitance (V_R = 20 Vdc, f = 1.0 MHz)	C_T	—	—	1.0	pF
Series Resistance (Figure 5) (I_F = 10 mA)	R_S	—	0.7	1.0	Ohms
Reverse Leakage Current (V_R = 150 Vdc)	I_R	—	—	0.1	μA
Reverse Recovery Time (I_F = I_R = 10 mA)	t_{rr}	—	300	—	ns



STYLE 1:
PIN 1. ANODE
2. CATHODE

CASE 182-02
TO-226AC (TO-92)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	—	1.27	—	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016



STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

CASE 318-07
TO-236AB
SOT-23

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.0350	0.0440
D	0.37	0.50	0.0150	0.0200
G	1.78	2.04	0.0701	0.0807
H	0.013	0.100	0.0005	0.0040
J	0.085	0.177	0.0034	0.0070
K	0.45	0.60	0.0180	0.0236
L	0.89	1.02	0.0350	0.0401
S	2.10	2.50	0.0830	0.0984
V	0.45	0.60	0.0177	0.0236

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 — SERIES RESISTANCE

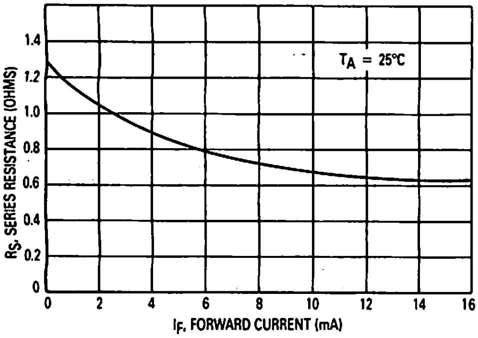


FIGURE 2 — FORWARD VOLTAGE

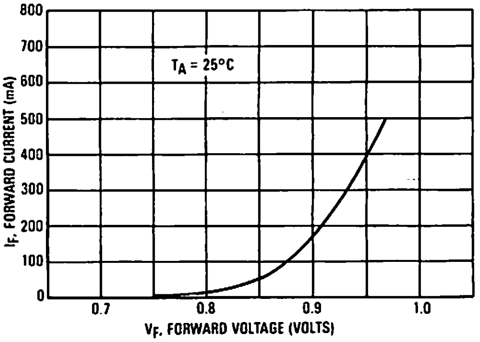


FIGURE 3 — DIODE CAPACITANCE

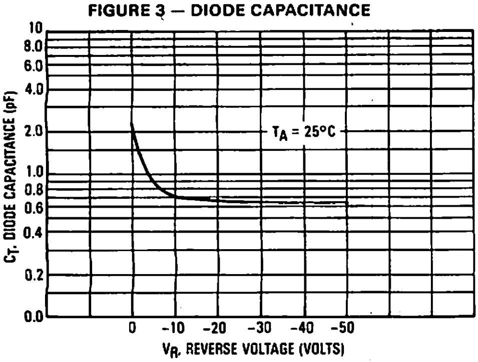


FIGURE 4 — LEAKAGE CURRENT

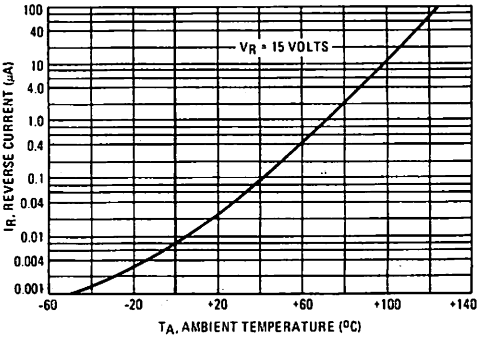
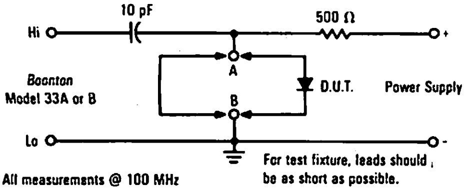


FIGURE 5 — FORWARD SERIES RESISTANCE TEST METHOD



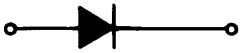
To measure series resistance, a 10 pF capacitor is used to reduce the forward capacitance of the circuit and to prevent shorting of the external power supply through the bridge. The small signal from the bridge is prevented from shorting through the power supply by the 500-ohm resistor. The resistance of the 10 pF capacitor can be considered negligible for this measurement.

1. The RF Admittance Bridge (Boonton 33A or B) must be initially balanced, with the test circuit connected to the bridge test terminals. The conductance scale will be set at zero and the capacitance scale will be set at 120 pF, as required when using the 100 MHz test coil.
2. Use a short length of wire to short the test circuit from point "A" to "B". Then connect the power supply providing 10 mA of bias current to the test circuit.
3. Adjust the capacitance scale arm of the bridge and the "G" zero control for a minimum null on the "null meter". The null occurs at approximately 130 pF.
4. Replace the wire short with the device to be tested. Bias the device to a forward conductance state of 10 mA.
5. Obtain a minimum null on the "null meter", with the capacitance and conductance scale adjustment arms.
6. Read conductance (G) direct from the scale. Now read the capacitance value from the scale (≈130 pF) and subtract 120 pF which yields capacitance (C). The forward resistance (R_S) can now be calculated from:

$$R_S = \frac{2.533\ G}{C^2}$$

Where:
G — in micromhos,
C — in pF,
R_S — in ohms

MPN3404



SILICON PIN DIODE

. . . designed primarily for VHF band switching applications but also suitable for use in general-purpose switching and attenuator circuits. Supplied in a cost effective TO-92 type plastic package for economical, high-volume consumer and industrial requirements.

- Rugged PIN Structure Coupled with Wirebond Construction for Optimum Reliability
- Low Series Resistance @ 100 MHz — R_S = 0.7 Ohms (Typ) @ I_F = 10 mAdc
- Sturdy TO-92 Style Package for Handling Ease

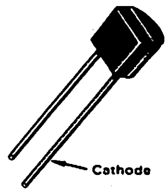
MAXIMUM RATINGS

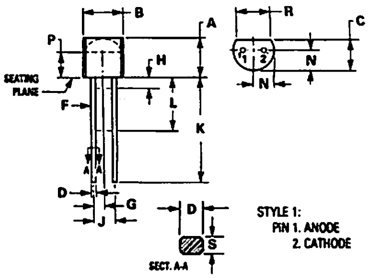
Rating	Symbol	Value	Unit
Reverse Voltage	V_R	20	Volts
Forward Power Dissipation @ T_A = 25°C Derate above 25°C	P_F	400 4.0	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μA)	$V_{(BR)R}$	20	–	–	Volts
Diode Capacitance (V_R = 15 Vdc, f = 1.0 MHz)	C_T	–	1.3	2.0	pF
Series Resistance (Figure 5) (I_F = 10 mA)	R_S	–	0.7	0.85	Ohms
Reverse Leakage Current (V_R = 15 Vdc)	I_R	–	–	0.1	μA

SILICON PIN
SWITCHING DIODE





STYLE 1:
PIN 1. ANODE
2. CATHODE

NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE P IS UNCONTROLLED.
2. DIMENSION F APPLIES BETWEEN H AND L. DIMENSION D AND S APPLIES BETWEEN L AND 12.70mm (0.5") FROM SEATING PLANE. LEAD DIMENSION IS UNCONTROLLED IN H AND BEYOND 12.70mm (0.5") FROM SEATING PLANE.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	–	1.27	–	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

CASE 182-02

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – SERIES RESISTANCE

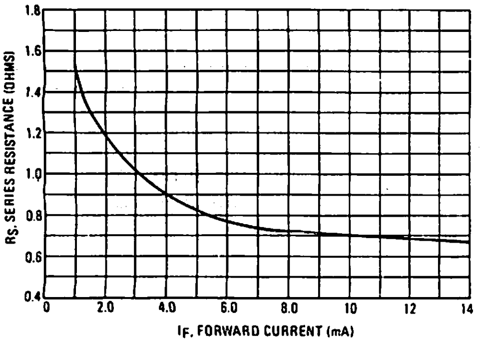


FIGURE 2 – FORWARD VOLTAGE

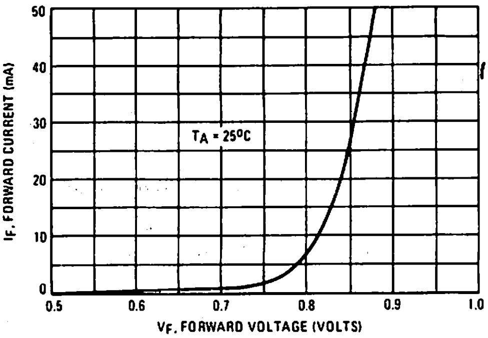


FIGURE 3 – DIODE CAPACITANCE

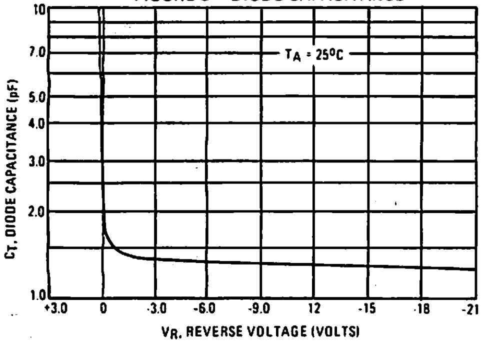


FIGURE 4 – LEAKAGE CURRENT

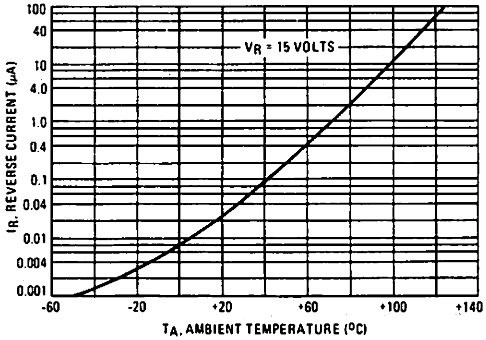
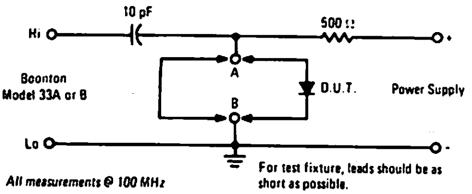


FIGURE 5 – FORWARD SERIES RESISTANCE TEST METHOD



To measure series resistance, a 10 pF capacitor is used to reduce the forward capacitance of the circuit and to prevent shorting of the external power supply through the bridge. The small signal from the bridge is prevented from shorting through the power supply by the 500-ohm resistor. The resistance of the 10 pF capacitor can be considered negligible for this measurement.

1. The RF Admittance Bridge (Boonton 33A or B) must be initially balanced, with the test circuit connected to the bridge test terminals. The conductance scale will be set at zero and the capacitance scale will be set at 120 pF, as required when using the 100 MHz test coil.
2. Use a short length of wire to short the test circuit from point "A" to "B". Then connect the power supply providing 10 mA of bias current to the test circuit.
3. Adjust the capacitance scale arm of the bridge and the "G" zero control for a minimum null on the "null meter". The null occurs at approximately 130 pF.
4. Replace the wire short with the device to be tested. Bias the device to a forward conductance state of 10 mA.
5. Obtain a minimum null on the "null meter", with the capacitance and conductance scale adjustment arms.
6. Read conductance (G) direct from the scale. Now read the capacitance value from the scale (≈ 130 pF) and subtract 120 pF which yields capacitance (C). The forward resistance (R_S) can now be calculated from:

$$R_S = \frac{2.533\,G}{C^2}$$

Where:
G – in micromhos,
C – in pF,
R_S – in ohms

6

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MV104

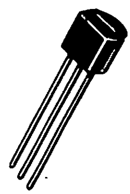
VVC

SILICON EPICAP DIODE

. . . designed for FM tuning, general frequency control and tuning, or any top-of-the-line application requiring back-to-back diode configurations for minimum signal distortion and detuning. This device is supplied in the popular TO-92 plastic package for high volume, economical requirements of consumer and industrial applications.

- High Figure of Merit – Q = 140 (Typ) @ V_R = 3.0 Vdc, f = 100 MHz
- Guaranteed Capacitance Range 37– 42 pF @ V_R = 3.0 Vdc (MV104)
- Dual Diodes – Save Space and Reduce Cost
- TO-92 Package for Easy Handling and Mounting
- Monolithic Chip Provides Near Perfect Matching – Guaranteed ± 1% (Max) Over Specified Tuning Range.

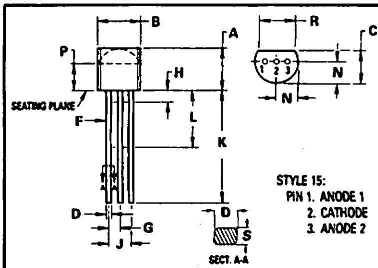
DUAL VOLTAGE-VARIABLE CAPACITANCE DIODE



CASE 29-04
TO-226AA

MAXIMUM RATINGS (Each Device)

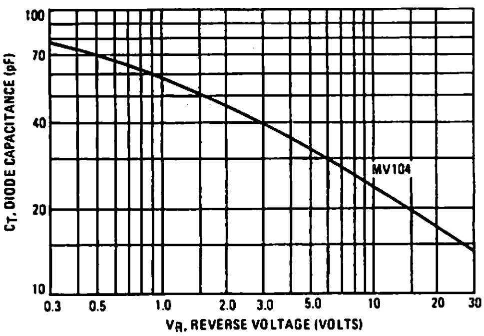
Rating	Symbol	Value	Unit
Reverse Voltage	V_R	32	Volts
Forward Current	I_F	200	mA
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	280 2.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
H	–	2.54	–	0.100
J	2.42	2.66	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.04	2.66	0.080	0.105
P	2.93	–	0.115	–
R	3.43	–	0.135	–
S	0.39	0.50	0.015	0.020

CASE 29-04
TO-226AA

FIGURE 1 — DIODE CAPACITANCE



6

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, Each Device)

Characteristic—All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	32	–	–	Vdc
Reverse Voltage Leakage Current (V_R = 30 Vdc) T_A = 25°C T_A = 60°C	I_R	– –	– –	50 500	nAdc
Diode Capacitance Temperature Coefficient (V_R = 4.0 Vdc, f = 1.0 MHz)	TC_C	–	280	–	ppm/°C

	C_T, Diode Capacitance V_R = 3.0 Vdc, f = 1.0 MHz pF		Q, Figure of Merit V_R = 3.0 Vdc f = 100 MHz		C_R, Capacitance Ratio C_3/C_{30} f = 1.0 MHz	
Device	Min	Max	Min	Typ	Min	Max
MV104	37	42	100	140	2.5	2.8

TYPICAL CHARACTERISTICS (Each Device)

FIGURE 2 – FIGURE OF MERIT versus VOLTAGE

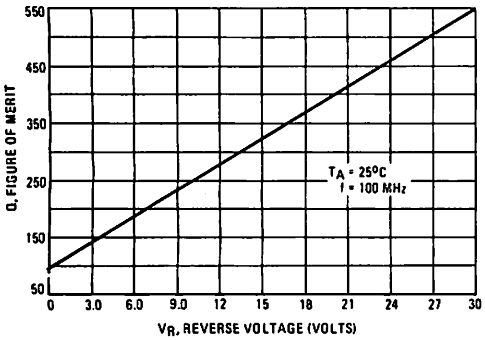


FIGURE 3 – FIGURE OF MERIT versus FREQUENCY

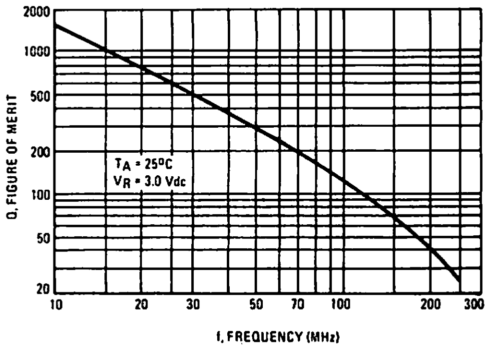


FIGURE 4 – DIODE CAPACITANCE versus TEMPERATURE

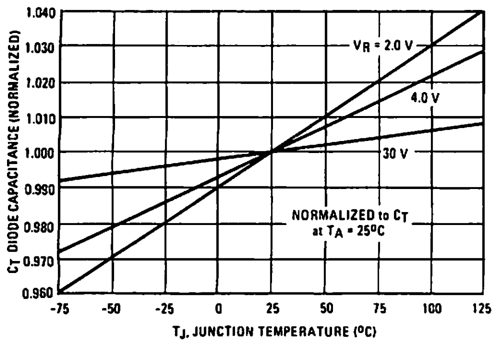
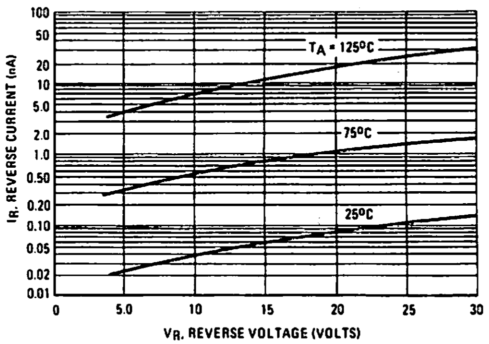


FIGURE 5 – REVERSE CURRENT versus REVERSE VOLTAGE



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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MV1401, H
MV1403, H
MV1404, H
MV1405, H

Tuning Diodes

SILICON HYPER-ABRUPT TUNING DIODES

. . . designed with high capacitance and a capacitance change of greater than TEN TIMES for a bias change from 2 to 10 volts. Provides tuning over broad frequency ranges; tunes AM radio broadcast band, general AFC and tuning applications in lower RF frequencies.

- High Capacitance: 120–550 pF
- Large Capacitance Change with Small Bias Change
- Guaranteed High Q
- Available in Standard Axial Glass Packages
- H Suffix Devices with 100% Screening

100% SCREENING FOR HIGH RELIABILITY

MV1401H, MV1403H, MV1404H, MV1405H are screened with the following tests:

Internal Visual Inspection
per 12M53957B (MIL-STD-750 METHOD 2073 PARAGRAPH 3.3 AND METHOD 2074 PARAGRAPH 3.1.3)

High Temperature Storage
T_A = 200°C, t ≥ 48 hours

Thermal Shock (Temperature Cycling)
MIL-STD-202, Method 107, Condition C except 10 cycles continuously performed
t(extremes) = 15 minutes

Constant Acceleration
MIL-STD-750, Method 2006
20,000 G's (Y1 axis only)

Hermetic Seal
MIL-STD-750, Method 1071
Fine Leak - Condition G
Gross Leak - Condition D

Electrical Test
I_R and C_T

High Temperature Reverse Bias
T_A = 120°C ± 5°C, t ≥ 96 hours
V_R = 80% of $V_{(BR)R}$ MIN
Lower temperature till T_A = 30 ± 5°C.
Maintain this temperature prior to removal of Reverse Bias Voltage. Perform Electrical Test within 24 hours following bias removal.

Electrical Test
I_R and C_T

HIGH TUNING RATIO VOLTAGE-VARIABLE CAPACITANCE DIODES

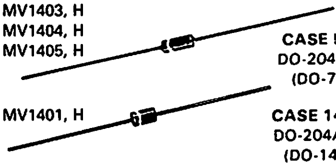
120–550 pF
12 VOLTS

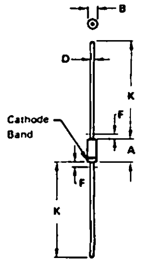
MV1403, H
MV1404, H
MV1405, H

CASE 51
DO-204AA
(DO-7)

MV1401, H

CASE 146
DO-204AB
(DO-14)

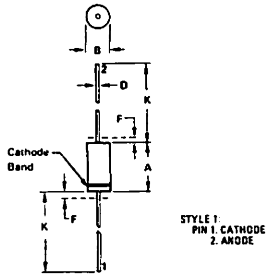




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	38.10	1.000	1.500

All JEDEC dimensions and notes apply

CASE 51-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.84	7.62	0.230	0.300
B	2.74	3.56	0.108	0.140
D	0.46	0.56	0.018	0.022
F	–	1.27	–	0.050
K	25.40	–	1.000	–

All JEDEC dimensions and notes apply.

CASE 146-01

6

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	12	Volts
Forward Current	I_F	250	mA
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Junction Temperature	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic — All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage *(I_R = 10 μAdc)*	$V_{(BR)R}$	12	—	—	Vdc
Leakage Current at Reverse Voltage (V_R = 10 Vdc, T_A = 25°C)	I_R	—	—	0.10	μAdc
Series Inductance (f = 250 MHz, Lead Length ≈ 1/16")	L_S	—	5.0	—	nH
Case Capacitance (f = 1.0 MHz, Lead Length ≈ 1/16")	C_C	—	0.25	—	pF

	C_T, Diode Capacitance						Q, Figure of Merit	TR, Tuning Ratio	
	V_R = 1.0 Vdc, f = 1.0 MHz pF			V_R = 2.0 Vdc, f = 1.0 MHz pF			V_R = 2.0 Vdc, f = 1.0 MHz	C_1/C_{10} f = 1.0 MHz	C_2/C_{10} f = 1.0 MHz
Device	Min	Nom	Max	Min	Nom	Max	Min	Min	Min
MV1401, H	468	550	633	—	—	—	200	14	—
MV1403, H	—	—	—	140	175	210	200	—	10
MV1404, H	—	—	—	96	120	144	200	—	10
MV1405, H	—	—	—	200	250	300	200	—	10

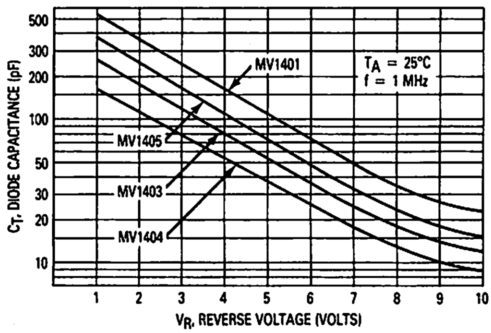
PARAMETER TEST METHODS

1. **L_S, SERIES INDUCTANCE**
   L_S is measured on a shorted package at 250 MHz using an impedance bridge (Boonton Radio Model 250A RX Meter).
2. **C_C, CASE CAPACITANCE**
   C_C is measured on an open package at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
3. **C_T, DIODE CAPACITANCE**
   ($C_T = C_C + C_J$) C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
4. **TR, TUNING RATIO**
   TR is the ratio of C_T measured at 2.0 Vdc (1.0 Vdc for MV1401) divided by C_T measured at 10 Vdc.
5. **Q, FIGURE OF MERIT**
   Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

(Boonton Electronics Model 33AS8). Use Lead Length ≈ 1/16".

FIGURE 1 — DIODE CAPACITANCE versus REVERSE VOLTAGE



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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

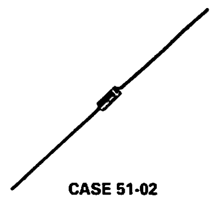
MV1620 THRU MV1650

Silicon Epicap Diodes

. . . epitaxial passivated tuning diodes designed for AFC applications in radio, TV, and general electronic-tuning.

- Maximum Working Voltage of 20 V
- Excellent Q Factor at High Frequencies
- Solid-State Reliability to Replace Mechanical Tuning Methods

VOLTAGE-VARIANCE CAPACITANCE DIODES
6.8–100 pF
20 VOLTS



CASE 51-02
TO-204AA
(DO-7)

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Reverse Voltage	V_R	20	Volts
Forward Current	I_F	250	mA
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Junction Temperature	T_J	+175	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic — All Types	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	20	—	—	Vdc
Reverse Voltage Leakage Current (V_R = 15 Vdc)	I_R	—	—	0.1	μAdc
Series Inductance (f = 250 MHz, lead length ≈ 1/16")	L_S	—	4.0	—	nH
Case Capacitance (f = 1.0 MHz, lead length ≈ 1/16")	C_C	—	0.17	—	pF

Device	C_T, Diode Capacitance V_R = 4.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 4.0 Vdc, f = 50 MHz	TR, Tuning Ratio C_2/C_{20} f = 1.0 MHz	
	Min	Nom	Max	Min	Min	Max
MV1620	6.1	6.8	7.5	300	2.0	3.2
MV1624	9.0	10.0	11.0	300	2.0	3.2
MV1626	10.8	12.0	13.2	300	2.0	3.2
MV1628	13.5	15.0	16.5	250	2.0	3.2
MV1630	16.2	18.0	19.8	250	2.0	3.2
MV1634	19.8	22.0	24.2	250	2.0	3.2
MV1636	24.3	27.0	29.7	200	2.0	3.2
MV1638	29.7	33.0	36.3	200	2.0	3.2
MV1640	35.1	39.0	42.9	200	2.0	3.2
MV1642	42.3	47.0	51.7	200	2.0	3.2
MV1644	50.4	56.0	61.6	150	2.0	3.2
MV1648	73.8	82.0	90.2	150	2.0	3.2
MV1650	90.0	100.0	110.0	150	2.0	3.2

TR, Tuning Ratio, is the ratio of C_T measured at 2.0 Vdc divided by C_T measured at 20 Vdc.

6

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

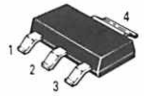
MV7005T1
MV7005T3

Silicon Epicap Diodes

. . . designed for high-capacitance, high-tuning ratio applications.

- Guaranteed Capacitance Range
- Surface Mount Package
- Available in 12 mm Tape and Reel
- Hyper Abrupt Junction Process Provides High Tuning Ratio
- T1 is Tape and Reel 7", 1000 Units
- T3 is Tape and Reel 13", 4000 Units

HIGH CAPACITANCE VOLTAGE-VARIABLE DIODES



CASE 318E-04, STYLE 2
SOT-223

DEVICE MARKING = V7005

MAXIMUM RATINGS (Each Diode)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	15	Volts
Forward Current	I_F	50	mA
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	280 2.8	mW mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Reverse Breakdown Voltage ($I_R = 10\ \mu Adc$)	$V_{(BR)R}$	15	—	Vdc
Reverse Voltage Leakage Current ($V_R = 9.0$ Vdc)	I_R	—	100	nAdc
Diode Capacitance ($V_R = 1.0$ Vdc, f = 1.0 MHz)	C_T	400	520	pF
Capacitance Ratio C1/C9 (f = 1.0 MHz)	C_R	12	—	—
Figure of Merit ($V_R = 1.0$ Vdc, f = 1.0 MHz)	Q	150	—	—

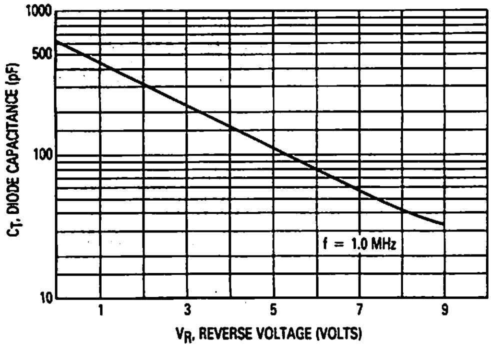


Figure 1. Diode Capacitance versus Reverse Voltage

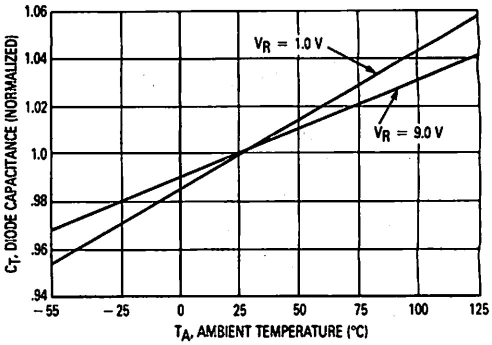


Figure 2. Diode Capacitance versus Ambient Temperature

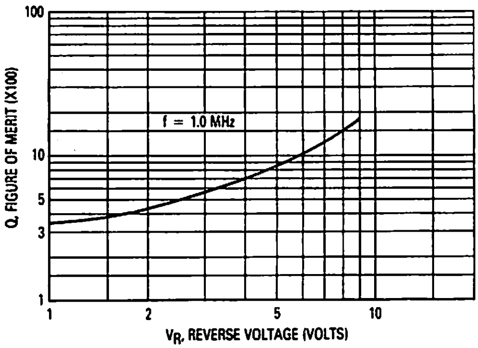


Figure 3. Figure of Merit

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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MVAM108
MVAM109
MVAM115
MVAM125

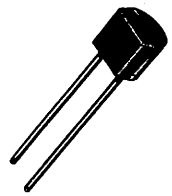
VVC

SILICON TUNING DIODE

. . . designed for electronic tuning of AM receivers and high capacitance, high tuning ratio applications.

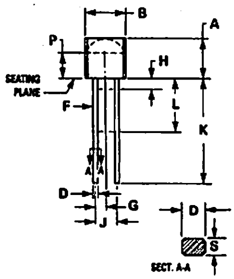
- High Capacitance Ratio — C_R = 15 (Min), *MVAM 108, 115, 125*
- Guaranteed Diode Capacitance — C_t = 440 pF (Min) — 560 pF (Max) @ V_R = 1.0 Vdc, f = 1.0 MHz, MVAM108, MVAM115, MVAM125
- Guaranteed Figure of Merit — Q = 150 (Min) @ V_R = 1.0 Vdc, f = 1.0 MHz.

TUNING DIODES WITH VERY HIGH CAPACITANCE RATIO



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R		Volts
MVAM108		12	
MVAM109		15	
MVAM115		18	
MVAM125		28	
Forward Current	I_F	50	mA
Power Dissipation @ T_A = 25°C Derate Above 25°C	P_D	280 2.8	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +125	°C

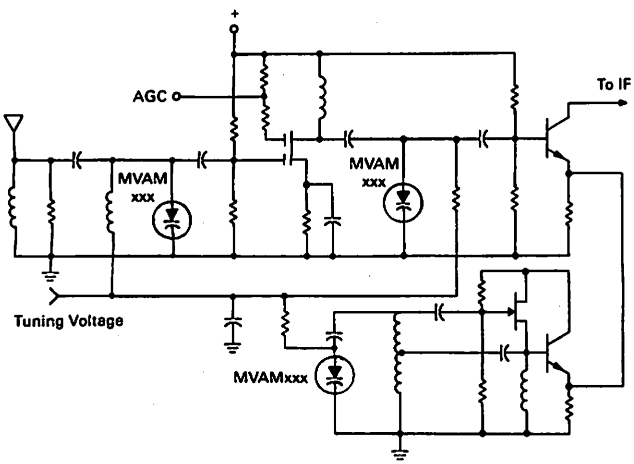


STYLE 1:
PIN 1. ANODE
2. CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	—	1.27	—	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

CASE 182-02

FIGURE 1 — TYPICAL AM RADIO APPLICATION



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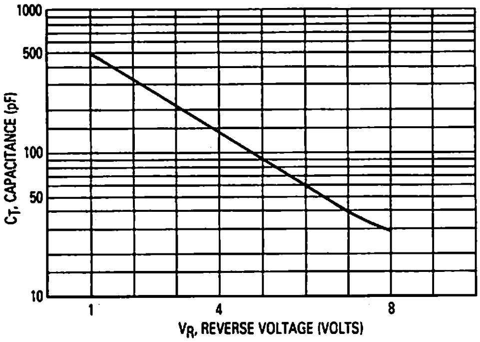
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, Each Device)

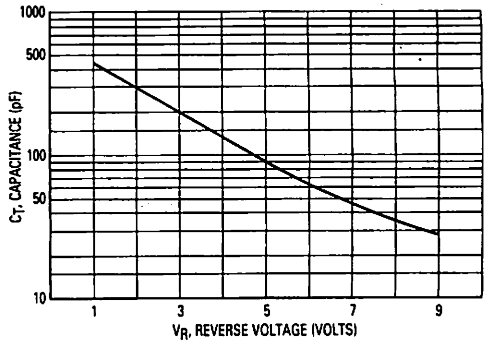
Characteristic — All Types		Symbol	Min	Typ	Max	Unit
Breakdown Voltage		$V_{(BR)R}$				Vdc
(I_R = 10 μAdc)	MVAM108		12	—	—	
	MVAM109		15	—	—	
	MVAM115		18	—	—	
	MVAM125		28	—	—	
Reverse Current		I_R				nAdc
(V_R = 8.0 V)	MVAM108		—	—	100	
(V_R = 9.0 V)	MVAM109		—	—	100	
(V_R = 15 V)	MVAM115		—	—	100	
(V_R = 25 V)	MVAM125		—	—	100	
Diode Capacitance Temperature Coefficient (1) (V_R = 1.0 Vdc, f = 1.0 MHz, T_A = −40°C to +85°)		TC_C	—	435	—	ppm/°C
Case Capacitance (f = 1.0 MHz, Lead Length 1/16")		C_C	—	0.18	—	pF
Diode Capacitance (2)		C_t				pF
(V_R = 1.0 Vdc, f = 1.0 MHz)	MVAM108, 115, 125		440	500	560	
	MVAM109		400	460	520	
Figure of Merit (f = 1.0 MHz, Lead Length 1/16", V_R = 1.0 Vdc)		Q	150	—	—	—
Capacitance Ratio						—
(f = 1.0 MHz)	MVAM108	C1/C8	15	—	—	
	MVAM109	C1/C9	12	—	—	
	MVAM115	C1/C15	15	—	—	
	MVAM125	C1/C25	15	—	—	

Notes:
(1) The effect of increasing temperature 1.0°C, at any operating point, is equivalent to lowering the effective tuning voltage 1.25 mV. The percent change of capacitance per °C is nearly constant from −40°C to +100°C.
(2) Upon request, diodes are available in matched sets. All diodes in a set can be matched for capacitance to 3% or 2.0 pF (whichever is greater) at all points along the specified tuning range.

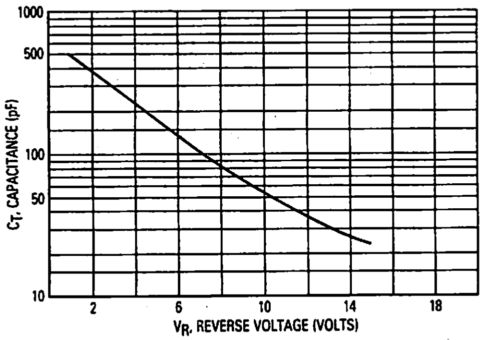
MVAM108
Figure 2. Capacitance versus Reverse Voltage



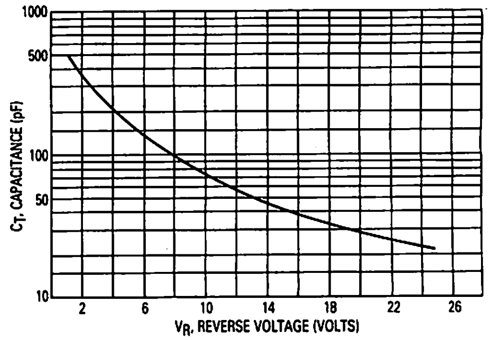
MVAM109
Figure 3. Capacitance versus Reverse Voltage



MVAM115
Figure 4. Capacitance versus Reverse Voltage



MVAM 125
Figure 5. Capacitance versus Reverse Voltage



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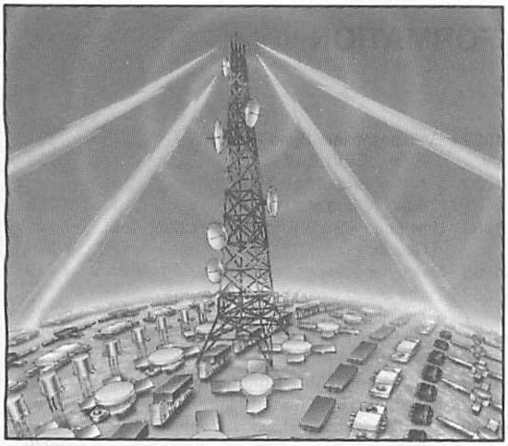

Volume II

Technical Information

7

APPLICATIONS INFORMATION

RF TRANSISTOR DESIGN

Class C Power

The primary concern of the RF transistor designer is meeting the requirements for output power, gain, and ruggedness at the specified frequency and supply voltage.

Most RF applications typically require 12.5 or 28 volt operation of a power device in a mobile transmitter, base station, or avionics application. This choice dictates the epitaxial layer resistivity. Low resistivity, about 1 ohm/cm, is used for mobile devices, while 28 V base station and avionics devices are usually built using epi with 2 ohm/cm resistivity. Epi resistivity controls collector breakdown voltage, since the resistivity value determines the maximum possible breakdown voltage. Typically, a particular device rarely achieves this bulk breakdown value because of junction curvature and surface effects. When high voltages are present in an amplifier, high breakdown voltages are needed if the transistor is to survive. High voltage breakdowns are usually obtained by such added features as collector depletion rings, or by a high voltage diffusion surrounding the relatively shallow RF base diffusion. Voltages in excess of 150 volts are easily obtained this way.

Output power is determined primarily by the "electrical size" of the chip. Two common methods of sizing are emitter diffusion periphery and base diffusion area. Emitter periphery sizing is based on the premise that there is some optimum current which should be injected for each mil of emitter periphery. The base area sizing is based on an optimum power density. Both of these techniques are oversimplifications which make it impossible to apply them to widely varying device geometries and applications. Motorola uses a different method of sizing based on each geometry's Current Factor. Current Factor values are obtained by considering both emitter periphery effects and power density. Proper weighting of both factors makes this technique of sizing widely applicable. No matter what sizing technique is chosen, the end result is that greater power-handling capability requires larger chips. Small-signal devices, with only a few milliwatts of output power, and large devices with 100 watts output, range from current factors of only 1 to nearly 2000.

An alternative approach to high output power is to use several smaller chips in parallel. Unless extreme care is taken, this approach can result in unequal current and power sharing. Single large chips are also susceptible to this sharing problem unless specific steps are taken to ensure even current distribution. The primary method of handling this problem is by the use of well-designed emitter resistor layouts. The lowest value of emitter resistance on a chip is chosen to prevent thermal runaway up to the highest temperatures the device may encounter, possibly up to 300°C during output impedance mismatch conditions. An appropriate matrix of emitter resistance values is constructed so that the overall current distribution among the many parallel emitter sites results in an even thermal distribution. Verification of thermal balance is obtained by precise infrared microscope measurements across the entire chip.

The thermal balance of larger chips is also improved considerably by "cell spreading." In this techique the base diffusion area is broken up into smaller areas, or cells, and each cell is sufficiently removed from those adjacent to eliminate thermal interaction. The net effect is to achieve lower thermal resistance. This is exceedingly important in large devices where high power dissipation levels can cause excessive junction temperature when thermal resistance is not minimized. Some symptoms of excessively high temperature operation are low efficiency, power slump, and, frequently, total device failure.

The overall ruggedness of a transistor is enhanced by many techniques. All of them are aimed at preventing two things: junction breakdown due to excessive voltages and failure due to hot-spotting. Here again, epitaxial layer resistivity and thickness are used to alter breakdown voltages and saturated output power. Thermal balancing by base cell spreading and using emitter resistors also has a strong effect on ruggedness. These techniques are commonly referred to as collector and emitter ballasting. Ballasting of either type can improve ruggedness for a fixed geometry size (current factor), but there is a definite trade-off with gain. Usually increasing ruggedness requires decreasing gain unless one is willing to pay the penalty of the cost of larger die.

Large die can also adversely affect gain, since it is a practical fact that gain decreases by 2 dB for each doubling in current factor. To offset this gain decrease, the designer has another technique available—increase the packing denisty within the chip. The most common method of measuring packing density is with the figure of merit obtained

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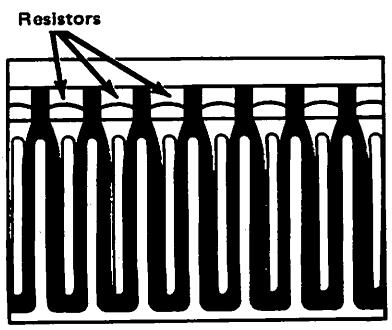
from the *ratio* of emitter periphery (Ep) to base area (B_A) of the chip. Higher Ep/B_A ratios result in higher gain. Typically, Ep/B_A ratios are as shown in the table.

Ep/B_A	FREQUENCY	GEOMETRY TYPE
0.5–1.5	3–30 MHz	Interdigitated
1.5–3.5	VHF	Interdigitated or Spine (Overlay)
3.5–4.5	UHF	Spine (Overlay) or Mesh (Network)
5.5–6.5	800–900 MHz	Mesh

Higher Ep/B_A ratios generally mean greater processing difficulties. These difficulties are somewhat offset by the choice of geometry type. Fundamentally, the interdigitated geometry requires narrow spacing between emitter and base fingers and narrow finger widths. The maximum Ep/B_A ratio obtainable with an interdigitated structure of uniform spacing "S" is given by

$$(Ep/B_A)\ MAX = \frac{0.45}{S}.$$

Spacings of 0.08 mil are the minimum easily obtainable with current technology, giving a maximum figure of merit of 5.6. Actual devices with this spacing are usually about 4.5. Building a large power device using this geometry calls for a great many narrow metallization fingers.



Enlargement of this "interdigitated" geometry shows emitter resistors that have been added to balance the current throughout the chip.

This approach increases the probability of a metallization defect linking adjoining fingers and enhances failures due to metal migration. The spine or mesh geometries used for higher figure of merit do not completely relieve the tight spacing requirements. In both cases, tight metal spacing is relieved while diffusion spacings are not. For example, 4.5 is the maximum Ep/B_A ratio for a 0.1 mil spacing with an interdigitated device. Motorola's family of UHF power devices MRF641 (15 watt), MRF644 (25 watt), MRF646 (45 watt), and MRF648 (60 watt) are constructed using a split mesh (adjoining emitter fingers are not interconnected). All four devices have an Ep/B_A ratio of 4 and are built with a 0.1 mil spacing between adjacent emitter and P+ diffusion areas. Similar tight spacing is required in the mesh geometry used for the 800–900 MHz 7, 20, 30, and 40 watt devices. Here the spacing is reduced to 0.06 mil, using a mesh geometry. Without tight spacing of emitter to P+ such as these devices have, high Ep/B_A ratios will not produce good gain. The introduction of the P+ is required to maintain full utilization of all elements of the emitter periphery. Introducing undulations in the shape of the emitter to increase the periphery without a closely spaced P+ will cause some elements of the periphery to be debiased due to uneven base voltage drops.

The metal migration failure rate as measured by MTBF (Mean Time Before Failure) depends on current density, metallization cross-sectional area, and activation energy. Activation energy may be varied by the choice of metallization with gold and aluminum being the two most common choices. Motorola uses gold metallization for both avionics and 28 volt base station devices where continuous operation is anticipated. Mobile devices are usually constructed of aluminum. In either case, devices are designed for a minimum of 10 years MTBF.

Linear Power

Linear operation is usually accomplished by building the same type of transistor structure as used in Class C operation. The major difference is the linearity requirements force the use of devices with larger current factors. They are also usually fabricated with slightly lower collector resistivity. The combination of these factors allows the device to maintain good linearity with high power output levels. Motorola has led the industry with its family of SSB large-chip transistors, MRF421, MRF422, MRF428. These chips are large, 140 X 250 mils, and have Current Factors approaching 2000. The higher voltage devices are built using a combination of both depletion rings and deep P+ high voltage diffusions. All feature thermal ballasting through emitter resistor matrices.

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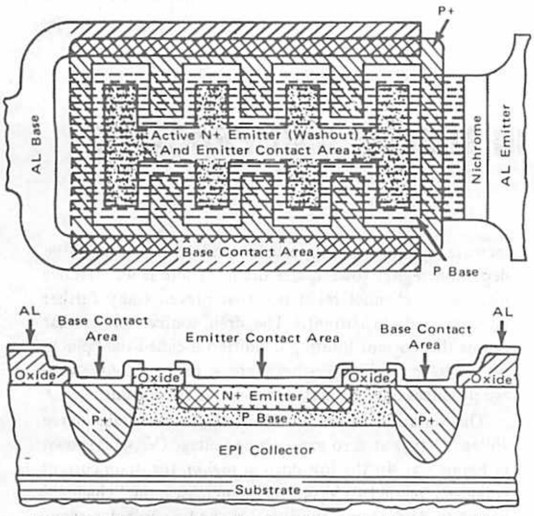
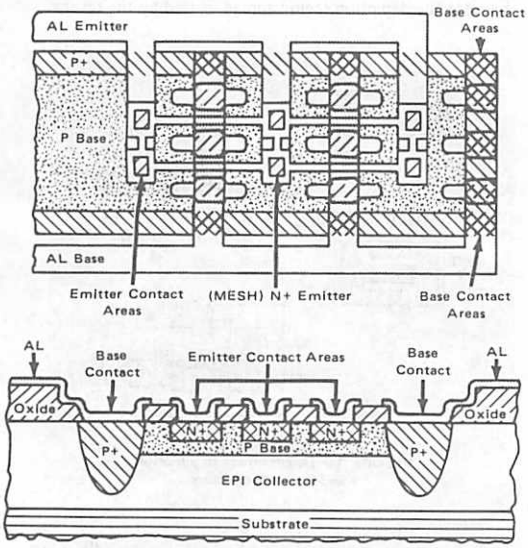


Overlay Structure. Individual emitter cell blocks are diffused into a common base region. Emitter interconnection runs are made over a passivating silicon dioxide layer, reducing the need for critically thin interdigitated metal fingers.



Network Emitter Structure. This structure maximizes emitter periphery to base area ratio but pays for it with increased production difficulty and increased contact resistance.

Motorola employs a thin nichrome barrier (not shown) between the silicon and the aluminum metalization in most network emitter and overlay devices to prevent aluminum metal migration thus improving long-term reliability.

Small Signal

Small-signal devices are constructed from the same types of geometries as used for power devices except on a much smaller scale of Current Factor. The small geometries do not suffer from the gain reduction due to size, allowing the use of lower E_P/B_A ratios for equivalent gain.

Quite commonly, small-signal transistors are not only required to have a minimum gain, but also a minimum f_t. This parameter is a measure of the total emitter-to-collector transit time. As the collector current is increased, the value of f_t increases initially, peaks, and then finally decreases. The peak value is determined by the base and emitter region transit times. This parameter is controlled by both the base junction depth and the emitter doping species. Using conventional diffusion processes with a single base and emitter diffusion, maximum achievable f_t for NPN transistors is about 3-4 GHz without severely degrading the normally desirable dc characteristics, namely BV_{CEO} and h_{FE}.

The logical solution is to use arsenic as the emitter dopant species. Arsenic has an advantage over the more commonly used phosphorus diffusion source. The concentration dependent diffusivity of arsenic causes a very abrupt emitter profile. The increased profile gradient reduces the storage of free carriers in the emitter space charge layer, reducing the layer transit time, and increasing f_t. Unfortunately, arsenic diffusion technology is difficult at best.

The simplest method for using arsenic as a dopant species is to implant it. Motorola has recently introduced transistors with implanted arsenic emitters. These devices have typical f_t of 8 GHz without sacrificing dc characteristics.

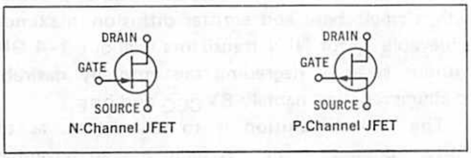
A family of low noise devices has also been fabricated using similar processes. Low noise figure (NF) places additional requirements on both f_t, the doping density of the base under the emitter, and the emitter diffusion width. Through special controlled processing, excellent NF values are obtained in the 1 to 2 GHz region. This performance requires high f_t, low base spreading resistance, and 0.05 mil wide arsenic implanted emitters.

7

FIELD EFFECT TRANSISTORS IN THEORY AND PRACTICE

INTRODUCTION

There are two types of field-effect transistors, the Junction Field-Effect Transistor (JFET) and the "Metal-Oxide Semiconductor" Field-Effect Transistor (MOSFET), or Insulated-Gate Field-Effect Transistor (IGFET). The principles on which these devices operate (current controlled by an electric field) are very similar – the primary difference being in the methods by which the control element is made. This difference, however, results in a considerable difference in device characteristics and necessitates variances in circuit design, which are discussed in this note.



JUNCTION FIELD-EFFECT TRANSISTOR (JFET)

In its simplest form the junction field-effect transistor starts with nothing more than a bar of doped silicon that behaves as a resistor (Figure 1a). By convention, the terminal into which current is injected is called the source terminal, since, as far as the FET is concerned, current originates from this terminal. The other terminal is called the drain terminal. Current flow between source and drain is related to the drain-source voltage by the resistance of the intervening material. In Figure 1b, p-type regions have been diffused into the n-type substrate of Figure 1a leaving an n-type channel between the source and drain. (A complementary p-type device is made by reversing all of the material types.) These p-type regions will be used to control the current flow between the source and the drain and are thus called gate regions.

As with any p-n junction, a depletion region surrounds the p-n junctions when the junctions are reverse biased (Figure 1c). As the reverse voltage is increased, the depletion regions spread into the channel until they meet, creating an almost infinite resistance between the source and the drain.

If an external voltage is applied between source and drain (Figure 1d) with zero gate voltage, drain current flow in the channel sets up a reverse bias along the surface of the gate, parallel to the channel. As the drain-source voltage increases, the depletion regions again spread into the channel because of the voltage drop in the channel which reverse biases the junctions. As V_{DS} is increased, the depletion regions grow until they meet, whereby any further increase in voltage is counterbalanced by an increase in the depletion region toward the drain. There is an effective increase in channel resistance that prevents any further increase in drain current. The drain-source voltage that causes this current limiting condition is called the "pinch-off" voltage (V_p). A further increase in drain-source voltage produces only a slight increase in drain current.

The variation in drain current (I_D) with drain-source voltage (V_{DS}) at zero gate-source voltage (V_{GS}) is shown in Figure 2a. In the low-current region, the drain current is linearly related to V_{DS}. As I_D increases, the "channel" begins to deplete and the slope of the I_D curve decreases. When the V_{DS} is equal to V_p, I_D "saturates" and stays relatively constant until drain-to-gate avalanche, $V_{BR(DSS)}$ is reached. If a reverse voltage is applied to the gates, channel pinch-off occurs at a lower I_D level (Figure 2b) because the depletion region spread caused by the reverse-

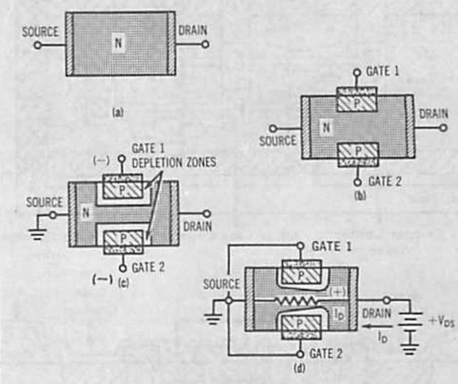


FIGURE 1 – Development of Junction Field-Effect Transistors

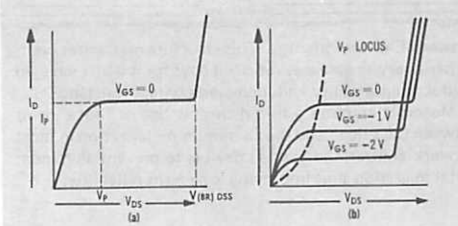
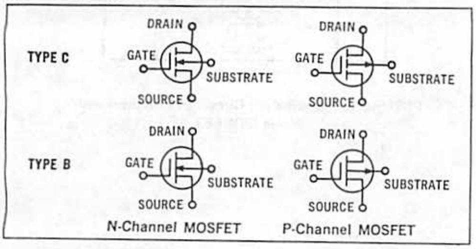


FIGURE 2 – Drain Current Characteristics

biased gates adds to that produced by V_{DS}. Thus reducing the maximum current for any value of V_{DS}.

Due to the difficulty of diffusing impurities into both sides of a semiconductor wafer, a single ended geometry is normally used instead of the two-sided structure discussed above. Diffusion for this geometry (Figure 3) is from one side only. The substrate is of p-type material onto which an n-type channel is grown epitaxially. A p-type gate is then diffused into the n-type epitaxial channel. Contact metalization completes the structure.

The substrate, which functions as Gate 2 of Figure 1, is of relatively low resistivity material to maximize gain. For the same purpose, Gate 1 is of very low resistivity material, allowing the depletion region to spread mostly into the n-type channel. In most cases the gates are internally connected together. A tetrode device can be realized by not making this internal connection.



MOS FIELD-EFFECT TRANSISTORS (MOSFET)

The metal-oxide-semiconductor (MOSFET) operates with a slightly different control mechanism than the JFET. Figure 4 shows the development. The substrate may be high resistivity p-type material, as for the 2N4351. This time two separate low-resistivity n-type regions (source and drain) are diffused into the substrate as shown in Figure 4b. Next, the surface of the structure is covered with an insulating oxide layer and a nitride layer. The oxide layer serves as a protective coating for the FET surface and to insulate the channel from the gate. However the oxide is subject to contamination by sodium ions which are found in varying quantities in all environments. Such contamination results in long term instability and changes in device characteristics. Silicon nitride is impervious to sodium ions and thus is used to shield the oxide layer from contamination. Holes are cut into the oxide and nitride layers allowing metallic contact to the source and drain. Then, the gate metal area is overlayed on the insulation, covering the entire channel region and, simultaneously, metal contacts to the drain and source are made as shown in Figure 4d. The contact to the metal area covering the channel is *the gate terminal.* Note that there is no physical penetration of the metal through the oxide and nitride into the substrate. Since the drain and source are isolated by the substrate, any drain-to-source current in the absence of gate voltage is extremely low because the structure is analogous to two diodes connected back to back.

The metal area of the gate forms a capacitor with the insulating layers and the semiconductor channel. The metal area is the top plate; the substrate material and channel are the bottom plate.

For the structure of Figure 4, consider a positive gate potential (see Figure 5). Positive charges at the metal side of the metal-oxide capacitor induce a corresponding negative charge at the semiconductor side. As the positive charge at the gate is increased, the negative charge "induced" in the semiconductor increases until the region beneath the oxide effectively becomes an n-type semiconductor region, and current can flow between drain and source through the "induced" channel. In other words, drain current flow is "enhanced" by the gate potential. Thus drain current flow can be modulated by the gate voltage; i.e. the channel resistance is directly related to the gate voltage. The n-channel structure may be changed to a p-channel device by reversing the material types.

An equivalent circuit for the MOSFET is shown in Figure 6. Here, $C_{g(ch)}$ is the distributed gate-to-channel

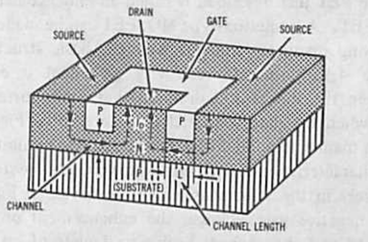


FIGURE 3 – Junction FET with Single-Ended Geometry

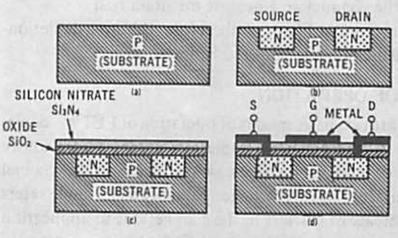


FIGURE 4 – Development of Enhancement-Mode N-Channel MOSFET

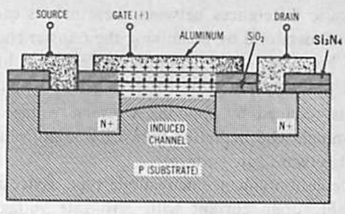


FIGURE 5 – Channel Enhancement. Application of Positive Gate Voltage Causes Redistribution of Minority Carriers in the Substrate and Results in the Formation of a Conductive Channel Between Source and Drain

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capacitance representing the nitride-oxide capacitance. C_{gs} is the gate-source capacitance of the metal gate area overlapping the source, while C_{gd} is the gate-drain capacitance of the metal gate area overlapping the drain. $C_{d(sub)}$ and $C_{s(sub)}$ are junction capacitances from drain to substrate and source to substrate. Y_{fs} is the transadmittance between drain current and gate-source voltage. The modulated channel resistance is r_{ds}. R_D and R_S are the bulk resistances of the drain and source.

The input resistance of the MOSFET is exceptionally high because the gate behaves as a capacitor with very low leakage ($r_{in} \approx 10^{14}\ \Omega$). The output impedance is a function of r_{ds} (which is related to the gate voltage) and the drain and source bulk resistances (R_D and R_S).

To turn the MOSFET "on", the gate-channel capacitance, $C_{g(ch)}$, and the Miller capacitance, C_{gd}, must be charged. In turning "on", the drain-substrate capacitance, $C_{d(sub)}$, must be discharged. The resistance of the substrate determines the peak discharge current for this capacitance.

The FET just described is called an enhancement-type MOSFET. A depletion-type MOSFET can be made in the following manner: Starting with the basic structure of Figure 4, a moderate resistivity n-channel is diffused between the source and drain so that drain current can flow when the gate potential is at zero volts (Figure 7). In this manner, the MOSFET can be made to exhibit depletion characteristics. For positive gate voltages, the structure enhances in the same manner as the device of Figure 4. With negative gate voltage, the enhancement process is reversed and the channel begins to deplete of carriers as seen in Figure 8. As with the JFET, drain-current flow depletes the channel area nearest the drain first.

The structure of Figure 7, therefore, is both a depletion-mode and an enhancement-mode device.

MODES OF OPERATION

There are two basic modes of operation of FET's – depletion and enhancement. Depletion mode, as previously mentioned, refers to the decrease of carriers in the channel due to variation in gate voltage. Enhancement mode refers to the increase of carriers in the channel due to application of gate voltage. A third type of FET that can operate in both the depletion and the enhancement modes has also been described.

The basic differences between these modes can most easily be understood by examining the transfer characteristics of Figure 9. The depletion-mode device has considerable drain-current flow for zero gate voltage. Drain current is reduced by applying a reverse voltage to the gate terminal. The depletion-type FET is not characterized with forward gate voltage.

The depletion/enhancement mode type device also has considerable drain current with zero gate voltage. This type device is defined in the forward region and may have usable forward characteristics for quite large gate voltages. Notice that for the junction FET, drain current may be enhanced by forward gate voltage only until the gate-source p-n junction becomes forward biased.

The third type of FET operates only in the enhancement mode. This FET has extremely low drain current flow for zero gate-source voltage. Drain current conduction occurs for a V_{GS} greater than some threshold value, $V_{GS(th)}$. For gate voltages greater than the threshold, the transfer characteristics are similar to the depletion/enhancement mode FET.

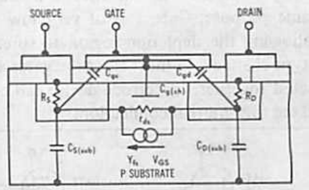

FIGURE 6 – Equivalent Circuit of Enhancement-Mode MOSFET

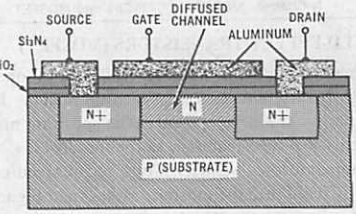

FIGURE 7 – Depletion Mode MOSFET Structure. This Type of Device may be Designed to Operate in Both the Enhancement and Depletion Modes

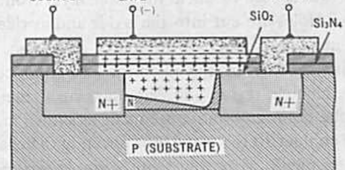

FIGURE 8 – Channel Depletion Phenomenon. Application of Negative Gate Voltage Causes Redistribution of Minority Carriers in Diffused Channel and Reduces Effective Channel Thickness. This Results in Increased Channel Resistance

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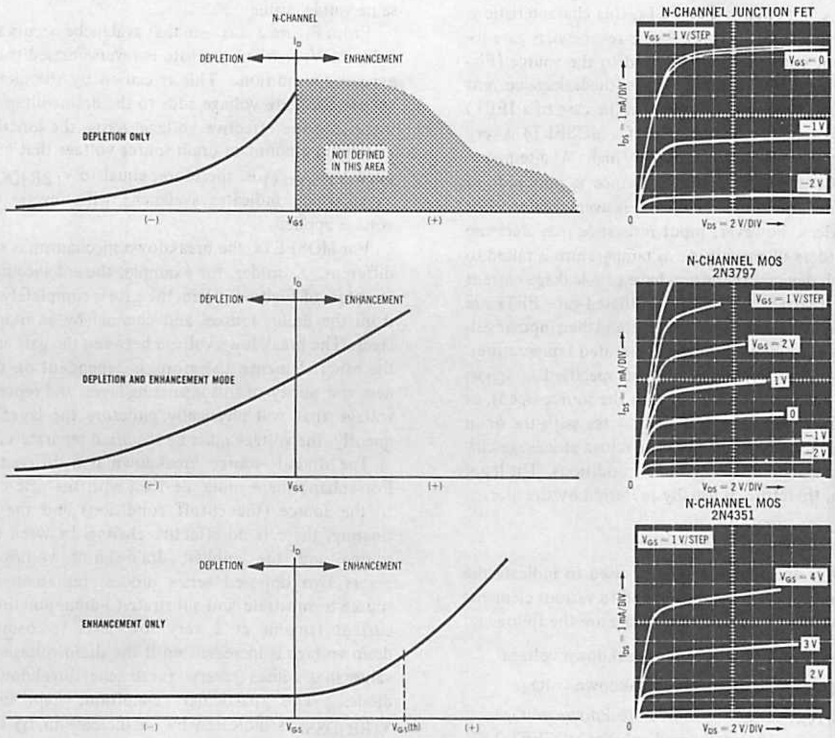


FIGURE 9 – Transfer Characteristics and Associated Scope Traces for the Three FET Types

ELECTRICAL CHARACTERISTICS

Because the basic mode of operation for field-effect devices differs greatly from that of conventional junction transistors, the terminology and specifications are necessarily different. An understanding of FET terminology and characteristics are necessary to evaluate their comparative merits from data-sheet specifications.

Static Characteristics

Static characteristics define the operation of an active device under the influence of applied dc operating conditions. Of primary interest are those specifications that indicate the effect of a control signal on the output current. The V_{GS}–I_D transfer characteristics curves are illustrated in Figure 9 for the three types of FETs. Figure 10 lists the data-sheet specifications normally employed to describe these curves, as well as the test circuits that yield the indicated specifications.

Of additional interest is the special case of tetrode-connected devices in which the two gates are separately accessible for the application of a control signal. The pertinent specifications for a junction tetrode are those which define drain-current cutoff when one of the gates is connected to the source and the bias voltage is applied to the second gate. These are usually specified as $V_{G1S(off)}$, Gate 1 – source cutoff voltage (with Gate 2 connected to source), and $V_{G2S(off)}$, Gate 2 – source cutoff voltage (with Gate 1 connected to source). The gate voltage required for drain current cutoff with one of the gates connected to the source is always higher than that for the triode-connected case where both gates are tied together.

Reach-through voltage is another specification uniquely applicable to tetrode-connected devices. This defines the amount of difference voltage that may be applied to the two gates before the depletion region of one spreads into the junction of the other – causing an increase in gate current to some small specified value. Obviously, reach-through is an undesirable condition since it causes a decrease in input resistance as a result of an increased gate current, and large amounts of reach-through current can destroy the FET.

7

Gate Leakage Current

Of interest to circuit designers is the input resistance of an active component. For FETs, this characteristic is specified in the form of I_{GSS} – the reverse-bias gate-to-source current with the drain shorted to the source (Figure 11). As might be expected, because the leakage current across a reverse-biased p-n junction (in the case of a JFET) and across a capacitor (in the case of a MOSFET) is very small, the input resistance is extremely high. At a temperature of 25°C, the JFET input resistance is hundreds of megohms while that of a MOSFET is even greater. For junction devices, however, input resistance may decrease by several orders of magnitude as temperature is raised to 150°C. Such devices, therefore, have gate-leakage current specified at two temperatures. Insulated-gate FETs are not drastically affected by temperature, and their input resistance remains extremely high even at elevated temperatures.

Gate leakage current may also be specified as I_{GDO} (leakage between gate and drain with the source open), or as I_{GSO} (leakage between gate and source with the drain open). These usually result in lower values of leakage current and do not represent worst-case conditions. The I_{GSS} specification, therefore, is usually preferred by the user.

Voltage Breakdown

A variety of specifications can be used to indicate the maximum voltage that may be applied to various elements of a FET. Among those in common use are the following:

$V_{(BR)GSS}$ = Gate-to-source breakdown voltage

$V_{(BR)DGO}$ = Drain-to-gate breakdown voltage

$V_{(BR)DSX}$ = Drain-to-source breakdown voltage (normally used only for MOSFETs)

In addition, there may be ratings and specifications indicating the maximum voltages that may be applied between the individual gates and the drain and source (for tetrode-connected devices). Obviously, not all of these specifications are found on every data sheet since some of them provide the same information in somewhat different form. By understanding the various breakdown mechanisms, however, the reader should be able to interpret the intent of each specification and rating. For example:

In junction FETs, the maximum voltage that may be applied between any two terminals is the lowest voltage that will lead to breakdown or avalanche of the gate junction. To measure $V_{(BR)GSS}$ (Figure 12a), an increasingly higher reverse voltage is applied between the gate and the source. Junction breakdown is indicated by an increase in gate current (beyond I_{GSS}) which signals the beginning of avalanche.

Some reflection will reveal that for junction FETs, the $V_{(BR)DGO}$ specification really provides the same information as $V_{(BR)GSS}$. For this measurement, an increasing voltage is applied between drain and gate. When this applied voltage becomes high enough, the drain-gate junction will go into avalanche, indicated either by a significant increase in drain current or by an increase in gate current (beyond I_{DGO}). For both $V_{(BR)DGO}$ and $V_{(BR)GSS}$ specifications, breakdown should normally occur at the same voltage value.

From Figure 2 it is seen that avalanche occurs at a lower value of V_{DS} when the gate is reverse biased than for the zero-bias condition. This is caused by the fact that the reverse-bias gate voltage adds to the drain voltage, thereby increasing the effective voltage across the junction. The maximum amount of drain-source voltage that may be applied $V_{DS(max)}$ is, therefore, equal to $V_{(BR)DGO}$ minus V_{GS}, which indicates avalanche with reverse bias gate voltage applied.

For MOSFETs, the breakdown mechanism is somewhat different. Consider, for example, the enhancement-mode structure of Figure 5. Here, the gate is completely insulated from the drain, source, and channel by an oxide-nitride layer. The breakdown voltage between the gate and any of the other elements, therefore, is dependent on the thickness and purity of this insulating layer, and represents the voltage that will physically puncture the layer. Consequently, the voltage must be specified separately.

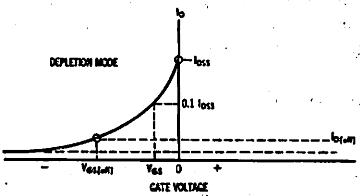
The drain-to-source breakdown is a different matter. For enhancement mode devices, with the gate connected to the source (the cutoff condition) and the substrate floating, there is no effective channel between drain and source and the applied drain-source voltage appears across two opposed series diodes, represented by the source-to-substrate and substrate-to-drain junctions. Drain current remains at a very low level (picoamperes) as drain voltage is increased until the drain voltage reaches a value that causes reverse (avalanche) breakdown of the diodes. This particular condition, represented by $V_{(BR)DSS}$, is indicated by an increase in I_D above the I_{DSS} level, as shown in Figure 12b.

For depletion/enhancement mode devices, the $V_{(BR)DSS}$ symbol is sometimes replaced by $V_{(BR)DSX}$. Note that the principal difference between the two symbols is the replacement of the last subscript s with the subscript x. Whereas the s normally indicates that the gate is shorted to the source, the x indicates that the gate is biased to cutoff or beyond. To achieve cutoff in these devices, a depleting bias voltage must be applied to the gate, Figure 12b.

An important static characteristic for switching FETs is the "on" drain-source voltage $V_{DS(on)}$. This characteristic for the MOSFETs is a function of V_{GS}, and resembles the $V_{CE(sat)}$ versus I_B characteristics of junction transistors. The curve for these characteristics can be used as a design guide to determine the minimum gate voltage necessary to achieve a specified output logic level.

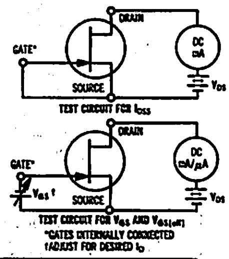
Dynamic Characteristics

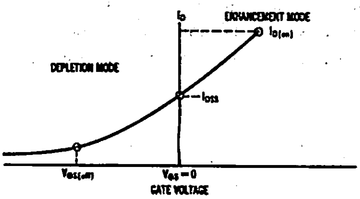
Unlike the static characteristics, the dynamic characteristics of field-effect transistors apply equally to all FETs. The conditions and presentation of the dynamic characteristics, however, depend largely upon the intended application. For example, the following table indicates the dynamic characteristics needed to adequately describe



DEPLETION MODE JFETs

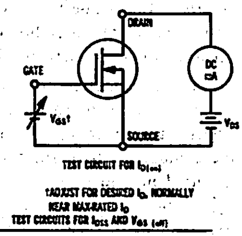
CHARACTERISTIC	DESCRIPTION
I_{DSS} @ $V_{GS} = 0$, $V_P < V_{DS} < V_{(BR)DSS}$	Zero-gate-voltage drain current. Represents maximum drain current.
$V_{GS(off)}$ @ $I_D = 0.001\ I_{DSS}$, $V_P < V_{DS} < V_{(BR)DSS}$	Gate voltage necessary to reduce I_D to some specified negligible value at the recommended V_{DS}, i.e. cutoff.
V_{GS} @ $I_D = 0.1\ I_{DSS}$, $V_P < V_{DS} < V_{(BR)DSS}$	Gate voltage for a specified value of I_D between I_{DSS} and I_D at cutoff – normally $0.1\ I_{DSS}$.

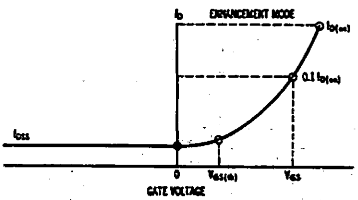




DEPLETION/ENHANCEMENT MODE MOSFETs

CHARACTERISTIC	DESCRIPTION
$I_{D(on)}$ @ $V_{GS} > 0$, $V_P < V_{DS} < V_{(BR)DSS}$	An arbitrary current value (usually near max rated current) that locates a point in the enhancement operating mode.
I_{DSS} @ $V_{GS} = 0$, $V_P < V_{DS} < V_{(BR)DSS}$	Zero-gate-voltage drain current.
$V_{GS(off)}$ @ $I_D = 0.001\ I_{DSS}$	Voltage necessary to reduce I_D to some specified negligible value at the recommended V_{DS}, i.e. cutoff.





ENHANCEMENT MODE MOSFETs

CHARACTERISTIC	DESCRIPTION
$I_{D(on)}$ @ $V_{GS} > 0$, $V_P < V_{DS} < V_{(BR)DSS}$	An arbitrary current value (usually near max rated current) that locates a point in the enhancement operating mode.
V_{GS} @ $0.1\ I_{D(on)}$	Gate-source voltage for a specified drain current of $0.1\ I_{D(on)}$.
$V_{GS(th)}$ @ $I_D = 0.001\ I_{D(on)}$ or less	Gate cutoff or turn-on voltage.
I_{DSS} @ $V_{GS} = 0$, $V_P < V_{DS} < V_{(BR)DSS}$	Leakage drain current.

$I_{D(on)}$ TEST CIRCUIT
SAME AS FOR DEPLETION/ENHANCEMENT
V_{GS} TEST CIRCUIT
SAME AS FOR $I_{D(on)}$
$V_{GS(th)}$ TEST CIRCUIT
SAME AS $V_{GS(off)}$ FOR JFET
EXCEPT REVERSE V_{GS} BATTERY POLARITY
I_{DSS} TEST CIRCUIT
SAME AS FOR JFET

FIGURE 10 – Static Characteristics for the Three FET Types are Defined by the Above Curves, Tables, and Test Circuits

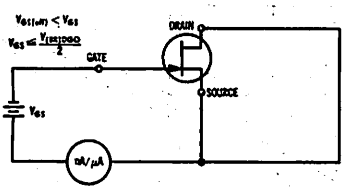


FIGURE 11 – Test Circuit for Leakage Current

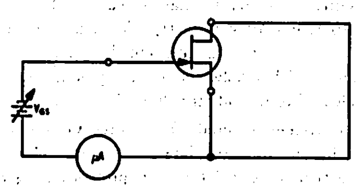


Figure 12a – $V_{(BR)GSS}$ Test Circuit

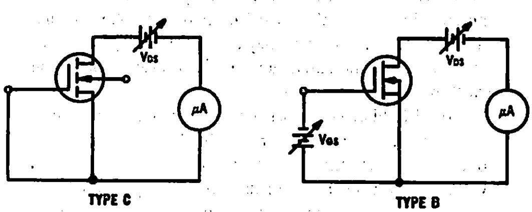


FIGURE 12b – $V_{(BR)DSS}$ and $V_{(BR)DSX}$ Test Circuit (Usually Used for MOSFETs Only).

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Audio	RF-IF	Switching	Chopper
y_{fs} (1 kHz)	y_{fs} (1 kHz)		
C_{iss}	C_{iss}	C_{iss}	C_{iss}
C_{rss}	C_{rss}	C_{rss}	C_{rss}
y_{os} (1 kHz)	GP	$Cd_{(sub)}$	$Cd_{(sub)}$
NF	$Re(y_{is})(HF)$	$r_{ds(on)}$	$r_{ds(on)}$
	$Re(y_{os})(HF)$	t_{d1}, t_{d2}	
	NF	t_r, t_f	

a FET for various applications.

y_{fs} The forward transadmittance is a key dynamic characteristic for field-effect transistors. It serves as a basic design parameter in audio and rf circuits and is a widely accepted figure of merit for devices.

Because field-effect transistors have many characteristics similar to those of vacuum tubes, and because many engineers still are more comfortable with tube parameters, the symbol g_m used for tube transconductance is often specified instead of y_{fs}. To further confuse things, the "g" school also uses a variety of subscripts. In addition to g_m, some data sheets show g_{fs} while others even show g_{21}.

Regardless of the symbol used, y_{fs} defines the relation between an input signal voltage and an output signal current:

$$y_{fs} = \Delta I_D / \Delta V_{GS} \Big|_{V_{DS} = K}$$

The unit is the mho – current divided by voltage. Figure 13 is a typical y_{fs} test circuit for a junction FET.

As a characteristic of all field-effect devices, y_{fs} is specified at 1 kHz with a V_{DS} the same as that for which $I_{D(on)}$ or I_{DSS} is characterized. Since y_{fs} has both real and imaginary components, but is dominated by the real component at low frequency, the 1 kHz characteristic is given as an absolute magnitude and indicated as $|y_{fs}|$.

It is interesting to note that y_{fs} varies considerably with I_D due to nonlinearity in the $I_D - V_{GS}$ characteristics. This variation, for a typical n-channel, JFET is illustrated in Figure 14. Obviously, the operating point must be carefully selected to provide the desired y_{fs} and signal swing.

For tetrode-connected FETs, three y_{fs} measurements are usually specified on data-sheet tables. One of these, with the two gates tied together, provides a y_{fs} value for the condition where a signal is applied to both gates simultaneously; the others provide the y_{fs} for the two gates individually. Generally, with the two gates tied together, y_{fs} is higher and more gain may be realized in a given circuit. Because of the increased capacitance, however, gain-bandwidth product is much lower.

For rf field-effect transistors, an additional value of y_{fs} is sometimes specified at or near the highest frequency of operation. This value should also be measured at the same voltage conditions as those used for $I_{D(on)}$ or I_{DSS}. Because of the importance of the imaginary component at radio frequencies, the high-frequency y_{fs} specification should be a complex representation, and should be given either in the specifications table or by means of curves showing typical variations, as in Figure 15 for the MPF102 JFET.

The real portion of this high-frequency y_{fs}, Re (y_{fs}) or G_{21}, is usually considered a significant figure of merit.

y_{os} Another FET parameter that offers a direct vacuum tube analogy is y_{os}, the output admittance:

$$y_{os} = \Delta I_D / \Delta V_{DS} \Big|_{V_{GS} = K}$$

In this case, the analogous tube parameter is r_p – i.e., $y_{os} = 1/r_p$. For depletion mode devices, y_{os} is measured with gate and source grounded (see Figure 16). For enhancement mode units, it is measured at some specified V_{GS} that permits substantial drain-current flow.

As with y_{fs}, many expressions are used for y_{os}. In

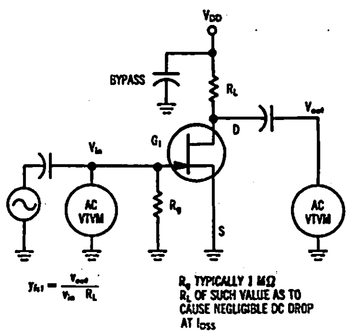

FIGURE 13 – Typical y_{fs} Test Circuit

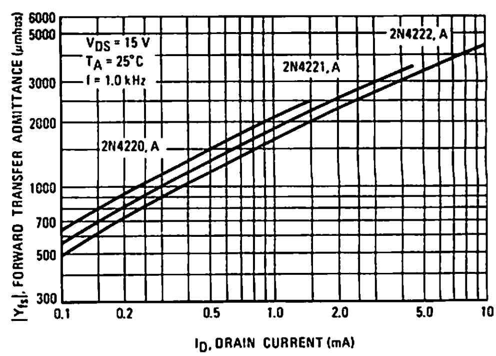

FIGURE 14 – Forward Transfer Admittance versus Drain Current for Typical JFETs

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addition to the obvious parallels such as y_{22}, g_{os}, and g_{22}, it is also sometimes specified as r_d, where $r_d = 1/y_{os}$.

Voltages and frequencies for measuring y_{os} should be *exactly* the same as those for measuring y_{fs}. Like y_{fs}, it is a complex number and should be specified as a magnitude at 1 kHz and in complex form at high frequencies.

μ Closely related to y_{os} and y_{fs} is the amplification factor, μ:

$$\mu = \Delta V_{DS}/\Delta V_{GS} \Big|_{I_D = K}$$

The amplification factor does not appear on the field-effect transistor registration format but can be calculated as y_{fs}/y_{os}. For most small-signal applications, μ has little circuit significance. It does, however, serve as a general indication of the quality of the field-effect manufacturing process.

C_{iss} The common-source-circuit input capacitance, C_{iss}, takes the place of y_{is} in low-frequency field-effect transistors. This is because y_{is} is entirely capacitive at low frequencies. C_{iss} is conveniently measured in the circuit of Figure 17 for the tetrode JFET. As with y_{fs}, two measurements are necessary for tetrode-connected devices.

At very high frequencies, the real component of y_{is} becomes important so that rf field-effect transistors should have y_{is} specified as a complex number at the same conditions as other high-frequency parameters. For tetrode-connected rf FETs, reading of both Gate 2 to source and Gate 1 tied to Gate 2 are necessary.

In switching applications C_{iss} is of major importance since a large voltage swing at the gate must appear across C_{iss}. Thus, C_{iss} must be charged by the input voltage before turn-on effectively begins.

C_{rss} Reverse transfer admittance (y_{rs}) does not appear on FET data sheets. Instead C_{rss}, the reverse transfer capacitance, is specified at low frequency. Since y_{rs} for a field-effect transistor remains almost completely capacitive and relatively constant over the entire usable FET frequency spectrum, the low-frequency capacitance is an adequate specification. C_{rss} is measured by the circuit of Figure 18. For tetrode FETs, values should be specified for Gate 1 and for both gates tied together.

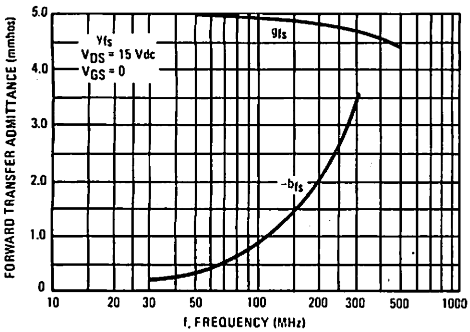

FIGURE 15 – Forward Transfer Admittance versus Frequency

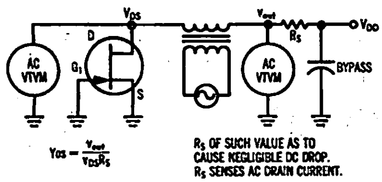

FIGURE 16 – Y_{os} Measurement Circuit for Depletion FETs

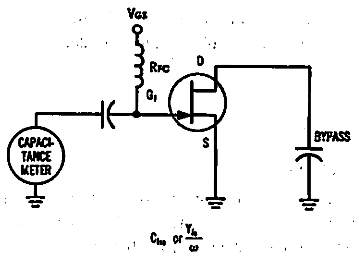

FIGURE 17 – C_{iss} Measurement Circuit

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Again, for switching applications C_{rss} is a critical characteristic. Similar to the C_{ob} of a junction transistor, C_{rss} must be charged and discharged during the switching interval. For a chopper application, C_{rss} is the feedthrough capacitance for the chopper drive.

$C_{d(sub)}$ For the MOSFET, the drain-substrate junction capacitance becomes an important characteristic affecting the switching behavior. $C_{d(sub)}$ appears in parallel with the load in a switching circuit and must be charged and discharged between the two logic levels during the switching interval.

Noise Figure (NF) Like all other active components, field-effect transistors generate a certain amount of noise. The noise figure for field-effect transistors is normally specified on the data sheet as "spot noise", referring to the noise at a particular frequency. The noise figure will vary with frequency and also with the resistance at the input of the device. Typical graphs of such variations are illustrated in Figure 19 for the 2N5458. From graphs of this kind the designer can anticipate the noise level inherent in his design.

$r_{ds(on)}$ Channel resistance describes the bulk resistance of the channel in series with the drain and source. From an applications standpoint, it is important primarily for switching and chopper circuits since it affects the switching speed and determines the output level. To complete the confusion of multiple symbols for FET parameters, channel resistance is sometimes indicated as $r_{d(on)}$ and also as r_{DS} and r_{ds}. In either case, however, it is measured, for JFETs, by tying the gates to the source, setting all terminals equal to 0 Vdc, and applying an ac voltage from drain to source (see Figure 20). The magnitude of the ac voltage should be kept low so that there will be no pinch-off in the channel. Insulated-gate FETs may be measured with dc gate bias in the enhancement mode.

APPLICATIONS

Device Selection

Obviously, different applications call for special emphasis on specific characteristics so that a simple figure of merit that compares devices for all potential uses would be hard to formulate. Nevertheless, an attempt to pinpoint the characteristics that are most significant for various applications has been made* to permit a rapid, first-order evaluation of competitive devices.

The most important single FET parameter, one that applies for any amplifier application, is y_{fs}. This parameter, or one of its many variations, is specified on most data

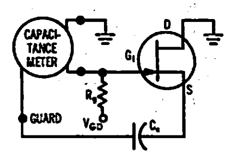

FIGURE 18 — Recommended C_{rss} Test Circuit

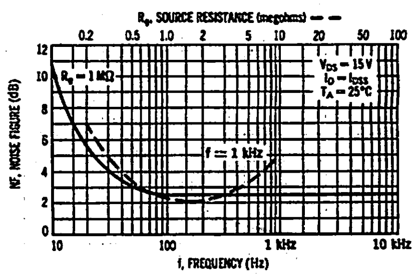

FIGURE 19 — Typical Variations of FET Noise Figure with Frequency and Source Resistance

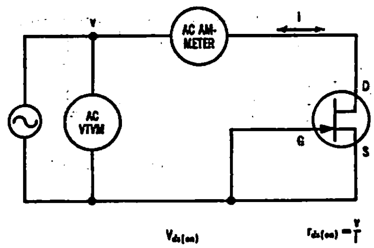

FIGURE 20 — Circuit for Measuring JFET Channel Resistance

*Christiansen, Donald, "Semiconductors: The New Figures of Merit," EEE, October, 1965.

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sheets, yet some evaluation is required to come up with a reasonable comparison. For example, in the table of electrical characteristics on most JFET data sheets, y_{fs} is specified at I_{DSS} ($V_{GS} = 0$) where, for JFETs devices, y_{fs} is maximum. This is illustrated in Figure 14, where typical variations of y_{fs} as a function of I_D are plotted. For some small-signal applications, the I_{DSS} ($V_{GS} = 0$) point can actually be used as a dc operating point because small-signal excursions into the forward bias region will not actually cause the gate-source junction to become forward-biased. However, in most practical uses, some bias is necessary to allow for the anticipated signal swing; and it must be recognized the y_{fs} goes down as the bias is increased.

It is seen, also, that maximum y_{fs} increases as I_{DSS} increases so that, where maximum y_{fs} is important, a device with a high I_{DSS} specification is normally desirable.

On the other hand, where power dissipation is a factor to be considered, the figure of merit $y_{fs}/V_{GS(off)}\ I_{DSS}$ has been proposed. This term factors in not only I_{DSS}, which should be low if power dissipation is to be low, but also $V_{GS(off)}$, which indicates maximum input voltage swing. Since the signal peaks are represented by $V_{GS} = V_{GS(off)}$ and $V_{GS} = 0$, the lower $V_{GS(off)}$, the higher the figure of merit. And, for amplifier applications requiring a large signal swing, $V_{(BR)GSS}/V_{GS(off)}$ (assuming that $V_{GS(off)}$ is the "pinch-off" voltage) is a satisfactory merit figure because it indicates the ratio of maximum and minimum drain voltages.

For high-frequency circuits, the input capacitance (C_{iss}) and the Miller-effect capacitance (C_{rss}) become important, so $y_{fs}/(C_{iss} + C_{rss})$ indicates a relative measure of device performance. For switching and chopper circuits, a figure of merit is not often useful. Here the magnitudes of C_{iss}, C_{rss}, $C_{d(sub)}$ and r_{ds} are of primary interest.

Circuits

The types of circuits that can utilize FETs are practically unlimited. In fact, many circuits designed to utilize small-signal pentode tubes can utilize FETs with only minor modifications. For example, the circuit in Figure 21 shows a typical rf stage for a broadcast-band auto radio. In this circuit, a MPF102 n-channel JFET has replaced the 12BL6 pentode normally employed. The specifications for the two devices, including the AGC characteristics, are similar enough to perform adequately in the circuit of Figure 21.

In an audio application, a field-effect transistor such as the 2N5460 can be combined with a high voltage bipolar transistor to make a simple line-operated phonograph amplifier such as that shown in Figure 22. The ceramic pickup is connected through a potentiometer volume control to the field-effect transistor. Collector current of the transistor, in turn, is set by the potentiometer in the source of the FET. With the proper bipolar output transistor, the circuit can be driven directly from the rectified line voltage, while the low voltage for the FET can be derived from a voltage divider in the power supply line.

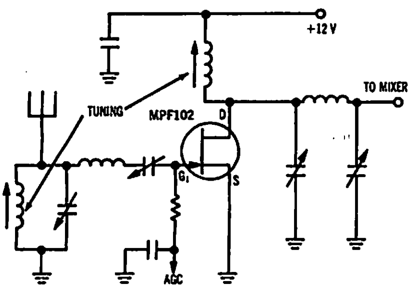

FIGURE 21 — RF Stage of Broadcast Auto Radio

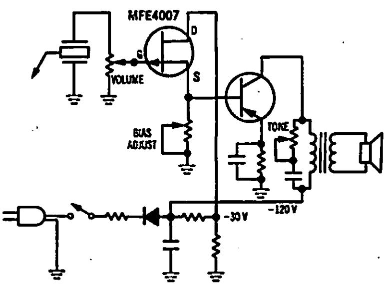

FIGURE 22 — Line Operated Phono Amplifiers

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Figure 23 shows three basic chopper circuits. The advantage of the more complex series-shunt circuit (24c) is that it balances out the leakage currents of the FETs in order to reduce voltage error and is used to attain high chopping frequencies. From an applications standpoint, the FET circuit is superior to a junction transistor circuit in that there is no offset voltage with the FET turned on. On the minus side, however, the field-effect-transistor chopper generally has a higher series resistance ($r_{ds(on)}$) than the junction transistor.

As newer and better FETs are introduced and as a larger number of designers learn to use them, the range of applications of FETs should broaden considerably.

With its high input impedance, the field-effect transistor will play an important role in input circuitry for instrumentation and audio applications where low-impedance junction transistors have generally been least successful.

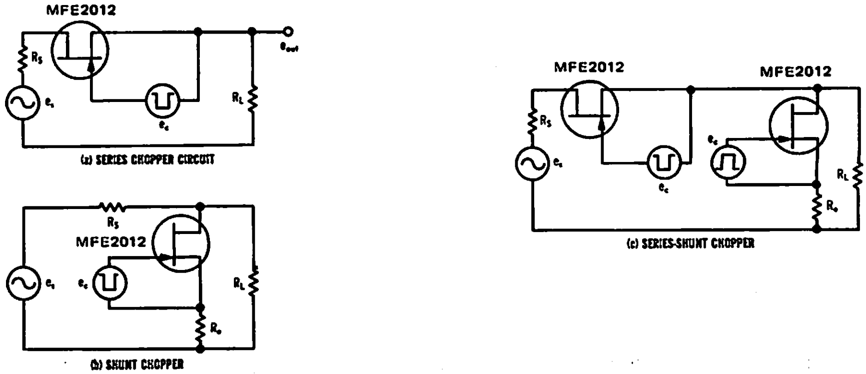

Figure 23 – FET Chopper Circuits

RF SMALL SIGNAL DESIGN USING TWO-PORT PARAMETERS

Prepared by:
Roy Hejhall

INTRODUCTION

Design of the solid-state, small-signal RF amplifier using two-port parameters is a systematic, mathematical procedure, with an exact solution (free from approximation) available for the complete design problem. The only sources of error in the final design are parameter variations resulting from transistor parameter distributions and strays in the physical circuit. Parameter distributions result from limits in measurement and random variations among identically designed transistors.

The purpose of this paper is to provide, in a single working reference, the important relationships necessary for the complete solution of the RF small-signal design problem using two-port parameters.

The major portion of the report presents design equations in terms of admittance parameters. A section on design with scattering parameters is also included.

This paper is based on work by Linvill[1], Stern[2], and others. Those who may wish to consider the derivations of some of the expressions should refer to the bibliography.

This report assumes that the reader is familiar with the two-port parameter method of describing a linear active network. Several references are available on this subject.[1,2,6,8,11,12]

It has also been assumed that a suitable transistor or other active device for the task at hand has been selected, and that two-port parameters are available for the frequency and bias point which will be used. Device selection will not be covered as a separate topic in this report; rather, a thorough understanding of the material in the report should provide the designer with the tools he needs to select transistors for a particular small-signal application.

The equations given in the text of this report are applicable to the common-emitter, common-base, or common-collector configuration, if the applicable set of parameters (common-emitter, common-base, or common-collector parameters) is used. Equations for the conversion of the admittance or hybrid parameters of any configuration to either of the other two configurations of the same parameter set are given in the appendix.

While directed primarily toward circuit design with conventional bipolar transistors, two-port network theory has the advantage of being applicable to any linear active network (LAN). The same design approach and equations may therefore be used with field effect transistors[7,9], integrated circuits[10], or any other device which may be described as a linear active two-port network.

Finally, various parameter interrelationships and other data are given in the Appendix.

GENERAL DESIGN CONSIDERATIONS

Design of the RF small-signal tuned amplifier is usually based on a requirement for a specified power gain at a given frequency. Other design goals may include bandwidth, stability, input-output isolation, and low noise performance. After a basic circuit type is selected, the applicable design equations can be solved.

Circuits may be categorized according to feedback (neutralization, unilateralization, or no feedback), and matching at transistor terminals (circuit admittances either matched or mismatched to transistor input and output admittances). Each of these circuit categories will be discussed, including the applicable design equations and the considerations leading to the selection of a particular configuration.

STABILITY

A major factor in the overall design is the potential stability of the transistor. This may be determined by computing the Linvill stability factor[1] C using the following expression:†

$$C = \frac{|y_{12}\, y_{21}|}{2g_{11}\, g_{22} - \mathrm{Re}\,(y_{12}y_{21})} \qquad (1)$$

When C is less than 1, the transistor is unconditionally stable. When C is greater than 1, the transistor is potentially unstable.

The C factor is a test for stability under a hypothetical worst case condition; that is, with both input and output transistor terminals open circuited. With no external feedback, an unconditionally stable transistor will not oscillate with any combination of source and load. If a transistor is potentially unstable, certain source and load combinations will produce oscillations.

Although the C factor may be used to determine the potential stability of a transistor, the conditions of open circuited source and load which are assumed in the C factor test are not applicable to a practical amplifier.

†Re $(Y_{12}Y_{21})$ = Real part of $(Y_{12}Y_{21})$

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Consequently it is also desirable to compute the relative stability of actual amplifier circuits, and Stern[2] has defined a stability factor k for this purpose. The k factor is similar to the C factor except that it also takes into account finite source and load admittances connected to the transistor. The expression for k is:

$$k = \frac{2\,(g_{11} + G_s)\,(g_{22} + G_L)}{|y_{12}y_{21}| + Re\,(y_{12}y_{21})} \qquad (2)$$

If k is greater than one, the circuit will be stable. If k is less than one, the circuit will be potentially unstable and will very likely oscillate at some frequency.

Note that the C factor simply predicts potential stability of a transistor with an open circuited source and load, while the k factor provides a stability computation for a specific circuit.

Stability considerations will be discussed further in the descriptions of each basic circuit type to follow.

GENERAL DESIGN EQUATIONS

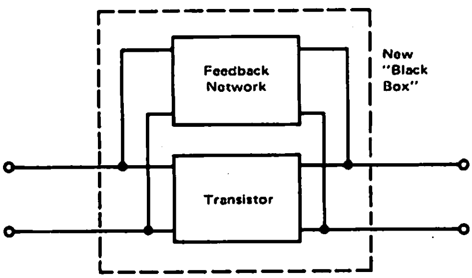
There are a number of design equations which are applicable to most types of amplifiers. These equations will be discussed first. Descriptions of specific amplifier types will then follow, and each will contain additional design equations applicable to that particular amplifier.

POWER GAIN

The general expression for power gain is:

$$G = \frac{|y_{21}|^2\,Re\,(Y_L)}{|Y_L + y_{22}|^2\,Re\,\left(y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L}\right)} \qquad (3)$$

Equation 3 applies to circuits with no external feedback. It can also be used with circuits which have external feedback if the composite y parameters of both the transistor and the feedback network are substituted for the transistor y parameters in the equation. The composite y parameters are determined by considering the transistor and the feedback network to be two "black boxes" in parallel:



For example, the above combination of transistor and feedback network may be characterized as a single "black box" by the following equations:†

$$\begin{aligned} y_{11c} &= y_{11t} + y_{11f} \\ y_{12c} &= y_{12t} + y_{12f} \\ y_{21c} &= y_{21t} + y_{21f} \\ y_{22c} &= y_{22t} + y_{22f} \end{aligned} \qquad (4)$$

Where:

y_{11c}, y_{12c}, y_{21c}, y_{22c} are the composite y parameters of the parallel combination of transistor and feedback network.

y_{11t}, y_{12t}, y_{21t}, y_{22t} are the y parameters of the transistor.

y_{11f}, y_{12f}, y_{21f}, y_{22f} are the y parameters of the feedback network.

Note that, since this approach treats the transistor and feedback network combination as a single "black box" with y_{11c}, y_{12c}, y_{21c}, and y_{22c} as its y parameters, the composite y parameters may therefore be substituted in any of the design equations applicable to a linear, active two-port analysis.

The neutralized and unilateralized amplifiers are special cases of this general concept, and equations associated with those special cases will be given later.

Equation 3 provides a solution for power gain of the linear active network (transistor) only. Input and output networks are considered to be part of the source and load, respectively. Two important points should therefore be kept in mind:

(1) Power gain computed from equation 3 will not take into account network losses. Input network loss reduces power delivered to the transistor. Power lost in the output network is computed as useful power output, since the load admittance Y_L is the combination of the output network and its load.

(2) Power gain is independent of source admittance. An input mismatch results in less input power being delivered to the transistor. Accordingly, note that equation 3 does not contain the term Y_S.

The power gain of a transistor together with its associated input and output networks may be computed by measuring the input and output network losses, and subtracting them from the power gain computed with equation 3.

In some cases it may be desirable to include the effects of input matching in power gain computations. A convenient term is transducer gain G_T, defined as output power delivered to a load by the transistor, divided by the

†Refer to Seshu and Balabanian, "Linear Network Analysis," John Wiley and Sons, 1959, P321

maximum input power available from the source.

The equation for transducer gain is:

$$G_T = \frac{4\,\mathrm{Re}\,(Y_s)\,\mathrm{Re}\,(Y_L)\,|y_{21}|^2}{|(y_{11} + Y_s)(y_{22} + Y_L) - y_{12}y_{21}|^2} \qquad (5)$$

In this equation, Y_L is the composite transistor load admittance-composed of both output network and its load, and Y_S is the composite transistor source admittance-composed of both input network and its source. Therefore, transducer gain includes the effects of the degree of admittance match at the transistor input terminals but does not take into account input and output network losses.

As in equation 3, the composite y parameters of a transistor feedback network combination may be substituted for the transistor y parameters when such a combination is used.

The Maximum Available Gain MAG is an often used transistor figure-of-merit. The MAG is the theoretical power gain of a transistor with its reverse transfer admittance y_{12} set equal to zero, and its source and load admittances conjugately matched to y_{11} and y_{22}, respectively.

If $y_{12} = 0$, the transistor exhibits an input admittance equal to y_{11} and an output admittance equal to y_{22}.†
The equation for MAG is, therefore, obtained by solving the general power gain expression, equation 3, with the conditions

$$y_{12} = 0$$
$$y_L = y_{22}^*$$
$$\text{and } y_s = y_{11}^*$$

where * denotes conjugate

which yields:

$$\mathrm{MAG} = \frac{|y_{21}|^2}{4\,\mathrm{Re}\,(y_{11})\,\mathrm{Re}\,(y_{22})} \qquad (6)$$

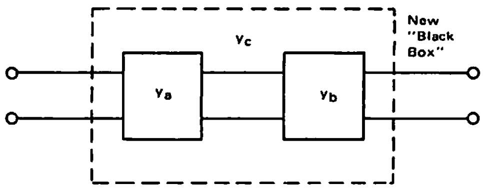
MAG is a figure of merit only, since it is physically impossible to reduce y_{12} to zero without changing the other parameters of the transistor. An external feedback network may be used to achieve a composite y_{12} of zero, but then the other composite parameters will also be modified according to the relationships given in the discussion of the composite transistor – feedback network "black box."

†Obtained by solving the equations for transistor Y_{IN} and Y_{OUT} with y_{12} equal to zero. These equations are given later in the report.

CASCADED LAN'S

Design calculations for cascaded LAN's may be performed by first computing composite two-port parameters as was done in the case of the parallel LAN's.

For the following cascaded LAN's



The composite y parameters are:

$$\begin{aligned} y_{11c} &= y_{11a} - \frac{y_{12a}\,y_{21a}}{y_{22a} + y_{11b}} \\ y_{22c} &= y_{22b} - \frac{y_{12b}\,y_{21b}}{y_{22a} + y_{11b}} \\ y_{21c} &= -\frac{y_{21a}\,y_{21b}}{y_{22a} + y_{11b}} \\ y_{12c} &= -\frac{y_{12a}\,y_{12b}}{y_{22a} + y_{11b}} \end{aligned} \qquad (7)$$

where y_{11c}, y_{22c}, y_{21c}, y_{12c} are the composite y parameters of the cascaded LAN's.

TRANSISTOR INPUT AND OUTPUT ADMITTANCES

The expression for the input admittance of a transistor is:

$$Y_{IN} = y_{11} - \frac{y_{12}\,y_{21}}{y_{22} + Y_L} \qquad (8)$$

The expression for the output admittance of a transistor is:

$$Y_{OUT} = y_{22} - \frac{y_{12}\,y_{21}}{y_{11} + Y_s} \qquad (9)$$

When the feedback parameter y_{12} is not zero, Y_{IN} is dependent on load admittance and Y_{OUT} is dependent on source admittance.

AMPLIFIER STABILITY

One of the major considerations in RF amplifier design is stability. The stability of a final design can be assured by including stability computations and considering stability in all design decisions relating to feedback and transistor source and load admittances.

The potential stability of the transistor should first be computed using equation 1.

The various alternatives concerning input – output matching and neutralization – unilateralization will now be discussed for both the unconditionally stable transistor and the potentially unstable transistor.

THE UNCONDITIONALLY STABLE TRANSISTOR

When the Linvill stability factor of the transistor as determined by equation 1 is less than one, the transistor is unconditionally stable. Oscillations will not occur using any combination of source and load admittances without external feedback. Stability is therefore eliminated as a factor in the remainder of the design, and complete freedom is possible with regard to matching and neutralization to optimize the amplifier for other performance requirements.

AMPLIFIERS WITHOUT FEEDBACK

The amplifier with no feedback is a logical choice for the unconditionally stable transistor in many applications since it may offer the advantages of fewer components and a simple tuning procedure.

Source and load admittances may be selected for maximum gain and/or any number of other requirements. Power gain and transducer gain may be computed using equations 3 and 5, respectively; input and output admittances may be computed using equations 8 and 9, respectively.

The amplifier stability factor may be computed using equation 2. While amplifier stability was assured from the beginning by the use of an unconditionally stable transistor, the designer may still wish to perform this computation to provide some insight into danger of instability under adverse environmental conditions, source and load variations, etc.

G_{max}

G_{max}, the highest transducer gain possible without external feedback, forms a special case of the no feedback amplifier.

The source and load admittances required to achieve G_{max} may be computed from the following:

$$G_s = \frac{1}{2\,\mathrm{Re}(y_{22})}\left|\left[2\,\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21})\right]^2 - \left|y_{12}y_{21}\right|^2\right|^{\frac{1}{2}} \quad (10)$$

$$B_s = -\,\mathrm{Im}(y_{11}) + \frac{\mathrm{Im}(y_{21}y_{12})}{2\,\mathrm{Re}(y_{22})} \quad (11)$$

$$G_L = \frac{1}{2\,\mathrm{Re}(y_{11})}\left|\left[2\,\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21})\right]^2 - \left|y_{12}y_{21}\right|^2\right|^{\frac{1}{2}} \quad (12)$$

$$B_L = -\,\mathrm{Im}(y_{22}) + \frac{\mathrm{Im}(y_{21}y_{12})}{2\,\mathrm{Re}(y_{11})} \quad (13)$$

Therefore, if the maximum possible power gain without feedback is desired for an amplifier, equations 10, 11 12, and 13 are used to compute Y_s and Y_L.

The magnitude of G_{max} may be computed from the following expressions:

$$G_{max} = \frac{|y_{21}|^2}{2\,\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) + \left|\left|2\,\mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21})\right|^2 - \left|y_{12}y_{21}\right|^2\right|^{\frac{1}{2}}} \quad (14)$$

Equations 10, 11, 12, and 13 can be obtained by differentiating equation 5 with respect to G_s, B_s, G_L, and B_L, and setting the four derivatives equal to zero. The G_s, B_s, G_L, and B_L thus computed can then be substituted in equation 5 to obtain the expression for G_{max}, equation 14.

THE LINVILL METHOD

The amplifier without feedback design problem may also be solved graphically using a technique developed by J. G. Linvill.† Linvill's technique is very useful for a certain class of problems. Since it is so fully discussed in many good references, we will not go into it further here. An advantage of the Linvill technique is that it provides a reasonably rapid graphic solution relating gain, bandwidth, and stability. A disadvantage is its scope of usefulness, since the standard Linvill solution applies only to an amplifier with no external feedback and the Y_s conjugately matched to the transistor input admittance, Y_{IN}.

THE UNILATERALIZED AMPLIFIER

Unilateralization consists of employing an external feedback network to achieve a composite y_{12} of zero.

While unilateralization is perhaps most often used to achieve stability with a potentially unstable transistor, other circuit considerations may also warrant the use of unilateralization with the unconditionally stable transistor. For example, the input-output isolation afforded by unilateralization may be desirable in a particular design.

Design equations for the unilateralized case are obtained by first computing the composite y parameters of the transistor – feedback network combination and then substituting the composite parameters in the general equations.

Referring to the discussion on composite y parameters and setting up the basic condition that y_{12c} must equal zero, the other composite y parameters can be computed. Assuming that a passive feedback network is being used, then

$$y_{11f} = y_{22f} = -y_{12f} = -y_{21f}.$$

$$\text{and since } y_{12c} = 0,\; y_{12t} + y_{12f} = 0$$

$$\text{then } y_{12t} = -y_{12f}.$$

$$\text{and } y_{12t} = -y_{12f} = y_{11f} = y_{22f} = -y_{21f}$$

†Application Note AN166 Motorola Semiconductor Products, Inc. Dept. TIC, 5005 E. McDowell Road, Phoenix, Arizona. See also reference 5 in the bibliography.

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Substituting the above results in equations 4 yields the following:

$$y_{11c} = y_{11t} + y_{12t}$$

$$y_{22c} = y_{22t} + y_{12t}$$

$$y_{12c} = y_{12t} - y_{12t} = 0$$

$$y_{21c} = y_{21t} - y_{12t}$$

Substituting these complete y parameters in equations 8, 9, 3, 7, and 5 respectively, yields equations 15, 16, 17 18, and 19 respectively for the unilateralized case.

Unilateralized input admittance

$$Y_{IN} = y_{11} + y_{12} \tag{15}$$

Unilateralized output admittance

$$Y_{OUT} = y_{22} + y_{12} \tag{16}$$

Unilateralized power gain, general expression:

$$G_{PU} = \frac{\left|y_{21} - y_{12}\right|^2 \mathrm{Re}(Y_L)}{\left|Y_L + y_{22} + y_{12}\right|^2 \mathrm{Re}(y_{11})} \tag{17}$$

Unilateralized power gain with Y_L conjugately matched to Y_{OUT}:

$$G_U = \frac{\left|y_{21} - y_{12}\right|^2}{4\,\mathrm{Re}(y_{11} + y_{12})\,\mathrm{Re}(y_{22} + y_{12})} \tag{18}$$

Unilateralized transducer gain:

$$G_{TU} = \frac{4\,\mathrm{Re}(Y_s)\,\mathrm{Re}(Y_L)\left|y_{21} - y_{12}\right|^2}{\left|(y_{11} + y_{12} + Y_s)(y_{22} + y_{12} + Y_L)\right|^2} \tag{19}$$

Note that equations 15, 16, 17, 18 and 19, are given entirely in terms of the transistor y parameters, not those of the feedback network or the composite.

Another benefit of unilateralization is input – output isolation. As can be seen in equations 15 and 16, Y_{IN} is completely independent of Y_L, and Y_{OUT} is similarly independent of Y_S. In a practical sense, this means that in a single or multi-stage amplifier using unilateralized stages, tuning of any one network will not affect tuning in other parts of the circuit. Thus, the troublesome task of having to re-peak an entire amplifier following a change in tuning at a single point can be eliminated.

NEUTRALIZATION

Neutralization consists of employing a feedback network to reduce y_{12} to some value other than zero. Neutralization is generally used for the same purposes as unilateralization, but provides something less than the ideal cancellation of the transistor feedback parameter which unilateralization achieves. A typical example of neutralization might be a feedback network which provides a composite b_{12} of zero while having only a negligible effect on the transistor g_{12}.

The equations for a particular neutralized case would be developed in the same manner as those for the unilateralized case. Since there are an infinite number of possibilities, no specific equations will be given here.

This completes the discussion of design with the unconditionally stable transistor. The potentially unstable transistor will now be considered.

THE POTENTIALLY UNSTABLE TRANSISTOR

When the Linvill stability factor of the transistor as determined by equation 1 is greater than one, the transistor is potentially unstable. Certain combinations of source and load admittances will cause oscillations if no feedback is used. In designing with the potentially unstable transistor, steps must be taken to insure that the amplifier will be stable.

Stability is usually achieved by one or both of two methods:

(1) Using a feedback network which reduces the composite y_{12} to a value which insures stability.

(2) Choosing a source and load admittance combination which provides stability.

A discussion of these basic methods is given below.

USING FEEDBACK TO ACHIEVE STABILITY

Either unilateralization or neutralization may be used to achieve stability. If unilateralization is used, the transistor-feedback network combination will be unconditionally stable. This may be verified by computing the Linvill stability factor of the combination. Since $y_{12c} = 0$, the numerator in equation 1 would be zero.

With stability thus assured, the remainder of the design may then be done to satisfy other requirements placed on the amplifier. After unilateralization has converted the potentially unstable transistor to an unconditionally stable combination, all other aspects of the design are identical to the unilateralized case with the unconditionally stable transistor. Power gains and input and output admittances may be computed using equations 15 through 19.

If neutralization is used to achieve stability, the Linvill stability factor can be used to compute the potential stability of any transistor – neutralization network combination. Since in this case $y_{12c} \neq 0$, C will have a value other than zero.

After unconditional stability of the transistor-neutralization network combination has been achieved, the design may then be completed by treating the combination as an unconditionally stable transistor, and proceeding with the case of the unconditionally stable transistor in an amplifier without feedback. Power gains, input and output admittances, and the circuit stability factor may be computed by using the composite parameters of the combination in equations 2, 3, 5, 8, and 9.

STABILITY WITHOUT FEEDBACK

A stable design with the potentially unstable transistor is possible without external feedback by proper choice of souce and load admittances. This can be seen by inspection of equation 2; G_s and/or G_L can be made large enough to yield a stable circuit regardless of the degree of potential instability of the transistor.

This suggests a relatively simple way to achieve a stable design with a potentially unstable transistor. A circuit stability factor k is selected, and equation 2 is used to arrive at values of G_s and G_L which will provide the desired k. In achieving a particular circuit stability factor, the designer may choose any of the following combinations of matching or mismatching of G_s and G_L to the transistor input and output conductances, respectively:

(1) G_s matched and G_L mismatched
(2) G_L matched and G_s mismatched
(3) Both G_s and G_L mismatched

Often a decision on which combination to use will be dictated by other performance requirements or practical considerations.

Once G_s and G_L have been chosen, the remainder of the design may be completed using the relationships which apply to the amplifier without feedback. Power gain and input and output admittances may be computed using equations 3, 5, 8, and 9.

Although the above procedure may be adequate in many cases, a more systematic method of source and load admittance determination is desirable for designs which demand maximum power gain per degree of circuit stability. Stern has analyzed this problem and developed equations for computing the conductance and susceptance of both Y_s and Y_L for maximum power gain for a particular circuit stability factor.[2,4] These equations are given here:

$$G_s = \sqrt{\frac{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}{2}} \cdot \sqrt{\frac{g_{11}}{g_{22}}} - g_{11} \qquad (20)$$

$$G_L = \sqrt{\frac{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}{2}} \cdot \sqrt{\frac{g_{22}}{g_{11}}} - g_{22} \qquad (21)$$

$$B_s = \frac{(G_s + g_{11})\ Z_o}{\sqrt{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}} - b_{11} \qquad (22)$$

$$B_L = \frac{(G_L + g_{22})\ Z_o}{\sqrt{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}} - b_{22} \qquad (23)$$

Where,

$$Z = \frac{(B_s + b_{11})(G_L + g_{22}) + (B_L + b_{22})\ k(L + M)/2(G_L + g_{22})}{\sqrt{k\ (L + M)}} \qquad (24)$$

$$L = \left|y_{12}y_{21}\right| \qquad (25)$$

$$M = \mathrm{Re}(y_{12}y_{21}) \qquad (26)$$

Defining D as the demoninator in equation 5 yields:

$$D = \frac{Z^4}{4} + \frac{\left[k(L + M) + 2M\right]\ Z^2}{2} - 2NZ\sqrt{k(L + M)} + A^2 + N^2 \qquad (27)$$

where,

$$A = \frac{k(L + M)}{2} - M, \qquad (28)$$

$$N = \mathrm{Im}(y_{12}y_{21}), \qquad (29)$$

and,

Z_o = that real value of Z which results in the smallest minimum of D, found by setting,

$$\frac{dD}{dZ} = Z^3 + \left[k(L + M) + 2M\right] Z - 2N\sqrt{k(L + M)} \qquad (30)$$

equal to zero.

Computation of Y_s and Y_L using equations 20 through 30 is a bit tedious to be done very frequently, and this may have discouraged wide usage of the complete Stern solution. However, examination of Stern's work suggests some interesting shortcuts:

(A) COMPUTATION OF G_s AND G_L ONLY, USING EQUATIONS 20 AND 21. If a value equal to $-b_{22}$ is then chosen for B_L, the resulting Y_L will be very close to the true Y_L for maximum gain. The transistor Y_{IN} can then be computed from Y_L using equation 8, and B_s can be set equal to $-\mathrm{Im}(Y_{IN})$.

Computation of B_s and B_L comprise by far the more complex portion of the Stern solution. This alternate method therefore permits the designer to closely approximate the exact Stern solution for Y_s and Y_L while avoiding that portion of the computations which are the most complex and time consuming. Further, the circuit can be designed with tuning adjustments for varying B_s and B_L, thereby creating the possibility of experimentally achieving the true B_s and B_L for maximum gain as accurately as if all the Stern equations had been solved.

(B) MISMATCHING G_s TO g_{11} AND G_L TO g_{22} BY AN EQUAL RATIO YIELDS A TRUE STERN SOLUTION FOR G_s AND G_L. This can be derived from equations 20 and 21, which lead to the following result:

$$\frac{G_L}{g_{22}} = \frac{G_s}{g_{11}} \qquad (31)$$

If a mismatch ratio, R, is defined as follows,

$$R = \frac{G_L}{g_{22}} = \frac{G_s}{g_{11}} \qquad (32)$$

then R may be computed for any particular circuit stability factor using the equation:

$$(1 + R)^2 = k\left[\frac{\left|y_{21}y_{12}\right| + \mathrm{Re}(y_{12}y_{21})}{2\ g_{11}\ g_{22}}\right] \qquad (33)$$

Equation 33 was derived from equation 2 and 32. Having thus determined R, G_s and G_L can be quickly found using equation 32.

B_s and B_L can then be determined in the manner described above in alternate method (A).

This alternate method may be advantageous if source and load admittances and power gains for several different values of k are desired. Once the R for a particular k has been determined, the R for any other k may be quickly found from the equation

$$\frac{(1 + R_1)^2}{(1 + R_2)^2} = \frac{k_1}{k_2} \tag{34}$$

where R_1 and R_2 are values of R corresponding to k_1 and k_2, respectively.

(C) COMPUTER DESIGN. The complete Stern design problem may be programmed into a computer. Power gain, circuit stability factor, Y_s and Y_L can be obtained from the computer for any value of k. MAG, G_U, and the Linvill stability factor of the transistor may also be included in the program.

After employing either the complete Stern solution or an alternate method to obtain Y_s and Y_L for the potentially unstable transistor in an amplifier without feedback, power gains and input and output admittances may be obtained using equations 3, 5, 8, and 9.

SENSITIVITY

In all but the unilateralized amplifier, Y_{IN} is a function of load admittance. Thus Y_{IN} changes with output circuit tuning, and this can be troublesome. Consequently, it is sometimes desirable to compute the extent of variation of Y_{IN} with changes in Y_L. A term, sensitivity δ, has been defined to provide a measure of this characteristic, and is equal to per cent change in Y_{IN} divided by per cent change in Y_L. The equation for sensitivity is:

$$\delta = \left|\frac{Y_L}{y_{22} + Y_L}\right| \cdot \left|\frac{g_{11}}{y_{11}}\right| \cdot \frac{K}{\left|\frac{y_{22} + Y_L}{g_{22}} + \frac{g_{11}}{y_{11}} K e^{j\theta}\right|} \tag{35}$$

where,

$$K = \left|\frac{y_{21}\, y_{12}}{g_{11}\, g_{22}}\right|$$

$$\theta = \arg(-y_{12}y_{21})$$

$$K e^{j\theta} = K(\cos\theta + j \sin\theta)$$

A more complete discussion of sensitivity is given in reference 6.

DESIGN WITH SCATTERING PARAMETERS

Scattering, or s parameters have greatly increased in popularity since the late 1960's, largely due to the appearance of sophisticated new equipment for performing s parameter measurements.

A summary of s parameter design equations is given below.

Power gain:

$$G = \frac{|s_{21}|^2 (1 - |\Gamma_L|^2)}{(1 - |s_{11}|^2) + |\Gamma_L|^2 (|s_{22}|^2 - |\Delta s|^2) - 2 \operatorname{Re}(\Gamma_L N)} \tag{36}$$

$$\Delta s = s_{11}s_{22} - s_{12}s_{21}$$

$$N = s_{22} - D s^*_{11}$$

Transducer gain:

$$G_T = \frac{|s_{21}|^2 (1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|(1 - s_{11}\Gamma_S)(1 - s_{22}\Gamma_L) - s_{12}s_{21}\Gamma_L\Gamma_S|^2} \tag{37}$$

Input reflection coefficient:

$$s'_{11} = s_{11} + \frac{s_{12}s_{21}\Gamma_L}{1 - s_{22}\Gamma_L} \tag{38}$$

Output reflection coefficient:

$$s'_{22} = s_{22} + \frac{s_{12}s_{21}\Gamma_S}{1 - s_{11}\Gamma_S} \tag{39}$$

Linvill stability factor:

$$C = K^{-1}$$

$$K = \frac{1 + |\Delta s|^2 - |s_{11}|^2 - |s_{22}|^2}{2|s_{12}s_{21}|} \tag{40}$$

$$\Delta s = s_{11}s_{22} - s_{12}s_{21}$$

Equation 40 which gives K, the reciprocal of C, is presented in this form because it is the s parameter stability expression most often seen in the literature. K in equation 40 must not be confused with Stern stability factor k given in equation 2.

Maximum unneutralized transducer gain, unconditionally stable LAN:

$$G_{max} = \left|\frac{s_{21}}{s_{12}}(K \pm \sqrt{K^2 - 1})\right| \tag{41}$$

$$K = C^{-1}$$

C = Linvill Stability Factor

Source and load reflection coefficients for a conjugate match of the unconditionally stable LAN in an amplifier without feedback:

$$\Gamma_{mS} = M^* \left[\frac{B_1 \pm \sqrt{B_1^2 - 4|M|^2}}{2|M|^2}\right] \tag{42}$$

$$\Gamma_{mL} = N^* \left[\frac{B_2 \pm \sqrt{B_2^2 - 4|N|^2}}{2|N|^2}\right] \tag{43}$$

Where $B_1 = 1 + |s_{11}|^2 - |s_{22}|^2 - |\Delta s|^2$

$$B_2 = 1 + |s_{22}|^2 - |s_{11}|^2 - |\Delta s|^2$$

$$M = s_{11} - (\Delta s)(s_{22}^*)$$

$$N = s_{22} - (\Delta s)(s_{11}^*)$$

A more comprehensive treatment of amplifier design with s parameters is given in references 8, 11, and 12.

One cautionary note is in order.

Several papers have been published on the subject of simplifying the s parameter design procedure by making the assumption that the reverse transfer parameter, s_{12}, is equal to zero. This procedure totally ignores the entire

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problem of amplifier stability.

Modern high gain solid-state RF devices will readily oscillate under a wide variety of circuit conditions. Stability problems are encountered even with extremely low feedback devices such as Linear IC's and dual gate MOSFETS. Therefore, amplifier design calculations which do not include device and circuit feedback are only an approximation which will yield either an inaccurate solution or possibly even an oscillator when the design is tested in the laboratory. Reference 13 provides more detail on the shortcomings of this procedure, including an amplifier design example which did turn out to be an oscillator.

SUMMARY OF DESIGN PROCEDURE

A summary of the amplifier design procedure using two-port parameters is given below.

1. Determine the potential instability of the active device.
2. If the device is not unconditionally stable, decide on a course of action to insure circuit stability.
3. Determine whether or not feedback is to be used.
4. Determine source and load admittances.
5. Design appropriate networks to provide the desired source and load admittances.

Stability (Steps 1 and 2 above)

A stability computation for the worst case conditions of open circuit source and load is provided by Linvill's stability factor C. If the C factor indicates unconditional stability, no combination of passive terminations can cause oscillations.

Stability calculations should include the total feedback of the amplifier. In the case of extremely low feedback devices such as dual gate MOSFET's and Linear IC's, external circuit feedback often eclipses the internal device feedback. In such a case, the designer should measure the external circuit feedback and include it in the design calculations. To accomplish this, see the earlier section of this note on the composite parameters of two-port LAN's in parallel.

If the device is unconditionally stable, the design may proceed to fulfill other objectives without fear of oscillations. If the device is potentially unstable, steps must be taken to prevent oscillations in the final design. Stability is achieved by proper selection of source and load admittances, by the use of feedback, or both.

Feedback (Step 3)

Feedback may be employed in the tuned high frequency amplifier to achieve stability, input-output isolation, or to alter the gain and terminal admittances of the active device. A decision to employ feedback would be based on whether or not its use was the optimum way to accomplish one of the foregoing objectives in a particular application.

If feedback is employed, the device parameters may be modified to include the feedback network in accordance with standard two-port network theory. The remainder of the design may then proceed by treating the transistor-feedback network combination as a single, new two-port linear active network.

Source and Load Admittances (Step 4)

Source and load admittance determination is dependent upon gain and stability considerations, together with practical circuit limitations.

If the device is either unconditionally stable itself or has been made stable with feedback, stability need not be a major factor in the determination of source and load. If the device is potentially unstable and feedback is not employed, then a source and load which will guarantee a certain degree of circuit stability must be used. Also, it is a good idea to check the circuit stability factor during this step even when an unconditionally stable device is used.

Finally, practical limitations in matching networks and components may also play an important part of source and load admittance determination.

Network Design (Step 5)

The final step consists of network synthesis to achieve the desired source and load admittances computed in step 4.

Sometimes, it will be difficult to achieve a desired source and load due to tuning range limitations, excess network losses, component limitations, etc. In such cases, the source and load admittances will be a compromise between desired performance and practical limitations.

SUMMARY

The small signal amplifier performance of a transistor is completely described by two-port admittance parameters. Based on these parameters, equations for computing the stability, gain, and optimum source and load admittances for the unilateralized, neutralized, and no-feedback amplifier cases have been discussed.

The unconditionally stable transistor will not oscillate with any combination of source and load admittances, and circuits using a stable transistor may be optimized for other performance requirements without fear of oscillations.

The potentially unstable transistor requires that steps be taken to guarantee a stable design. Stability is usually achieved by unilateralization, neutralization, or selection of source and load admittances which result in a stable amplifier.

Unilateralization and neutralization reduce the composite reverse transfer admittance. They may be used to achieve stability, input – output isolation, or both.

Maximum power gain per degree of circuit stability without feedback may be achieved using Stern's equations.

The degree of input – output isolation is described by the term sensitivity, which makes it possible to compute changes in input admittance for any change in load admittance.

The theory and design equations in this report are applicable to any linear active device which may be characterized as a two-port network. Therefore, the term "transistor" used herein refers generally to all such devices, including FETs and integrated circuits.

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GLOSSARY

C = Linvill's stability factor
k = *Stern's stability factor*
G_s = Real part of the source admittance
G_L = Real part of the load admittance
B_s = Imaginary part of the source admittance
B_L = Imaginary part of the load admittance
g_{11} = Real part of y_{11}
g_{22} = Real part of y_{22}
G = Generalized power gain
Y_L = Complex load admittance
Y_s = Complex source admittance
G_T = Transducer gain
MAG = Maximum available gain
* = Conjugate
Y_{IN} = Input admittance
Y_{OUT} = Output admittance
G_{max} = Maximum gain without feedback
G_U = Unilateralized gain
G_{TU} = Unilateralized transducer gain
δ = Sensitivity
s'_{11} = Input reflection coefficient
s'_{22} = Output reflection coefficient
Γ_L = Load reflection coefficient
Γ_S = Source reflection coefficient
K = Scattering parameter stability factor

APPENDIX I

A. Conversions among parameter types for y, z, h, and g parameters.

h to y

$$y_{11} = \frac{1}{h_{11}} \quad y_{12} = \frac{-h_{12}}{h_{11}} \quad y_{21} = \frac{h_{21}}{h_{11}} \quad y_{22} = \frac{\Delta h}{h_{11}}$$

where $\Delta h = h_{11} h_{22} - h_{12} h_{21}$

y to h

$$h_{11} = \frac{1}{y_{11}} \quad h_{12} = \frac{-y_{12}}{y_{11}} \quad h_{21} = \frac{y_{21}}{y_{11}} \quad h_{22} = \frac{\Delta y}{y_{11}}$$

where $\Delta y = y_{11} y_{22} - y_{12} y_{21}$

h to z

$$z_{11} = \frac{\Delta h}{h_{22}} \quad z_{12} = \frac{h_{12}}{h_{22}} \quad z_{21} = \frac{-h_{21}}{h_{22}} \quad z_{22} = \frac{1}{h_{22}}$$

z to h

$$h_{11} = \frac{\Delta z}{z_{22}} \quad h_{12} = \frac{z_{12}}{z_{22}} \quad h_{21} = \frac{-z_{21}}{z_{22}} \quad h_{22} = \frac{1}{z_{22}}$$

where $\Delta z = z_{11} z_{22} - z_{12} z_{21}$

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h to g

$$g_{11} = \frac{h_{22}}{\Delta h} \qquad g_{12} = \frac{-h_{12}}{\Delta h} \qquad g_{21} = \frac{-h_{21}}{\Delta h} \qquad g_{22} = \frac{h_{11}}{\Delta h}$$

where $\Delta h = h_{11}h_{22} - h_{12}h_{21}$

g to h

$$h_{11} = \frac{g_{22}}{\Delta g} \qquad h_{12} = \frac{-g_{12}}{\Delta g} \qquad h_{21} = \frac{-g_{21}}{\Delta g} \qquad h_{22} = \frac{g_{11}}{\Delta g}$$

where $\Delta g = g_{11}g_{22} - g_{12}g_{21}$

z to y

$$y_{11} = \frac{z_{22}}{\Delta z} \qquad y_{12} = \frac{-z_{12}}{\Delta z} \qquad y_{21} = \frac{-z_{21}}{\Delta z} \qquad y_{22} = \frac{z_{11}}{\Delta z}$$

where $\Delta z = z_{11}z_{22} - z_{12}z_{21}$

y to z

$$z_{11} = \frac{y_{22}}{\Delta y} \qquad z_{12} = \frac{-y_{12}}{\Delta y} \qquad z_{21} = \frac{-y_{21}}{\Delta y} \qquad z_{22} = \frac{y_{11}}{\Delta y}$$

where $\Delta y = y_{11}y_{22} - y_{12}y_{21}$

z to g

$$g_{11} = \frac{1}{z_{11}} \qquad g_{12} = \frac{-z_{12}}{z_{11}} \qquad g_{21} = \frac{z_{21}}{z_{11}} \qquad g_{22} = \frac{\Delta z}{z_{11}}$$

where $\Delta z = z_{11}z_{22} - z_{12}z_{21}$

g to z

$$z_{11} = \frac{1}{g_{11}} \qquad z_{12} = \frac{-g_{12}}{g_{11}} \qquad z_{21} = \frac{g_{21}}{g_{11}} \qquad z_{22} = \frac{\Delta g}{g_{11}}$$

where $\Delta g = g_{11}g_{22} - g_{12}g_{21}$

g to y

$$y_{11} = \frac{\Delta g}{g_{22}} \qquad y_{12} = \frac{g_{12}}{g_{22}} \qquad y_{21} = \frac{-g_{21}}{g_{22}} \qquad y_{22} = \frac{1}{g_{22}}$$

where $\Delta g = g_{11}g_{22} - g_{12}g_{21}$

y to g

$$g_{11} = \frac{\Delta y}{y_{22}} \qquad g_{12} = \frac{y_{12}}{y_{22}} \qquad g_{21} = \frac{-y_{21}}{y_{22}} \qquad g_{22} = \frac{1}{y_{22}}$$

where $\Delta y = y_{11}y_{22} - y_{12}y_{21}$

B. Conversions among common emitter, common base, and common collector parameters of the same type for y, and h parameters.

Common emitter y parameters in terms of common base and common collector y parameters.

$$y_{11e} = y_{11b} + y_{12b} + y_{21b} + y_{22b} = y_{11c}$$

$$y_{12e} = -(y_{12b} + y_{22b}) = -(y_{11c} + y_{12c})$$

$$y_{21e} = -(y_{21b} + y_{22b}) = -(y_{11c} + y_{21c})$$

$$y_{22e} = y_{22b} = y_{11c} + y_{12c} + y_{21c} + y_{22c}$$

Common base y parameters in terms of common emitter and common collector y parameters.

$$y_{11b} = y_{11e} + y_{12e} + y_{21e} + y_{22e} = y_{22c}$$

$$y_{12b} = -(y_{12e} + y_{22e}) = -(y_{21c} + y_{22c})$$

$$y_{21b} = -(y_{21e} + y_{22e}) = -(y_{12c} + y_{22c})$$

$$y_{22b} = y_{22e} = y_{11c} + y_{12c} + y_{21c} + y_{22c}$$

Common collector y parameters in terms of common emitter and common base y parameters.

$$y_{11c} = y_{11e} = y_{11b} + y_{12b} + y_{21b} + y_{22b}$$

$$y_{12c} = -(y_{11e} + y_{12e}) = -(y_{11b} + y_{21b})$$

$$y_{21c} = -(y_{11e} + y_{21e}) = -(y_{11b} + y_{12b})$$

$$y_{22c} = y_{11e} + y_{12e} + y_{21e} + y_{22e} = y_{11b}$$

Common emitter h parameters in terms of common base and common collector h parameters.

$$h_{11e} = \frac{h_{11b}}{(1 + h_{21b})(1 - h_{12b}) + h_{22b}h_{11b}} \approx \frac{h_{11b}}{1 + h_{21b}} = h_{11c}$$

$$h_{12e} = \frac{h_{11b}h_{22b} - h_{12b}(1 + h_{21b})}{(1 + h_{21b})(1 - h_{12b}) + h_{22b}h_{11b}} \approx \frac{h_{11b}h_{22b}}{1 + h_{21b}} - h_{12b} = 1 - h_{12c}$$

$$h_{21e} = \frac{-h_{21b}(1 - h_{12b}) - h_{22b}h_{11b}}{(1 + h_{21b})(1 - h_{12b}) + h_{22b}h_{11b}} \approx \frac{-h_{21b}}{1 + h_{21b}} = -(1 + h_{21c})$$

$$h_{22e} = \frac{h_{22b}}{(1 + h_{21b})(1 - h_{12b}) + h_{22b}h_{11b}} \approx \frac{h_{22b}}{1 + h_{21b}} = h_{22c}$$

Common has h parameters in terms of common emitter and common collector h parameters.

$$h_{11b} = \frac{h_{11e}}{(1 + h_{21e})(1 - h_{12e}) + h_{11e}h_{22e}} \approx \frac{h_{11e}}{1 + h_{21e}}$$

$$= \frac{h_{11c}}{h_{11c}h_{22c} - h_{21c}h_{12c}} \approx \frac{-h_{11c}}{h_{21c}}$$

$$h_{12b} = \frac{h_{11e}h_{22e} - h_{12e}(1 + h_{21e})}{(1 + h_{21e})(1-h_{12e}) + h_{11e}h_{22e}} \approx \frac{h_{11e}h_{22e}}{1 + h_{21e}} - h_{12e}$$

$$= \frac{h_{21c}(1-h_{12c}) + h_{11c}h_{22c}}{h_{11c}h_{22c} - h_{21c}h_{12c}} \approx (h_{12c} - 1) - \frac{h_{11c}h_{22c}}{h_{21c}}$$

$$h_{21b} = \frac{-h_{21e}(1-h_{12e}) - h_{11e}h_{22e}}{(1 + h_{21e})(1-h_{12e}) + h_{11e}h_{22e}} \approx \frac{-h_{21e}}{1 + h_{21e}}$$

$$= \frac{h_{12c}(1 + h_{21c}) - h_{11c}h_{22c}}{h_{11c}h_{22c} - h_{21c}h_{12c}} \approx \frac{-(1 + h_{21c})}{h_{21c}}$$

$$h_{22b} = \frac{h_{22e}}{(1 + h_{21e})(1-h_{12e}) + h_{11e}h_{22e}} \approx \frac{h_{22e}}{1 + h_{21e}}$$

$$= \frac{h_{22c}}{h_{11c}h_{22c} - h_{21c}h_{12c}} \approx \frac{h_{22c}}{h_{21c}}$$

Common collector h parameters in terms of common base and common emitter h parameters.

$$h_{11c} = \frac{h_{11b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b}h_{11b}} \approx \frac{h_{11b}}{1 + h_{21b}} = h_{11e}$$

$$h_{12c} = \frac{1 + h_{21b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b}h_{11b}} \approx 1 \approx 1-h_{12e}$$

$$h_{21c} = \frac{h_{12b} - 1}{(1 + h_{21b})(1-h_{12b}) + h_{22b}h_{11b}} \approx \frac{-1}{1 + h_{21b}} = -(1 + h_{21e})$$

$$h_{22c} = \frac{h_{22b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b}h_{11b}} \approx \frac{h_{22b}}{1 + h_{21b}} = h_{22e}$$

Expressions for voltage gain, current gain, input impedance, and output impedance in terms of y, z, h, and g parameters.

Voltage Gain

$$A_V = \frac{z_{21}Z_L}{\Delta z + z_{11}Z_L} = \frac{-y_{21}}{y_{22} + Y_L} = \frac{-h_{21}Z_L}{h_{11} + \Delta h Z_L} = \frac{g_{21}Z_L}{g_{22} + Z_L}$$

$$= \frac{S_{21}(1 + \Gamma_L)}{(1 - S_{22}\Gamma_L)(1 + S'_{11})}$$

Current Gain

$$A_I = \frac{-z_{21}}{z_{22} + Z_L} = \frac{-y_{21}Y_L}{\Delta y + y_{11}Y_L} = \frac{h_{21}Y_L}{h_{22} + Y_L} = \frac{-g_{21}}{\Delta g + g_{11}Z_L}$$

Input Impedance

$$Z_{IN} = \frac{\Delta z + z_{11}Z_L}{z_{22} + Z_L} = \frac{y_{22} + Y_L}{\Delta y + y_{11}Y_L} = \frac{\Delta h + h_{11}Y_L}{h_{22} + Y_L}$$

$$= \frac{g_{22} + Z_L}{\Delta g + g_{11}Z_L}$$

Output Impedance

$$Z_{OUT} = \frac{\Delta z + z_{22}Z_s}{z_{11} + Z_s} = \frac{y_{11} + Y_s}{\Delta y + y_{22}Y_s} = \frac{h_{11} + Z_s}{\Delta h + h_{22}Z_s}$$

$$= \frac{\Delta g + g_{22}Y_s}{g_{11} + Y_s}$$

Conversion between y parameters and s (scattering) parameters:

$$s_{11} = \frac{(1-y_{11})(1+y_{22}) + y_{12}y_{21}}{(1+y_{11})(1+y_{22}) - y_{12}y_{21}} \dagger$$

$$s_{12} = \frac{-2y_{12}}{(1+y_{11})(1+y_{22}) - y_{12}y_{21}} \dagger$$

$$s_{21} = \frac{-2y_{21}}{(1+y_{11})(1+y_{22}) - y_{12}y_{21}} \dagger$$

$$s_{22} = \frac{(1+y_{11})(1-y_{22}) + y_{21}y_{12}}{(1+y_{11})(1+y_{22}) - y_{12}y_{21}} \dagger$$

$$y_{11} = \left[\frac{(1+s_{22})(1-s_{11}) + s_{12}s_{21}}{(1+s_{11})(1+s_{22}) - s_{12}s_{21}}\right]\frac{1}{Z_o}$$

$$y_{12} = \left[\frac{-2s_{12}}{(1+s_{11})(1+s_{22}) - s_{12}s_{21}}\right]\frac{1}{Z_o}$$

$$y_{21} = \left[\frac{-2s_{21}}{(1+s_{11})(1+s_{22}) - s_{12}s_{21}}\right]\frac{1}{Z_o}$$

$$y_{22} = \left[\frac{(1+s_{11})(1-s_{22}) + s_{12}s_{21}}{(1+s_{22})(1+s_{11}) - s_{12}s_{21}}\right]\frac{1}{Z_o}$$

where Z_O= the characteristic impedance of the transmission lines used in the scattering parameter system, usually 50 ohms.

Conversion between h parameters and s parameters:

$$s_{11} = \frac{(h_{11}-1)(h_{22}+1) - h_{12}h_{21}}{(h_{11}+1)(h_{22}+1) - h_{12}h_{21}} \dagger\dagger$$

$$s_{12} = \frac{2h_{12}}{(h_{11}+1)(h_{22}+1) - h_{12}h_{21}} \dagger\dagger$$

$$s_{21} = \frac{-2h_{21}}{(h_{11}+1)(h_{22}+1) - h_{12}h_{21}} \dagger\dagger$$

$$s_{22} = \frac{(1+h_{11})(1-h_{22}) + h_{12}h_{21}}{(h_{11}+1)(h_{22}+1) - h_{12}h_{21}} \dagger\dagger$$

$$h_{11} = \left[\frac{(1+s_{11})(1+s_{22}) - s_{12}s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}s_{21}}\right]Z_o$$

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$$h_{12} = \frac{2s_{12}}{(1-s_{11})(1+s_{22}) + s_{12}\,s_{21}}$$

$$h_{21} = \frac{-2s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}\,s_{21}}$$

$$h_{22} = \left[\frac{(1-s_{22})(1-s_{11}) - s_{12}\,s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}\,s_{21}}\right]\frac{1}{Z_o}$$

---

†In converting from y to s parameters, the y parameters must first be multiplied by Z_o, and then substituted in the equations for conversion to s parameters.

††In converting from h to s parameters, the h parameters must first be normalized to Z_o in the following manner and then substituted in the equations for conversion to s parameters:

Parameter	To Normalize
h_{11}	divide by Z_o
h_{12}	use as is
h_{21}	use as is
h_{22}	multiply by Z_o

Conversion between z parameters and s parameters:

$$z_{11} = \left[\frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}\right] Z_o$$

$$z_{12} = \left[\frac{2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}\right] Z_o$$

$$z_{21} = \left[\frac{2S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}\right] Z_o$$

$$z_{22} = \left[\frac{(1+S_{22})(1-S_{11}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}\right] Z_o$$

$$s_{11} = \frac{(Z_{11}-1)(Z_{22}+1) - Z_{12}Z_{21}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}} \quad †††$$

$$s_{12} = \frac{2Z_{12}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}} \quad †††$$

$$s_{21} = \frac{2Z_{21}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}} \quad †††$$

$$s_{22} = \frac{(Z_{11}+1)(Z_{22}-1) - Z_{12}Z_{21}}{(Z_{11}+1)(Z_{22}+1) - Z_{12}Z_{21}} \quad †††$$

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†††In converting from z to s parameters, the z parameters must first be divided by Z_o, and then substituted in the equations for conversion to s parameters.

MATCHING NETWORK DESIGNS WITH COMPUTER SOLUTIONS

Prepared by:
Frank Davis

INTRODUCTION

One of the problems facing the circuit design engineer is the design of high-frequency matching networks. Careful design of a network that will accomplish the required matching, harmonic attenuation, bandwidth, etc., and yield components of practical size can result in many hours spent with pencil and slide rule.

The design of matching networks for high frequency circuits involves an infinite number of possibilities, and a complete tabulation of possible network solutions would be virtually impossible. However, it is often necessary to design matching networks with a 50 + j 0 ohm impedance at one port. This, combined with a restricted range of impedance values to be matched, imposed by network and device limitations, makes practical a tabulation of some of the more commonly used networks. These design solutions are given in this report.

The network solutions included in this report have the limitation that one terminating impedance must be 50 + j 0 ohms. These networks are often used for matching in transistor RF power amplifier circuits that have a 50-ohm source or load. When the network does not have a 50-ohm termination at either port, the mathematical procedure given for each network in Appendix I can be used for the solution.

COMPONENT CONSIDERATIONS

Four networks are presented in this report with solutions in the form of computer tabulations. Each network has its own limitations. Although the network configuration is normally up to the discretion of the design engineer, it is sometimes necessary to use one configuration in preference to another in order to obtain component values that are more realistic from a practical standpoint.

Component selection in the UHF and VHF frequency ranges becomes a major problem, and the network configuration to obtain realistic component values is of vital importance to the design engineer. Design calculations for matching networks can become completely meaningless unless the components for the network are measured at the operating frequency.

For example, a 100 pF silver mica capacitor that meets all specifications at 1 MHz can have as much capacitance as 300 pF at 100 MHz. At some frequency, the capacitor's series lead inductance will finally tune out the capacitance, thus leaving the capacitor net inductive.

Values of inductance in the low nanohenry range are also difficult to obtain, since the inductance of a one-inch straight piece of #20 solid tinned wire is approximately 20 nH.

Component tolerances have no meaning at VHF frequencies and above unless they are specified at the operating frequency. It cannot be over-emphasized that components must be measured at the operating frequency.

NETWORK SOLUTIONS

The resistor and capacitor shown in the box labeled "device to be matched" represent the complex input or output impedance of a transistor. These complex impedances have been represented in series form in some cases and parallel form in others, depending on which form is most convenient for network calculation. The resultant impedance of the network, when terminated with 50 + j 0 ohms, must be equal to the conjugate of the impedance in the box. The computer tabulations provide this solution.

Network A (see Figure 1) is applicable only when the "device to be matched" has a series real part of less than 50 ohms. As we can see from the computer tabulation, as the series real part approaches 50 ohms, the reactance of C_1 approaches infinity. However, in RF power amplifiers, we normally find that the series real part of both the input and the output is less than 50 ohms, making this matching network applicable to most RF power amplifier stages. Where the terminating impedance is other than 50 ohms, the mathematical procedure for the network solution is given in Appendix I.

Network B (see Figure 2) is the Pi network widely used in vacuum tube transmitters. As is apparent from the computer tabulation, this network is often impractical for use where R_1 is small. For values of R_1 less than 50 ohms, the inductance of L becomes impractically small while the capacitance of both C_1 and C_2 become very large. Where the Pi network configuration must be used to match low values of impedance, a double Pi network, in which the Q of the first section is very low, can be utilized to yield practical components.

Network C has been solved in two forms (see Figure 3). Both of these networks have the limitation that R_1 must be less than 50 ohms. However, it must be stressed that this network configuration quite often yields the most practical components where low values of R_1 must be matched.

Network D (see Figure 4) is a "Tee" network. This network is useful for matching impedance less than or greater than 50 ohms. It has been observed in laboratory tests that this network configuration also yields very high collector efficiencies when used for output matching in transistor RF power amplifier stages.

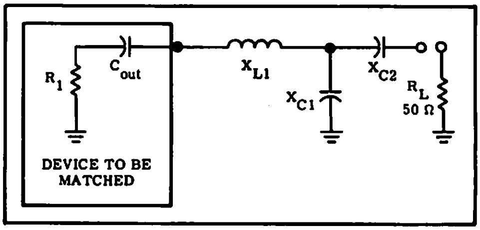

FIGURE 1 — NETWORK A

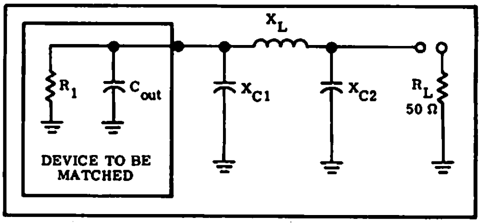

FIGURE 2 — NETWORK B

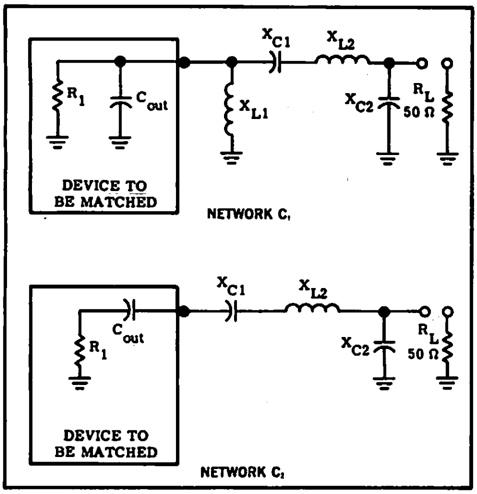

FIGURE 3

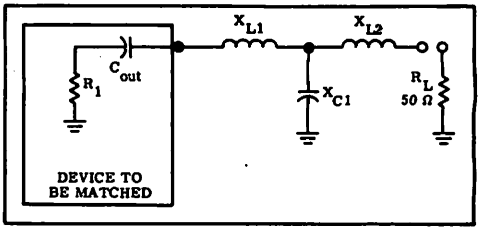

FIGURE 4 — NETWORK D

SUMMARY

Four computer-solved networks have been presented. The mathematical procedure for the solution of each network has been given in Appendix I.* Although the networks have found major use in matching solid-state RF power amplifier stages, they are also applicable to any circuit where the individual network's limitations are fulfilled.

*For the derivation of the equations used, refer to Electronic Circuit Analysis, Volume 1, "Passive Networks," Philip Cutler.

APPENDIX I

To convert a parallel resistance and reactance combination to series:

$$R_s = \frac{R_p}{1 + (R_p/X_p)^2}$$

$$X_s = R_s \frac{R_p}{X_p}$$

To convert a series resistance and reactance combination to parallel:

$$R_p = R_s[1 + (X_s/R_s)^2]$$

$$X_p = \frac{R_p}{X_s/R_s}$$

<u>To solve network A:</u>

1. Select a Q

$$X_{L1} = QR_1 + X_{C\,out}$$

$$X_{C2} = A R_L$$

$$X_{C1} = \frac{(B/A)(B/Q)}{(B/A)-(B/Q)} = \frac{B}{Q - A}$$

$$\text{where } A = \sqrt{\left[\frac{R_1(1+Q^2)}{R_L}\right] - 1}$$

$$B = R_1(1 + Q^2)$$

<u>To solve network B:</u>

1. Select a Q

$$X_{C1} = R_1/Q$$

$$X_{C2} = R_L\sqrt{\frac{R_1/R_L}{(Q^2+1)-(R_1/R_L)}}$$

$$X_L = \frac{QR_1 + (R_1R_L/X_{C2})}{Q^2 + 1}$$

<u>To solve network C_1:</u>

1. Select a Q

$$X_{L1} = X_{C\,out}$$

$$X_{C1} = QR_1$$

$$X_{C2} = R_L\sqrt{\frac{R_1}{R_L - R_1}}$$

$$X_{L2} = X_{C1} + \left(\frac{R_1R_L}{X_{C2}}\right)$$

<u>To solve network C_2:</u>

1. Select a Q
2. L_1 is not used in this network

$$X_{C1} = QR_1$$

$$X_{C2} = R_L\sqrt{\frac{R_1}{R_L - R_1}}$$

$$X_{L2} = X_{C1} + \left(\frac{R_1R_L}{X_{C2}}\right) + X_{C\,out}$$

<u>To solve network D:</u>

1. Select a Q

$$X_{L1} = (R_1Q) + X_{C\,out}$$

$$X_{L2} = R_L B$$

$$X_{C1} = \frac{(A/Q)(A/B)}{(A/Q)+(A/B)} = \frac{A}{Q + B}$$

$$\text{where } A = R_1(1 + Q^2)$$

$$B = \sqrt{\left(\frac{A}{R_L}\right) - 1}$$

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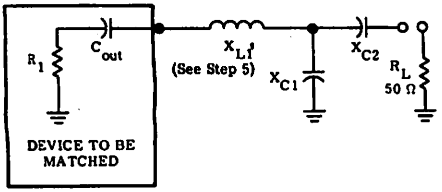
NETWORK A



TO DESIGN A NETWORK USING THE TABLES

1. Transform the parallel impedance of the device to be matched to series form ($R_1 + jX_{C_{out}}$).
2. Define Q, in column one, as X_{L1}/R_1.
3. Choose a Q.
4. For a Q, find the R_s to be matched in the R column and read the reactive value of the components.
5. X_{L1}' is equal to the quantity X_{L1} obtained from the tables plus $|X_{C_{out}}|$.
6. This completes the network.

Q	X_{L1}	X_{C1}	X_{C2}	R_1
1	26	65	10	26
1	27	75.3	14.14	27
1	28	85.68	17.32	28
1	29	96.66	20	29
1	30	108.5	22.36	30
1	32	136	26.46	32
1	34	170	30	34
1	36	213.8	33.16	36
1	38	272.5	36.05	38
1	40	355	38.7	40
1	42	479	41.23	42
1	44	686.32	43.59	44
1	46	1102	45.83	46
1	48	2351	48	48
2	22	32.7	15.8	11
2	24	38.6	22.4	12
2	26	45	27.4	13
2	28	51.2	31.6	14
2	30	58	35.4	15
2	32	65.3	38.7	16
2	34	73.1	41.8	17
2	36	81.4	44.7	18
2	38	90.3	47.4	19
2	40	100	50	20
2	42	110.4	52.4	21
2	44	122	55	22
2	46	134	57	23
2	48	147	59	24
2	50	161	61	25
2	52	177	63	26
2	54	194	65	27
2	56	213	67	28
2	58	233	69	29
2	60	256	71	30
2	64	310	74	32
2	68	377	77	34
2	72	464	81	36
2	76	582	84	38
2	80	746	87	40
2	84	995	89	42
2	88	1409	92	44
2	92	2241	95	46
2	96	4739	97	48
3	18	23.5	22.3	6
3	21	29.6	31.6	7
3	24	35.9	38.7	8
3	27	42.7	44.7	9
3	30	50	50	10
3	33	57.8	54.8	11
3	36	66	59	12
3	39	75	63.2	13

Q	X_{L1}	X_{C1}	X_{C2}	R_1
3	42	84	67	14
3	45	95	71	15
3	48	105	74	16
3	51	117	77	17
3	54	130	81	18
3	57	143	84	19
3	60	158	87	20
3	63	173	89	21
3	66	190	92	22
3	69	209	95	23
3	72.	228	97	24
3	75	250	100	25
3	78	274	102	26
3	81	299	105	27
3	84	327	107	28
3	87	358	110	29
3	90	393	112	30
3	96	473	116	32
3	102	575	120	34
3	108	706	124	36
3	114	882	128	38
3	120	1129	132	40
3	126	1502	136	42
3	132	2124	140	44
3	138	3372	143	46
3	144	7119	146	48
4	12	13.2	7.1	3
4	16	20	30	4
4	20	26.9	41.8	5
4	24	34.2	51	6
4	28	42.1	58.7	7
4	32	50.6	66	8
4	36	60	72	9
4	40	69	77	10
4	44	80	83	11
4	48	91	88	12
4	52	103	92	13
4	56	115	97	14
4	60	129	101	15
4	64	144	105	16
4	68	159	109	17
4	72	176	113	18
4	76	194	117	19
4	80	214	120	20
4	84	235	124	21
4	88	257	127	22
4	92	282	131	23
4	96	308	134	24
4	100	337	137	25
4	104	368	140	26
4	108	403	143	27

Q	X_{L1}	X_{C1}	X_{C2}	R_1
4	112	440	146	28
4	116	482	149	29
4	120	527	152	30
4	128	635	157	32
4	136	770	162	34
4	144	945	168	36
4	152	1180	173	38
4	160	1510	177	40
4	168	2007	182	42
4	176	2837	187	44
4	184	4500	191	46
4	192	9497	196	48
5	10	10.8	10	2
5	15	18.3	37.4	3
5	20	26.3	52	4
5	25	34.8	63.2	5
5	30	44	73	6
5	35	54	81	7
5	40	65	89	8
5	45	76	96	9
5	50	88	102	10
5	55	101	108	11
5	60	115	114	12
5	65	130	120	13
5	70	146	125	14
5	75	163	130	15
5	80	181	135	16
5	85	201	140	17
5	90	222	145	18
5	95	245	149	19
5	100	269	153	20
5	105	295	157	21
5	110	323	162	22
5	115	354	166	23
5	120	387	169	24
5	125	423	173	25
5	130	462	177	26
5	135	505	181	27
5	140	553	184	28
5	145	604	188	29
5	150	662	191	30
5	160	796	198	32
5	170	965	204	34
5	180	1184	210	36
5	190	1477	217	38
5	200	1890	222	40
5	210	2510	228	42
5	220	3548	234	44
5	230	5628	239	46
5	240	11874	245	48

7

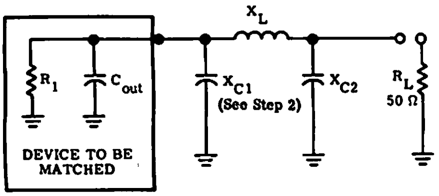
Q	X_{L1}	X_{C1}	X_{C2}	R_1
6	12	13.9	34.6	2
6	18	22.7	55.2	3
6	24	32.2	70	4
6	30	42.5	82	5
6	36	53.6	93	6
6	42	65.5	102	7
6	48	78	110	8
6	54	92	119	9
6	60	107	126	10
6	66	122	133	11
6	72	139	140	12
6	78	157	147	13
6	84	176	153	14
6	90	197	159	15
6	96	219	165	16
6	102	242	170	17
6	108	267	175	18
6	114	295	181	19
6	120	324	186	20
6	126	355	191	21
6	132	389	195	22
6	138	426	200	23
6	144	466	205	24
6	150	509	209	25
6	156	556	214	26
6	162	608	218	27
6	168	664	222	28
6	174	727	226	29
6	180	795	230	30
6	192	957	238	32
6	204	1160	246	34
6	216	1422	253	36
6	228	1775	260	38
6	240	2270	267	40
6	252	3015	274	42
6	264	4260	281	44
6	276	6755	287	46
6	288	14250	294	48
7	14	16.7	50	2
7	21	26.8	71	3
7	28	38	87	4
7	35	50	100	5
7	42	63	112	6
7	49	77	122	7
7	56	92	132	8
7	63	108	141	9
7	70	125	150	10
7	77	143	158	11
7	84	163	166	12
7	91	184	173	13
7	98	206	180	14
7	105	230	187	15
7	112	256	193	16
7	119	283	200	17
7	126	313	206	18
7	133	344	212	19
7	140	379	218	20
7	147	415	224	21
7	154	455	229	22
7	161	498	234	23
7	168	544	239	24
7	175	595	245	25
7	182	650	250	26

Q	X_{L1}	X_{C1}	X_{C2}	R_1
7	189	710	255	27
7	196	776	260	28
7	203	849	265	29
7	210	929	269	30
7	224	1117	278	32
7	238	1354	287	34
7	252	1661	296	36
7	266	2071	304	38
7	280	2649	312	40
7	294	3518	320	42
7	308	4971	328	44
7	322	7882	335	46
7	336	16626	343	48
8	8	8.7	27.4	1
8	16	19.3	63.2	2
8	24	31	85	3
8	32	43.6	102	4
8	40	57.4	117	5
8	48	72	130	6
8	56	88	142	7
8	64	105	153	8
8	72	124	164	9
8	80	143	173	10
8	88	164	182	11
8	96	187	191	12
8	104	211	199	13
8	112	236	207	14
8	120	264	215	15
8	128	293	222	16
8	136	324	230	17
8	144	358	237	18
8	152	394	243	19
8	160	433	250	20
8	168	475	256	21
8	176	521	263	22
8	184	570	269	23
8	192	623	275	24
8	200	681	281	25
8	208	744	286	26
8	216	812	292	27
8	224	888	297	28
8	232	971	303	29
8	240	1062	308	30
8	256	1277	318	32
8	272	1548	329	34
8	288	1899	338	36
8	304	2368	348	38
8	320	3028	357	40
8	336	4022	366	42
8	352	5682	375	44
8	368	9009	383	46
9	9	10	40	1
9	18	21.9	76	2
9	27	35	99	3
9	36	49.4	118	4
9	45	65	134	5
9	54	82	149	6
9	63	100	162	7
9	72	119	174	8
9	81	139	185	9
9	90	162	196	10
9	99	185	206	11

Q	X_{L1}	X_{C1}	X_{C2}	R_1
9	108	210	216	12
9	117	237	225	13
9	126	266	234	14
9	135	297	243	15
9	144	330	251	16
9	153	365	259	17
9	162	403	267	18
9	171	444	275	19
9	180	488	282	20
9	189	535	289	21
9	198	586	296	22
9	207	641	303	23
9	216	701	310	24
9	225	766	316	25
9	234	837	323	26
9	243	914	329	27
9	252	999	335	28
9	261	1092	341	29
9	270	1196	347	30
9	288	1438	359	32
9	306	1743	370	34
9	324	2137	381	36
9	342	2665	391	38
9	360	3407	402	40
9	378	4525	412	42
9	396	6393	422	44
10	10	11.2	50.5	1
10	20	24.5	87	2
10	30	39	112	3
10	40	55	133	4
10	50	72	151	5
10	60	91	167	6
10	70	111	181	7
10	80	132	195	8
10	90	155	207	9
10	100	180	219	10
10	110	206	230	11
10	120	234	241	12
10	130	264	251	13
10	140	296	261	14
10	150	330	271	15
10	160	367	280	16
10	170	406	289	17
10	180	448	297	18
10	190	494	306	19
10	200	543	314	20
10	210	595	322	21
10	220	652	330	22
10	230	713	337	23
10	240	780	345	24
10	250	852	352	25
10	260	930	359	26
10	270	1016	366	27
10	280	1111	373	28
10	290	1214	379	29
10	300	1329	383	30
10	320	1598	399	32
10	340	1937	411	34
10	360	2375	423	36
10	380	2961	435	38
10	400	3787	446	40
10	420	5029	458	42
10	440	7104	469	44

NETWORK B

The following is a computer solution for the Pi network when R_L equals 50 ohms.



TO DESIGN A NETWORK USING THE TABLES

1. Define Q, in column one, as R_1/X_{C1}.
2. C_1 actual is equal to C_1 – parallel C_{out} of device to be matched.
3. This completes the network.

Q	X_{C1}	X_{C2}	X_L	R_1
1	1	5.03	5.47	1
1	2	7.14	8	2
1	3	8.79	10.03	3
1	4	10.21	11.8	4
1	5	11.47	13.4	5
1	10	16.67	20	10
1	15	21	25.35	15
1	20	25	30	20
1	25	28.87	34.15	25
1	30	32.73	37.91	30
1	35	36.69	41.35	35
1	40	40.82	44.49	40
1	45	45.23	47.37	45
1	50	50	50	50
1	55	55.28	52.37	55
1	60	61.24	54.49	60
1	65	68.14	56.35	65
1	70	76.38	57.91	70
1	75	86.6	59.15	75
1	80	100	60	80
1	85	119.02	60.35	85
1	90	150	60	90
2	0.5	3.17	3.56	1
2	1	4.49	5.25	2
2	1.5	5.51	6.64	3
2	2	6.38	7.87	4
2	2.5	7.14	9	5
2	5	10.21	13.8	10
2	7.5	12.63	17.87	15
2	10	14.74	21.56	20
2	12.5	16.67	25	25
2	15	18.46	28.25	30
2	17.5	20.17	31.35	35
2	20	21.82	34.33	40
2	22.5	23.43	37.21	45
2	25	25	40	50
2	27.5	26.55	42.71	55
2	30	28.1	45.35	60
2	32.5	29.64	47.93	65
2	35	31.18	50.45	70
2	37.5	32.73	52.91	75
2	40	34.3	55.32	80
2	42.5	35.89	57.69	85
2	45	37.5	60	90
2	47.5	39.14	62.27	95
2	50	40.82	64.49	100
2	62.5	50	75	125
2	75	61.24	84.49	150
2	87.5	76.38	92.91	175
2	100	100	100	200
2	112.5	150	105	225

Q	X_{C1}	X_{C2}	X_L	R_1
3	0.33	2.24	2.53	1
3	0.67	3.17	3.76	2
3	1	3.88	4.76	3
3	1.33	4.49	5.65	4
3	1.67	5.03	6.47	5
3	3.33	7.14	10	10
3	5	8.79	13.03	15
3	6.67	10.21	15.8	20
3	8.33	11.47	18.4	25
3	10	12.63	20.87	30
3	11.67	13.72	23.26	35
3	13.33	14.74	25.56	40
3	15	15.72	27.81	45
3	16.67	16.67	30	50
3	18.33	17.58	32.14	55
3	20	18.46	34.25	60
3	21.67	19.33	36.32	65
3	23.33	20.17	38.35	70
3	25	21	40.35	75
3	26.67	21.82	42.33	80
3	28.33	22.63	44.28	85
3	30	23.43	46.21	90
3	31.67	24.22	48.12	95
3	33.33	25	50	100
3	41.67	28.87	59.12	125
3	50	32.73	67.91	150
3	58.33	36.69	76.35	175
3	66.67	40.82	84.49	200
3	75	45.23	92.37	225
3	83.33	50	100	250
4	6.25	8.7	14.33	25
4	12.5	12.5	23.53	50
4	18.75	15.55	31.83	75
4	25	18.26	39.64	100
4	31.25	20.76	47.12	125
4	37.5	23.15	54.36	150
4	43.75	25.46	61.39	175
4	50	27.74	68.27	200
4	56.25	30	75	225
4	62.5	32.27	81.61	250
4	75	36.93	94.48	300
4	100	47.14	119.07	400
4	125	59.76	142.25	500
4	150	77.46	163.96	600
4	175	108.01	183.77	700
4	200	200	200	800
5	0.2	1.39	1.58	1
5	5	7	11.67	25
5	10	10	19.23	50
5	15	12.37	26.08	75

Q	X_{C1}	X_{C2}	X_L	R_1
5	20	14.43	32.55	100
5	25	16.31	38.78	125
5	30	18.06	44.82	150
5	35	19.72	50.72	175
5	40	21.32	56.5	200
5	45	22.87	62.18	225
5	50	24.4	67.78	250
5	60	27.39	78.76	300
5	80	33.33	100	400
5	100	39.53	120.48	500
5	120	46.29	140.31	600
5	140	54.01	159.54	700
5	160	63.25	178.17	800
5	180	75	196.15	900
5	200	91.29	213.37	1000
5	220	117.26	229.58	1100
5	240	173.21	244.09	1200
6	0.17	1.16	1.32	1
6	4.17	5.85	9.83	25
6	8.33	8.33	16.22	50
6	12.5	10.28	22.02	75
6	16.67	11.95	27.52	100
6	20.83	13.46	32.82	125
6	25	14.85	37.97	150
6	29.17	16.16	43.01	175
6	33.33	17.41	47.96	200
6	37.5	18.61	52.83	225
6	41.67	19.76	57.63	250
6	50	22	67.08	300
6	66.67	26.26	85.45	400
6	83.33	30.43	103.29	500
6	100	34.64	120.7	600
6	116.67	39.01	137.76	700
6	133.33	43.64	154.5	800
6	150	48.67	170.94	900
6	166.67	54.23	187.08	1000
6	183.33	60.55	202.93	1100
6	200	67.94	218.46	1200
6	216.67	76.87	233.66	1300
6	233.33	88.19	248.48	1400
6	250	103.51	262.83	1500
6	266.67	126.49	276.55	1600
6	283.33	168.33	289.32	1700
6	300	300	300	1800
7	0.14	1	1.14	1
7	3.57	5.03	8.47	25
7	7.14	7.14	14	50
7	10.71	8.79	19.03	75
7	14.29	10.21	23.8	100
7	17.86	11.47	28.4	125

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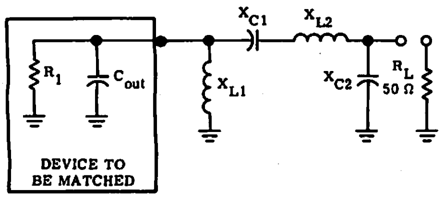
Q	X_{C1}	X_{C2}	X_L	R_1
7	21.43	12.63	32.87	150
7	25	13.72	37.26	175
7	28.57	14.74	41.56	200
7	32.14	15.72	45.81	225
7	35.71	16.67	50	250
7	42.86	18.46	58.25	300
7	57.14	21.82	74.33	400
7	71.43	25	90	500
7	85.71	28.1	105.35	600
7	100	31.18	120.45	700
7	114.29	34.3	135.32	800
7	128.57	37.5	150	900
7	142.86	40.82	164.49	1000
7	171.43	48.04	192.98	1200
7	200	56.41	220.82	1400
7	228.57	66.67	248	1600
7	257.14	80.18	274.45	1800
7	285.71	100	300	2000
7	314.29	135.4	324.25	2200
7	342.86	244.95	345.8	2400
8	0.13	0.88	1	1
8	3.13	4.4	7.45	25
8	6.25	6.25	12.31	50
8	9.38	7.68	16.74	75
8	12.5	8.91	20.94	100
8	15.63	10	25	125
8	18.75	11	28.95	150
8	21.88	11.93	32.82	175
8	25	12.8	36.63	200
8	28.13	13.64	40.38	225
8	31.25	14.43	44.09	250
8	37.5	15.94	51.4	300
8	50	18.73	65.66	400
8	62.5	21.32	79.58	500
8	75	23.79	93.25	600
8	87.5	26.2	106.71	700
8	100	28.57	120	800
8	112.5	30.94	133.14	900
8	125	33.33	146.15	1000
8	150	38.25	171.82	1200
8	175	43.5	197.07	1400
8	200	49.24	221.92	1600
8	225	55.71	246.39	1800
8	250	63.25	270.48	2000
8	275	72.37	294.15	2200
8	300	84.02	317.36	2400
9	8.33	6.83	14.93	75
9	11.11	7.91	18.69	100
9	13.89	8.87	22.32	125
9	16.67	9.74	25.85	150
9	19.44	10.56	29.31	175
9	22.22	11.32	32.72	200
9	25	12.05	36.08	225
9	27.78	12.74	39.4	250
9	33.33	14.05	45.95	300
9	44.44	16.44	58.74	400
9	55.56	18.63	71.24	500
9	66.67	20.7	83.53	600
9	77.78	22.69	95.64	700
9	88.89	24.62	107.62	800
9	100	26.52	119.48	900
9	111.11	28.4	131.23	1000
9	133.33	32.16	154.46	1200
9	155.56	36	177.37	1400
9	177.78	40	200	1600
9	200	44.23	222.37	1800
9	222.22	48.8	244.5	2000
9	244.44	53.8	266.4	2200
9	266.67	59.41	288.05	2400

Q	X_{C1}	X_{C2}	X_L	R_1
10	0.1	0.7	0.8	1
10	5	5	9.9	50
10	10	7.11	16.87	100
10	15	8.75	23.34	150
10	20	10.15	29.55	200
10	25	11.41	35.6	250
10	30	12.57	41.52	300
10	40	14.66	53.11	400
10	50	16.57	64.44	500
10	60	18.36	75.58	600
10	70	20.06	86.58	700
10	80	21.69	97.46	800
10	90	23.28	108.24	900
10	100	24.85	118.94	1000
10	120	27.91	140.09	1200
10	140	30.97	161	1400
10	160	34.05	181.68	1600
10	180	37.21	202.17	1800
10	200	40.49	222.47	2000
10	220	43.93	242.61	2200
10	240	47.58	262.59	2400
12	25	10.39	34.79	300
12	33.33	12.08	44.52	400
12	41.67	13.61	54.05	500
12	50	15.02	63.43	600
12	58.33	16.35	72.7	700
12	66.67	17.61	81.87	800
12	75	18.82	90.97	900
12	83.33	20	100	1000
12	100	22.27	117.89	1200
12	116.67	24.46	135.6	1400
12	133.33	26.61	153.15	1600
12	150	28.73	170.57	1800
12	166.67	30.86	187.86	2000
12	183.33	33	205.06	2200
12	200	35.17	222.15	2400
12	216.67	37.39	239.16	2600
12	233.33	39.66	256.07	2800
12	250	42.01	272.9	3000
12	291.67	48.3	314.64	3500
12	333.33	55.47	355.9	4000
12	375	63.96	396.67	4500
12	416.67	74.54	436.92	5000
12	458.33	88.64	476.57	5500
12	500	109.54	515.44	6000
14	21.43	8.86	29.91	300
14	28.57	10.29	38.3	400
14	35.71	11.56	46.51	500
14	42.86	12.73	54.6	600
14	50	13.83	62.59	700
14	57.14	14.87	70.51	800
14	64.29	15.86	78.37	900
14	71.43	16.81	86.17	1000
14	85.71	18.62	101.63	1200
14	100	20.35	116.95	1400
14	114.29	22.02	132.15	1600
14	128.57	23.64	147.24	1800
14	142.86	25.24	162.25	2000
14	157.14	26.81	177.17	2200
14	171.43	28.38	192.02	2400
14	185.71	29.94	206.81	2600
14	200	31.51	221.54	2800
14	214.29	33.09	236.21	3000
14	250	37.12	272.66	3500
14	285.71	41.34	308.82	4000
14	321.43	45.86	344.7	4500
14	357.14	50.77	380.33	5000
14	392.86	56.22	415.69	5500
14	428.57	62.42	450.79	6000

Q	X_{C1}	X_{C2}	X_L	R_1
16	18.75	7.73	26.23	300
16	25	8.96	33.59	400
16	31.25	10.06	40.8	500
16	37.5	11.07	47.9	600
16	43.75	12	54.93	700
16	50	12.88	61.89	800
16	56.25	13.72	68.79	900
16	62.5	14.52	75.65	1000
16	75	16.05	89.26	1200
16	87.5	17.48	102.74	1400
16	100	18.86	116.12	1600
16	112.5	20.18	129.42	1800
16	125	21.47	142.64	2000
16	137.5	22.73	155.8	2200
16	150	23.96	168.9	2400
16	162.5	25.18	181.95	2600
16	175	26.39	194.96	2800
16	187.5	27.59	207.92	3000
16	218.75	30.59	240.16	3500
16	250	33.61	272.18	4000
16	281.25	36.71	304.01	4500
16	312.5	39.9	335.66	5000
16	343.75	43.25	367.15	5500
16	375	46.8	398.49	6000
18	16.67	6.86	23.35	300
18	22.22	7.94	29.9	400
18	27.78	8.91	36.33	500
18	33.33	9.79	42.66	600
18	38.89	10.61	48.92	700
18	44.44	11.38	55.13	800
18	50	12.11	61.28	900
18	55.56	12.8	67.4	1000
18	66.67	14.12	79.54	1200
18	77.78	15.35	91.57	1400
18	88.89	16.52	103.51	1600
18	100	17.65	115.38	1800
18	111.11	18.73	127.2	2000
18	122.22	19.79	138.95	2200
18	133.33	20.81	150.66	2400
18	144.44	21.82	162.33	2600
18	155.56	22.81	173.96	2800
18	166.67	23.79	185.55	3000
18	194.44	26.2	214.4	3500
18	222.22	28.57	243.08	4000
18	250	30.94	271.6	4500
18	277.78	33.33	300	5000
18	305.56	35.76	328.27	5500
18	333.33	38.25	356.44	6000
20	15	6.16	21.03	300
20	20	7.13	26.94	400
20	25	8	32.73	500
20	30	8.78	38.44	600
20	35	9.51	44.09	700
20	40	10.19	49.69	800
20	45	10.84	55.24	900
20	50	11.46	60.76	1000
20	60	12.62	71.71	1200
20	70	13.7	82.57	1400
20	80	14.72	93.35	1600
20	90	15.7	104.07	1800
20	100	16.64	114.73	2000
20	110	17.55	125.35	2200
20	120	18.44	135.93	2400
20	130	19.3	146.47	2600
20	140	20.14	156.98	2800
20	150	20.97	167.46	3000
20	175	22.99	193.54	3500
20	200	24.96	219.48	4000
20	225	26.9	245.3	4500
20	250	28.82	271.01	5000
20	275	30.74	296.62	5500
20	300	32.67	322.15	6000

NETWORK C_1

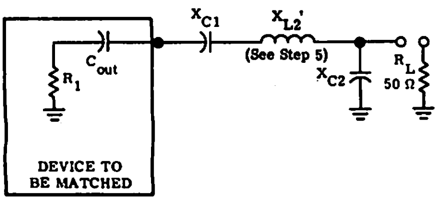
The following is a computer solution for an RF matching network. This computer solution is applicable for two forms of matching networks.



TO DESIGN A NETWORK USING THE TABLES

1. $X_{L1} = X_{C\,out}$.
2. Define Q, in column one, as X_{C1}/R_1.
3. All network values can now be read from the charts in terms of reactance.
4. This completes network C_1.

NETWORK C_2



TO DESIGN A NETWORK USING THE TABLES

1. L_1 is not used in this network.
2. Transform the impedance of the device to be matched to series form ($R_1 + jX_{C\,out}$).
3. Define Q, in column one, as X_{C1}/R_1.
4. For a desired Q, find the R_s to be matched in the R_1 column and read the reactive value of the components.
5. X_{L2}' is equal to the quantity X_{L2} obtained from the tables plus $|X_{C\,out}|$.
6. This completes network C_2.

Q	X_{C1}	X_{C2}	X_{L2}	R_1
1	1	7.14	8	1
1	2	10.21	11.8	2
1	3	12.63	14.87	3
1	4	14.74	17.56	4
1	5	16.67	20	5
1	6	18.46	22.25	6
1	7	20.17	24.35	7
1	8	21.82	26.33	8
1	9	23.43	28.21	9
1	10	25	30	10
1	11	26.55	31.81	11
1	12	28.1	33.35	12
1	13	29.64	34.93	13
1	14	31.13	36.45	14
1	15	32.73	37.91	15
1	16	34.3	39.32	16
1	17	35.89	40.69	17
1	18	37.5	42	18
1	19	39.14	43.27	19
1	20	40.82	44.49	20
1	21	42.55	45.68	21
1	22	44.32	46.82	22
1	23	46.15	47.92	23
1	24	48.04	48.98	24
1	25	50	50	25
1	26	52.04	50.98	26
1	27	54.17	51.92	27
1	28	56.41	52.82	28
1	29	58.76	53.68	29
1	30	61.24	54.49	30
1	32	66.67	56	32
1	34	72.89	57.32	34
1	36	80.18	58.45	36

Q	X_{C1}	X_{C2}	X_{L2}	R_1
1	38	88.98	59.35	38
1	40	100	60	40
1	42	114.56	60.33	42
1	44	135.4	60.25	44
1	46	169.56	59.56	46
1	48	244.95	57.8	48
2	2	7.14	9	1
2	4	10.21	13.8	2
2	6	12.63	17.87	3
2	8	14.74	21.56	4
2	10	16.67	25	5
2	12	18.46	28.25	6
2	14	20.17	31.35	7
2	16	21.82	34.33	8
2	18	23.43	37.21	9
2	20	25	40	10
2	22	26.55	42.71	11
2	24	28.1	45.35	12
2	26	29.64	47.93	13
2	28	31.18	50.45	14
2	30	32.73	52.91	15
2	32	34.3	55.32	16
2	34	35.89	57.69	17
2	36	37.5	60	18
2	38	39.14	62.27	19
2	40	40.82	64.49	20
2	42	42.55	66.68	21
2	44	44.32	68.82	22
2	46	46.15	70.92	23
2	48	48.04	72.98	24
2	50	50	75	25
2	52	52.04	76.98	26

Q	X_{C1}	X_{C2}	X_{L2}	R_1
2	54	54.17	78.92	27
2	56	56.41	80.82	28
2	58	58.76	82.68	29
2	60	61.24	84.49	30
2	64	66.67	88	32
2	68	72.89	91.32	34
2	72	80.18	94.45	36
2	76	88.98	97.35	38
2	80	100	100	40
2	84	114.56	102.33	42
2	88	135.4	104.25	44
2	92	169.56	105.56	46
2	96	244.95	105.8	48
3	3	7.14	10	1
3	6	10.21	15.8	2
3	9	12.63	20.87	3
3	12	14.74	25.56	4
3	15	16.67	30	5
3	18	18.46	34.25	6
3	21	20.17	38.35	7
3	24	21.82	42.33	8
3	27	23.43	46.21	9
3	30	25	50	10
3	33	26.55	53.71	11
3	36	28.1	57.35	12
3	39	29.64	60.98	13
3	42	31.18	64.45	14
3	45	32.73	67.91	15
3	48	34.3	71.32	16
3	51	35.89	74.69	17
3	54	37.5	78	18
3	57	39.14	81.27	19

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Q	X_{C1}	X_{C2}	X_{L2}	R_1
3	60	40.82	84.49	20
3	63	42.55	87.68	21
3	66	44.32	90.82	22
3	69	46.15	93.93	23
3	72	48.04	96.98	24
3	75	50	100	25
3	78	52.04	102.98	26
3	81	54.17	105.92	27
3	84	56.41	108.82	28
3	87	58.76	111.68	29
3	90	61.24	114.49	30
3	96	66.67	120	32
3	102	72.89	125.32	34
3	108	80.18	130.45	36
3	114	88.98	135.35	38
3	120	100	140	40
3	126	114.56	144.33	42
3	132	135.4	148.25	44
3	138	169.56	151.56	46
3	144	244.95	153.8	48
4	4	7.14	11	1
4	8	10.21	17.8	2
4	12	12.63	23.87	3
4	16	14.74	29.56	4
4	20	16.67	35	5
4	24	18.46	40.25	6
4	28	20.17	45.35	7
4	32	21.82	50.33	8
4	36	23.43	55.21	9
4	40	25	60	10
4	44	26.55	64.71	11
4	48	28.1	69.35	12
4	52	29.64	73.93	13
4	56	31.18	78.45	14
4	60	32.73	82.91	15
4	64	34.3	87.32	16
4	68	35.89	91.69	17
4	72	37.5	96	18
4	76	39.14	100.27	19
4	80	40.82	104.49	20
4	84	42.55	108.68	21
4	88	44.32	112.82	22
4	92	46.15	116.92	23
4	96	48.04	120.98	24
4	100	50	125	25
4	104	52.04	128.98	26
4	108	54.17	132.92	27
4	112	56.41	136.82	28
4	116	58.76	140.68	29
4	120	61.24	144.49	30
4	128	66.67	152	32
4	136	72.89	159.32	34
4	144	80.18	166.45	36
4	152	88.98	173.35	38
4	160	100	180	40
4	168	114.56	186.33	42
4	176	135.4	192.25	44
4	184	169.56	197.56	46
4	192	244.95	201.8	48
5	5	7.14	12	1
5	10	10.21	19.8	2
5	15	12.63	26.87	3
5	20	14.74	33.56	4
5	25	16.67	40	5
5	30	18.46	46.25	6
5	35	20.17	52.35	7
5	40	21.82	58.33	8
5	45	23.43	64.21	9
5	50	25	70	10
5	55	26.55	75.71	11
5	60	28.1	81.35	12
5	65	29.64	86.93	13
5	70	31.18	92.45	14
5	75	32.73	97.91	15
5	80	34.3	103.32	16
5	85	35.89	108.69	17
5	90	37.5	114	18
5	95	39.14	119.27	19
5	100	40.82	124.49	20
5	105	42.55	129.68	21
5	110	44.32	134.82	22
5	115	46.15	139.92	23
5	120	48.04	144.98	24
5	125	50	150	25
5	130	52.04	154.98	26
5	135	54.17	159.92	27
5	140	56.41	164.82	28
5	145	58.76	169.68	29
5	150	61.24	174.49	30
5	160	66.67	184	32
5	170	72.89	193.32	34
5	180	80.18	202.45	36
5	190	88.98	211.35	38
5	200	100	220	40
5	210	114.56	228.33	42
5	220	135.4	236.25	44
5	230	169.56	243.56	46
5	240	244.95	249.8	48
6	6	7.14	13	1
6	12	10.21	21.8	2
6	18	12.63	29.87	3
6	24	14.74	37.56	4
6	30	16.67	45	5
6	36	18.46	52.25	6
6	42	20.17	59.35	7
6	48	21.82	66.33	8
6	54	23.43	73.21	9
6	60	25	80	10
6	66	26.55	86.71	11
6	72	28.1	93.35	12
6	78	29.64	99.93	13
6	84	31.18	106.45	14
6	90	32.73	112.91	15
6	96	34.3	119.32	16
6	102	35.89	125.69	17
6	108	37.5	132	18
6	114	39.14	138.27	19
6	120	40.82	144.49	20
6	126	42.55	150.68	21
6	132	44.32	156.82	22
6	138	46.15	162.92	23
6	144	48.04	168.98	24
6	150	50	175	25
6	156	52.04	180.98	26
6	162	54.17	186.92	27
6	168	56.41	192.82	28
6	174	58.76	198.68	29
6	180	61.24	204.49	30
6	192	66.67	216	32
6	204	72.89	227.32	34
6	216	80.18	238.45	36
6	228	88.98	249.35	38
6	240	100	260	40
6	252	114.56	270.33	42
6	264	135.4	280.25	44
6	276	169.56	289.56	46
6	288	244.95	297.8	48
7	7	7.14	14	1
7	14	10.21	23.8	2
7	21	12.63	32.87	3
7	28	14.74	41.56	4
7	35	16.67	50	5
7	42	18.46	58.25	6
7	49	20.17	66.35	7
7	56	21.82	74.33	8
7	63	23.43	82.21	9
7	70	25	90	10
7	77	26.55	97.71	11
7	84	28.1	105.35	12
7	91	29.64	112.93	13
7	98	31.18	120.45	14
7	105	32.73	127.91	15
7	112	34.3	135.32	16
7	119	35.89	142.69	17
7	126	37.5	150	18
7	133	39.14	157.27	19
7	140	40.82	164.49	20
7	147	42.55	171.68	21
7	154	44.32	178.82	22
7	161	46.15	185.92	23
7	168	48.04	192.98	24
7	175	50	200	25
7	182	52.04	206.98	26
7	189	54.17	213.92	27
7	196	56.41	220.82	28
7	203	58.76	227.68	29
7	210	61.24	234.49	30
7	224	66.67	248	32
7	238	72.89	261.32	34
7	252	80.18	274.45	36
7	266	88.98	287.35	38
7	280	100	300	40
7	294	114.56	312.33	42
7	308	135.4	324.25	44
7	322	169.56	335.56	46
7	336	244.95	345.8	48
8	8	7.14	15	1
8	16	10.21	25.8	2
8	24	12.63	35.87	3
8	32	14.74	45.56	4
8	40	16.67	55	5
8	48	18.46	64.25	6
8	56	20.17	73.35	7
8	64	21.82	82.33	8
8	72	23.43	91.21	9
8	80	25	100	10
8	88	26.55	108.71	11
8	96	28.1	117.35	12
8	104	29.64	125.93	13
8	112	31.18	134.45	14
8	120	32.73	142.91	15
8	128	34.3	151.32	16
8	136	35.89	159.69	17
8	144	37.5	168	18
8	152	39.14	176.27	19
8	160	40.82	184.49	20
8	168	42.55	192.68	21
8	176	44.32	200.82	22
8	184	46.15	208.92	23
8	192	48.04	216.98	24
8	200	50	225	25
8	208	52.04	232.98	26
8	216	54.17	240.92	27
8	224	56.41	248.82	28
8	232	58.76	256.68	29
8	240	61.24	264.49	30
8	256	66.67	280	32
8	272	72.89	295.32	34
8	288	80.18	310.45	36
8	304	88.98	325.35	38

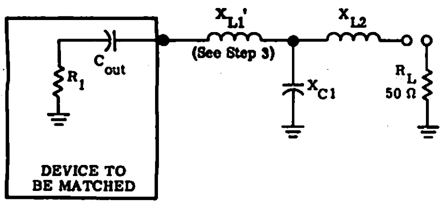
Q	X_{C1}	X_{C2}	X_{L2}	R_1
8	320	100	340	40
8	336	114.56	354.33	42
8	352	135.4	368.25	44
8	368	169.56	381.56	46
8	384	244.95	393.8	48
9	9	7.14	16	1
9	18	10.21	27.8	2
9	27	12.63	38.87	3
9	36	14.74	49.56	4
9	45	16.67	60	5
9	54	18.46	70.25	6
9	63	20.17	80.35	7
9	72	21.82	90.33	8
9	81	23.43	100.21	9
9	90	25	110	10
9	99	26.55	119.71	11
9	108	28.1	129.35	12
9	117	29.64	138.93	13
9	126	31.18	148.45	14
9	135	32.73	157.91	15
9	144	34.3	167.32	16
9	153	35.89	176.69	17
9	162	37.5	186	18
9	171	39.17	195.27	19
9	180	40.82	204.49	20
9	189	42.55	213.68	21
9	198	44.32	222.82	22
9	207	46.15	231.92	23

Q	X_{C1}	X_{C2}	X_{L2}	R_1
9	414	169.56	427.56	46
9	432	244.95	441.8	48
9	216	48.04	240.98	24
9	225	50	250	25
9	234	52.04	258.98	26
9	243	54.17	267.92	27
9	252	56.41	276.82	28
9	261	58.76	285.88	29
9	270	61.24	294.49	30
9	288	66.67	312	32
9	306	72.89	329.32	34
9	324	80.18	346.45	36
9	342	88.98	363.35	38
9	360	100	380	40
9	378	114.56	396.33	42
9	396	135.4	412.25	44
10	10	7.14	17	1
10	20	10.21	29.8	2
10	30	12.63	41.87	3
10	4C	14.74	53.56	4
10	50	16.67	65	5
10	60	18.46	76.25	6
10	70	20.17	87.35	7
10	80	21.82	98.33	8
10	90	23.43	109.21	9
10	100	25	120	10
10	110	26.55	130.71	11

Q	X_{C1}	X_{C2}	X_{L2}	R_1
10	120	28.1	141.35	12
10	130	29.64	151.93	13
10	140	31.18	162.45	14
10	150	32.73	172.91	15
10	160	34.3	183.32	16
10	170	35.89	193.69	17
10	180	37.5	204	18
10	190	39.14	214.27	19
10	200	40.82	224.49	20
10	210	42.55	234.68	21
10	220	44.32	244.82	22
10	230	46.15	254.92	23
10	240	48.04	264.98	24
10	250	50	275	25
10	260	52.04	284.98	26
10	270	54.17	294.92	27
10	280	56.41	304.82	28
10	290	58.76	314.68	29
10	300	61.24	324.49	30
10	320	66.67	344	32
10	340	72.89	363.32	34
10	360	80.18	382.45	36
10	380	88.98	401.35	38
10	400	100	420	40
10	420	114.56	438.33	42
10	440	135.4	456.25	44
10	460	169.56	473.56	46
10	480	244.95	489.8	48

NETWORK D

The following is a computer solution for an RF "Tee" matching network.
Tuning is accomplished by using a variable capacitor for C_1. Variable matching may also be accomplished by increasing X_{L2} and adding an equal amount of X_C in series in the form of a variable capacitor.



TO DESIGN A NETWORK USING THE TABLES

1. Define Q, in column one, as X_{L1}/R_1.
2. For an R_1 to be matched and a desired Q, read the reactances of the network components from the charts.
3. X_{L1}' is equal to the quantity X_{L1} obtained from the tables plus $|X_{C_{out}}|$.
4. This completes the network.

Q	X_{L1}	X_{L2}	X_{C1}	R_1
1	26	10	43.33	26
1	27	14.14	42.09	27
1	28	17.32	41.59	28
1	29	20	41.43	29
1	30	22.36	41.46	30
1	32	26.46	41.85	32
1	34	30	42.5	34
1	36	33.17	43.29	36
1	38	36.06	44.16	38
1	40	38.72	45.08	40
1	42	41.23	46.04	42
1	44	43.59	47.01	44
1	46	45.83	48	46
1	48	47.96	49	48
1	50	50	50	50
1	55	54.77	52.49	55
1	60	59.16	54.96	60
1	65	63.25	57.4	65
1	70	67.08	69.79	70
1	75	70.71	62.13	75
1	80	74.16	64.43	80
1	85	77.46	66.69	85
1	90	80.62	68.9	90
1	95	83.67	71.07	95
1	100	86.6	73.21	100
1	125	100	83.33	125
1	150	111.8	92.71	150

Q	X_{L1}	X_{L2}	X_{C1}	R_1
1	175	122.47	101.46	175
1	200	132.29	109.72	200
1	225	141.42	117.54	225
1	250	150	125	250
1	275	158.11	132.14	275
1	300	165.83	139	300
2	22	15.81	23.75	11
2	24	22.36	24.52	12
2	26	27.39	25.51	13
2	28	31.62	26.59	14
2	30	35.36	27.7	15
2	32	38.73	28.83	16
2	34	41.83	29.96	17
2	36	44.72	31.09	18
2	38	47.43	32.22	19
2	40	50	33.33	20
2	42	52.44	34.44	21
2	44	54.77	35.54	22
2	46	57.01	36.62	23
2	48	59.16	37.7	24
2	50	61.24	38.76	25
2	52	63.25	39.82	26
2	54	65.19	40.86	27
2	56	67.08	41.9	28
2	58	68.92	42.92	29
2	60	70.71	43.93	30
2	64	74.16	45.93	32

Q	X_{L1}	X_{L2}	X_{C1}	R_1
2	68	77.46	47.9	34
2	72	80.62	49.83	36
2	76	83.67	51.72	38
2	80	86.6	53.59	40
2	84	89.44	55.43	42
2	88	92.2	57.23	44
2	92	94.87	59.01	46
2	96	97.47	60.77	48
2	100	100	62.5	50
2	110	106.07	66.73	55
2	120	111.8	70.82	60
2	130	117.26	74.8	65
2	140	122.47	78.66	70
2	150	127.48	82.43	75
2	160	132.29	86.1	80
2	170	136.93	89.69	85
2	180	141.42	93.2	90
2	190	145.77	96.63	95
2	200	150	100	100
2	250	169.56	115.93	125
2	300	187.08	130.62	150
2	350	203.1	144.34	175
2	400	217.94	157.26	200
2	450	231.84	169.51	225
2	500	244.95	181.19	250
2	550	257.39	192.37	275
2	600	269.26	203.11	300

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Q	X_{L1}	X_{L2}	X_{C1}	R_1
3	18	22.36	17.41	6
3	21	31.62	19.27	7
3	24	38.73	21.19	8
3	27	44.72	23.11	9
3	30	50	25	10
3	33	54.77	26.86	11
3	36	59.16	28.69	12
3	39	63.25	30.48	13
3	42	67.08	32.25	14
3	45	70.71	33.98	15
3	48	74.16	35.69	16
3	51	77.46	37.37	17
3	54	80.62	39.02	18
3	57	83.67	40.66	19
3	60	86.6	42.26	20
3	63	89.44	43.85	21
3	66	92.2	45.42	22
3	69	94.87	46.96	23
3	72	97.47	48.49	24
3	75	100	50	25
3	78	102.47	51.49	26
3	81	104.88	52.97	27
3	84	107.24	54.42	28
3	87	109.54	55.87	29
3	90	111.8	57.29	30
3	96	116.19	60.11	32
3	102	120.42	62.87	34
3	108	124.5	65.57	36
3	114	128.45	68.23	38
3	120	132.29	70.85	40
3	126	136.01	73.42	42
3	132	139.64	75.96	44
3	138	143.18	78.45	46
3	144	146.63	80.91	48
3	150	150	83.33	50
3	165	158.11	89.25	55
3	180	165.83	94.99	60
3	195	173.21	100.56	65
3	210	180.28	105.97	70
3	225	187.08	111.25	75
3	240	193.65	116.4	80
3	255	200	121.43	85
3	270	206.16	126.35	90
3	285	212.13	131.17	95
3	300	217.94	135.89	100
3	375	244.95	158.25	125
3	450	269.26	178.89	150
3	525	291.55	198.17	175
3	600	312.25	216.33	200
3	675	331.66	233.57	225
3	750	350	250	250
3	825	367.42	265.74	275
3	900	384.06	280.87	300
4	12	7.07	12.31	3
4	16	30	14.78	4
4	20	41.83	17.57	5
4	24	50.99	20.32	6
4	28	58.74	23	7
4	32	65.57	25.6	8
4	36	71.76	28.15	9
4	40	77.46	30.64	10
4	44	82.76	33.07	11
4	48	87.75	35.45	12
4	52	92.47	37.78	13
4	56	96.95	40.07	14
4	60	101.24	42.32	15
4	64	105.36	44.54	16
4	68	109.32	46.72	17
4	72	113.14	48.86	18
4	76	116.83	50.97	19
4	80	120.42	53.06	20
4	84	123.9	55.11	21
4	88	127.28	57.14	22
4	92	130.58	59.14	23
4	96	133.79	61.12	24
4	100	136.93	63.07	25
4	104	140	65	26
4	108	143	66.91	27
4	112	145.95	68.8	28
4	116	148.83	70.67	29
4	120	151.66	72.51	30
4	128	157.16	76.16	32
4	136	162.48	79.73	34
4	144	167.63	83.24	36
4	152	172.63	86.68	38
4	160	177.48	90.07	40
4	168	182.21	93.4	42
4	176	186.82	96.69	44
4	184	191.31	99.92	46
4	192	195.7	103.11	48
4	200	200	106.25	50
4	220	210.36	113.93	55
4	240	220.23	121.36	60
4	260	229.67	128.59	65
4	280	238.75	135.61	70
4	300	247.49	142.46	75
4	320	255.93	148.15	80
4	340	264.1	155.68	85
4	360	272.03	162.07	90
4	380	279.73	168.32	95
4	400	287.23	174.46	100
4	500	322.1	203.5	125
4	600	353.55	230.33	150
4	700	382.43	255.4	175
4	800	409.27	279.02	200
4	900	434.45	301.44	225
4	1000	458.26	322.82	250
4	1100	480.88	343.3	275
4	1200	502.49	362.99	300
5	10	10	10	2
5	15	37.42	13.57	3
5	20	51.96	17.22	4
5	25	63.25	20.75	5
5	30	72.8	24.16	6
5	35	81.24	27.47	7
5	40	88.88	30.69	8
5	45	95.92	33.82	9
5	50	102.47	36.88	10
5	55	108.63	39.87	11
5	60	114.46	42.8	12
5	65	120	45.68	13
5	70	125.3	48.49	14
5	75	130.38	51.26	15
5	80	135.28	53.99	16
5	85	140	56.67	17
5	90	144.57	59.31	18
5	95	149	61.91	19
5	100	153.3	64.47	20
5	105	157.48	67	21
5	110	161.55	69.49	22
5	115	165.53	71.96	23
5	120	169.41	74.39	24
5	125	173.21	76.79	25
5	130	176.92	79.17	26
5	135	180.55	81.52	27
5	140	184.12	83.85	28
5	145	187.62	86.15	29
5	150	191.05	88.43	30
5	160	197.74	92.91	32
5	170	204.21	97.31	34
5	180	210.48	101.63	36
5	190	216.56	105.88	38
5	200	222.49	110.06	40
5	210	228.25	114.17	42
5	220	233.88	118.21	44
5	230	239.37	122.2	46
5	240	244.74	126.13	48
5	250	260	130	50
5	275	262.68	139.46	55
5	300	274.77	148.64	60
5	325	286.36	157.54	65
5	350	297.49	166.21	70
5	375	308.22	174.66	75
5	400	318.59	182.91	80
5	425	328.63	190.97	85
5	450	338.38	198.85	90
5	475	347.85	206.57	95
5	500	357.07	214.14	100
5	625	400	250	125
5	750	438.75	283.12	150
5	875	474.34	314.08	175
5	1000	507.44	343.26	200
5	1125	538.52	670.95	225
5	1250	567.89	397.36	250
5	1375	595.82	422.67	275
5	1500	622.49	446.99	300
6	12	34.64	11.06	2
6	18	55.23	15.62	3
6	24	70	20	4
6	30	82.16	24.2	5
6	36	92.74	28.26	6
6	42	102.23	32.2	7
6	48	110.91	36.02	8
6	54	118.95	39.74	9
6	60	126.49	43.38	10
6	66	133.6	46.93	11
6	72	140.36	50.41	12
6	78	146.8	53.83	13
6	84	152.97	57.18	14
6	90	158.9	60.47	15
6	96	164.62	63.71	16
6	102	170.15	66.89	17
6	108	175.5	70.03	18
6	114	180.69	73.12	19
6	120	185.74	76.17	20
6	126	190.66	79.18	21
6	132	195.45	82.15	22
6	138	200.12	85.08	23
6	144	204.69	87.97	24
6	150	209.17	90.83	25
6	156	213.54	93.66	26
6	162	217.83	96.46	27
6	168	222.04	99.23	28
6	174	226.16	101.96	29
6	180	230.22	104.67	30
6	192	238.12	110.01	32
6	204	245.76	115.25	34
6	216	253.18	120.39	36
6	228	260.38	125.45	38
6	240	267.39	130.42	40
6	252	274.23	135.31	42
6	264	280.89	140.13	44
6	276	287.4	144.88	46
6	288	293.77	149.55	48
6	300	300	154.17	50
6	330	315.04	165.44	55
6	360	329.39	176.36	60
6	390	343.15	186.97	65
6	420	356.37	197.3	70
6	450	369.12	207.36	75
6	480	381.44	217.19	80
6	510	393.38	226.79	85
6	540	404.97	236.18	90
6	570	416.23	245.38	95
6	600	427.2	254.4	100
6	750	478.28	297.13	125
6	900	524.4	336.61	150
6	1050	566.79	373.5	175
6	1200	606.22	408.29	200
6	1350	643.23	441.3	225
6	1500	678.23	472.79	250
6	1650	711.51	502.96	275
6	1800	743.3	531.96	300
7	14	50	12.5	2
7	21	70.71	17.83	3
7	28	86.6	22.9	4
7	35	100	27.78	5
7	42	111.8	32.48	6
7	49	122.47	37.04	7
7	56	132.29	41.47	8
7	63	141.42	45.79	9
7	70	150	50	10
7	77	158.11	54.12	11
7	84	165.83	58.16	12
7	91	173.21	62.12	13
7	98	180.28	66	14
7	105	187.08	69.82	15
7	112	193.65	73.58	16

Q	X_{L1}	X_{L2}	X_{C1}	R_1
7	119	200	77.27	17
7	126	206.16	80.91	18
7	133	212.13	84.5	19
7	140	217.94	88.04	20
7	147	223.61	91.53	21
7	154	229.13	94.97	22
7	161	234.52	98.37	23
7	168	239.79	101.73	24
7	175	244.95	105.05	25
7	182	250	108.33	26
7	189	254.95	111.58	27
7	196	259.81	114.79	28
7	203	264.58	117.97	29
7	210	269.26	121.11	30
7	224	278.39	127.31	32
7	238	287.23	133.39	34
7	252	295.8	139.36	36
7	266	304.14	145.23	38
7	280	312.25	151	40
7	294	320.16	156.68	42
7	308	327.87	162.27	44
7	322	335.41	167.78	46
7	336	342.78	173.21	48
7	350	350	178.57	50
7	385	367.42	191.66	55
7	420	384.06	204.34	60
7	455	400	216.67	65
7	490	415.33	228.66	70
7	525	430.12	240.35	75
7	560	444.41	251.76	80
7	595	458.86	262.91	85
7	630	471.7	273.82	90
7	665	484.77	284.51	95
7	700	497.49	294.99	100
7	875	556.78	344.63	125
7	1050	610.33	390.49	150
7	1225	659.55	433.36	175
7	1400	705.34	473.78	200
7	1575	748.33	512.14	225
7	1750	788.99	548.73	250
7	1925	827.65	583.79	275
7	2100	864.58	617.5	300
8	8	27.39	7.6	1
8	16	63.25	14.03	2
8	24	85.15	20.1	3
8	32	102.47	25.87	4
8	40	117.26	31.42	5
8	48	130.38	36.77	6
8	56	142.3	41.95	7
8	64	153.3	46.99	8
8	72	163.55	51.9	9
8	80	173.21	56.7	10
8	88	182.35	61.39	11
8	96	191.05	65.98	12
8	104	199.37	70.49	13
8	112	207.36	74.91	14
8	120	215.06	79.26	15
8	128	222.49	83.54	16
8	136	229.67	87.74	17
8	144	236.64	91.89	18
8	152	243.41	95.97	19
8	160	250	100	20
8	168	256.42	103.97	21
8	176	262.68	107.9	22
8	184	268.79	111.77	23
8	192	274.77	115.59	24
8	200	280.62	119.38	25
8	208	286.36	123.11	26
8	216	291.98	126.81	27
8	224	297.49	130.47	28
8	232	302.9	134.09	29
8	240	308.22	137.67	30

Q	X_{L1}	X_{L2}	X_{C1}	R_1
8	256	318.59	144.73	32
8	272	328.63	151.65	34
8	288	338.38	158.46	36
8	304	347.85	165.14	38
8	320	357.07	171.71	40
8	336	366.06	178.18	42
8	352	374.83	184.56	44
8	368	383.41	190.83	46
8	384	391.79	197.02	48
8	400	400	203.13	50
8	440	419.82	218.04	55
8	480	438.75	232.49	60
8	520	456.89	246.53	65
8	560	474.34	260.2	70
8	600	491.17	273.52	75
8	640	507.44	286.52	80
8	680	523.21	299.23	85
8	720	538.52	311.66	90
8	760	553.4	323.84	95
8	800	567.89	335.78	100
8	1000	635.41	392.36	125
8	1200	696.42	444.63	150
8	1400	752.5	493.49	175
8	1600	804.67	539.57	200
8	1800	853.67	583.29	225
8	2000	900	625	250
8	2200	944.06	664.96	275
8	2400	986.15	703.38	300
9	9	40	8.37	1
9	18	75.5	15.6	2
9	27	98.99	22.4	3
9	36	117.9	28.88	4
9	45	134.16	35.09	5
9	54	148.66	41.09	6
9	63	161.86	46.91	7
9	72	174.07	52.56	8
9	81	185.47	58.07	9
9	90	196.21	63.45	10
9	99	206.4	68.71	11
9	108	216.1	73.86	12
9	117	225.39	78.92	13
9	126	234.31	83.88	14
9	135	242.9	88.76	15
9	144	251.2	93.55	16
9	153	259.23	98.28	17
9	162	267.02	102.93	18
9	171	274.59	107.51	19
9	180	281.96	112.03	20
9	189	289.14	116.49	21
9	198	296.14	120.89	22
9	207	302.99	125.23	23
9	216	309.68	129.53	24
9	225	316.23	133.77	25
9	234	322.65	137.97	26
9	243	328.94	142.12	27
9	252	335.11	146.22	28
9	261	341.17	150.28	29
9	270	347.13	154.3	30
9	288	358.75	162.23	32
9	306	370	170	34
9	324	380.92	177.63	36
9	342	391.54	185.14	38
9	360	401.87	192.52	40
9	378	411.95	199.78	42
9	396	421.78	206.93	44
9	414	431.39	213.98	46
9	432	440.79	220.93	48
9	450	450	227.78	50
9	495	472.23	244.52	55
9	540	493.46	260.74	60
9	585	513.81	276.51	65
9	630	533.39	291.85	70

Q	X_{L1}	X_{L2}	X_{C1}	R_1
9	675	552.27	306.8	75
9	720	570.53	321.4	80
9	765	588.22	335.67	85
9	810	605.39	349.63	90
9	855	622.09	363.31	95
9	900	638.36	376.71	100
9	1125	714.14	440.24	125
9	1350	782.62	498.94	150
9	1575	845.58	553.81	175
9	1800	904.16	605.54	200
9	2025	959.17	654.64	225
9	2250	1011.19	701.48	250
9	2475	1060.66	746.36	275
9	2700	1107.93	789.51	300
10	10	50.5	9.17	1
10	20	87.18	17.2	2
10	30	112.47	24.74	3
10	40	133.04	31.91	4
10	50	150.83	38.8	5
10	60	166.73	45.45	6
10	70	181.25	51.89	7
10	80	194.68	58.16	8
10	90	207.24	64.26	9
10	100	219.09	70.23	10
10	110	230.33	76.06	11
10	120	241.04	81.78	12
10	130	251.3	87.38	13
10	140	261.15	92.89	14
10	150	270.65	98.29	15
10	160	279.82	103.61	16
10	170	288.7	108.85	17
10	180	297.32	114.01	18
10	190	305.7	119.09	19
10	200	313.85	124.1	20
10	210	321.79	129.05	21
10	220	329.55	133.93	22
10	230	337.12	138.75	23
10	240	344.53	143.51	24
10	250	351.78	148.22	25
10	260	358.89	152.87	26
10	270	365.86	157.47	27
10	280	372.69	162.03	28
10	290	379.41	166.53	29
10	300	386.01	170.99	30
10	320	398.87	179.78	32
10	340	411.34	188.4	34
10	360	423.44	196.87	36
10	380	435.2	205.2	38
10	400	446.65	213.38	40
10	420	457.82	221.44	42
10	440	468.72	229.37	44
10	460	479.37	237.19	46
10	480	489.8	244.9	48
10	500	500	252.5	50
10	550	524.64	271.07	55
10	600	548.18	289.07	60
10	650	570.75	306.56	65
10	700	592.45	323.58	70
10	750	613.39	340.18	75
10	800	633.64	356.37	80
10	850	653.26	372.21	85
10	900	672.31	387.7	90
10	950	690.83	402.87	95
10	1000	708.87	417.74	100
10	1250	792.94	488.23	125
10	1500	868.91	553.36	150
10	1750	938.75	614.25	175
10	2000	1003.74	671.66	200
10	2250	1064.78	726.14	225
10	2500	1122.5	778.12	250
10	2750	1177.39	827.92	275
10	3000	1229.84	875.8	300

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Prepared by:
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SYSTEMIZING RF POWER AMPLIFIER DESIGN

INTRODUCTION

Two of the most popular RF small signal design techniques are:

1) the use of two port parameters, and
2) the use of some type of equivalent circuit for the transistor.

Early attempts to adapt these techniques to power amplifier design led to poor results and frustration.

In the mid-1960's, Motorola pioneered the concept of solid state power amplifier design through the use of large signal transistor input and output impedances. This system has since achieved almost universal acceptance by solid state communications equipment manufacturers. It provides a systematic design procedure to replace what used to be a trial and error process. This note is a description of the concept and its use in transmitter design.

LIMITATIONS OF SMALL-SIGNAL PARAMETERS

As a vivid example to show the short-comings of trying to adapt small-signal parameters to power amplifier design, the 2N3948 transistor was considered. A performance comparison was made of the 2N3948 operating at 300 MHz as a Class A small-signal amplifier, and as a Class C* power amplifier delivering a power output of 1 W. Table I shows the results of this comparison.

	CLASS A Small-signal amplifier V_{CE} = 15 Vdc; I_c = 80 mA; 300 MHz	CLASS C Power amplifier V_{CE} = 13.6 Vdc; P_o = 1 W
Input resistance	9 Ohms	38 Ohms
Input capacitance or inductance	0.012 μH	21 pF
Transistor output resistance	199 Ohms	92 Ohms
Output capacitance	4.6 pF	5.0 pF
G_{PE}	12.4 dB	8.2 dB

Table I — Small- and large-signal performance data for the 2N3948 show the inadequacy of using small-signal characterization data for large-signal amplifier design. Resistances and reactances shown are parallel components. That is, the large-signal input impedance is 38 ohms in parallel with 21 pF, etc.

The most striking difference in this comparison is in the device input impedance. As operation is changed from small-signal to large-signal conditions, the complex input impedance of the 2N3948 undergoes a considerable change in magnitude and actually changes from inductive to capacitive reactance.

Note also that the transistor's output resistances and power gains are considerably different for the two modes of operation. This example clearly demonstrates the inaccuracies that would result in a power-amplifier design based on the small-signal parameters of this device.

IMPORTANCE OF LARGE-SIGNAL PARAMETERS

The network theory for power amplifier design is well known but is useless unless the designer has valid input and output impedance data for the transistor. The design method described in this report hinges primarily on the direct measurement of these parameters for use in network synthesis equations. Large-signal impedance data, together with power output and gain data, provide the designer with the information necessary to design his amplifier networks and to predict the performance that should be achieved when the design is completed.

A clear understanding of the test conditions and method of presentation for the large signal impedance data is important.

TEST CONDITIONS

The term "large-signal input impedance" and "large-signal output impedance" refer to the actual transistor terminal impedances when operating in a matched amplifier at the desired RF power output level and dc supply voltage.

"Matched" is defined as the condition where the input and output networks of the test amplifier provide a conjugate match to the transistor, such that the input and output impedances of the amplifier are 50 + j 0 ohms.

Large-signal impedances should not be confused with small-signal, two port parameters which are normally measured at low signal levels with Class A bias and the transistor (or IC) connected directly to a short, open, or 50 ohm termination.

Most of the data which appears on Motorola RF power transistor data sheets is measured in common emitter, Class C amplifiers; as this condition covers the majority of device applications.

One significant exception to this involves transistors characterized for Class B linear power amplifier service. Examples of such transistors are the Motorola 2N5941-2 series. Since these transistors are designed specifically for linear service, their large-signal impedances were measured in a linear power amplifier test circuit with a two tone test signal instead of the conventional single frequency signal. For further information on these transistors see the

*Class C, as used here, refers to operation with both the emitter and base at dc ground potential and with the collector supply as the only dc voltage applied, regardless of resulting device conduction angle. Usually, the emitter is connected directly to chassis ground and the base is dc grounded through an inductive network element or choke.

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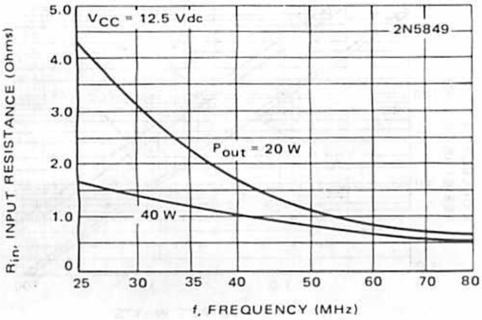

FIGURE 1 – Parallel Equivalent Input Resistance versus Frequency

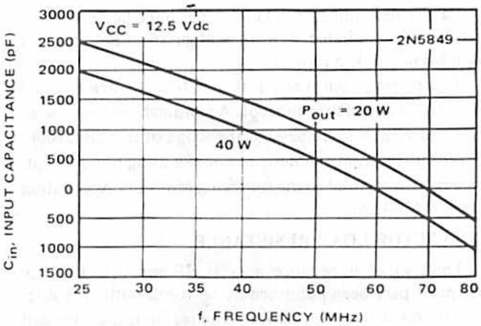

FIGURE 2 – Parallel Equivalent Input Capacitance versus Frequency

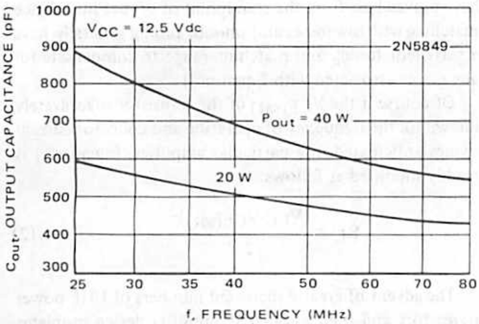

FIGURE 3 – Parallel Equivalent Output Capacitance versus Frequency

Motorola 2N5941-2 data sheet.

DATA FORMAT

Much of the information on device data sheets is presented in parallel equivalent form of resistance and capacitance. Figures 1-3 form an example of this type of presentation. The data may also be presented in series equivalent form. It makes no difference which form is used as long as the designer pays particular attention to the form and uses the data accordingly. As a convenience, the series-parallel equivalent conversion equations are given in Appendix A.

For example, reading the complex input impedance, from Figures 1 and 2 at 50 MHz with 40 W output and a 12.5 Vdc collector supply, we obtain a value of 0.8 ohms resistance in parallel with a 500 pF capacitance.

Another form of impedance data presentation uses the series equivalent form plotted on a Smith Chart. This form is popular with UHF power transistors due to the extensive use of the Smith Chart in microstrip network synthesis. Figure 4 is an example of large-signal impedances plotted on a Smith Chart plot. Note that Figure 4 includes complete complex output impedance data, not just the output capacitance. This topic is discussed more fully in the section on collector load resistance.

AMPLIFIER DESIGN

After selection of a transistor with the required performance capabilities, the next step in the design of a power amplifier is to determine the large-signal input and output impedances of the transistor. When using devices for which the data is available, this step involves nothing more than reading the complex impedance values off of the data sheet. If only output capacitance is given on the data sheet, the collector load resistance may be calculated in the manner described in the Collector Load Resistance Section of this note.

Again, the designer is cautioned to carefully determine whether the data sheet impedance curves are in parallel or series equivalent form, and to use the data accordingly. If the data is not available, a later section of this note contains information on large-signal impedance measurement.

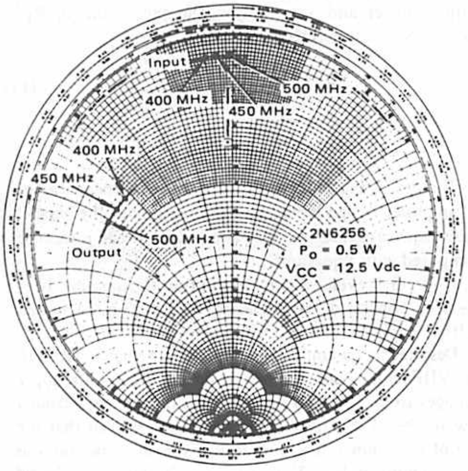

FIGURE 4 – Large Signal Input and Output Series Impedances, 2N6256

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Having determined the large-signal impedances, the designer selects a suitable network configuration and proceeds with his network synthesis.

The primary purpose of this note is to describe the large-signal impedance concept. Accordingly, network selection and synthesis are beyond the scope of this discussion. For specific transmitter design examples using this concept, the reader is referred to the following Motorola Application Note: AN-548A.

COLLECTOR LOAD RESISTANCE

Large-signal impedance data at HF and VHF have for the most part been published by Motorola without collector load resistance information. The reason is that the load resistance can easily be calculated. The conditions necessary to obtain this load resistance derivation will now be discussed.

If certain simplifying assumptions are made, the theoretical collector voltage of a power amplifier with a tuned output network is a sine wave which swings from zero to 2 V_{CC}, where V_{CC} is the dc collector supply voltage. These assumptions include:

1. $V_{CE(sat)}$ is equal to zero.
2. The output network has sufficient loaded Q to produce a sine wave voltage regardless of transistor conduction angle.
3. The voltage drop in the dc collector supply feed system is zero.
4. The collector load impedance at all harmonics of the operating frequency is zero.

Obviously none of the foregoing assumptions is true, and the most serious discrepancies probably arise from assumptions 1 and 4. However, conditions are close enough to give good results.

Let us assume for a moment that this theoretical condition does exist. The parallel equivalent collector load resistance, R_L', then becomes a function of desired RF output power and V_{CC} only. The expression for R_L' given in equation 1 is readily derived.

$$R_L' = \frac{(V_{CC})^2}{2P} \qquad (1)$$

where P = RF output power

Therefore, the complex collector load impedance for an amplifier design would be the conjugate of the parallel equivalent output capacitance and collector load resistance computed with Equation 1.

Figure 5 provides a graphic solution to Equation 1 for the four popular dc supply levels of 12.5, 13.6, 24 and 28 volts.

Despite the assumptions required, experience with HF and VHF lumped-component, power amplifiers with supply voltages from 7 to 30 Vdc and power output levels from a few tenths of a watt to 300 watts have proven that the use of Equation 1 to compute R_L' for network synthesis yields good results. That is to say, the types of HF and VHF lumped component collector output networks which

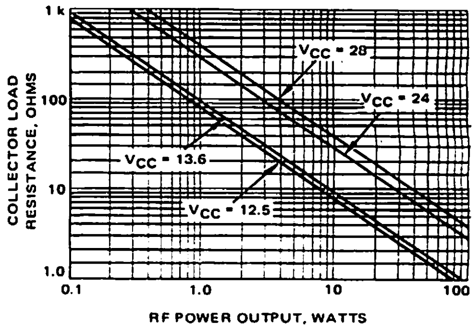


FIGURE 5 – Collector Load Resistance versus Power Output

have proved best from the standpoint of proper impedance matching with low losses and smooth tuning generally have a sufficient tuning and matching range to compensate for any errors associated with Equation 1.

Of course if the $V_{CE(sat)}$ of the transistor is accurately known for the frequency of operation and collector current swings anticipated in a particular amplifier, Equation 1 is readily modified as follows:

$$R_L' = \frac{(V_{CC} \cdot V_{CE(sat)})^2}{2P} \qquad (2)$$

The advent of greatly increased numbers of UHF power transistors and their associated amplifier design problems brought some revisions to Motorola's methods of presenting large-signal transistor impedances for UHF devices. Among the reasons for this are the popularity of microstrip matching networks and the higher $V_{CE(sat)}$ values at UHF.

The major difference in the data format involves output impedance, which is presented in full complex form instead of plotting parallel equivalent output capacitance only and using Equation 1 to compute the load resistance. Further, the UHF devices are measured in a microstrip test amplifier for the purpose of determining the transistor impedances in an environment which is as close as possible to that of the majority of the actual applications of the device. And finally, a Smith Chart plot is used as this is more convenient to the microstrip network designer, who often makes extensive use of the Smith Chart as a design tool.

Future Motorola data sheets may also include collector load resistance data at frequencies below UHF. The information is automatically generated for the test circuit in use while measuring C_{in}, R_{in} and C_{out}.

PARAMETER MEASUREMENT

Although design engineers will find large-signal impedance characterization on Motorola data sheets for RF power transistors, it may help to know how this data is obtained. The transistor is placed in a test circuit designed to provide wide tuning capabilities. Design of the first test amplifier for a new transistor type is based on estimates of input and output impedance.

Since the input and output impedances are needed to design an amplifier which is then used to measure the impedances of the device, we have a "chicken or the egg" type of problem. Wide tuning range networks help compensate for errors in the impedance estimates and they also permit the same characterization amplifier to be used at multiple power output levels.

The amplifier is tuned for a careful impedance match *at both input and output*. Several precautions are in order to insure that this is accomplished.

Tuning for maximum power output is valid only if the source and load impedances are an accurate 50 + j 0 ohms. Usually a good 50 ohm load is available in the laboratory. Such a load should be used, as tuning for maximum output power for a given input power is the best method to use on the amplifier output network.

The input network poses some additional problems. First, many laboratory RF power sources are not accurate 50 ohm generators. A generator impedance that is not 50 ohms can introduce errors in measuring gain as well as input impedances. In addition, a source with high harmonic levels can cause difficulties in low Q input networks.

A good solution to this problem is to use a dual directional coupler or directional power meter in the coax line between the generator and the test amplifier. The amplifier is then tuned for zero reflected power, thus indicating that the input network is really matching the transistor input impedance to 50 + j 0 ohms.

In practice, the reflected power usually will not null all the way to zero, so one should insure that the null is at least as deep as that obtained with a good 50 ohm passive termination.

In some cases, the amplifier will reflect enough harmonic power to prevent a satisfactory reflected power null from being obtained. A good solution to this problem is to place a fundamental frequency bandpass filter at the reflected power port of the dual directional coupler.

A typical test amplifier for HF and VHF measurements is shown in Figure 6. For UHF device characterization, amplifiers employing microstrip matching networks are *most commonly* employed.

After the test amplifier has been properly tuned, the dc power, signal source, circuit load, and test transistor are disconnected from the circuit. Then the signal source and output load circuit connections are each terminated with 50 ohms. After performing these substitutions, complex impedances are measured at the base and collector circuit connections of the test transistor (points A and B respectively in Figure 7). The desired data, the transistor input and output impedances, will be the conjugates of the base circuit connection and the collector circuit connection, impedances respectively.

By operating test amplifiers at several different frequencies with at least two power outputs, sufficient data can be obtained to characterize a transistor for the majority of its power applications.

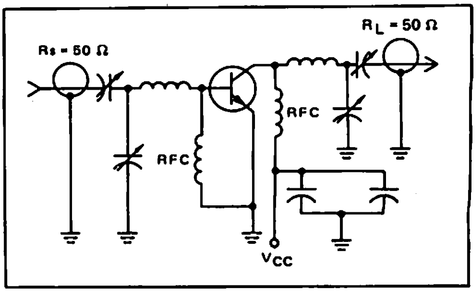
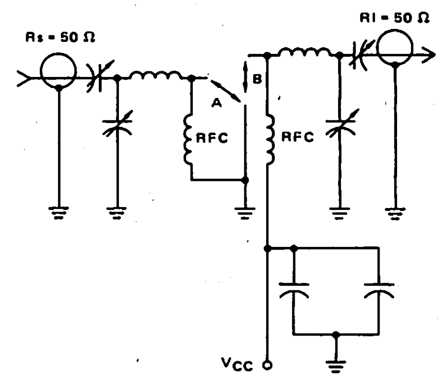


FIGURE 6 – Typical Test Amplifier Circuit



Complex impedances are measured at the base and collector circuit connections of the test transistor (points A and B respectively). Desired data will be the conjugates of these impedances.

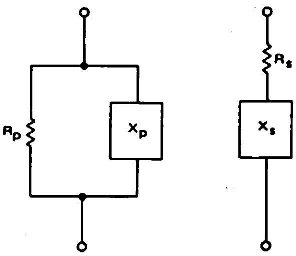
FIGURE 7 – Test Circuit with Transistor Removed

SUMMARY

The large-signal impedance characterization of RF power transistors has provided the most systematic and successful power amplifier design method the author has encountered since the concept was explored in depth in the mid 1960's.

APPENDIX A

PARALLEL-TO-SERIES AND SERIES-TO-PARALLEL IMPEDANCE CONVERSION EQUATIONS.



$$R_p = R_s\left[1 + \left(\frac{X_s}{R_s}\right)^2\right]$$

$$X_p = \frac{R_p \cdot R_s}{X_s}$$

$$R_s = \frac{R_p}{1 + \left(\frac{R_p}{X_p}\right)^2}$$

$$X_s = \frac{R_s \cdot R_p}{X_p}$$

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UHF AMPLIFIER DESIGN USING DATA SHEET DESIGN CURVES

INTRODUCTION

The design of UHF amplifiers usually involves a particular set of device parameters of which h, y, and s parameters are probably the most familiar. These parameters are commonly used to determine device loading (input and output) admittances for particular gain and stability criteria. The design procedure for determining gain and stability usually involves a mathematical solution, a graphical approach, or a combination of both.

This report describes a design technique for the unneutralized case whereby the device loading admittances are taken directly from device design curves. An example is given of how these design parameters are used to design a single stage 1 GHz microstrip amplifier and predicted results are compared to actual measured values. Practical circuit construction techniques are also discussed for the benefit of readers unfamiliar with microstrip techniques.

STABILITY CONSIDERATIONS

Two very important methods[1] for expressing stability involve Linvill's stability factor "C" and Stern's stability factor "k". The first deals primarily with the device since an open termination is assumed on both the input and output and is formulated:

$$C = \frac{|y_{12} y_{12}|}{2g_{11}\, g_{22} - Re\,(y_{12} y_{21})}.$$

If "C" is greater than 1, the transistor is potentially unstable. However, if C is less than 1, the transistor is unconditionally stable. The C factor versus frequency for the common base and common emitter configurations (2N4957) are shown in Figures 10 and 17 respectively.

The second method is primarily circuit oriented and is used to compute the relative stability of an actual amplifier circuit for the particular source and load terminations used. If "k" is greater than 1, the circuit is stable. If "k" is less than 1 the circuit is potentially unstable

Stern has developed equations for calculating the input and output loading admittances for maximum power gain with a particular stability factor, k. These values of input and output admittances in conjunction with the device parameters can then be used to calculate the transducer gain.[1]

$$k = \frac{2\,(g_{11} + G_s)\,(g_{22} + G_L)}{|y_{12} y_{21}| + Re\,(y_{12} y_{21})}$$

$$G_s = \sqrt{\frac{k\left[|y_{12} y_{21}| + Re(y_{12} y_{21})\right]}{2}}\,\sqrt{\frac{g_{11}}{g_{22}}} - g_{11}$$

$$G_L = \sqrt{\frac{k\left[|y_{12} y_{21}| + Re(y_{12} y_{21})\right]}{2}} \cdot \sqrt{\frac{g_{22}}{g_{11}}} - g_{22}$$

$$B_s = \frac{(G_s + g_{11})\, Z_o}{\sqrt{k\left[|y_{12} y_{21}| + Re\, y_{12} y_{21}\right]}} - b_{11}$$

$$B_L = \frac{(G_L + g_{22})\, Z_o}{\sqrt{k\left[|y_{12} y_{21}| + Re(y_{12} y_{21})\right]}} - b_{22}$$

Where,

$$Z = \frac{(B_s + b_{11})(G_L + g_{22}) + (B_L + b_{22})\, k(L+M)/2(G_L + g_{22})}{\sqrt{k\,(L+M)}}$$

$$L = |y_{12} y_{21}|$$

$$M = Re(y_{12} y_{21})$$

Defining D as the denominator in G_T expression yields:

$$D = \frac{Z^4}{4} + \frac{[k(L+M) + 2M]\, Z^2}{2} - 2NZ\sqrt{k(L+M)} + A^2 + N^2$$

where, $A = \frac{k(L+M)}{2} - M,$

$N = Im(y_{12} y_{21}),$

and,

Z_o = that real value of Z which results in the smallest minimum of D, found by setting,

$$\frac{dD}{dZ} = Z^3 + [k(L+M) + 2M]\, Z - 2N\sqrt{k(L+M)}.$$

equal to zero.

$$G_T = \frac{4\, Re\,(Y_s)\, Re\,(Y_L)\, |y_{21}|^2}{|(y_{11} + Y_s)(y_{22} + Y_L) - y_{12} y_{21}|^2}$$

k	=	Stern's stability factor
G_s	=	Real part of the source admittance
G_L	=	Real part of the load admittance
B_s	=	Imaginary part of the source admittance
B_L	=	Imaginary part of the load admittance
g_{11}	=	Real part of y_{11}
g_{22}	=	Real part of y_{22}
Y_L	=	Complex load admittance
Y_s	=	Complex source admittance
G_T	=	Transducer gain
Y_{IN}	=	Input admittance
Y_{OUT}	=	Output admittance
G_{max}	=	Maximum gain without feedback

Computer solutions of these equations for various values of k versus frequency have been plotted in Appendix I for the 2N4957. These curves include common-base (Figures 10 through 16) and common-emitter (Figures 17 through 22).

From these curves, the designer can determine the input and output loading admittances for maximum power gain at a particular circuit stability. In addition, the transducer power gain under these conditions can also be determined. Thus the designer, rather than reading s or y parameters from a curve and using this information to design an amplifier, has all the design equations solved and presented in convenient, computer-derived design curves.

The following example demonstrates how these curves can be utilized in the design of a 1 GHz amplifier using the 2N4957. In addition, a second example is shown to demonstrate the special case where input admittance is determined primarily by noise figure considerations rather than by maximum power gain.

1 GHz AMPLIFIER DESIGN

A preliminary investigation of stability and power gain, common-emitter and common-base, can be quickly made from the design curves. For instance, the unilateralized gain (Figure 8) at 1 GHz is approximately 15 dB for either the common-emitter or common-base configuration. Also, the C factor for the common-base configuration (Figure 10) is greater than one and indicates potential device instability. However, the C factor for the common-emitter configuration (Figure 17) is less than one and indicates unconditional device stability.

Figures 16 and 22 are key curves that show transducer power gain for the common base and common emitter configuration respectively. Assuming a circuit stability factor of 4*, power gain is approximately 15 dB, common-base. Although the common-emitter curve is not extended to 1 GHz (since this is a region of unconditional stability) power gain for k = 4 would be obviously much less than 15 dB.

Using the common base configuration with k = 4, the required input and output admittance for maximum power gain can be determined directly from Figures 11 through 16.

For instance, the real part of the output admittance can be read from either Figure 11 or 12. Figure 12 is an expanded version of Figure 11 and is intended to facilitate lower frequency use. The imaginary portion of the output admittance is shown in Figure 13. Figures 14 and 15 show the real and imaginary portions of the input admittance respectively. The resultant input and output admittances are shown in Figure 1 and are summarized:

Conditions: (2N4957)

V_{CE} = 10 V
I_C = 2 mA
f = 1 GHz
G_T = 15 dB
k = 4

Input admittance = 69.5 mmhos +j27.1 mmhos
Output admittance = 1.53 mmhos -j7.46 mmhos

It becomes apparent that the emitter must "see" an admittance of 69.5 mmhos shunted by a susceptance of +j27.1 mmhos. The latter, in terms of a lumped constant element, would be a lossless capacitor. Likewise, the collector would be required to see an admittance of 1.53 mmhos shunted by -j7.46 mmhos. The latter, in terms of a lumped-constant element, would be a lossless coil. This loading will result in a stability factor, k, of 4 and a power gain of 15 dB, the maximum power gain possible for k = 4. This loading does not include stray capacitance. If stray capacitance is assumed to be 1 pF, the actual load is 1.53 mmhos -j13.5 mmhos (see Figure 1).

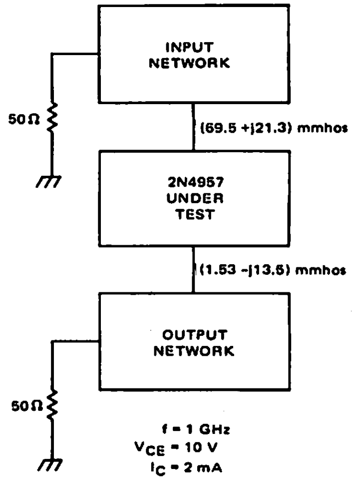

FIGURE 1 — COMMON BASE INPUT AND OUTPUT ADMITTANCES INCLUDING STRAY CAPACITANCE

To facilitate instrumentation, both the source and load impedance will be 50 ohms. This admittance level must be transformed to the required device loading admittance. Micro strip techniques provide a convenient method of achieving this transformation without circuit reproducibility and component loss problems that are common with many lumped constant circuits at this frequency.

The Smith Chart is a convenient design tool for solving transmission line problems of this type. Since space does not permit, familiarity with this chart will be assumed.

*For the purpose of this report a stability factor of 4 is chosen. Values of k less than 4 may not prove to be advantageous from the standpoint of regeneration and parameter spread.

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The same procedure is followed in designing the input network (see Figure 5). Again, a stray capacitance of 1 pF is assumed. Thus, the actual input loading becomes 69.5 mmhos +j21.3 mmhos. First, the 20 mmho load is plotted (see Point T, Figure 6). Next, point W is plotted (69.5 mmhos +j21.3 mmhos). Adjusting the SWR with C_3 (point V) allows a transmission line of length L_2 to transform the admittance at point V to the desired level at the base (point W).

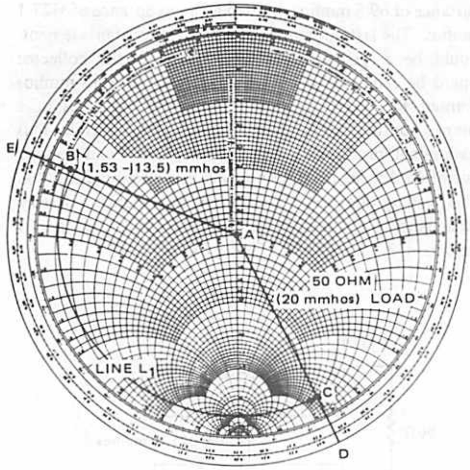

FIGURE 2 – OUTPUT NETWORK DESIGN

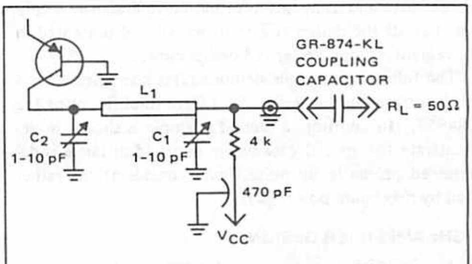

FIGURE 3 – OUTPUT NETWORK

Starting with the output circuit, both the 50 ohm (20 mmhos) load and the desired collector admittance are plotted on the Smith Chart (see Figure 2). As a starting point, a characteristic admittance of 20 mmhos will be assumed. First, the 20 mmho load is plotted (point A, Figure 2), then point B is plotted (1.53 mmhos -j13.5 mmhos).

Although many different methods exist for transforming point A to point B (see Figure 2), a direct, and as it turns out, practical approach is that shown in Figure 3. This circuit uses C_1 in parallel with R_L to vary the SWR of point A (Figure 2) to point C. Since point C has the same SWR as point B, a line L_1 with an electrical length equal to $0.405\lambda_2$ (point E) minus 0.214λ (point D) will complete the transformation. Collector tuning is available with component C_2. This variable capacitor provides the difference between the assumed stray capacitance and the actual circuit stray capacitance.

The required SWR could have been realized by using an inductor in place of C_1. However, an inductor would have either forced the bias feed-point to be changed to the collector lead or necessitated a dc- isolated coil. Although this is readily attainable using transmission line techniques, the variable component C_1 is more convenient. A typical curve of Q versus capacitance for (C_1) is shown in Figure 4.

The output bias is fed through a 4000 ohm resistor rather than an RF choke. The resultant 8 volt drop across this resistor is easier to contend with than the circuit instabilities sometimes associated with RF chokes.

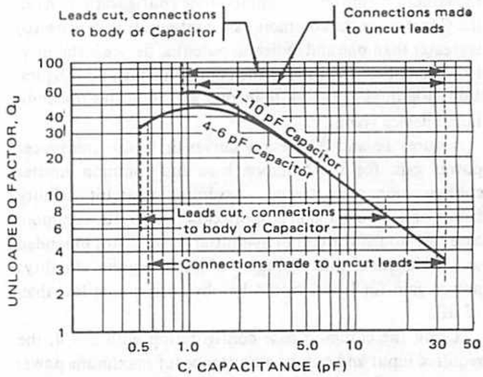

FIGURE 4 – Q versus CAPACITANCE FOR C_1 @ 1 GHz

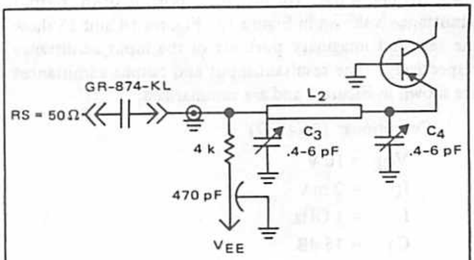

FIGURE 5 – INPUT NETWORK

CIRCUIT CONSTRUCTION

The transmission line lengths L_1 and L_2 are readily transferred to micro-strip lengths once the wavelength and line-width are known. Hopefully, this information is available from the manufacturer, but if not, it must be measured before the design can be completed. The laminate used for this application required a line-width of approximately 0.16 inches for a 20 mmho characteristic admittance. This value proved adequate both from a realizable design solution on the Smith Chart and also from a practicable circuit construction standpoint.

The actual laminate thickness depends to a large extent on the desired characteristic impedance and the frequency of operation The line thickness for a 50 ohm line is approximately 0.16 inch for a 1/16 inch laminate and approximately 0.035 inch for the same laminate 1/64 inch thick. As the intended frequency of operation is increased, the line width becomes a larger percentage of the line length.[4] Higher ratios of line width to length may result in undesirable modes of operation. Decreasing the laminate thickness results in a smaller line width for the same characteristic (assuming TEM operation) and a smaller line width to length ratio.

The dielectric constant for the material used was 2.6. The actual wavelength in the laminate is:

$$\lambda\,(\text{actual}) = \frac{\lambda\,(\text{air})}{\sqrt{2.6}} = \frac{11.8 \text{ inches}}{\sqrt{2.6}} = 7.34 \text{ inches}$$

Since $L_1 = 0.191\lambda$,

The physical length of L_1 is 1.4 inches

Correspondingly, L_2 is 0.062λ or 0.455 inches.

It should be pointed out that the actual wavelength[3] for this laminate is somewhat larger than that calculated from the dielectric constant. A careful measurement[4] of wavelength versus characteristic impedance (line width) demonstrates this phenomena. The slight increase in wavelength (6%) from that calculated using the dielectric constant was judged insignificant. However, this error increases for larger values of characteristic impedance and may prove to be quite significant for other laminates or narrower line widths. A good precaution would be to measure wavelength versus line width on each laminate used before TEM propagation is assumed.

Although the lines can be produced by a masking-etch process, adequate results can be obtained by cutting the desired strip from a thin copper sheet and glueing this strip to the teflon glass board. The latter is a convenient method for making rapid design changes.

The author observes several precautions which may or may not be necessary for all applications:

1. All breadboards have a ground strap which encompasses the outer periphery of the board. This strip is soldered to both the top and bottom copper sheets to effectively ground the outer periphery of the amplifier on all four sides. The circuit dimensions are held to a minimum to keep the ground planes as short as possible.

2. All RF connectors are carefully connected with grounding surfaces soldered to the ground plate. For instance, mount the connectors* perpendicularly to the board at a point where the connection to the center conductor is a minimum length. Completely solder the outer conductor to the copper sheet on the opposite side of the board. Poorly mounted connectors may result in poor transitions and unpredictable impedance transformations. For example, tacking the outer barrel of this connector to the line side of the board may seriously alter the predicted impedance level at the collector.

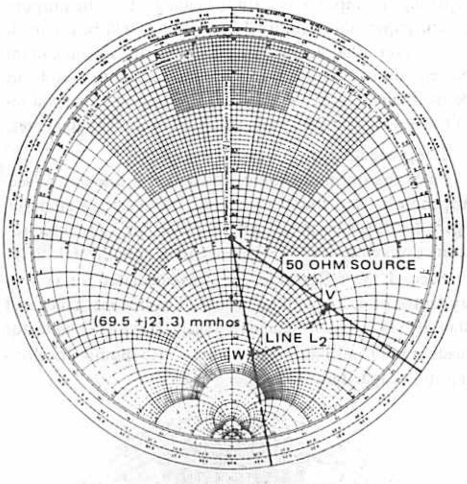

FIGURE 6 – INPUT NETWORK DESIGN

The amplifier was constructed as specified and the admittance levels were measured at the emitter and collector pins. These admittance levels were checked and adjusted to the original design values with C_1, C_2, C_3, and C_4

The 2N4957 was then soldered directly into the circuit with minimum lead length. The resultant power gain was 14.3 dB and the noise figure, 6.5 dB, which is within 1 dB of the original design requirements. Attempts to re-adjust the input loading and output loading for lower noise figure resulted in lower noise figure with decreased circuit stability. Although the circuit (adjusted for minimum noise figure) didn't oscillate, the calculated k factor from the resultant input and output admittances was approximately 2.

*General Radio Cable Connector 874-G58B.

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LOW NOISE DESIGN

Improvement in noise figure is possible by arbitrarily adjusting the input and output loading. For the purpose of this paper, the stability factor (k = 4) will be retained.

However, the design curves represent the maximum power gain case. Although the circuit stability factor can be maintained at k = 4, varying the source loading will result in less power gain than indicated in the design curves.

The procedure for this case is as follows:

First, the optimum source resistance is calculated (see Appendix) and found to be 43Ω.* The calculated noise figure for this source is 5 dB. In addition, the source reactance was empirically determined to be inductive (j119Ω).

Second, the collector loading was calculated for a stability factor of 4. Using these values of source resistance and stability factor, the calculated gain (G_T) and collector loading is 11.8 dB and 3.41 mmhos –7.5 mmhos (neglecting stray capacitance).

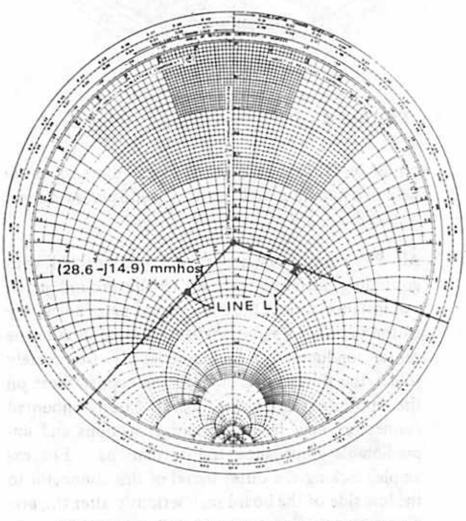

FIGURE 7 – LOW NOISE INPUT DESIGN

The output network was readily adjusted to the desired collector loading. However, the input line was too short and required re-design (see *Figure 7*). The calculated value of this line length is 1.15 inches as contrasted with .46 inches used in the first example. The complete amplifier is shown in Figure 9.

The resultant power gain and noise figure was 11.8 dB and 5.5 dB. These figures compare well with the calculated design.

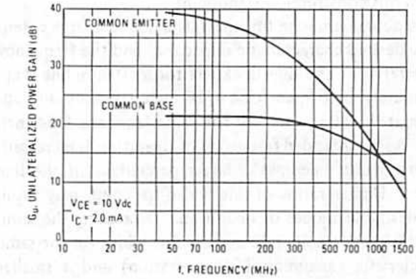

FIGURE 8 – UNILATERALIZED POWER GAIN versus FREQUENCY

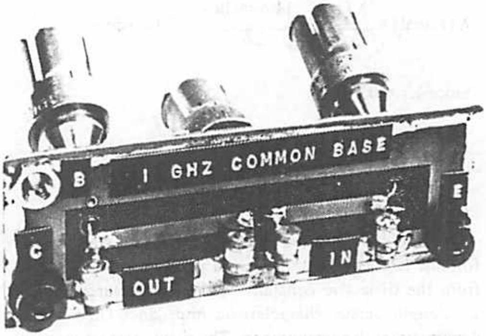

FIGURE 9 – 1 GHz AMPLIFIER

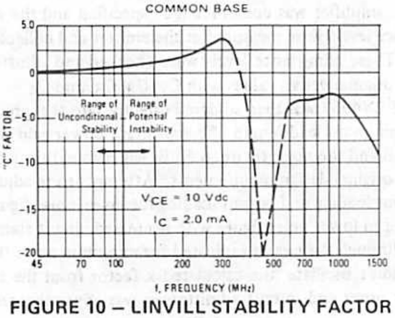

FIGURE 10 – LINVILL STABILITY FACTOR versus FREQUENCY

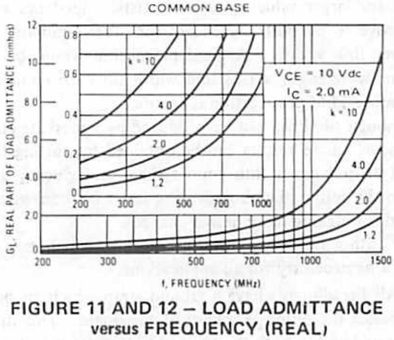

FIGURE 11 AND 12 – LOAD ADMITTANCE versus FREQUENCY (REAL)

*The actual value of optimum source resistance was empirically determined to be 35Ω. Consequently this value was used for the input circuit design rather than 43Ω.

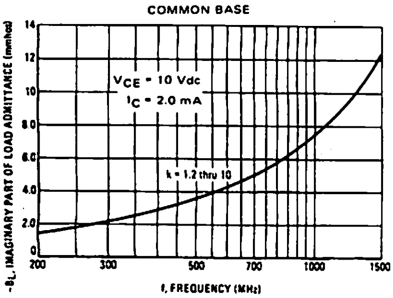

FIGURE 13 – LOAD ADMITTANCE versus FREQUENCY (IMAGINARY)

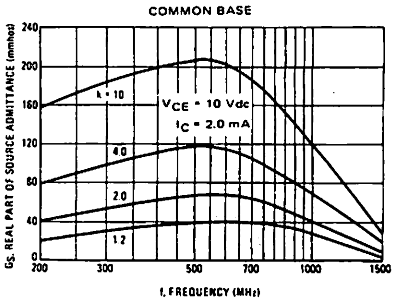

FIGURE 14 – SOURCE ADMITTANCE versus FREQUENCY (REAL)

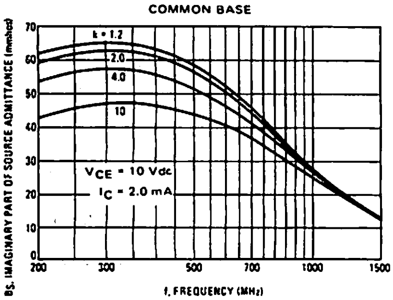

FIGURE 15 – SOURCE ADMITTANCE versus FREQUENCY (IMAGINARY)

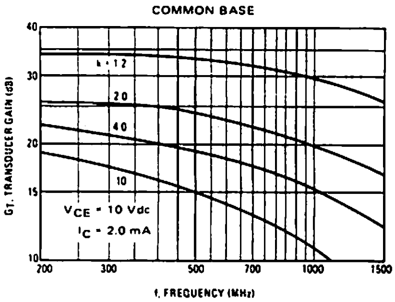

FIGURE 16 – TRANSDUCER GAIN versus FREQUENCY

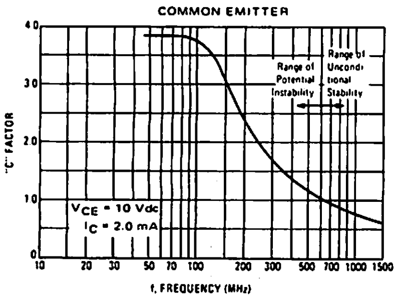

FIGURE 17 – LINVILL STABILITY FACTOR versus FREQUENCY

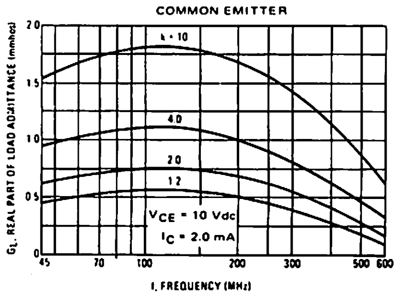

FIGURE 18 – LOAD ADMITTANCE versus FREQUENCY (REAL)

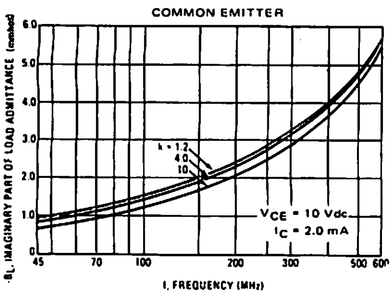

FIGURE 19 – LOAD ADMITTANCE versus FREQUENCY (IMAGINARY)

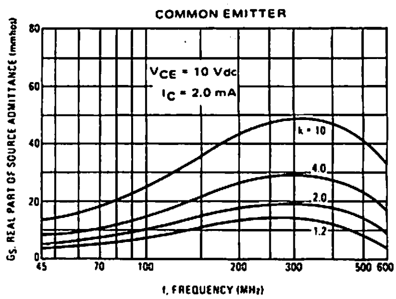

FIGURE 20 – SOURCE ADMITTANCE versus FREQUENCY (REAL

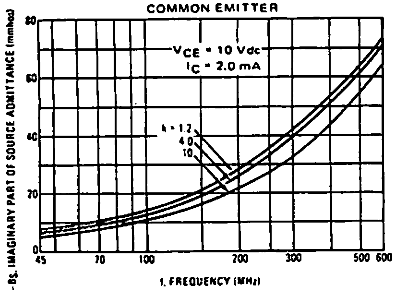

FIGURE 21 – SOURCE ADMITTANCE versus FREQUENCY (IMAGINARY)

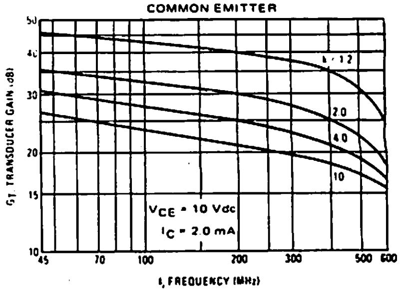

FIGURE 22 – TRANSDUCER GAIN versus FREQUENCY

APPENDIX

LOW NOISE DESIGN

The procedure followed in designing this amplifier is to first calculate the optimum source resistance for optimum noise figure and then calculate the collector loading for a required value of k.

A first approximation of optimum source resistance for optimum noise figure is:[2]

$$R_{gF(opt)} = \sqrt{k_2{}^2 + \frac{k_1}{k_3}}$$

$$k_1 = r_b + \frac{r_e}{2}$$

$$k_2 = r_b + r_e$$

$$k_3 = \frac{1 + (B_o + 1)\left(\frac{f}{f_{ab}}\right)^2}{2B_o r_e}$$

Assuming the above parameters for the 2N4957 are:

r_b = 12.5 ohms
r_e = 13 ohms
B_o = 40
f_{ab} = 1600 MHz,
$\therefore R_{gF(opt)}$ = 43 ohms

The noise figure using this source resistance is available from Nielsen's equation:[2]

$$NF = 1 + \frac{r_e}{2R_g} + \frac{r_b}{R_g} + \frac{(R_g + r_e + r_b)^2}{2\,B_o\,R_g\,r_e}\left[1 + (B_o + 1)\left(\frac{f}{f_{ab}}\right)^2\right]$$

Using the previous parameter values,

$$NF = 5\ \text{dB}$$

Since the impedance level is different at the base, the collector loading must be re-designed.

Using Stern's stability equator for k = 4 (see Table 1):

$$k = \frac{2\,(g_{11} + G_s)(g_{22} + G_L)}{|y_{12}y_{21}| + \mathrm{Re}\,(y_{12}y_{21})}$$

and calculating G_L for G_S = 25 mmhos (40 ohms)

$$G_L = 3.41\ \text{mmhos}$$

The transducer gain can be calculated from these impedance levels:

$$G_T = \frac{4\,\mathrm{Re}\,(Y_s)\,\mathrm{Re}\,(Y_L)\,|y_{21}|^2}{|(y_{11} + Y_s)(y_{22} + Y_L) - y_{12}y_{21}|^2}$$

$$G_T = 11.8\ \text{dB}$$

TABLE 1
f = 1 GHz V_{CB} = 10 V I_C = 2 mA
y_{ib} = 25 -j25
y_{ob} = 0.55 +j7.54
y_{fb} = -4.99 +j41
y_{rb} = -0.01 -j1.19

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3. F. Assadourian and E. Rimai, "*Simplified Theory of* Microstrip Transmission Systems", Proc. IRE, pp. 1651-1663, December 1953.
4. M. Arditi, "Experimental Determination of the Properties of Microstrip Components," Electrical Communication, December 1953.

MICROSTRIP DESIGN TECHNIQUES FOR UHF AMPLIFIERS

Prepared by:
Glenn Young

INTRODUCTION

This note uses a 25 watt UHF amplifier design as a vehicle to discuss microstrip design techniques. The design concentrates on impedance matching and microstrip construction considerations. A basic knowledge of Smith chart techniques is helpful in understanding this note. [1]

The amplifier itself, as shown in Figure 1, provides 25 watts of output power in the 450 - 512 MHz UHF band. It is designed for 12.5 volt operation which makes it useful for mobile transmitting equipment. A variety of police, taxi, trucking and utility maintenance communication systems operate in this band.

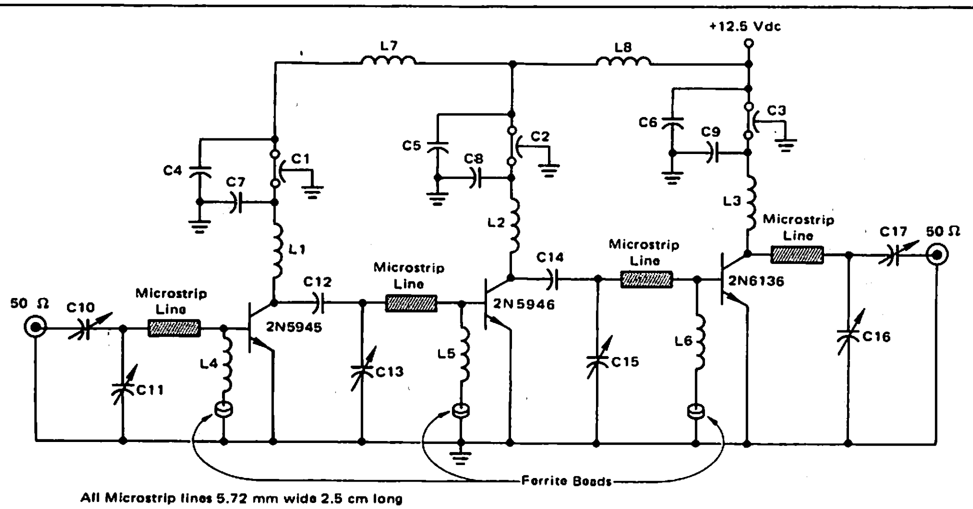
A summary of the performance of the completed amplifier operating with a 12.5 volt supply at 512 MHz indicates a power gain of 16 dB and a bandwidth (-1 dB) of 8 MHz. Overall efficiency is 48.5% and all harmonics are a minimum of 20 dB below the fundamental output.

Sections on construction and device handling considerations are also presented.

MICROSTRIP DESIGN CONSIDERATIONS

Microstrip design was used for this amplifier due to its inherent superiority over other methods at this frequency. These techniques not only offer good compatibility with the Motorola "stripline" package but they also offer very good reproducibility. Microstrip construction is more efficient than lumped constant equivalents since microstrip lines are less lossy than lumped constant components.

Microstrip board with Teflon bonded fiberglass dielectric rather than the higher dielectric constant ceramics was chosen due to the ease of working with that type of material. A substrate thickness of 1/16-inch is convenient since a line of the same width as the transistor leads (0.225 inch) produces a reasonable characteristic impedance (Z_O) of 40.65 ohms. The value of the characteristic impedance is



All Microstrip lines 5.72 mm wide 2.5 cm long

C1,2,3, 470 pf feedthru
C4,5,6 1.0 μf Tantalum
C7,8,9 0.1 μf Ceramic
C10,11,13,15,16,17 1.5-20 pf Compression Trimmer AHCO 420
C12,14 10 pf Microwave capacitor ATC type 100-B-10-M-MS or equiv.

L1, L2, L3 – 5 turns #20 Closewound 3/16" I.D.
L4, L5, L6 – 0.15 μh molded choke
L7, L8 – Ferroxcube VK 200 20/4B or equiv.
Ferrite beads are Ferroxcube 56 590 65/3B or equiv.

FIGURE 1 – Schematic Diagram of 25 W UHF Amplifier

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All that remains to finish the solution is to determine the amount of reactance necessary to reach the source at point F. To do this, it is first necessary to transpose point D, which is an admittance, to an impedance. This is accomplished by rotating point D one-quarter wavelength on a constant VSWR circle. This moves point D to point E which is on the 2.04 reactance line thus representing a series reactance of:

$$X_{CS} = (X_E) \bullet (Z_o) = (2.04) \bullet (40.65) = 82.9 \text{ ohms} \quad (13)$$

A series capacitance with this reactance is:

$$C_S = \frac{1}{(2\pi)(f)(X_{CS})} = \frac{1}{(2\pi)(470 \times 10^6)(82.9)} = 4.08 \text{ pF} \quad (14)$$

This completes the solution for the input network.

The interstage networks as well as the output network are solved in similar fashion with the following differences. In the case of the interstage networks when the imaginary term of the source impedance is other than zero, point F would be plotted at the complex conjugate of the source impedance. In the output network solution the "source" is the output load of the amplifier (50 + j0) and the "load" is the collector impedance of the output device.

	450 MHz	480 MHz	512 MHz
Power Gain	18 db	17.2 db	16 db
Bandwidth (-1 db)	5 MHz	6 MHz	8 MHz
Overall Efficiency	44.5%	46.5%	48.5%
Harmonics	All Harmonics Better Than -20 db		
Stability	Amplifier Stable under all Conditions of Drive down to V_{CC} = 5.0 volts		
Power Output	25 w	25 w	25 w
Burnout	No Damage to any Transistor with Load Open & Shorted with 0 to ± 180° Phase Angle		

FIGURE 5 – Typical Performance Specifications

Figure 5 gives details on the performance of the completed amplifier. The use of the porcelain dielectric chip capacitors for the series elements in the interstage networks was found to provide an additional 2.5 to 3.0 dB of gain over that obtained with compression trimmers as well as reducing the number of tuning adjustments necessary.

CONSTRUCTION CONSIDERATIONS

As in all RF power applications, solid emitter grounds are imperative. In microstrip amplifiers gain can be increased more than 1 dB by grounding both of the emitter leads to the bottom foil of the microstrip board by wrapping strips of copper foil thru the transistor mounting hole as shown in Figure 6.

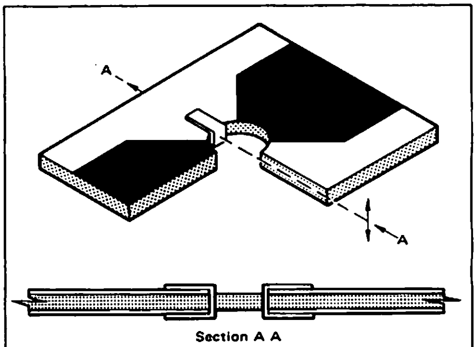

FIGURE 6 – Proper Emitter Grounding Method

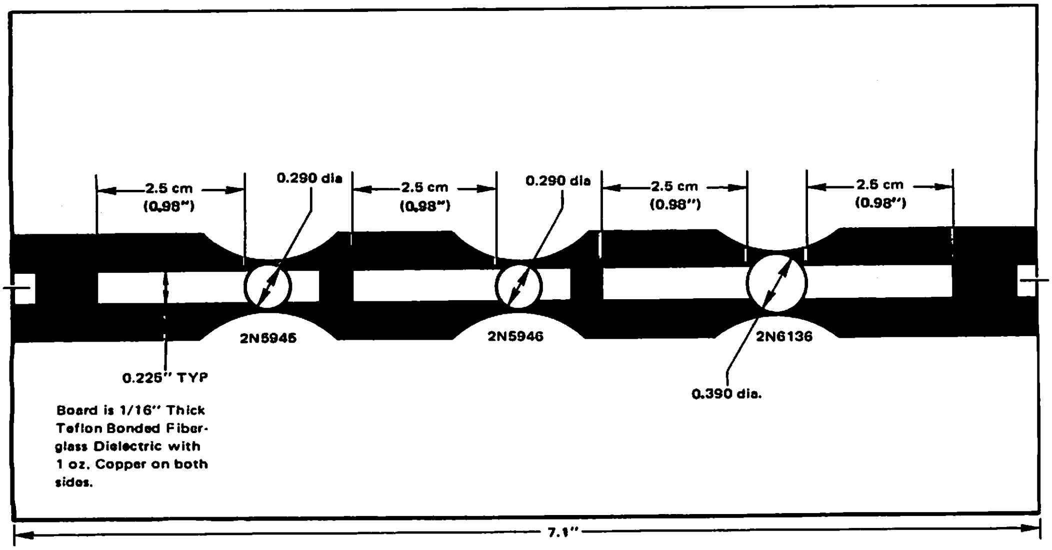

FIGURE 7a – Microstrip Board Layout

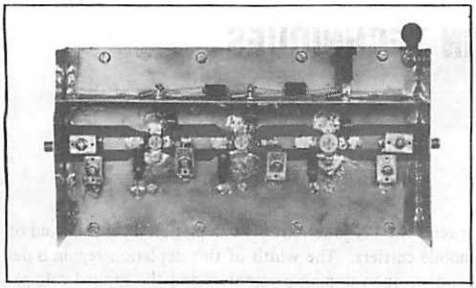

FIGURE 7b – Photograph of Amplifier

Stability under normal operating conditions is essential, however, stability should be maintained over as wide a range of supply voltage and drive levels as possible. If amplifier stability is maintained at all RF drive levels with the supply voltage reduced to between three and five volts, the designer can be practically certain that the amplifier will remain stable under all conditions of load. Maintaining stability is a key factor in protecting these transistors from damage. In a stable amplifier that has adequate heat sinking, these transistors will withstand high VSWR loads including open and shorted loads without damage. The major controlling factors in obtaining wide range stability are:

1) Mechanical layout: Good mechanical layout includes good emitter grounds (as previously described), compact layout and short ground paths.

2) Biasing: The devices are all zero biased for Class "C" operation. The use of relatively low Q base chokes with ferrite beads on the ground side will maintain good base circuit stability. In some applications, the use of a resistor in series with the ground side of the base chokes on the output and driver stages may enhance the stability. Approximate values of these resistors should be 10 ohms, 1/2 watt for the driver and 1.0 ohms, 1/2 watt for the output device. The addition of these series resistors will cause a slight loss in gain; (about 0.1 to 0.2 dB overall).

3) Collector supply feed method: The collector supply feed system is designed to provide decoupling at or near the operating frequency and a low collector load impedance at frequencies much lower than the operating frequency.

4) Heat sinking: In order to protect against burnout under all conditions of load, adequate heat-sinking must be provided. In heat sinking the device it is imperative to use a good grade of thermal compound, such as Dow-Corning 340, on the interface between the device and its heat sink.

Figure 7a shows the microstrip board layout while Figure 7b is a photo of the completed amplifier.

DEVICE HANDLING CONSIDERATIONS

Although the Motorola stripline package is a rugged assembly, some care in its handling should be observed. The most important mechanical parameter is stud-torque, specified on the data sheet at 6.5 inch-pounds maximum. This data sheet specification is an absolute maximum and should not be exceeded under any circumstances. A good limit to use in production assembly is 6 inch-pounds and if for any reason repeated assembly/dissassembly is required torque should be limited to 5 inch-pounds.

Another major precaution to observe is to avoid upward pressure on the leads near the case body. Stresses of this type can crack or dislodge the cap. This type stress sometimes occurs due to adverse tolerance build-up in dimensions when the device is mounted thru a microstrip board onto a heat sink. Many times this type of stress is applied even in the most carefully thought out designs due to solder build-up on the copper foil when a device is replaced. In device replacement care should be taken to flow all solder away from the mounting area before the stud nut is torqued. Finally, one must be sure to torque the stud nut before soldering the device leads. Refer to Motorola Application Note AN-555 for details on mounting Motorola "stripline packaged transistors.

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TUNING DIODE DESIGN TECHNIQUES

Prepared by:
Doug Johnson

INTRODUCTION

Voltage variable capacitors or tuning diodes are best described as diode capacitors employing the junction capacitance of a reverse biased PN junction. There is a wide range of available capacitances and different device types. The capacitance of these devices varies inversely with the applied reverse bias voltage.

Tuning diodes or Motorola's "Epicaps*" have several advantages over the more common variable capacitor. They are much smaller in size and lend themselves to circuit board mounting. They are available in most of the same capacitance values as air variable capacitors. Tuning diodes offer the designer the unique feature of remote tuning.

Epicaps, as opposed to earlier versions of voltage variable capacitors exhibit many new improvements. Lower leakage, significantly higher Q and uniformity are just some of these advantages. However, the capacitance of all tuning diodes inherently varies with temperature and may require compensation. A simple scheme is available for compensation of the temperature drift, resulting in stabilities as good as, or better than, that of air capacitors. This note contains the details for compensating Motorola's Epicap diodes.

SIMPLIFIED THEORY

A tuning diode is a silicon diode with very uniform and stable capacitance versus voltage characteristics when operated in its reverse biased condition. In accordance with semiconductor theory, a depletion region is set up around the PN junction. The depletion layer is devoid of mobile carriers. The width of this depletion region is dependent upon doping parameters and the applied voltage. Figure 1A shows a PN junction with reverse bias applied, while Figure 1B shows the analogy, a parallel plate capacitor. The equation for the capacitance of a parallel plate capacitor given below predicts the capacitance of a tuning diode.

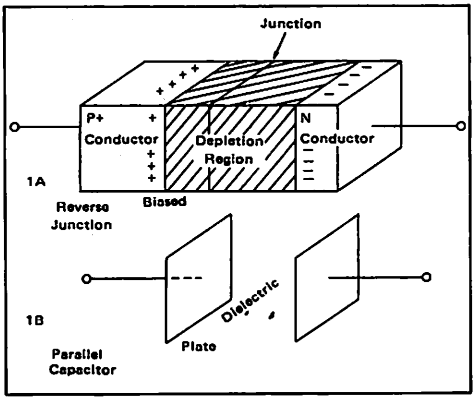

FIGURE 1 — Tuning Diode Capacitor Analogy

$$C = \frac{\epsilon A}{d} \tag{1}$$

where ϵ = dielectric constant of silicon equal to $11.8 \times \epsilon_0$
$\epsilon_0 = 8.85 \times 10^{-12}$ F/m
A = Device cross sectional area
d = Width of the depletion layer.

The depletion layer width d may be determined from semiconductor junction theory.

The more accepted method of determining tuning diode capacitance is to use the defining formula for capacitance.

$$C = \frac{dQ}{dV} \tag{2}$$

The charge, Q per unit area, is defined as:

$$Q = \epsilon E \tag{3}$$

where E = Electric field

So we have capacitance per unit area:

$$c = \frac{C}{A} = \epsilon \frac{dE}{dV} \tag{4}$$

Norwood and Shatz[1] use these ideas to develop a general formula:

$$c = \left[\frac{q B \epsilon^{m+1}}{(m+2)(V+\phi)}\right]^{1/m+2} \tag{5}$$

m = Impurity exponent
c = Capacitance per unit area

Lumping all the constant terms together, including the area of the diode, into one constant, C_D, we arrive at:

$$C_J = \frac{C_D}{(V+\phi)^{\gamma}} \tag{6}$$

where γ = Capacitance Exponent, a function of impurity exponent
ϕ = The junction contact potential ($\approx$ 0.7 Volts)

7

The capacitance constant, C_D, can be shown to be a function of the capacitance at zero voltage and the contact potential. At room temperature we have:

$$C_D = C_o(\phi)^{\gamma} \quad (7)$$

C_o = Value of capacitance at zero voltage

The simple formula given in Eq. 6, very accurately predicts the voltage-capacitance relationship of Epicaps. There are many detailed derivations [1,2,3,4,5] of junction capacitance, so further explanation is not necessary in this note.

The capacitance of commercial tuning diodes must be modified by the case capacitance.

The equation then becomes:

$$C = C_c + C_J \quad (8)$$

where

C_c = Case capacitance typically 0.1 to 0.25 pF

C_J = Junction capacitance given by equation 6.

TUNING RATIOS

The tuning or capacitance ratio, TR, denotes the ratio of capacitance obtained with two values of applied bias voltage. This ratio is given by the following expression for the Epicap junction.

$$TR = \frac{C_J(V_2)}{C_J(V_1)} = \left[\frac{V_1+\phi}{V_2+\phi}\right]^{\gamma} \quad (9)$$

where $C_J(V_1)$ = Junction capacitance at V_1

$C_J(V_2)$ = Junction capacitance at V_2

where $V_1 > V_2$

In specifying TR, some Epicap data sheets use four volts for V_2. However, in order to achieve larger tuning ratios, the devices may be operated at slightly lower bias levels with some degradation in the Q specified at four volts. (See the discussion of Q versus voltage in the circuit Q section, later in this note). Furthermore, care must be taken when operating Epicaps at these low reverse bias levels to avoid swinging the diode into forward conduction upon application of large ac signals. These large signals may also produce distortion due to capacitance modulation effects.

Since the effects of ϕ and case capacitance, C_c, are usually small, Eq. 9 may be simplified to the following for most design work:

$$TR = \frac{C(V_{min})}{C(V_{max})} = \left(\frac{V_{max}}{V_{min}}\right)^{\gamma} \quad (10)$$

The frequency ratio is equal to the square root of the tuning ratio. This tunable frequency ratio assumes no stray circuit capacitance.

Another parameter of importance is γ, the capacitance exponent. Physically, γ depends on the doping geometry employed in the diode. Varactor diodes with γ values from 1/3 to 2 can be manufactured by various processing techniques. The types of junctions, their doping profiles, and resulting values of γ are shown in Figure 2. These graphs show the variation of the number of acceptors (N_A) and the number of donors (N_D) with distance from the junction.

Abrupt junctions are the easiest to manufacture and most Epicaps are of this type. This type of junction gives a γ of approximately 1/2 and a tuning ratio on the order 3 with the specified voltage range. Therefore the corresponding frequency range which may be tuned is about 1.7 to 1.0. A typical example is the MV2101:

$$C(V_2) = C(30\text{ V}) = 2.5\text{ pF}$$
$$C(V_1) = C(4\text{ V}) = 6.8\text{ pF}$$
$$TR = 2.7$$
$$\gamma = 0.47$$

The subscripts on the capacitance refer to the bias voltage applied.

In many applications, such as tuning the television channels, or the AM broadcast band, a wider frequency range is required. In this event, the designer must use a hyper-abrupt junction Epicap. The hyper-abrupt diode has a γ of 1 or 2, and much larger frequency ranges. Table I shows typical types of tuning diodes available, their tuning ratios, frequency ratios and junction types.

TABLE I SAMPLE TUNING DIODE TYPES

Device Series	Capacitances Available	Tuning Ratio	γ	Frequency Ratio	Junction Type
1N5139	47-6.8 pF	2.7-3.4	0.47	1.6-1.8	Abrupt
MV2101	100-6.8 pF	1.6-3.3	0.47	1.6-1.8	Abrupt
BB105	10 pF	4-6	1.0	2-2.4	Hyper-Abrupt
MV1400	550-120 pF	10-14	2.0	3.2-3.7	Hyper-Abrupt
MV109	30 pF	5-6.5	1.0	2.2-2.5	Hyper-Abrupt

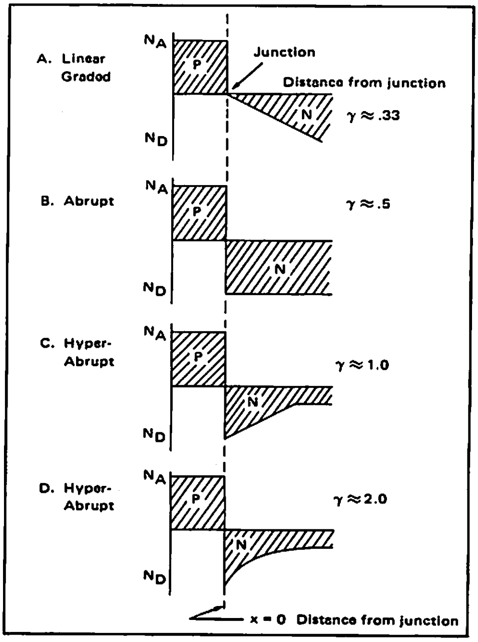

FIGURE 2 — Doping Profiles and Capacitance Exponent for Some Common Tuning Diode Types

The hyper-abrupt devices are constructed with special epitaxial growth and diffusion techniques, which creates a doping profile similar to that shown in Figures 2C and 2D. The Q of the BB105 and MV109 series hyper-abrupt diodes is as high as abrupt junction Epicaps. Their capacitance range is from a few picofarads to 10 or 20 pF, and their major application is in television tuners. The MV1400 series are high capacitance devices for applications below 10 MHz. They are suitable for tuning elements in AM broadcast band receivers and similar low frequency applications.

CIRCUIT Q

Popular types of mechanical tuning capacitors often have Q's on the order of a thousand or greater. The Q of tuned circuits using these capacitors is generally dependent only on the coil. When using an Epicap, however, one must be conscious of the tuning diode Q as well. The Q of the tuning diode is not constant being dependent on bias voltage and frequency. The Q of tuning diode capacitors falls off at high frequencies, because of the series bulk resistance of the silicon used in the diode. The Q also falls off at low frequencies because of the back resistance of the reverse-biased diode.

The equivalent circuit of a tuning diode is often described as shown: [7]

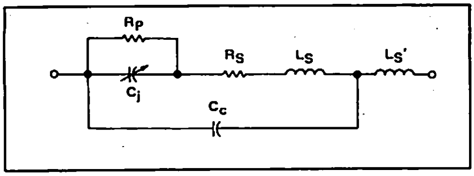

FIGURE 3 – Equivalent Circuit of Epicap Diode

where

R_P = Parallel resistance or back resistance of the diode
R_S = Bulk resistance of the silicon in the diode
L_S' = External lead inductance
L_S = Internal lead inductance
C_C = Case capacitance

Normally we may neglect the lead inductance and case capacitance. This results in the simplified circuit of Figure 4.

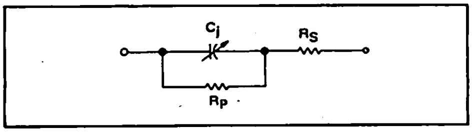

FIGURE 4 – Simplified Equivalent Circuit of Epicap Diodes

The tuning diode Q may be calculated with equation 11.

$$Q = \frac{2\pi fC\, R_p^2}{R_s + R_p + (2\pi fC)^2 R_s R_p^2} \qquad (11)$$

This rather complicated equation is plotted in Figure 5 for

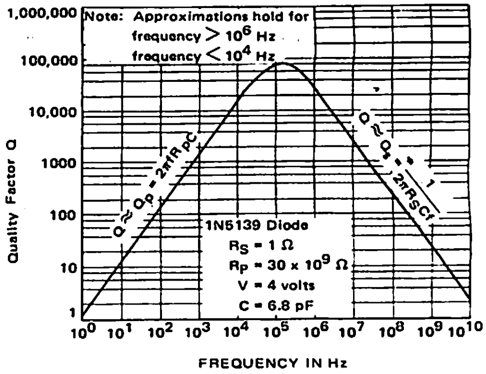

FIGURE 5 – Graph of Q versus Frequency

R_S = 1.0 ohm, R_P = 30 x 10^9 ohms, at V = 4 volts and C = 6.8 pF, typical for a 1N5139 Epicap at room temperature.

At frequencies above several MHz, the Q decreases directly with increasing frequency by the simpler formula given below:

$$Q \approx Q_S = \frac{1}{2\pi fCR_s} \quad \text{(High frequency Q)} \qquad (12)$$

The emphasis today is on decreasing R_s so better high frequency Q can be obtained. At low frequencies Q increases with frequency since only the component resulting from R_P, the back resistance of the diode, is of consequence.

$$Q \approx Q_P = 2\pi fCR_P \text{ (Low frequency Q)} \qquad (13)$$

Q is also dependent on voltage and temperature. Higher reverse bias voltage yields a lower value of capacitance, and also since R_s decreases with increasing bias voltage, the Q increases with increasing voltages. Similarly, low reverse bias voltages accompany larger capacitances, and lower Q's. Increasing temperature also lowers the Q of tuning diodes. As the junction temperature increases, the leakage current

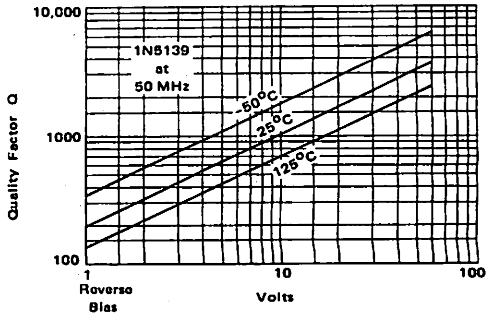

FIGURE 6 – Q versus Reverse Bias and Temperature

increases, lowering R_p. There is also a slight decrease in R_s with increasing temperature, but the effects of the decreasing R_p are greater and this causes the Q to decrease. The effects of temperature and voltage on the Q of a 1N5139 at 50 MHz are plotted in Figure 6.

TEMPERATURE

The Q and tuning ratio of Epicaps are parameters that every design engineer must be aware of in his circuits. Another equally important characteristic of tuning diodes is their temperature coefficient. A typical example of the capacitance versus temperature drift is shown in Figure 7.

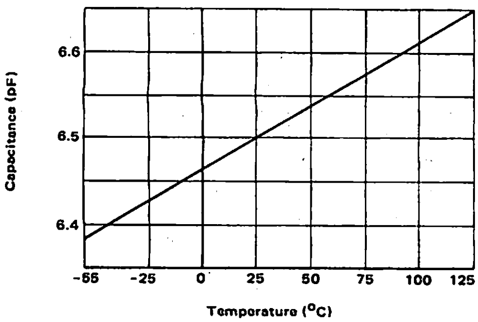

FIGURE 7 – Capacitance versus Temperature for a MV2101 Epicap Biased at 4 Volts

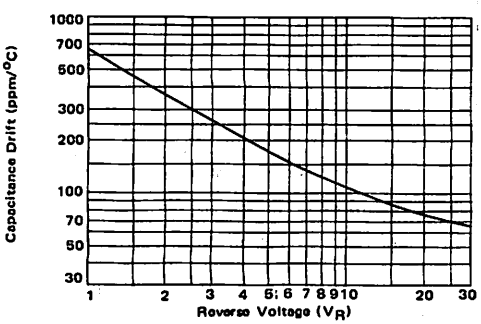

FIGURE 8 – Capacitance Drift in ppm/°C versus Voltage MV2101 Diode

The temperature constant, T_C, is a function of applied bias. Figure 8 shows T_C for a typical Motorola Epicap. Note that for low bias levels, on the order of a volt or two, the T_C is as high as +600 parts per million per degree centigrade (ppm/°C). This represents a frequency change of -300 ppm/°C which at 100 MHz means a frequency shift of 30 kHz per degree. It is obvious that a temperature compensation scheme is desirable for any frequency control not using feedback techniques.

In Figure 9, the actual capacitance drift of a MV2101 per degree centigrade is plotted. The graph illustrates that

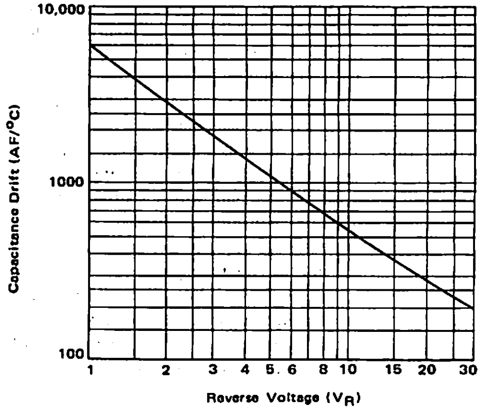

FIGURE 9 – Capacitance Drift in Attofarads/°C versus Voltage for the MV2101 Tuning Diode

Attofarads = (pF x 10^{-6})

a simple negative temperature coefficient compensating capacitor will not compensate for the tuning diode T_C because the change in capacitance is not constant with voltage.

A popular method of temperature compensating Epicaps involves the use of a forward biased diode. The voltage drop of a forward biased diode decreases as the temperature rises, thus applying a changing voltage to the Epicap. In the network shown in Figure 10, an increase in temperature

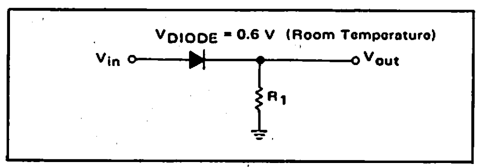

FIGURE 10 – Simple Temperature Compensating Network

will result in a decrease of the diode voltage V_{DIODE} to perhaps 0.5 V. If V_{in} is maintained constant, the available output voltage V_{out} will rise by 0.1 V. This increase in output voltage will lower the capacitance of the tuning diode and partially offset the initial capacitance increase caused by the temperature change. This method has been explored in detail and specific compensating circuits for Epicaps have been designed. The following sections describe the results of this work.

THEORY OF TEMPERATURE CHANGE

Before proceeding further with schemes to correct the temperature drift, it is informative to investigate the physical mechanisms responsible for the changing capacitance. Equations 6 and 8 may be combined to give the basic expression for capacitance below:

$$C = \frac{C_d}{(V+\phi)^{\gamma}} + C_c \qquad (14)$$

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We can pinpoint the terms in Eq. 14 that may account for capacitance changes. The contact potential, ϕ, is a strong function of temperature, varying on the order of -2 mV/^{o}C. C_d is a function of geometric dimensions which can change with temperature and ϵ which changes with temperature. Case capacitance also changes with temperature. For this analysis we will assume the only terms not temperature dependent are the supply voltage V, and the capacitance exponent, which is a function only of the slope of the doping profile.

The contact potential, ϕ, is readily calculated from semiconductor theory, and the equations predict a large change with temperature. This change in ϕ will produce a much larger change in capacitance for lower voltages than for higher voltages, and therefore accounts for the majority of capacitance change in tuning diode temperature drift. See Table II.

TABLE II

Calculated capacitance change versus applied voltage in ppm/^{o}C for:

$$\frac{d\phi}{dT} = -2 \text{ mV}/^{o}\text{C}$$

$$C = \frac{C_d}{(V+\phi)^{\gamma}} + C_c$$

Applied Bias Voltage (Volts)	Capacitance Drift In (ppm/^{o}C)
1	587
2	261
4	204
10	88.7
20	45.6
30	30.7

Comparing Table II with Figure 8, we see that a +40 to +50 ppm/^{o}C temperature drift still remains. Therefore ϕ is not the only mechanism responsible for temperature drift and others must be sought. There is a change with temperature in physical dimensions in any material which has an affect on the order of 1 ppm/^{o}C for a tuning diode. However, this change is too small to be of any significance. Another possibility is a change in dielectric constant. Silicon, depleted of its charge carriers, forms a dielectric layer with a relative dielectric constant of 11.8. The dielectric constant of silicon has a temperature coefficient of +35 ppm/^{o}C. [1] These effects change the value of C_d with temperature.

Another effect which sometimes must be considered is the change in case capacitance with temperature. The case capacitance is about 0.25 pF for the plastic TO-92 case. And there is a change of +25 AF (attofarads = 10^{-6} pF) per degree centigrade. The glass DO-7 case exhibits a capacitance of about 0.20 pF and a change of +30 AF/^{o}C. These are small changes for most low voltage capacitances, but become increasingly important as the voltage is increased and capacitance is reduced. Also these effects are only important for the low capacitance devices. For instance, consider the 1N5139 series which are packaged in the DO-7 glass case. Table III shows how large an effect case capacitance has on the capacitance drift of these diodes.

TABLE III Effect Of Case Capacitance Changes On 1N5139 And 1N5148 Epicaps

Bias Voltage (Volts)	1N5139 Capacitance (pF)	1N5139 Changes attributable to case capacitance (ppm/^{o}C)	1N5148 Capacitance (pF)	1N5148 Changes attributable to case capacitance (ppm/^{o}C)
2.0	8.9	3.4	61	0.5
4.0	6.4	4.7	47	0.6
10.0	4.8	6.3	32	1.0
30.0	3.0	10.0	19	1.6
60.0	2.2	14.0	13	2.3

In summary, the largest changes are caused by the change in contact potential. This effect is most noticeable at low voltage, high capacitance levels. The change in silicon dielectric is the next most important factor providing a change that is uniform for all devices and voltages. Case capacitance changes are most noticeable in the low capacitance, high voltage range, and may be neglected for all devices except those low capacitance devices.

THE POWER SUPPLY

We previously assumed that the supply voltage did not change with temperature. This is rarely the case, and special consideration must be given to this part of the design. All our efforts to temperature compensate the tuning diode may be in vain if the power supply has a large T_C or is otherwise unstable. Figure 11 shows the common method of supplying voltage to a tuning diode.

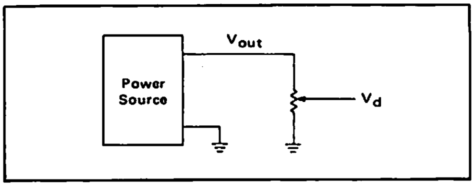


FIGURE 11 — Common Means of Supplying Bias Voltage to a Varactor Diode

POWER SOURCE

The power source is the most critical part of the circuit in Figure 11. It must be extremely stable in order to achieve good varactor tuning stability. The full drift of the power supply as expressed in ppm/^{o}C will appear at V_d regardless of the setting of the potentiometer. For example, if V_{out} is 40 volts with a drift of 100 ppm/^{o}C (4 mV/^{o}C), V_d may be 10 V, but *will still have a drift* of 100 ppm/^{o}C (1 mV/^{o}C). A 50 ppm/^{o}C stability figure in V_d translates into a 25 ppm/^{o}C stability of capacitance, when the capacitance exponent is 0.5. For hyper-abrupt junctions we realize capacitance stabilities of 50 and 100 ppm/^{o}C for exponents of 1 and 2 respectively.

There are many differing power supply regulators available to the designer. Zener diodes are relatively inexpensive, but have a poor temperature coefficient. Temperature compensated zeners are very expensive and have a limited voltage range. The MC1723, a monolithic integrated circuit voltage regulator, has excellent temperature characteristics, 37 volt output capability, and wide temperature range.

TABLE IV Summary of Power Regulators

Device	Voltage Range	Temperature Range	Voltage ppm/°C Max T_C	Voltage ppm/°C Typical T_C	Capacitance ppm/°C Typical γ = 0.5	Relative cost
1N5260 Zener	33	-65 +200°C	975	975	475	Low
1N4752 Zener	33	-65 +200°C	850	850	425	Low
1N3157 Temperature Compensated Zener	8.4	-50 +125°C	10	10	5	High
MC1723 Regulator	37	-55 +125°C	20	12	6	Medium
MFC6030 Functional Regulator	32	0° +70°C	50	15	7.5	Low
MC7800 Fixed Voltage Regulators	28	0° +125°C		40-60	20-30	Medium
MVS460 TO-92 Regulator	31 V	0 +70°C	-100 +50	-25	12	Low

Notes:
1) See Figure 12 for some typical circuit connections
2) More information on regulators is available in literature 8,9,10
3) To compute frequency change (ppm/°C), divide capacitance (ppm/°C) change by 2.

The MFC6030 Functional* integrated circuit is less costly and exhibits almost as good a temperature constant.

The MC7800 fixed output voltage regulators are extremely simple to use in that they have only input, output and ground terminals and require no external components other than possibly a high frequency bypass capacitor. (The latter item is generally required with all IC regulators to prevent high frequency oscillations).

The MVS460 is a two leaded IC regulator especially designed for use with tuning diodes. It represents a simple, inexpensive solution to the voltage regulator problem. Table IV contains a summary of available power supply regulators.

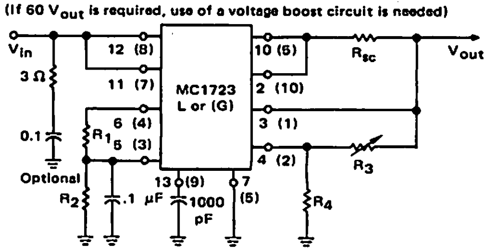
VARIABLE RESISTOR

The variable resistor is considerably less critical. Since it is being used as a voltage divider, all that is required is that the resistive material be uniform so any change in resistance is uniform throughout the potentiometer. Wire wound, and special high quality cermet film variable resistors are suitable for these applications. Generally speaking, a linear potentiometer should have a T_C of $\pm$150 ppm/°C or better. Special taper potentiometers should have a T_C of $\pm$50 ppm/°C or better.

The variable resistance cannot be made too large or there will be appreciable voltage drop as the reverse current in the diode increases. The reverse current in a silicon diode generally doubles every 10°C so this becomes an important problem at temperatures above 50°C. If the temperature is expected to run as high as 70°C, one must limit the variable resistor to 50 kΩ or the effect will be a greater than 5 ppm/°C capacitance change. If 50°C is the upper temperature limit, the resistance may be upped to 150 kΩ. These values apply to all of Motorola's Epicap series. When the tuning diodes are used in applications where temperature will greatly exceed 70°C, the divider resistance should be kept below 10 kΩ. This low value requires large power supply currents and would be undesirable in some applications. However, since the Motorola MC1723 is the recommended power source at these temperatures, voltage control may be accomplished using the regulator without relying on an external divider potentiometer, as shown in Figure 12A. The MC1723's low output impedance of 0.05 ohms will easily and reliably handle the change in current demanded by the Epicap as it heats up. Figure 12B shows another popular regulator circuit. If higher or lower voltages are needed, schemes such as voltage boost[8] and floating regulators may be used.

*Trademark of Motorola Inc.

(If 60 V_{out} is required, use of a voltage boost circuit is needed)



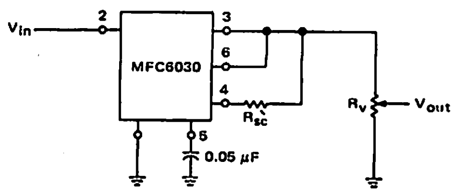
Numbers in parenthesis refer to G package.

R_{sc}	10 Ω	¼W	10%
R_1	5 kΩ	1%	Accurately Match T_C to within better than 20 ppm/°C.
R_2	2 kΩ	1%	
R_3	0-50 kΩ		50 ppm/°C potentiometer
R_4	2 kΩ	1%	20 ppm/°C

V_{in} = 40 V

V_{out} variable 2-37 Volts

FIGURE 12A – High Stability Regulator -50 to +125°C



V_{in} = 35 Volts max

R_{sc} = 20 Ω ¼W 10%

R_v = Variable Resistor feeding the Epicap

$R_v \approx$ 50 k 50 ppm

V_{out} 0-33 Volts

FIGURE 12 B – Regulator Using MCF6030, 0° – 70°C

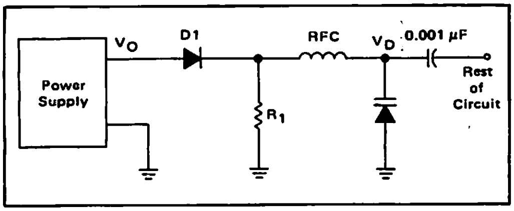


FIGURE 13 — Temperature Compensation Using A Silicon Diode

TEMPERATURE COMPENSATION

It has been previously noted that the most effective means of temperature compensation is simply to use a silicon junction biased in the forward direction. A circuit employing this technique is shown in Figure 13.

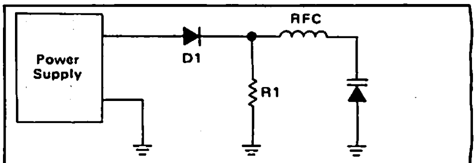
Diode D1 has a forward voltage drop on the order of 0.6 volts, and a temperature coefficient of -0.002 V/°C. Assuming a constant voltage from the supply, the reduction in diode voltage with increasing temperature, increases the voltage available to the tuning diode, V_D. The higher tuning diode voltage, V_D, lowers the capacitance enough to compensate for the increase due to temperature. However, merely using a random diode with an arbitrary value of R1 will not result in very accurate temperature compensation.

Different correction devices exhibit different T_C (changes in voltage drop with temperature) values because of differing doping schemes. For example, a typical Epicap exhibits a T_C of approximately $-$ 1.5 mV/°C while some high current rectifier junctions measure as high as -2.6 mV/°C. So it is necessary to investigate many different junction devices in order to find a diode that adequately compensates the tuning diode drift.

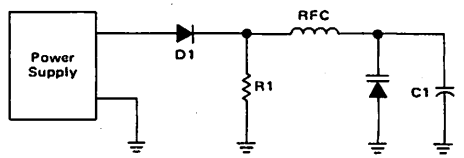
The tuning diode's change with temperature must be accurately determined. Also of major importance is the value of R1. A typical junction may have a T_C of -1.5 mV/°C at 10 mA junction current, and a T_C of -2.8 mV/°C at 1 μA junction current. Thus the value of R1, the bias resistor, must be chosen to yield the optimum value of compensating diode current.

Detailed analysis was performed on 160 low cost junction devices in order to arrive at suitable compensation schemes for Motorola's Epicaps. The results appear in Table V. The correction diodes represent the devices which provided the most accurate and reliable compensation. A computer program was devised to optimize the value of Rl in each case. Two different methods of compensation were analyzed. Method one searches for the lowest ppm values without using C1, the temperature compensating capacitor. At some voltages the temperature corrected tuning diode will have a negative temperature coefficient, while at others it will be positive. In general the results are better than ±50 ppm over the entire range from 2 volts to the breakdown voltage of the Epicap diode.

Method two attempts to cluster the residual capacitance at some standard value after the diode has performed its correction. This value (due to silicon dielectric change, case capacitance change, etc.) is easily "tuned out" by means of a small negative temperature coefficient capacitor.



METHOD ONE — Schematic Diagram



METHOD TWO — Schematic Diagram

Note 1: To find the value of negative temperature coefficient capacitor, C1, use equation 15.

$$C_1 = \frac{C_X \cdot C_{TD}}{N} \text{ in pF} \qquad (15)$$

where

C_X = Value listed above in Table V
C_{TD} = Capacity in pF of the tuning diode at four volts
N = Temperature coefficient of capacitor.
If a N750 is used, N = 750.

Note 2: For MV2305 series, the ppm/°C drift values specified hold for 1.5 V to the breakdown voltage.

Consideration must be given to the stability of R1. As the resistance of R1 increases with changing temperature, less current will be drawn through D1, thus decreasing its voltage drop. The result will be a rise in the voltage applied to the Epicap. Analysis of this effect is shown in Table VI.

The results of using a MV2111 in the compensation circuits are shown in Figures 14A and 14B. Only the diode, resistor R1, tuning diode, and capacitor C1 if used were subjected to temperature changes. Thus, any effect of power supply variation and variable resistor instability were neglected.

TABLE VI

	TUNING DIODE BIAS VOLTAGE				
ppm Accuracy of R1	1 V	2 V	5 V	25 V	
±10 ppm	1	1	–	–	PPM CAPACITANCE CHANGE
±25 ppm	3	2	1	–	
±50 ppm	6	4	2	1	
±100 ppm	12	7	4	2	
±200 ppm	24	14	8	4	

Keeping cost in mind, ±100 ppm or ±50 ppm 1% resistors are recommended for R1.

Actual circuits constructed will not be as accurate as these test results because the power supply and variable resistor will contribute some instability. Some of the variations that will occur are shown in Table VII.

The effects of tuning diode variation and correction diode variation are accounted for in Table V. The effects

TABLE V

Tuning Diode	Correction Diode	Method One R1	Typ ppm Method One -50 to 125°C	Max ppm Method One -50 to 125°C	Method Two R1	Method Two C_X Note 1	Typ ppm Method Two -50 to 125°C	Max ppm Method Two -50 to 125°C
MV2101 Series	MSD6100	50 k to 70 k	-30 to +40	±50	8.2 k	23	±15	±25
	1N4001	20 k to 30 k	-40 to +40	±60	–	–	–	–
	*2N5221	250 k to 400 k	-30 to +40	±55	33 k	23	±15	±25
	*MPS5172	250 k to 400 k	-35 to +40	±60	47 k	23	±15	±25
	*MPS3904	--	–	–	180 k	23	±20	±30
1N5139 Series	MSD6100	400 k to 600 k	-30 to +50	±60	120 k	16	±25	±35
	1N4001	400 k to 600 k	-30 to +45	±50	82 k	15	±20	±30
	MPS5172	–	–	–	600 - 800 k	15	±25	±35
MV2305 Series Note 2	MSD6100	40 k to 60 k	-40 to +50	±60	–	–	–	–
	1N4001	15 k to 25 k	±45	±65	–	–	–	–
	*2N5221 *MPS5172	250 k tp 350 k	±45	±70	18 k	35	±15	±25
	*MPS3904	–	–	–	100 k	34	±15	±25
MV3500 Series	MSD6100	30 k to 40 k	±40	±60	–	–	–	–
	*2N5221 *MPS5172	120 k to 180 k	-35 to +45	±55	–	–	–	–
	*MPS3904	–	–	–	56 k	22	±15	±25
1N5441 & 1N5461 Series	MSD6100	400 k to 500 k	±45	±60	68 k	22	±20	±30
	1N4001	400 k to 500 k	±50	±60	22 k	22	±20	±30
	*2N5221 *MPS5172	–	–	–	390 k	22	±20	±35

*Base-Emitter junction used as a diode.

TABLE VII Other Error Contributing Factors In Temperature Compensation

	Typical ppm/°C
Power Supply Variation	±8
R1 Changes	±5
Changes in Epicap Current through Potentiometer	±5
Potentiometer Nonlinearities	±2
Tuning Diode Variation	±10
Correction Diode Variation	±15

of power supply and potentiometers must be accounted for separately and decrease the total accuracy. If a ±25 ppm/°C correction scheme is used, but the power supply has ±25 ppm/°C stability, an overall stability of ±35 ppm is obtained. This apparent error results from the fact that the error factors cannot be added directly, but must be summed as vectors in accordance to the rules of error theory. It is important to consider the whole circuit when designing for temperature compensation.

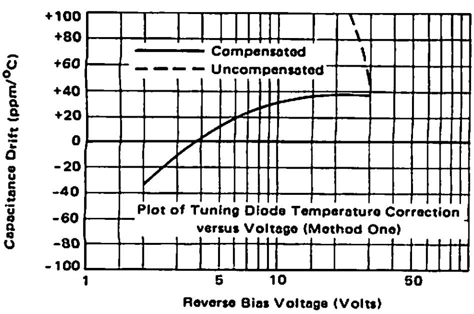


FIGURE 14A – MV2111, MSD6100 Compensation Diode
R1 = 68 k

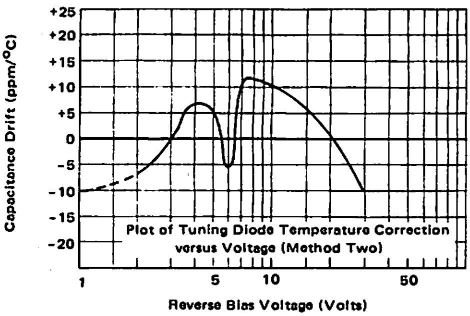


FIGURE 14B – MV2111, MSD6100 Compensating Diode
R1 = 8.2 k
C1 = 3.3 pF (N330)
0.00109 pF/°C

HYPER-ABRUPT TEMPERATURE DRIFT

The hyper-abrupt tuning diode is more sensitive than other types to temperature variations resulting in a greater need for temperature compensation. Also their drift with temperature is not as uniform as abrupt junction tuning diodes. Their drift factors expressed in ppm/°C run as high as 800 to 1200 for the units with a γ of 2. Units having a γ of 1 typically show 300 to 400 ppm/°C capacitance changes. These higher drift rates are caused by the

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hyper-abrupt tuning diode's greater sensitivity to changes in voltage, and the fact that the majority of capacitance change is caused by the change in contact potential, ϕ. This greater sensitivity to voltage changes means that power supply and other instabilities will also have a larger effect than with regular abrupt junction tuning diodes.

As a first order approximation, a MPS3904 transistor's emitter-base junction with a 50 k resistor used for R1 will improve the temperature drift in capacitance to better than 200 ppm/°C. Improvement from this point can only be obtained by a trial and error method described below.

Figure 15 shows the variation in compensation as R1 is varied for the MV3142, a hyper-abrupt tuning diode. As R1 is increased in value, the ppm/°C value is made more negative. The effect of the change is greatest at lower voltages.

To completely compensate the drift factor of the MV3142 shown in Figure 15 would be very difficult due to the variation of the curve shape. However, improved compensation may be achieved by limiting the diode to an operating voltage range of 2 to 15 volts. Starting with an R1 value of 50 k, the tuning diode and compensation circuit should be varied in temperature, while measuring the capacitance change. If the drift factor is more positive than desired, R1 may be increased in value. Referring to Figure 15, a temperature drift factor of +40 ppm/°C at 2 V may be larger than can be tolerated. Substituting a 200 k resistor will reduce the value to 25 ppm/°C at 2 V. In order to accurately compensate at any voltage, it is only necessary to vary R1 while measuring the capacitance drift. If the required value for R1 becomes larger than 750 k, the compensating junction type should be switched to a MSD6100, and the bias resistor started at 50 k again.

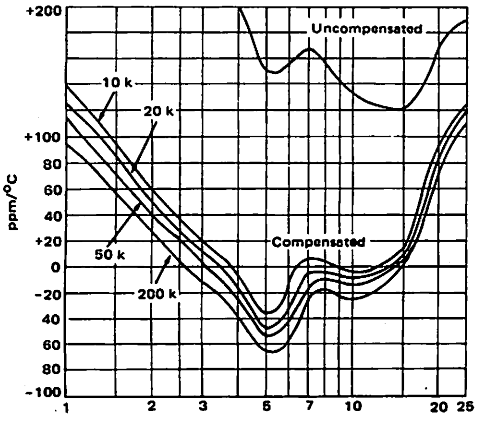

FIGURE 15 – MV3142 Tuning Diode Compensation For Differing Values of R1

SUMMARY

Voltage variable capacitors are rapidly replacing air variable capacitors in many applications. These devices offer many advantages over previous variable capacitors, such as the ability to employ remote tuning. By carefully considering the proper design conditions, such as temperature drift, and designing accordingly, Epicaps can replace air capacitors in virtually all but high power applications. The designer must be aware of the tuning range and Q limitation in order to use these devices effectively. Temperature drift should cease to be a problem when proper compensation schemes are used.

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7

MOUNTING STRIPLINE-OPPOSED-EMITTER (SOE) TRANSISTORS

Prepared by Lou Danley

INTRODUCTION

The Stripline Opposed Emitter (SOE) package presently used by Motorola for a number of rf power transistors represents a major advancement in high frequency and thermal performance. This Application Note discusses the SOE package, it advantages and limitations as well as a number of considerations to avoid improper usage.

An understanding of a few basic principles in regard to mounting and heat-sinking of this package can help avoid cases of poor performance or device damage.

Two general package types – the stud-mounted and flange-mounted SOE packages will be discussed. Each of the general types is available in a variety of sizes. Typical package outlines of the two SOE packages are shown in Figure 1.

ADVANTAGES OF THE SOE PACKAGE

The primary electrical advantages of the SOE packages are the low inductance strip line leads which interface very well with the microstrip lines often used in UHF-VHF equipment and the good collector to base isolation provided by the two emitter leads. The two emitter concept promotes symmetry in board layout when combining devices to obtain higher output power. Both emitter leads should always be used for best performance.

DESCRIPTION OF THE SOE PACKAGE

Figure 2 displays the component parts on a stud-mounted SOE package. This package will be used as an example since both the stud and flange-mounted packages are very similar in construction. The body of the package is a Berylium Oxide (BeO) disc. Berylium Oxide was chosen due to its high thermal conductivity. Attached to the bottom of the disc is a copper stud which is for heat transfer and mechanical mounting. The lead frame is attached to a metalized pattern on to the top surface of the BeO disc. The actual shape of the leads differs between the various package types. Finally an Alumina ceramic cap is attached to the top of the disc over the leads providing a protective cover for the transistor die.

An understanding of the basic structure of the SOE package is essential to proper usage of these devices in respect to heat-sinking and mechanical mounting. Since these two areas present the greatest problem to users, they will be discussed in detail.

HEAT-SINKING THE SOE PACKAGE

In order to properly understand the thermal considerations involved in mounting SOE type packages, it is necessary to lay some groundwork in the area of heat flow. Table I gives equivalent Thermal and Electrical parameters which may be used to relate Thermal properties to more familiar electrical units.

Semiconductor power devices are usually guaranteed to have a certain thermal performance as stated by the thermal resistance of the device from the junction to the case, or mounting surface – θ_{JC}. How to get the heat out of the

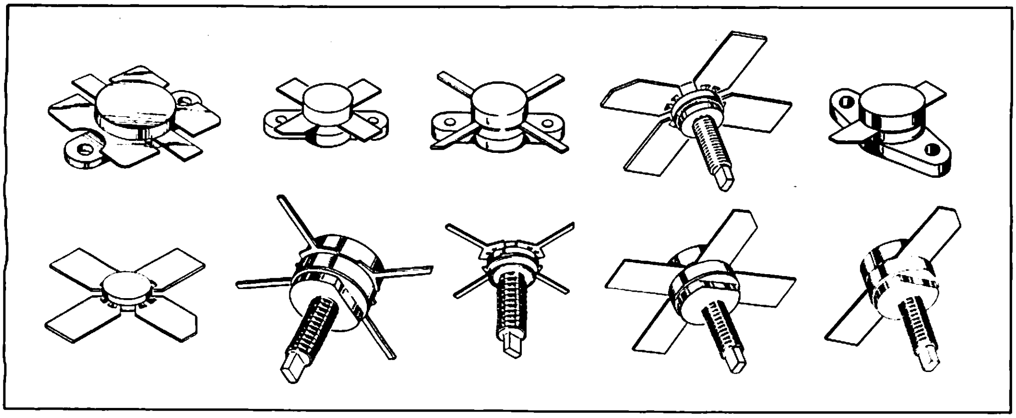

FIGURE 1 – SOE Packages

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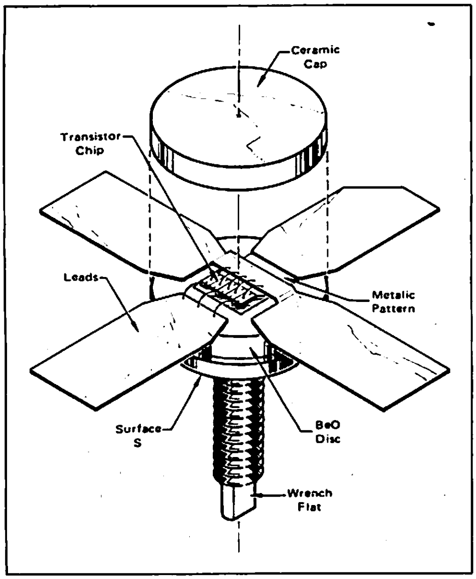

FIGURE 2 – Component Parts of SOE Package

case has generally been left to the user. In any dynamic heat flow problem, the heat must go somewhere, otherwise there will be a continuous rise in the temperature of the system. In text books, there always seems to be an "infinite heat sink" available which can absorb any amount of heat with no temperature rise whatsoever. In the practical sense, however, such a heat sink does not really exist. Practical heat sinks must be characterized by a certain temperature rise for a given ambient condition, with a known amount of heat input (power to be dissipated) after equilibrium conditions have been achieved. Characterization of heat-sink systems is best achieved by examining the complete system under controlled conditions.

TABLE I – Thermal Parameters and Their Electrical Analogs

	Thermal		Electrical Analog	
Symbol	Parameter	Units*	Symbol	Parameter
ΔT	Temperature difference	$^{\circ}C$	V	Voltage
H	Heat flow	watts	I	Current
θ	Thermal resistance	$^{\circ}C/watt$	R	Resistance
γ	Heat capacity	$\frac{watt\text{-}sec}{^{\circ}C}$	C	Capacity
K	Thermal conductivity	$\frac{cal}{sec\text{-}cm\text{-}^{\circ}C}$	σ	Conductivity
Q	Quantity of heat	cal	q	Charge
t	Time	sec	t	Time
$\theta\gamma$	Thermal time constant	sec	RC	Time constant

*Note the one major difference in thermal and electrical units; Q is in units of energy, whereas q is simply a charge. Hence H is in units of power and may be equated to an electrical power dissipation.

For example, the normal environment for a land-mobile VHF transmitter might be the trunk of a taxi cab in the hot Arizona summer. In such an environment, temperatures might reach as high as 80°C (176°F). The heat-sink system for such a radio should therefore be tested at a minimum ambient temperature of 80°C. The method that should be applied in this test would utilize a fine wire thermocouple rigidly secured to the stud of the rf power transistor for which the test is being conducted. The system, which in this case would include all parts of the radio which would contribute heat, should then be operated under maximum heat generating conditions, in the high temperature environment specified. Careful measurement of the temperature of the device under test would then give the difference in temperature between the case of the transistor and the controlled ambient.

If the case and ambient temperatures are known, as well as the power levels in the transistor, the thermal resistance from the transistor case to the ambient can be calculated. The first step is to obtain the power being dissipated by the device.

$$P_d = P_1 + P_2 - P_3 \qquad (1)$$

where: P_d = power being dissipated by the transistor in watts;
P_1 = dc power into the transistor in watts;
P_2 = rf power into the transistor in watts;
P_3 = rf power out of the transistor in watts.

This value of P_d is used to obtain the θ_{CA} value from the equation:

$$\theta_{CA} = \frac{T_C - T_A}{P_d} \qquad (2)$$

where: θ_{CA} = thermal resistance device case to ambient;
T_C = device case temperature;
T_A = ambient temperature.

In order to determine the maximum temperature rise in the transistor element (junction temperature rise) under any given operating condition the following equation may be used.

$$T_j = (\theta_{JC} + \theta_{CA}) P_d + T_A \qquad (3)$$

where: T_j = junction temperature;
θ_{JC} = published thermal resistance – junction to case.

If power is dissipated in a power transistor, the case temperature will rise above the ambient temperature by an amount determined by θ_{JC} and θ_{CA}. Since the value to θ_{JC} is fixed by the transistor type being used, θ_{CA} is the only factor with which the user can control the junction temperature for a given power dissipation.

Since heat generated by the transistor must be radiated to the ambient by the heat sink, a low θ_{CA} requires an effective heat sink. In general, an efficient heat sink requires that material with high thermal conductivity and high specific heat be used. A table of thermal properties for various materials is given in the Appendix. A well-designed heat sink requires that all thermal paths be as short as possible and of maximum cross-sectional area. Examples of thermal resistance calculations for a bar and a flat disc of thermal conducting material are given in the Appendix.

The equations given in the Appendix however, assume no thermal resistance between the case and the heat sink.

The primary heat conducting surface on stud-mounted SOE packages is the flat metal surface between the actual stud and BeO case body labeled surface S in Figure 2. This surface, which has a D-flat on some case types, must make good contact with the heat sink to allow good thermal conduction. To insure good contact: a) the heat sink mounting surface must be flat, b) the mounting hole must be burr free, the proper size and perpendicular to the mounting surface, c) the proper sized nut should be used and d) the nut should be properly torqued. Recommended mounting hardware is given in the section on device mounting.

With flange-mounted devices the primary parameters affecting thermal transfer are the flatness of the heat sink surface and the flatness of the device flange. The flange-mounted package requires that good contact be made between the flange and the heat-sink surface, particularly directly beneath the BeO disc.

With either of these packages it has been found that a considerable improvement in thermal transfer can be achieved through the proper use of one of the silicone based "heat-sink compounds" which are marketed by several vendors. Dow Corning and Wakefield Engineering are both suppliers of good thermal compounds. It should be pointed out however, that these compounds have a thermal conductivity approximately equal to that of Mica (0.0018 Cal/Sec-cm-°C) which is poor compared to that of Aluminum (0.49 Cal/Sec-cm-°C). However by comaprison, the thermal conductivity of still air is approximately 0.000006 Cal/Sec-cm-°C). The quantity of silicone grease used must be kept to the absolute minimum required to fill in any air gaps which might occur between the transistor mounting surface and the heat-sink surface. In the case of the stud-mounted package this is the gap after the transistor has been secured with the proper stud torque. Contributions of as high as 0.5°C/watt to the overall thermal resistance can occur if the heat-sink compound is used in a sloppy and excessive manner.

MOUNTING SOE DEVICES

The second area demanding consideration by a user of SOE transistors is mechanical mounting. Failure to observe proper mounting procedures can result in device destruction. This section will discuss both the stud-mounted, and the flange-mounted SOE devices.

Seven general considerations for properly mounting SOE transistors are listed briefly below. More detailed discussion will follow.

A. The device should never be mounted in such a manner as to place ceramic to metal joints in tension.

B. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.

C. When the device is mounted in a printed circuit board with the copper (stud or flange) and BeO portion of the header passing through a hole in the circuit board, adequate clearance must be provided for the BeO to prevent shear forces from being applied to the leads.

D. Some clearance must be allowed between the leads and the circuit board when the device is properly secured to the heat sink.

E. The device should be properly secured into the heat sinks before the device leads are attached (soldered) into the circuit.

F. The leads must not be used to prevent device rotation on stud type devices during stud torque application. A wrench flat is provided for this purpose.

G. With stud packages, maximum stud torque, as stated later in this note, and on the respective device data sheets must not be exceeded. If repeated assembly/disassembly operation is expected, a lesser torque should be used.

Most of the considerations listed above are designed to prevent tension at the metal-ceramic interfaces on the SOE package. Improper mechanical design can lead to application of stresses to these joints resulting in device destruction. Three joints are considered: The cap to the BeO disc, the leads to the disc, and the stud or flange to the disc.

The joint between the ceramic cap and the BeO ceramic disc is composed of a material which loses strength above 175°C. While the strength of the material returns upon cooling, any force applied to the cap at high temperature may result in failure of the cap to ceramic joint.

The lead frame and stud or flange attachment will be grouped together since they are very similar. Although the SOE package used by Motorola makes use of high temperature (> 700°C) solder alloys for lead frame and flange or stud attachment, care should be taken to avoid the application of tensile forces to the joint in the mounting of the transistor into a system. Such forces could result if the device were mounted with improper mounting clearances.

MOUNTING THE STUD TYPE SOE TRANSISTOR

Figure 3 shows a cross-section of a printed circuit board and heat sink assembly for mounting a stud type SOE device. Let us define H as the distance from the top surface of the printed circuit board to the D-flat heat sink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the SOE

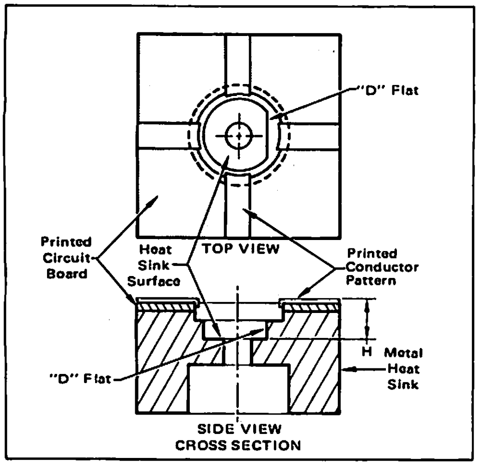

FIGURE 3 – Typical Stud-Mounting Method

package, there is no possibility of tensile forces in the copper stud – BeO ceramic joint. If, however, H is greater than the package dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurances are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heat sink surface will occur as the difference between H and the package dimension becomes larger, this may result in device failure as power is applied.

Proper stud torque is an important consideration when mounting stud type SOE devices.* The stud section of the SOE package is composed of a special copper alloy chosen because of its high thermal conductivity. However when this material is used in studded semiconductor device packages, it is necessary to place severe restrictions on the amount of tightening torque which can be applied to a nut used to secure the device to a heat sink.

*The Motorola Outline Dictionary calls for Class 2A threads. The National Bureau of Standards Handbook H28 entitled Screw Thread Standards, paragraph 4.2 on page 2.17, reads in part as follows:

> "However, for threads with additive finish, the maximum diameters of Class 2A threads may be exceeded by the amount of the allowance; i.e., the 2A maximum diameters apply to an unplated part or to a part before plating whereas the basic diameters (the 2A maximum diameter plus allowance) apply to a part after plating."

Also, footnote b, page 2.37 reads:

> "For Class 2A threads having an additive finish, the maximum is increased to the basic size, the value being the same as for Class 3A."

This means that for plated parts, the no-go gauge used is the 2A minimum and the go gauge used is the 2A maximum plus the allowance or, in other words, the 3A maximum.

The recommended torque values are listed below for the two thread sizes presently being employed on Motorola rf power transistor packages.

Recommended maximum torque for stud SOE transistors follows:

	8 - 32 Threads	10 - 32 Threads
One time maximum	6.5 lb.-in.	11.0 lb.-in.
Repeated assembly-assembly maximum	5.0 lb.-in.	8.5 lb.-in.

An evaluation of the effects of measured torque on the studs under consideration requires a known set of conditions. The system used to generate the data shown in Figure 4 consisted of a 1/8 inch aluminum plate with a deburred clearance hole for the stud under test, a steel washer to be positioned between the plate and appropriate steel nut. A calibrated torque wrench was used as the driving means. On each unit under test, the spacing separating four threads positioned between the nut and heat-sink surface was measured. After mounting the device on the aluminum plate and applying a known amount of torque the spacing was again measured and the results recorded.

The results of this test show that up to the maximum torque specified, the permanent elongation of the threads increases linearly with applied torque. At the torque specified this elongation does not exceed acceptable limits.

MOUNTING THE FLANGE TYPE SOE TRANSISTOR

The mounting and heat sinking of the flange type package is similar to that of the stud type package. The main considerations with the flange package are avoiding tensile stresses at the metal-ceramic joints and providing a flat heat conducting surface beneath the flange.

Figure 5 shows a typical mounting technique for flange type SOE rf power transistors. Again H is defined as the distance from the top of the printed circuit board to the heat-sink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur. Because of the ability

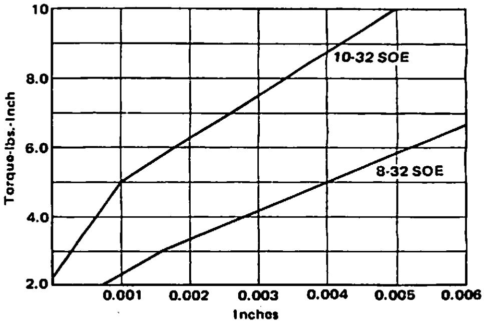

FIGURE 4 – Permanent Elongation Over a Four Tooth Length

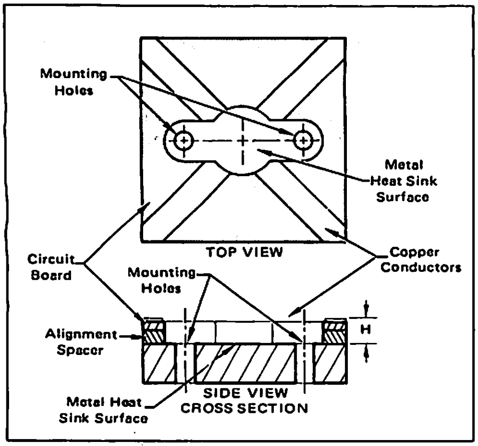

FIGURE 5 – Flange Type SOE Transistor Mounting Method

of the copper flange to bend under the types of loads encountered when the mounting screws are tightened, permanent deformation of the flange may result. Corrective action after the flange has been bent will not necessarily insure proper thermal contact with the heat sink.

The flange surface as supplied with Motorola SOE transistors is either flat or slightly convex. It is important that the mating heat-sink surface also be flat or slightly convex to provide the best contact when the device is properly secured.

The holes for the mounting screws should be deburred because any irregularity of the surface at these two points is equivalent to concavity of the heat-sink surface which will degrade thermal contact between the transistor and the heat sink.

Since the flange may be permanently deformed during mounting, the device should not be dismounted and remounted in another position.

CONCLUSION

The SOE package is an excellent rf power transistor package. However, improper heat sinking and mechanical mounting can result in device damage. A number of considerations have been presented to inform the potential user of the hazards of improper mounting. Proper usage of the SOE package requires no great difficulty if the designer is aware of the limitations and construction of the package.

A list of recommended mounting hardware and a suggested mounting procedure follows:

Table of Recommended Mounting Hardware Which Can be Supplied With Motorola Stud Type SOE Transistor

Stud Thread Size	Motorola Part Numbers		
	Nut	Flat Washer	Lock Washer
10-32	02BSB51568F044	04BSB51567F040	04BSB51566F028
8-32	02BSB51568F042	04BSB51567F038	04BSB51566F030
6-32	02BSB51568F040	04BSB51567F036	04BSB51566F032

STEPS IN A PROPER MOUNTING PROCEDURE

1. Compare the distance between the heat sink surface and the top of the printed circuit board with the minimum dimension of the transistor from the mounting surface to the bottom of the leads. The transistor dimension, as stated on the device data sheet, should be the greater distance to avoid the chance of stresses on the various joints of the SOE package.

2. Bore the proper sized mounting hole or holes for the stud or mounting screws. These holes should be perpendicular to the heat sink surface and they should be properly deburred.

3. Place a limited amount of thermal compound on the heat sink surface where it will contact the flange or mounting surface above the stud. Insert the transistor and mount with the proper hardware as suggested in the preceeding table.

   In the case of the stud device, torque the nut to the proper value.

4. Solder the leads to the printed circuit board using the minimum amount of heat and the least possible time of application. The leads should be soldered as close to the package as possible to minimize series lead inductance.

5. With the unit exposed to the highest expected ambient temperature, and power applied, measure the temperature at the stud or flange surface with a thermocouple to insure that this temperature is not excessive. Before production quantities are commited, it is suggested that a sample assembly to be tested under worst case heat generating conditions.

APPENDIX

In order to aid in heat-sink design, a table of thermal properties of common materials and a pair of thermal conductivity examples are presented.

Table AI gives three important thermal properties of common heat-sink materials. In order to evaluate materials for use in heat sinks these three thermal properties should be considered.

Thermal conductivity is a measure of the ability of a material of known cross-sectional area to transfer heat a given distance in a given time with a given temperature difference. Generally metals are good thermal conductors.

Specific heat is a measure of the amount of heat a given mass of material can accept for a given rise in temperature. The scale is normalized to the heat capacity of water (H_2O = 1.0).

Mass density is simply the mass per unit volume of a material. This parameter is important in heat sink design to the extent that large heat sinks of dense material carry with them a serious weight penalty.

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TABLE AI – Typical Thermal Properties of Materials

Material	Thermal Conductivity K (cal/sec-cm-°C)	Specific Heat S (cal/gm-°C)	Mass Density ρ (gm/cm°C)
Silver	0.97	0.056	10.5
Copper	0.92	0.093	8.9
Gold	0.69	0.030	19.3
Beryllia-Ceramic	0.55	0.31	2.8
Aluminum	0.49	0.22	2.7
Brass	0.26	0.094	8.6
Silicon	0.20	0.18	2.4
Germanium	0.14	0.074	5.5
Steel	0.12	0.12	7.8
Solder	0.09	0.04	8.7
Kovar	0.046	0.11	8.2
Alumina-Ceramic	0.04	0.21	3.7
Plastic-Epoxy	0.0026	0.2	2.0
Glass	0.0026	0.20	2.2
Mica	0.0018	0.20	3.2
Teflon	0.00056	0.25	2.2
Air	0.000057	0.24	0.0013
Heat Sink Compound	0.0018	–	–

Example 1.

In order to present some of the important characteristics to be used in heat sink design, the examination of two admittedly simplified models is desirable. The analogy between electrical resistivity and thermal resistivity will be employed.

The first of these is shown in Figure A1.

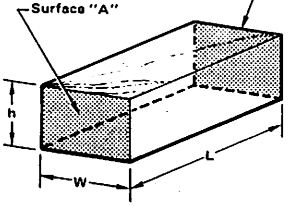

FIGURE A1 – A Bar of Thermal Conducting Material

The electrical resistance from Surface A to Surface B of this bar of conductive material is:

$$R = \frac{\rho L}{hW} \qquad \text{(A1)}$$

Using the electrical to thermal analogs:

$$\theta = \frac{L}{KhW} = \frac{L}{KA} \qquad \text{(A2)}$$

This simplified model might represent a pedestal mount or a device mount in the center of a bar connecting at either end to a housing, and demonstrates the need for thermally conducting paths of high cross-sectional area and the shortest possible length.

Example 2.

The second simple model represents the mounting of the power device on a plate of conducting material which provides the conducting path to the ambient conditions.

Consider the simple disc geometry shown in Figure A2 as a donut-shaped sheet resistor. Equation A3 represents the electrical resistance between r1 and r2,

$$R = \frac{\rho}{2\pi x} \ln\left(n \frac{r_2}{r_1}\right) \qquad \text{(A3)}$$

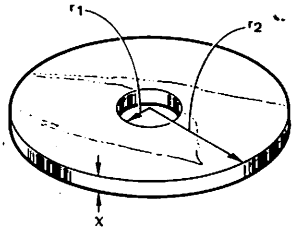

FIGURE A2 – Disc-Shaped Thermal Conductor

using the first term of the appropriate power series expansion

$$R \approx \frac{\rho}{\pi x}\left(\frac{r_2 - r_1}{r_2 + r_1}\right). \qquad \text{(A4)}$$

Where: ρ = Resistivity;

$\rho = \frac{1}{\sigma}$;

σ = Conductivity.

Replacing the electrical terms with their thermal analogs we find:

$$\theta = \frac{1}{K\pi x}\left(\frac{r_2 - r_1}{r_2 + r_1}\right)$$

Note the inverse linear dependence of thermal resistance on the thickness of the conducting sheet.

This model demonstrates a major factor in designing heat sink structures for stud type power transistors. All other factors being equal, the thickness of the thermally conducting plate is of prime importance in the solution of heat flow problems.

7

BROADBAND LINEAR POWER AMPLIFIERS USING PUSH-PULL TRANSISTORS

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INTRODUCTION

Linear power amplifier operation, as used in SSB transmitters, places stringent distortion requirements on the high-power stages. To meet these distortion requirements and to attain higher power levels than can be generally achieved with a single transistor, a push-pull output configuration is often employed. Although parallel operation can often meet the power output demands, the push-pull mode offers improved even-harmonic suppression making it the better choice. The exact amount of even-harmonic suppression available with push-pull stages is highly dependent on several factors, the most significant one being the matching between the two output devices. Nevertheless, even in the worst case the suppression provided in push-pull designs is superior to that of single-ended circuits. Device matching however is not limited to push-pull circuits since it is also required to a lesser degree in parallel transistor designs.

Two linear power amplifier designs are to be discussed in this Application Note. The 80 Watt design is intended for mobile communications systems operating from a 12.5 V power sources. The other supplies 160 W when operated from a 28 V line and it is intended for fix location systems. Both designs cover the 3–30 MHz band and utilize a driver stage to provide a total power gain of about 30 dB. Each amplifier requires some amount of heat-sinking for proper operation. The 28 V amplifier requires a heat-sink with a thermal characteristic of 0.85°C/W while the 12.5 V version uses a heat-sink with a 1.40°C/W thermal resistance. With these heat-sinks, cooling fans are not required for normal conditions, since with speech operation the average power is some 15 dB below peak levels. However, if two-tone bench testing is to exceed more than a duration of a few minutes, a cooling fan should be provided.

To assure ruggedness, engineering models of both amplifiers were subjected to open and short circuit output mismatches for several minutes at full power levels without any apparent damage to any of the transistors. This is very important in most equipment designs to avoid possible downtime for transistor replacements.

A 28 V, 160 W AMPLIFIER

An amplifier which can supply 160 watts (PEP) into a 50 Ω load with IMD performance of -30 dB or better is shown in the schematic diagram of Figure 1 and photos of Figures 2 and 3. Two 2N5942 transistors are employed in the design. These transistors are specified at 80 watts (PEP) output with intermodulation distortion products (IMD) rated at -30 dB. For broadband linear operation, a quiescent collector current of 60-80 mA for each transistor should be provided. Higher quiescent current levels will reduce fifth order IMD products, but will have little effect on third order products except at lower power levels. Generally, third order distortion is much more significant than the fifth order products.

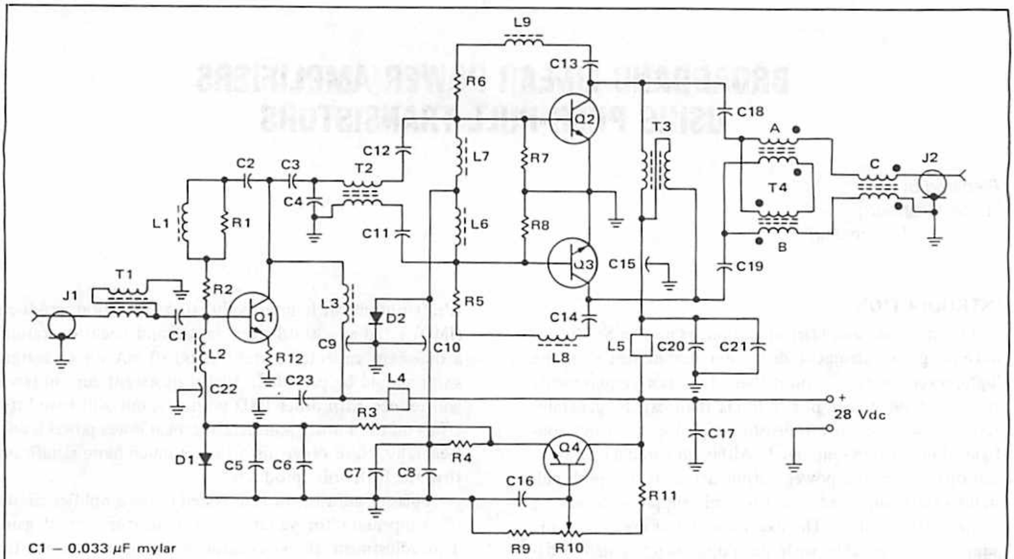
A biasing adjustment is provided in the amplifier circuit to compensate for variations in transistor current gain. This adjustment allows control of the idling current for both the output and driver devices. This control is also useful if the amplifier is operated from a supply other than 28 volts.

Even with the biasing control, it is strongly suggested that the output transistors be beta matched. As with any push-pull design, both dc current gain and power gain at a midband frequency should be matched within about 15-20%. This matching may require more stringent limits if broad-banding is necessary since broad-band operation requires more effective cancellation of even harmonics. In the engineering model used, the transistors were not perfectly matched. Four "similar" pairs were selected from a total of ten randomly chosen 2N5942 transistors. Table I shows the measured harmonic suppression which is degraded by the mismatch in the output transistor parameters. This data was taken with a single frequency test and 80 watts average output.

TABLE I – HARMONIC SUPPRESSION OF 28 V AMPLIFIER AT FULL OUTPUT POWER

Harmonic		2nd	3rd	4th	5th
Frequency	3 MHz	-16 dB	-30 dB	-22 dB	-37 dB
	6 MHz	-15 dB	-20 dB	-21 dB	-37 dB
	12 MHz	-16 dB	-24 dB	-22 dB	-34 dB
	30 MHz	-35 dB	-20 dB	-51 dB	-44 dB

A 2N6370 transistor is employed as a driver. This device is specified at -30 dB IMD when delivering 10 watts (PEP). However, at about 4.5 W (PEP) output, which is the maximum necessary to drive two 2N5942 transistors, the IMD is typically better than -40 dB with Class B biasing. A quiescent collector current level of at least 10-15 mA provides best IMD performance with the 2N6370. Higher current levels will not improve linearity, but will degrade driver efficiency.



C1 – 0.033 μF mylar
C2, C3 – 0.01 μF mylar
C4 – 620 pF dipped mica
C5, C7, C16 – 0.1 μF ceramic
C6 – 100 μF/15 V electrolytic
C8 – 500 μF/6 V electrolytic
C9, C10, C15, C22 – 1000 pF feed through
C11, C12 – 0.01 μF
C13, C14 – 0.015 μF mylar
C17 – 10 μF/35 V electrolytic
C18, C19, C21 – Two 0.068 μF mylars in parallel
C20 – 0.1 μF disc ceramic
C23 – 0.1 μF disc ceramic
R1 – 220 Ω, 1/4 W carbon
R2 – 47 Ω, 1/2 W carbon
R3 – 820 Ω, 1 W wire W
R4 – 35 Ω, 5 W wire W
R5, R6 – Two 150 Ω, 1/2 W carbon in parallel
R7, R8 – 10 Ω, 1/2 W carbon
R9, R11 – 1 k, 1/2 W carbon
R10 – 1 k, 1/2 W potentiometer
R12 – 0.85 Ω (6 5.1 Ω or 4 3.3 Ω 1/4 W resistors in parallel, divided equally between both emitter leads)

T1 – 4:1 Transformer, 6 turns, 2 twisted pairs of #26 AWG enameled wire (8 twists per inch)
T2 – 1:1 Balun, 6 turns, 2 twisted pairs of #24 AWG enameled wire (6 twists per inch)
T3 – Collector choke, 4 turns, 2 twisted pairs of #22 AWG enameled wire (6 twists per inch)
T4 – 1:4 Transformer Balun, A&B – 5 turns, 2 twisted pairs of #24, C – 8 turns, 1 twisted pair of #24 AWG enameled wire (All windings 6 twists per inch). (T4 – Indiana General F624-19Q1, – All others are Indiana General F627-8Q1 ferrite toroids or equivalent.)

PARTS LIST

L1 – .33 μH, molded choke
L2, L6, L7 – 10 μH, molded choke
L3 – 1.8 μH (Ohmite 2-144)
L4, L5 – 3 ferrite beads each
L8, L9 – .22 μH, molded choke

Q1 – 2N6370
Q2, Q3 – 2N5942
Q4 – 2N5190
D1 – 1N4001
D2 – 1N4997
J1, J2 – BNC connectors

FIGURE 1 – 160 Watt (PEP) Broadband Linear Amplifier

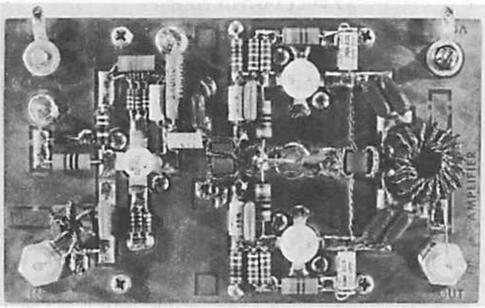


FIGURE 2 – Photo of 28 V Linear Amplifier

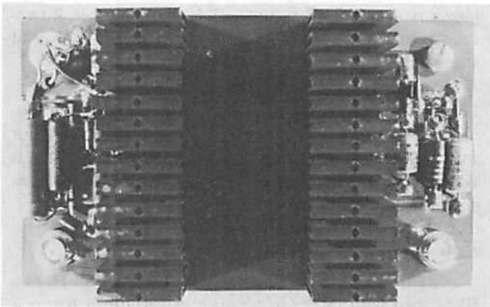


FIGURE 3 – Photo of Back Side of 28 V Linear Amplifier

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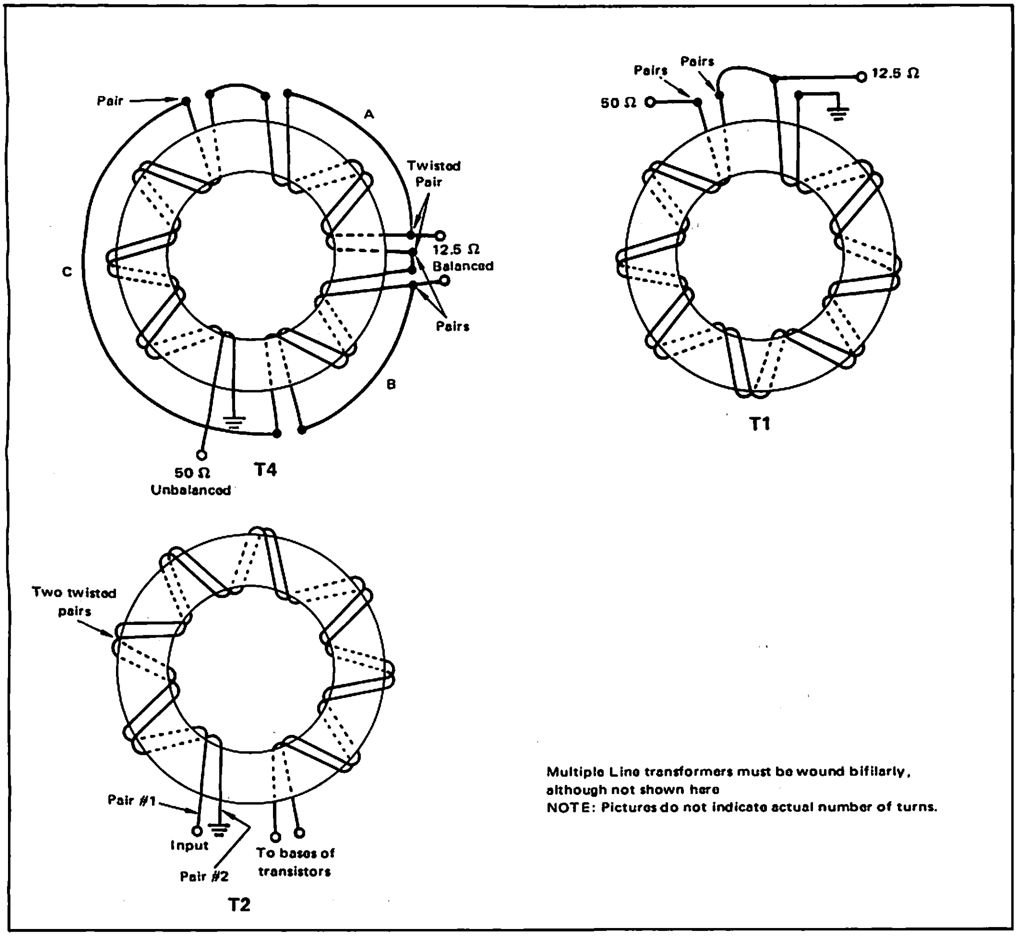

FIGURE 4 — Transformer Details for 28 V Linear Amplifier

Feedback

To compensate for variations in output with changes in operating frequency, negative voltage feedback is employed on both the final amplifier and driver stages. At the low end of the desired frequency band, approximately 4.5 dB of feedback is introduced in the final stage and 15 dB in the driver stage. With this feedback and the feedback networks shown in the schematic diagram, Figure 1, a total gain variation of 0.5 dB was measured on an engineering prototype amplifier over a 3-30 MHz range. The total gain differential in three identical amplifiers constructed for evaluation was less than 1.5 dB.

Transformers Employed

In order to achieve the desired broadband response, transmission line-type transformers were employed for coupling and signal-splitting. These transformers utilize twisted-pair windings and toroidal cores. Transformers T1, T2 and T3 have turn ratios of 4:1, 1:1 and 1:4 respectively. Additional information on these transformers can be found in the references. A short description of each of the transformers will follow.

Transformer T1 provides an impedance transformation to match the 50 Ω source to the low impedance level required at the base of Q1. This transformer consists of six turns of two twisted pairs wound on a toroidal core. The two pairs (four separate wires), are twisted together and the two wires from each original pair are soldered together at each end. Each pair thus connected is shown as a single wire in Figure 4. The pairs can easily be identified by choosing wires with two different colors of insulation.

Transformer T2 is a 1:1 Balun consisting of six turns of two-twisted pairs of wire (four wires total). As shown in Figure 4 each of the pairs is treated as a single wire.

<u>Transformer T3</u> consists of four turns of two twisted pairs. Again both wires of each pair are soldered together at each end.

<u>Transformer T4</u> is a 1:4 ratio unbalanced to balanced unit with three separate windings.

A lumped-constant equivalent conventional transformer diagram of transformer T4 is shown in Figure 5. The two windings in a single twisted pair are indicated by similar capital and lower case letters (i.e. windings A and a). The output line of the balun is in the same direction as windings A and B while the grounded line is in the opposite direction from the winding it is connected to. Windings A, a, B and b consist of 5 turns of two twisted pairs while C and c are formed from eight turns of a single pair. Connections are shown in Figure 4. The three windings are bifilar wound, although for simplicity the figures do not show this.

Referring to Figure 5 the equivalent connection diagram of T4, it can be seen that the sum of the voltages across c and C should be equal to the voltage across windings DE. From this, winding cC (a twisted pair) should have twice as many turns as twisted pairs aA and bB. Deviations of about 10-20% from the 2:1 ratio do not produce noticeable effects.

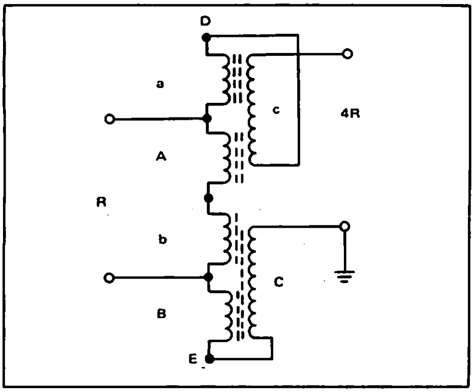

FIGURE 5 — Equivalent Lumped Element Form of T4.

The ferrite core used for T4 in the parts list of Figure 1 has a specified maximum flux density of about 100 gauss. The flux density may be computed from equation 1.

$$\text{Bmax} = \frac{V \times 10^8}{4.44\,fnA} \quad \text{gauss} \qquad (1)$$

where:

V = RMS voltage across the winding = 89
f = frequency in Hertz = 3×10^6
n = number of turns (windings Aa and Bb only. Windings Cc cancel each other) = 20
A = cross sectional area of Toroid in Cm^2 = 0.25
$4.44 = 2\pi \times 0.707$

therefore:

$$\text{Bmax} = \frac{89 \times 10^8}{4.44\,(3 \times 10^6)\,20\,(.25)} = 133 \text{ gauss}$$

Despite this slight overrating, this density is not excessive.

Amplifier Performance

The data shown in the following curves was obtained from measurement performed on an engineering model of the 28 V 160 Watt (PEP) amplifier.

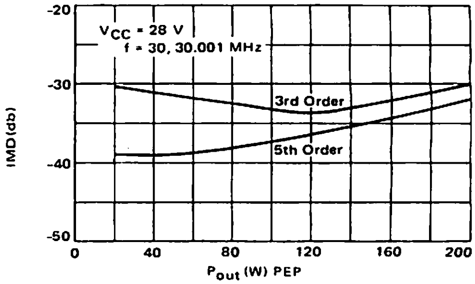

FIGURE 6 — IMD as a Function of Output Power for 28 V Amplifier

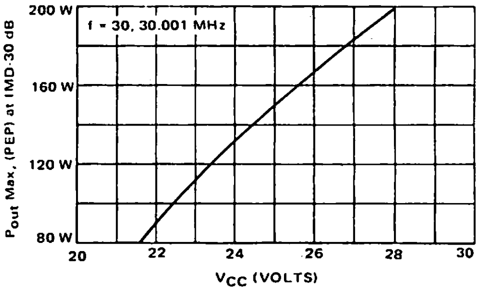

FIGURE 7 — Output Power for -30 dB IMD as a Function of V_{CC} for 28 V Amplifier

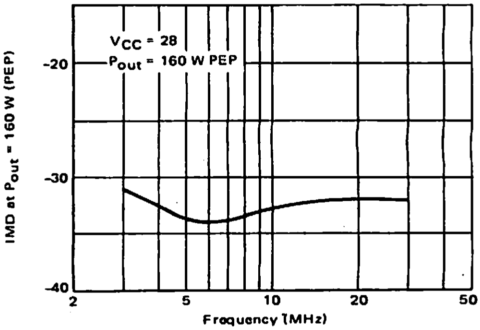

FIGURE 8 — IMD versus Frequency

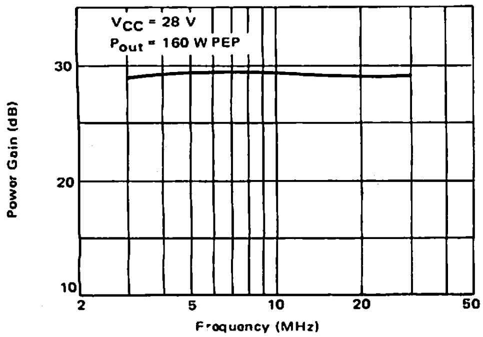

FIGURE 9 – Power Gain versus Frequency

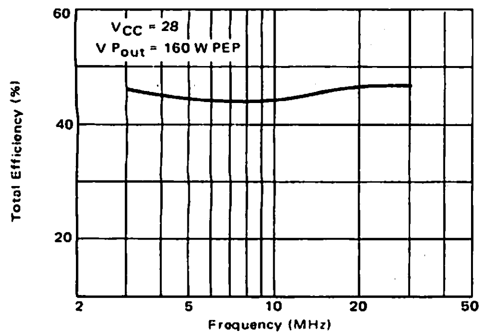

FIGURE 10 – Total Efficiency versus Frequency

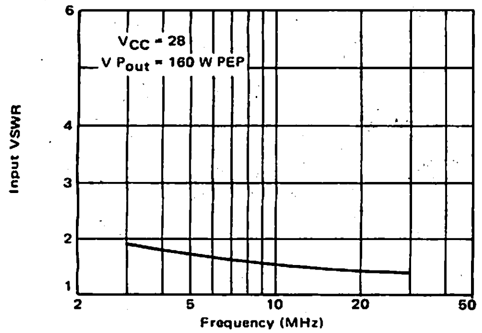

FIGURE 11 – VSWR versus Frequency

AN 80 WATT (PEP) 12.5 – 13.6 V AMPLIFIER

To complement the 28 Volt amplifier discussed previously, a second amplifier designed for 12 V operation was constructed and evaluated. This amplifier is shown in Figures 12, 13 and 14. It utilizes a 2N6367 and a pair of 2N6368 transistors. The 2N6367 transistor is employed as a driver and is specified for up to 9 watts (PEP) output. In the amplifier design the driver must supply only 5 watts (PEP) at 30 MHz with a resulting IMD performance of about –37 to –38 dB. At lower operating frequencies, drive requirements drop to the 2-3 Watt (PEP) range and IMD performance improves to better than 40 dB. The 2N6367 data sheet suggests a quiescent collector current of 35 mA, but it was found that increasing this to 40 mA yielded somewhat better linearity in broadband operation.

Two 2N6368 transistors are employed in the final stage of the transmitter design in a push-pull configuration. These devices are rated at 40 Watts (PEP) and –30 dB maximum IMD, although –35 dB performance is more typical for narrow band operation.

The 2N6368 data sheet suggests a quiescent collector current level of 50 mA, but a level of 60 mA for each transistor was used in this design for improved linearity.

Without frequency compensation, the completed amplifier can deliver 90 Watts (PEP) in the 25-30 MHz band with IMD performance down –30 dB. If only the power amplifier stage is frequency compensated, 95 Watts (PEP) can be obtained at 6-10 MHz.

Gain Compensation

Negative collector-to-base feedback is employed in both the driver and output stages for gain compensation. The feedback networks consist of: a) a dc blocking capacitor, b) a series resistor, to limit the amount of feedback at the low frequencies and c) a series inductor with a parallel resistor to determine the feedback slope.

In general, the use of negative feedback lowers the input impedance, and reduces the gain of the amplifier. However, it also improves the linearity since some of the output signal is fed back to the input and reamplified, tending to cancel the distortion originally generated. This is only true at the low frequencies where the phase errors are small. The phase error is caused by reactive elements in the feedback path. Since the basis for the compensation is to introduce more feedback at low frequencies, it will also equalize the input impedance to some degree. This, in turn, should result in a lower VSWR over the band.

The following two tables illustrate the affect of compensation on the final amplifier stage. This data was taken with a 9:1 ratio transformer connected between 50 Ω source and the input balun to the final stage.

From this table it can be seen that efficiency is reduced by applying compensation. For this reason only 3 dB of compensation was utilized on the final stage. The driver stage, where efficiency is not of primary concern, was actually over compensated. This stage has a gain of 16 dB at 30 MHz but only 13 dB at 3 MHz.

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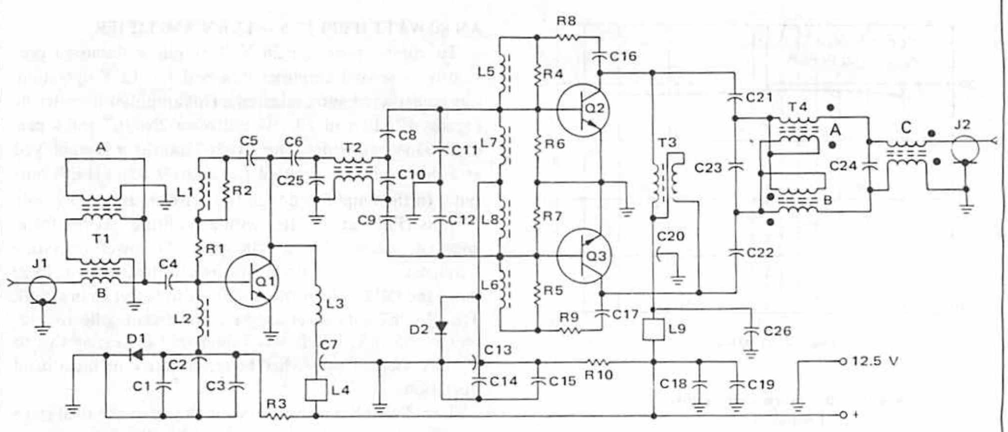

C1, C14, C18 – 0.1 μF ceramic.
C2, C7, C13, C20 – 0.001 μF feed through.
C3 – 100 μF/3V.
C4, C6 – 0.033 μF mylar
C5 – 0.0047 μF mylar.
C8, C9 – 0.015 and 0.033 μF mylars in parallel.
C10 – 470 pF mica.
C11, C12 – 560 pF mica.
C15 – 1000 μF/3 V
C16, C17 – 0.015 μF mylar
C19 – 10 pF 15 V
C21, C22 – two 0.068 μF mylars in parallel.
C23 – 330 pF mica
C24 – 39 pF mica
C25 – 680 pF mica
C26 – .01 μF ceramic

R1, R6, R7 – 10 Ω, 1/2 W carbon.
R2 – 51 Ω, 1/2 W carbon
R3 – 240 Ω, 1 wire W
R4, R5 – 18 Ω, 1 W carbon
R8, R9 – 27 Ω, 2 W carbon
R10 – 33 Ω, 6 W wire W

L1 – 0.22 μh molded choke
L2, L7, L8 – 10 μh molded choke
L5, L6 – 0.15 μh
L3 – 25 t, #26 wire, wound on a 100 Ω, 2 W resistor. (1.0 μh)
L4, L9 – 3 ferrite beads each.

T1 – 2 twisted pairs of #26 wire, 8 twists per inch. A = 4 turns, B = 8 turns. Core- -Stackpole 57-9322-11, Indiana General F627-8Q1 or equivalent
T2 – 2 twisted pairs of #24 wire, 8 twists per inch, 6 turns. (Core as above.)
T3 – 2 twisted pairs of #20 wire, 6 twists per inch, 4 turns. (Core as above.)
T4 – A and B = 2 twisted pairs of #24 wire, 8 twists per inch. 5 turns each. C = 1 twisted pair of #24 wire, 8 turns. Core - - Stackpole 57-9074-11, Indiana General F624-19Q1 or equivalent.

Q1 – 2N6367
Q2, Q3 – 2N6368

D1 – 1N4001
D2 – 1N4997

J1, J2 – BNC connectors

FIGURE 12 – Schematic Diagram of 12.5 V Amplifier

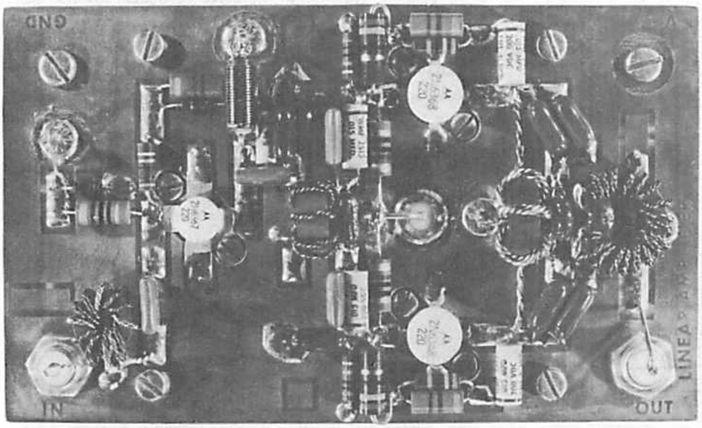

FIGURE 13 – Photo of Top View of 12.5 V Linear Amplifier

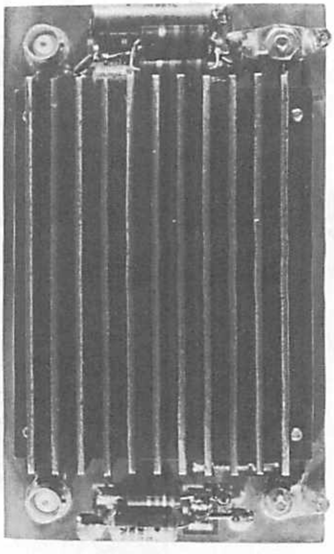

FIGURE 14 – Photo of Bottom of 12.5 V Linear Amplifier

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TABLE II – PERFORMANCE OF 12.5 V OUTPUT STAGE WITH AND WITHOUT GAIN COMPENSATION

With Feedback	GPE	EFF.	IMD	VSWR
3 MHz	16 dB	45.5%	-30 dB	1.6
12 MHz	15.3 dB	46.5%	-31 dB	2.1
30 MHz	12 dB	43.0%	-31 dB	1.05
Without Feedback	**GPE**	**EFF.**	**IMD**	**VSWR**
3 MHz	19.2 dB	48.0%	-26 dB	6.5
12 MHz	16.2 dB	46.8%	-30 dB	2.4
30 MHz	12.5 dB	43.0%	-33 dB	1.05

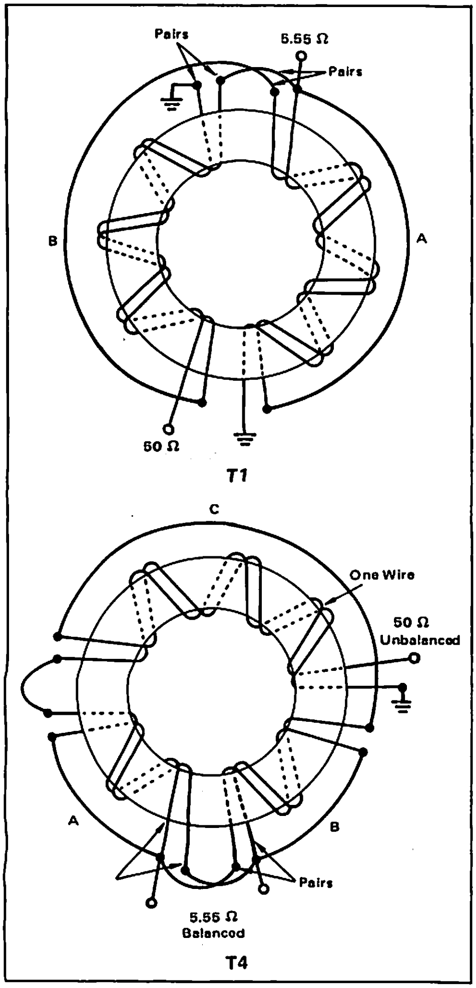

FIGURE 15 – Transformer Details for 12.5 V Linear Amplifier (See Figure 4)

Transformer T1 consists of two twisted pairs of wires which can be wound on either a single or two separate toroids. In the two core approach, both windings have an equal number of turns (four). If a single core is utilized, winding Aa uses four turns while winding Bb uses eight turns. These lines must be wound bifilar on the core. See Figure 15. The single core approach was used in the engineering model.

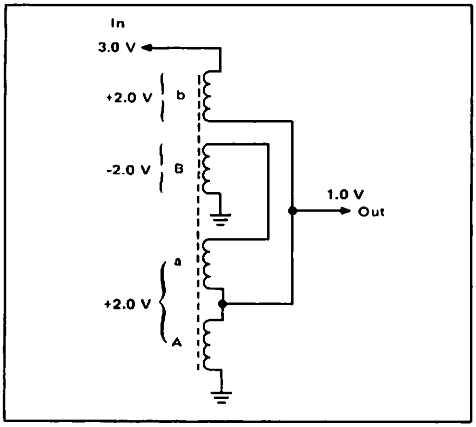

FIGURE 16 – Equivalent Lumped Element Form of T1

A lumped-constant equivalent conventional transformer diagram of transformer T1 is shown in Figure 16. Examination reveals that since winding B is directly in parallel with the series combination of aA, line Bb must have twice the number of turns as winding Aa. (The lower case and capital letters refer to the two wires in a given twisted-pair). As an example of the voltage relationships for the various windings in this transformer, an arbitrary 3 V input has been shown in the Figure. It can be seen that the voltages generated across windings b and B are out of phase and cancel each other. Therefore, the resulting output is 1 V (3 V-2 V).

This transformer may be considered as a combination of a 4:1 ratio transformer (aA) and a 1:1 balun (bB), where the balun performs the voltage subtraction.

Transformer T2 consists of two twisted pairs on a single core. Both wires of each pair are soldered together at each end. See Figure 15.

Transformer T3 also uses two twisted pairs wound on a single core. Each pair is treated as a single wire by soldering the two wires at each end.

Transformer T4 uses three separate bifilar windings on a single core. Windings aA and bB are balanced while Cc is unbalanced. Both aA and bB utilize five turns and Cc uses eight turns. This is the nearest whole number of turns possible to the desired ratio of 1:1.5 for winding Aa and

Bb to winding cC. Deviations of 10-20% of this ratio are allowable without noticeable effects.

Figure 17 shows the lumped equivalent transformer of

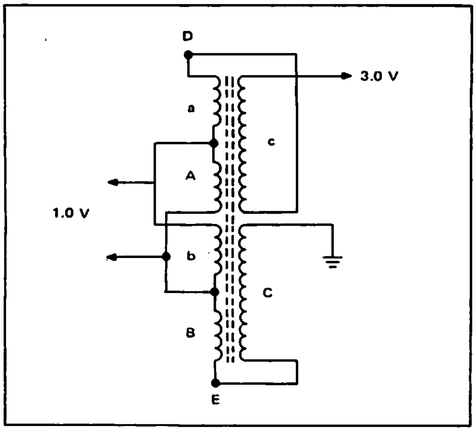

FIGURE 17 – Equivalent Lumped Element Form of T4

T4 and the ratio of voltages on the various windings if one volt is applied to the input. It can be seen that the voltage developed across c and C must equal the voltage between points D and E on the diagram. Since windings A and b are paralleled and connected to the input, they see one volt. Thus the voltage from point D to point E would be 3 V (1 V from A and b plus 1 V from winding a plus 1 V from winding B). Therefore, the output voltage is 3.0 volts and the voltage across winding c = -1.5 V and winding C = 1.5 V.

When using twisted-pair transmission line transformers, windings with four or more pairs should be avoided as it is difficult to twist such lines uniformly.

A second amplifier was evaluated with T4 replaced by a balun and an unsymmetrical 1:9 ratio transformer. Performance results were very similar to that obtained from the first version except that much more high frequency compensation was necessary. This was required because it is difficult to obtain the low characteristic impedance required for the balun. For this reason capacitors C10, C11, C12 and C25 were unusually large in value.

Performance

Typical performance of the 12.5 volt linear amplifiers is provided in the following curves. A calibration curve for use to correlate low frequency readings on a power meter is also given in Figure 24.

The harmonic suppression measurements taken at full output power levels with a single tone test are illustrated in Table II. This data suggests that a suitable low-pass filter between the amplifier output and the antenna will be required to meet harmonic suppression requirements. This filter's necessity is common to most broadband amplifier designs.

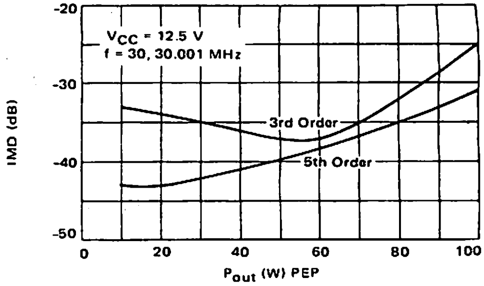

FIGURE 18 – IMD as a Function of Output Power For Push-Pull Linear Amplifier

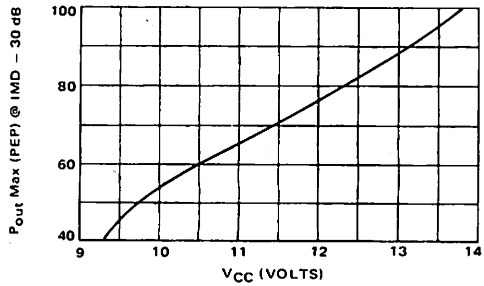

FIGURE 19 – Maximum Output Power @ -30 dB IMD versus V_{CC} for 12.5 V Power Amplifier

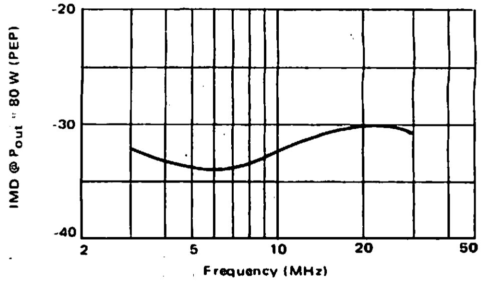

FIGURE 20 – IMD versus Frequency

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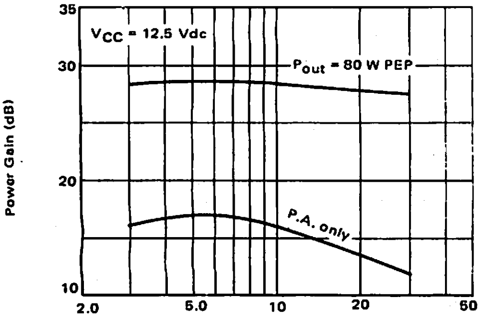

FIGURE 21 — Power Gain versus Frequency

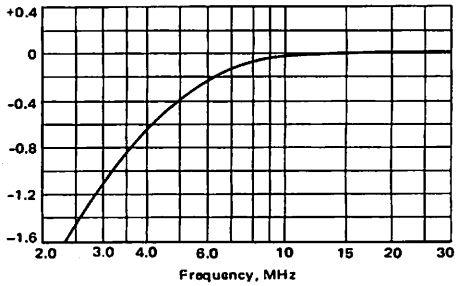

FIGURE 24 — Response of H.P. 431-432 Power Meters at Low Frequencies

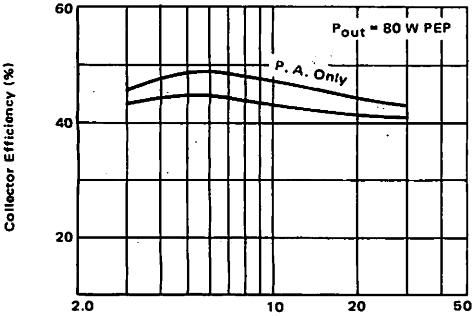

FIGURE 22 — Efficiency versus Frequency

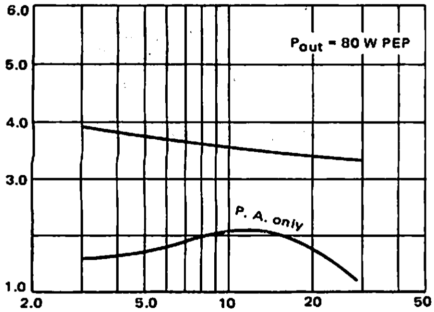

FIGURE 23 — VSWR versus Frequency

Transformer Data

As with the 28 V amplifier, transmission line type transformers are employed throughout the 12 V design. Although this type of transformer does not provide optimum impedance match, it is easy to duplicate for consistant performance results. A similar amplifier was constructed with a standard 2:1 ratio coupling transformer instead of the 1:1 ratio balun (T2). This amplifier featured a 40-60% improvement in VSWR at all frequencies while gain and IMD were basically unchanged from the performance of the model using transmission line type transformers.

Splitting the compensating capacitor for transformer T2 into three parts (C10, C11 and C12) will result in considerably lower IMD at higher frequencies. Capacitors C11 and C12 should be well matched and therefore should be either ±5% or better tolerance fixed value units, or variable capacitors such as Arco 466 and 469.

Two factors must be considered in the choice of toroidal core materials. The first is core losses. The second is the power handling capability which is limited by both magnetic saturation and heat generation.

For the input transformer (T1) core losses are of primary concern. For the material chosen in this design, a loss factor of 1-2 mW/cm^3 at 3 MHz is typical. This increases to 5-10 mW/cm^3 at 30 MHz. For the size of core used in T1, a maximum core loss of 1.5-7.0 mW can be expected. While this figure seems negligible, it is advantageous to use the smallest practical sized core for the input transformer consistent with the wire size and required number of turns.

Conversely the core of the output transformer (T4) should be as large as possible to be able to handle the required power levels and remain in the linear operating region of the materials' B-H curve. If the core is operated near the saturation region of the core material, distortion will be generated on the carrier and envelope. This saturation occurs first at low frequencies. However, core heating due to losses is most prevalent at higher frequencies, being a function of flux density and operating frequency. The maximum recommended flux density for a 1/2" O.D. toroid (such as Indiana General F627-8 or Stackpole 57-9322), is 45 to 70 gauss. From the B-H curves it can be seen that this is well into the linear region.

For the 12-volt amplifier, a flux density of roughly 180 gauss would be required for a 1/2" O.D. core. Use of a larger core reduces the density to about 130 gauss. As stated in the 28 V amplifier section, although this is in excess of the 100 gauss limit suggested for the particular core type, it was not found to be excessive. In fact, some of the 1/2" O.D. toroids were tested at three to four times the maximum recommended flux density, and then compared to a larger toroid of the same material. The distortion in each core was small enough not to be noticed in an oscilloscope. However, there was some amount of heat generated in the small toroid at the high frequencies. Excessive heating is the primary problem that one should be first concerned about.

As a rule of thumb, the required minimum transformer inductance can be determined to have at least 4-5 times the reactance of the high impedance port at the lowest operating frequency. This means that for T4, the reactance would be 250 ohms, which corresponds to roughly 14 μH at 3 MHz

Employing a different wire size or wire with a different thickness of dielectric or changing the number of twists per inch will alter the line impedance. However, this is one of the least critical points in the design of broadband linear amplifiers and will mainly affect the amount of high frequency compensation required. The variations in the transistor input and output impedance over a decade frequency range are several times larger than the changes in transformer impedance due to wire sizes or twist variations. Although compromises in matching are necessary to tune the wide frequency range, they are most serious in the output stage where a mismatch can significantly degrade total linearity.

The maximum theoretical linear output powers for the 28 V and 12.5 V amplifiers would be 120 W and 50 W respectively, when 4:1 and 9:1 output transformers are employed.

However, due to stray inductances in the circuit, and line impedances usually being higher than optimum, the actual impedance ratios of the transformers will be somewhat higher.

Thus, if the phase and even harmonic distortions are minimized it is possible to obtain higher power levels with fairly low IMD readings despite slight flat-topping of the envelope.

Construction Notes (12.5 V version)

The circuit board for both amplifier designs is made of two-sided copper-fiberglass laminate. A full sized pattern is given in Figures 25 and 26. The ground planes on each side are connected together at several points with the feed-through capacitors, the BNC connectors and the mounting screws. From experience with an earlier broadband amplifier, it was learned that a good ground plane is extremely important because of the high currents and low impedance levels involved. The power supply impedance must be as low as possible.

The ac impedance of the supply should not be higher than 0.01 ohm at the lowest envelope frequency.

All dc connections are made on the back side of the board which is separated from the heat sink by 3/32 inches. The base bias resistors (R3, R10), and all by-pass capacitors, except the feed-throughs, are on the back side of the board in each end of the heat sink. Diode D2 is press fitted into the heat sink for temperature compensation of the quiescent collector currents of the 2N6368 transistors. Ceramic capacitors have been avoided, except for certain by-pass applications, because they have spurious resonances and, their capacitance values are voltage and temperature sensitive. Parallel capacitors are employed to increase the current carrying capability and to decrease the possibility of self resonances. The peak RF current in

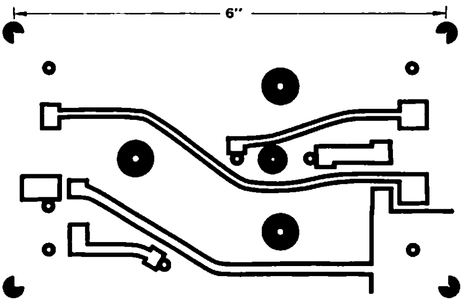

FIGURE 25 – Bottom PC Board Pattern

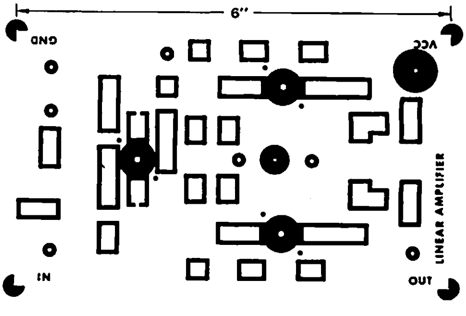

FIGURE 26 – Top Side of PC Board

TABLE III – HARMONIC SUPPRESSION versus FREQUENCY

Harmonic		2nd	3rd	4th	5th
Frequency	3 MHz	-19 dB	-15 dB	-26 dB	-29 dB
	6 MHz	-17 dB	-18 dB	-23 dB	-35 dB
	12 MHz	-30 dB	-20 dB	-28 dB	-34 dB
	30 MHz	-35 dB	-25 dB	-50 dB	-62 dB

the output transformer primary is $\sqrt{\frac{80\ W}{6.25\ \Omega}} = 3.54A$. Half of this is supplied by each 2N6368. Thus, the collector isolation capacitors will have to handle 1.77A peak and 1.26A average currents. Even the lead sizes in most capacitors are insufficient for these current levels. In general, the low impedances involved in a 12.5 volt amplifier of this power level make the layout, construction and component selection somewhat critical compared to a higher voltage unit.

CONSTRUCTION NOTES (28 V version)

The 28 volt unit is less critical than the 12.5 V amplifier as far as the physical circuit lay-out is concerned. However, the same precautions should be taken in grounding the by-pass capacitors and the transformer high frequency-compensation capacitors. It is recommended that variable capacitors, such as the ARCO 460 line be used initially for the compensating capacitors. Then after establishing satisfactory operation of the unit, they can be changed to fixed value capacitors.

IMPROVED PERFORMANCE

Since the original work on these amplifiers, device improvements have been made. Both IMD and load mismatch ruggedness characteristics can be enhanced by substituting the MRF463 or MRF464 for the 2N5942 in the 28-Volt amplifier. The MRF460 is recommended for upgrading the 12-Volt amplifier using the 2N6368. Neither of these new devices require circuit modifications for optimum operation.

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IMPEDANCE MATCHING NETWORKS APPLIED TO RF POWER TRANSISTORS

Prepared by:
B. Becciolini

1. INTRODUCTION

Some graphic and numerical methods of impedance matching will be reviewed here. The examples given will refer to high frequency power amplifiers.

Although matching networks normally take the form of filters and therefore are also useful to provide frequency discrimination, this aspect will only be considered as a corollary of the matching circuit.

Matching is necessary for the best possible energy transfer from stage to stage. In RF-power transistors the input impedance is of low value, decreasing as the power increases, or as the chip size becomes larger. This impedance must be matched either to a generator — of generally 50 ohms internal impedance — or to a preceding stage. Impedance transformation ratios of 10 or even 20 are not rare. Interstage matching has to be made between two complex impedances, which makes the design still more difficult, especially if matching must be accomplished over a wide frequency band.

2. DEVICE PARAMETERS

2.1 INPUT IMPEDANCE

The general shape of the input impedance of RF-power transistors is as shown in Figure 1. It is a large signal parameter, expressed here by the parallel combination of a resistance R_p and a reactance X_p (Ref. (1)).

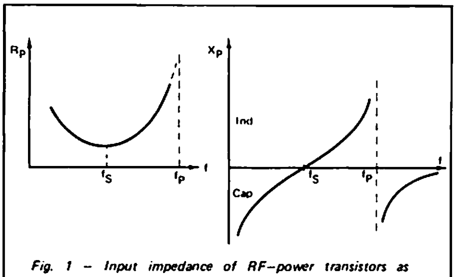


Fig. 1 – Input impedance of RF-power transistors as a function of frequency

The equivalent circuit shown in Figure 2 accounts for the behaviour illustrated in Figure 1.

With the presently used stripline or flange packaging, most of the power devices for VHF low band will have their R_P and X_P values below the series resonant point fs. The input impedance will be essentially capacitive.

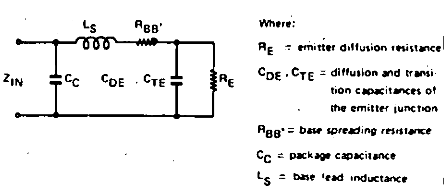


Fig. 2 – Equivalent circuit for the input impedance of RF-power transistors

Most of the VHF high band transistors will have the series resonant frequency within their operating range, i.e. be purely resistive at one single frequency f_S, while the parallel resonant frequency f_P will be outside.

Parameters for one or two gigahertz transistors will be beyond f_S and approach f_P. They show a high value of R_P and X_P with inductive character.

A parameter that is very often used to judge on the broadband capabilities of a device is the input Q or Q_{IN}, defined simply as the ratio R_P/X_P. Practically Q_{IN} ranges around 1 or less for VHF devices and around 5 or more for microwave transistors.

Q_{IN} is an important parameter to consider for broadband matching. Matching networks normally are low-pass or pseudo low-pass filters. If Q_{IN} is high, it can be necessary to use band-pass filter type matching networks and to allow insertion losses. But broadband matching is still possible. This will be discussed later.

2.2. OUTPUT IMPEDANCE

The output impedance of the RF-power transistors, as given by all manufacturers' data sheets, generally consists of only a capacitance C_{OUT}. The internal resistance of the transistor is supposed to be much higher than the load and is normally neglected. In the case of a relatively low internal resistance, the efficiency of the device would decrease by the factor:

$$1 + R_L/R_T$$

where R_L is the load resistance, seen at the collector-emitter terminals, and R_T the internal transistor resistance equal to:

$$\frac{1}{\omega_T \cdot (C_{TC} + C_{DC})},$$

defined as a small signal parameter, where:

ω_T = transit angular frequency

$C_{TC} + C_{DC}$ = transition and diffusion capacitances at the collector junction

The output capacitance C_{OUT}, which is a large signal parameter, is related to the small signal parameter C_{CB}, the collector-base transistion capacitance.

Since a junction capacitance varies with the applied voltage, C_{OUT} differs from C_{CB} in that it has to be averaged over the total voltage swing. For an abrupt junction and assuming certain simplifications, $C_{OUT} = 2\ C_{CB}$.

Figure 3 shows the variation of C_{OUT} with frequency. C_{OUT} decreases partly due to the presence of the collector lead inductance, but mainly because of the fact that the base-emitter diode does not shut off anymore when the operating frequency approaches the transit frequency f_T.

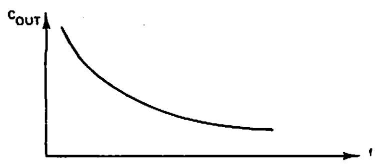


Fig. 3 – Output capacitance C_{OUT} as a function of frequency

3. OUTPUT LOAD

In the absence of a more precise indication, the output load R_L is taken equal to:

$$R_L = \frac{[V_{CC} - V_{CE\ (sat)}]^2}{2\,P_{OUT}}$$

with $V_{CE\ (sat)}$ equal to 2 or 3 volts, increasing with frequency.

The above equation just expresses a well-known relation, but also shows that the load, in first approximation, is not related to the device, except for $V_{CE\ (sat)}$. The load value is primarily dictated by the required output power and the peak voltage; it is not matched to the output impedance of the device.

At higher frequencies this approximation becomes less exact and for microwave devices the load that must be presented to the device is indicated on the data sheet. This parameter will be measured on all Motorola RF-power devices in the future.

Strictly speaking, impedance matching is accomplished only at the input. Interstage and load matching are more impedance transformations of the device input impedance and of the load into a value R_L (sometimes with additional reactive component) that depends essentially on the power demanded and the supply voltage.

4. MATCHING NETWORKS

In the following, matching networks will be described by order of complexity. These are ladder type reactance networks.

The different reactance values will be calculated and determined graphically. Increasing the number of reactances broadens the bandwidth. However, networks consisting of more than four reactances are rare. Above four reactances, the improvement is small.

4.1 NUMERICAL DESIGN

4.1.1 Two-Resistance Networks

Resistance terminations will first be considered. Figure 4 shows the reactive L-section and the terminations to be matched.

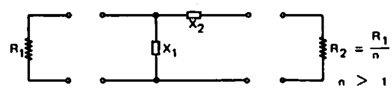


Fig. 4 – Two-Reactance Matching Network

Matching or exact transformation from R_2 into R_1 occurs at a single frequency f_o.

At f_o, X_1 and X_2 are equal to:

$$X_1 = \pm R_1 \sqrt{\frac{R_2}{R_1 - R_2}} = R_1 \frac{1}{\sqrt{n-1}}$$

$$X_2 = \mp \sqrt{R_2 (R_1 - R_2)} = R_1 \frac{\sqrt{n-1}}{n}$$

At f_o: $X_1 \cdot X_2 = R_1 \cdot R_2$

X_1 and X_2 must be of opposite sign. The shunt reactance is in parallel with the larger resistance.

The frequency response of the L-section is shown in Figure 5, where the normalized current is plotted as a function of the normalized frequency.

If X_1 is capacitive and consequently X_2 inductive, then:

$$X_1 = -\frac{f_o}{f} R_1 \sqrt{\frac{R_2}{R_1 - R_2}} = -\frac{f_o}{f} R_1 \frac{1}{\sqrt{n-1}}$$

and $$X_2 = \frac{f}{f_o} \sqrt{R_2 (R_1 - R_2)} = \frac{f}{f_o} R_1 \frac{\sqrt{n-1}}{n}$$

7

The normalized current absolute value is equal to:

$$\left|\frac{I_2}{I_0}\right| = \frac{2\sqrt{n}}{\sqrt{(n-1)^2 \cdot (\frac{f}{f_o})^4 - 2(\frac{f}{f_o})^2 + (n+1)^2}}$$

where $I_o = \frac{\sqrt{n}\,E}{2.R_1}$, and is plotted in Figure 5 (Ref. (2)).

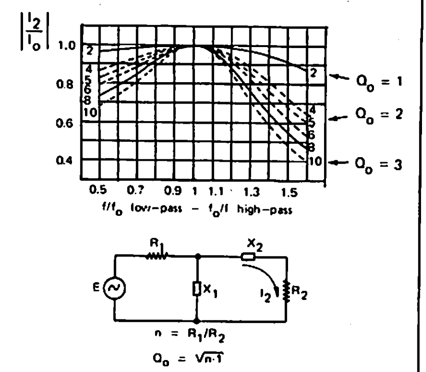


Fig. 5 – Normalized frequency response for the L-section in low-pass or high-pass form

If X_1 is inductive and consequently X_2 capacitive, the only change required is a repacement of f by f_o and vice-versa. The L-section has low pass form in the first case and high-pass form in the second case.

The Q of the circuit at f_o is equal to:

$$Q_o = \frac{X_2}{R_2} = \frac{R_1}{X_1} = \sqrt{n-1}$$

For a given transformation ratio n, there is only one possible value of Q. On the other hand, there are two symmetrical solutions for the network, that can be either a low-pass filter or a high-pass filter.

The frequency f_o does not need to be the center frequency, $\frac{f_1 + f_2}{2}$, of the desired band limited by f_1 and f_2.

In fact, as can be seen from the low-pass configuration of Figure 5, it may be interesting to shift fo toward the high band edge frequency f_2 to obtain a larger bandwidth w, where $w = \frac{2\,(f_1 + f_2)}{f_2 - f_1}$

This will, however, be at the expense of poorer harmonic rejection.

Example:

For a transformation ratio n = 4, it can be determined from the above relations:

Bandwidth w	0.1	0.3
Max insertion losses	0.025	0.2
X_1/R_1	1.730	1.712

If the terminations R_1 and R_2 have a reactive component X, the latter may be taken as part of the external reactance as shown in Figure 6.

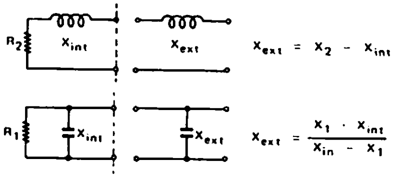


Fig. 6 – Termination Reactance Compensation

This compensation is applicable as long as

$$Q_{INT} = \frac{X_{INT}}{R_2} \text{ or } \frac{R_1}{X_{INT}} < n-1$$

Tables giving reactance values can be found in Ref. (3) and (4).

4.1.1.1 Use of transmission lines and inductors

In the preceding section, the inductance was expected to be realized by a lumped element. A transmission line can be used instead (Fig 7).

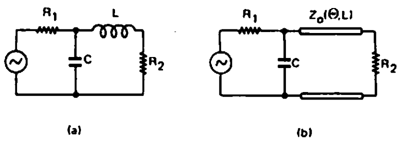


Fig. 7 – Use of a transmission line in the L-section

As can be seen from the computed selectivity curves (Fig. 8) for the two configurations, transmission lines result in a larger bandwidth. The gain is important for a transmission line having a length $L = \lambda/4$ ($\Theta = 90°$) and a characteristic impedance $Z_0 = \sqrt{R_1 \cdot R_2}$. It is not significant for lines short with respect to $\lambda/4$. One will notice that there is an infinity of solutions, one for each value of C, when using transmission lines.

4.1.2 Three-reactance matching networks

The networks which will be investigated are shown in Figure 9. They are made of three reactances alternatively connected in series and shunt.

A three-reactances configuration allows to make the quality factor Q of the circuit and the transformation ratio $n = \frac{R_2}{R_1}$ independent of each other and consequently to choose the selectivity between certain limits.

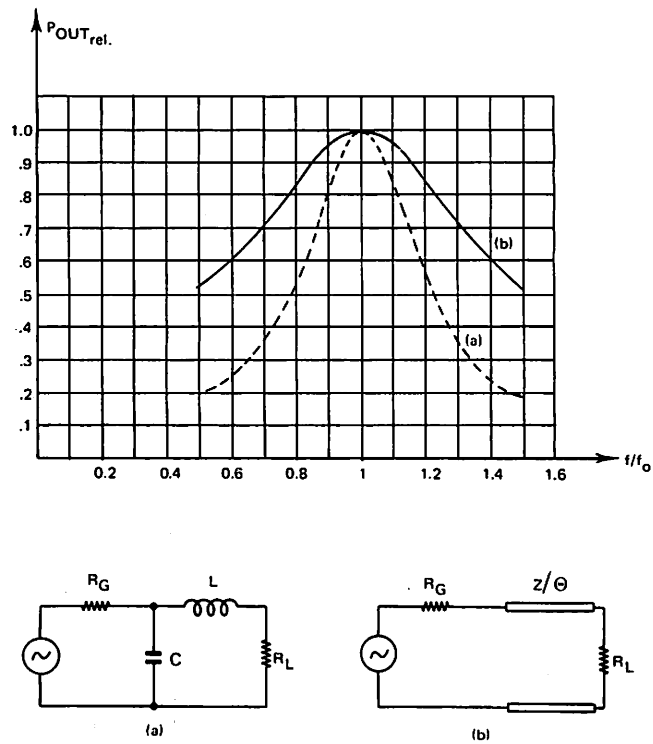
For narrow band designs, one can use the following formulas (Ref. (5) AN-267, where tables are given):

Network (a):

$$X_{C1} = R_1/Q \quad \text{Q must be first selected}$$

$$X_{C2} = R_2 \sqrt{\frac{R_1 R_2}{(Q^2+1) - \frac{R_1}{R_2}}}$$

$$X_L = \frac{QR_1 + (R_1 R_2/X_{C2})}{Q^2 + 1}$$



Transformation ratio n = 10

Fig. 8 – Bandwidth of the L–section for n = 10
(a) with lumped constants
(b) with a transmission line (λ/4)

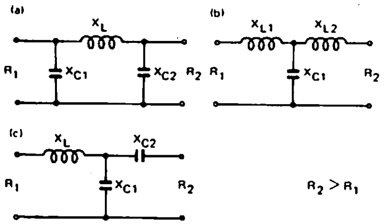


Fig. 9 – Three-reactance matching networks

Network (b) :

Q must first be selected

$$X_{L1} = R_1 Q$$

$$X_{L2} = R_2 . B \qquad A = R_1 \; (1 + Q^2)$$

$$X_{C1} = \frac{A}{Q + B} \qquad B = \sqrt{\frac{A}{R_2} - 1}$$

Network (c) :

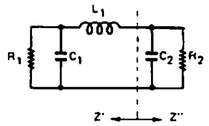
Q must first be selected

$$X_{L1} = Q.R_1$$

$$X_{C2} = A.R_2 \qquad A = \sqrt{\frac{R_1 \; (1+Q^2)}{R_2} - 1}$$

$$X_{C1} = \frac{B}{Q - A} \qquad B = R_1 . (1 + Q^2)$$

With a three-*reactance* configuration, there are not enough degrees of freedom to permit X' = –X'' and simultaneously obtain the same variation of frequency on both curves from M' to point N'.



$$Z' = \frac{R_1}{1 + \omega^2 R_1^2 C_1^2} + j\omega \left[L_1 - \frac{R_1^2 C_1}{1 + \omega^2 R_1^2 C_1^2} \right] = R' + jX'$$

$$Z'' = \frac{R_2}{1 + \omega^2 C_2^2 R_2^2} - \frac{j\omega C_2 R_2^2}{1 + \omega^2 C_2^2 R_2^2} = R'' + jX''$$

$$|X'| = \left(\frac{L_1}{C_1 R_1^2} - \frac{R'}{R_1} \right) \sqrt{\frac{R_1}{R'} - 1}$$

$$|X''| = \sqrt{R' R_2 - R'^2}$$

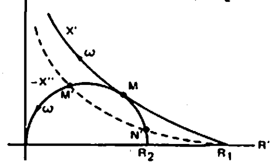


Fig. 10 – Z-plane representation of the circuit of Fig. 9 (a)

The network which yields the most practical component values, should be selected for a given application.

The three-reactance networks can be thought of as being formed of a L-section (two reactances) and of a compensation reactance. The L-section essentially performs the impedance transformation, while the additional reactance compensates for the reactive part of the transformed impedance over a certain frequency band.

Figure 10 shows a representation in the Z-plane of the circuit of Figure 9 (a) split into two parts R_1-C_1-L_1 and C_2-R_2.

Exact transformation from R_1 into R_2 occurs at the points of intersection M and N. Impedances are then conjugate or Z' = R' + jX' and Z'' = R'' + jX'' with R' = R'' and X' = –X''.

The only possible solution is obtained when X' and -X'' are tangential to each other. For the dashed curve, representing another value of L_1 or C_1, a wider frequency band could be expected at the expense of some ripple inside the band. However, this can only be reached with four reactances as will be shown in section 4.1.3.

Exact transformation can, therefore, only be obtained at one frequency.

The values of the three reactances can be calculated by making X' = -X'', R' = R'' and $\frac{dX'}{dR'} = -\frac{dX''}{dR''}$.

The general solution of these equations leads to complicated calculations. Therefore, computed tables should be used.

One will note on Figure 10 that the compensation reactance contributes somewhat to impedance transformation, i.e. R' varies when going from M to R_2.

The circuit of Figure 9 (b) is dual with respect to the first one and gives exactly the same results in a Y-plane representation.

Circuit of Figure 9 (c) is somewhat different since only one intersection M exists as shown in Figure 11. Narrower frequency bands must be expected from this configuration. The widest band is obtained for $C_1 = \infty$.

Again, if one of the terminations has a reactive component, the latter can be taken as a part of the matching network, provided it is not too large (see Fig. 6).

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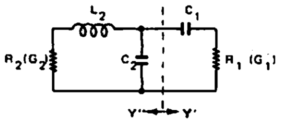


$$Y' = G' + jB' = \frac{\omega^2 C_1^2 R_1}{1+\omega^2 C_1^2 R_1^2} - \frac{j\omega C_1}{1+\omega^2 C_1^2 R_1^2}$$

$$Y'' = G'' + jB'' = \frac{R_2}{R_2^2+\omega^2 L_2^2} + j\omega C_2 - \frac{j\omega L_2}{R_2^2+\omega^2 L_2^2}$$

$$B' = -\sqrt{G'/R_1 - G'^2} \qquad B'' = (1/kR_2 - G'')\sqrt{1/G''R_2 - 1}$$

$$k = L_2 / C_2 R_2^2$$

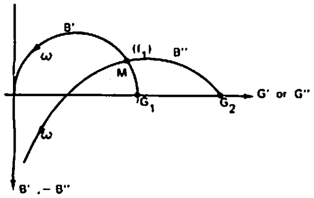


Fig. 11 – Y-plane representation of the circuit of fig. 9 (c)

4.1.3 Four-reactance networks

Four-reactance networks are used essentially for broadband matching. The networks which will be considered in the following consist of two two-reactance sections in cascade. Some networks have pseudo low-pass filter character, others band-pass filter character. In principle, the former show narrower bandwidth since they extend the impedance transformation to very low frequencies unnecessarily, while the latter insure good matching over a wide frequency band around the center frequency only (see Fig. 14).

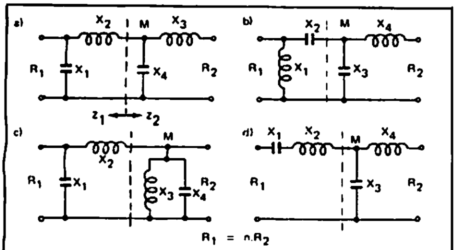


Fig. 12 – Four-reactance networks

The two-reactance sections used in above networks have either transformation properties or compensation properties. Impedance transformation is obtained with one series reactance and one shunt reactance. Compensation is made with both reactances in series or in shunt.

If two cascaded transformation networks are used, transformation is accomplished partly by each one.

With four-reactance networks there are two frequencies. f_1 and f_2, at which the transformation from R_1 into R_2 is exact. These frequencies may also coincide.

For network (b) for instance, at point M, R_1 or R_2 is transformed into $\sqrt{R_1R_2}$ when both frequencies fall together. At all points (M), Z_1 and Z_2 are conjugate if the transformation is exact.

In the case of Figure 12 (b) the reactances are easily calculated for equal frequencies:

$$X_1 = \frac{R_1}{\sqrt{\sqrt{n}-1}}, \quad X_2 = R_1\sqrt{\frac{\sqrt{n}-1}{n}} \qquad X_1.X_4 = R_1.R_2 = X_2.X_3$$

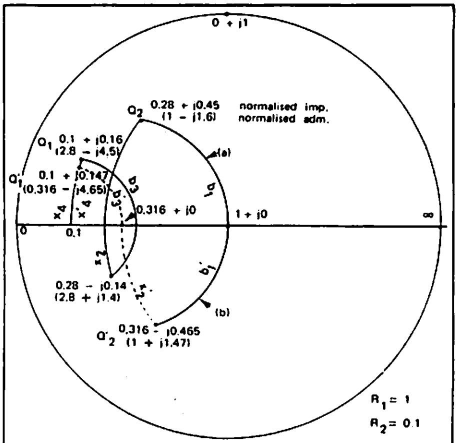
$$X_3 = \frac{R_1}{\sqrt{n}\,(\sqrt{n}-1)}, \quad X_4 = \frac{R_1}{n}\sqrt{\sqrt{n}-1}$$

For network (a) normally, at point (M), Z_1 and Z_2 are complex. This pseudo low-pass filter has been computed elsewhere (Ref. (3)). Many tables can be found in the literature for networks of four and more reactances having Tchebyscheff character or maximally-flat response (Ref. (3), (4) and (6)).

Figure 13 shows the transformation path from R_1 to R_2 for networks (a) and (b) on a Smith-Chart (refer also to section 4.2, Graphic Design).

Case (a) has been calculated using tables mentioned in Ref. (4).

Case (b) has been obtained from the relationship given above for $X_1 \ldots X_4$. Both apply to a transformation ratio equal to 10 and for $R_1 = 1$.



(a) $X_1 = 0.624$ ($B_1 = 1.6$ $\quad X_3 = 0.169$ ($B_3 = 5.9$
$X_2 = 0.59 \quad X_4 = 0.160$
$Q_1 = 1.6 = Q_2$

(b) $X'_1 = 0.68$ ($B'_1 = 1.47$ $\quad X'_3 = 0.215$ ($B'_3 = 4.65$
$X'_2 = 0.465 \quad X'_4 = 0.147$
$Q'_1 = Q'_2 = 1.47$

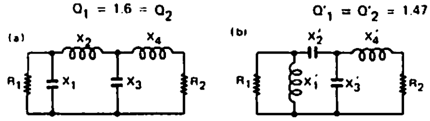


Fig. 13 – Transformation paths for networks (a) and (b)

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There is no simple relationship for $X'_1 \ldots X'_4$ of network (b) if f_1 is made different from f_2 for larger bandwidth.

Figure 14 shows the respective bandwidths of network (a) and (b) for the circuits shown in Figure 13.

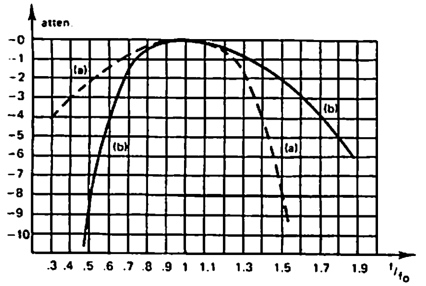


Fig. 14 – Selectivity curves for networks (a) and (b) of Fig. 13

If the terminations contain a reactive component, the computed values for X_1 or X_4 may be adjusted to compensate for this.

For configuration (a), it can be seen from Figure 13, that in the considered case the Q's are equal to 1.6.

For configuration (b) Q'_1, which is equal to Q'_2, is fixed for each transformation ratio.

n	2	4	8	10	16
$Q'_1 = Q'_2$	0.65	1	1.35	1.46	1.73

$$Q' = \sqrt{\sqrt{n} - 1}$$

The maximum value of reactance that the terminations may have for use in this configuration can be determined from the above values of Q'.

If R1 is the load resistance of a transistor, the internal transistor resistance may not be equal to R_1. In this case the selectivity curve will be different from the curves given in Figure 14. Figure 15 shows the selectivity for networks (a) and (b) when the source resistance R_1 is infinite.

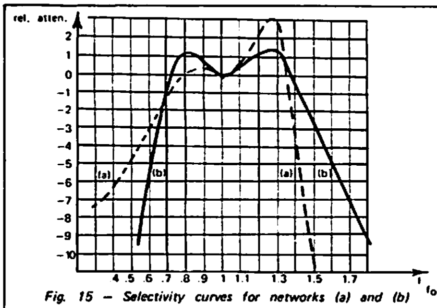


Fig. 15 – Selectivity curves for networks (a) and (b) of Fig. 13 with infinite R_1

From Figure 15 it can be seen that network (a) is more sensitve to R_1 changes than network (b).

As mentioned earlier, the four-reactance network can also be thought of as two cascaded two-reactance sections; one used for transformation, the other for compensation. Figure 16 shows commonly used compensation networks, together with the associated L-section.

The circuit of Figure 16 (a) can be compared to the three-reactance network shown *in Figure 9 (c). The* difference is that capacitor C_2 of that circuit has been replaced by a L-C circuit. The resulting improvement may be seen by comparing Figure 17 with Figure 11.

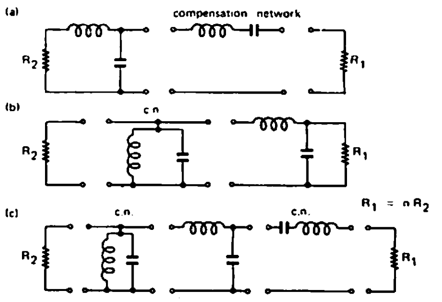
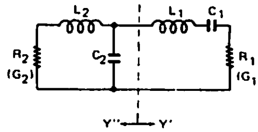


Fig. 16 – Compensation networks used with a L-section



$$Y' = G' + jB' = \frac{R_1}{R_1^2 + (\omega L_1 - 1/\omega C_1)^2} - \frac{j(\omega L_1 - 1/\omega C_1)}{R_1^2 + (\omega L_1 - 1/\omega C_1)^2}$$

$$Y'' = G'' + jB'' = \frac{R_2}{R_2^2 + \omega^2 L_2^2} + j\omega(C_2 - \frac{L_2}{R_2^2 + \omega^2 L_2^2})$$

$$B' = \pm\sqrt{\frac{G'}{R_1} - G'^2}$$

$$B'' = (1/kR_2 - G'')\sqrt{\frac{1}{G''R_2} - 1} \qquad k = \frac{L_2}{C_2 R_2^2}$$

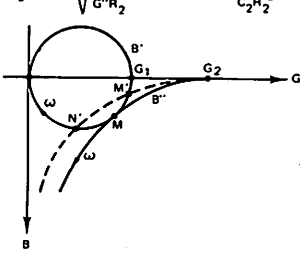


Fig. 17 – Y–plane representation of the circuit of Fig. 16 (a)

By adding one reactance, exact impedance transformation is achieved at two frequencies. It is now possible to choose component values such that the point of intersection M' occurs at the same frequency f_1 on both curves and simultaneously that N' occurs at the same frequency f_2 on both curves. Among the infinite number of possible intersections, only one allows to achieve this.

When M' and N' coincide in M, the new condition $\frac{dX'}{df} = \frac{dX''}{df}$ can be added to the condition $X' = -X''$ (for three-networks) and similarly $R' = R''$ and $\frac{dR'}{df} = \frac{dR''}{df}$.

If f_1 is made different from f_2, a larger bandwidth can be achieved at the expense of some ripple inside the band.

Again, a general solution of the above equations leads to still more complicated calculations than in the case of three-reactance networks. Therefore, tables are preferable (Ref. (3), (4) and (6)).

The circuit of Figure 16 (b) is dual of the circuit of of Figure 14 (a) and does not need to be treated separately. It gives exactly the same results in the Z-plane. Figure 16 (c) shows a higher order compensation requiring six reactive elements.

The above discussed matching networks employing compensation circuits result in narrower bandwidths than the former solutions (see paragraph 4.1.3) using two transformation sections. A matching with higher order compensation such as in Figure 16 (c) is not recommended. Better use can be made of the large number of reactive elements using them all for transformation.

When the above configurations are realized using short portions of transmission lines, the equations or the usual tables no longer apply. The calculations must be carried out on a computer, due to the complexity. However, a graphic method can be used (see next section) which will consist essentially in tracing a transformation path on the Z-Y-chart using the computed lumped element values and replacing it by the closest path obtained with distributed constants. The bandwidth change is not significant as long as short portions of lines are used (Ref. (13)).

4.1.4 Matching networks using quarter-wave transformers

At sufficiently high frequencies, where $\lambda/4$-long lines of practical size can be realized, broadband transformation can easily be accomplished by the use of one or more $\lambda/4$-sections.

Figure 18 summarizes the main relations for (a) one-section and (b) two-section transformation.

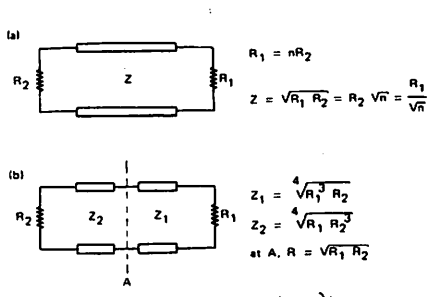


Fig. 18 – Transformation networks using $\lambda/4$-long transmission lines

A compensation network can be realized using a $\lambda/2$-long transmission line.

Figures 19 and 20 show the selectivity curves for different transformation ratios and section numbers.

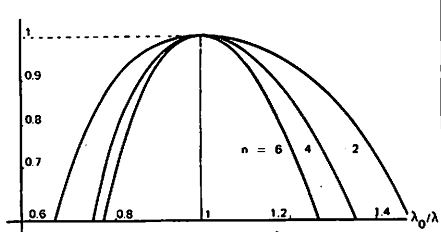


Fig. 19 – Selectivity curves for two $\lambda/4$-section networks at different transformation ratios

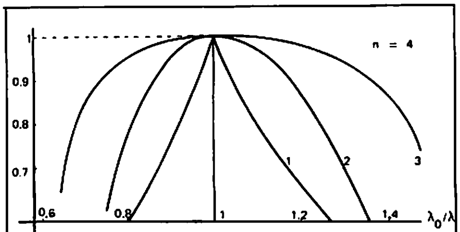


Fig. 20 – Selectivity curves for one, two and three $\lambda/4$-sections

Exponential lines

Exponential lines have largely frequency independent transformation properties.

The characteristic impedance of such lines varies exponentially with their length l:

$$Z = Z_0 . e^{kl}$$

where k is a constant,

but these properties are preserved only if k is small.

4.1.5 Broadband matching using band-pass filter type networks. High Q case.

The above circuits are applicable to devices having low input or output Q, if broadband matching is required. Generally, if the impedances to be matched can be represented for instance by a resistor R in series with an inductor L (sometimes a capacitor C) within the band of interest and if L is sufficiently low, the latter can be incorporated into the first inductor of the matching network. This is also valid if the representation consists of a shunt combination of a resistor and a reactance

Practically this is feasible for Q's around one or two. For higher Q's or for input impedances consisting of a series or parallel resonant circuit (see Fig. 2), as it appears to be for large bandwidths, a different treatment must be followed.

Let us first recall that, as shown by Bode and Fano (Ref. (7) and (8)), limitations exist on the impedance matching of a complex load. In the example of Figure 21, the load to be matched consists of a capacitor C and a resistor R in shunt.

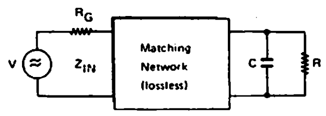


Fig. 21 – General matching conditions

The reflection coefficient between transformed load and generator is equal to:

$$\Gamma = \frac{Z_{IN} - R_g}{Z_{IN} + R_g}$$

$\Gamma = 0$, perfect matching.

$\Gamma = 1$, total reflection.

The ratio of reflected to incident power is:

$$\frac{Pr}{Pi} = |\Gamma|^2$$

The fundamental limitation on the matching takes the form:

$$\int_{\omega=0}^{\infty} \ln\left(\frac{1}{|\Gamma|}\right) d\omega \leq \frac{\pi}{RC} \qquad \text{Bode equation}$$

and is represented in Figure 22.

The meaning of Bode equation is that the area S under the curve cannot be greater than $\frac{\pi}{RC}$ and therefore, if matching is required over a certain bandwidth, this can only be done at the expense of less power transfer within the band. Thus, power

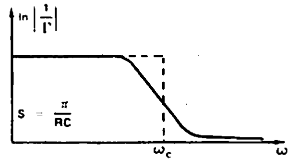


Fig. 22 – Representation of Bode equation

transfer and bandwidth appear as interchangeable quantities.

It is evident that the best utilization of the area S is obtained when $|\Gamma|$ is kept constant over the desired band ω_c and made equal to 1 over the rest of the spectrum. Then $|\Gamma| = e^{-\frac{\pi}{\omega_c RC}}$ within the band and no power transfer happens outside.

A network fulfilling this requirement cannot be obtained in practice as an infinite number of reactive elements would be necessary.

If the attenuation a is plotted versus the frequency for practical cases, one may expect to have curves like the ones shown in Figure 23 for a low-pass filter having Tchebyscheff character.

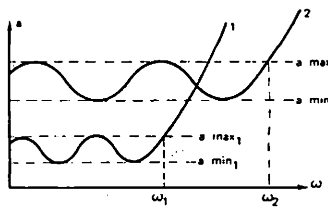


Fig. 23 – Attenuation versus angular frequency for different bandwidths with same load

For a given complex load, an extension of the bandwidth from ω_1 to ω_2, is possible only with a simultaneous increase of the attenuation a. This is especially noticeable for Q's exceeding one or two (see Figure 24).

Thus, devices having relatively high input Q's are useable for broadband operation, provided the consequent higher attenuation or reflection introduced is acceptable.

The general shape of the average insertion losses or attenuation a (neglecting the ripple) of a low-pass impedance matching network is represented in Figure 24 as a function of 1/Q for different numbers of network elements n (ref. (3)).

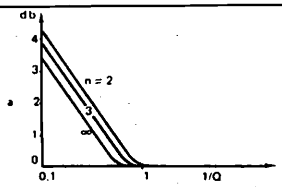


Fig. 24 – Insertion losses as a function of 1/Q

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For a given Q and given ripple, the attenuation decreases if the number n of the network elements increases. But above n = 4, the improvement is small.

For a given attenuation a and bandwidth, the larger n the smaller the ripple.

For a given attenuation and ripple, the larger n the larger the bandwidth.

Computations show that for $Q < 1$ and $n \leqslant 3$ the attenuation is below 0.1 db approximately. The impedance transformation ratio is not free here. The network is a true low-pass filter. For a given load, the optimum generator impedance will result from the computation.

Before impedance transformation is introduced, a conversion of the low-pass prototype into a band-pass filter type network must be made. Figure 25 summarizes the main relations for this conversion.

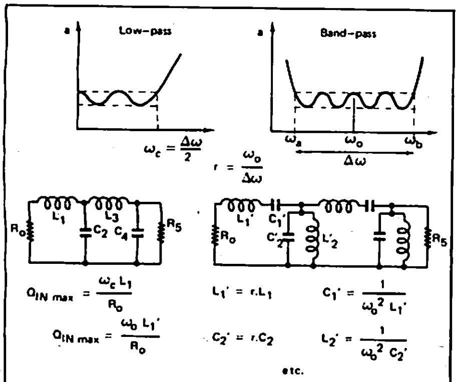

Fig. 25 – Conversion from low-pass into band-pass filter

r is the conversion factor.

For the band-pass filter, Q_{IN} max or the maximum possible input Q of a device to be matched, has been increased by the factor r (from Figure 25, $Q'_{IN\,max} = r.Q_{IN\,max}$).

Impedance inverters will be used for impedance transformation. These networks are suitable for insertion into a band-pass filter without affecting the transmission characteristics.

Figure 26 shows four impedance inverters. It will be noticed that one of the reactances is negative and must be combined in the band-pass network with a reactance of at least equal positive value. Insertion of the inverter can be made at any convenient place (Ref. (3) and (9)).

When using the band-pass filter for matching the input impedance of a transistor, reactances L'_1 C'_1 should be made to resonate at ω_o by addition of a convenient series reactance.

As stated above, the series combination of Ro, L'_1 and C'_1 normally constitutes the equivalent input network of a transistor when considered over a large bandwidth. This is a good approximation up to about 500 MHz.

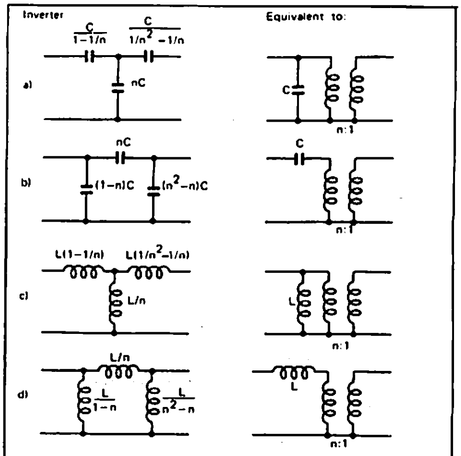

Fig. 26 – Impedance inverters

In practice the normal procedure for using a band-pass filter type matching network will be the following:

(1) For a given bandwidth, center frequency and input impedance of a device to be matched e.g. to 50 ohms, first determine Q_{IN}' from the data sheet as $\frac{\omega_o L'_1}{R_o}$ after having eventually added a series reactor for centering,

(2) Convert the equivalent circuit $R_o L_1{}'$ $C_1{}'$ into a low-pass prototype R_o L_1 and calculate Q_{IN} using the formulas of Figure 25,

(3) Determine the other reactance values from tables (Ref. (3)) for the desired bandwidth,

(4) Convert the element values found by step (3) into series or parallel resonant circuit parameters,

(5) Insert the impedance inverter in any convenient place.

In the above discussions, the gain roll-off has not been taken into account. This is of normal use for moderate bandwidths (30% for ex.). However, several methods can be employed to obtain a constant gain within the band despite the intrinsic gain decrease of a transistor with frequency.

Tables have been computed elsewhere (Ref. (10)) for matching networks approximating 6 db/octave attenuation versus frequency.

Another method consists in using the above mentioned network and then to add a compensation circuit as shown for example in Figure 27.

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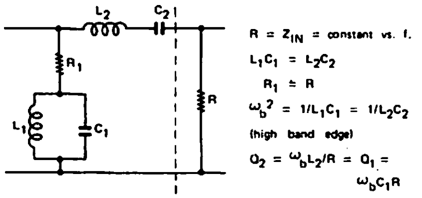


Fig. 27 – Roll–off compensation network

Resonance ω_b is placed at the high edge of the frequency band. Choosing Q correctly, roll-off can be made 6 db/octave.

The response of the circuit shown in Figure 27 is expressed by:

$$\frac{1}{1+Q^2\left(\frac{\omega}{\omega_b}-\frac{\omega_b}{\omega}\right)^2}\text{, where } \omega<\omega_b$$

This must be equal to $\frac{\omega}{\omega_b}$ for 6db/octave compensation.

At the other band edge a, exact compensation can be obtained if:

$$Q=\frac{\left(\frac{\omega_b}{\omega_a}\right)^2-1}{\frac{\omega_a}{\omega_b}-\left(\frac{\omega_b}{\omega_a}\right)^2}$$

4.1.6 Line Transformers

The broadband properties of line transformers make them very useful in the design of broadband impedance matching networks (Ref. (11) and (12)).

A very common form is shown by Figure 28. This is a 4:1 impedance transformer. Other transformation ratios like 9 : 1 or 16 : 1 are also often used but will not be considered here.

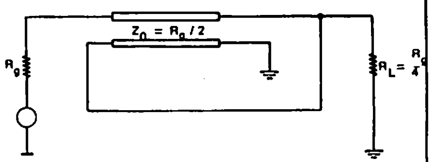


Fig. 28 – 4:1 line transformer

The high frequency cut-off is determined by the length of line which is usually chosen smaller than λ min/8. Short lines extend the high frequency performance.

The low frequency cut-off is determined first by the length of line, long lines extending the low frequency performance of the transformer. Low frequency cut-off is also improved by a high even mode impedance, which can be achieved by the use of ferrite material. With matched ends, no power is coupled through the ferrite which cannot saturate.

For matched impedances, the high frequency attenuation a of the 4 : 1 transformer is given by:

$$a=\frac{(1+3\cos 2\pi\, l/\lambda)^2+4\sin^2 2\pi\, l/\lambda}{4(1+\cos 2\pi\, l/\lambda)^2}$$

For $l=\lambda/4$, $a = 1.25$ or 1 db ; for $l=\lambda/2$, $a=\infty$.

The characteristic impedance of the line transformer must be equal to:

$Zo = \sqrt{Rg.R}$.

Figures 29 and 30 show two different realizations of 4 : 1 transformers for a 50 to 12.5 ohm-transformation designed for the band 118-136 MHz.

The transformers are made of two printed circuit boards or two ribbons stuck together and connected as shown in Figures 29 and 30.

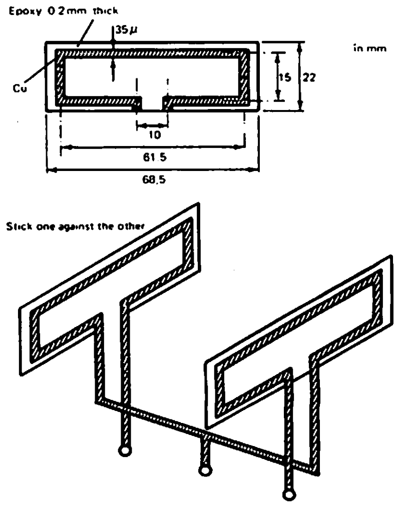
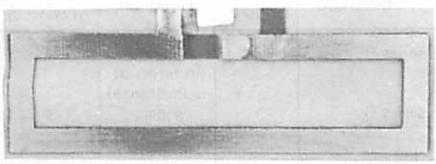
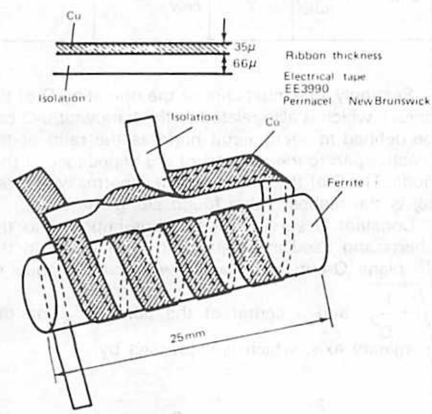


Fig. 29 – 4:1 line transformer on p.c. board

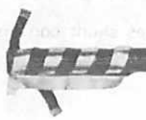


Line transformer on p.c. board (Fig. 29)



Stick one ribbon (1.5mm wide) against the other (2.5)
Total length per ribbon 9cm
Turns 3.5

Fig. 30 – 4:1 copper ribbon line transformer with ferrite



Line transformer on ferrite (Fig. 30)

4.2 GRAPHIC DESIGN

The common method of graphic design makes use of the Impedance-Admittance Chart (Smith Chart).

It is applicable to all ladder-type networks as encountered in matching circuits.

Matching is supposed to be realized by the successive algebraic addition of reactances (or susceptances) to a given start impedance (or admittance) until another end impedance (or admittance) is reached.

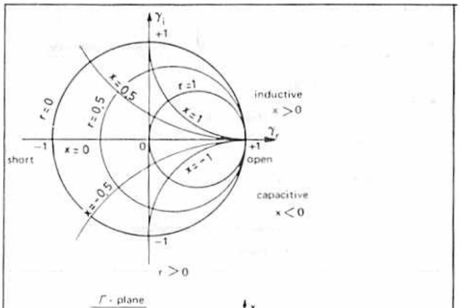
Impedance chart and admittance chart can be superimposed and used alternatively due to the fact that an immittance point, defined by its reflection coefficient Γ with respect to a reference, is common to the Z-chart and the Y-chart, both being representations in the Γ-plane.

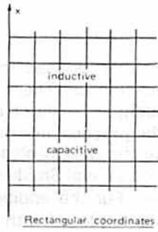
$$\Gamma = \frac{Z-R_s}{Z+R_s} = \gamma_r + j\gamma_i$$

$$\Gamma = \frac{G_s-Y}{G_s+Y} \qquad R_s = \frac{1}{G_s} = \text{Characteristic impedance of the line}$$

More precisely, the Z-chart is a plot in the Γ-plane, while the Y-chart is a plot in the −Γ-plane. The change from the Γ to −Γ-plane is accounted for in the construction rules given below.

Figure 31 and 32 show the representation of normalized Z and Y respectively, in the Γ-plane.





$$\frac{Z}{R_s} = z = r + jx$$

$$r = \frac{1-\gamma_r^2-\gamma_i^2}{(1-\gamma_r)^2 + \gamma_i^2}$$

$$x = \frac{2\gamma_i}{(1-\gamma_r)^2 + \gamma_i^2}$$

$$\gamma_r = \frac{r^2 + x^2 - 1}{(r+1)^2 + x^2}$$

$$\gamma_i = \frac{2x}{(r+1)^2 + x^2}$$

$$r \text{ circles} \begin{cases} \text{Radius} : 1/(1+r) \\ \text{Center at} \quad \gamma_r = \frac{r}{1+r}, \ \gamma_i = 0 \end{cases}$$

$$x \text{ circles} \begin{cases} \text{Radius} : 1/x \\ \text{Center at} \quad \gamma_r = 1, \ \gamma_i = 1/x \end{cases}$$

Fig. 31 – Representation of the normalized Z values in the Γ-plane

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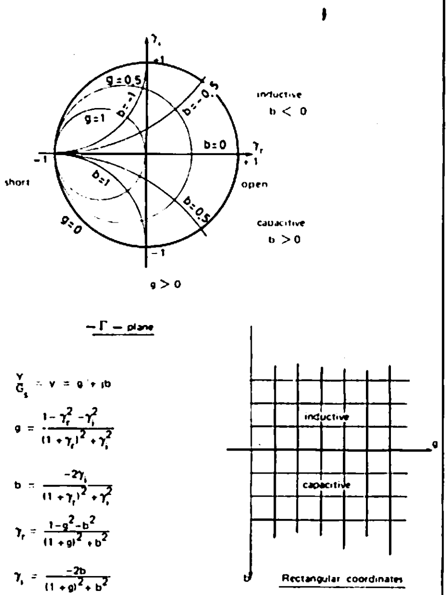


$\frac{Y}{G_s} = y = g + jb$

$g = \frac{1-\gamma_r^2-\gamma_i^2}{(1+\gamma_r)^2+\gamma_i^2}$

$b = \frac{-2\gamma_i}{(1+\gamma_r)^2+\gamma_i^2}$

$\gamma_r = \frac{1-g^2-b^2}{(1+g)^2+b^2}$

$\gamma_i = \frac{-2b}{(1+g)^2+b^2}$

g circles: Radius $1/(1+g)$; Center at $\gamma_r = -g/(1+g)$; $\gamma_i = 0$

b circles: Radius $1/b$; Center at $\gamma_r = -1$, $\gamma_i = -1/b$

Fig. 32 – Representation of the normalized Y–values in the Γ– plane

Addition of	Chart to be used	Direction	Using curve of constant
series R	Z	open (in terms of admittance)	x
series G	Y	short (in terms of admittance)	b
series C $(+\frac{1}{j\omega C})$	Z	ccw	r
shunt C $(+j\omega C)$	Y	cw	g
series L $(+j\omega L)$	Z	cw	r
shunt L $(+\frac{1}{j\omega L})$	Y	ccw	g

Secondly, one must choose the operating Q of the circuit, which is also related to the bandwidth. Q can be defined at each circuit node as the ratio of the reactive part to the real part of the impedance at that node. The Q of the circuit, which is normally referred to, is the highest value found along the path.

Constant Q curves can be superimposed to the charts and used in conjunction with them. In the Γ -plane, Q-curves are circles with a radius equal to $\sqrt{1+\frac{1}{Q^2}}$ and a center at the point $\pm\frac{1}{Q}$ on the imaginary axis, which is expressed by:

$$Q = \frac{x}{r} = \frac{2\gamma_i}{1-\gamma_r^2-\gamma_i^2} \qquad \gamma_r^2 + (\gamma_i + \frac{1}{Q})^2 = 1 + \frac{1}{Q^2}.$$

The Z-chart is used for the algebraic addition of series reactances. The Y-chart is used for the algebraic addition of shunt reactances.

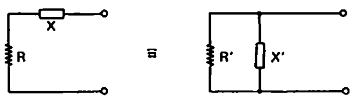
For the practical use of the charts, it is convenient to make the design on transparent paper and then place it on a usual Smith-chart of impedance type (for example). For the addition of a series reactor, the chart will be placed with "short" to the left. For the addition of a shunt reactor, it will be rotated by 180° with "short" (always in terms of impedance) to the right.

The following design rules apply. They can very easily be found by thinking of the more familiar Z and Y representation in reactangular coordinates.

For joining two impedance points, there are a infinity of solutions. Therefore, one must first decide on the number of reactances that will constitute the matching network. This number is related essentially to the desired bandwidth and the transformation ratio.

The use of the charts will be illustrated with the help of an example.

The following series shunt conversion rules also apply:



$$R = \frac{R'}{1+\frac{R'^2}{X'^2}} \qquad G' = \frac{1}{R'} = \frac{R}{R^2+X^2}$$

$$X = \frac{X'}{1+\frac{X'^2}{R'^2}} \qquad -B' = \frac{1}{X'} = \frac{X}{R^2+X^2}$$

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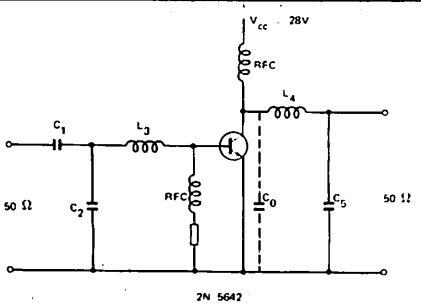


Fig. 33 – Narrow-band VHF power amplifier

Figure 33 shows the schematic of an amplifier using the 2N5642 RF power transistor. Matching has to be achieved at 175 MHz, on a narrow band basis.

The rated output power for the device in question is 20 W at 175 MHz and 28 V collector supply. The input impedance at these conditions is equal to 2.6 ohms in parallel with -200 pF (see data Sheet). This converts to a resistance of 1.94 ohms in series with a reactance of 1.1 ohm.

The collector load must be equal to:

$$\frac{[\,V_{cc} - V_{ce\,(sat)}\,]^2}{2 \times P_{out}} \text{ or } \frac{(28-3)^2}{40} = 15.6 \text{ ohms.}$$

The collector capacitance given by the data sheet is 40 pF, corresponding to a capacitive reactance of 22.7 ohms.

The output impedance seen by the collector to insure the required output power and cancel out the collector capacitance must be equal to a resistance of 15.6 ohms in parallel with an inductance of 22.7 ohms. This is equivalent to a resistance of 10.6 ohms in series with an inductance of 7.3 ohms.

The input Q is equal to, 1.1/1.94 or 0.57 while the output Q is 7.3/10.6 or 0.69.

It is seen that around this frequency, the device has good broadband capabilities. Nevertheless, the matching circuit will be designed here for a narrow band application and the effective Q will be determined by the circuit itself not by the device.

Figure 34 shows the normalized impedances (to 50 ohms).

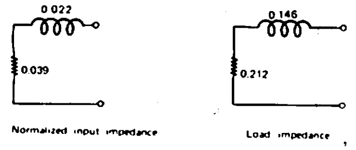


Fig 34 – Normalized input and output impedances for the 2N5642

Figure 35 shows the diagram used for the graphic design of the input matching circuit. The circuit Q must be larger than about 5 in this case and has been chosen equal to 10. At Q = 5, C_1 would be infinite. The addition of a finite value of C_1 increases the circuit Q and therefore the selectivity. The normalized values between brackets in the Figure are admittances (g + jb).

At f = 175MHz, the following results are obtained:

$$\omega L_3 = 50 x_3 = 50\,(0.39 - 0.022) = 18.5 \text{ ohms} \qquad \therefore L_3 = 16.8 \text{ nH}$$

$$\omega C_2 = \frac{1}{50} b_2 = \frac{1}{50}\,(2.5 - 0.42) = 0.0416 \text{ mhos} \qquad \therefore C_2 = 37.8 \text{ pF}$$

$$\frac{1}{\omega C_1} = 50 x_1 = 50\,.\,1.75 = 87.5 \text{ ohms} \qquad \therefore C_1 = 10.4 \text{ pF}$$

Figure 36 shows the diagram for the output circuit, designed in a similar way.

Here, the results are (f = 175MHz) :

$$\omega L_4 = 50.x_4 = 50\,.\,(0.4 + 0.146) = 27.3 \text{ ohms} \qquad \therefore L_4 = 24.8 \text{ nH}$$

$$\omega C_5 = \frac{1}{50} b_5 = \frac{1}{50}\,.\,1.9 = 0.038 \text{ mhos} \qquad \therefore C_5 = 34.5 \text{ pF}$$

The circuit Q at the output is equal to 1.9.

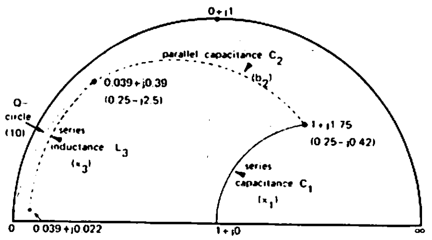


Fig. 35 – Input circuit design

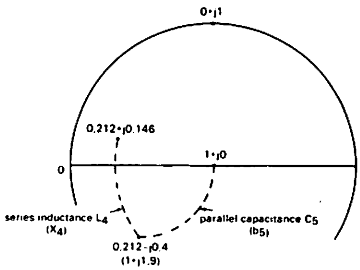


Fig 36 Output circuit design

The selectivity of a matching circuit can also be determined graphically by changing the x or b values according to a chosen frequency change. The diagram will give the VSWR and the attenuation can be computed.

The graphic method is also useful for conversion from a lumped circuit design into a stripline design. The immittance circles will now have their centres on the 1 + jo point.

At low impedance levels (large circles), the difference between lumped and distributed elements is small.

5. PRACTICAL EXAMPLE

The example shown refers to a broadband amplifier stage using a 2N 6083 for operation in the VHF-band 118-136 MHz. The 2N 6083 is a 12.5 V-device and, since amplitude modulation is used at these transmission frequencies, that choice supposes low level modulation associated with a feedback system for distortion compensation.

Line transformers will be used at the input and output. Therefore the matching circuits will reduce to two-reactance networks, due to the relatively low impedance transformation ratio required.

5.1 DEVICE CHARACTERISTICS

Input impedance of the 2N 6083 at 125 MHz:

$$R_p = 0.9 \text{ ohms}$$

$$C_p = -390 \text{ pF}$$

Rated output power:

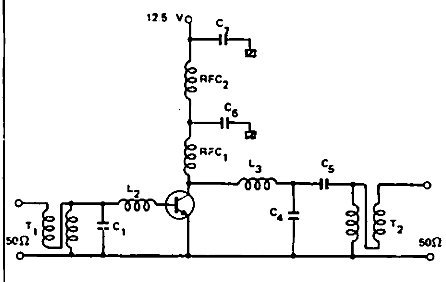
30W for 8W input at 175MHz. From the data sheet it appears that at 125MHz, 30W output will be achieved with about 4W input.

Output impedance:

$$\frac{[V_{cc} - V_{ce\,(sat)}]^2}{2 \times P_{out}} = \frac{100}{60} = 1.67 \text{ ohms}$$

$$C_{out} = 180 \text{ pF at 125 MHz}$$

5.2 CIRCUIT SCHEMATIC



C_1 = 300 pF (chip)	T_1, T_2 see Figure 30
L_2 = 4.2 nH (adjust)	RFC_1 = 7 turns
L_3 = 8 nH (adjust)	6.3 mm coil diameter
C_4 = 130 pF (chip)	0.8 mm wire diameter
C_5 = 750 pF (chip)	RFC_2 = 3 turns on ferrite bead
C_6 = 2.2 μF	C_7 = 0.68 μF

Fig. 37 – Circuit schematic

5.3 TEST RESULTS

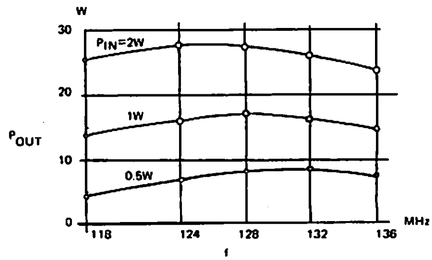


Fig. 38 – P_{OUT} vs frequency

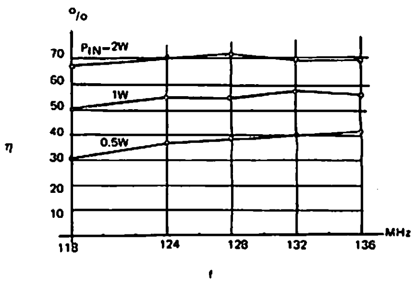


Fig. 39 – η vs frequency

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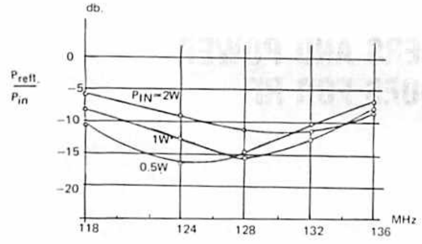
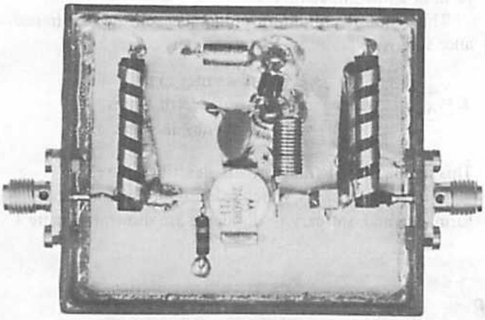


Fig. 40 – $P_{REFL.}/P_{IN}$ vs frequency



118–136 MHz amplifier (see Fig. 37) before coil adjustment.

Acknowledgements:

The author is indebted to Mr. T. O'Neal for the fruitful discussions held with him. Mr. O'Neal designed the circuit shown in Figure 37; Mr. J. Hennet constructed and tested the lab model.

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BROADBAND TRANSFORMERS AND POWER COMBINING TECHNIQUES FOR RF

Prepared by
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INTRODUCTION

The following discussion focuses on broadband transformers for RF power applications with practical examples of various types given with performance data. Detailed design formula are available in the Reference section. Power combining techniques useful in designing high power amplifiers are discussed in detail.

BROADBAND TRANSFORMERS

The input and output transformers are among the most critical components in the design of a multi-octave amplifier. The total performance of the amplifier (linearity, efficiency, VSWR, gain flatness) will depend on their quality. Transformers with high impedance ratios and for low impedances are more difficult to design in general. In the transmission line transformers very low line impedances are required, which makes them impractical for higher than 16:1 impedance ratios in a 50-Ohm system. Other type transformers require tight coupling coefficients between the primary and secondary, or excessive leakage inductances will reduce the effective bandwidth. Twisted line transformers (Figure 1C, D, F, G) are described in References 1, 2, and 4. Experiments have shown that the dielectric losses in certain types of magnet wire, employed for the twisted lines, can limit the power handling capability of such transformers. This appears as heat generated within the transformer at higher frequencies, although part of this may be caused by the losses in the magnetic core employed to improve the low frequency response. At low frequencies, magnetic coupling between the primary and secondary is predominant. At higher frequencies the leakage inductance increases and the permeability of the magnetic material decreases, limiting the bandwidth unless tight capacitive coupling is provided. In a transmission line transformer this coupling can be clearly defined in the form of a line impedance.

The required minimum inductance on the low impedance side is:

$$L = \frac{4\,R}{2\pi f} \quad \text{where} \quad \begin{aligned} L &= \text{Inductance in } \mu\text{H} \\ R &= \text{Impedance in Ohms} \\ f &= \text{Frequency in MHz} \end{aligned}$$

This applies to all transformers described here.

Some transformers, which exhibit good broad band performance and are easy to duplicate are shown in Figure 1.

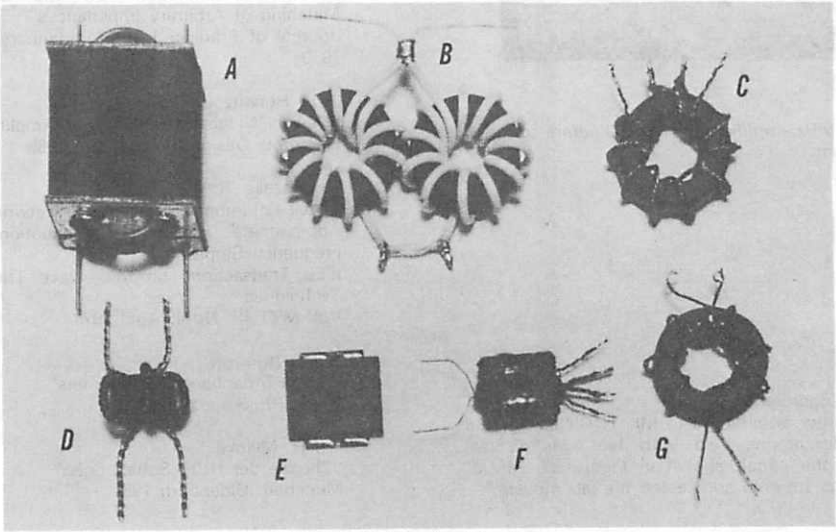


FIGURE 1 – HF Broadband Transformers

Transformers E and F are intended for input applications, although A in a smaller physical form is also suitable. In E, the windings are photo etched on double sided copper-Kapton* (or copper-fiberglass) laminate. The dielectric thickness is 3 mils, and the winding area is 0.25 in^2.

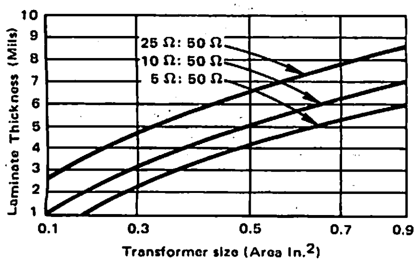


FIGURE 2 — Laminate Thickness versus Winding Area

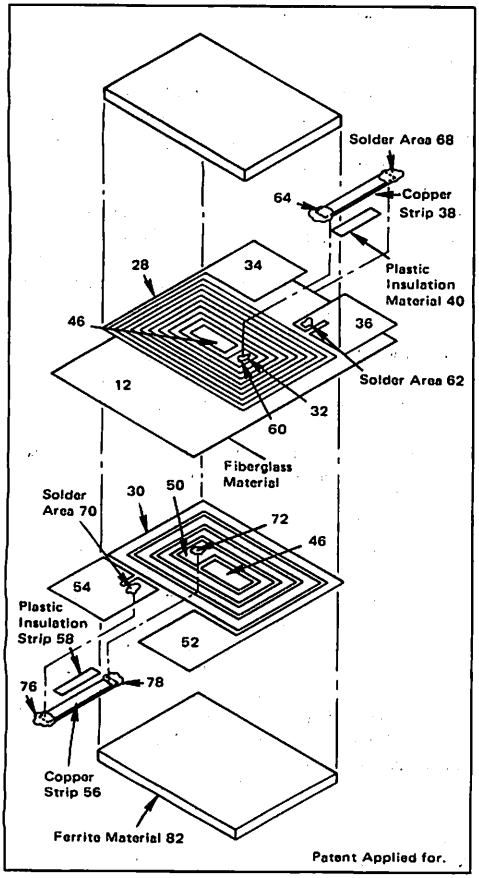


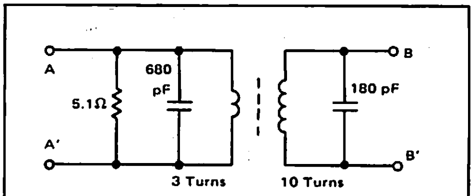
FIGURE 3 — Detailed Structure of Transformer Shown in Figure 1E

*Trademark of E. I. DuPont, De Nemours and Co., Inc.

Ferrite plates (μ_r = 2000 to 3000) are cemented on each side to improve the low frequency response. This type transformer in the size shown, can handle power levels to 10 W. Figure 2 shows curves for laminate thickness versus winding area for various impedance ratios.

Impedance ratios of this transformer are not limited to integers as 1:1, 4:1 —– N:L, and the dc isolated primary and secondary have an advantage in certain circuit configurations. This design will find its applications in high volume production or where the small physical size is of main concern. Table 1 shows the winding configuration and measured data of the transformer shown in Figure 3.

TABLE 1 — Impedance at Terminals BB' Transformer Terminated as Shown



f (MHz)	R_p (Ohms)	X_p (Ohms)
1.0	50.7	+j 81
2.0	53.0	+j 185
4.0	53.1	+j 1518
8.0	53.5	-j 214
16.0	50.5	-j 79
32.0	52.9	-j 30

In the transformer shown in Figure 1F and Table 2, a regular antenna balun core is employed (Indiana General F684-1 or equivalent). Lines A and B each consist of two twisted pairs of AWG #30 enameled wire. The line impedances are measured as 32 Ohms, which is sufficiently close to the optimum 25 Ohms calculated for 4:1 impedance ratio. ($Z_0 = \sqrt{R_{in} \cdot R_L}$).

Windings a and b are wound one on top of the other, around the center section of the balun core. Line c should have an optimum Z_0 of 50 Ohms. It consists of one pair of AWG #32 twisted enameled wire with the Z_0 measured as 62 Ohms. The balun core has two magnetically isolated toroids on which c is wound, divided equally between each. The inductance of c should approach the combined inductance of Lines a and b (Reference 4, 6).

The reactance in the 50 Ohm port (BB') should measure a minimum of + j 200. To achieve this for a 4:1 transformer, a and b should each have three turns, and for a 9:1 transformer, four turns. When the windings are connected as a 9:1 configuration, the optimum Z_0 is 16.6 Ohms, and a larger amount of high frequency compensation will be necessary. Lower impedance lines can be realized with heavier wires or by twisting more than two pairs together. (e.g., four pairs of AWG #36 enameled wire

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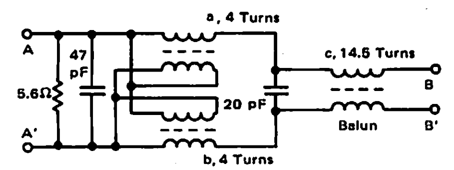
would result in the Z_0 of approximately 18 Ohms.) Detailed information on the manufacture of twisted wire transmission lines can be found in References 2, 4, and 8.

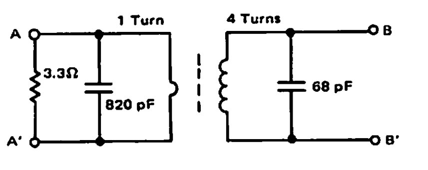
TABLE 2 — Impedance at Terminals BB' Transformer Terminated as Shown



f (MHz)	R_p (Ohms)	X_p (Ohms)
1.0	53.0	+j 185
2.0	52.6	+j 330
4.0	52.9	+j 430
8.0	53.1	+j 600
16.0	53.2	+j 750
32.0	53.5	+j 3060

Figure 1A shows one of the most practical designs for higher impedance ratios (16 and up). The low impedance winding always consists of one turn, which limits the available ratios to integers 1, 4, 9 — N. Data taken of this type of a 16:1 transformer is shown in Table 3, while Figure 4 illustrates the physical construction. Two tubes, 1.4" long and 1/4" in diameter — copper or brass — form the primary winding. The tubes are electrically shorted on one end by a piece of copper-clad laminate with holes for the tubes and the tube ends are soldered to the copper foil. The hole spacing should be larger than the outside diameter of the ferrite sleeves.

TABLE 3 — Impedance at Terminals BB' Transformer Terminated as Shown



f (MHz)	R_p (Ohms)	X_p (Ohms)
1.0	54.0	+j 1030
2.0	54.0	+j 3090
4.0	54.0	+j 5800
8.0	53.9	-j 300
16.0	53.1	-j 760
32.0	53.2	-j 600

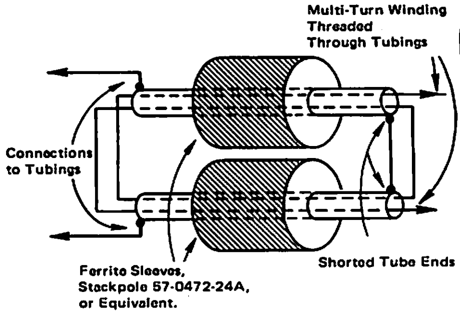


FIGURE 4 — Physical Construction of a 16:1 Transformer (Actual Number of Turns Not Shown)

A similar piece of laminate is soldered to the opposite ends of the tubes, and the copper foil is divided into two sections, thus isolating the ends where the primary connections are made. The secondary winding is formed by threading wire with good RF insulating properties through the tubes for the required number of turns.

Although the measurements indicate negligible differences in performance for various wire sizes and types (stranded or solid), the largest possible diameter should be chosen for lower resistive losses. The initial permeability of the ferrite sleeves is determined by the minimum inductance required for the lowest frequency of operation according to the previous formula. Typical μ_r's can vary from 800 to 3000 depending upon the cross sectional area and lowest operating frequency. Instead of the ferrite sleeves, a number of toroids which may be more readily available, can be stacked.

The coupling coefficient between the primary and secondary is almost a logarithmic function of the tube diameter and length. This factor becomes more important with very high impedance ratios such as 36:1 and up, where higher coupling coefficients are required. The losses in the ferrite are determined by the frequency, permeability and flux density. The approximate power handling capability can be calculated as in Reference 4 and 6, but the ferrite loss factor should be taken into consideration. The μ_r in all magnetic materials is inversely proportional to the frequency, although very few manufacturers give this data.

Two other variations of this transformer are shown in Figure 5. The smaller version is suitable for input matching, and can handle power levels to 20 W. It employs a stackpole dual balun ferrite core 57-1845-24B. The low impedance winding is made of 1/8" copper braid. The portions of braid going through the ferrite are rounded, and openings are made in the ends with a pointed tool. The high impedance winding is threaded through the rounded portions of the braid, which was uncovered in each end of the ferrite core. (See Figures 4 and 5.)

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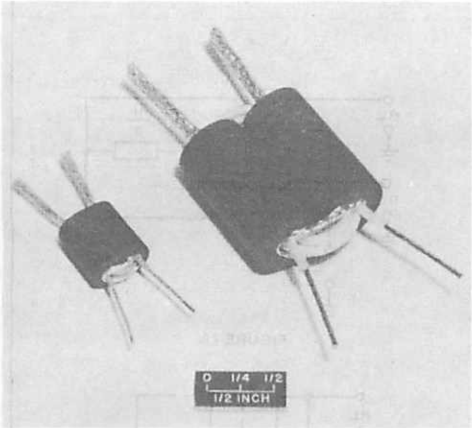


FIGURE 5 – Variations of Transformers in Figure 1A

The construction technique of the larger version transformer is similar, except two separate ferrite sleeves are employed. They can be cemented together for easier handling. This transformer is intended for output applications, with a power handling capability of 200-250 W employing Stackpole 57-0472-27A ferrites. For more detail, see Reference 7.

The transformer shown in Figure 1B is superior in bandwidth and power handling capability. Table 4 shows data taken on a 4:1 transformer of this type. The transmission lines (a and b) are made of 25-Ohm miniature co-axial cable, Microdot 260-4118-000 or equivalent. Two 50 Ohm cables can also be connected in parallel.

The balun, normally required to provide the balanced to unbalanced function is not necessary when the two transmission lines are wound on separate magnetic cores, and the physical length of the lines is sufficient to provide the necessary isolation between AA′ and BB′. The minimum line length required at 2.0 MHz employing Indiana General F627-19-Q1 or equivalent ferrite toroids is 4.2 inches, and the maximum permissible length at 30 MHz would be approximately 20 inches, according to formulas 9 and 10 presented in Reference 2. The 4.2 inches would amount to four turns on the toroid, and measures 1.0 μH. This complies with the results obtained with the formula given earlier for *minimum* inductance calculations.

Increasing the minimum required line length by a factor of 4 will provide the isolation, and the total length is still within the calculated limits. The power loss in this PTFE insulated co-axial cable is 0.03 dB/ft at 30 MHz in contrast to 0.12 dB/ft for a twisted wire line. The total line loss in the transformer will be about 0.1 dB

The number of turns on the toroids has been increased beyond the point where the flux density of the magnetic core is the power limiting factor. The combined line and core losses limit the power handling capability to approximately 300 W, which can be slightly increased by employing lower loss magnetic material.

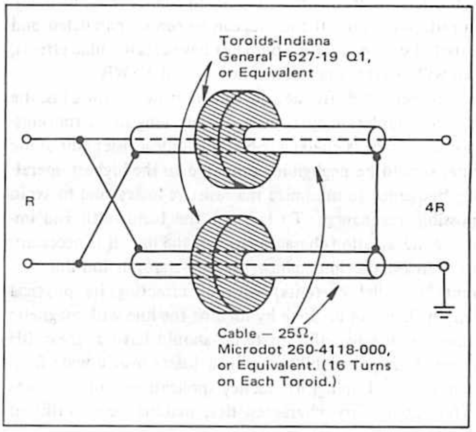
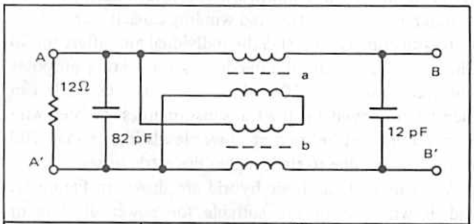


FIGURE 6 – Transformer Construction (Figure 1B)

Note the connection arrangement (Figure 6), where the braid of the cable forms the high current path of the primary.

TABLE 4 – Impedance at Terminals BB′ Transformer Terminated as Shown



f (MHz)	R_p (Ohms)	X_p (Ohms)
1.0	48.3	+j 460
2.0	48.1	+j 680
4.0	48.0	+j 920
8.0	48.0	+j 1300
16.0	48.1	+j 900
32.0	48.1	+j 690

HIGH-FREQUENCY POWER COMBINING TECHNIQUES EMPLOYING HYBRID COUPLERS

The zero degree hybrids described here are intended for adding the powers of a multiple of solid-state amplifiers, or to combine the outputs of groups of amplifiers, usually referred to as modules. With this technique, powers to the kW level at the high-frequency bands can be realized.

When reversed, the hybrids can be used for splitting signals into two or more equal phase and amplitude ports. In addition, they provide the necessary isolation between the sources. The purpose of the isolation is to keep the system operative, even at a reduced power level during a possible failure in one amplifier or module. The isolation is especially important in output combining of linear

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amplifiers, where a constant load impedance must be maintained. Sometimes the inputs can be simply paralleled, and a partial system failure would not have catastrophic effects, but will merely result in increased input VSWR.

For very high frequencies and narrow bandwidths, the hybrid couplers may consist of only lengths of transmission line, such as co-axial cable. The physical lengths of the lines should be negligible compared to the highest operating frequency to minimize the resistive losses, and to avoid possible resonances. To increase the bandwidth and improve the isolation characteristics of the line, it is necessary to increase the impedance for non-transmission line currents (parallel currents) without effecting its physical length. This can be done by loading the line with magnetic material. Ideally, this material should have a linear BH curve, high permeability and low losses over a wide frequency range. For high-frequency applications, some ferrites offer satisfactory characteristics, making bandwidths of four or more octaves possible.

Depending upon the balance and phase differences between the sources, the currents should be mostly cancelled in the balun lines. In a balanced condition, very little power is dissipated in the ferrite cores, and most occurring losses will be resistive. Thus, a straight piece of transmission line loaded with a high permeability ferrite sleeve, will give better results than a multiturn toroid arrangement with its inherent higher distributed winding capacitance.

It is customary to design the individual amplifiers for 50 Ohm input and output impedances for testing purposes and standardization. 50-and 25-Ohm co-axial cable can then be employed for the transmission lines. Twisted wire lines should not be used at power levels higher than 100 Watts average, due to their higher dielectric losses.

Variations of the basic hybrid are shown in Figure 7A and B where both are suitable for power dividing or combining.

The balancing resistors are necessary to maintain a low VSWR in case one of the 50-Ohm points reaches a high impedance as a result of a transistor failure. As an input power splitter, neither 50-Ohm port will ever be subjected to a short due to the base compensation networks, should a base-emitter junction short occur. An open junction will result in half of the input power being dissipated by the balancing resistor, the other half still being delivered to the amplifier in operation. The operation is reversed when the hybrid is used as an output combiner. A transistor failure will practically always cause an increase in the amplifier output impedance. Compared to the 50-Ohm load impedance it can be regarded as an open circuit. When only one amplifier is operative, half of its output power will be dissipated by R, the other half being delivered to the load. The remaining active source will still see the correct load impedance, which is a basic requirement in combining linear amplifiers. The resistors (R) should be of noninductive type, and rated for 25% of the total power, unless some type of automatic shutoff system is incorporated. The degree of isolation obtainable depends upon the frequency, and the overall design of the hybrid. Typical

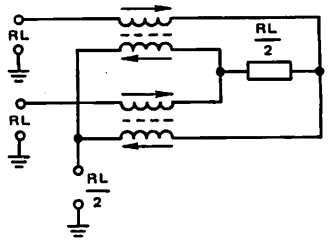

FIGURE 7A

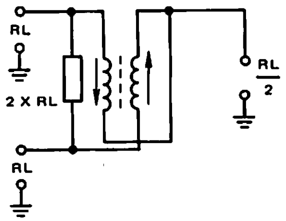

FIGURE 7B

FIGURE 7 — Variations of Basic Hybrid

figures for 2 to 30 MHz operation are 30-40 dB. Figures 8A and B show 4 port "totem pole" structures derived from Figures 7A and 7B. Both can be used with even number of sources only, e.g. 4, 8, 16, etc. For type 8B, it is more practical to employ toroidal multi-turn lines, rather than the straight line alternatives, discussed earlier. The power output with various numbers of inoperative sources can be calculated as follows, if the phase differences are negligible: (Reference 2)

$$P_{out} = \left(\frac{P}{N}\right) N_1$$

where: P = Total power of operative sources
N = Total number of sources
N_1 = Number of operative sources

Assuming the most common situation where one out of four amplifiers will fail, 75% of the total power of the remaining active sources will be delivered to the load.

Another type of multiport hybrid derived from Figure 7A is shown in Figure 9. It has the advantage of being capable of interfacing with an odd number of sources or loads.

In fact, this hybrid can be designed for any number of ports. The optimum values of the balancing resistors will vary according to this and also with the number of ports assumed to be disabled at one time. Two other power combining arrangements are shown in Figures 10 and 11.

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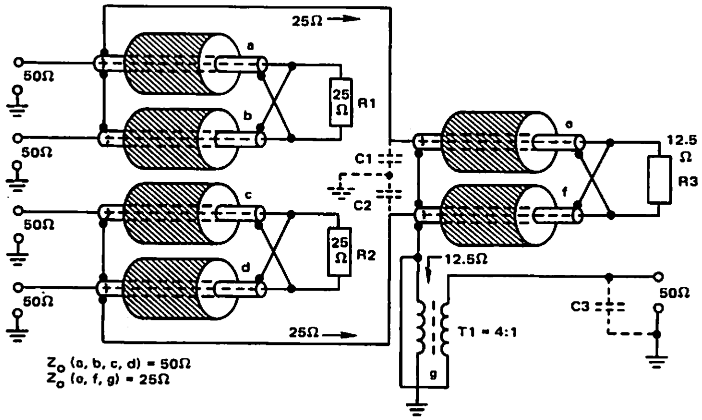

FIGURE 8A

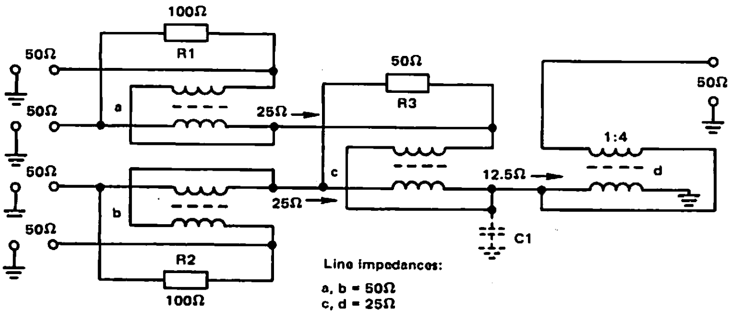

FIGURE 8B

FIGURE 8 — Four Port "Totem Pole" Structure

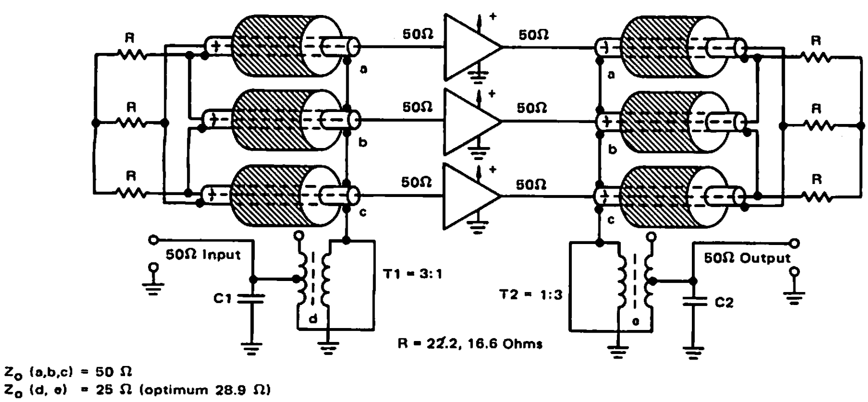

FIGURE 9 — Three-Port Hybrid Arrangement

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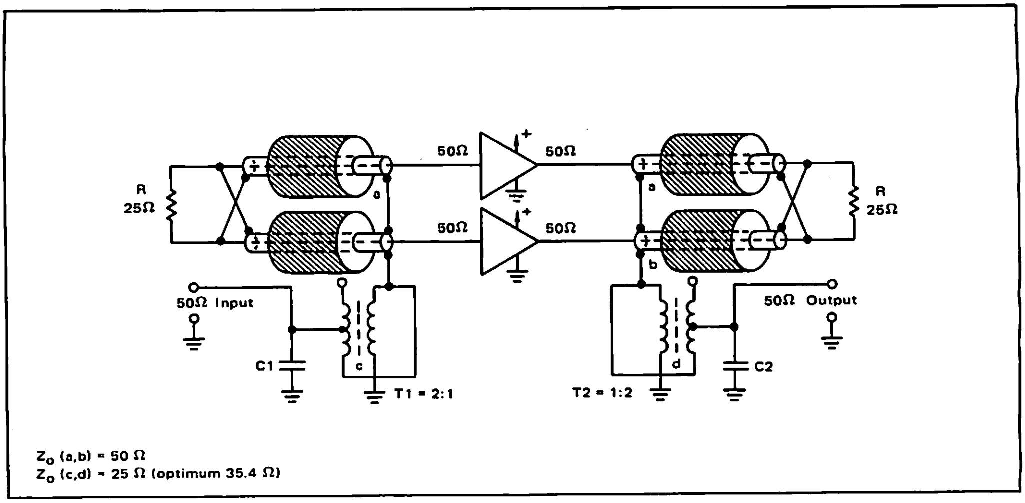

FIGURE 10 — Two-Port Hybrid System

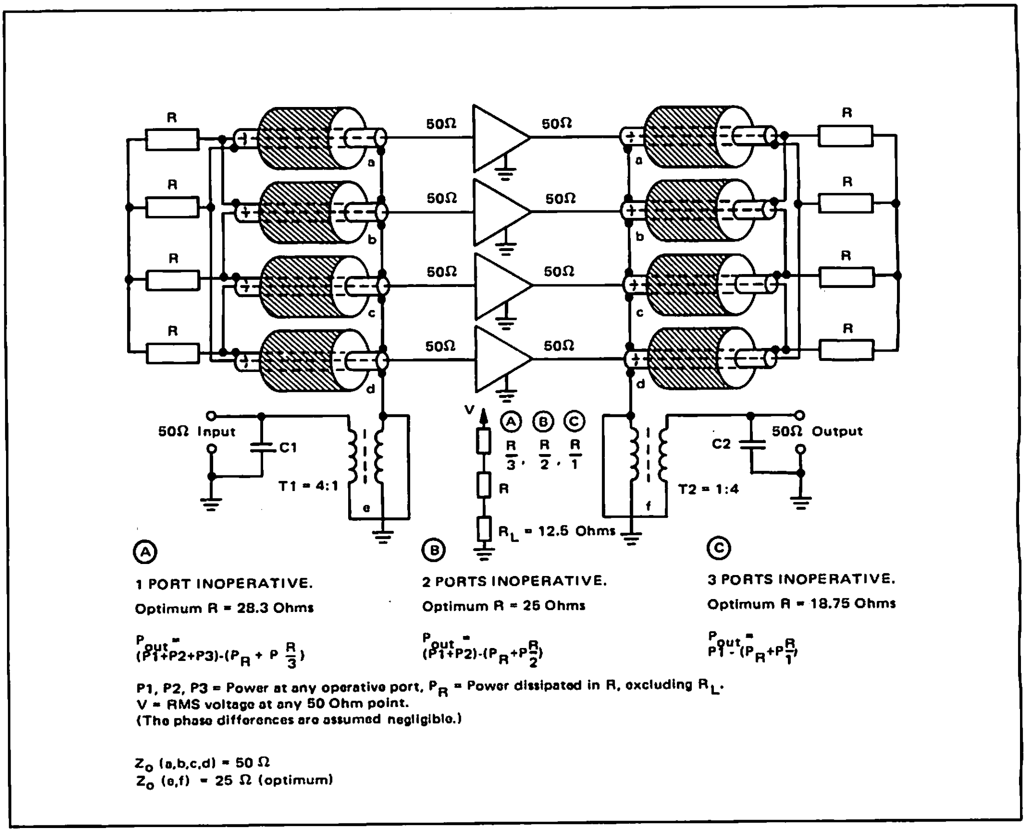

FIGURE 11 — Four-Port Hybrid System

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The isolation characteristics of the four-port output combiner were measured, the data being shown in Table 5. The ferrite sleeves are Stackpole 57-0572-27A, and the transmission lines are made of RG-142/U co-axial cable. The input power dividers described here, employ Stackpole 57-1511-24B ferrites, and the co-axial cable is Microdot 250-4012-0000.

TABLE 5 – Isolation Characteristics of Four Port Output Combiner

f (MHz)	Isolation, Port-to-Port (dB)
2.0	27.0-29.4
4.0	34.8-38.2
7.5	39.0-41.2
15	32.1-33.5
20	31.2-33.0
30	31.0-33.4

The input and output matching transformers (T1 – T2) will be somewhat difficult to implement for such impedance ratios as 2:1 and 3:1. One solution is a multi-turn toroid wound with co-axial cable, such as Microdot 260-4118-000. A tap can be made to the braid at any point, but since this is 25-Ohm cable, the Z_0 is optimum for a 4:1 impedance ratio only. Lower impedance ratios will normally require increased values for the leakage inductance compensation capacitances (C1 – C2). For power levels above 500-600 W, larger diameter co-axial cable is desirable, and it may be necessary to parallel two higher impedance cables. The required cross sectional area of the toroid can be calculated according to the B_{max} formulas presented in References 4 and 6.

The 2 to 30 MHz linear amplifier (shown in Figure 13) consists of two 300 W modules (8). This combined amplifier can deliver 600 W peak envelope power. The CW power output is limited to approximately 400 W by the heatsink and the output transformer design.

The power combiner (Figure 13A) and the 2:1 step-up transformer (Figure 13B) can be seen in the upper right corner. The input splitter is located behind the bracket (Figure 13C). The electrical configuration of the hybrids is shown in Figures 7A and 10. Note the loops equalizing the lengths of the co-axial cables in the input and output to assure a minimum phase difference between the two modules.

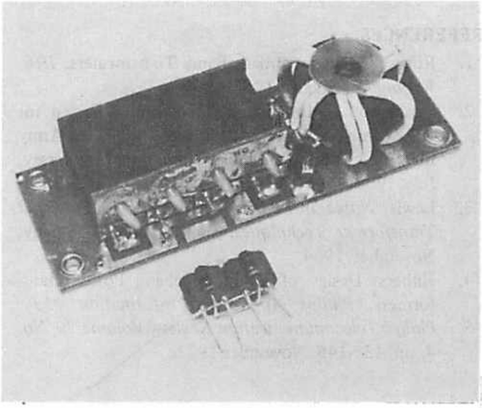

FIGURE 12 – Two-Four Port Hybrids

The one at the lower left is intended for power divider applications with levels to 20 – 30 W. The larger one was designed for amplifier output power combining, and can handle levels to 1 – 1.5 kW. (The balancing resistors are not shown with this unit.)

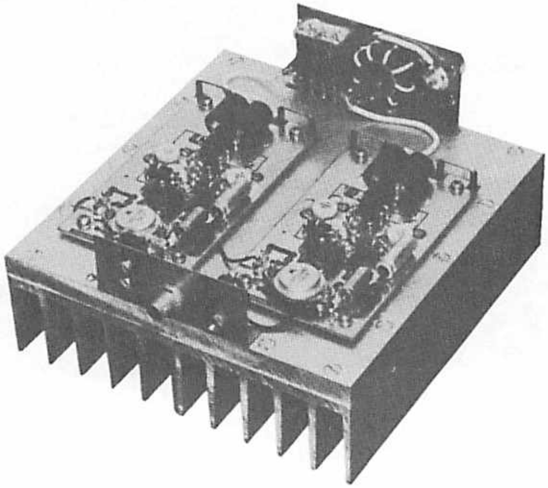

FIGURE 13 – 2 to 30 MHz Linear Amplifier Layout

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A TWO-STAGE 1 kW SOLID-STATE LINEAR AMPLIFIER

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INTRODUCTION

This application note discusses the design of 50 W and 300 W linear amplifiers for the 1.6 to 30 MHz frequency band. Both amplifiers employ push-pull design for low, even harmonic distortion. This harmonic distortion and the 50 Vdc supply voltage make the output impedance matching easier for 50-Ohm interface, and permits the use of efficient 1:1 and 4:1 broadband transformers.

Modern design includes integrated circuit bias regulators and the use of ceramic chip capacitors throughout the RF section, making the units easily mass producible.

Also, four 300 W modules are combined to provide a 1 to 1.2 kW PEP or CW output capability. The driver amplifier increases the total power gain of the system to approximately 34 dB.

Although the transistors employed (MRF427 and MRF428) are 100% tested against 30:1 load mismatches, in case of a slight unbalance, the total dissipation ratings may be well exceeded in a multi-device design. With high drive power available, and the power supply current limit set at much higher levels, it is always possible to have a failure in one of the push-pull modules under certain load mismatch conditions. It is recommended that some type of VSWR based protective circuitry be adapted in the equipment design, and separate dc regulators with appropriate current limits provided for each module.

The MRF428 is a single chip transistor with the die size of 0.140 x 0.248", and rated for a power output of 150 W PEP or CW. The single chip design eliminates the problem of selecting two matched die for balanced power distribution and dissipation. The high total power dissipation rating (320 W) has been achieved by decreasing the thermal resistance between the die and the mount by reducing the thickness of the BeO insulator to 0.04" from the standard 0.062", resulting in $R_{\theta JC}$ as low as $0.5^{\circ}C/W$.

The MRF427 is also a single chip device. Its die size is 0.118 x 0.066", and is rated at 25 W PEP or CW. This being a high voltage unit, the package is larger than normally seen with a transistor of this power level to prevent arcing between the package terminals.

The MRF427 and MRF428 are both emitter-ballasted, which insures an even current sharing between each cell, and thus improving the device ruggedness against load mismatches.

The recommended collector idling currents are 40 mA and 150 mA respectively. Both devices can be operated in Class A, although not specified in the data sheet, providing the power dissipation ratings are not exceeded.

GENERAL DESIGN CONSIDERATIONS

Similar circuit board layouts are employed for the four 300 W building block modules and the preamplifier. A compact design is achieved by using ceramic chip capacitors, of which most can be located on the lower side of the board. The lead lengths are also minimized resulting in smaller parasitic inductances and smaller variations from unit-to-unit.

Loops are provided in the collector current paths to allow monitoring of the individual collector currents with a clip-on current meter, such as the HP-428B. This is the easiest way to check the device balance in a push-pull circuit, and the balance between each module in a system such as this.

The power gain of each module should be within not more than 0.25 dB from each other, with a provision made for an input Pi attenuator to accommodate device pairs with larger gain spreads. The attenuators are not used in this device however, due to selection of eight closely matched devices.

In regards to the performance specifications, the following design goals were set:

Devices: 8 x MRF428 + 2 x MRF427A
Supply Voltage: 40 – 50 V
η, Worst Case: 45% on CW and 35% under two-tone conditions
IMD, d_3: -30 dB Maximum (1 kW PEP, 50 V and 800 W PEP, 40 V)
Power Gain, Total: 30 dB Minimum
Gain Variation: 2.0 – 30 MHz: ±1.5 dB Maximum
Input VSWR: 2.0:1 Maximum
Continuous CW Operation, 1 kW: 50% Duty Cycle, 30-minute periods, with heatsink temperature <75°C.
Load Mismatch Susceptibility: 10:1, any phase angle

Determining the figures above is based on previous performance data obtained in test circuits and broadband amplifiers. Some margin was left for losses and phase errors occurring in the power splitter and combiner.

THE BIAS VOLTAGE SOURCE

Figure 1 shows the bias voltage source employed with each of the 300 W modules and the preamplifier. Its basic components are the integrated circuit voltage regulator MC1723C, the current boost transistor Q3 and the temperature sensing diode D1.

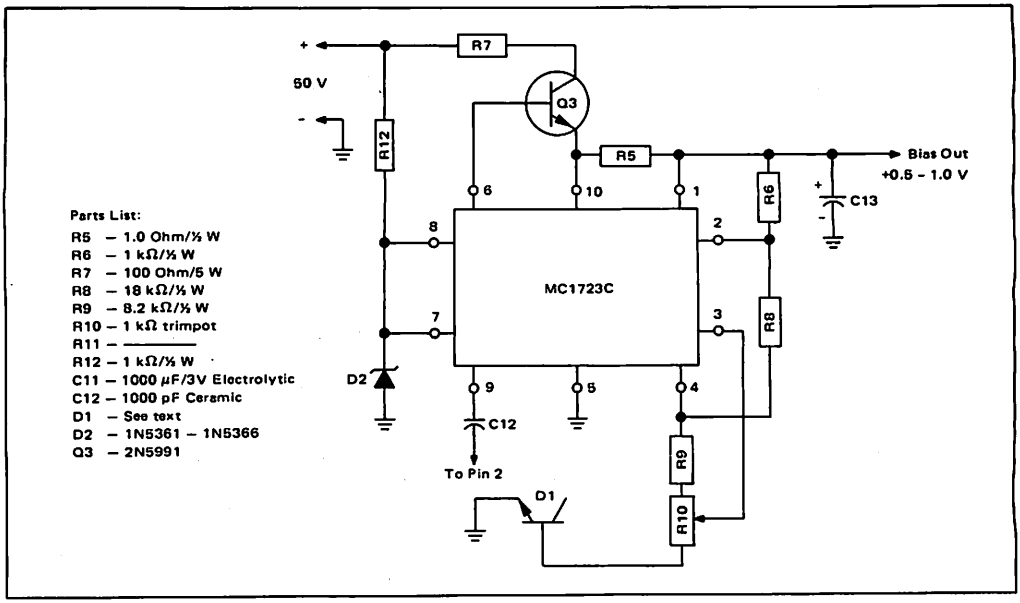

FIGURE 1 — Bias Voltage Source

Although the MC1723C is specified for a minimum V_O of 2 Volts, it can be used at lower levels with relaxed specifications, which are sufficient for this application. Advantages of this type bias source are:

1. Line voltage regulation, which is important if the amplifier is to be operated from various supply voltages.
2. Adjustable current limit.
3. Very low stand-by current drain.

Figure 1 is modified from the circuit shown on the MC1723 data sheet by adding the temperature sensing diode D1 and the voltage adjust element R10. D2 and R12 reduce the supply voltage to a level below 40 V, which is the maximum input voltage of the regulator.

D1 is the base-emitter junction of a 2N5190, in a Case 77 plastic package. The outline dimensions allow its use for one of the circuit board stand-offs, attaching it automatically to the heatsink for temperature tracking.

The temperature compensation has a slight negative coefficient. When the collector idling current is adjusted to 300 mA at 25°C, it will be reduced to 240 – 260 mA at a 60°C heatsink temperature. (-1.15 to -1.7 mA/C°.)

The current limiting resistor R5 sets the limiting to approximately 0.65 A, which is sufficient for devices with a minimum h_{FE} of 17, ($I_B = \frac{I_C}{h_{FE}}$) when the maximum average I_C is 10.9 A. (2 MHz, 50 V, 250 CW.) Typically, the MRF428 h_{FE}'s are in the 30's.

The measured output voltage variations of the bias source (0 – 600 mA) are ±5 to 7 mV, which amounts to a source impedance of approximately 20 milliohms.

THE 300 W AMPLIFIER MODULE

Input Matching

Due to the large emitter periphery of the MRF428, the series base impedance is as low as 0.88, -J.80 Ohm at 30 MHz. In a push-pull circuit a 16:1 input transformer would provide the best impedance match from a 50-Ohm source. This would however, result in a high VSWR at 2 MHz, and would make it difficult to implement the gain correction network design. For this reason a 9:1 transformer, which is more ideal at the lower frequencies, was chosen. This represents a 5.55 Ohm base-to-base soure impedance.

In a Class C push-pull circuit, where the conduction angle is less than 180°, the base-to-base impedance would be about four times the base-to-emitter impedance of one device. In Class A where the collector idling current is approximately half the peak collector current, the conduction angle is 360°, and the base-to-base impedance is twice the input impedance of one transistor. When the forward base bias is applied, the conduction angle increases and the base-to-base impedance decreases rapidly, approaching that of Class A in Class AB.

A center tap, common in push-pull circuits, is not necessary in the input transformer secondary, if the transistors are balanced. (C_{ib}, h_{FE}, V_{BEf}.) The base current return path is through the forward biased base-emitter

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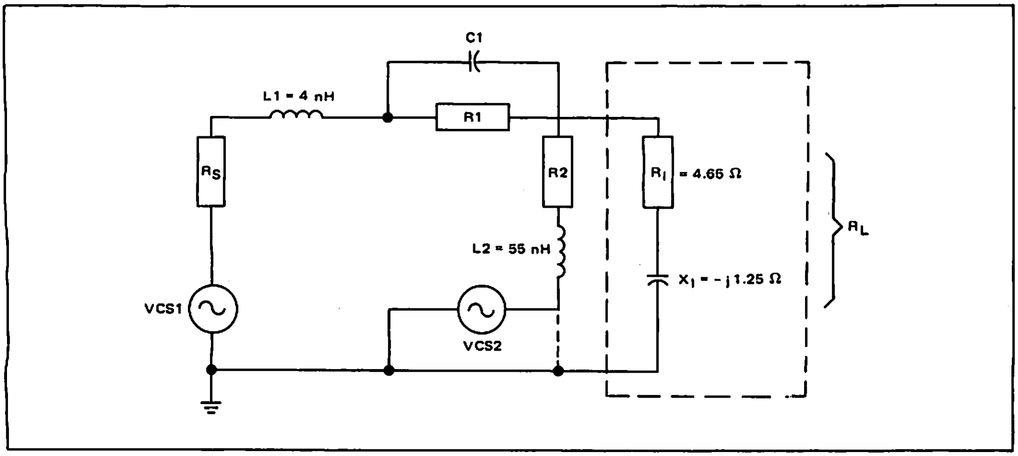

FIGURE 2 — Equivalent Base Input Circuit

junction of the off transistor. This junction acts as a *clamping diode*, and the power gain is somewhat dependent upon the amount of the bias current. The equivalent input circuit (Figure 2) represents one half of the push-pull circuit, and for calculations R_S equals the total source impedance (R_S') divided by two.

Since a junction transistor is a current amplifier, it should ideally be driven from a current source. In RF applications this would result in excessive loss of power gain. However, input networks can be designed with frequency slopes having some of the current source characteristics at low frequencies, where excess gain is available.

The complex base input characteristics of a transistor would place requirements for a very sophisticated input compensation network for optimum overall performance. The design goal here was to maintain an input VSWR of 2:1 or less and a maximum gain variation of ±1.5 dB from 2 to 30 MHz. Initial calculations indicated that these requirements can be met with a simple RC network in conjunction with negative collector-to-base feedback. Figure 2 shows this network for one device. L1 and L2 represent lead lengths, and their values are fixed. The feedback is provided through R2 and L2. Because the calculations were done without the feedback, this branch is grounded to simulate the operating conditions.

The average power gain variation of the MRF428 from 2 to 30 MHz is 13 dB. Due to phase errors, a large amount of negative feedback in an RF amplifier decreases the linearity, or may result in instabilities. Experience has shown that approximately 5 – 6 dB of feedback can be tolerated without noticeable effects in linearity or stability, depending upon circuit layout. If the amount of feedback is 5 dB, 8 dB will have to be absorbed by the input network at 2 MHz.

Omitting the reactive components, L1, L2, C1, and the phase angle of X_I which have a negligible effect at 2 MHz, a simple L-pad was calculated with $R_S = 2.77\ \Omega$, and $R_L = \sqrt{4.65^2 + 1.25^2} = 4.81\ \Omega$.

From the device data sheet we find the G_{PE} at 2 MHz is about 28 dB, indicating 0.24 W at R_L will produce an output power of 150 W, and the required power at R_S = 0.24 W + 8 dB = 1.51 W.

Figuring out currents and voltages in various branches, results in: R1 = 1.67 Ω and R2 = 1.44 Ω.

The calculated values of R1 and R2 along with other known values and the device input data at four frequencies were used to simulate the network in a computer program. An estimated arbitrary value of 4000 pF for C1 was chosen, and VCS2 represents the negative feedback voltage (Figure 2.) The optimization was done in two separate programs for R1, R2, C1 and VCS2 and in several steps. The goals were: a) VCS and R2 for a transducer loss of 13 dB at 2 MHz and minimum loss at 30 MHz. b) R1 and C1 for input VSWR of <1.1:1 and <2:1 respectively. The optimized values were obtained as:

C1 = 5850 pF	R2 = 1.3 Ω
R1 = 2.1 Ω	VCS2 = 1.5 V

The minimum obtainable transducer loss at 30 MHz was 2.3 dB, which is partly caused by the highest reflected power at this frequency, and can be reduced by "over-compensation" of the input transformer. This indicates that at the higher frequencies, the source impedance (R_S) is effectively decreased, which leaves the input VSWR highest at 15 MHz.

In the practical circuit the value of C1 (and C2) was rounded to the nearest standard, or 5600 pF. For each half cycle of operation R2 and R4 are in series and the value of each should be $\frac{1.3\ \Omega}{2}$ for VCS2 = 1.5 V. Since the voltage across ac and bd = V_{CE}, a turns ratio of 32:1 would be required. It appears that if the feedback voltage

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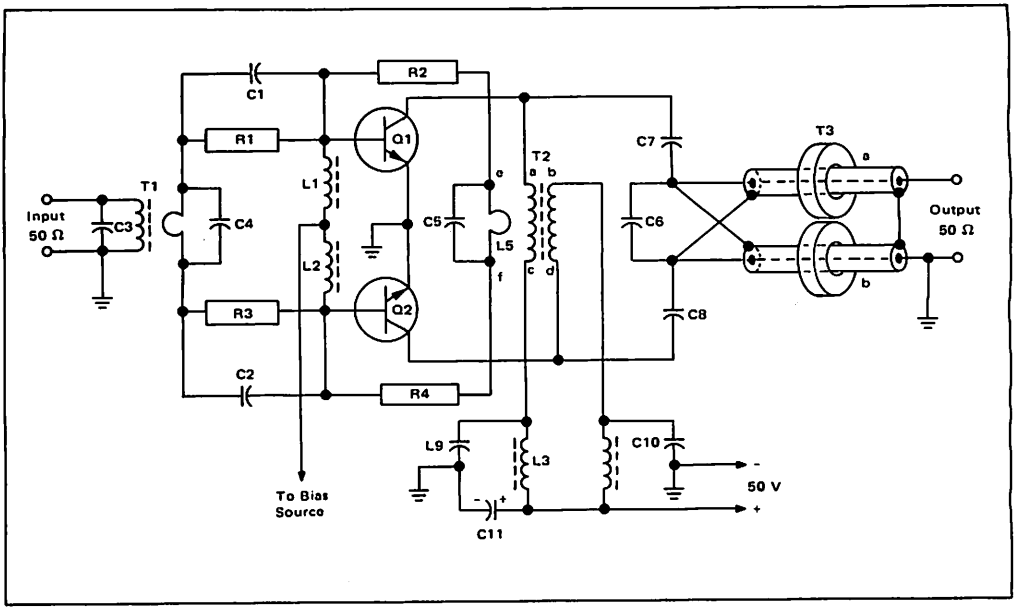


FIGURE 3 –

on the bases remains unchanged, the ratio of the voltage across L5 (VCS2) and R2R4 can be varied with only a small effect to the overall input VSWR. To minimize the resistive losses in the bifilar winding of T2 (Figure 3), the highest practical turns ratio should not be much higher than required for the minimum inductance, which is

$$\frac{4R}{2\pi f} = \frac{50}{12.5} = 4.0\ \mu\text{H}.$$

R = Collector-to-Collector Impedance = 12.5 Ω

f = 2 MHz

ac or bd will then be 1.0 μH, which amounts to 5 turns. (See details on T2.) 25% over this represents a 7:1 ratio setting VCS2 to 6.9 V.

In addition to providing a source for the negative feedback, T2 supplies the dc voltage to the collectors as well as functions as a center tap for the output transformer T3.

The currents for each half cycle are in opposite phase in ac and bd, and depending on the coupling factor between the windings, the even harmonic components will see a much lower impedance than the fundamental. The optimum line impedance for ac, bd would equal one half the collector-to-collector impedance, but experiments have shown that increasing this number by a factor of 2-3 affects the 2nd and 4th harmonic amplitudes by only 1 to 2 dB.

Since the minimum gain loss obtainable at 30 MHz with network as in Figure 2, and the modified VCS2 source was about 3.8 dB at 30 MHz, C5 was added with the following in mind: C5 and L5 form a parallel resonant circuit with a Q of approximately 1.5. Its purpose is to increase the shunting impedance across the bases, and to disturb the 180° phase difference between the input signal and the feedback voltage at the higher frequencies. This reduces the gain loss of 3.8 dB, of which 1.4 dB is caused by the feedback at 30 MHz. The amount depends upon the resonant frequency of C5 L5, which should be above the highest operating frequency, to avoid possible instabilities.

When L5 is 45 nH, and the resonance is calculated for 35 MHz, the value of C5 becomes 460 pF, which can be rounded to the closest standard, or 470 pF. The phase shift at 30 MHz is:

$$\text{Tan}^{-1}\left[\frac{2\pi f L}{R\left(1-\dfrac{f^2}{f_o^2}\right)}\right] = \text{Tan}^{-1}\left[\frac{6.28 \times 30 \times 0.045}{6.8\left(1-\dfrac{900}{1225}\right)}\right]$$

$$= \text{Tan}^{-1}\left(\frac{8.48}{1.80}\right) = 78.0^\circ$$

The impedance is: $\dfrac{R}{\cos\theta} = \dfrac{6.8}{\cos 78^\circ} = 32.7\ \Omega$

At 2 MHz the numbers are respectively 4.76° and 6.83 Ω.

The 1.4 dB feedback means that the feedback voltage is 16% of the input voltage at the bases. By the aid of vectors, we can calculate that the 78° phase shift and the increased impedance reduces this to 4%, which amounts to 0.35 dB. These numbers were verified in another computer program with VCS2 = 6.9 V, and including C5. New values for R1 and R2 were obtained as 1.95 Ω and 6.8 Ω respectively, and other data as shown in Table 1.

The VSWR was calculated as

$$\frac{Z1 - Z2}{Z1 + Z2} \quad \text{where:}$$

Z1 = Impedance at transformer secondary.

TABLE1:

Frequency MHz	Input VSWR	Input Impedance Real	Input Impedance Reactive	Attenuation dB
2.0	1.07	2.79	-0.201	13.00
4.0	1.16	2.66	-0.393	12.07
7.5	1.33	2.35	-0.615	10.42
15	1.68	1.77	-0.611	7.40
20	1.82	1.57	-0.431	5.90
30	1.74	1.62	-0.21	2.70

Although omitted from the preliminary calculations, the 2 x 5 nH inductances, comprising of lead length, were included in this program.

The input transformer is a 9:1 type, and uses a television antenna balun type ferrite core, made of high permeability material. The low impedance winding consists of one turn of 1/8" copper braid. The sections going through the openings in the ferrite core are rounded to resemble two pieces of tubing electrically. The primary consists of AWG #22 TFE insulated wire, threaded through the rounded sections of braid, placing the primary and secondary leads in opposite ends of the core. (4) (5). The saturation flux density is about 60 gauss which is well below the limits for this core. For calculation procedures, see discussion about the output transformer.

This type physical arrangement provides a tight coupling, reducing the amount of leakage flux at high frequencies. The wire gauge, insulation thickness, and number of strands have a minimal effect in the performance except at very high impedance ratios, such as 25:1 and up. The transformer configuration is shown in Figure 4. By using a vector impedance meter, the values for C3 and C4 were measured to give a reasonable input match at 30 MHz, (Z_{in} = 1.62 - j 0.21 x 2 = 3.24 - j 0.42) with the smallest possible phase angle.

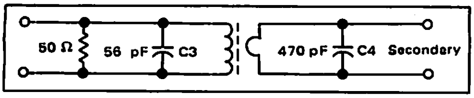


FIGURE 4 — Transformer Configuration

When the high impedance side was terminated into 50 Ω, the following readings were obtained at the secondary:

Z2 = Input impedance of compensation network x 2 (R_S in Figures 2 and 3) as in computer data presented ahead.

The effect of the lower VSWR to the power loss in the input network can be calculated as follows:

$$10 \text{ Log} \left[\frac{\left(1 - \left(\frac{S1 - 1}{S1 + 1}\right)^2\right)}{\left(1 - \left(\frac{S2 - 1}{S2 + 1}\right)^2\right)} \right]$$

where:
S1 = VSWR 1 (Lower)
S2 = VSWR 2 (Higher)

$$\text{which at 30 MHz} = 10 \text{ Log} \frac{\left(1 - \left(\frac{1.11 - 1}{1.11 + 1}\right)^2\right)}{\left(1 - \left(\frac{1.74 - 1}{1.74 + 1}\right)^2\right)}$$

$$= 10 \text{ Log} \left(\frac{0.997}{0.927}\right) = 0.32 \text{ dB}, 2.7 - 0.32 = 2.38 \text{ dB}$$

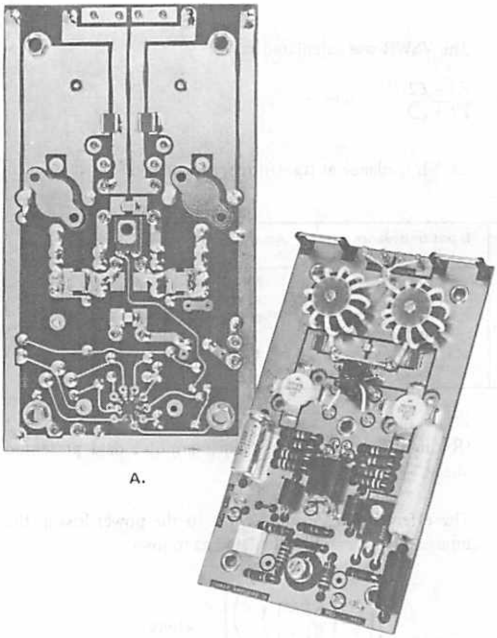
These figures for other frequencies are presented with the data below. Later, some practical experiments were done with moving the resonance of C5 L5 lower, to find out if instabilities would occur in a practical circuit. When the resonance was equal to the test frequency, slight break-up was noticed in the peaks of a two-tone pattern. It was then decided to adjust the resonance to 31 MHz, where C5 = 560 pF, and the phase angle at 30 MHz increases to 87°. The transducer loss is further reduced by about 0.2 dB.

Several types of output transformer configurations were considered. The 12.5 Ω collector-to-collector im-

TABLE 2:

Frequency MHz	R_S Ohms	X_S Ohms	VSWR	Attenuation dB
2.0	5.59	+0.095	1.05	12.99
4.0	5.55	+0.057	1.15	12.06
7.5	5.50	+0.046	1.32	10.40
15	4.90	+0.25	1.48	7.28
20	4.32	+0.55	1.38	5.63
30	3.43	+0.73	1.11	2.38

(Above readings with transformer and compensation network.)



A.

B.

FIGURE 5 – Bottom and Top of the 300 W Module Circuit Board

pedance estimated earlier, would require a 4:1 transformer for a 50 Ω output. The type used here as the input transformer exhibits good broad band characteristics with a convenient physical design. However, according to the low frequency minimum inductance formula presented earlier in connection with T2, the initial permeability required would be nearly 3000, with the largest standard core size available. High permeability ferrites are almost exclusively of Nickel-Manganese composition, and are lossy at radio frequencies. Although their Curie points are higher than those of lower permeability Nickel-Zinc ferrites, the core losses would degrade the amplifier performance. With the core losses being a function of the power level, these rules can sometimes be disregarded in low power applications.

A coaxial cable version was adapted for this design, since the transmission line type transformers are theoretically ideal for RF applications, especially in the 1:4 impedance ratio. A balanced to unbalanced function would normally require three separate transmission lines including a balun (5) (6). It appears that the third line can be omitted, if lines a and b (Figure 3) are wound on separate magnetic cores, and the physical length of the lines is sufficient to provide the necessary isolation between the collectors and the load. In accordance to formulas in (7), the minimum line length required at 2 MHz, employing Stackpole 57-9074 or equivalent ferrite toroids is 4.2", and the maximum permissible line length at 30 MHz would be approximately 20". The 4.2" amounts to four turns on the toroid, and measures 1.0 μH, which in series with the second line is sufficient for 2 MHz. Increasing the minimum required line length by a factor of 4 is still within the calculated limits, and in practical measurements the isolation has been found to be over 30 dB across the band. The main advantage with this arrangement is a simplified electrical and physical lay-out.

The maximum flux density of the toroids is approximately 200 gauss (3), and the number of turns has been increased beyond the point where the flux density of the magnetic core is the power limiting factor.

The 1:4 output transformer is not the optimum in this case, but it is the closest practical at these power levels. The optimum power output at 50 V supply voltage and 50 Ω load is:

$$V_{RMS} = 4 \times (V_{CC} - V_{CE(sat)} \times 0.707) = 135.75\text{ V, when } V_{CE(sat)} = 2\text{ V}$$

$$I = \frac{135.75}{50} = 2.715\text{ A}, P_{out} = 2.715 \times 135.75 = 368.5\text{ W}$$

The optimum V_{CC} at P_{out} = 300 W would be:

$$V_{CC} = V_{CE(sat)} + (\sqrt{R_{in} \times 2\,P_{out}}) = 2 + (\sqrt{6.25 \times 300}) = 45.3\text{ V}$$

The above indicates that the amplifier sees a lower load line, and the collector efficiency will be lowered by 1-2%. The linearity at high power levels is not affected, if the device h_{FE} is maintained at the increased collector currents. The linearity at low power levels may be slightly decreased due to the larger mismatch of the output circuit.

The required characteristic line impedance (a and b, Figure 3) for a 1:4 impedance transformer is: $\sqrt{R_{in}\,R_L} = \sqrt{12.5 \times 50} = 25\ \Omega$, enables the use of standard miniature 25 Ω coaxial cable (i.e., Microdot 260-4118-000) for the transmission lines. The losses in this particular cable at 30 MHz are 0.03 dB/ft. With a total line length of 2 x 16.8" (2 x 4 x 4.2"), the loss becomes 0.084 dB, or

$$300 - \left(\frac{300}{10\ \text{antilog}\ 0.084\ \text{dB}}\right) = 5.74\text{ W}.$$

For the ferrite material employed, Stackpole grade #11 (or equivalent Indiana General Q1) the manufacturers data is insufficient for accurate core loss calculations (6). The B_H curves indicate that 100-150 gauss is well in the linear region.

The toroids measure 0.87" x 0.54" x 0.25", and the 16.8" line length figured above, totals to 16 turns if tightly wound, or 12-14 turns if loosely wound. The flux density can then be calculated as:

$$B_{max} = \frac{V_{max} \times 10^2}{2\,\pi\,f\,n\,A}$$

where: f = Frequency in MHz
n = Total number of turns.
A = Cross sectional area of the toroid in cm^2.
V = Peak voltage across the 50 Ω load,

$$\sqrt{\left(\frac{300}{50}\right)}\left(\frac{50}{0.707}\right) = 173\text{ V}$$

$$B_{max}\ (\text{for each toroid}) = \frac{86.5 \times 10^2}{6.28 \times 2 \times 28 \times .25} = 98.3\text{ gauss}$$

Practical measurements showed the core losses to be negligible compared to the line losses at 2 MHz and 30 MHz. However, the losses increase as the square of B_{max} at low frequencies.

With the amount of HF compensation dependent upon circuit layout and the exact transformer construction, no calculations were made on this aspect for the input (or output) transformers. C3, C4, and C6 were selected by employing adjustable capacitors on a prototype whose values were then measured.

A photo of the circuit board is shown in Figure 5, A-bottom and B-top. The performance data of the 300 W module can be seen in Figure 6.

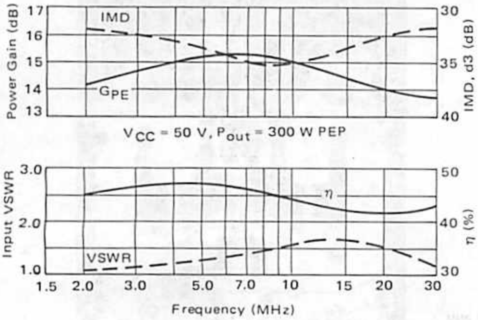


FIGURE 6 – IMD, Power Gain, Input VSWR and Efficiency versus Frequency of a 300 W Module

THE DRIVER AMPLIFIER

The driver uses a pair of MRF427 devices, and the same circuit board layout as the power amplifier, with the exception of the type of the output transformer.

The input transformer is equal to what is used with the power amplifier, but has a 4:1 impedance ratio. The required minimum inductance in the one turn secondary (Figures 3 and 4) being considerably higher in this case,

$$\frac{4R}{2\pi f} = \frac{4 \times 12.5}{12.5} = 4\ \mu H$$

the A_L product of the core is barely sufficient. The measured inductances between a number of cores range 3.8 - 4.1 μH.

This formula also applies to the output transformer, which is a 1:1 balun. The required minimum inductance at 2 MHz is 16 μH, amounting to 11 turns on a Ferroxcube 2616P-A100-4C4 pot core, which was preferred over a toroid because of ease of mounting and other physical features. Although twisted wire line would be good at this power level, the transformer was wound with RG-196 coaxial cable, which is also used later for module-driver interconnections.

The required worst case driver output is 4 x 12 W = 48 W. The optimum P_{out} with the 1:1 output transformer is

$$\frac{V_{RMS}}{50} \times V_{RMS} = \frac{67.7}{50} \times 67.7 = 92\ W.$$

The MRF 427 is specified for a 25 W power output. Having a good h_{FE} versus I_C linearity, the 1 to 2 load mismatch has an effect of 2-3 dB in the IMD at the 10% power level, and the reduced efficiency in the driver is insignificant regarding the total supply current in the system.

The component values for the base input network and the feedback were established with the aid of a computer, and information on the device data sheet, as described earlier with the 300 W module. The HF compensation was done in a similar manner as well. Neither amplifier employs LF compensation. C7 and C8 are dc blocking capacitors, and their value is not critical.

In T2 (Figure 7), b and c represent the RF center tap, but are separated in both designs – partly because of circuit lay-out convenience and partly for stabilization purposes.

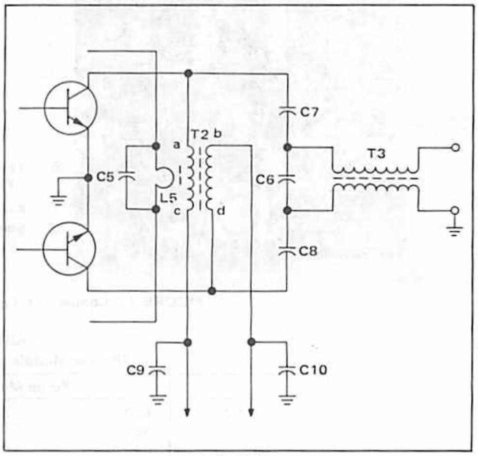


FIGURE 7

The test data of the driver is presented later along with the final test results.

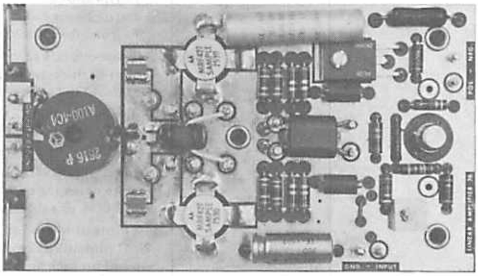


FIGURE 8 – Driver Amplifier Board Layout

COMBINING FOUR 300 W POWER MODULES

The Input Power Divider

The purpose of the power divider is to divide the input power into four equal sources, providing an amount of isolation between each. The outputs are designed for 50 Ω impedance, which sets the common input at 12.5 Ω. This requires an additional 4:1 step down transformer to provide a 50 Ω load for the driver amplifier. Another requirement is a 0° phase shift between the input and the 50 Ω outputs, which can be accomplished with 1:1 balun transformers. (a, b, c and d in Figure 10.) For im-

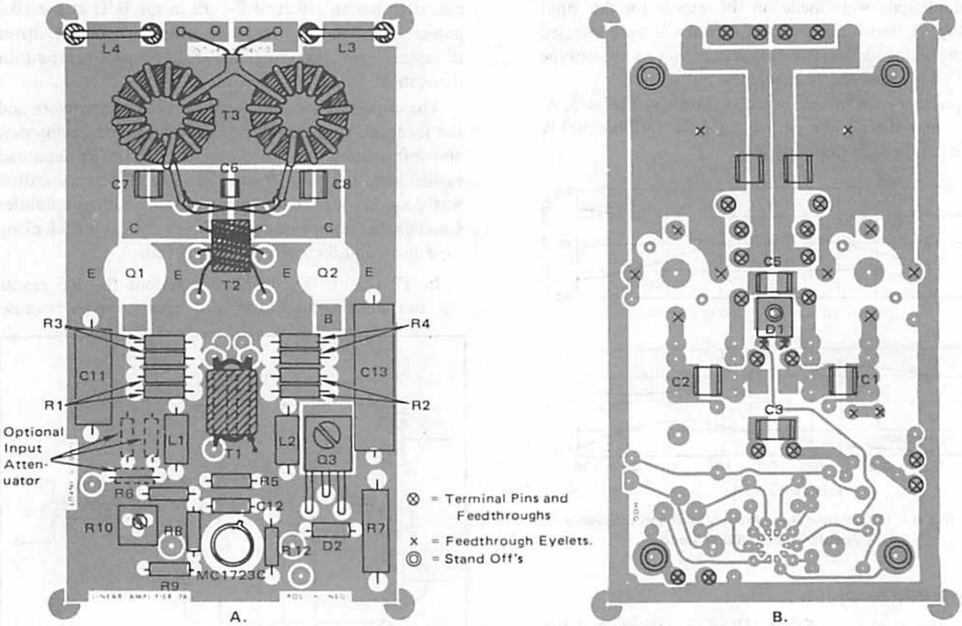


FIGURE 9 – Component Layout of the 300 W Amplifier Module

PARTS LIST*
(Power Module and Driver Amplifier)

	Power Module	Driver Amplifier
C1, C2	5600 pF	3300 pF
C3	56 pF	39 pF
C4	470 pF	Not Used
C5	560 pF	470 pF
C6	75 pF	51 pF
C7, C8	0.1 μF	0.1 μF
C9, C10	0.33 μF	0.33 μF
C11	10 μF/150 V	10 μF/150 V
R1, R2	2 x 3.9 Ω/½ W in parallel	2 x 7.5 Ω/½ W in parallel
R3, R4	2 x 6.8 Ω/½ W in parallel	2 x 18 Ω/½ W in parallel
L1, L2	Ferroxcube VK200 19/4B ferrite choke	Ferroxcube VK 200 19/4B ferrite choke
L3, L4	6 ferrite beads each, Ferroxcube 56 590 65/3B	6 ferrite beads each, Ferroxcube 56 590 65/3B
	All capacitors, except C11, are ceramic chips. Values over 100 pF are Union Carbide type 1225 or 1813 or Varadyne size 18 or 14. Others ATC Type B.	
T1	9:1 type, see text. (Ferrite cores for both: Stackpole 57-1845-24B or Fair-Rite Products 287300201 or equivalent.)	4:1 type, see text.
T2	7 turns of bifilar or loosely twisted wires. (AWG #20.) Ferrite cores for both: Stackpole 57-9322, Indiana General F627-8Q1 or equivalent.	
T3	14 turns of Microdot 260-4118-00 25 Ω miniature coaxial cable wound on each toroid. (Stackpole 57-9074, Indiana General F624-19Q1 or equivalent.)	11 turns of RG-196, 50 Ω miniature coaxial cable wound on a bobbin of a Ferroxcube 2616P-A100-4C4 pot core.

*Parts & kits for this amplifier are available from Communication Concepts, 121 Brown St., Dayton, Ohio 45402 (513) 220-9677 proved low frequency isolation characteristics the line impedance must be increased for the parallel currents. This can be done, without affecting the physical length of the line, by loading the line with magnetic material. In this type transformer, the currents cancel, making it possible to employ high permeability ferrite and a relatively short physical length for the transmission lines. In an absolutely balanced condition, no power will be dissipated in the magnetic cores, and the line losses are reduced. The minimum required inductance for each line can be calculated as shown for the driver amplifier output transformer, which gives a number of 16 μH minimum at 2 MHz. A low inductance value degrades the isolation characteristics between the 50 Ω output ports, to maintain a low VSWR in case of a change in the input impedance of one or more of the power modules. However, because of the base compensation networks, the power splitter will never be subjected to a completely open or shorted load.

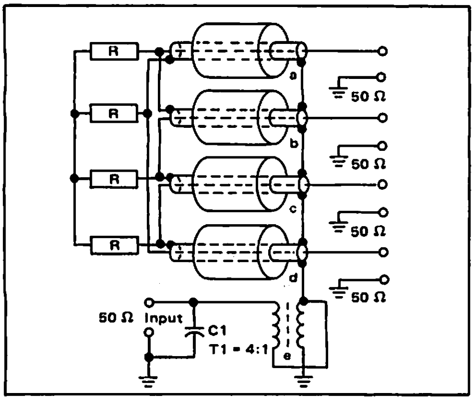


FIGURE 10 — Four Port Power Divider

The purpose of the balancing resistors (R) is to dissipate any excess power, if the VSWR increases. Their optimum values, which are equal, are determined by the number of 50 Ω sources assumed unbalanced at one time, and the resistor values are calculated accordingly.

Examining the currents with one load open, it can be seen that the excess power is dissipated in one resistor in series with three parallel resistors. Their total value is 50 - 12.5 = 37.5 Ω. Similarly, if two loads are open, the current flows through one resistor in series with two parallel resistors, totaling 37.5 Ω again. This situation is illustrated in Figure 11.

Except for a two port power divider [5], the resistor values can be calculated for odd or even number systems as:

$$R = \left(\frac{R_L - R_{in}}{n+1}\right) n \quad \text{where:}$$

R_L = Impedance of the output ports, 50 Ω.
R_{in} = Impedance of the input port, 12.5 Ω.
n = Number of output ports properly terminated.

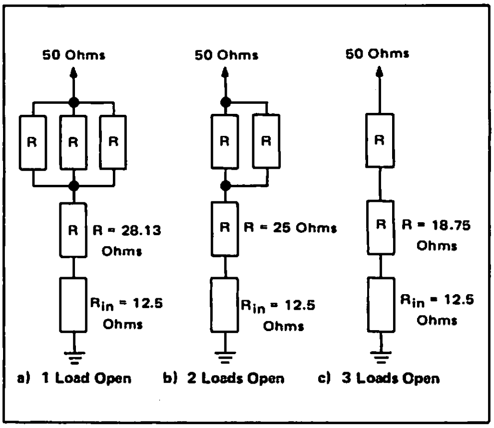


FIGURE 11

Although these resistor values are not critical in the input divider, the formula also applies to the output power combiner, where mismatches have a larger effect in the total power output and linearity.

The practical power divider employs large ferrite beads (Fair-Rite Products 2673000801 or Stackpole 57-1511-24B or equivalent) over a 1.2 inch piece of RG-196 coaxial cable. The arrangement is shown in Figure 10. Both above ferrite materials have a μr of about 2500, and the inductance for one turn is in excess of 10 μH.

The step-down transformer (T1, Figure 10) is wound on a Stackpole 57-9322-11 toroid with 25 Ω miniature coaxial cable. (Microdot 260-4118-000 or equivalent.) Seven turns will give a minimum inductance of 4/16 μH, required at 2 MHz.

For the preamplifier interface, C1 could be omitted in order to achieve the lowest input VSWR.

The structure is mounted between two phenolic terminal strips as can be seen in the foreground of Figure 14, providing a sufficient number of tie points for the coaxial cable connections.

THE OUTPUT COMBINER

The operation of the output combiner is reversed from that of the input power divider. In this application we have four -50 Ω inputs and one 12.5 Ω output, which is transformed to 50 Ω by a 1:4 impedance ratio transformer.

An arrangement similar to the input power divider is employed in the combiner. The baluns consist of straight pieces of coaxial cable loaded by a sleeve of magnetic material (ferrite). The line length is determined by the physical dimensions of the ferrite sleeves. The μr versus cross sectional area should be calculated or measured to give sufficient loading inductance.

Straight line baluns as these have the advantage over multiturn toroidal types in introducing a smaller possibility for phase errors, due to the smaller length of the line. The largest possible phase errors occur in the input and output connecting cables, whose lengths are 18" and 10" respectively. All four input and output cables must be of equal length within approximately ¼", and the excess in some, caused by the asymmetrical system layout, can be coiled or formed into loops.

The output connecting cables between the power amplifier outputs and the combiner are made of low loss RG-142B/U coaxial cable, that can adequately handle the 300 W power with the average current of 2.45 A.

The balun transmission lines are also made of RG-142B/U coaxial cable, with an outer diameter of 0.20". The line length is not critical as it is well below the maximum length permitted for 30 MHz (7). The minimum inductance, as in the input divider, is 16 μH per line. Measurements were made between two port combiners, one having the line inductance of 17 μH (7 Ferroxcube 768 series 3E2A toroids) and the other 4.2 μH (one Stackpole 57-0572-27A ferrite sleeve). The results are shown in Table 3.

The power output with various numbers of disabled sources, referring to Figures 11 and 12 can be calculated as:

$$P_n - P_R + \frac{P_R}{n}$$

where: n = Number of Operative Sources.
P_n = Total Power of Operative Sources.
P_R = Power Dissipated in Balancing Resistors.

For one disabled source:

$$P_R = 250\left(\frac{28.13}{50}\right) = 140.65,$$

$$P_{out} = (250 \times 3) - \left(140.65 + \frac{140.65}{3}\right) =$$

$$750 - 187.5 = 562.5 \text{ W}$$

This is assuming that the phase errors between the active sources are negligible. Otherwise the formula in (7) can

f MHz	Isolation dB (Line Inductance 17 μH)	Isolation dB Line Inductance 4.2 μH)
2.0	40.2	29.1
4.0	40.0	38.3
7.5	39.6	39.1
15	37.5	37.8
20	35.8	36.2
30	33.4	33.5

TABLE 3:

The main difference is at 2 MHz – and it was decided that the 29 dB of isolation is sufficient, as the high frequency isolation in either case is not much better. The 3E2A and other similar materials are rather lossy at RF, and with their low Curie points, would present a danger of overheating in case of a source unbalance.

Figure 12 shows the electrical design of the four-port power combiner.

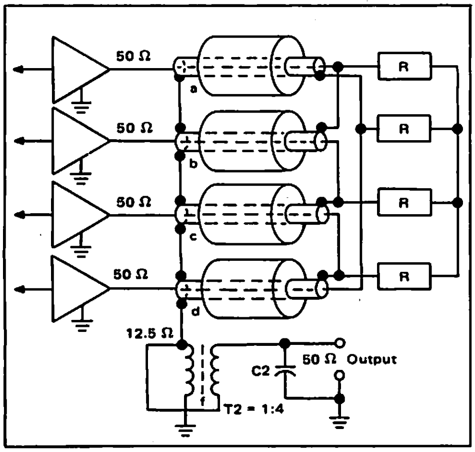


FIGURE 12 – Four Port Output Combiner

be adapted, but if the errors between the active sources are unequal, the situation will get rather complex.

From above we see that 140.65 W will be dissipated by one of the balancing resistors and only 15.6 W by the other three. For this high power dissipation the resistors must be the type which can be mounted to a heat sink, and noninductive. After experiments with the "noninductive" wirewound resistors which exhibited excess inductance at 30 MHz and were bulky with 50 and 100 W ratings, thin film terminations were specially fabricated in-house for this application.* These terminations are deposited on a BeO wafer, which is attached to a copper flange. They are rated for 50 W continuous power, but can be operated at 100 or even 150 W for nonextended periods if the flange temperature is kept moderately low. The balancing resistors can be seen on the upper side of the combiner, which is shown in the foreground of Figure 15.

The purpose of the step-up transformer T2, (Figure 12) is to transform the 12.5 Ω impedance from the combiner up to 50 Ω. It is a standard 1:4 unbalanced-to-unbalanced transmission line type transformer, (6, 7, 8) in which the line is made of two RG-188 coaxial cables connected in parallel in the manner as shown in Figure 13.

Normally the loss in RG-188 at 30 MHz is 0.08 dB/foot. In this connection arrangement, the currents in both directions are carried by the braid in parallel with the

*Similar attenuators and terminations are available from Solitron, EMC Technology, Inc., and other manufacturers of microwave components.

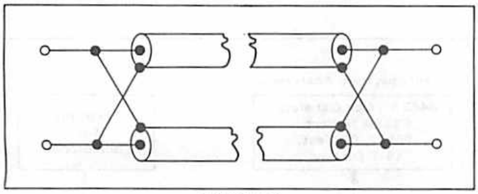


FIGURE 13

inner conductor and the power loss is reduced to approximately 0.025 dB/foot. The impedance becomes 25 Ω, and depending on how close the cables are to each other physically, it can be as low as 22 Ω. The minimum line inductance can be calculated as shown before, and is 16 μH for the 50 Ω side. This inductance is achieved by winding several turns of the dual cable line on a magnetic core. In contrast to the balun transformers in the combiner, the line currents do not cancel and the magnetic core must handle the full power, and must be made of lower loss material. The form of a toroid was figured to require the shortest line length for a specific inductance, and out of the standard sizes, two stacked units resulted in a shorter line length than a single larger one with similar cross sectional area.

Six turns on two Indiana General F626-12-Q1 toroids give 4.8 and 23 μH for the secondary; the line length being 16 inches.

In continuous operation the core temperature was measured as 95-90°C. This resulted in a decision to change the core material to Q2, which exhibits about 70% lower losses at 30 MHz. The permeability is also lower (35), and with the same number of turns gives only 13 μH.

The line length could not be increased according to (7), and the measurements indicated no difference in operation at 2 MHz, so the Q2 toroids with the low inductance were considered permanent.

The maximum flux density of the toroids is calculated as shown before:

$$B_{max} = \frac{V_{max} \times 10^2}{2\pi f \eta A} \text{ gauss, where:}$$

V = Peak voltage across the secondary, (50 point) 316.2 V
f = Frequency in MHz (2.0)
η = Number of turns at the 50 Ω point. (12)
A = Core cross sectional area (1.21 cm²)

$$B_{max} = \frac{316.2 \times 10^2}{6.28 \times 2 \times 12 \times 1.21} = 260 \text{ gauss}$$

From the BH curves we can see that the linear portion extends to 800-1000 gauss, and the saturation occurs at over 3000 gauss. Comparable materials are Stackpole grade 14 and Fair-rite products 63.

The core losses are minimal compared to the line losses, which for the 16" length amount to 0.035 dB or 0.81%.

As in the input transformer, the HF compensation (C2) was not required. The lay-out of the combiner and T2 is

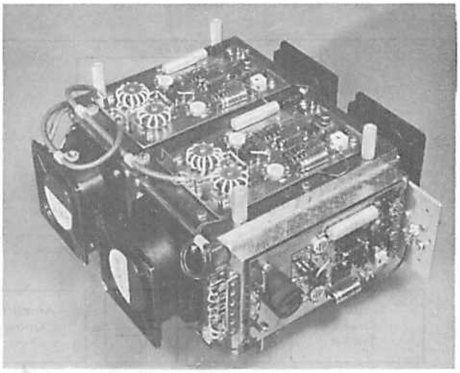


FIGURE 14 – 1 kW Linear Amplifier showing the input power divider in the foreground, to the right is the preamplifier. Two of the four 300 W modules can be seen on the upper side of the structure. The other two modules are shown in Figure 15.

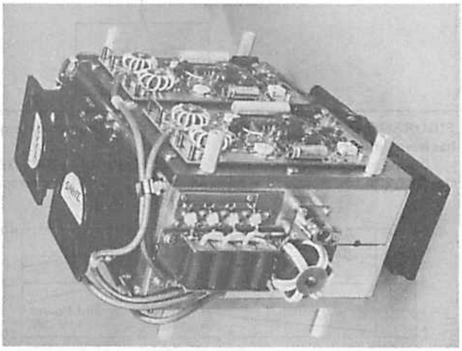


FIGURE 15 – 1 kW Linear Amplifier showing the output combiner in the foreground, to the right is the 1:4 stepup transformer. The four balancing resistors, mounted to the heat sink, can be seen directly above the combining network.

such that minimum lead lengths are obtained, and the structure is mounted on a PC board having feedthrough eyelets to a continuous ground plane on its lower side.

MEASUREMENTS

Six 300 W modules were built using matched pair production MRF428's. The maximum gain distribution was 0.9 dB, and in the four units selected for the amplifier, the gain varied from 13.7 to 14.1 dB at 30 MHz, so it was not necessary to utilize the option of the input attenuators.

Figure 16 shows the test set-up arrangement employed for testing the modules and the combined amplifier.

The heatsink design was not optimized as it was felt to be outside the scope of this report; concentration was made in the electrical design. However, it was calculated to be sufficient for short period testing under two-tone or CW conditions at full power. The heatsink consists of

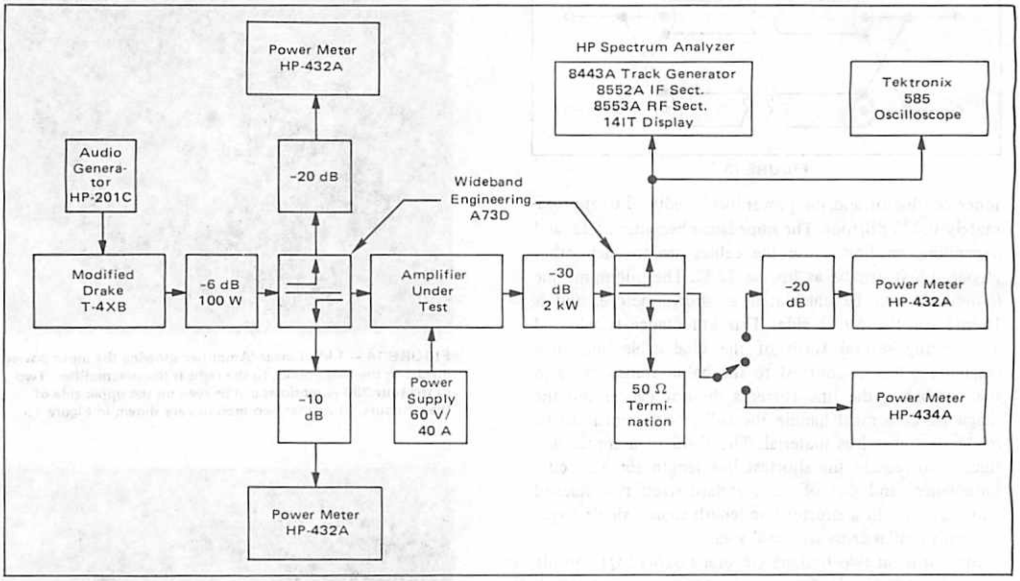


FIGURE 16 — For two tone operation, a signal from an external audio oscillator is added to a signal from the T-4XB built-in oscillator, which has been adjusted to 800 Hz.

During single tone testing, the external oscillator (1200 Hz) is switched off. A calorimeter wattmeter in the output can be used to calibrate the HP-432A's at frequencies below ≈10 MHz, where their response roll-off begins.

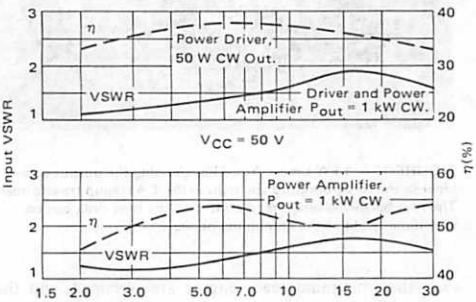


FIGURE 17 — VSWR and Efficiency versus Frequency

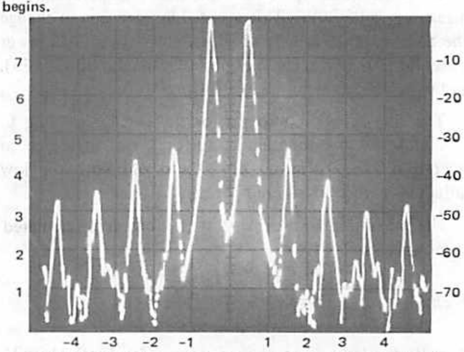


FIGURE 19 — Photo of Spectrum Analyzer Display Showing the IMD Products to the 9th Order. Power Output = 1 kW at 30 MHz (50 V).

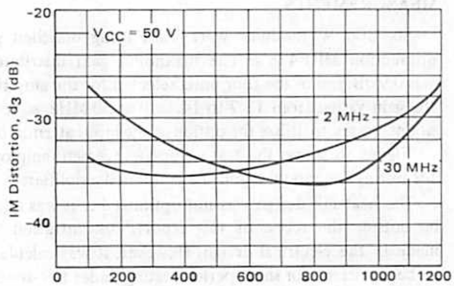


FIGURE 18 — IMD versus Power Output

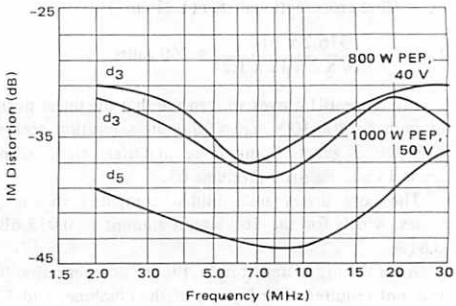


FIGURE 20 — IMD versus Frequency

four 9" lengths of Thermalloy 6151 extrusion, each having a free air thermal resistance of 0.7°C/W. They are bolted in pairs to two 9" x 8½" x 3/8" copper plates, to which the four power modules are mounted. Assuming a coefficient of 0.85 between two parallel extrusions, a total thermal resistance of 0.4°C/W is realized. Two of these dual extrusions are mounted back-to-back to provide

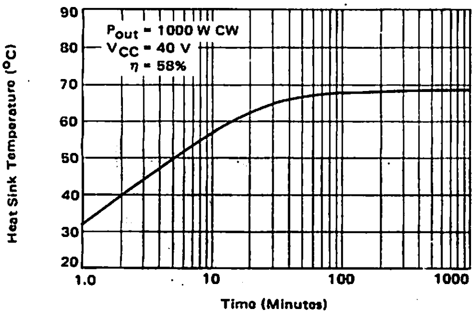


FIGURE 21 — Heat Sink Temperature versus Time

a channel for the air flow from four Rotron SP2A2 4" fans. Two are mounted in each end of the heatsink, and the four fans operating in the same direction provide an air flow of approximately 150 CFM.

The third order harmonic is 14 dB below the fundamental at certain frequencies, as can be seen in Figure 22. This number is typical in a four octave amplifier, and it is obvious that some type of output filter is required when it is used for communications purposes.

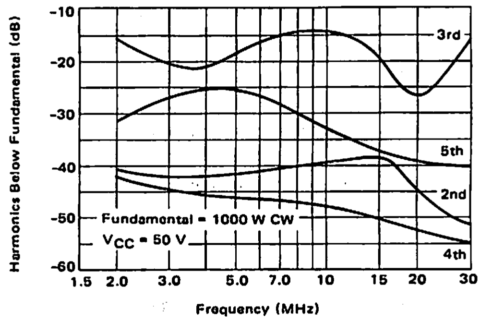


FIGURE 22 — Output Harmonic Contents versus Frequency

The 10:1 load mismatch was simulated with 34 feet of RG-58 coaxial cable, which has an attenuation of approximately 0.9 dB at 30 MHz, representing 1.8 dB return loss. The coaxial was terminated into an LC network consisting of a 2 x 15 – 125 pF variable capacitor and two inductors as shown in Figure 23.

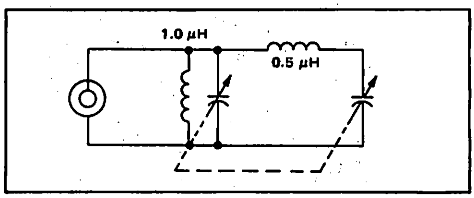
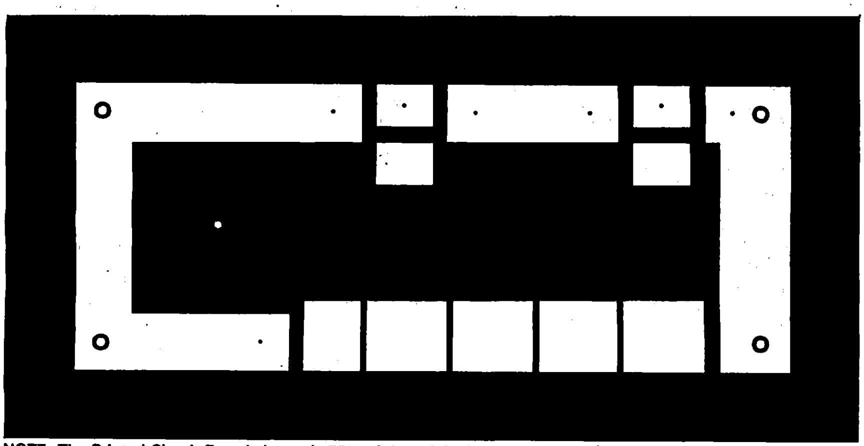


FIGURE 23 — Load Mismatch Test Circuit



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 24 — Circuit Board Layout of the Power Combiner Assembly

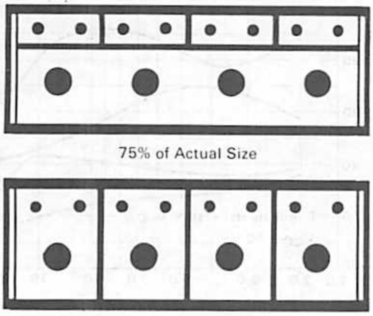
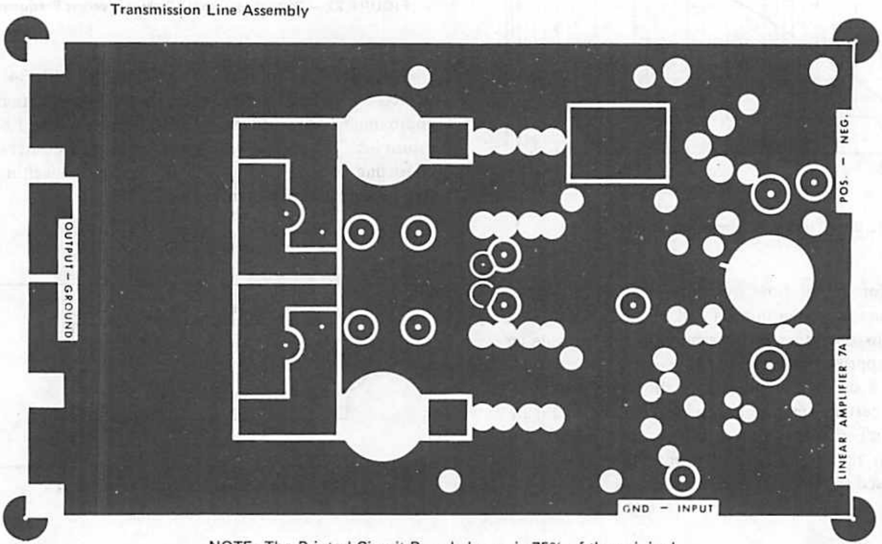


FIGURE 25 – Board Layout of the Power Combiner Transmission Line Assembly

The high current mode appears at a phase angle of -90° and 20 Ω, where the monitored individual collector currents increased to 6.8 A. At 50 V this amounts to 340 W, which almost entirely represents device dissipation.

At 20:1 load mismatch an equal power dissipation is reached at a power output of approximately 650 W CW.

Since the collector voltages remain below the device breakdown at the high impedance mode (+90°C, 150 Ω), it may be concluded, that the load mismatch susceptibility is limited by overdissipation of the transistors.



NOTE: The Printed Circuit Board shown is 75% of the original.

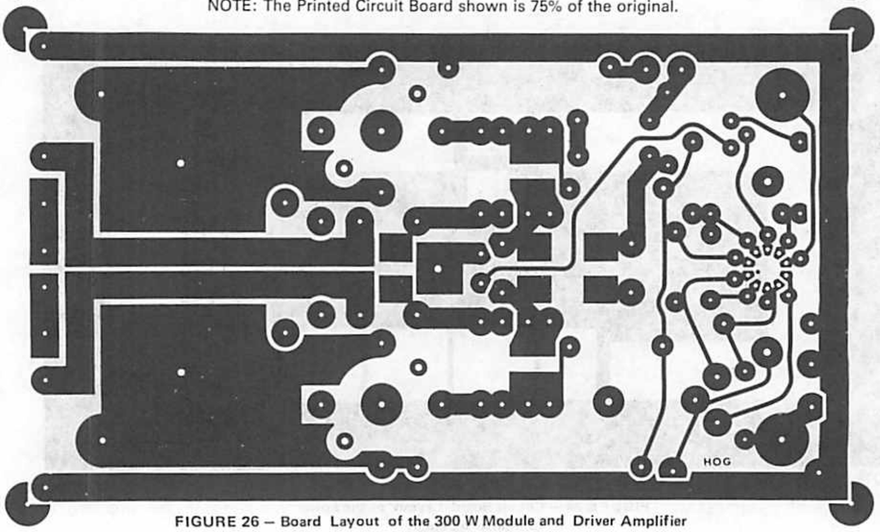


FIGURE 26 – Board Layout of the 300 W Module and Driver Amplifier

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LINEAR AMPLIFIERS FOR MOBILE OPERATION

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INTRODUCTION

The three versions of the amplifier described here are intended mainly for amateur radio applications, but are suitable for other applications such as marine radio with slight modifications.

100 W is obtained with two MRF455's. MRF460 or MRF453 is also adaptable to this design, resulting in approximately 1.0 to 2.5 dB higher overall power gain than the values shown. The MRF454 devices which can be directly substituted with MRF458's for slightly lower IMD, deliver the 140 W, and two MRF421 devices are used in the 180 W version.

The use of chip capacitors results in good repeatability, making the overall design suitable for mass production.

There are several precautions and design hints to be taken into consideration regarding transistor amplifiers:

1. Eliminate circuit oscillation. Oscillations may cause overdissipation of the device or exceed the breakdown voltages.
2. Limit the power supply current to prevent excessive dissipation.
3. Adopt protective circuitry, such as fast acting ALC.
4. Ensure proper attachment of the device to a heatsink using Silicone grease (such as Corning 340 or GC Electronics 8101) to fill all thermal gaps.

THE TRANSISTORS

The MRF421 with a specified power output of 100 W PEP or CW is the largest of the three RF devices. The maximum dissipation limit is 290 Watts, which means that the continuous collector current could go as high as 21.3 A at 13.6 V operated into any load. The data sheet specifies 20 A; this is actually limited by the current carrying capability of the internal bonding wires. The values given are valid at a 25°C mount temperature.

The minimum recommended collector idling current in Class AB is 150 mA. This can be exceeded at the expense of collector efficiency, or the device can be operated in Class A at an idling current of approximately one fourth the maximum specified collector current. This rule of thumb applies to most RF power transistors, although not specified for Class A operation.

The MRF454 is specified for a power output of 80 W CW. Although the data sheet does not give broadband performance or IMD figures, typical distortion products are ≈ -31 to -33 dB below one of the two test tones (7) with a 13.6 V supply. This device has the highest figure of merit (ratio of emitter periphery and base area), which correlates with the highest power gain.

The maximum dissipation is 250 Watts, and the maximum continuous collector current is 20 A. The minimum recommended collector idling current is 100 mA, and like the MRF421, can be operated in Class A.

The data sheet specification for the MRF455 is 65 W CW, but it can be operated in SSB mode, and typically makes -32 to -34 dB IMD in reference to one of the two test tones at 50 W PEP, 13.6 volts. It contains the same die as MRF453 and MRF460, but is tested for different parameters and employs a smaller package. The MRF455/MRF453/MRF460 has a higher figure of merit than the two devices discussed earlier. Due to this and the higher associated impedance levels, the power gain exceeds that of the MRF454 and MRF421 in a practical circuit. The minimum recommended collector idling current is 40 mA for Class AB, but can be increased up to 3.0 A for Class A operation.

It should be noted that the data sheet figures for power gain and linearity are lowered when the device is used in multi-octave broadband circuit. Normally the device input and output impedances vary by at least a factor of three from 1.6 to 30 MHz. Therefore, when impedance correction networks are employed, some of the power gain and linearity must be sacrificed.

The input correction network can be designed with RC or RLC combinations to give better than 1 dB gain flatness across the band with low input VSWR. In a low-voltage system, little can be done about the output without reducing the maximum available voltage swing.

At power levels up to 180 Watts and 13.6 V, the peak currents approach 30 A, and every 100 mV lost in the emitter grounding or collector dc feed also have a significant effect in the peak power capability. Thus, these factors must be emphasized in RF power circuit design.

THE BASIC CIRCUIT

Figure 1 shows the basic circuit of the linear amplifier. For different power levels and devices, the impedance ratios of T1 and T3 will be different and the values of R1, R2, R3, R4, R5, C1, C2, C3, C4 and C6 will have to be changed.

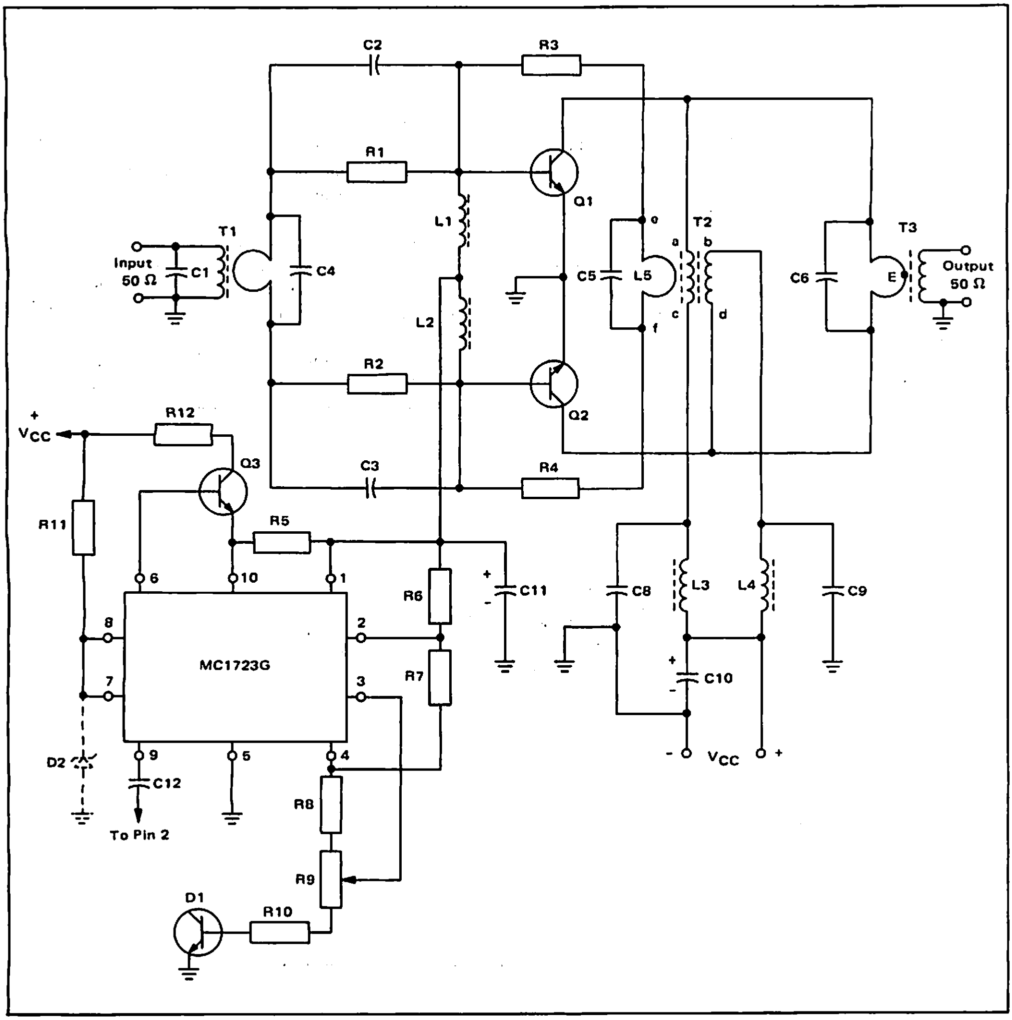

FIGURE 1 — Basic Circuit of Linear Amplifier

The Bias Voltage Source

The bias voltage source uses active components (MC1723G and Q3) rather than the clamping diode system as seen in some designs. The advantages are line voltage regulation capability, low stand-by current, (≈1.0 mA) and wide range of voltage adjustability. With the component values shown, the bias voltage is adjustable from 0.5 to 0.9 Volts, which is sufficient from Class B to Class A operating conditions.

In Class B the bias voltage is equal to the transistor V_{BE}, and there is no collector idling current present (except small collector-emitter leakage, I_{CES}), and the conduction angle is 180°.

In Class A the bias is adjusted for a collector idling current of approximately one-half of the peak current in actual operating conditions, and the conduction angle is 360°.

In Class AB, (common for SSB amplifiers) the bias is set for a low collector quiescent current, and the conduction angle is usually somewhat higher than 180°.

The required base bias current can be approximated as:

$$\frac{I_C}{h_{FE}},$$

where:

I_C = Collector current, assuming an efficiency of 50%

and P_{out} of 180 W is: $\frac{2P_{out}}{V_{CC}} = \frac{360}{13.6} = 26.47$ A.

h_{FE} = Transistor dc beta (typical 30, from data sheet)

Bias current $= \frac{26.47}{30} = 0.88$ A

R12 shares the dissipation with Q3, and its value must be such that the collector voltage never drops below approximately 2.0 V (e.g. $\frac{(13.6-2)}{0.88} = 13.2\ \Omega$). The MRF421 devices used for this design had h_{FE} values on the high side (45), and R12 was calculated as 20Ω, which is also sufficient for the lower power versions.

R5 determines the current limiting characteristics of the MC1723, and 0.5 Ω will set the limiting point to 1.35 A, ± 10%.

For SSB operation, excluding two-tone testing, the duty cycle is low, and the energy charged in C11 can supply higher peak bias currents than required for 180 W PEP.

It is possible to operate the basic regulator circuit, MC1723, at lower output voltages than specified, with modified component values, at a cost of reduced line and output voltage regulation tolerances which are still more than adequate for this application. Temperature sensing diode D1 is added for bias tracking with the RF power transistors. The base-emitter junction of a 2N5190 or similar device can be used for this purpose. The temperature tracking within 15% to 60°C is achieved, even though the die processing is quite different from that of the RF transistors. The physical dimensions of Case 77 (2N5190) permits its use for the center stand-off of the circuit board.

The measured output voltage variations of the bias source from zero to 1.0 A were ± 8-12 mV resulting in a source impedance of ≈ 30 mΩ.

The Input Frequency Correction Network

The input correction network consists of R1, R2, C2 and C3. With the combination of the negative feedback derived from L5 through R3 and R4 (Figure 1), it forms an attenuator with frequency selective characteristics. At 30 MHz the input power loss is 1-2 dB, increasing to 10-12 dB at 1.6 MHz. This compensates the gain variations of the RF transistors over the 1.6 to 30 MHz band, resulting in an overall gain flatness of approximately ±1.0 to ±1.5 dB.

Normally an input VSWR of 2.0:1 or lower (Figure 8) is possible with this type of input network (considered sufficient for most applications). More sophisticated LRC networks will yield slightly better VSWR figures, but are more complex and sometimes require individual adjustments.

Additional information on designing and optimizing these networks can be found in reference(2).

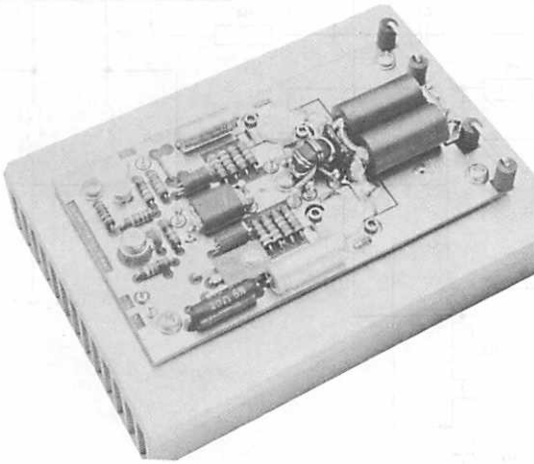

FIGURE 2 — Photograph of 180 W Version of the Linear Amplifier

The Broadband Transformers

The input transformer T1 and the output transformer T3 are of the same basic type, with the low impedance winding consisting of two pieces of metal tubing, electrically shorted in one end and the opposite ends being the connections of this winding (Figure 3A). The multiturn high impedance winding is threaded through the tubing so that the low and high impedance winding connections are in opposite ends of the transformer.

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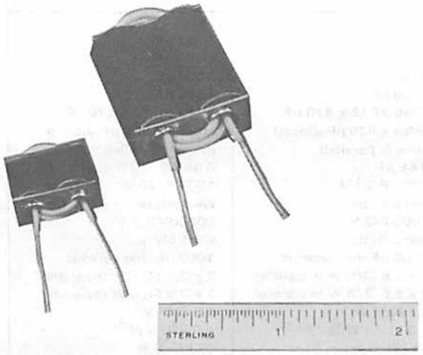
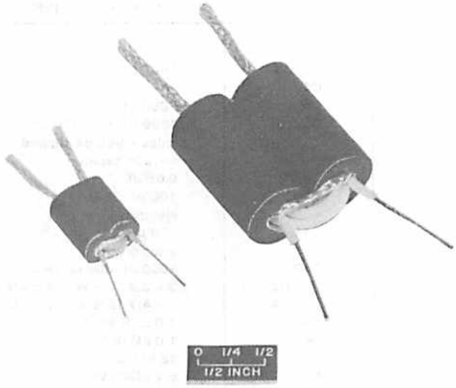


A.



B.

FIGURE 3 – Two Variations of the Input and Output Transformers (T1 and T3)

The physical configuration can be implemented in various manners. A simplified design can be seen in Figure 3B. Here the metal tubing is substituted with copper braid, obtained from any co-axial cable of the proper diameter [4]. The coupling coefficient between the primary and secondary windings is determined by the length-to-diameter ratio of the metal tubing or braid, and the gauge and insulation thickness of the wire used for the high impedance winding. For high impedance ratios (36:1 and higher), miniature co-axial cable where only the braid is used, leaving the inner conductor disconnected gives the best results. The high coefficient of coupling is important only at the high-frequency end of the band, e.g. 20 to 30 MHz. Additional information on these transformers can be found in reference [5].

Both transformers are loaded with ferrite material to provide sufficient low-frequency response. The minimum required inductance in the one turn winding can be calculated as:

$$L = \frac{R}{2\Pi f}$$

where L = Inductance in μH
R = Base-to-Base or Collector-to-Collector Impedance
f = Lowest Frequency in MHz

For example, in the 180 Watt version the input transformer is of 16:1 impedance ratio, making the secondary impedance 3.13 Ω with a 50 Ω interface.

Then: $L = \frac{3.13}{6.28 \times 1.6} = 0.31\ \mu H$

For the output transformer having a 25:1 impedance ratio to a 50 Ω interface, $L = \frac{2}{6.28 \times 1.6} = 0.20\ \mu H$.

It should be noted that in the lower power versions, where the input and output impedances are higher and the transformers have lower impedance ratios, the required minimum inductances are also higher.

T2, the collector choke supplying the dc to each collector, also provides an artificial center tap for T3. This combination functions as a real center tapped transformer with even harmonic cancellation. T2 provides a convenient low impedance source for the negative feedback voltage, which is derived from a separate one turn winding.

T3 alone does not have a true ac center tap, as there is virtually no magnetic coupling between its two halves. If the collector dc feed is done through point E (Figure 1) without T2, the IMD or power gain is not affected, but the even harmonic suppression may be reduced by as much as 10 dB at the lower frequencies.

The characteristic impedance of ac and bd (T2) should equal one half the collector-to-collector impedance but is not critical, and for physical convenience a bifilar winding is recommended.

The center tap of T2 is actually bc (Figure 1), but for stabilization purposes, b and c are separated by RF chokes by-passed individually by C8 and C9.

TABLE 1 — Parts List*

	100 W AMPLIFIER	140 W AMPLIFIER	180 W AMPLIFIER
C1	51 pF	51 pF	82 pF
C2, C3	5600 pF	5600 pF	6800 pF
C4	–	390 pF	1000 pF
C5	680 pF	680 pF	680 pF
C6	1620 pF (2 x 470 pF chips + 680 pF dipped mica in parallel)	1760 pF (2 x 470 pF chips + 820 pF dipped mica in parallel)	1940 pF (2 x 470 pF chips + 1000 pF dipped mica in parallel)
C8, C9	0.68 μF	0.68 μF	0.68 μF
C10	100 μF/20 V electrolytic	100 μF/20 V electrolytic	100 μF/20 V electrolytic
C11	500 μF/3 V electrolytic	500 μF/3 V electrolytic	500 μF/3 V electrolytic
C12	1000 pF disc ceramic	1000 pF disc ceramic	1000 pF disc ceramic
R1, R2	2 x 3.9 Ω/½ W in parallel	2 x 3.6 Ω/½ W in parallel	2 x 3.3 Ω/½ W inparallel
R3, R4	2 x 4.7 Ω/½ W in parallel	2 x 5.6 Ω/½ W in parallel	2 x 3.9 Ω/½ W inparallel
R5	1.0 Ω/½ W	0.5 Ω/½ W	0.5 Ω/½ W
R6	1.0 kΩ/½ W	1.0 kΩ/½ W	1.0 kΩ/½ W
R7	18 kΩ/½ W	18 kΩ/½ W	18 kΩ/½ W
R8	8.2 kΩ/½ W	8.2 kΩ/½ W	8.2 kΩ/½ W
R9	1.0 kΩ trimpot	1.0 kΩ trimpot	1.0 kΩ trimpot
R10	150 Ω/½ W	150 Ω/½ W	150 Ω/½ W
R11	1.0 kΩ/½ W	1.0 kΩ/½ W	1.0 kΩ/½ W
R12	20 Ω/5 W	20 Ω/5 W	20 Ω/5 W
L1, L2	Ferroxcube VK200 19/4B ferrite choke		
L3, L4	Two Fair-Rite Products ferrite beads 2673021801 or equivalent on AWG #16 wire each.		
L5	1 separate turn through toroid of T2.		
T1	9:1 (3:1 turns ratio)	9:1 (3:1 turns ratio)	16:1 (4:1 turns ratio)
	Ferrite core: Stackpole 57-1845-24B, Fair-Rite Products 2873000201 or two Fair-Rite Products 0.375" OD x 0.200" ID x 0.400", Material 77 beads for type A (Figure 3) transformer. See text.		
T2	6 turns of AWG #18 enameled, bifilar wire		
	Ferrite core: Stackpole 57-9322, Indiana General F627-8 Q1 or equivalent.		
T3	16:1 (4:1 turns ratio)	16:1 (4:1 turns ratio)	25:1 (5:1 turns ratio)
	Ferrite core: 2 Stackpole 57-3238 ferrite sleeves (7D material) or number of toroids with similar magnetic characteristics and 0.175" sq. total cross sectional area. See text.		
	All capacitors except C12, part of C5 and the electrolytics are ceramic chips. Values over 82 pF are Union Carbide type 1225 or Varadyne size 14. Others are type 1813 or size 18 respectively.		
Q1, Q2	MRF453, MRF460, MRF455	MRF454, MRF458,	MRF421
Q3		2N5989 or equivalent	
D1		2N5190 or equivalent	
D2		Not Used	
	c.	b.	a.
	Dotted line in performance data.	Dashed line in performance data.	Solid line in performance data.

*Note: parts & kits for this amplifier are available from Communication Concepts, 121 Brown St., Dayton, Ohio 45402 (513) 220-9677

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GENERAL DESIGN CONSIDERATIONS

As the primary and secondary windings of T3 are electrically isolated, the collector dc blocking capacitors (which may also function as low-frequency compensation elements) have been omitted. This decreases the loss in RF voltage between the collectors and the transformer primary, where every 100 mV amounts to approximately 2 W in output power at 180 W level. The RF currents at the collectors operating into a 2Ω load are extremely high, e.g.: $I_{RF} = \sqrt{\frac{180}{2.0}} = 9.5$ A, or peak $\frac{9.5}{0.707} = 13.45$ A.

Similarly, the resistive losses in the collector dc voltage path should be minimized. From the layout diagram of the lower side of the circuit board (Figure 4), V_{CC} is brought through two 1/4" wide runs, one on each side of the board. With the standard 1.0 oz. laminate, the copper thickness is 1.4 thousands of an inch, and their combined cross sectional area would be equivalent to AWG #20 wire. This is not adequate to carry the dc collector current which under worst case conditions can be over 25 A. Therefore, the high power version of this design requires 2 oz. or heavier copper laminate, or these runs should be reinforced with parallel wires of sufficient gauge.

The thermal design (determining the size and type of a heat sink required) can be accomplished with information in the device data sheet and formulas presented in references 5 and 6. As an example, with the 180 W unit using MRF421's, the Junction-to-Ambient Temperature

($R\theta JA$) is calculated first as $R\theta JA = \frac{T_J - T_A}{P}$ where:

T_J = Maximum Allowed Junction Temperature (150°C).
T_A = Ambient Temperature (40°C).

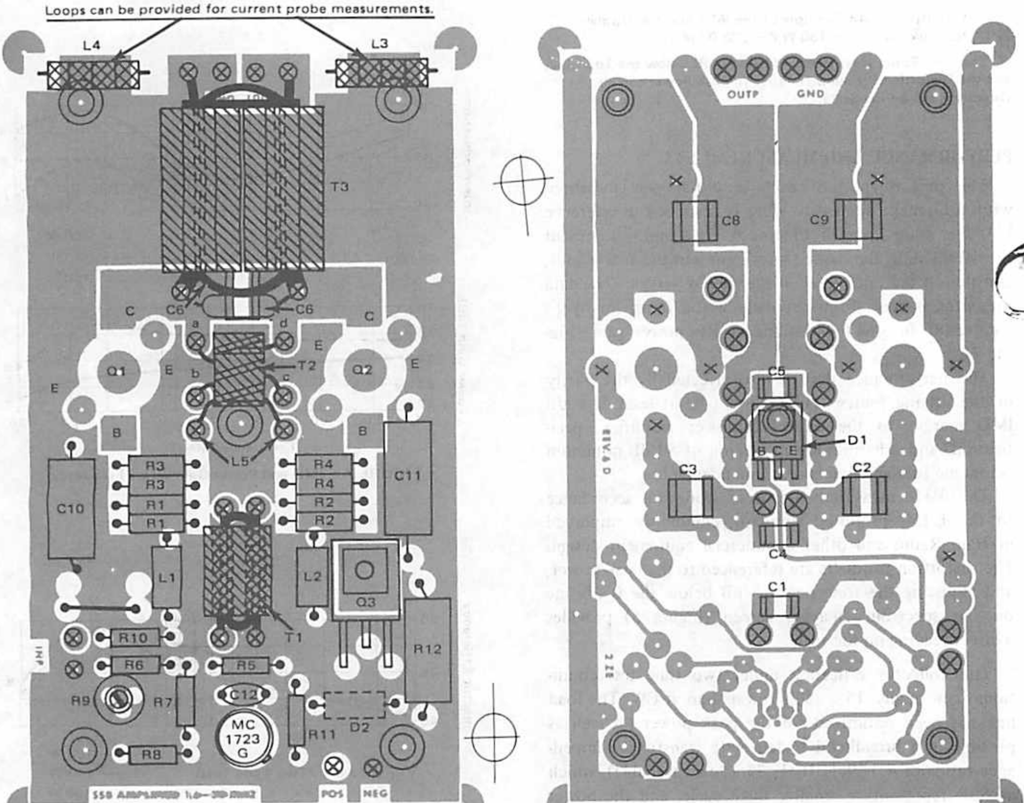
P = Dissipated Power $(\frac{180}{\eta}) \times (100 - \eta)$
η = Collector Efficiency (%).

If the worst case efficiency at 180 W CW is 55%, then

$P = 148$ W, and $R\theta JA = \frac{150 - 40}{(\frac{148}{2})} = 1.49°$ C/W (for one device). The Heat Sink-to-Ambient Thermal Resistance, $R\theta SA = R\theta JA - (R\theta JC + R\theta CS)$ where: $R\theta JC$ = Device Junction-to-Case Thermal Resistance, 0.60°C/W* (from data sheet).
$R\theta CS$ = Thermal Resistance, Case-to-Heat Sink, 0.1°C/W (from table in reference 5).

Then: $R\theta SA = \frac{1.49 - (0.60 + 0.1)}{2} = 0.395°$ C/W

This number can be used to select a suitable heat sink for the amplifier. The information is given by most manufacturers for their standard heat sinks, or specific lengths of extrusion. As an example, a 9.1" length of thermalloy 6153 or a 7.6" length of Aavid Engineering 60140 extrusion would be required for 100% duty cycle, unless the air velocity is increased by a fan or other means.



◎ = Board Stand Off's
⊗ = Terminal Pins and Feedthroughs
X = Feedthrough Eyelets

* The $R\theta JC$ figure of 0.875°C/W given for the MRF421 is in error, and will be corrected in the future prints of the data sheet.

FIGURE 4 — Component Layout of the Basic Amplifier

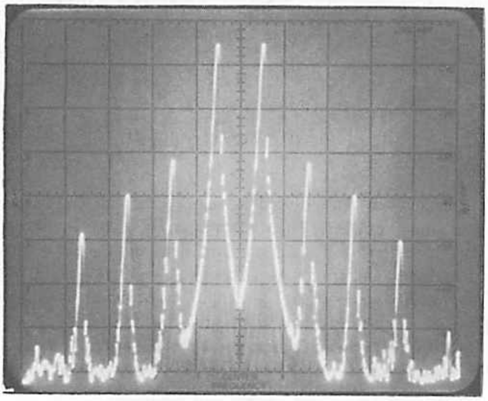


FIGURE 5 – An Example of the IMD Spectral Display (c. Power Output = 180 W PEP, 30.00 MHz)

The Two Tones Have Been Adjusted 6 dB Below the Top Line, and the Distortion Products Relative to Peak Power can be Directly Read on the Scale.

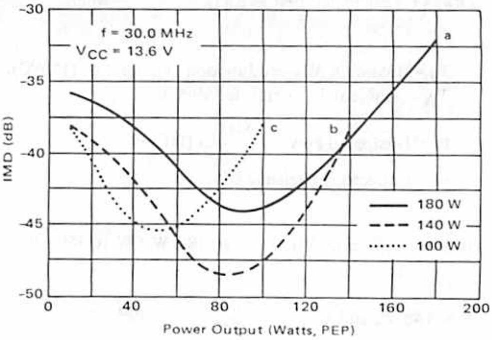


FIGURE 6 – Intermodulation Distortion versus Power Output

PERFORMANCE AND MEASUREMENTS

The performance of each amplifier was measured with equipment similar to what is described in reference [2]. The solid lines in Figures 6, 7, 8 and 9 represent the 100 W unit, the dashed lines represent the 140 W unit, and the dotted lines refer to the 180 W version. The data presented is typical, and spreads in the transistor h_{FE}'s will result in slight variations in RF power gain (Figure 7).

The performance data is also affected by the purity of the driving source. There should be at least 5–6 dB IMD margin to the expected power amplifier specification, and a harmonic suppression of 50 dB minimum below the fundamental is recommended [7].

The IMD measurements were done in accordance to the E.I.A. proposed standard, commonly employed in Ham Radio and other commercial equipment design. The distortion products are referenced to the peak power, and adjusting the tone peaks 6 dB below the 0 dB line on the spectrum analyzer screen (Figure 5) provides a direct reading on the scale.

The collector efficency under two tone test conditions is normally 15 – 20% lower than at CW. The load line has been optimized for the peak power (as well as possible in a broadband system with transformer impedance ratios of 4:1, 9:1, 16:1, 25:1, etc. available), which at SSB represents a smaller duty cycle, and the power output varies between zero and maximum. Typical figures are 40 – 45% and 55 – 65% respectively.

The stability and load mismatch susceptibility were tested at 15 and 30 MHz employing an LC network [2] to simulate high and low reactive loads at different phase angles. The maximum degree of load mismatch was controlled by placing high power 50-Ohm attenuators between the amplfiier output and variable LC network.

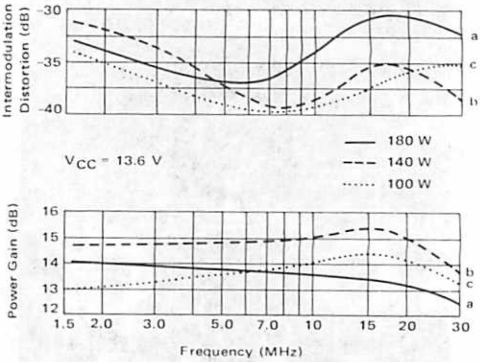


FIGURE 7 – IMD and Power Gain versus Frequency

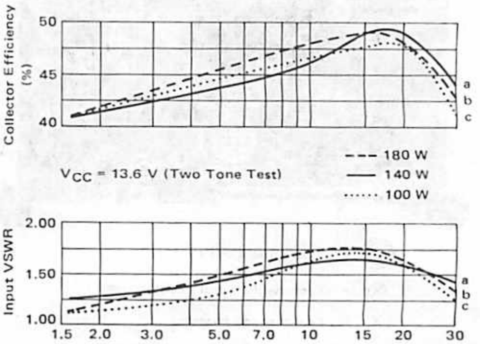


FIGURE 8 – Input VSWR and Collector Efficiency versus Frequency

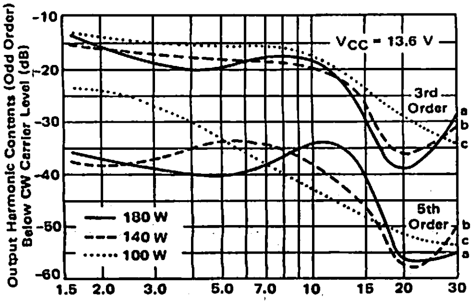


FIGURE 9 — Output Harmonic Contents (Odd Order) versus Frequency

A 2 dB attenuator limits the output VSWR to 4.5:1, 3 dB to 3.0:1, 6 dB to 1.8:1 etc., assuming that the simulator is capable of infinite VSWR at some phase angle. The attenuators for -1.0 dB or less were constructed of a length of RG-58A co-axial cable, which at 30 MHz has an attenuation of 3.0 dB/100 ft. and at 15 MHz 2.0 dB/100 ft. Combinations of the cable and the resistive attenuators can be used to give various degrees of total attenuation.

The tests indicated the 100 W and 140 W amplifiers to be stable to 5:1 output VSWR at all phase angles, and the 180 W unit is stable to 9:1. All units passed a load mismatch test at full rated CW power at an output load mismatch of 30:1, which they were subjected to, until the heat sink temperature reached 60°C. For this, the load mismatch simulator was motor driven with a 2 second cycle period.

Output Filtering

Depending on the application, harmonic suppression of -40 dB to -60 dB may be required. This is best accomplished with low-pass filters, which (to cover the entire range) should have cutoff frequencies e.g. 35 MHz, 25 MHz, 15 MHz, 10 MHz, 5.5 MHz and 2.5 MHz.

The theoretical aspect of low-pass filter design is well covered in the literature (8).

A simple Chebyshev type constant K, 2 pole filter (Figure 10) is sufficient for 40 – 45 dB output harmonic suppression.

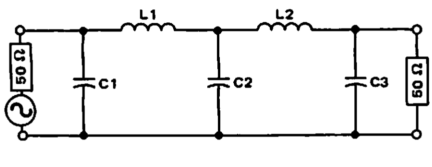


FIGURE 10

The filter is actually a dual pi-network, with each pole introducing a -90° phase shift at the cutoff frequency, where L1, L2, C1 and C3 should have a reactance of 50 Ohms, and C2 should be 25 Ohms. If C2 is shorted, the resonances of L1C1 and L2C3 can be checked with a grid-dip meter or similar instrument for their resonant frequencies.

The calculated attenuation for this filter is 6.0 dB per element/octave, or -45 dB for the 3rd harmonic. In practice, only -35 to -40 dB was measured, but this was due to the low Q values of the inductors (approximately 50). Air core inductors give excellent results, but toroids of magnetic materials such as Micrometals grade 6 are also suitable at frequencies below 10 MHz. Dipped mica capacitors can be used throughout.

If the filters are correctly designed and the component tolerances are 5% or better, the power loss will be less than 1.0 dB.

NOTE: The use of these amplifiers is illegal for Class D Citizens band service.

SUMMARY

The basic circuit layout (Figure 1) has been successfully adopted by several equipment manufacturers. Minor modifications may be necessary depending on the availability of specific components. For instance, the ceramic chip capacitors may vary in physical size between various brands, and recent experiments show that values > 0.001 μF can be substituted with unencapsulated polycarbonate stacked-foil capacitors. These capacitors are available from Siemens Corporation (type B32540) and other sources. Also T1 and T2 can be constructed from stacks of ferrite toroids with similar material characteristics. Toroids are normally stock items, and are available from most ferrite suppliers.

The above is primarily intended to give an example of the device performance in non-laboratory conditions, thus eliminating the adjustments from unit to unit.

REFERENCES:

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3. Granberg, H.: *Get 300 W PEP Linear Across 2 to 30 MHz From This Push-Pull Amplifier,* EB-27A Motorola Semiconductor Products Inc..
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5. White, John: Thermal Design of Transistor Circuits, *QST*, April 1972, pp. 30-34.
6. *Mounting Stripline-Opposed-Emitter (SOE) Transistors,* AN-555 Motorola Semiconductor Products Inc..
7. Granberg, H.: *Measuring the Intermodulation Distortion of Linear Amplifiers,* EB-38 Motorola Semiconductor Products Inc..
8. *Reference Data for Radio Engineers,* ITT, Howard & Sams Co., Inc.

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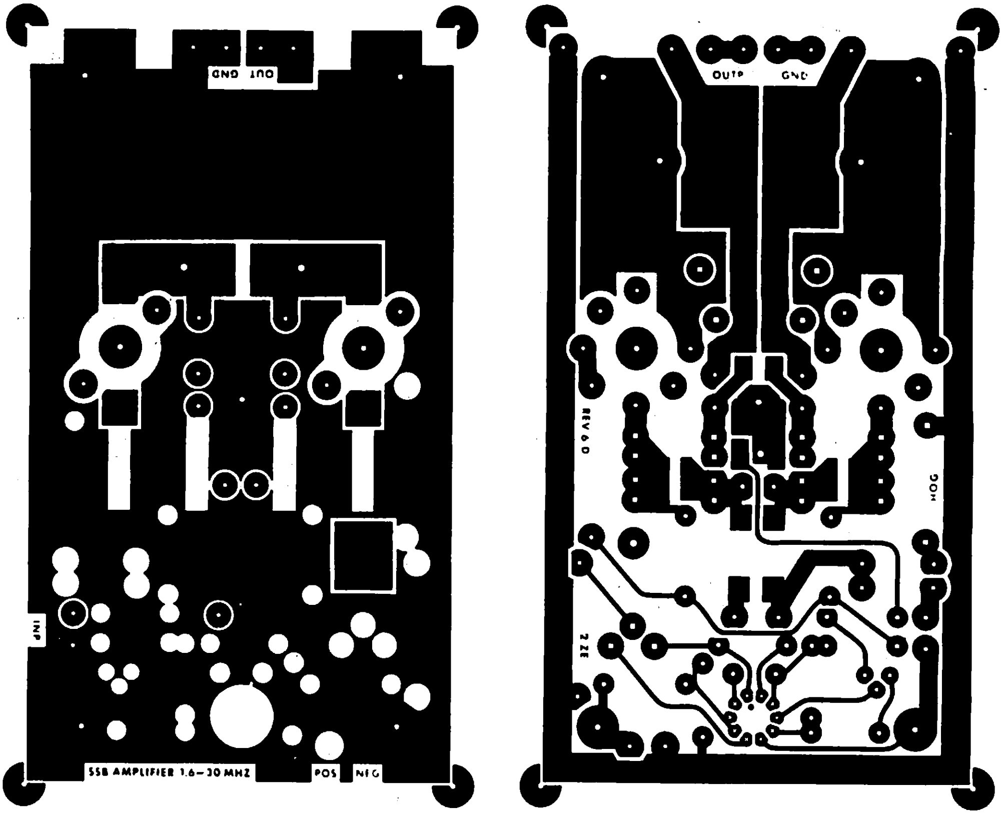
The PCB layout below is a supplement to Figure 4 and may be used for generating printed circuit artwork.



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 11 — Printed Circuit Board Layout

LOW-DISTORTION 1.6 TO 30 MHz SSB DRIVER DESIGNS

Prepared by
Helge O. Granberg
RF Circuits Engineering

GENERAL CONSIDERATION

Two of the most important factors to be considered in broadband linear amplifier design are the distortion and the output harmonic rejection.

The major cause for intermodulation distortion is amplitude nonlinearity in the active element. The nonlinearity generates harmonics, and the fundamental odd-order products are defined as $2f_1-f_2$, $2f_2-f_1$, $3f_2-2f_2$, $3f_2-2f_1$, etc., when a two-tone test signal is used. These harmonics may not always appear in the amplifier output due to filtering and cancellation effects, but are generated within the active device. The amplitude and harmonic distortion cannot really be distinguished, except in a case of a cascaded system, where even-order products in each stage can produce odd-order products through mixing processes that fall in the fundamental region.[2] This, combined with phase distortion – which in practical circuits is more apparent at higher frequencies – can make the distortion analysis extremely difficult;[5,2] whereas, if only amplitude distortion was present, the effect of IMD in each stage could easily be calculated.

In order to expect a low harmonic output of the power amplifier, it is also important for the driving source to be harmonic-free. This is difficult in a four-octave bandwidth system, even at 10-20 watt power levels. Class A biasing helps the situation, and Class A push-pull yields even better results due to the automatic rejection of even harmonics.

Depending on the application, a full Class A system is not always feasible because of its low efficiency. The theoretical maximum is 50%, but practical figures are not higher than 25% to 35%. It is sometimes advantageous to select a bias point somewhere between Class AB and A which would give sufficiently good results, since filtering is required in the power amplifier output in most instances anyway.

In order to withstand the high level of steady dc bias current, Class A requires a much larger transistor die than Class B or AB for a specific power output. There are sophisticated methods such as generating the bias voltage from rectified RF input power, making the dc bias proportional to the drive level.[1] This also yields to a better efficiency.

20 W, 25 dB AMPLIFIER WITH LOW-COST PLASTIC DEVICES

The amplifier described here provides a total power gain of about 25 dB, and the construction technique allows the use of inexpensive components throughout. The plastic RF power transistors, MRF475 and MRF476, featured in this amplifier, were initially developed for the CB market. The high manufacturing volume of these TO-220 packaged parts makes them ideal for applications up to 50 MHz, where low cost is an important factor.

The MRF476 is specified as a 3-watt device and the MRF475 has an output power of 12 watts. Both are extremely tolerant to overdrive and load mismatches, even under CW conditions. Typical IMD numbers are better than -35 dB, and power gains are 18 dB and 12 dB, respectively, at 30 MHz.

The collectors of the transistors are electrically connected to the TO-220 package mounting tab which must be isolated from the ground with proper mounting hardware (TO-220 AB) or by floating heat dissipators. The latter method, employing Thermalloy 6107 and 6106 heat dissipators, was adapted for this design. Without an airflow, the 6106 and 6107 provide sufficient heat sinking for about 30% duty cycle in the CW mode. Collector idle currents of 20 mA are recommended for both devices, but they were increased to 100 mA for the MRF475 and to 40 mA for the MRF476 to reduce the higher order IMD products and to achieve better harmonic suppression.

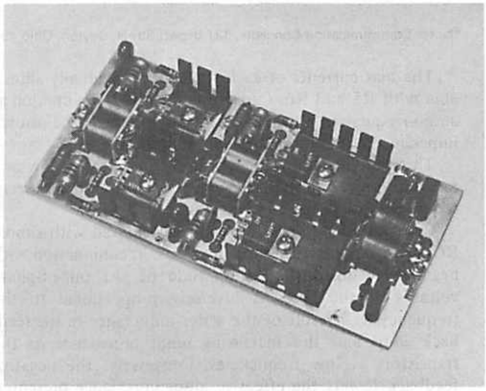
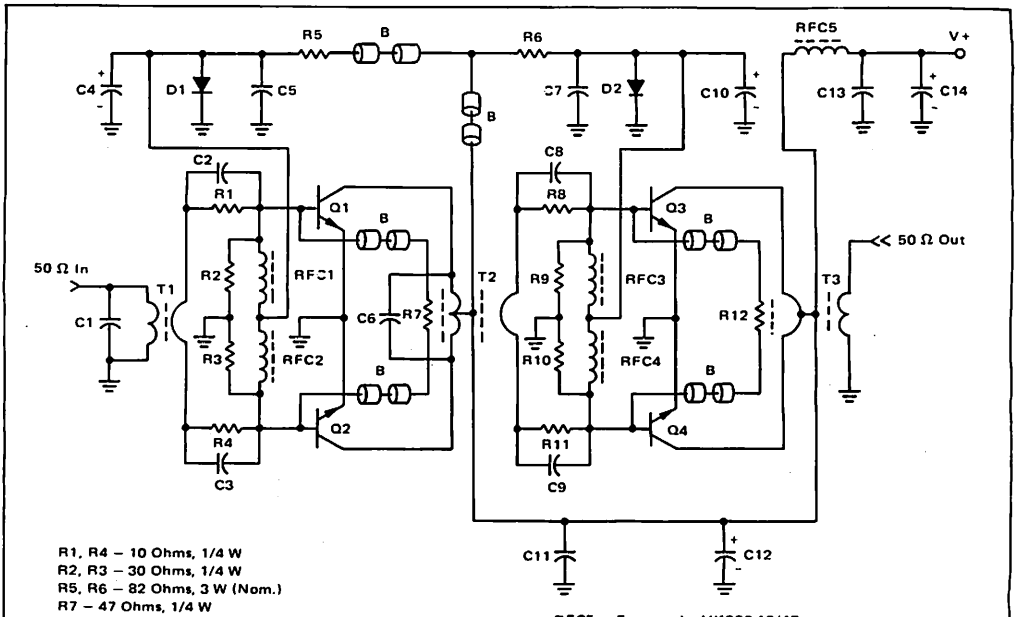


FIGURE 1

Biasing and Feedback

The biasing is achieved with the well-known clamping diode arrangement (Figure 2). Each stage has it own diode, resistor, and bypass network, and the diodes are mounted between the heat dissipators, being in physical contact with them for temperature-tracking purposes. A better thermal contact is achieved through the use of silicone grease in these junctions.



R1, R4 – 10 Ohms, 1/4 W
R2, R3 – 30 Ohms, 1/4 W
R5, R6 – 82 Ohms, 3 W (Nom.)
R7 – 47 Ohms, 1/4 W
R8, R11 – 6.8 Ohms, 1/4 W
R9, R10 – 15 Ohms, 1/4 W
R12 – 130 Ohms, 1/4 W

C1 – 39 pF Dipped Mica
C2, C3 – 680 pF Ceramic Disc
C4, C10 – 220 µF, 4 V, Tantalum
C5, C7, C11, C13 – 0.1 µF Ceramic Disc
C6 – 56 pF Dipped Mica
C8, C9 – 1200 pF Ceramic Disc
C12, C14 – 10 µF, 25 V Tantalum

RFC5 – Ferroxcube VK200 19/4B
RFC1, 2, 3, 4 – 10 µH Molded Choke

B – Ferrite Beads (Fair-Rite Prod. Corp. #2643000101 or Ferroxcube #56 590 65/3B)

D1, D2 – 1N4001

Q1, Q2 – MRF476
Q3, Q4 – MRF475

T1, T2 – 4:1 Impedance Transformer
T3 – 1:4 Impedance Transformer

FIGURE 2*

*Note: Communication Concepts, 121 Brown Street, Dayton, Ohio 45402 (513) 220-9677

The bias currents of each stage are individually adjustable with R5 and R6. Capacitors C4 and C10 function as audio-frequency bypasses to further reduce the source impedance at the frequencies of modulation.

This biasing arrangement is only practical in low and medium power amplifiers, since the minimum current required through the diode must exceed I_C/h_{fe}.

Gain leveling across the band is achieved with simple RC networks in series with the bases, in conjunction with negative feedback. The amplitude of the out-of-phase voltages at the bases is inversely proportional to the frequency as a result of the series inductance in the feedback loop and the increasing input impedance of the transistors at low frequencies. Conversely, the negative feedback lowers the effective input impedance presented to the source (not the input impedance of the device itself) and with proper voltage slope would equalize it. With this technique, it is possible to maintain an input VSWR of 1.5:1 or less from 1.6 to 30 MHz.

Impedance Matching and Transformers

Matching of the input and output impedances to 50 ohms, as well as the interstage matching, is accomplished with broadband transformers (Figures 3 and 4).

Normally only impedance ratios such as 1:1, 4:1, 9:1, etc., are possible with this technique, where the low-impedance winding consists of metal tubes, through which an appropriate number of turns of wire is threaded to form the high-impedance winding. To improve the broadband characteristics, the winding inductance is increased with magnetic material. An advantage of this design is its suitability for large-quantity manufacturing, but it is difficult to find low-loss ferrites with sufficiently high permeabilities for applications where the physical size must be kept small and impedance levels are relatively high. Problems were encountered especially with the output transformer design, where an inductance of 4 µH minimum is required in the one-turn winding across the collectors, when the load impedance is

$$\frac{2(V_{CE} - V_{CEsat})^2}{P_{out}} = \frac{2(13.6 - 2.5)^2}{20} = 12.3 \text{ ohms.}$$ [4,8]

Ferrites having sufficiently low-loss factors at 30 MHz range only up to 800–1000 in permeability and the inductance is limited to 2.5–3.0 µH in the physical size required. This would also limit the operation to approximately 4 MHz, below which excessive harmonics are

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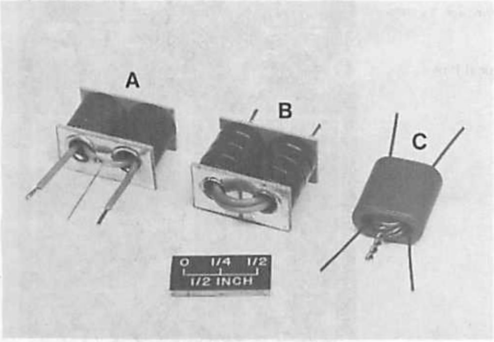

FIGURE 3

Examples of broadband transformers. Variations of these are used in all designs of this article (see text). All ferrites in transformers are Fair-Rite Products Corp. #2643006301 ferrite beads.* The turns ratios shown in Figure 4 are imaginary and do not necessarily lead to correct design practices.

generated and the efficiency will degrade. One possible solution is to increase the number of turns, either by using the metal tubes for only part of the windings as in Figure 4B, or simply by winding the two sets of windings randomly through ferrite sleeves or a series of beads (Figures 3C and 4C). In the latter, the metal tubes can be disregarded or can be used only for mounting purposes. T3 was eventually replaced with a transformer of this type, although not shown in Figure 1.

Below approximately 100 MHz, the input impedances of devices of the size of MRF475 and smaller are usually capacitive in reactance, and the X_S is much smaller than the R_S, (Low Q). For practical purposes, we can then use the formula $\sqrt{(R_S^2 + X_S^2)}$ to find the actual input impedance of the device. The data-sheet numbers for 30 MHz are 4.5, -j2.4 ohms, and we get $\sqrt{(4.5^2 + 2.4^2)} = 5.1$ ohms. The base-to-base impedance in a push-pull circuit would be four times the base-to-emitter impedance of one transistor. However, in Class AB, where the base-emitter junction is forward biased and the conduction angle is increased, the impedance becomes closer to twice that of one device. The rounded number of 11 ohms must then be matched to the driver output. The drive power required with the 10 dB specified minimum gain is

$$P_{out}/\mathrm{Log}^{-1}(G_{PE}/10) = 2.0\ \mathrm{W}$$

and the driver output impedance using the previous formula is $2(11.1^2)/2 = 123$ ohms. The 11 ohms in series with the gain-leveling networks (C8, R8 and C9, R11) is 17 ohms. The closest practical transformer for this interface would be one with 9:1 impedance ratio. This would present a higher-than-calculated load impedance to the driver collectors, and for the best linearity the output load should be lower than required for the optimum gain and efficiency. Considering that the device input impedance increases at lower frequencies, a better overall match is possible with a 4:1, especially since the negative feedback is limited to only 4 dB at 2 MHz due to its effect on the efficiency and linearity.

*Wallkill, N.Y. 12589

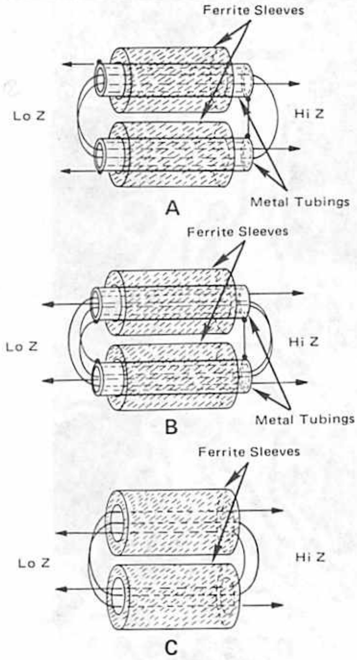

FIGURE 4

The maximum amount of feedback a circuit can tolerate depends much on the physical layout, the parasitic inductances, and impedance levels, since they determine the phase errors in the loop. Thus, in general, the high-level stages should operate with lower feedback than the low-level stages.

The maximum amount of feedback the low-level driver can tolerate without noticeable deterioration in IMD is about 12 dB. This makes the total 16 dB, but from the data sheets we find that the combined gain variation for both devices from 2 to 30 MHz is around 29 dB. The difference, or 13 dB, should be handled by the gain-leveling networks.

The input impedance of the MRF476 is 7.55, -j0.65 ohms at 30 MHz resulting in the base-to-base impedance of $2 \times \sqrt{(7.55^2 + 0.65^2)} = 15.2$ ohms. This, in series with networks R1, C1 and R4, C3 (2 x 4.4 ohms), gives 24 ohms, and would require a 2:1 impedance ratio transformer for a 50-ohm interface. However, due to the influence of strong negative feedback in this stage, a better overall matching is possible with 4:1 ratio. The input networks were designed in a manner similar to that described in Reference 8.

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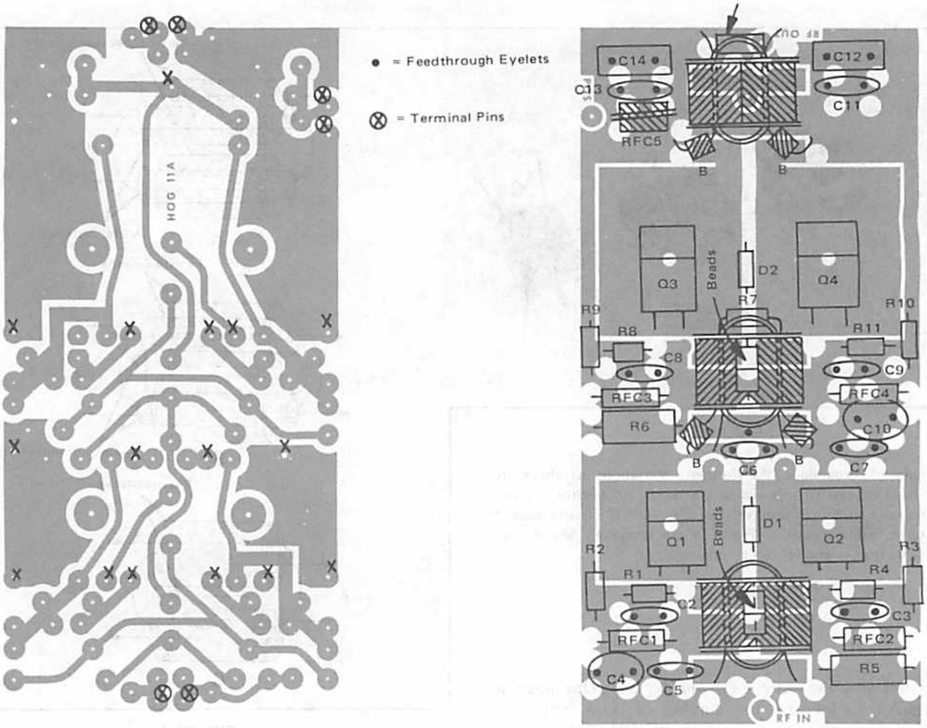


FIGURE 5
Component Layout Diagram of Low-Cost 20 W Amplifier

The leads of R7 and R12 form the one-turn feedback windings in T2 and T3. Ferrite beads in dc line can be seen located under T1 and T2.

Measurements and Performance Data

At a power output of 20 W CW, all output harmonics were measured about 30 dB or more below the fundamental, except for the third harmonic which was only attenuated 17 dB to 18 dB at frequencies below 5 MHz. Typical numbers for the higher order distortion products (d_9 and d_{11}) are in the order o. -60 dB above 7 MHz and -50 dB to -55 dB at the lower frequencies. These both can be substantially reduced by increasing the idle currents, but larger heat sinks would be necessary to accommodate the increased dissipation.

The efficiency shown in Figure 6 represents the overall figure for both stages. Currents through the bias networks, which are 82/(13.6 - 0.7) = 0.16 A each, are excluded. Modified values for R5 and R6 may have to be selected, depending on the forward voltage characteristics of D1 and D2.

Although this amplifier was designed to serve as a 1.6 to 30 MHz broadband driver, it is suitable for the citizens band use as well. With some modifications and design shortcuts, the optimization can be concentrated to one frequency.

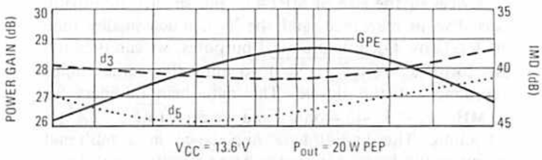


FIGURE 6
Intermodulation distortion and power gain versus frequency

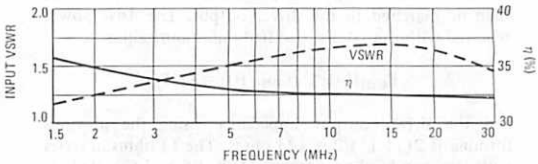
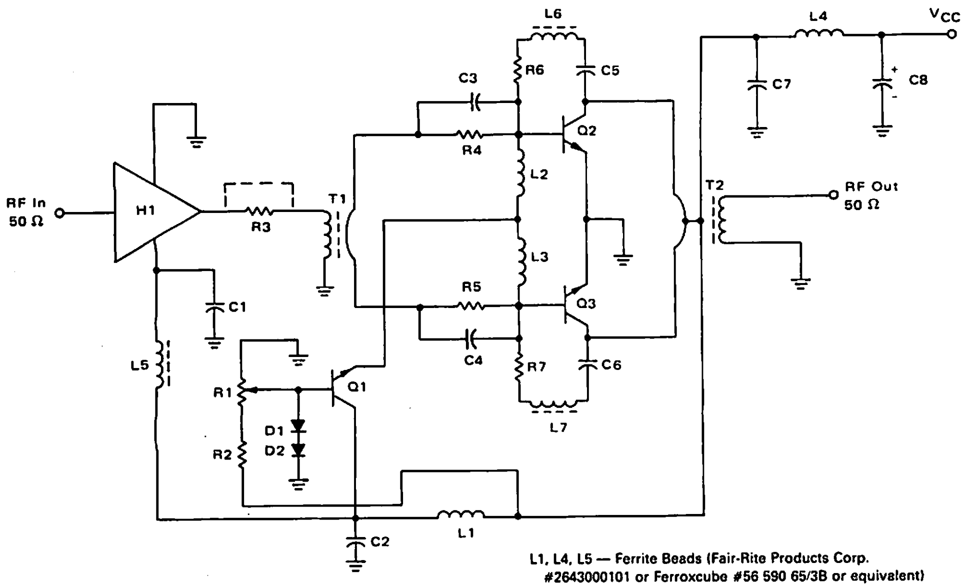


FIGURE 7
Input VSWR and combined collector efficiency of both stages



L1, L4, L5 — Ferrite Beads (Fair-Rite Products Corp. #2643000101 or Ferroxcube #56 590 65/3B or equivalent)
L2, L3 — 10 μH Molded Choke
L6, L7 — 0.1 μH Molded Choke

R1 — 1 k Trimpot
R2 — 1 k Ohm, 1/4 W
R3 — Optional
R4, R5 — 5, 6 Ohms, 1/4 W
R6, R7 — 47 Ohms, 1/4 W

Q1 — MJE240
Q2, Q3 — MRF433

H1 — MHW591

C1, C2, C5, C6, C7 — 0.01 μF Chip
C3, C4 — 1800 pF Chip
C8 — 10 μF/35 V Electrolytic

T1, T2 — 4:1 and 1:4 Impedance Transformers, respectively. (See discussion on transformers.) Ferrite Beads are Fair-Rite #2643006301 or equivalent)

FIGURE 8*

*Note: parts & kits for this amplifier are available from Communications Concepts, 121 Brown St., Dayton, Ohio 45402 (513) 220-9677

The output matching is done with a transformer similar to that described in the first part of this paper (Figures 4B, 4C). This transformer employs a multi-turn primary, which can be provided with a center tap for the collector dc feed. In addition to a higher primary *inductance, more effective* coupling between the two transformer halves is obtained, which is important regarding the even-order harmonic suppression.

28-Volt Version

A 28-V version of this unit has also been designed with the MHW592 and a pair of MRF401s. The only major change required is the output transformer, which should have a 1:1 impedance ratio in this case. The transformer consists of six turns of RG-196 coaxial cable wound on an Indiana General F-627-8-Q1 toroid. Each end of the braid is connected to the collectors, and the inner conductor forms the secondary. A connection is made in the center of the braid (three turns from each end) to form the center tap and dc feed.

The MRF433 and MRF401 have almost similar input characteristics, and no changes are necessary in the input circuit, except for the series feedback resistors, which should be 68–82 ohms and 1 W.

In designing the gain-leveling networks, another approach can be taken, which does not involve the computer program described in Reference 8. Although the input VSWR is not optimized, it has proved to give satisfactory results.

The amount of negative feedback is difficult to determine, as it depends on the device type and size and the physical circuit layout. The operating voltage has a minimal effect on the transistor input characteristics, which are more determined by the electrical size of the die. High-power transistors have lower input impedances and higher capacitances, and phase errors are more likely to occur due to circuit inductances.

Since the input capacitance is an indication of electrical size of the device, we can take the paralleled value (X_P) at 2 MHz, which is $X_S + (R_S^2/X_S)$ and for MRF433 $3.5 + (9.1^2/3.5) = 27$ ohms. The X_P of the largest devices available today is around 10 ohms at 30 MHz, and experience has shown that the maximum feedback should be limited to about 5 dB in such case. Using these figures

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as constants, and assuming the G_{PE} is at least 10 dB, we can estimate the amount of feedback as: $5/(10^2/27) + 5 = 6.35$ dB, although only 4 dB was necessary in this design due to the low ΔG_{PE} of the devices.

The series base resistors (R4 and R5) can be calculated for 4 dB loss as follows:

$$\frac{[(V_{in} \times \Delta 4dB) - V_{in}]}{I_{in}} = \frac{[(0.79 \times 1.58) - 0.79]}{0.04}$$

$$= 11.45 \text{ ohms, or}$$

$$11.45/2 = 5.72 \text{ ohms each.}$$

$Z_{in}(2\text{ MHz}) = \sqrt{(9.1^2 + 3.5^2)} = 9.75$ ohms, in Class AB push-pull 19.5 ohms.

$P_{in} = 20\text{ W} - 28\text{ dB} = 20/630 = 0.032\text{ W}$

$V_{RMS}\text{ (base to base)} = \sqrt{(0.032 \times 19.5)} = 0.79\text{ V}$

$I_{in} = V_{in}/R_{in} = 0.79/19.5 = 0.04\text{ A}$

$\Delta V4\text{ dB} = \sqrt{[\text{Log}^{-1}(4/10)]} = 1.58\text{ V}$

The parallel capacitors (C3 and C4) should be selected to resonate with R (5.7 ohms) somewhere in the mid-band. At 15 MHz, out of the standard values, 1800 pF appears to be the closest, having a negligible reactance at 2 MHz, and 2.8 ohms at 30 MHz, where most of the capacitive reactance is cancelled by the transformer winding inductance.

Measurements and Performance Data

The output harmonic contents of this amplifier are substantially lower than normally seen in a Class AB system operating at this power level and having a 4.5-octave bandwidth. All harmonics except the third are attenuated more than 30 dB across the band. Between 20 and 30 MHz, -40 to -55 dB is typical. The third harmonic

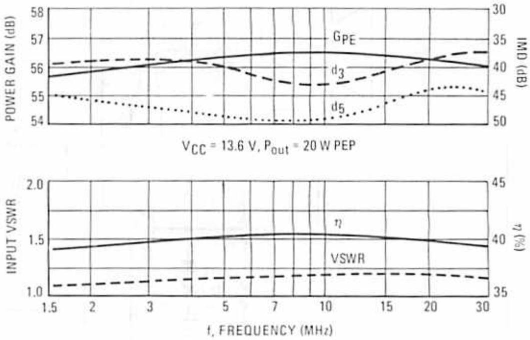

FIGURE 10

Intermodulation Distortion and Power Gain versus Frequency (Upper Curves). Input VSWR and Collector Efficiency (excluding MHW591) (Lower Curves).

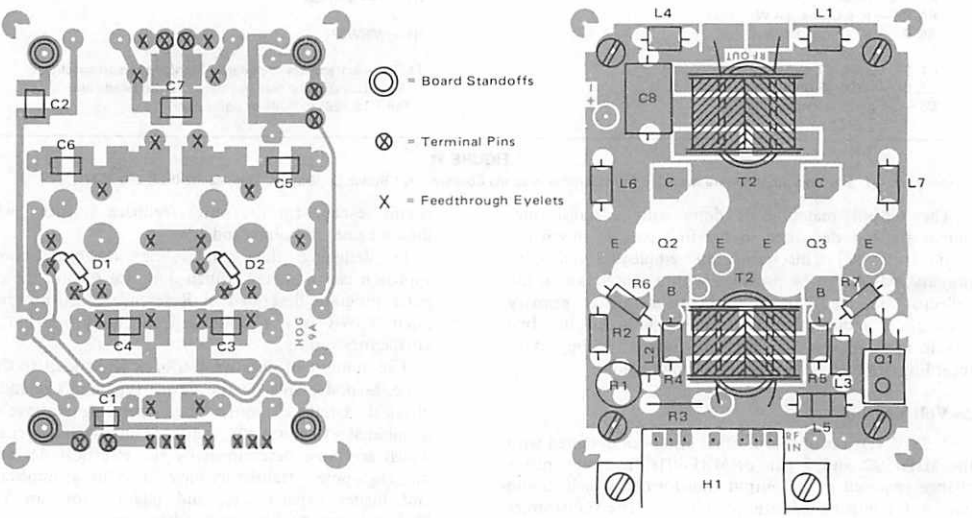

FIGURE 9
Component Layout Diagram of
20 W, 55 dB High-Performance Driver

The leads of D1 and D2 are bent to allow the diodes to contact the transistor mounting flanges.

Note that the mounting pad of Q1 must be connected to the lower side of the board through an eyelet or a plated through-hole.

has its highest amplitude (-20 to -22 dB), as can be expected, below 20 MHz. The measurements were done at an output level of 20 W CW and with 200 mA collector idle current per device. Increasing it to 400 mA improves these numbers by 3-4 dB, and also reduces the amplitudes of d_5, d_7, d_9, and d_{11} by an average of 10 dB, but at the cost of 2-3 dB higher d_3.

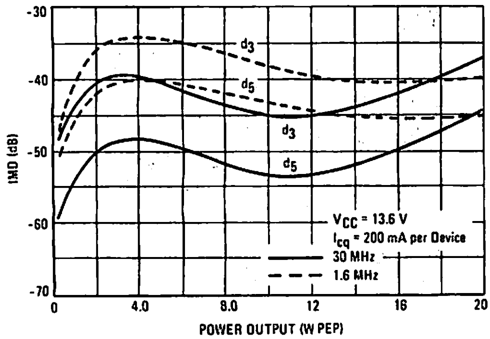

FIGURE 11 — IMD versus Power Output

CONCLUSION

The stability of both designs (excluding the 28 V unit) was tested into reactive loads using a setup described in Reference 8. Both were found to be stable into 5:1 load mismatch up to 7 MHz, 10:1 up to 30 MHz, except the latter design did not exhibit breakups even at 30:1 in the 20-30 MHz range. If the test is performed under two-tone conditions, where the power output varies from zero to maximum at the rate of the frequency difference, it is easy to see at once if instabilities occur at any power level.

The two-tone source employed in all tests consists of a pair of crystal oscillators, separated by 1 kHz, at each test frequency. The IMD (d_3) is typically -60 dB and the harmonics -70 dB when one oscillator is disconnected for CW measurements.

HP435 power meters were used with Anzac CH-130-4 and CD-920-4 directional couplers and appropriate attenuators. Other instruments included HP141T analyzer system and Tektronix 7704A oscilloscope-spectrum analyzer combination.

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6. K. Simons, Technical Handbook for CATV Systems, Third Edition, Jerrold Electronics Corp.
7. Data Sheets, Motorola MRF475, MRF476, MRF433, and MHW591
8. H. Granberg, "Two-Stage 1 KW Solid-State Linear Amplifier," AN-758, Motorola Semiconductor Products Inc.
9. Phillips, "Transistor Engineering," McGraw-Hill.

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The PCB layouts below are a supplement to Figures 5 and 9 and may be used for generating printed circuit artwork.

NOTE: The Printed Circuit Board shown is 75% of the original.

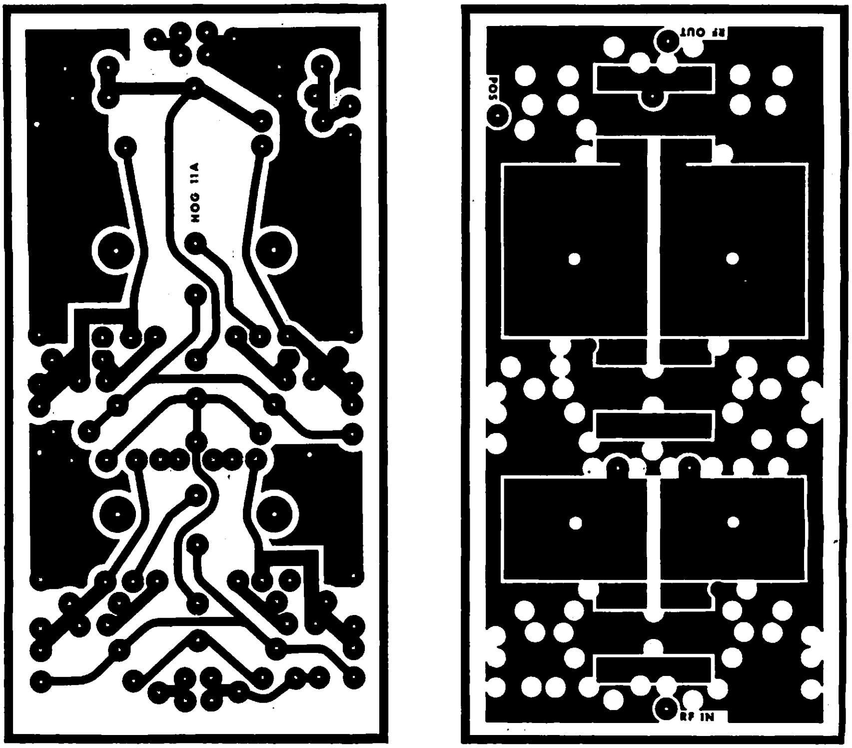

FIGURE 12 — PCB Layout of Low-Cost 20 W Amplifier

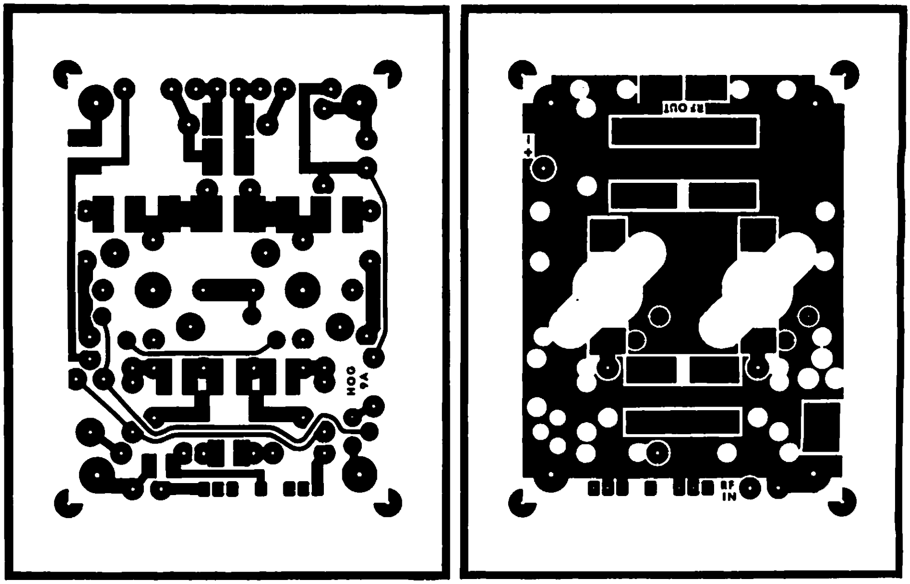

FIGURE 13 — PCB Layout of 20 W, 55 dB High-Performance Driver

THERMAL RATING OF RF POWER TRANSISTORS

Prepared by:
Robert J. Johnsen

Reliability is of primary concern to many users of transistors. The degree of reliability achieved is controlled by the device user because he determines the stress levels applied by his circuit and environmental conditions. This application note will permit the device user to estimate transistor reliability from the circuit designer's point of view, namely power dissipation and case temperature.

Introduction

The temperature-dependent thermal properties of silicon and beryllium oxide have been measured and documented by many laboratories during the last twenty years. Only in rare cases has this information been disseminated by semiconductor device manufacturers to the users. The purpose of this note is to clarify and correct some long-standing industry-wide assumptions which have been commonly maintained about thermal resistance and high temperature derating.

Most manufacturer's data sheets include a single thermal resistance number ($R_{\theta JC}$) and use this number to *calculate a linear* derating constant out to some specified maximum junction temperature. The number cited on the data sheet was probably measured in the 25°C to 50°C range, and assumed constant over the whole range of temperatures up to the maximum specified junction temperature. How often have you calculated a junction temperature from a data sheet, as $T_J = T_A + (\theta_{JC})P_D$? Unfortunately, the thermal resistance of silicon increases by 80% from 25°C to 200°C. The thermal resistance of BeO changes by 30%, if the case temperature goes from 25°C to 100°C. Knowledge of the basic physical properties of the materials and the methods used to calculate and measure thermal resistance will assist the device user in transistor selection and equipment design.

NOTE: °K = °C + 273.

Temperature-Dependent Thermal Properties Of Silicon and Beryllia

The temperature-dependent thermal conductivities of silicon and beryllium oxide are seen in Figures 1 through 3 and Table 1. The temperature ranges are somewhat wider than are necessary for typical transistor operation, but are shown to emphasize the wide variation in thermal conductivities. Fulkerson et al[3] tabulate the values for thermal conductivity and resistivity of silicon from 100°K to 1350°K (see Table 1), and they find that the thermal resistivity of silicon as a function of temperature can be estimated by a linear approximation over the temperature range shown.

(400 - 660°K)

$$1/k = -0.1171 + 2.954 \times 10^{-3}\ T\ (^{\circ}K) \qquad (1)$$

(600 - 1050°K)

$$1/k = -0.9609 + 4.229 \times 10^{-3}\ T\ (^{\circ}K) \qquad (2)$$

A similar least-square fit to Fulkerson's data over the range 200 to 700°K, within 1%, is given by:

(200 - 700°K)

$$1/k = -0.2286 + 3.1683 \times 10^{-3}\ T\ (^{\circ}K) \qquad (3)$$

Similarly for beryllia, one can fit the data of Elston et al[2] over the range of 200 to 800°K, with equation (4).

(200 - 800°K)

$$1/k = 1.943 \times 10^{-5}\ T\ (^{\circ}K)^{1.7} \qquad (4)$$

where k is the thermal conductivity in units of watts/cm°K.

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TABLE 1 — *Smoothed* Data for Thermal Conductivity and Resistivity of Silicon (Ref. 3)

T (°K)	Smoothed ORNL Values k (W cm^{-1} deg^{-1})	W = 1/k (cm deg W^{-1})
100	7.52	0.133
150	3.88	0.258
200	2.44	0.410
250	1.78	0.563
300	1.40	0.716
350	1.15	0.870
400	0.939	1.065
450	0.825	1.212
500	0.736	1.359
550	0.663	1.508
600	0.604	1.656
650	0.555	1.803
700	0.500	1.999
750	0.452	2.210
800	0.413	2.420
850	0.380	2.634
900	0.351	2.845
950	0.327	3.055
1000	0.306	3.268
1050	0.287	3.479
1100	0.273	3.65
1150	0.261	3.82
1200	0.251	3.97
1250	0.245	4.08
1300	0.241	4.14
1350	0.239	4.18

FIGURE 1 — Temperature Dependent Thermal Conductivity of *Silicon* (Ref. 1)

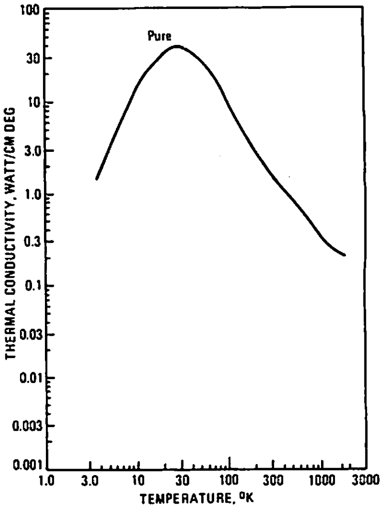


FIGURE 2 — Thermal Conductivity of BeO (Ref. 2)

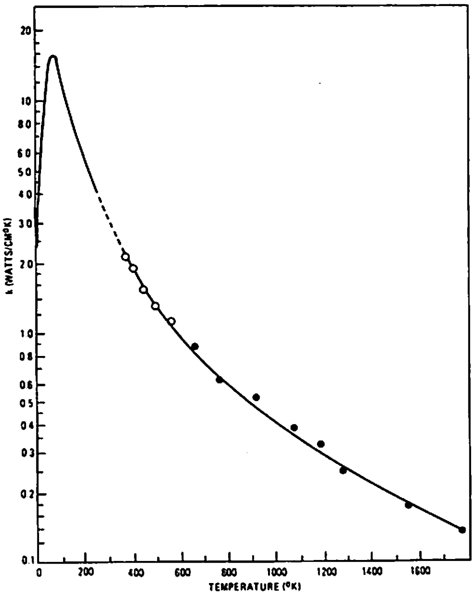
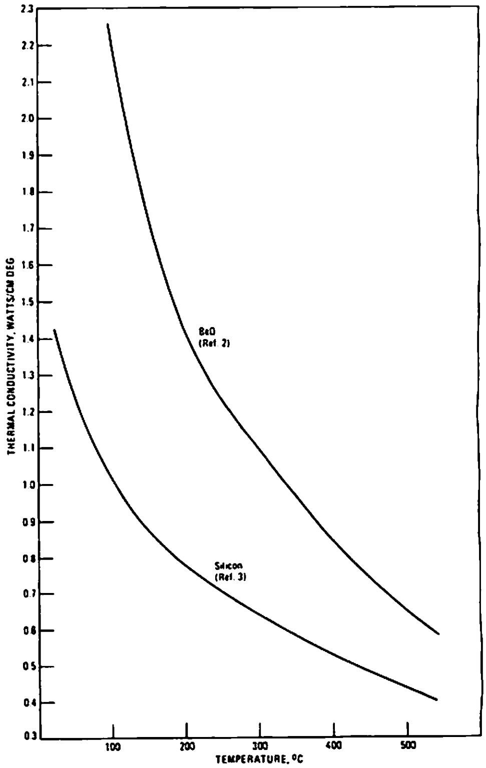


FIGURE 3 — Thermal Conductivity



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Geometric Factors and Thermal Resistance Calculation

The thermal resistance of most silicon RF transistors is controlled by the bulk properties of silicon and beryllium oxide, geometry of the heat generating (base) areas, and the temperature of the heat sink (case). The interfaces generally are well behaved and contribute little to the overall total thermal resistance if the device, die and package elements are assembled and handled properly.

Die temperature calculations are performed in two steps. The first uses the method of Linsted and Surtey[4] to calculate the temperature distribution of a die by using a double Fourier series solution to Laplace's equation. Figure 4 shows the device geometry and some of the boundary conditions. Equation (5) will calculate the temperature rise at any (x,y,z) point in the die, where A,B,C,D,F are die and heat-generating area boundaries. Q is the heat input in watts, and k is the thermal conductivity of the material in watts/cm^{o}K (Linsted's equation).

$$\begin{aligned} T = & -\frac{Q}{K}\left(\frac{CD}{AB}\right)(z-F) \\ & + \sum_{m=1}^{\infty}\left(-\frac{Q}{K}\right)\left(\frac{2BC}{m^2\pi^2 A}\right)e^{m\pi z/B}\left(\frac{1-\exp\left[2m\pi(F-z)/B\right]}{1+\exp\left(2m\pi F/B\right)}\right)\left[\sin\left(\frac{m\pi D}{B}\right)\cos\left(\frac{m\pi y}{B}\right)\right] \\ & + \sum_{n=1}^{\infty}\left(-\frac{Q}{K}\right)\left(\frac{2AD}{n^2\pi^2 B}\right)e^{n\pi z/A}\left(\frac{1-\exp\left[2n\pi(F-z)/A\right]}{1+\exp\left(2n\pi F/A\right)}\right)\left[\sin\left(\frac{n\pi C}{A}\right)\cos\left(\frac{n\pi x}{A}\right)\right] \\ & + \sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\left(-\frac{Q}{K}\right)\left(\frac{4}{\pi^2 mn\gamma}\right)\left(\frac{1-\exp\left[2\gamma(F-z)\right]}{1+\exp\left(2\gamma F\right)}\right) \\ & \cdot e^{\gamma z}\sin\left(\frac{n\pi C}{A}\right)\sin\left(\frac{m\pi D}{B}\right)\cos\left(\frac{n\pi x}{A}\right)\cos\left(\frac{m\pi y}{B}\right) \end{aligned} \tag{5}$$

where

$$\gamma^2 = \pi^2\left[\left(\frac{n}{A}\right)^2 + \left(\frac{m}{B}\right)^2\right]$$

The Fourier series solutions are amenable to computer calculation and converge adequately within ten to twenty terms. Figure 5 shows the treatment of multiple base cell transistors. Lines of symmetry between adjacent base cells are considered to be adiabatic die boundaries as assumed by Lindsted. The power dissipated is assumed to be equally shared among the several base cells. The result of this calculation is the temperature rise of the silicon chip, assuming a constant thermal resistance for bulk silicon. The same model is used to calculate the temperature rise for the beryllia piece, using the silicon die area as the power dissipating area for the beryllia, again assuming the thermal resistance of the beryllia as a constant. The thermal resistances of the silicon die and the beryllia substrate are in series, so adding the above numbers gives a value for the thermal resistance of the device at a particular temperature and a power level low enough to avoid the effects of the temperature variations of the respective thermal resistances.

The second step in the thermal resistance calculation takes into account the temperature-dependent thermal resistivity. The calculated thermal resistance of the beryllia piece (from the previous section) is mathematically divided into fifty layers, each with 1/50 of the total BeO thermal resistance. The first layer at the bottom is assumed to have its temperature at the heat-sink ambient with its thermal resistance value corrected to the proper temperature using the equations for the temperature-dependent resistivity. The power flux through the first layer then leads to its temperature rise, and this new temperature determines the thermal resistivity value for the second layer. Its temperature rise is calculated, and so on, until the result for the top surface of the fiftieth layer gives the temperature rise above the ambient for the beryllia piece.

The same method is used for the silicon die, using the beryllia top surface temperature as the starting point, and correcting the thermal resistance of each of fifty layers based upon the temperature of the layer directly beneath it, until the top surface of the silicon die result gives the calculated die temperature for that particular case of ambient temperature and power dissipation. The results of these calculations indicate that the thermal resistance of a given device is not a constant number, but is a function of the dissipated power and the ambient (case) temperature. Another result is that the junction temperature of a device dissipating power will rise more than 1^{o}C for a 1^{o}C rise in ambient temperature, because of the increase in thermal resistance. Figures 6 through 9 show the calculated thermal resistance and die temperature for several different devices as a function of ambient temperature and power dissipation.

FIGURE 4 — Model for Heat Flow

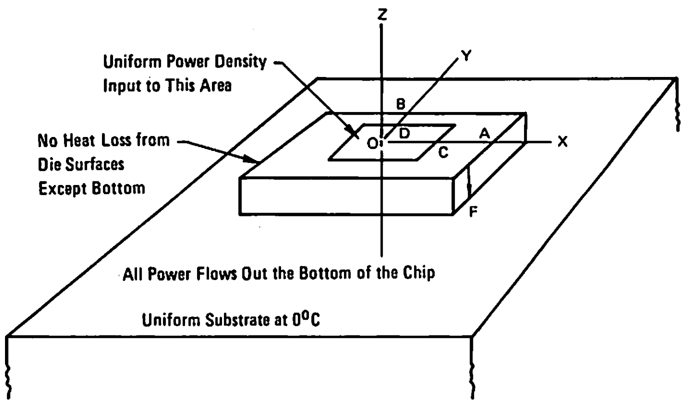


FIGURE 5 — Array of Base Areas in a Silicon Die

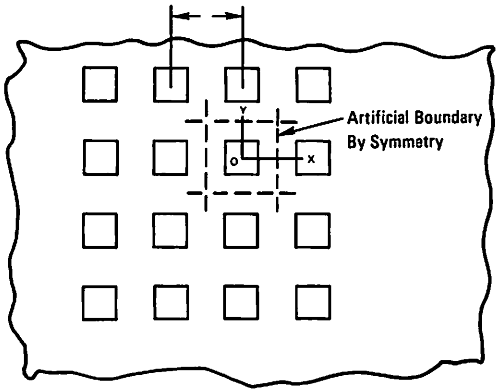


FIGURE 6 — Junction Temperature and Thermal Resistance as a Function of Power Dissipated, Flange (Heat Sink) Temperature

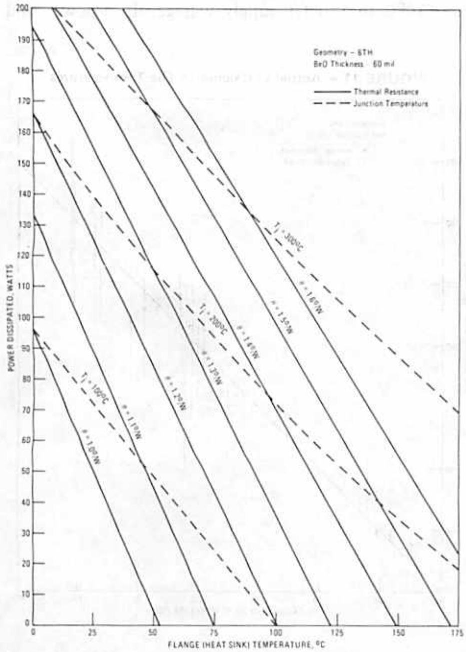


FIGURE 7 — Junction Temperature and Thermal Resistance as a Function of Power Dissipated, Flange (Heat Sink) Temperature

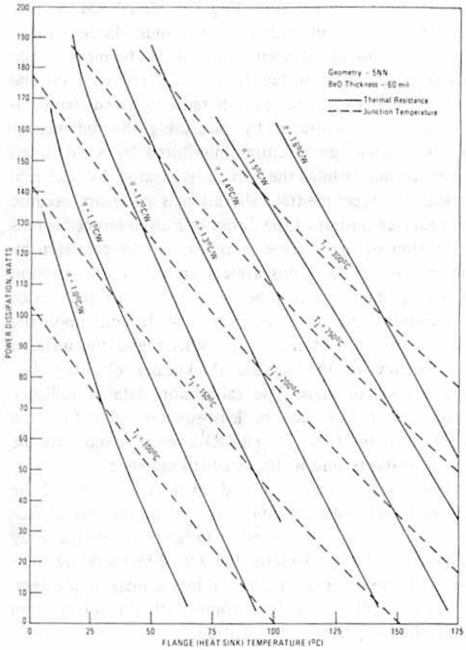


FIGURE 8 — Junction Temperature and Thermal Resistance as a Function of Power Dissipated, Flange (Heat Sink) Temperature

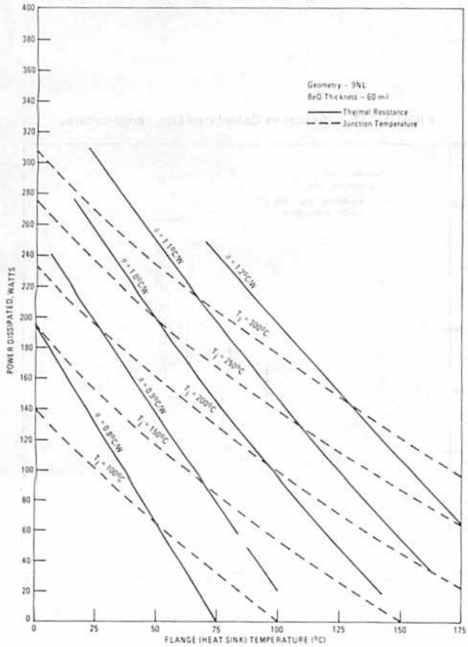
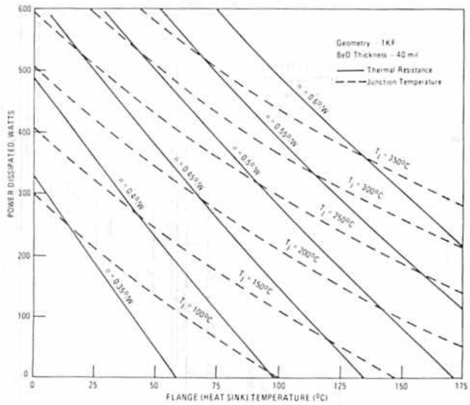


FIGURE 9 — Junction Temperature and Thermal Resistance as a Function of Power Dissipated, Flange (Heat Sink) Temperature



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Experimental Verification Of Calculated Die Temperature

Actual temperature measurements are made with an infrared microscope, Barnes Eng. Co. Model RM2A. This instrument uses an indium antimonide diode photo-detector at liquid nitrogen temperatures to measure the infrared radiance emitted from a 1.5 mil spot on the surface being examined. The IR radiance versus temperature curve is calibrated by measuring the radiance at various known temperatures monitored by a calibrated thermocouple while the device is heated by external means. An experimental calibration is necessary because the radiance output of the device at a given temperature is a function of the average emissivity in the area seen by the microscope, and this average emissivity is a function of the geometry and processing history of the device in question. The effective emissivity depends upon the relative amounts of metal and silicon and the infrared transparency of the varying thicknesses of SiO_2 glass in the field of view. The calibration data of radiance versus temperature can be least-squares curve fit to an equation of the form $T = (A)(R)^b$, where A and b are the fitted constants, and R the measured radiance.

The device is then powered up in its circuit, and the radiance data collected point-by-point around the surface of the silicon die. A computer program inputs the array of radiance data, calculates the actual temperature from the calibration equation, and prints a map of the temperature profile, as well as some statistical information about the temperature distribution.

Figures 10 through 12 are plots showing the correlation of measured to calculated temperature for several geometries, under various conditions of flange temperature (30°C to 150°C), supply voltage, drive power, and

FIGURE 11 — Actual vs Calculated Die Temperatures

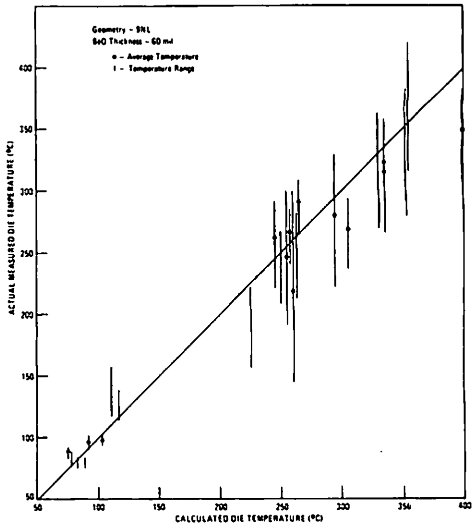


FIGURE 10 — Actual vs Calculated Die Temperatures

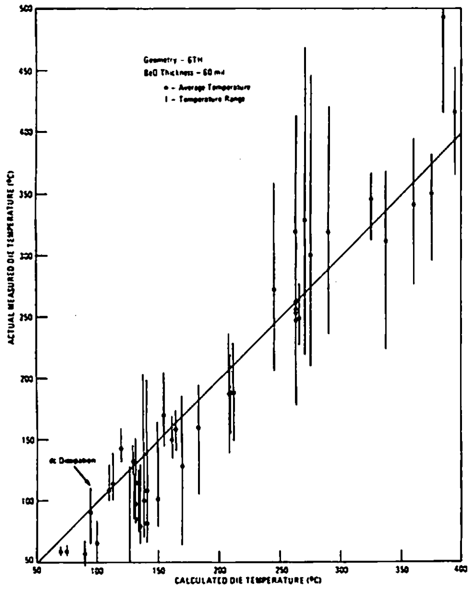
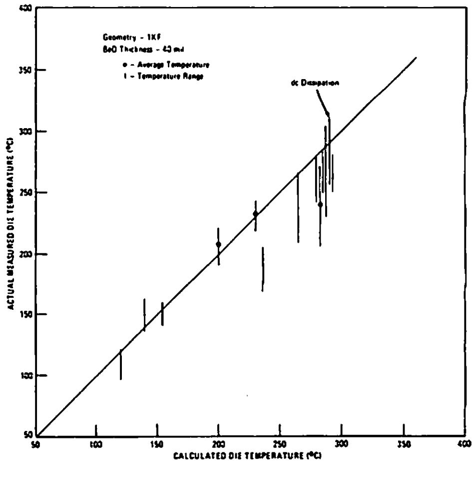


FIGURE 12 — Actual vs Calculated Die Temperatures



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output load magnitude and phase angles from 50 Ω to over 30:1 VSWR. The calculated temepratures seem to be somewhat higher than measured at the higher power levels. The calculated temperatures are based on the calculated power dissipation, disregarding RF losses in the actual loads and circuits.

Metal Migration and Mean Time to Failure

The calculated/observed temperature agreements are seen to be close enough so that the calculated temperature can be used as the basis for reliability calculations of Mean Time Before Failure (MTBF) for metal migration based upon Black's[5] work.

$$\mathrm{MTBF} = \frac{(\text{cross section})^3}{I^2 \cdot f(T^o)} \tag{6}$$

Equation (6) is the equation used for calculating metal migration lifetime, where the cross section refers to the conducting stripe dimensions in cm^2, and I is the current in the stripe in amps. $f(T^o)$ is an Arrhenius function of the stripe material, having the form:

$$f(T^o) = B \exp(-\phi/KT) \tag{7}$$

The material dependent parameters B and ϕ are shown in Table 2. K is Boltzman's constant, and T is in degrees Kelvin. A series of graphs (Figures 13 through 16) have been constructed, one for each device, that present the results of the calculations of device temperature and MTBF as a function of power and ambient temperature.

The temperature lines are valid for any combination of supply voltage, efficiency and drive power, by reading the power axis as power dissipated. The MTBF lines, because of the current dependence, have been constructed based upon the assumptions of 12.5-volt supply and 50% efficiency, so that the power axis should be interpreted as output power. It is possible to use the MTBF set of lines at other conditions. Enter the graphs by reading the power output parameter as power dissipated, and find the MTBF, then scale the MTBF by the ratio square of the $\eta = 50\%$ current to the actual current.

$$\mathrm{MTBF} = \mathrm{MTBF}\ (\text{from graph}) \times \left(\frac{I\ @\ \eta = 50\%}{I\ \text{actual}}\right)^2 \tag{8}$$

TABLE 2 — Material Dependent Parameters

Material	B	ϕ
Large Crystal Glassed Al (Ref. 5)	8.5×10^{-10}	1.2
Al-2% Cu Alloy (Ref. 6)	7.9×10^{-17}	0.6

FIGURE 13 — Metal Migration — MTBF

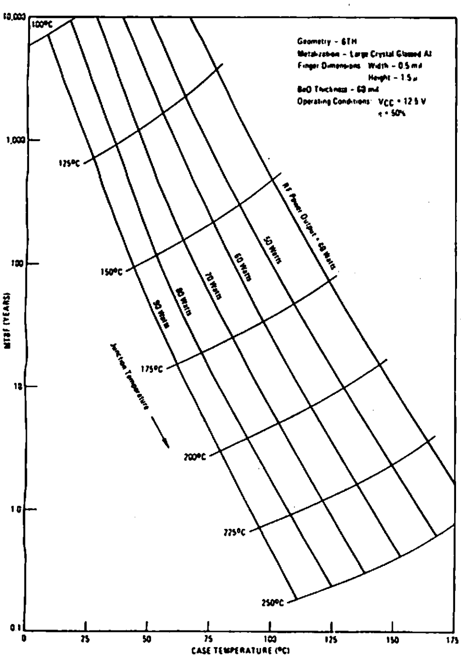

FIGURE 14 — Metal Migration — MTBF

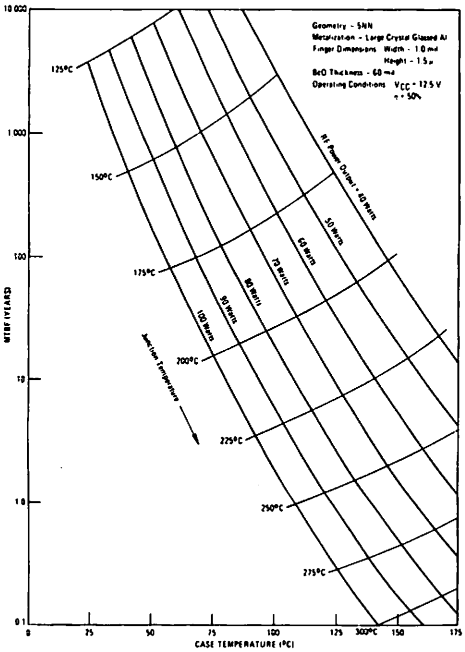

FIGURE 15 – Metal Migration – MTBF

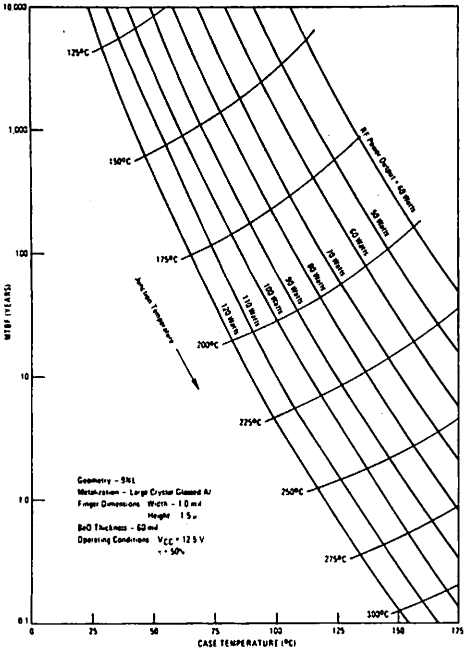

FIGURE 16 – Metal Migration – MTBF

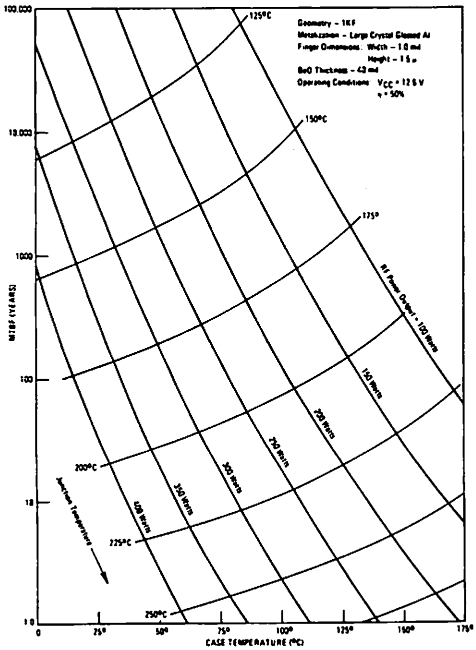

FIGURE 17 – Geometry Code to Standard Part Cross-Reference

Geometry Code	12.5	28		50	V_{CC} (V)
	Al	Al	Au	Al	Metal
1KF	MRF421	MRF422		MRF428A	
5NN	MRF243 MRF453/A MRF455/A MRF460		MRF316		
9NL	MRF245 MRF454/A	MRF463 MRF464/A	MRF317		
6TH	MRF648		MRF327 MRF328		

To Scale Metal Migration MTBF
From 12.5 V to Other Operating Voltages

Keeping P_D and η constant, then the current for 28 V operation compared with that for 12.5 V operation is given by:

$$I_{12.5} \times 12.5 = I_{28} \times 28$$

$$\frac{I_{12.5}}{I_{28}} = \frac{28}{12.5}$$

From Black's[5] equation:

$$MTBF \propto \frac{1}{I^2}$$

For like geometries, the ratio of the MTBF at 28 V to the MTBF at 12.5 V is:

$$MTBF_{28} = MTBF_{12.5} \times \frac{28}{12.5}^{2}$$

$$MTBF_{28} = MTBF_{12.5} \times 5.02$$

Similarly, for 50 V operation:

$$MTBF_{50} = MTBF_{12.5} \times 16.$$

Conclusion

We have discussed the elements of thermal resistance and metal migration lifetime with particular attention paid to their variation with temperature as functions of power dissipation and ambient temperature.

Graphical presentations of the results are included which should be useful to the device user who is interested in better reliability in his application.

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7

A SIMPLIFIED APPROACH TO VHF POWER AMPLIFIER DESIGN

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This note discusses the design of 35-W and 75-W VHF linear amplifiers. The construction technique features printed inductors, the design theory of which is fully described. Complete constructional details, including a printed circuit layout, facilitate easy reproduction of the amplifiers.

Solid-state VHF amplifier design can be simplified by employing printed or etched lines for impedance matching. The lines, having a distant ground-plane reference and high Z_O, can be treated as lumped constant inductors, and make design and duplication easier than with wire-wound inductors.

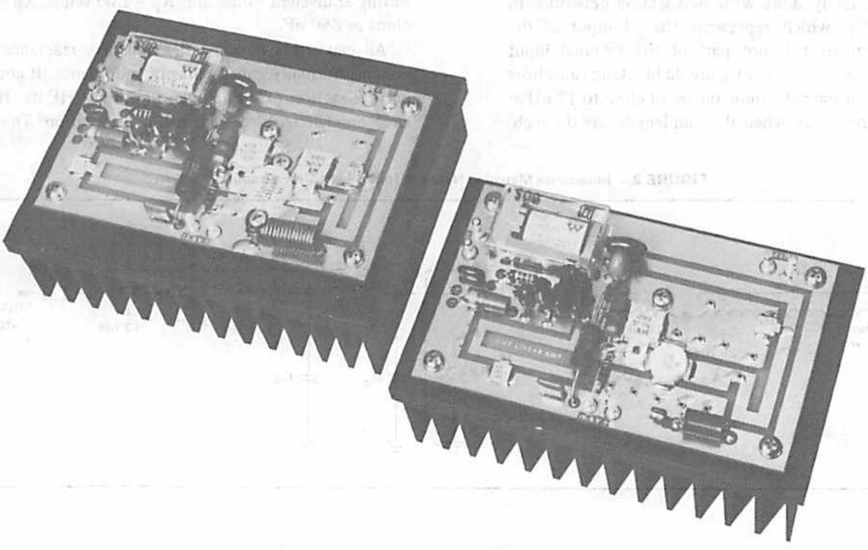
An example is an optimized 35-W amplifier which yields over 10 dB of power gain across the 2-meter amateur band. It employs an inexpensive, non-internally matched transistor, the MRF240, which has good linear characteristics for SSB operation.

A higher power version with the same board layout is concentrated around the MRF247, although this results in some compromise in the impedance matching.

A carrier operated T/R switch (COR) is incorporated, allowing applications such as a booster amplifier for hand-held and mobile radios.

Both designs are biased class AB for linear operation, but are suitable for FM operation as well. Figure 1 shows the two amplifiers.

FIGURE 1 — 35-watt and 75-watt Engineering Models



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GENERAL

VHF solid state amplifier design is almost exclusively done with lumped constant LC matching networks. Broadband transformer matching is feasible when extremely wide bandwidths are required. Transmission lines for impedance transformation usually require quarter-wave electrical lengths and make designs bulky at VHF unless materials with high dielectric constant are used. Transmission lines can be realized with coaxial cable or printed lines (strip-lines) on a circuit board with a continuous ground plane, separated by a suitable dielectric material. The printed airlines discussed here are, in fact, high characteristic impedance transmission lines which, for the purposes of design calculation, are treated as inductors; therefore the quality of the board material is less critical. The printed airlines also have the advantage of repeatability and easy access for designing multi-element networks. The network calculations can be done in the same manner as if lumped-constant, round-wire inductors were used.

Input and output impedance matching in transistor amplifiers is required to transform the source impedance (usually 50 ohms) to the low complex input impedance of the device. The output load impedance, which is a function of the supply voltage and power level, must also be matched to a 50-ohm load except in multistage driver designs.

At VHF, the input and output impedances of a power transistor are both usually inductive in reactance (designated as +JX in data sheets), becoming capacitive (-JX) at lower frequencies. For transistors such as MRF240, 2N6084 and 2N5591, the crossover point is around 100 MHz. This is determined by the transistor die size, geometry and package type, and smaller devices can be capacitive up to UHF frequencies.

Since the bandwidth required here is only a fraction of an octave, (140-150 MHz) the impedance matching can be adequately done with two section networks. In Figure 2, X_1, which represents the +J input of the MRF240 transistor is not part of the external input matching network. C_1 and C_6 are dc blocking capacitors with measured parasitic inductances of close to 12 nH at the center frequency when the lead lengths are 0.1 inch. These inductances, as well as the relay inductance, are added to the values of L_1 and L_5.

If the relay were used in a 50-ohm system, it would result in 0.3 dB power loss due to impedance mismatch and losses. This can be minimized if the relay inductance is used as part of a resonant circuit, but the series inductance (37 nH per contact pair) obviously places an upper frequency limit.

The simplest approach to matching network design is with a purely resistive source and load. This can be accomplished by compensating the +J with an equal amount of capacitance (–J). C_3 and C_4 are used to accomplish the compensation in Figure 2. This is not always practical, however, especially when maximum bandwidths are required. In this case, only part of the inductive component may be cancelled, leaving the base and collector still inductively reactive. In either case, it may be considered that part of the impedance-matching occurs within the device package itself; this is more obvious with internally matched devices, which are discussed later.

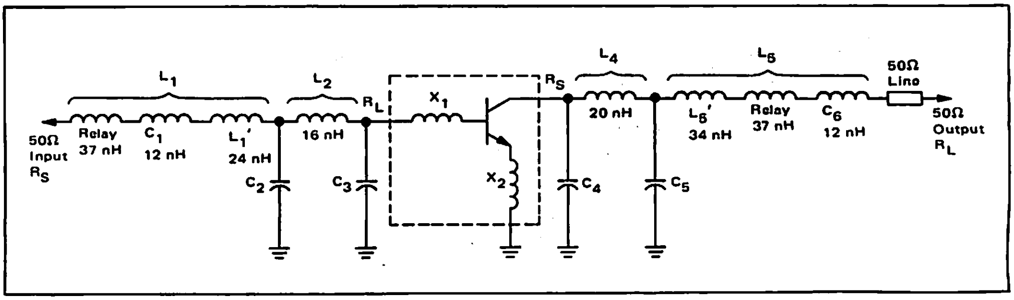
35-W LINEAR AMPLIFIER

The MRF240 was chosen for this application due to its ruggedness against load mismatch and inherently high power gain for a non-internally matched device. The transistor is rated for an output power of 40 W and a power gain of 8 dB at 175 MHz. A typical power gain at 145 MHz is 10 to 11 dB. At this frequency the input and output impedances of the MRF240 are 0.6 +J 0.8 ohms and 2.0 +J 0.1 ohms respectively (P_{out} = 35 W).

Before designing the matching networks, the values of C_3 and C_4 must be established to cancel the inductive reactance components at the base and the collector. For the input, the series numbers 0.6 +J 0.8 must be converted to parallel equivalent values, either by using a Smith chart or equations in references 3 and 4. The resulting equivalent values are: R_P = 1.67 ohms, X_P = 1.25 ohms or 880 pF.

All capacitors have a series inductive reactance component, normally called parasitic inductance. It could be only a fraction of a microhenry, but at VHF its effect is large enough to be taken into consideration. The para-

FIGURE 2 — Impedance Matching Network for 35 watt VHF Amplifier



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sitic inductance results in an increased effective value of capacitance, and is frequency and impedance-level dependent.

The unencapsulated mica capacitors, widely used in VHF power applications, range from 1 to 2 nH in parasitic inductance for a single plate type, (up to 360 to 390 pF nominal values) depending on the mounting technique. Assuming a parasitic inductance of 1.5 nH, the equivalent low-frequency value can be calculated with Equation 1 as:

$$C_{Equiv} = \frac{C}{1 + [(2\pi f)^2 \; LC] \; 10^{-9}} \qquad (1)$$

where C = effective capacitance required in pF
L = parasitic inductance in nH
f = frequency in MHz

Substituting the values in equation (1):

$$C_{Equiv} = \frac{880}{1 + [(910)^2 \times 1.5 \times 880] \; 10^{-9}} = 420 \text{ pF}$$

Thus, for the required 880 pF, a capacitor of this type with equivalent low-frequency value of 420 pF, or the closest standard (390 pF), should be used.

Similarly, converting the output impedance (2.0 +J 0.1 ohms) to parallel form, R_P = 2.01 ohms and X_P = +J 26.8 ohms. The X_C represents a capacitance value of 47 pF for C_4 (from Equation 2), or a 43 pF nominal value.

$$C = \left(\frac{1}{\frac{X_C}{2\pi f}}\right) 10^6 \qquad (2)$$

where X_C = capacitive reactance in ohms
C = capacitance in pF
f = frequency in MHz

This high reactance in parallel with the low collector impedance had no noticeable effect and was completely omitted in later functional tests of the unit. It would be easy to see from a Smith chart that the resistive components of 1.67 ohms and 2.01 ohms remain unchanged, and can be treated as a purely resistive load and source for the matching network calculations.

At high frequencies the base-emitter impedance of the transistor die itself is always lower than the collector output impedance. With power devices, both can be only a fraction of an ohm. The input impedance is increased by the base and emitter bonding wire and package lead frame inductances, which are effectively in series with the transistor base (Figure 2, X_1 and X_2). The collector has normally much less series inductance since it is attached directly to the package bonding pad.

From this it can be seen that part of the matching network is actually built into the transistor package, and it is obvious that the amplifier bandwidth cannot be accurately determined by calculating the Q values of the external matching networks. (See the discussion of a 75-W linear amplifier.)

As an approximation, the 3 dB bandwidth can be used to obtain a starting point. Assuming a 15 MHz bandwidth at ±1.5 dB is desired at 145 MHz center frequency, a loaded Q of approximately 9 is required. For simplicity this number is applied to both input and output network design.

In Figure 2, X_1 and X_2 represent the inductive impedance component of the transistor and are shown only to give an idea of the transistor internal structure. The values of L_1, L_2 and C_2 can be obtained from the Appendix, or calculated by using Equation 3:

$$XL_1 = R_S B$$

$$XL_2 = R_L Q$$

$$XC_2 = \frac{A}{Q + B} \qquad (3)$$

$$A = R_L (1 + Q^2)$$

$$B = \sqrt{\frac{A}{R_S} - 1}$$

where R_S = source impedance
R_L = load impedance

For Q = 9:

$$XL_1 = R_S B = 50 \times 1.32 = 66 \text{ ohms}$$

$$XL_2 = R_L Q = 1.67 \times 9 = 15 \text{ ohms}$$

$$XC_2 = \frac{A}{Q + B} = \frac{137}{9 + 1.32} = 13.3 \text{ ohms}$$

$$A = 1.67 (1 + 9^2) = 137$$

$$B = \sqrt{\frac{A}{50 - 1}} = 1.32$$

where R_S = 50 ohms, R_L = 1.67 ohms

Since $$L = \left(\frac{XL}{2\pi f}\right) 10^3 \qquad (4)$$

where XL = inductive reactance in ohms
L = inductance in nH
f = frequency in MHz

we have from Equations 3 and 4:

L_1 = 73 nH
L_2 = 16 nH
C_2 = 82 pF

Subtracting the relay inductance (37 nH) and the parasitic inductance of the blocking capacitor C_1 (12 nH) from the total value of L_1, $L_1' = 24$ nH. This means the total printed line inductance must be $L_1' + L_2 = 24 + 16 = 40$ nH.

Calculating the values of the output network in a similar manner, the values for L_4, L_5 and C_5 are obtained as 20 nH, 83 nH and 70 pF, respectively, and L_5' becomes 34 nH.

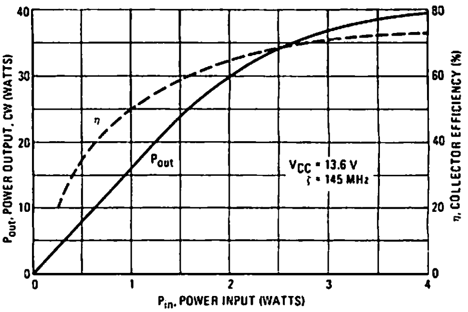
The capacitors employed for C_2 and C_5 are of the same unencapsulated mica type as C_3, but smaller in size, and their parasitic inductance is only about 1 nH. The equivalent values for C_2 and C_5 would then be 77 pF and 66 pF according to Equation 1. These are nonstandard values, and considering a 5% tolerance, a 68 pF marked value can be used for both.

Inductors L_1, L_2, L_4 and L_5 are comprised of etched lines on the circuit board. To determine their widths and lengths, the inductance of each line per unit length must be established. From the tables in the Reference section, it can be extrapolated that the inductance of #25 round wire is 24 nH per inch and #26 wire nearly 26 nH per inch. When a ground plane is 0.15 inch below, which in this case is the heat sink, and the side grounds are off an equal distance, the inductance is about one-half of this, which has been verified by measurement.

If the circuit board is made of 1-ounce, copper-clad material, (one ounce of copper per one square foot) the copper thickness is 1.4 mils. With a one mil solder plating, the total thickness is 2.4 mils, and a 100-mil-wide strip would be equivalent to a #26 round wire having a 240 square mil cross sectional area. Similarly, a 130-mil-wide strip would be equivalent to a #25 round wire with 312 square mil area. A wider line would have lower losses but would also be physically longer for a given inductance. As a compromise, a narrow line was used for the input in this design, and a wider line for the output, where the losses due to the high RF currents are more evident. Bends in the line have a minimal effect to the inductance compared to the presence of the ground plane.

From the above, the resulting inductances for the 100 mil and 130 mil lines are 13 nH per inch and 12 nH per inch, respectively. This means that for $L_1 + L_2$ a total length of 3.1 inches is required, and 4.4 inches for $L_4 + L_5'$. Then, for $L_2 = 16$ nH, C_2 should be located 1.3 inches from the transistor base along the input line. For $L_4 = 20$ nH, C_5 should be 1.6 inches from the collector along the output line. The Power Output and Efficiency vs. Power Input of the 35-W amplifier is shown in Figure 3.

FIGURE 3 — Power Input vs. Power Output and Collector Efficiency of 35-W Amplifier

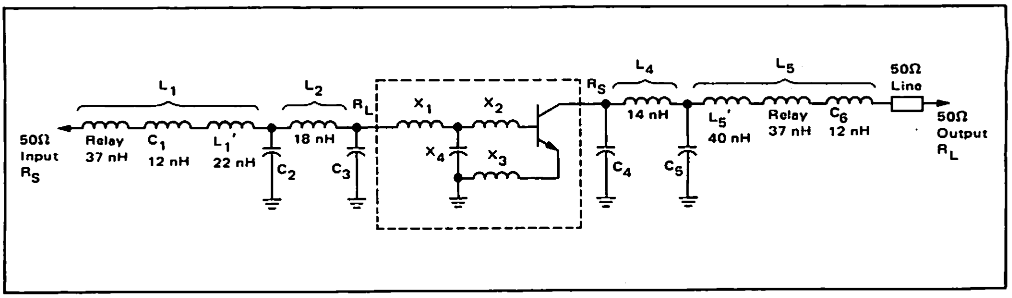


75-W LINEAR AMPLIFIER

The MRF247 employed in this design is a version of the well-known MRF245, which has been reprocessed to improve the linear characteristics. It is a much larger device than the MRF240, resulting in lower input and output impedances. However, it employs internal base matching with a built-in MOS capacitor to bring the base impedance up to a level where external low loss matching networks can be realized.

In Figure 4 the dashed line encircles the specially designed T matching network, including the metal oxide capacitor X_4. X_1, X_2, and X_3 represent the bonding wires whose inductances can be varied by controlling the loop heights. This network will be part of the total matching network designed to match the transistor to function in a practical circuit.

FIGURE 4 — 75-Watt Amplifier Impedance Matching Network



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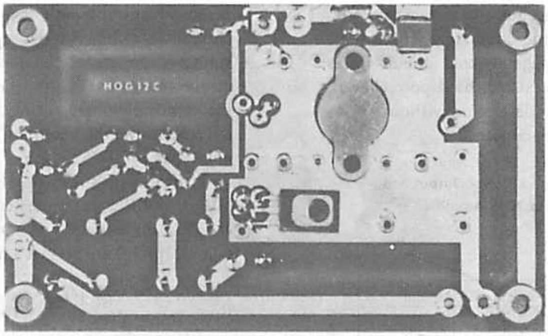
Underside View of 75-W Amplifier



The internal matching still leaves the input impedance inductively reactive.

The MRF247 input impedance under forward biased conditions (100 mA) is 0.45 +J 0.85 ohms at 145 MHz, which translates to 2.06 +J 1.08 ohms in parallel form. A capacitive reactance of -J 1.08 ohms, converting to 1018 pF is required for C_3. The nominal value equivalent value, using Equation 1, is obtained as 450 pF.

Since the remaining resistive component of the base impedance (2.06 ohms) is only slightly higher than that of the MRF240, only minor changes in the input matching network are necessary. When $L_1 + L_2$ is fixed, and only their ratio can be varied, the resulting Q will be lower for the increased R_L. If only $L_1 + L_2$ is known, the Q can be calculated with Equation 5 as:

$$Q = \frac{\left[4X_T^2 + (R_S^2/R_L + X_T^2/R_L - R_S)\,4(R_S - R_L)\right]^{1/2} - 2X_T}{2(R_S - R_L)} \qquad (5)$$

where

$X_T = XL_1 + XL_2$ or $XL_4 + XL_5$

R_S = source impedance
R_L = load impedance

Reverse for output network calculations

Therefore,

$$Q = \frac{\sqrt{[26244 + (1214 + 3185 - 50)(192)]} - 162}{95.88}$$

$$Q = \frac{928 - 162}{95.88} = 7.99$$

$$Q = 8$$

where

$X_T = XL_1 + XL_2 = 81$ ohms

RS = 50 ohms

RL = 2.06 ohms

Then, with Equations 1, 2, 3 and 4, the values for L_1, L_2 and C_2 can be calculated as: L_1 = 71 nH, L_2 = 18 nH, C_2 = 63 pF (56 pF nearest standard). The position of C_2 will be approximately 1.6 inches from the transistor base. (See line inductance calculations in the discussion for the 35-watt amplifier.)

The measured output impedance of MRF247 is 0.65 +J 0.45 ohms, which is much lower and more reactive than the values shown for MRF240. The output matching must also be done with the existing total line inductance, $(L_4 + L_5)$ and it can be expected that a higher factor of compromise in the output matching is evident regarding the network bandwidth.

The above impedance numbers convert to 0.96 ohms resistive and -J 1.39 ohms reactive in parallel form. Since -J 1.39 ohms = 790 pF, a nominal value of 400 pF (C_4) is required at the collector. To find the Q:

$X_T = 94$ ohms $(XL_4 + XL_5)$

$R_S = 0.96$ ohms

$R_L = 50$ ohms

Then:

Q = 13.7 (Eq. 5), and:

L_4 = 13 ohms = 14 nH

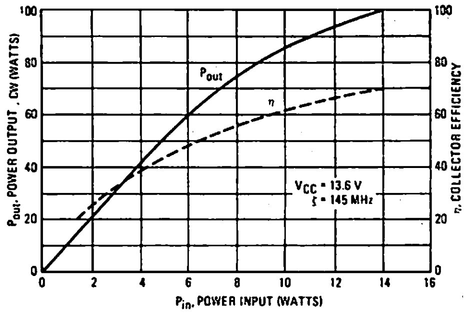
L_5 = 81 ohms = 89 nH

C_5 = 11.8 ohms = 93 pF

A practical value of 82-91 pF can be used for C_5, and it should be located 1.1 inches along the output line from the collector, to give the above inductance values for L_4 and L_5.

Although the output Q is higher than the value calculated earlier for the 40 W unit, the total bandwidth of this version is increased as shown in Figure 7. The input matching network is usually dominant in determining the total bandwidth since the impedance transformation required is greater than the output requires, although the output circuit also has secondary effect. The internal matching elements of the device further make the total effective Q even lower than the calculated value, which in this case was 8. The higher output Q usually results in higher collector efficiency and better harmonic suppression, but at the same time the circulating RF currents will increase, resulting in higher overall circuit losses which is especially noticeable at increased power levels. These factors are difficult to determine without knowing all the internal transistor parameters.

FIGURE 5 — Power Input vs. Power Output and Collector Efficiency of 75-W Amplifier



CLASS AB BIASING AND OTHER CONSIDERATIONS

The biasing system, as seen in Figure 6, uses a forward biased transistor, Q_2, to provide a voltage source of 0.6 to 0.7 volts. When the collector is connected to the base, a second current path is formed, decreasing the base current according to the h_{FE}, and thus lowering the voltage drop across the base-emitter junction. In this manner the voltage drop can be adjusted by selecting the appropriate h_{FE} for Q_2. For the 2N5190 series h_{FE} is typically in the range of 80-100, although the minimum spec is 20-25.

Typical h_{FE}'s for the MRF240 and MRF247 are 50-60, and the worst case collector currents around 4A and 9A respectively. The minimum base currents required, $I_E(Q_2)$ are 80 mA and 180 mA (I_C/h_{FE}).

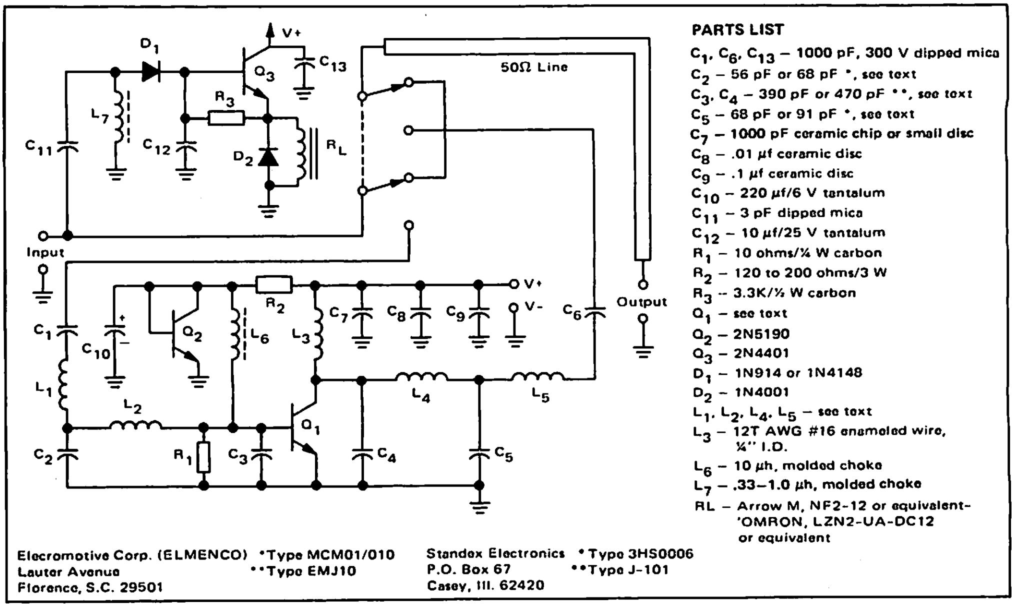
$$R_2 = \frac{V_{CC} - V_{BE}(Q_2)}{I_E(Q_2)} = 160 \text{ ohms and } 75 \text{ ohms.}$$

The bias, which should not exceed 50 mA for MRF240 and 150 mA for MRF247, can be further adjusted by varying the value of R_2, but the minimum $I_E(Q_2)$ should be maintained.

It should be noted that since Q_2 is attached to the heat sink for temperature tracking purposes, its collector must be electrically isolated from the ground. The anodized surface of the heat sink is normally sufficient, or a separate insulating washer can be employed.

The 0.3 dB relay insertion loss mentioned earlier amounts to a VSWR of 1.7:1. However, the reflected power is only 0.2% (VSWR = 1.1:1) in a straight-through mode (receive), indicating that most of the relay losses are due to contact resistance and the dielectric insula-

FIGURE 6



tion resistance, rather than impedance mismatch.

Both amplifier designs may be employed in FM applications without modification. The bias networks may be omitted and L_6 connected to ground, which modifies the operation to Class C. The increased input impedance of the device operating class C results in increased input VSWR, but it will still remain less than 1.5:1 for the 145–150 MHz band.

FIGURE 7 — IMD vs. Power Output

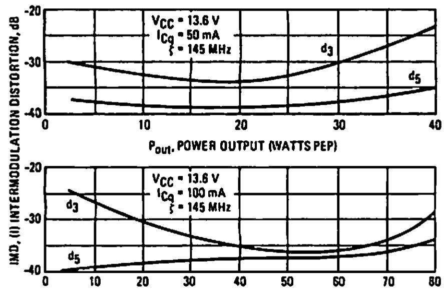
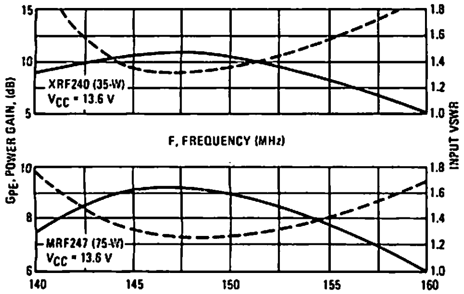


FIGURE 8 — Power Gain and VSWR vs. Frequency



The two amplifiers may be connected in cascade to provide a total power gain of around 20 dB; however, an attenuator of 4 to 6 dB is required between the two units to prevent overdrive of the MRF247. Since 10 to 20 watts will be dissipated in the attenuator, it cannot be built from discrete resistors. Most convenient, size and costwise, are the thin film attenuators such as those manufactured by Pyrofilm.

The COR circuit requires 400 to 500 mW for the relay to switch. At this drive level, without the attenuator, the second amplifier would already produce full power output.

The COR (Figure 5) incorporates one of the standard circuits popular with mobile add-on amplifiers. Part of the RF input signal is being rectified by D_1. The dc turns on Q_3 which activates the relay. L_7 and R_3 provide the bias for D_1 and Q_3, and D_2 suppresses inductive transients produced by the relay coil inductance. A time constant for SSB operation is provided by C_{12}, whose value can be changed according to individual requirements. For FM this capacitor can also be omitted along with the bias network.

The repeatability of these amplifiers has been proven by constructing more than half a dozen units. Capacitors C_2 and C_5 were simply located within the marked areas on the circuit board (see Figure 9 and the photograph). On these capacitors, 20% tolerances can be allowed, but this may result in adjustments of each individual unit for optimum performance.

References

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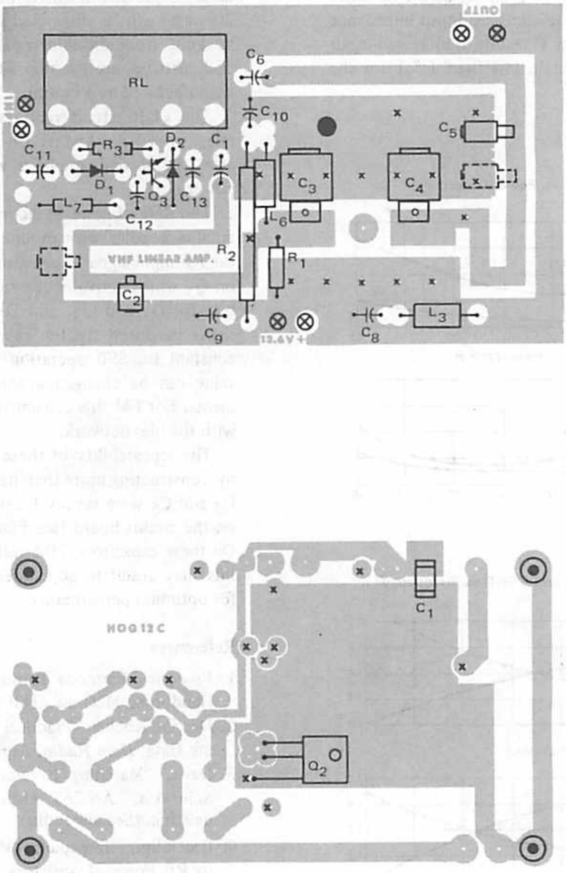
2. Donald Kochen, Practical VHF and UHF Coil Winding Data, *Ham Radio,* April 1971
3. Davis, "Matching Network Design with Computer Solutions," AN-267, Motorola Semiconductor Products Inc. (See appendix).
4. Becciolini, "Impedance Matching Networks Applied to RF Power Transistors," AN-721, Motorola Semiconductor Products Inc.

FIGURE 9 – Component Layout Diagram of 35W and 75W Amplifiers

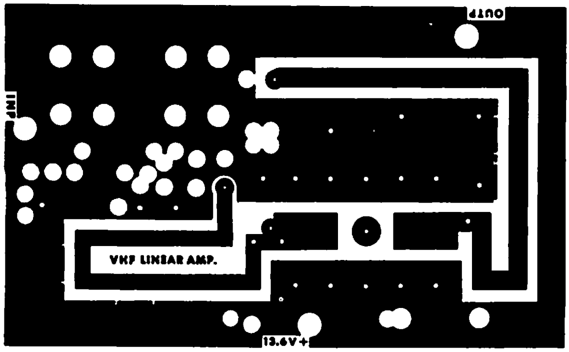


× DENOTES FEED THROUGH EYELETS OR PLATED THROUGH HOLES

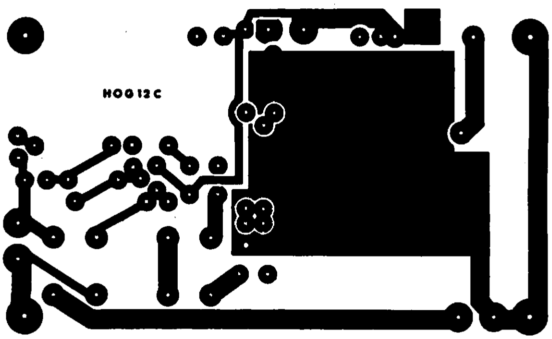
⊗ DENOTES TERMINAL PINS

◎ DENOTES BOARD STANDOFFS

FIGURE 10 — Printed Circuit Board Layout



NOTE: The Printed Circuit Board shown is 75% of the original.



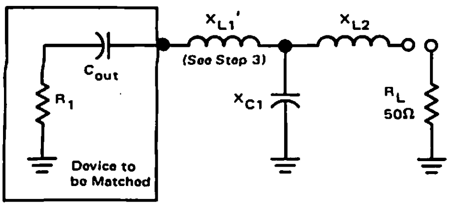
APPENDIX

This information was originally published in Motorola Application Note AN-267, "Matching Network Designs with Computer Solutions."

NETWORK D

The following is a computer solution for an RF "Tee" matching network.

Tuning is accomplished by using a variable capacitor for C_1. Variable matching may also be accomplished by increasing X_{L2} and adding an equal amount of X_C in series in the form of a variable capacitor.



TO DESIGN A NETWORK USING THE TABLES

1. Define Q, in column one, as X_{L1}/R_1.
2. For an R_1 to be matched and a desired Q, read the reactances of the network components from the charts.
3. X_{L1}' is equal to the quantity X_{L1} obtained from the tables plus $|X_{C_{out}}|$.
4. This completes the network.

Q	X_{L1}	X_{L2}	X_{C1}	R_1
8	8	27.39	7.6	1
8	16	63.25	14.03	2
8	24	85.15	20.1	3
8	32	102.47	25.87	4
8	40	117.26	31.42	5
8	48	130.38	36.77	6
8	56	142.3	41.95	7
8	64	153.3	46.99	8
8	72	163.55	51.9	9
8	80	173.21	56.7	10
8	88	182.35	61.39	11
8	96	191.05	65.98	12
8	104	199.37	70.49	13
8	112	207.36	74.91	14
8	120	215.06	79.26	15
8	128	222.49	83.54	16
8	136	229.67	87.74	17
8	144	236.64	91.89	18
8	152	243.41	95.97	19
8	160	250	100	20
8	168	256.42	103.97	21
8	176	262.68	107.9	22
8	184	268.79	111.77	23
8	192	274.77	115.59	24
8	200	280.62	119.38	25
8	208	286.36	123.11	26
8	216	291.98	126.81	27
8	224	297.49	130.47	28
8	232	302.9	134.09	29
8	240	308.22	137.67	30
8	256	318.59	144.73	32
8	272	328.63	151.65	34
8	288	338.38	158.46	36
8	304	347.85	165.14	38
8	320	357.07	171.71	40
8	336	366.06	178.18	42
8	352	374.83	184.56	44
8	368	383.41	190.83	46
8	384	391.79	197.02	48
8	400	400	203.13	50
8	440	419.82	218.04	55
8	480	438.75	232.49	60
8	520	456.89	246.53	65
8	560	474.34	260.2	70
8	600	491.17	273.52	75
8	640	507.44	286.52	80
8	680	523.21	299.23	85
8	720	538.52	311.66	90
8	760	553.4	323.84	95
8	800	567.89	335.78	100
8	1000	635.41	392.36	125
8	1200	696.42	444.63	150
8	1400	752.5	493.49	175
8	1600	804.67	539.57	200
8	1800	853.67	583.29	225
8	2000	900	625	250
8	2200	944.06	664.96	275
8	2400	986.15	703.38	300

Q	X_{L1}	X_{L2}	X_{C1}	R_1
9	9	40	8.37	1
9	18	75.5	15.6	2
9	27	98.99	22.4	3
9	36	117.9	28.88	4
9	45	134.16	35.09	5
9	54	148.66	41.09	6
9	63	161.86	46.91	7
9	72	174.07	52.56	8
9	81	185.47	58.07	9
9	90	196.21	63.45	10
9	99	206.4	68.71	11
9	108	216.1	73.86	12
9	117	225.39	78.92	13
9	126	234.31	83.88	14
9	135	242.9	88.76	15
9	144	251.2	93.55	16
9	153	259.23	98.28	17
9	162	267.02	102.93	18
9	171	274.59	107.51	19
9	180	281.96	112.03	20
9	189	289.14	116.49	21
9	198	296.14	120.89	22
9	207	302.99	125.23	23
9	216	309.68	129.53	24
9	225	316.23	133.77	25
9	234	322.65	137.97	26
9	243	328.94	142.12	27
9	252	335.11	146.22	28
9	261	341.17	150.28	29
9	270	347.13	154.3	30
9	288	358.75	162.23	32
9	306	370	170	34
9	324	380.92	177.63	36
9	342	391.54	185.14	38
9	360	401.87	192.52	40
9	378	411.95	199.78	42
9	396	421.78	206.93	44
9	414	431.39	213.98	46
9	432	440.79	220.93	48
9	450	450	227.78	50
9	495	472.23	244.52	55
9	540	493.46	260.74	60
9	585	513.81	276.51	65
9	630	533.39	291.85	70
9	675	552.27	306.8	75
9	720	570.53	321.4	80
9	765	588.22	335.67	85
9	810	605.39	349.63	90
9	855	622.09	363.31	95
9	900	638.36	376.71	100
9	1125	714.14	440.24	125
9	1350	782.62	498.94	150
9	1575	845.58	553.81	175
9	1800	904.16	605.54	200
9	2025	959.17	654.64	225
9	2250	1011.19	701.48	250
9	2475	1060.66	746.36	275
9	2700	1107.93	789.51	300

"A 15-WATT AM AIRCRAFT TRANSMITTER POWER AMPLIFIER USING LOW-COST PLASTIC TRANSISTORS"

Prepared by
Dave Hollander

INTRODUCTION

This application note describes a 15 watt carrier power, amplitude modulated broadband amplifier covering the 118-136 MHz AM aircraft band. Simplicity and low cost are emphasized in this design through the use of Motorola's common emitter TO-220 VHF power transistors. The power amplifier is designed to operate from 13.5 VDC. High level AM modulation is accomplished by a series modulator operating from a 27 volt supply.

CIRCUIT DESCRIPTION

The transmitter power amplifier has three stages using an MRF340 transistor as a pre-driver, a MRF342 as a driver, and a MRF344 as the final amplifier. All three devices are common emitter where the mounting tab is the emitter. The pre-driver stage is forward biased to enhance linearity and dynamic range. Amplitude modulation is applied fully to all three stages.

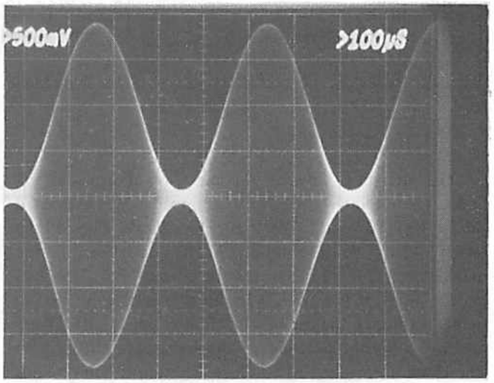
The P.A. is designed to operate with 50 ohm source and load impedances.

DESIGN CONSIDERATIONS

The design objectives are that the transmitter must be capable of operating over the range of 118 to 136 MHz with a minimum carrier output power of 15 watts. It must also be capable of being amplitude modulated greater than +85% over the frequency range, and the transmitter should be free from instability.

Other important considerations involve the interstage and the output networks. The output network is to operate efficiently at both the carrier power of 15 watts and the peak power of 60 watts while providing harmonic suppression. The interstage networks transform the output impedance of the device to the input impedance of the following device during modulation of all three stages.

FIGURE 1 – Modulated Output Waveform of Power Amplifier



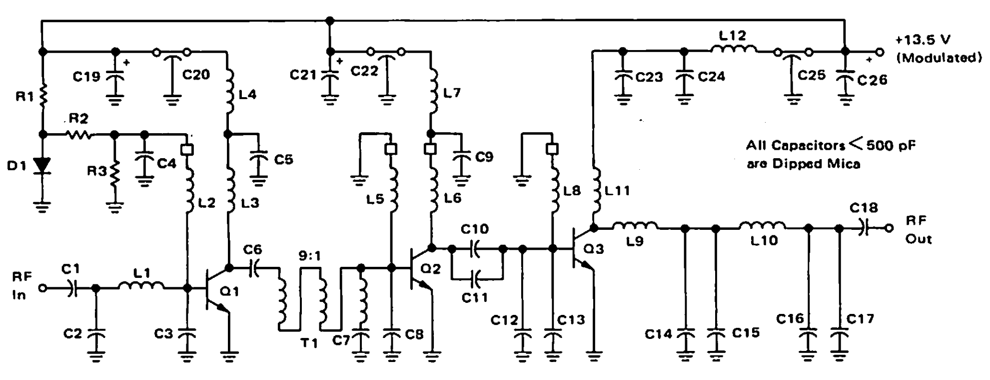
f = 136 MHz   Pcarrier = 15 Watts (2 cms)
% Upward Modulation = 90%

In designing the networks, the Smith Chart is used to obtain initial values. These values were then optimized using a computer aided design program.

Figure 2 shows a schematic diagram of the transmitter P.A. RF circuitry.

The pre-driver stage uses a simple π-section input matching network. Forward bias for this stage is obtained through the network consisting of R_1, R_2, R_3, D_1, and is applied to Q_1 through L_2. The quiescent current is approximately 20ma for the MRF340.

FIGURE 2 — Schematic Diagram



C1 — 200 pF
C2, C3 — 47 pF
C4, C5, C9, C23 — .001 Disc Ceramic
C6, C16 — 39 pF
C7 — 68 pF
C8, C12 — 200 pF UNELCO
C10 — 62 pF
C11 — 43 pF
C13 — 80 pF UNELCO
C14 — 56 pF
C15 — 75 pF
C17 — 10 pF
C18 — 300 pF

C19, C21, C26 — 1µf/50V
C20, C22, C25 — 680 pF Feed through
C24 — 0.1 µf
D1 — IN4002
All inductors other than molded chokes are wound with #18 AWG 1/8" ID
L1 — 3T
L2, L5, L8 — .15 µH molded choke with ferrite bead
L3 — 7T
L4, L7, L12 — .18 µH molded choke
L6, L10 — 4T
L9 — piece of wire — 3/4" long

L11 — 7T
R1 — 820Ω 1/4 W
R2 — 39Ω 1/4 W
R3 — 82Ω 1/4 W
T1 — 9:1 Unbalanced to unbalanced XFMR #24 AWG 12 crests per inch 3.5" long
Q1 — MRF340
Q2 — MRF342
Q3 — MRF344

The interstage between Q_1 and Q_2 is designed as follows. The effective collector load impedance is estimated to be 100-j50 ohms. The input impedance, Z_{IN}, of the MRF 342 is 1.75+j2 ohms at 136 MHz (as taken from the data sheet). One way to match the output of the MRF340 to the input of the MRF342 with a minimum of components is through the use of a 9:1 transformer (1,2). Figure 3 shows a Smith Chart plot of the interstage network with the chart normalized to 50 ohms. Starting at point A, this impedance is rotated to point B by a shunt capacitor C_8. The impedance at this point is approximately 5 to 5.5 ohms. A 9:1 transformer transforms this impedance to approximately 50 ohms. Point C, the 50 ohm point, is rotated to D by series capacitor C_6. Point D is then rotated to point E, the complex conjugate of the output impedance of Q_1, by shunt inductor L_3.

A different approach is used for the Q_2 - Q_3 interstage network. The MRF342 output impedance Z_{OL}, and the MRF344 input impedance Z_{IN}, are taken from the data sheets. Figure 4 shows a Smith Chart plot of this network with the chart normalized to 50 ohms. Point A is the input impedance of the MRF344. This impedance is rotated to the real axis by shunt capacitors — C_{12} and C_{13}. Point B is then rotated to point C by series capacitors — C_{10} and C_{11}. This impedance is then transformed to the complex conjugate of the output impedance of the MRF342 by shunt inductor L_6.

The MRF344 output matching network consists of a shunt inductor at the collector of Q_3 followed by two L-sections. L-sections were used because they provide excellent harmonic suppression and good efficiency over the entire band. Figure 5 shows a Smith Chart of the output network, with the chart normalized to 50 ohms.

All impedance matching element values calculated using the Smith Chart and optimized with the computer program were used as starting points in building the networks. The final component values shown in Figure 2 were derived through on-the-bench tuning and adjustment and differ from the calculated values as the Figure 2 values cover 118-136 MHz. The calculated values are only for 136 MHz.

Since low cost is a key factor in the use of the TO-220 devices, inexpensive components are used wherever applicable. Molded chokes, dipped mica and dipped ceramic capacitors are used throughout the circuit. One of the problems encountered when using dipped micas at VHF is their series lead inductance. The higher capacitance values approach resonance at VHF. Selected values were measured on an HP network analyzer at 125 MHz. The results are shown in Table 1.

TABLE 1

Cnominal (PF)	Cmeasured (PF)
5	5
10	10
25	26
30	33
39	45
50	64
75	106
100	161
200	750

Note: All lead lengths kept to an absolute minimum (<0.1 inch)

The data obtained shows that values below 75pf are usable. Lead length should be kept to a minimum when using both the dipped mica and the disc ceramic capacitors. UNELCO capacitors are used in place of the dipped micas at the base of Q_2 and Q_3, since the net required capacitance and base current is very high.

CONSTRUCTION TECHNIQUES

The amplifier is assembled on a 2" X 5" double sided printed circuit board. Board material is G-10 with a thickness of 0.062". A 1:1 photomaster of the top side of the board is shown in Figure 6. Eyelets are placed through the board at points marked by the letter "O". The eyelets are soldered to both sides of the PCB to connect the top ground to the bottom side ground return. Feed-thru capacitors are mounted on the DC feed bar which is made of G-10 PCB. A 1:1 photomaster of the feedbar is also shown in Figure 6. Eyelets are placed at points marked by an "O" and feed-thru capacitors are placed at points marked by an "X". The DC feedbar is soldered to the main board. The location of the critical components is shown in Figure 7. Construction details of the 9:1 impedance transformer are shown in Figure 8. (1,2)

For reliable operation, the transistors must not only be heatsunk, but they must also be mounted properly for emitter RF ground return. Figure 9 shows mounting details for the TO-220 package. More detailed information on mounting is available in AN-778.(3) The entire assembly is mounted on a 6" extruded aluminum heatsink using 4-40 X ¼ machine screws. The heatsink surface should be flat and free of burrs, particularly around the transistor mounting holes.

FIGURE 3 – MRF340 – MRF342 Interstage Network

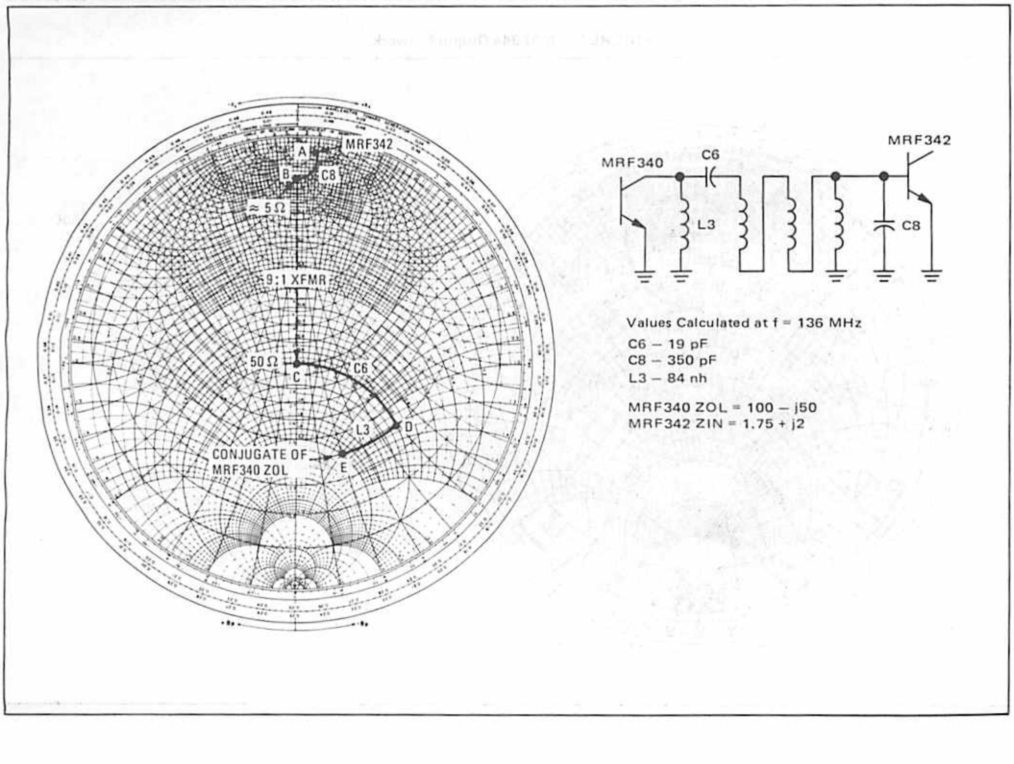


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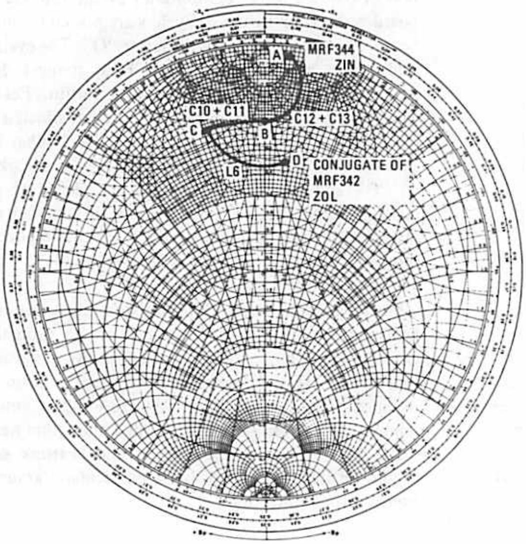
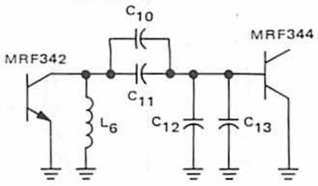
FIGURE 4 – MRF342-MRF344 Interstage Network



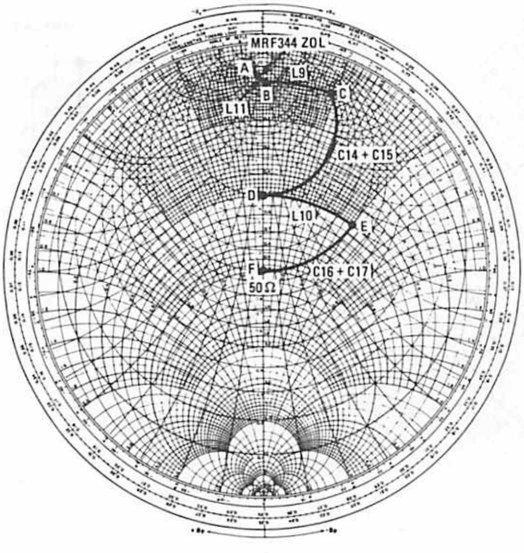


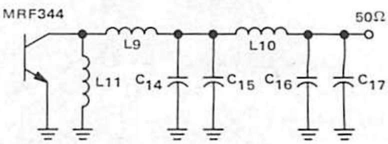
Values Calculated at f = 136 MHz

C10 + C11 – 130 pF
C12 + C13 – 365 pF
L6 – 15 nh

MRF342 ZOL = 17-j4.7
MRF344 ZIN = 1.25 + j2.86

FIGURE 5 – MRF344 Output Network





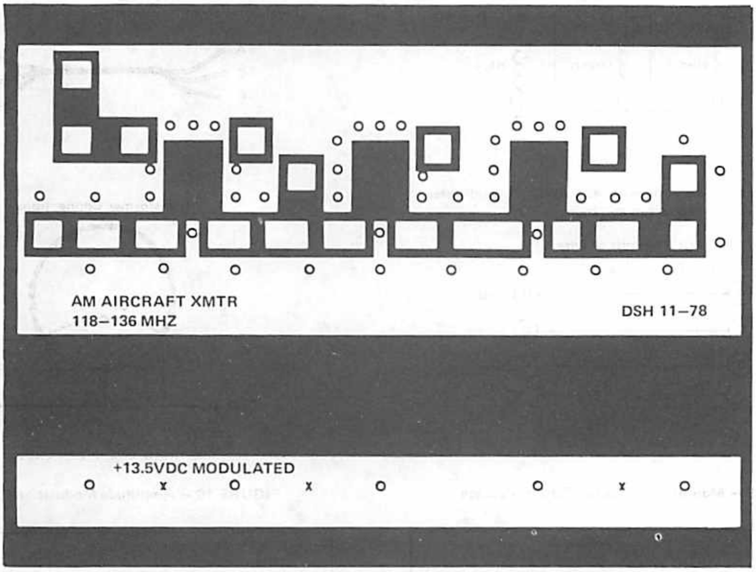
Calculated Values at f = 136 MHz

C14 + C15 = 100 pF
C16 + C17 = 23 pF
L9 = 11 nh
L10 = 28nh
L11 = 90 nh

MRF344 ZOL = 4.2-j0.32

7

FIGURE 6 — Photomaster



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 7 — Location of Critical Components

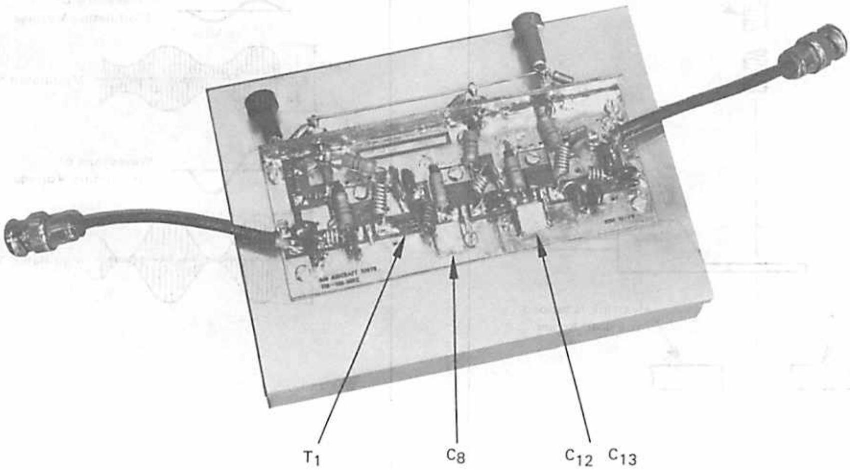


FIGURE 8 — Construction Details of the 9:1 Unbalanced to Unbalanced Transformer

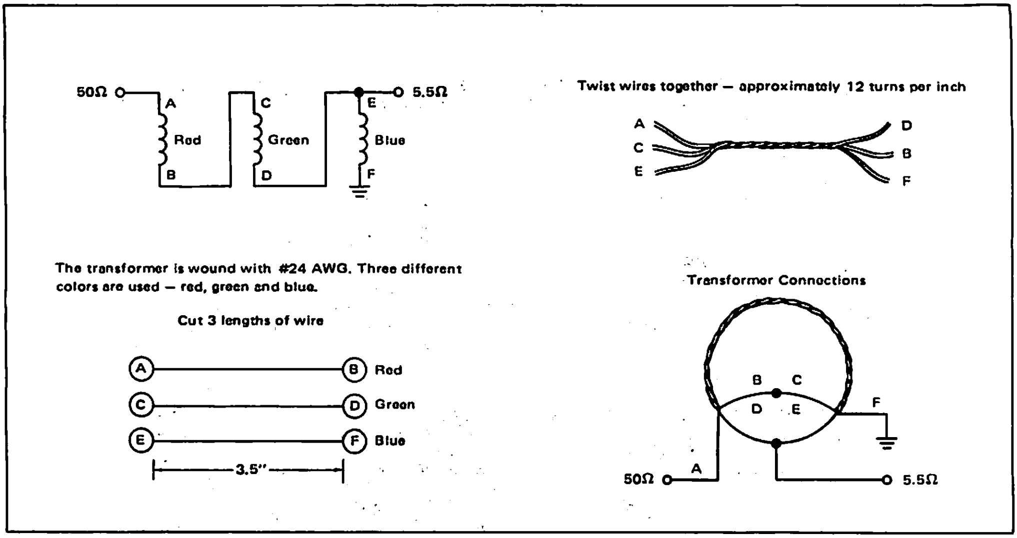


FIGURE 9 — Mounting Details for TO-220 Package

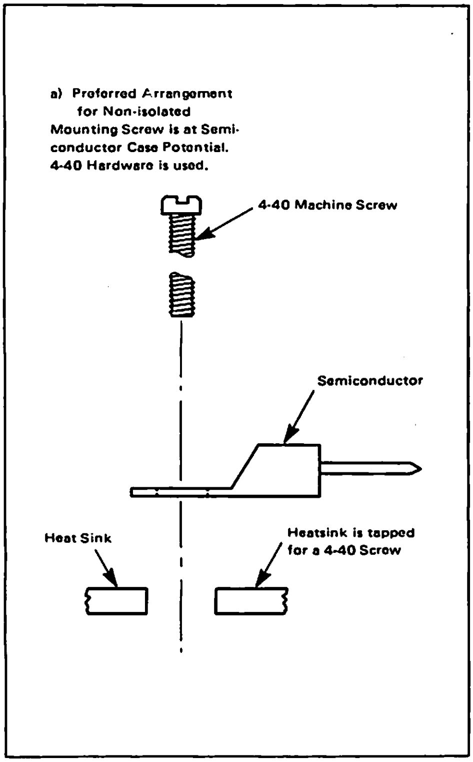
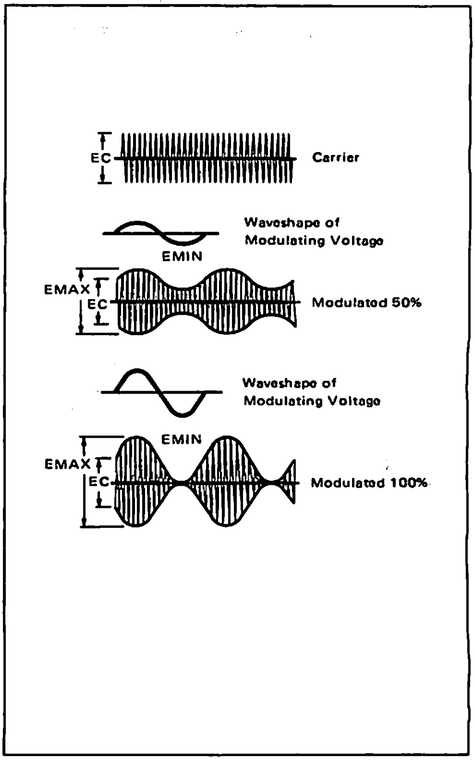


FIGURE 10 — Amplitude Modulation Waveforms



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MODULATION

In an amplitude modulated waveform the amplitude of each cycle of the modulated wave varies in accordance with the modulating signal. Using voice modulation, the resultant waveform is not only complex, but difficult to analyze. Therefore, when testing and analyzing the transmitter P.A., a simple 1 KHz sine wave is used as the modulating signal. When analyzing an AM waveform, one of the things to consider is the modulation factor (M). M is usually expressed as percent modulation and is calculated as follows:

$$M = \frac{Emax - Emin}{Emax + Emin} \times 100\%$$

Figure 10 shows amplitude modulation waveforms.

The above formula is valid only when the modulation process is symmetrical and little distortion is present. If significant assymmetry is present then up modulation and down modulation must be analyzed separately.

$$M = \frac{Emax - Ec}{Ec} \times 100\% \quad \text{For positive peak modulation}$$

$$M = \frac{Ec - Emin}{Ec} \times 100\% \quad \text{For negative peak modulation}$$

When a carrier is modulated by a pure sine wave, two sidebands are generated at the carrier frequency plus and minus the modulating frequency. The power level of the sidebands is dependent upon the percentage of modulation. At 100% modulation, the total power contained in the sidebands is one-half the carrier power or one-fourth in each sideband. For modulation levels of less than 100%, the total power is:

$$PSB = \frac{1}{2} m^2 PC$$

where m = modulation factor
Pc = carrier power

Collector modulation is a commonly used method for modulating a solid state transmitter. Using this method, the modulating voltage is applied to a collector through a transformer. The secondary winding of the transformer must be capable of handling the DC current required by the transistor and have low DC resistance, so as not to cause a significant voltage drop. The voltage drop will reduce the voltage applied to the collector of the stage being modulated.

Another form of collector modulation uses a series modulator. This type of modulator is used to evaluate the transmitter in this application note.(4) A series modulator uses audio power transistors instead of a transformer secondary. A schematic diagram of the series modulator is shown in Figure 11. 27 volts is applied to the modulator and the quiescent DC voltage applied to the transmitter is set by the 10KΩ potentiometer.

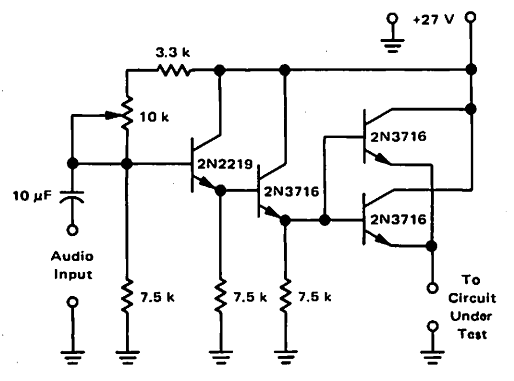
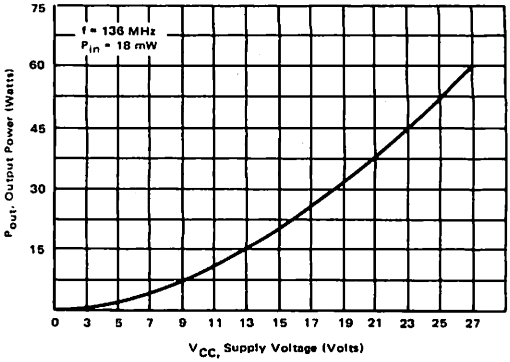


FIGURE 11 – Series Modulator

Table 2 – Performance of the 15 Watt Amplifier

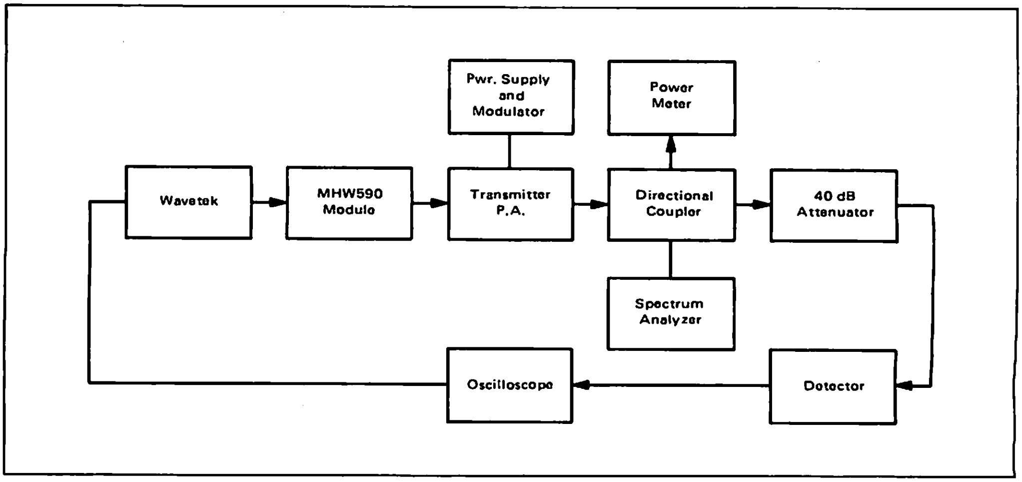
	118 MHz	127 MHz	136 MHz
P_{in} (mW)	14.0	15.0	18.0
Pcarrier (W)	15.0	15.0	15.0
Total Current (Adc)	2.2	2.0	2.5
Power Supply Voltage (Vdc)	13.5	13.5	13.5
Upward Modulation (%)	89.0	88.0	90.0
Harmonic Rejection (dB) (Relative to Peak Power)			
2f 3f	55.0 58.0	55.0 58.0	52.0 57.0
Load Mismatch	Capable of Operating into 3:1 Load VSWR.		

OUTPUT POWER VERSUS SUPPLY VOLTAGE



P_{out} is initially set at the carrier power of 15 watts at 13.5 Vdc, then the supply votlage is varied from 0 to 27 Vdc keeping P_{in} constant. This demonstrates the peak power output capability of the transmitter P.A.

FIGURE 12 – Block Diagram of Swept Set-Up for Tuning Up the Transmitter



TEST SET-UP

When adjusting a broadband RF power amplifier, it is advantageous to have a swept test station. Using a swept set-up, one can observe the following:

1) The effect of varying individual component values
2) Bandwidth
3) Instability
4) Input VSWR bandwidth.

A Wavetek 1002 Sweep Generator driving a Motorola MHW590 module is recommended as a drive source. Figure 12 shows a block diagram of the swept set-up used to test and evaluate the amplifier.

REFERENCES

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2. Granberg, H. "Broadband Transformers and Power Combining Techniques for RF," Motorola AN-749
3. Roehr, Bill, "Mounting Techniques for Power Semiconductors," Motorola AN-778
4. "A 13-W Broadband AM Aircraft Transmitter," Motorola AN-507
5. Terman, Frederick E., "Electronic and Radio Engineering," McGraw-Hill

POWER MOSFETs versus BIPOLAR TRANSISTORS

Prepared by
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Sr. Staff Engineer

What is better, if anything, with the power FETs if we can get a bipolar transistor with an equal power rating for less than half the price?

Several manufacturers have recently introduced power FETs for RF amplifier applications. Devices with 100 W output capabilities are available for VHF frequencies and smaller units are made for UHF operation. All are enhancement mode devices, which means that the gate must be biased with positive voltage (N channel) in respect to the source to "turn it on." Early designs were so called V-MOS FETs, where the channel is in a V-groove. The V-groove must be etched with a special process, and the silicon material must have a different crystal orientation from the material normally used for bipolar transistors. The difficulty of the etching process in production has led to the development of other types of channel structures such as HEX and T, which are still vertical channel structures, but V-groove is eliminated, and the gate is on a straight surface. Thus, for an equal gate periphery, more room

TABLE A

	Bipolar	TMOS FET
Z_{in} RS/ XS(30 MHz):	0.65 - J0.35 Ohms	2.20 - J2.80 Ohms
Z_{in} RS/ XS(150 MHz):	0.40 + J1.50 Ohms	0.65 - J0.35 Ohms
Z_{OL} (Load Impedance):	Almost equal in each case, depending on power level and supply voltage.	
Biasing:	Not required, except for linear operation, high current voltage source necessary.	Some gate bias always required. Low current source, such as resistor divider sufficient.
Ruggedness:	Fails usually under current conditions. Thermal runaway and secondary breakdown possible.	Failure modes: Gate punch through, exceeding of breakdown voltages, over dissipation.
Linearity:	Low order distortion depends on die size and geometry. High order IMD is a function of type and value of ballast resistors.	Low order distoriton worse than bipolar for a given die size and geometry. High order IMD better due to lack of ballast resistors.
Advantages:	Wafer processing easier. Low collector-emitter saturation voltage, which makes devices for low voltage operation possible.	Input impedance more constant under varying drive level. Lower high order IMD. Easier to broadband. Devices or die can be paralleled. High voltage devices easy to implement.
Disadvantages:	Low input impedance with high reactive component. Internal matching required to lower Q. Input impedance varies with drive level. Devices or die cannot easily be paralled.	Larger die required for comparable power level. Nonrecoverable gate breakdown. High drain — source saturation voltage, which makes low voltage, high power devices less feasible.

on the surface is required. Japanese manufacturers seem to favor geometries with horizontal channels. They are similar to small signal MOSFETs with a number of them paralleled on one chip. This technique represents even more wasteful use of the die surface than HEX or TMOS. Typically a power FET requires 50 to 100 percent more die area than a bipolar transistor for equal power output performance. For TMOS the number is about 50 percent. This is mainly due to the higher saturation voltage, but the geometry also gives some 30 percent less gate periphery than available base area in bipolar. Since the price of a solid state device is a function of a die size, we get fewer watts per dollar. This is completely opposite from what the industry has been trying to do in the past years with bipolar transistors. So, one may ask: What is better, if anything, with the power FETs if we can get a bipolar transistor with an equal power rating for less than half the price? This is where we come to the purpose of this article, which is to discuss the characteristics of the FET and bipolar device. Both have the same basic geometry, but with some mask changes, one was processed as a MOSFET and the other as a bipolar.

CIRCUIT CONFIGURATIONS

Since the gate of a MOSFET device is essentially a capacitor, which consists of MOS capacitance distributed between the channel and the surface metalization, the input Q is normally extremely high. For this reason, the gate must be de-Q'ed with a shunt resistance or applying negative feedback or a combination of the two. Unless this is done properly, the affect of feedback capacitance (C_{rss}) will result in conditions, where stable operation is impossible to achieve.

Figure 1 shows a Smith Chart plot of a 150 W MOS FET and a bipolar device using the same basic geometry for comparison purposes. The gate of the FET has been shunted by a resistance of 20 ohms. Without the shunt resistance the input impedance would be a pure capacitive reactance, if package inductances are disregarded.

The input Q is an inverse function of the broadbandability of a device. With the techniques mentioned above, the Q can be controlled to a large degree, but some power gain will be sacrificed, unless only some type of selective negative feedback is employed for that purpose. Amplifiers in the 100 W power level, covering five octaves can be designed, and the limiting factor only seems to be the proper design of the broadband matching transformers.

Due to the lack of base diode junctions inherent to bipolar devices, where the diode forward conductance depends on the drive level, the MOSFET gate impedance varies only slightly with the input voltage amplitude. The gate MOS capacitance should be more or less independent of voltage, depending on the die processing. This is considered one of the advantages with FETs, especially regarding amplitude modulated applications, where a constant load for the driver stage is important. Negative feedback should be limited, since it tends to deteriorate this characteristic. Another advantage is the AGC capability by varying the gate voltage. In common source configuration, depending on the initial power gain, etc., an AGC range of 20 dB is achievable.

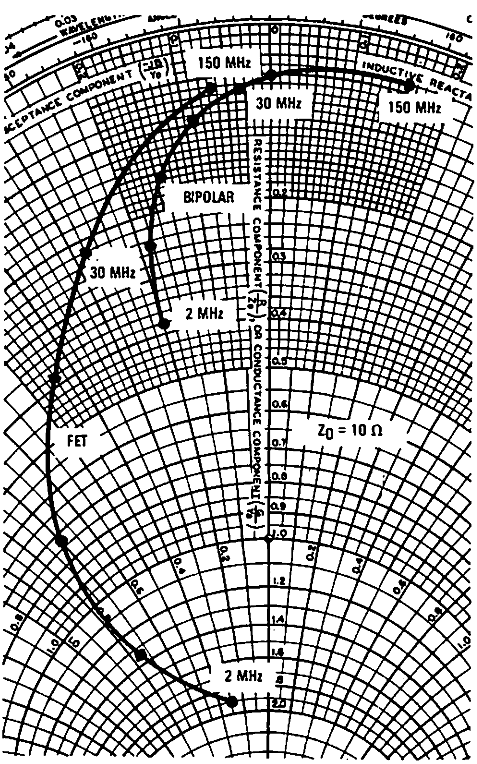

FIGURE 1 — 150 Watt MOSFET and Bipolar Comparison

Common gate configuration has some advantages, although it is not useful in applications requiring linearity. The load impedance is reflected back to the gate and in effect is in parallel with the source to ground impedance. The total input impedance is more constant with frequency than in common source mode, but varies greatly with output power level and supply voltage. As in a comparable configuration with bipolar transistors, the overall power gain is low, but the unity gain frequency ($f\alpha$) extends higher, which makes the common gate circuit attractive at UHF designs. It also

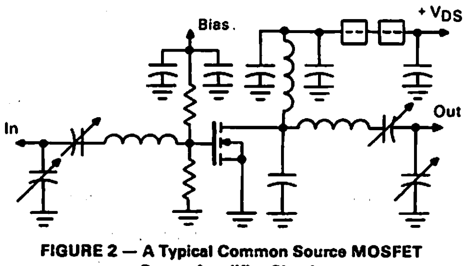

FIGURE 2 — A Typical Common Source MOSFET Power Amplifier Circuit

has more tendency for parasitic oscillations, since the input and output are in the same phase. The de-Q'ing of the input can be done in the same manner as in a common source circuit, but negative feedback is not as easy to implement. This circuit also exhibits greater power gain versus bias voltage variation characteristics. In applications, where 40 dB to 50 dB AGC range is required, the common gate configuration should be considered.

A common drain configuration represents the emitter follower in bipolar circuits. In both cases the input impedance is high and the load impedance is effectively in series with the input. The input capacitance, (drain-to-gate, or collector-to-base) is lower than in common source or common gate circuits, and several times lower for the FET than bipolar for equal die size. This is due to lack of the diode junction. A MOSFET source follower can not be regarded as having current gain as the emitter follower. The amplification rather takes place through impedance transformation. Due to the fair amount of input de-Q'ing required, the available power gain is lower than in common source circuit for example. Having less than unity voltage gain, the circuit exhibits exceptional stability, and negative feedback is not necessary, nor can it be easily implemented. Push pull broadband circuits for a frequency range of 2 to 50 MHz have been designed for 200-300 watt power levels. Their inherent characteristics are good linearity and gain flatness without any leveling networks. High power SSB amplifiers are probably the most suitable application for common drain operation. The AGC range is comparable to that in common source, but higher voltage swing is required. It must be noted that the MOS devices used must have high gate rupture voltage, since during the negative half cycle of the input signal, the gate voltage approaches the level of V_{DS}.

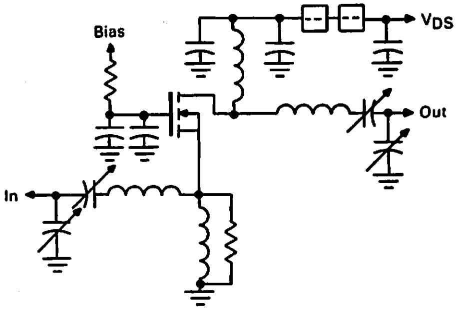

FIGURE 3 — A Typical Common Gate MOSFET Power Amplifier Circuit

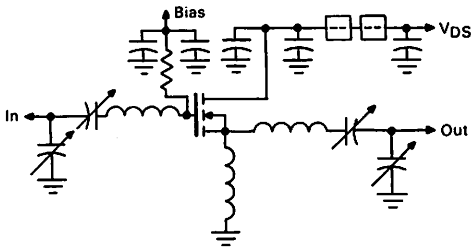

FIGURE 4 — A Typical Common Drain, Narrow Band MOSFET Power Amplifier Circuit

LINEARITY ASPECTS

Some literature claims that MOS power FETs are inherently more linear than the bipolar transistors. This is only true up to the point where envelope distortion, caused by saturation, instabilities or other reasons, is not present. It is also a function of the bias current (I_{DQ}). The FETs usually require higher idling currents than the bipolars to get full advantage of their linearity. Bipolars are usually biased only to get the base-emitter diode into forward conduction, whereafter increasing the bias helps little. Class A is an exception, but the device must then be operated at 20-25 percent of the rated Class AB level.

Probably the main advantage with the MOS power FETs is their greatly superior high order IM distortion performance. This is mainly due to the fact that ballasting resistors are not required with FETs. In bipolar RF power transistors, nonlinear feedback is distributed to each emitter site through the MOS capacitance from the collector. In devices using diffused silicon resistors, this effect is even worse, and caused by additional nonlinear diode capacitance between the collector and the emitters. The high order IMD (9th and up) is actually in direct relation to the ballasting resistor values, which must be optimized for an even power distribution along the die. Too low values would result in a fragile device, and the opposite would, in addition to the IMD problem, result in high collector-emitter saturation voltage and low power gain.

The feedback capacitance, drain-to-gate or collector-to-base for example, also has a secondary effect in IMD. In both cases it is a function of the die geometry, and is usually lower with devices with higher figure of merit, such as the ones made for UHF and microwave applications. A MOS power FET exhibits some five times lower feedback capacitance than a bipolar transistor with a similar geometry. In a bipolar transistor this capacitance partly consists of the collector-base junction, which is highly nonlinear with voltage. This, together with the varying input impedance, generates internal feedback, which is nonlinear and produce high order IMD to some degree. A more noticeable effect is that the low order IMD goes up with reduced drive levels as shown in Figure 6.

This can be related to different turn on characteristics between the two device types. When a bipolar device is biased to Class AB, the bias does not usually, completely overcome the V_{BE} knee. Thus, at lower signal levels, the remaining nonlinear portion covers a larger area of the total voltage swing. Increasing the bias from the normally recommended Class AB values will help and full Class A should eliminate the problem completely.

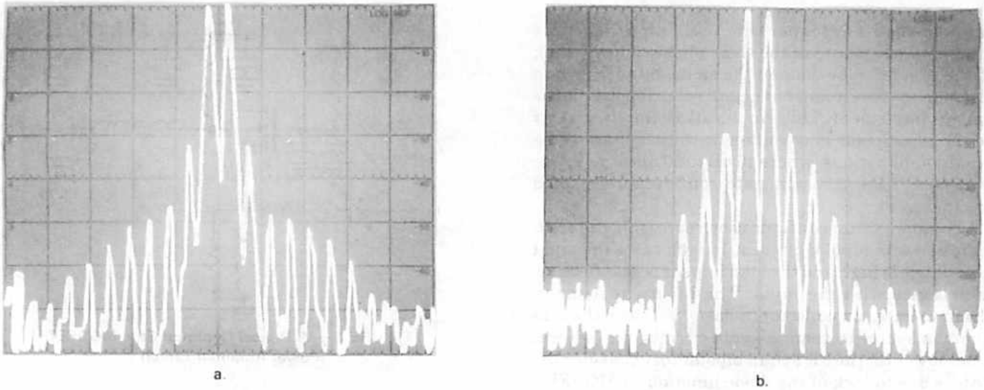

FIGURE 5 — Two Tone Spectrographs of 300 W PEP, 50 V Amplifier Outputs
a. using bipolar transistors and b. with TMOS power FETs. 500 mA of bias current per device was used in each case. Doubling the bias current has a minimal effect in a. but b. the 7th order products would be lowered by 10–12 dB.

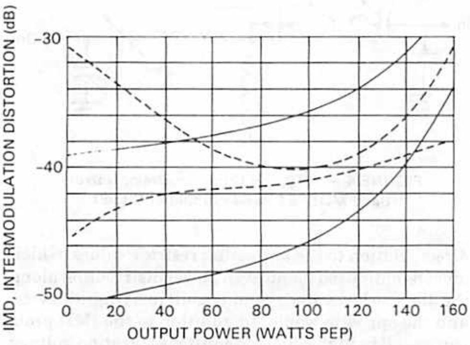

FIGURE 6 — IM Distortion as a Function of Power Output. Solid Curves MOSFET, Dashed Curves Bipolar Transistor

CLASS D/E APPLICATIONS

Switching mode RF power amplifiers have only become feasible since the introduction of the power FET. Being a majority carrier device, the FET does not exhibit the storage time phenomena, that limits the switching speed of a bipolar. For a given device, the switching speed is mainly determined by the speed the gate capacitance can be charged and discharged. If the capacitance is in the order of several hundred pF, a smaller FET is required to provide the fast charge-discharge switch. For low power stages, bipolars can be used, since the storage time is mainly an inverse function of the f_T and device size. The advantages of a Class D amplifier are high efficiency, linearity and ruggedness, since power is ideally dissipated only during the switching transitions.

These amplifiers are readily applicable for FM modulation, after harmonic filtering. The analog gain is obtained by pulse-width modulation of the input switching signal, and demodulation of the output with suitable filters. Linearity is required only from the modulator, which is easy to achieve at small signal levels. The high speed voltage controlled one shot MC10198 should be ideal for a linear pulse-width modulator. By properly adjusting its operating point, low level AM or suppressed carrier double sideband signals can be generated.

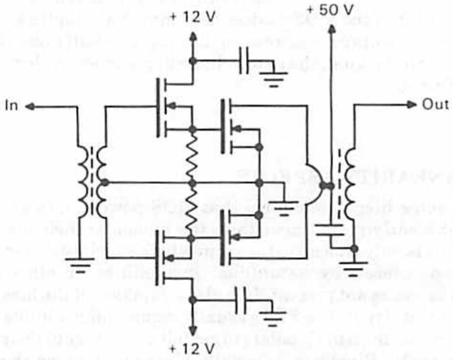

FIGURE 7 — A Typical Power MOSFET Class D RF Amplifier, Arranged in Push-Pull Configuration

GENERAL

All MOSFETs can in theory have a positive temperature coefficient on the gate threshold voltage. This means that the gate threshold voltage increases with temperature, trying to "turn the device off." In addition the g_m will decrease, which also helps in preventing the thermal runaway, which is commonly a problem with bipolars. The coefficient of the gate threshold voltage is also a function of the drain current. Normally the coefficient is negative at low current levels, and turns positive at higher currents. The turnaround point, which can be controlled by doping the other fabrication steps, must be at a current level not to exceed the maximum dissipation rating, taking the derating factor into account. Thus, the power MOS devices can be easily biased to Class A, without fear of a thermal runaway.

Two types of high frequency noise are generated by bipolar transistors. Shot noise is caused by the forward biased junctions, and thermal noise by moving carriers upon flow of electrons. Both have different noise spectrums, and only the latter is present in a FET. In a transmitter, where the devices are biased for linear operation, the shot noise becomes a problem, especially if a receiver is in close proximity, as in transceiver designs. Also, if several stations are operated near each other, the noise can be transmitted through the antenna, disturbing the reception at nearby stations. In most instances, the bias of the power devices must be switched on and off during the transmit and receive functions, which will prevent a full break-in operation. Measurements of 150 W devices, intended for SSB applications, were performed at 30 MHz, at the proper idling current levels. The difference in the total noise figure between a bipolar and a FET is about three to one, or 7 dB and 2.2 dB respectively. The amount of noise that can be tolerated varies with each situation, and whether the difference above is significant in practice depends on other factors involving the design of the equipment.

CONCLUSION

From the above we must conclude that it is doubtful the power FET ever will replace the bipolar transistor in all areas of communications equipment. It will have its applications in low and medium power VHF and UHF amplifiers, eliminating the need for internal matching, and up to medium power low band and VHF SSB, where the high order IMD is beginning to be more and more in emphasis due to the crowded frequency spectrums. The author's personal opinion is that the power FET is the most feasible device for the amplitude compandored sideband (ACSB) applications, proposed for future use in land mobile communications. The system principle requires extreme linearity in the amplifying stages, which in the past has only been achieved with Class A operation. The power FET also opens new applications for high efficiency switching mode power amplifiers, which have not been possible in the past for reasons described earlier. The possible upper frequency limit would be dictated by the physical lay-out of the system.

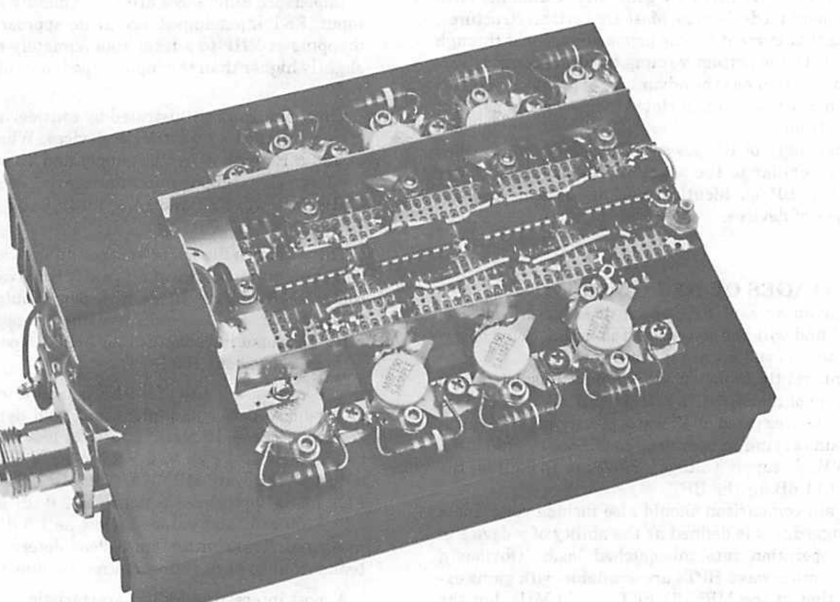

FIGURE 8 — An Experimental Three Stage, One Kilowatt Class D Amplifier.
The unit operates up to 10 MHz yielding an efficiency of 85 percent. The power gain is 30 dB.

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VHF MOS POWER APPLICATIONS

Prepared by
Roy Hejhall
Sr. Staff Engineer

INTRODUCTION

The assumption is made that the reader is familiar with the types, construction, and electrical characteristics of FETS. References 1 and 2 contain information on this subject.

Silicon RF power FETs are generally N-Channel MOS enhancement mode devices. Most are vertical structures, meaning that current flow is primarily vertical through the chip with the bottom forming the drain contact. Vertical construction has the advantage of providing greater current density which translates to more watts per unit area of silicon.

The assembly of RF power FET wafers into finished devices is similar to the assembly of bipolar RF power transistors (BPTs). Identical packaging is utilized for both types of devices.

ADVANTAGES OF RF POWER FETS

The advantages of FETs have been described elsewhere,[3,4] and will not be repeated in detail. Some observations on this subject are given below.

The inherently higher power gain is illustrated by a comparison of the MRF171 FET and MRF315 BPT. Both are VHF devices rated at 45 watts power output. Typical power gains at similar operating conditions ($f = 150$ MHz, $P_{out} = 45$ W, dc supply voltage $= 28$ V) are 15.0 dB for the FET and 11 dB for the BPT.

Any gain comparison should also include ruggedness data. Ruggedness is defined as the ability of a device to survive operation into mismatched loads. Obviously, UHF and microwave BPTs are available with gains exceeding that of the MRF171 FET at 150 MHz, but the higher frequency BPTs will not survive much abuse at VHF. The superior ruggedness of the FET is even more impressive when it is recognized that no source site ballasting is used.

Another gain comparison at VHF is provided by the MRF174 FET and MRF317 BPT. The MRF317 is rated at 100 watts output, and contains an internal input matching network which increases the device gain by typically 5.0 dB. The MRF174 is rated at 125 watts output and has no internal input matching, yet the typical gain of the MRF174 at 125 watts output is 12 dB while the typical gain of the MRF317 is 10 dB at 100 watts output (both devices operating at 150 MHz with a 28 Vdc supply).

Impedance differences are found mainly at the device input. FET input impedance at dc approaches infinity, dropping at VHF to a level approximately equal to, but slightly higher than the input impedances of comparable BPTs.

This point can be illustrated by considering again the aforementioned 45 watt VHF devices. When operating at 150 MHz with a 28 Vdc supply and 45 watts output, the large-signal input impedances are $1.89 - j4.81$ ohms for the MRF171 FET and $1.2 + j1.0$ ohms for the MRF315 BPT.

These devices illustrate another difference. The large-signal input impedance of FETs at VHF is capacitive. By contrast, most VHF BPTs with power outputs greater than 20 watts have an inductive input impedance at 150 MHz. The input impedance of the MRF315 passes through resonance at about 100 MHz.

The low-noise figure of the FETs facilitates the design of low-noise power amplifiers and high dynamic range receiver front ends. Noise figures of less than 3.0 dB at $f = 150$ MHz, $V_{DS} = 28$ V, $I_D = 2.0$ A have been measured with the 125 watt MRF174. The MRF134 5.0 W VHF FET has a typical noise figure of 2.0 dB at 150 MHz, 28 V, 100 mA, and values as low as 1.5 dB have been measured. Transmitter noise floor determines the antenna front to back ratio required for duplex systems.

A most interesting FET characteristic is the inherent gain control mechanism. The power output of a FET amplifier can be varied from full rated output over a range of greater than 20 dB (with RF input power held constant) by varying the dc gate voltage. Further, the device gate does not draw dc current, so the dc source utilized for gain control does not have to deliver any power to the FET. This capability, which does not exist in the RF power BPT, facilitates the design of systems requiring gain control, either manual or automatic.

AMPLIFIER DESIGN

The design of TMOS FET RF power amplifiers has much in common with the design of BPT amplifiers. The amplifier must include dc circuitry to apply bias voltages and RF matching networks to perform the necessary impedance transformation over the frequency band of interest. Amplifier design consists of the synthesis of circuitry to perform the above tasks.

A positive dc supply voltage is required on the drain. To date most RF power FETs have been designed for the standard BPT operating collector voltages, i.e. 12.5 V, 28 V, and 50 V. Some higher voltage FETs are also available. The FETs described are designed for 28 V operation.

There is no FET parallel to the popular zero base bias BPT amplifier. The typical FET RF power amplifier requires forward gate bias for optimum power output and gain. That is the bad news; the good news is that the FET gate is a dc open circuit and the bias network may often be just a simple resistive divider.

A convenient gate bias source is the drain supply. When utilizing this technique care must be taken in filtering the bias circuitry. An inadequately filtered bias circuit connected to the drain supply can form an output-to-input feedback path for oscillations.

BPT amplifiers. These networks usually take the form of broadband transformers at HF, lumped reactive elements at VHF, and microstrip lines with RF chip capacitors at UHF.[5,6]

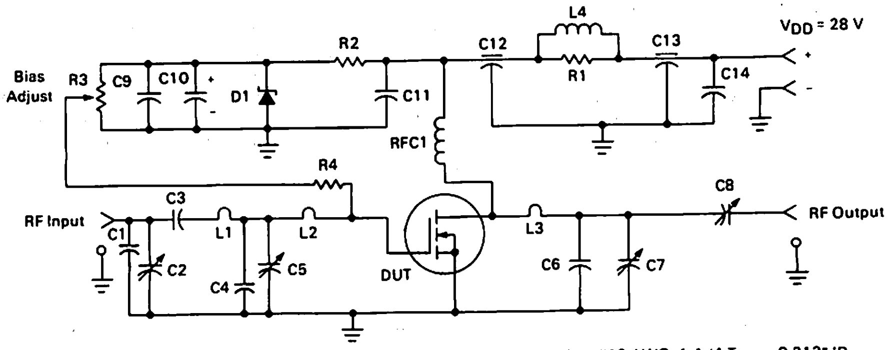
Solid-state power amplifier drain or collector load impedances are set primarily by supply voltage and power level. Therefore, FET and BPT amplifiers with like performance parameters can utilize similar output networks.

The inductive input impedance of high power VHF BPTs usually dictates that the input network design include shunt capacitors placed as close to the transistor package as is physically possible. FETs, with their capacitive input impedances at VHF, do not require these critical capacitive circuit elements.

Figure 1 shows a 125 watt 150 MHz amplifier which utilizes the MRF174 TMOS FET. Note the following items which have been discussed previously:

1. No shunt capacitors at the gate.
2. Resistive bias network operating from the drain supply voltage.
3. Impedance matching networks similar to those of a comparable BPT amplifier (except for item 1 above).

FIGURE 1 — 125 Watt, 150 MHz TMOS FET Amplifier



C1 — 35 pF Unleco
C2, C5 — Arco 462, 5-80 pF
C3 — 100 pF Unleco
C4 — 25 pF Unleco
C6 — 40 pF Unleco
C7 — Arco 461, 2.7-30 pF
C8 — Arco 463, 9-180 pF
C9, C11, C14 — 0.1 μF Erie Redcap
C10 — 50 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — #16 AWG, 1-1/4 Turns, 0.213" ID
L2 — #16 AWG, Hairpin 0.25" 0.062"
L3 — #14 AWG, Hairpin 0.47" 0.2"
L4 — 10 Turns #16 AWG Enameled Wire on R1
RFC1 — 18 Turns #16 AWG Enameled Wire, 0.3" ID
R1 — 10 Ω, 2.0 W
R2 — 1.8 kΩ, 1/2 W
R3 — 10 kΩ, 10 Turn Bourns
R4 — 10 kΩ, 1/4 W

FET amplifier I_{DQ} (quiescent drain current) is not critical and values in the 10-150 mA range are suggested. I_{DQ} may be varied from less than 100 mA to values approaching Class A operation without large changes in gain and efficiency at full rated power. Linear applications are an exception to this where I_{DQ} should be selected to optimize linearity.

The design of RF impedance matching networks for FET amplifiers is similar to the corresponding task for

This amplifier operates from a 28 volt dc supply. It has a typical gain of 12 dB, and can survive operation into a 30:1 VSWR load at any phase angle with no damage.

The amplifier has an AGC range in excess of 20 dB. This means that with input power held constant at the level that provides 125 watts output, the output power may be reduced to less than 1.0 watt continuously by driving the dc gate voltage negative from its I_{DQ} value. Figure 2 illustrates this performance feature. Note that

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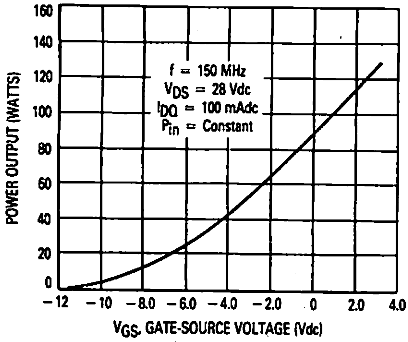


FIGURE 2 — Gain Control Performance of 125 Watt Amplifier

a negative voltage capability would have to be added to the bias system to take full advantage of this AGC performance.

Another useful feature of RF power FETs is that they have less variation of input and output impedances with power level than does a BPT. This characteristic permits the use of small-signal 2 port scattering parameters to develop useful design information for gain, stability, and impedances.[7] S-parameters are often found on RF power FET data sheets. While s-parameters will not provide an exact design solution for high power operation, they do produce a useful first approximation.

Power FETs with outputs below the 40 watt range often have such high gain at HF and VHF that stability problems may be encountered. This problem can be addressed by the classic methods used to stabilize RF small-signal amplifiers — loading of input or output terminals, feedback, or both. Here is an area where s-parameters are useful in calculating the effects of circuit techniques for achieving stability. References 7 and 8 discuss amplifier stability.

Figure 3 shows a 5.0 watt 150 MHz amplifier utilizing the MRF134 TMOS power FET. The MRF134 is a very high gain FET which is potentially unstable at both VHF and UHF. Note that a 68 ohm input loading resistor has been utilized to enhance stability. This amplifier has a gain of 14 dB and a drain efficiency of 55%. Figure 4 shows a 5.0 watt 400 MHz amplifier with a nominal gain of 10.5 dB.

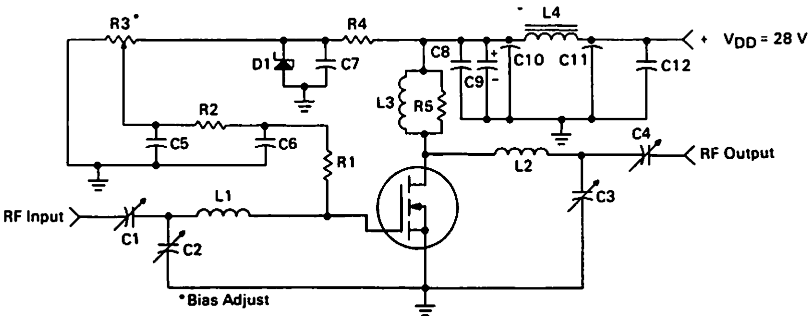
CAUTIONARY NOTES

Some precautions regarding FET RF power amplifiers should be mentioned.

One involves temperature coefficient. Literature abounds with statements that FETs are totally immune to thermal runaway because of their negative temperature coefficient. Actually, many RF power FETs have a positive temperature coefficient over a portion of their operating range. Increasing drain current usually shifts the coefficient from positive to negative. See Figure 5.

DC bias experiments have been conducted with several RF TMOS FETs. While they all had positive temperature coefficients over a portion of their operating ranges, none exhibited a tendency toward thermal runaway at drain currents ranging from less than 100 mA to full Class A bias. Thermal runaway does not appear to be a problem, but the positive temperature coefficients suggest that the designer should not completely ignore the thermal aspects of dc bias design.

FIGURE 3 — 5.0 Watt, 150 MHz TMOS FET Amplifier



C1, C4 — Arco 406, 15-115 pF
C2 — Arco 403, 3-35 pF
C3 — Arco 402, 1.5-20 pF
C5, C6, C7, C8, C12 — 0.1 μF Erie Redcap
C9 — 10 μF, 50 V
C10, C11 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 3 Turns, 0.310" ID, #18 AWG Enamel, 0.2" Long
L2 — 3-1/2 Turns, 0.310" ID, #18 AWG Enamel, 0.25" Long
L3 — 20 Turns, #20 AWG Enamel Wound on R5
L4 — Ferroxcube VK-200 — 19/4B
R1 — 68 Ω, 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
R5 — 1.0 MΩ, 2.0 W Carbon
Board — G10, 62 mils

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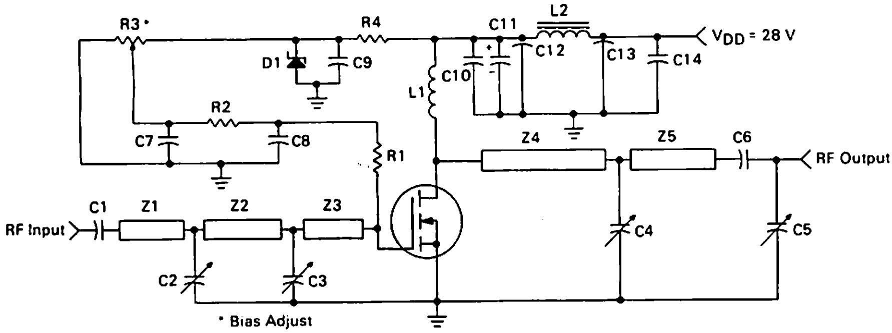
FIGURE 4 — 5.0 Watt, 400 MHz TMOS FET Amplifier



* Bias Adjust

C1, C6 — 270 pF, ATC 100 mils
C2, C3, C4, C5 — 0-20 pF Johanson
C7, C9, C10, C14 — 0.1 μF Erie Redcap, 50 V
C8 — 0.001 μF
C11 — 10 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener
L1 — 6 Turns, 1/4" ID, #20 AWG Enamel
L2 — Ferroxcube VK-200 — 19/4B
R1 — 68 Ω, 1.0 W Thin Film
R2 — 10 kΩ, 1/4 W
R3 — 10 Turns, 10 kΩ Beckman Instruments 8108
R4 — 1.8 kΩ, 1/2 W
Z1 — 1.4" × 0.166" Microstrip
Z2 — 1.1" × 0.166" Microstrip
Z3 — 0.95" × 0.166" Microstrip
Z4 — 2.2" × 0.166" Microstrip
Z5 — 0.85" × 0.166" Microstrip
Board — Glass Teflon, 62 mils

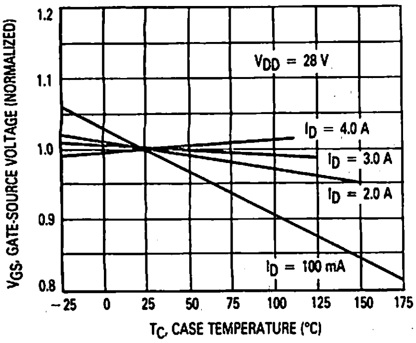


FIGURE 5 — Gate-Source Voltage versus Case Temperature For Constant Values of Drain Current MRF174

A second potential problem is the danger of permanent damage to FET gates from static electricity. Fortunately, the larger capacitances of power devices reduce this danger. No special precautions have been taken to protect the FETs described from static damage, and there were no failures known to be caused by static induced voltages. However, it is worthwhile to exercise the usual precautions taken in handling all MOS devices.

SUMMARY

The construction, characteristics, and advantages of RF power FETs have been described with emphasis on the VHF frequency range. Particular attention was given to the excellent gain control characteristics of these devices.

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7

800 MHz TEST FIXTURE DESIGN

by
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Although this article presents techniques for the general case of UHF-800 MHz circuit design, the emphasis is placed specifically on test fixture design for 800 MHz. Text fixtures tend to be the last consideration for most RF power amplifier development programs, yet they are the most valuable tool available for measuring and maintaining device consistency. Minimum power gain, collector efficiency and broadband performance requirements, though they are always detailed in some form of written specification, are meaningless unless they are demonstrated and controlled by a test fixture. A good test fixture will assure correlation between the customer and vendor and function as a trouble shooting tool in the event of radio problems. When alternate sources are pursued for a stage, test fixtures can shorten qualification cycles. But the prevention of gradual shifts in RF performance over the lifetime of a product is the major purpose of a test fixture.

Motorola has recognized the importance for good test fixtures and has established general guidelines for their implementation.

Each hi-tech product is tied to a well defined test fixture, which has the following general specifications:

- Broadband performance, demonstrating typical characteristics throughout the band. (Ex.: UHF; 450–512 MHz, 800; 800–870 MHz)
- A 3" x 5" mechanical format, which is rugged for high volume test applications.
- Simple RF match construction to represent realistic radio performance.
- Devices must meet all minimum test requirements at the specified test frequency. UHF: 470 MHz, 800: 870 MHz.

The repeatability, mechanical ruggedness and broadband performance are all very important factors needing consideration in the design of test fixtures. The remainder of this article goes into detail, using the MRF846 as an example.

The schematic representation of the fixture outlined in this article is shown below (Figure 1).

C_I and C_O represent the shunt capacitors at the input and output (respectively) which cancel most of the inductive reactance associated with the transistor's input and output impedance. Mini clamped-mica capacitors are used for these components and are physically located beneath the common lead wear blocks. Inductance "L" is introduced by the input (and output) wear blocks. Because of this parasitic inductance, L, trimmer capacitors (C'_I or C'_O) are required to transform the now reactive impedance back to real before launching off into the λ/4 transmission lines.

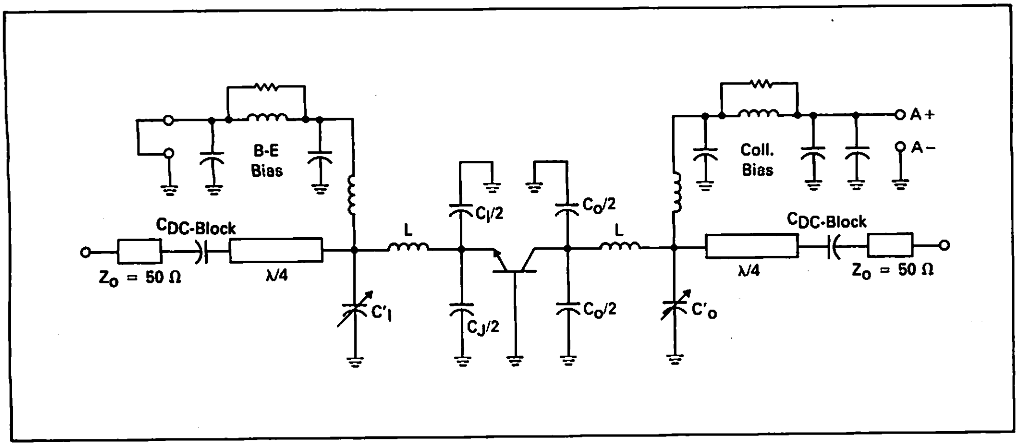

FIGURE 1 — SCHEMATIC REPRESENTATION OF TEST FIXTURE

The transistor's input and output impedance can be represented as a combined series resistor and inductor as shown in Figure 2.

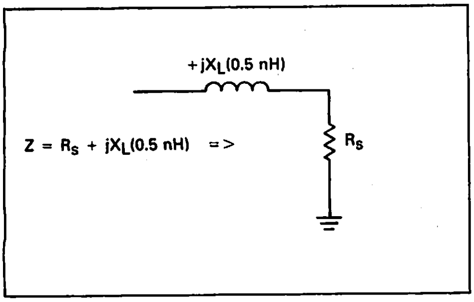

FIGURE 2 — EQUIVALENT CIRCUIT FOR Z_{in} OR Z_{out}

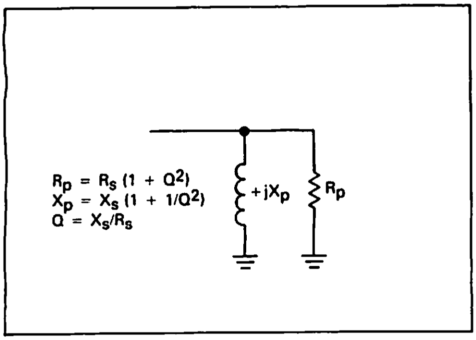

FIGURE 3 — PARALLEL EQUIVALENT CIRCUIT

This series combination can be transformed into a parallel equivalent by using the equations shown in Figure 3. The capacitors C_I and C_O are selected by calculating the value necessary to form a parallel resonance with X_p. Since all capacitors have a finite, series lead inductance, the capacitor is actually considered as a simple series resonant circuit. The resulting effect is the capacitance is always higher than the marked value and goes through resonance at some frequency. Mini clamped-mica capacitors are recommended for test fixture design due to the very low parasitic inductance associated with them which increases the usable range of capacitances. (They are also extremely high "Q"). A typical measured series inductance for clamped-mica capacitors is about 0.5 nH. The equivalent capacitance is calculated by subtracting the series lead inductance from the capacitive reactance, or $X_c(\text{equiv}) = X_c - X_{L(0.5\text{ nH})}$.

Since two capacitors are used in parallel, the total capacitance is derived as shown in Figure 4.

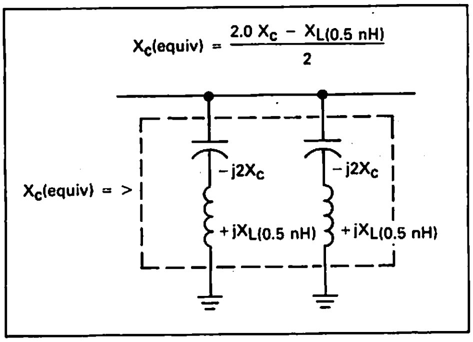

FIGURE 4 — EQUIVALENT REACTANCE FOR CAPACITORS IN PARALLEL

A value of 2.0 X_c is used in the above example since each capacitor will contribute only ½ to the total capacitance. By setting X_c(equiv.) equal to the parallel equivalent reactance calculated in Figure 3, the exact capacitor values may be determined.

$$X_p = \frac{2.0\,X_c - X_{L(0.5\,nH)}}{2}$$

$$X_c = \frac{2.0\,X_p + X_{L(0.5\,nH)}}{2} \qquad (X_c = 1/2\,fC)$$

$$C = \frac{1}{\pi f\,(2.0\,X_p + X_{L(0.5\,nH)})}$$

Introducing an actual example at this time should help in explaining the remaining steps involved in a test fixture design. The MRF846 is a 40 W, 12.5 V, 800 MHz device whose input and output impedances are:

TABLE 1 — Z_{in}, Z_{out} FOR MRF846

Frequency	Z_{in}	Z_{out}
800 MHz	1.1 + j4.8	1.20 + j2.4
836 MHz	1.0 + j4.9	1.15 + j2.5
870 MHz	1.0 + j5.0	1.10 + j2.7
900 MHz	0.9 + j5.1	1.10 + j2.8

Since X_p will vary as a function of frequency, C_I and C_O need only be calculated for one point within the frequency band. Typically, the input response of an RF power transistor is optimized about the center of the band. Hence, the input R_p and X_p are generally calculated at this frequency $[(f_h + f_l)/2]$.

The output response is different. If C_O were selected for a resonance to occur with X_p at band-center, an unacceptable performance roll-off would be seen at the upper end of the frequency band. Overall performance is best when C_O is calculated at a frequency within 20% of the upper end of the band. Since device gain increases as frequency decreases, the performance at lower frequencies is generally no problem.

Using the MRF846 as an example, input and output capacitor values may be determined as follows:

INPUT:

Frequency = 836 MHz

$Z_{in} = 1 + j4.9$
$= 4.9 \quad Q = 4.9/1$

$X_p = 4.9\left(1 + \frac{1}{(4.9)^2}\right)$
$= 5.1\ \Omega$

$X_{L(0.5\,nH)} = 2.0\pi (836 \times 10^6)(0.5 \times 10^{-9})$
$= 2.63\ \Omega$

$C = 1/[\pi(836 \times 10^6)(2 \times 5.1 + 2.63)] = 29.7$ pF

2–15 pF Capacitors would be the best choice.

OUTPUT:

Frequency = 870 MHz

$Z_o = 1.1 + j2.7;\ Q = 2.7/1.1$
$= 2.45$

$X_p = 2.7\left(1 + \frac{1}{(2.45)^2}\right)$
$= 3.15\ \Omega$

$X(0.5\,nH) = 2.0\pi (870 \times 10^6)(0.5 \times 10^{-9})$
$= 2.7\ \Omega$

$C = 1/[\pi(870 \times 10^6)(2 \times 3.15 + 2.7)] = 40.7$ pF

2–20 pF Capacitors would be the best choice.

(20 pF Capacitors were not available, so an 18 pF & a 24 pF capacitor were chosen instead. The total C = 42 pF.)

Though the MRF846 test fixture used at Motorola does use these capacitor values, the above calculations may act only as a good starting point. Empirical measurements and more precise impedance measurements for a given application may result in minor deviations from these values.

Assuming no additional circuit parasitics had to be accounted for, the quarter wave transmission line sections could now be determined. The input (and output) fixture wear blocks do, however, contribute additional series lead inductance to the impedances. These inductances are counteracted by the trim capacitors C'_I and C'_O. The wear block inductance could be calculated and then used to determine the proper capacitance values. However, since there are other, less obvious frequency and grounding effects which may influence the impedance transformation, it is a more practical (and generally a more accurate) procedure to measure the impedance which will be transformed by the transmission line to 50 Ω.

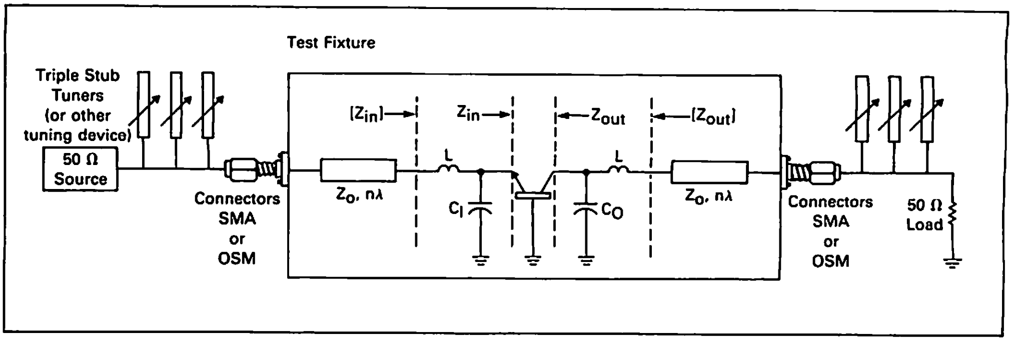

FIGURE 5 — BASIC CIRCUIT TO MEASURE Z_{in}, Z_{out}

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The capacitors C_I and C_O should be mounted into the test fixture and a known characteristic impedance transmission line soldered into place as shown below in Figure 5.

Triple stub tuners are used on the input and output to tune for maximum output power and minimum reflected power at various frequencies throughout the band. Band edges and band center are generally adequate for a good circuit design. Due to higher impedance levels produced by adding C_I and C_O, (Z_{in}) and (Z_{out}) are measured instead of the real transistor impedances, Z_{in} and Z_{out}. Also, by measuring impedances in the actual applications fixture, the design can be optimized for the particular fixture. Perhaps a maximum gain tuning point is not what is desired. Obtaining impedances for an efficiency/gain compromise may be more desirable. If this is the case, an impedance table for the appropriate conditions may be obtained. It is then for these impedances that C_I, C_O and Z_o will be calculated.

The procedure for obtaining the impedances is simple and requires a vector voltmeter (VVM) or a network analyzer. Both are used at Motorola, but a vector voltmeter is less expensive and if used with a high directivity directional coupler, (>40 dB), is very accurate. The set-up is constructed as shown in Figure 5. With frequency set, stub tuners are adjusted for the desired performance. Again, using the MRF846 as an example, numbers shown in Table 2 were measured for P_{in} = 12.0 W, V_{CC} = 12.5 V.

The output stub tuners were adjusted for maximum gain at each frequency and the input stub tuners were adjusted for zero watts reflected power. After each measurement, the impedance presented to the fixture by the triple stub tuner and load (or source) combination is measured by the vector voltmeter. The impedance is then translated by the transmission line used in the test fixture to obtain (Z_{in}) and (Z_{out}). In the above example a 26 Ω, 0.309λ (@836 MHz) transmission line was arbitrarily chosen to be in the MRF846 measurements. By using the equation: $Z \angle\theta = R_o\,[(1 + \Gamma\angle\theta)\,/\,(1 - \Gamma\angle\theta]$ or various computer or calculator programs, the transformation is easily calculated. The most important part of the whole procedure is obtaining an accurate measurement from the stub tuners. Prior to making any measurements, the vector voltmeter must be referenced to a short (180° on a Smith Chart). As a means of accounting for the errors introduced by the connectors at the fixture's input and output, that same connector is used for a referencing short as shown in Figure 6.

The measurement reference plane is now the edge of the connector used on the test fixture, which is also the beginning of the transmission line. Assuming the same reference plane is maintained during the measurements, an accurate impedance value will be produced. A good technique for maintaining the appropriate reference plane is accomplished by creating a new connector to measure the triple stub tuners. Two connectors are attached as shown in Figure 7.

TABLE 2 — PERFORMANCE OF MRF846 versus FREQUENCY

806 MHz	838 MHz	870 MHz
P_{out} = 50.0 W Eff. = 53.3% Prefl. = 0 W	P_{out} = 48.3 W Eff. = 55.2% Prefl. = 0 W	P_{out} = 44 W Eff. = 58% Prefl. = 0 W

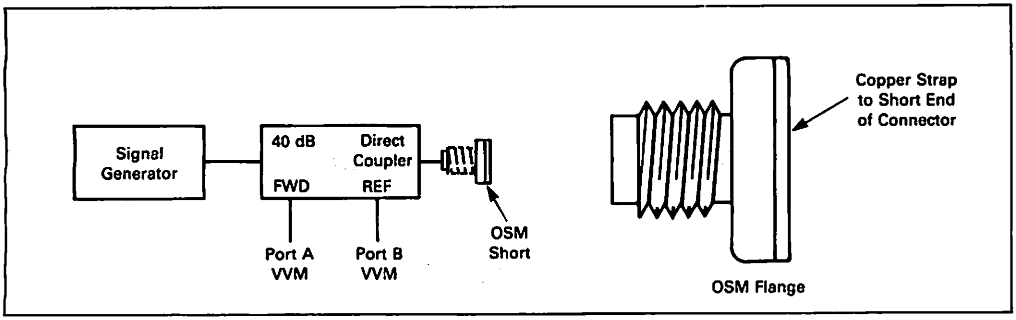

FIGURE 6 — ESTABLISHING REFERENCE PLANE

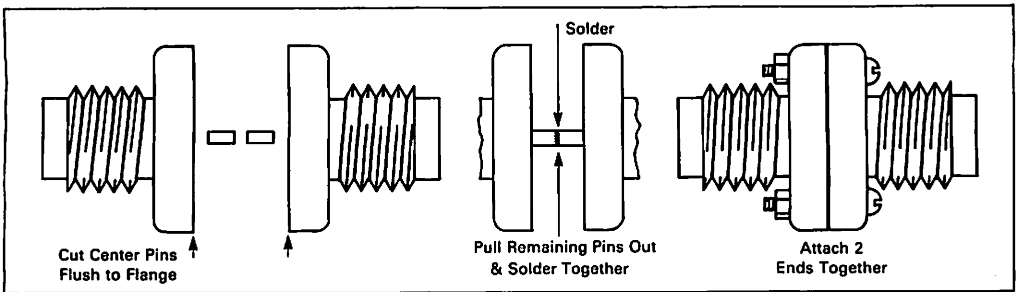

FIGURE 7 — MAINTAINING REFERENCE PLANE

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The triple stub tuner, load combination may now be measured with an adequate degree of accuracy using the test setup shown in Figure 8.

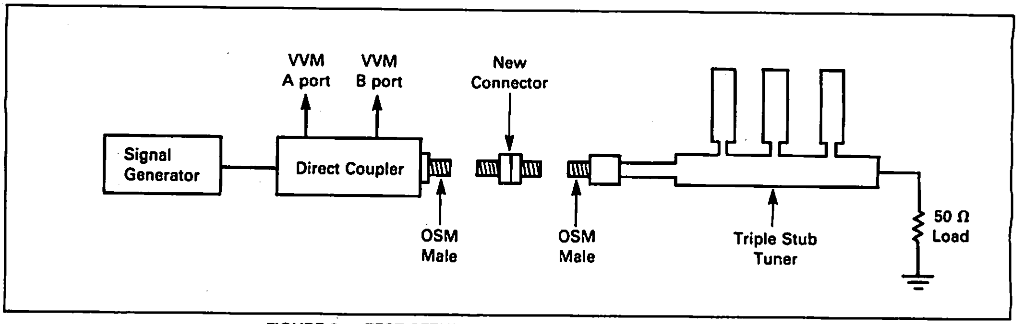

FIGURE 8 — TEST SETUP TO MEASURE STUB TUNER W/LOAD

Repeat the process for the input stub tuner combination. Two numbers are obtained for each frequency which (Z_{in}) and (Z_{out}) can be calculated from, as shown in the MRF846 example below:

TABLE 3 — MEASURED Z VALUES FOR TEST FIXTURE

Frequency		Measured $\Gamma\angle\theta$	$\Gamma\angle\theta$ converted to Impedance in Ohms	Impedance Transformed Over 26 Ω Line in Ohms
806 MHz	INPUT	$0.35\angle 155°$	24.97 + j8.42	20.72 − j5.64 = $[Z_{in}^*]$
	OUTPUT	$0.37\angle 144°$	24.86 + j12.53	17.72 − j6.66 = $[Z_{out}^*]$
838 MHz	INPUT	$0.26\angle 166°$	29.78 + j3.98	21.35 + j0 = $[Z_{in}^*]$
	OUTPUT	$0.22\angle 154°$	33.30 + j6.58	18.68 + j.74 = $[Z_{out}^*]$
870 MHz	INPUT	$0.14\angle -169°$	38.25 − j1.99	20.21 + j6.92 = $[Z_{in}^*]$
	OUTPUT	$0.07\angle -158°$	44.10 − j2.24	17.90 + j8.3 = $[Z_{out}^*]$

Note: $[Z_{out}^*]$ is conjugate of $[Z_{out}]$
$[Z_{in}^*]$ is conjugate of $[Z_{in}]$

The new impedances can be obtained by using a Smith Chart or using the equation $Z\angle\theta = R_0\,[(1 + \Gamma\angle\theta)/(1 - \Gamma\angle\theta)]$. These impedances (shown in the last column of Table 3) are the impedances which the test fixture will be optimized around. Once again, it is convenient to convert these numbers into parallel equivalents. By doing so, the values of C'_I and C'_O become more obvious. Table 4 shows this process.

TABLE 4 — CONVERSION OF Z VALUES TO C VALUES

Series Impedance $[Z_{in}]$ & $[Z_{out}]$	R_p	X_p	Capacitance Required
20.72 + j5.64	22.26	j81.8	2.42 pF C'_I
17.72 + j6.66	20.2	j53.8	3.67 pF C'_O
21.35 + j0	21.35	—	0.0 pF C'_I
18.68 + j.74	18.7	j472	0.40 pF C'_O
20.21 − j6.92	21.6	−j68.3	−2.68 pF C'_I
17.90 − j8.3	21.75	−j46.9	−3.90 pF C'_O

From Table 4, notice the calculated values of C_I and C_O come close to giving the desired frequency response. C'_I is zero at the band center, indicating the capacitors selected for the input are optimum. The values for C'_O produce a slight skew in performance toward the high end of the band. Capacitor values for the output could be reduced slightly, but they will remain the same until final fixture performance is determined.

Since C'_I and C'_O are very small capacitor values, little or no capacitance is actually needed for C'_I or C'_O. However, to allow minor tuning adjustments, a small trimmer capacitor is included at the wear block/transmission line interface.

The final calculation which needs to be performed is that of finding the optimum characteristic impedance for the transmission line. The recommended approach for doing this is to use a computer optimization program which will iterate any number of variables for a desired frequency response. The variables available to be optimized at this point are Z_0, C'_I and C'_O and even $n\lambda$ (transmission line length). Z_0, C'_I and C'_O are the very minimum variables.

In the example of the MRF846, where input R_p varies from 22.3 Ω to 21.6 Ω over the frequency band, a close approximation can be had by using a mean value of 21.9 Ω. This results in a Z_0 of 50 x 21.9 = 33 Ω. The output R_p starts at 20.2 Ω, dips to 18.7 Ω and goes back up to 21.75 Ω. Using the same method as before, Z_0 is calculated as 50 x 20.2 = 31.7 Ω where 20.2 Ω is the mean value of 18.7 and 21.75. Using a computer optimization program, a 32 Ω, quarter wave transmission line is optimum for the input and a 30 Ω quarter wave line is optimum for the output. These are the values used in the MRF846 test fixture.

After constructing the MRF846 test fixture and tuning the small trimmer capacitors for best overall gain and input reflected response, the average data shown in Figure 9 was obtained.

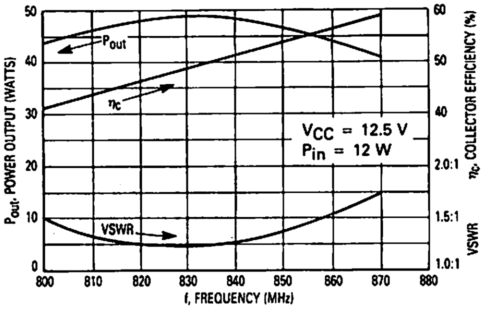

FIGURE 9 — TEST FIXTURE PERFORMANCE OF MRF846

The goal was to demonstrate 12/40 W across the band with less than 2.0:1 input VSWR and greater than 45% collector efficiency. Further optimization could be done by performing impedance measurements on additional transistors or characterizing the test fixture more accurately. However, the above performance is very satisfactory to the required performance. The best compromise for a second pass fixture would be to trade-off gain at 806 and 838 MHz for efficiency, and redesign input and output matching networks for the new impedance tables. This, of course, is only one of the many procedures which may be followed in developing an 800 MHz test fixture.

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MOUNTING TECHNIQUES FOR POWERMACRO TRANSISTOR

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For reliable operation, the PowerMacro plastic molded transistor must be properly mounted. Methods of mounting and heatsinking are discussed. Tradeoffs of implementation and thermal performance are considered.

INTRODUCTION

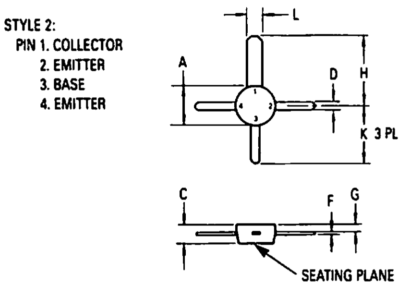
The Stripline Opposed Emitter (SOE) package when used to mount an RF power transistor for output power levels less than 2.0 watts is excellent electrically but relatively expensive for the function performed. This application note describes an equally effective electrical package called the PowerMacro package.

The primary advantages of the PowerMacro package are (1) its low cost and (2) that it is a drop-in replacement for the 0.204" SOE pill or stud package using the same transistor die. Note that this package will also substitute for most low power applications of an SOE device with comparable RF and thermal performance.

The PowerMacro package has excellent thermal properties; however, it is essential to utilize proper mounting techniques. Therefore, this application note emphasizes thermal considerations and methods of heat sinking the package.

DESCRIPTION OF THE POWERMACRO PACKAGE

Figure 1 is the case outline drawing of the Power Macro package. It is similar to the Macro-X package except for the wider collector lead. Figure 2 is a cut away view showing the component parts of a PowerMacro package. The package consists of an epoxy molded copper leadframe which has a 100 mil wide collector lead. A transistor die is silicon-gold eutectic die bonded to the collector lead and is wirebonded in a manner similar to the SOE package. Completion of the assembly process is accomplished by molding the copper leadframe and tin plating the four leads.



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.63	1.01	0.025	0.040
H	8.84	9.72	0.348	0.383
K	7.24	8.13	0.285	0.320
L	2.46	2.64	0.097	0.104

FIGURE 1 — Case Outline Drawing of the PowerMacro Package

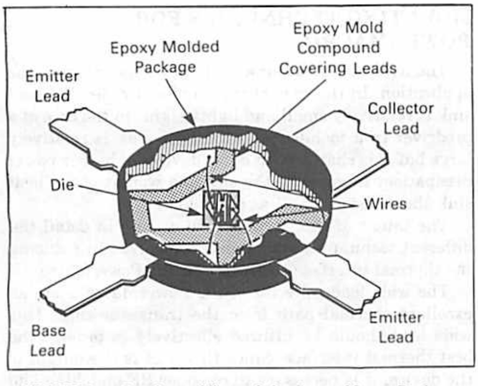


FIGURE 2 — Cut Away View of the PowerMacro Package

THERMAL RATING OF THE POWER MACRO TRANSISTOR

The RF PowerMacro transistor is guaranteed to have a certain thermal performance defined by the total device dissipation, P_D, at a certain case temperature, T_C, which is measured on the collector lead immediately adjacent to the package body. The parameters are defined for T_J max of 150°C. In order to use the thermal data presented on the RF data sheet, the concepts and ground rules for heat flow must be defined. Table 1 compares the thermal parameters to their more familiar electrical analogs. The task of the designer is to get the heat out the collector *lead (case) of the PowerMacro transistor.* This presents a classical heat transfer problem ideally calling for an "infinite heat sink" which can absorb any amount of heat with no temperature rise, ΔT, whatsoever. In a realistic sense, such a heat sink does not exist; however, a practical solution can be obtained. A practical heat sink is characterized by a certain temperature rise, ΔT, for a given ambient condition with a known amount of heat input or power dissipation, P_D.

TABLE 1. Thermal Parameter and Their Electrical Analogs

Symbol	Thermal Parameter	Units*	Electrical Analog Symbol	Electrical Analog Parameter
ΔT	Temperature Difference	°C	V	Voltage
H	Heat Flow	Watts	I	Current
θ	Thermal Resistance	°C/Watts	R	Resistance
γ	Heat Capacity	$\frac{\text{Watt-Sec}}{°C}$	C	Capacity
K	Thermal Conductivity	$\frac{\text{Cal}}{\text{Sec-cm}}$ °C	σ	Conductivity
Q	Quantity of Heat	Cal	q	Charge
t	Time	Sec	t	Time
$\theta\gamma$	Thermal Time Constant	Sec	RC	Time Constant

*Note the one major difference in thermal and electrical units — Q is in units of energy, whereas q is simply charge. Hence, H is in units of power and may be equated to an electrical power dissipation.

When the collector lead and ambient temperature of PowerMacro transistor and power dissipation are known, then the thermal resistance from case-to-ambient can be calculated. First, the power being dissipated in the device, P_D, is obtained by:

$$P_D = P_{DC} + P_{in} \text{-} P_{out} - P_{ref}$$

Where: P_D = Power dissipated in transistor in watts;
P_{DC} = DC power into transistor in watts;
P_{in} = RF power into transistor in watts;
P_{out} = RF power out of the transistor in watts;
P_{ref} = RF input power reflected in watts;
P_D is used in the equation below to obtain θ_{CA}.

$$\theta_{CA} = \frac{T_C - T_A}{P_D}$$

Where: θ_{CA} = Thermal resistance device case to ambient
T_C = Device case temperature
T_A = Ambient temperature
The junction temperature under a given operating condition is defined by:

$$T_J = (\theta_{JC} + \theta_{CA}) P_D + T_A$$

Where: T_J = Junction temperature
θ_{JC} = Published thermal resistance junction-to-case.

Since θ_{JC} is fixed by the transistor type used, the user can only control the junction temperature by θ_{CA}.

A low θ_{CA} requires an effective heat sink and interface between the case and heat sink. In general, an effective heat sink requires that materials with high thermal conductivity and high specific heat be used. A table of thermal properties for various materials is found in the Appendix. A well designed interface and heat sink requires that all thermal paths be as short as possible and of maximum cross sectional area.

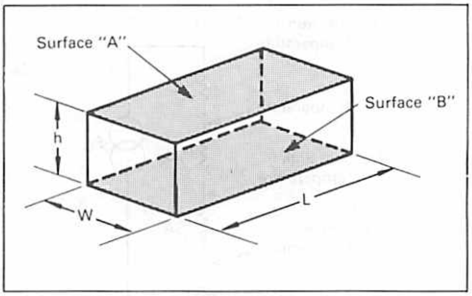


FIGURE 3 — Bar of Conducting Material

The thermal resistivity from Surface A to Surface B in the conductive bar shown in Figure 3 is:

$$\theta = \frac{h}{KWL} = \frac{h}{KA}$$

Where: h = Length of thermal path
A = Cross-sectional area of thermal path
K = Thermal conductivity

In order to define the thermal resistance factors still further for our purpose, θ_{CA} is defined as:

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Where: θ_{CS} = Interface thermal resistance — case to heat sink
θ_{SA} = Heat sink thermal resistance — heat sink to ambient

Thus the thermal resistance, junction-to-ambient is the sum of individual components and T_J is then defined as:

$$T_J = P_D(\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A$$

This gives the basic thermal resistance model for the PowerMacro as indicated by Figure 4.

The thermal resistance of the transistor (the junction-to-case thermal resistance), θ_{JC}, is not constant; it is a function of biasing and temperature as given on the data sheet. The thermal resistance of the heat sink is also variable; it decreases as ambient temperature increases.

The interface thermal resistance, θ_{CS}, is affected by the mounting technique and interface material used.

Since this thermal resistance may be significant compared to the others, it will receive primary emphasis in the following section on mounting techniques.

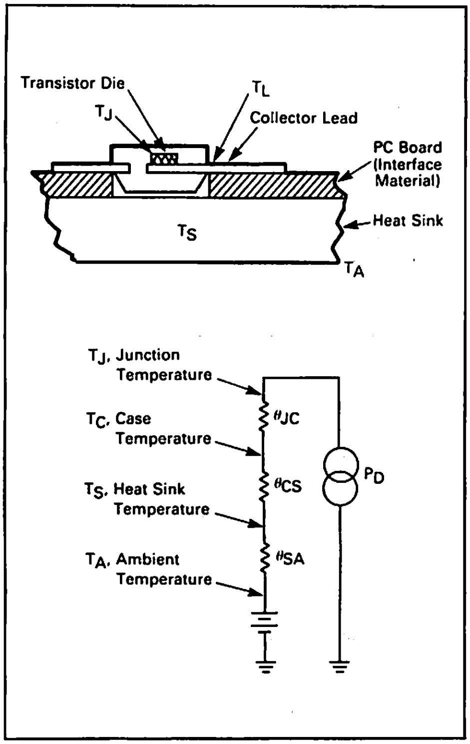


FIGURE 4 — Thermal Resistance Model for the PowerMacro Transistor

MOUNTING TECHNIQUES FOR POWERMACRO

The available heat sink will vary depending on the application. In the case of the handheld radio, the heat sink is relatively small and lightweight. In the case of a predriver in a mobile radio the heat sink is relatively large but it is shared with other devices of higher power dissipation. In general, the size and weight of the heat sink should be as small as possible.

The intent of this section is to discuss in detail the different techniques and tradeoffs involved in reducing the thermal interface resistance in the PowerMacro.

The wide lead collector of the PowerMacro offers an excellent thermal path from the transistor chip. This wide lead should be utilized effectively to provide the best thermal interface. Since this lead is the output of the device, it is necessary to consider RF matching and DC biasing. Thus, the lead is usually mounted to some PC board material such as G-10, glass teflon, alumina, or beryllium oxide (BeO). Table A1 in the Appendix lists the typical thermal data from IR scans of the MRF553 PowerMacro transistor (1.5 Watts P_{out} — 7.5/12.5 V VHF device). The analysis compares two PC board materials:

1. G-10
2. Alumina

for various operating conditions of P_{out}, P_D, T_J (die junction temperature), T_C (collector lead temperature), and T_S (heat sink temperature) and $T_A \approx 25°C$.

Figure A1 shows the circuit used to provide the thermal data of the MRF553 device mounted to a 62 mil thick G-10 PC board. The device is soldered to the PC board which is mounted to a 3″ x 5″ x 3/4″ aluminum heat sink.

Figure A2 shows the circuit used to provide the thermal data of the MRF553 device mounted with alumina interface. The device is soldered into a specially constructed socket (see Figure A3) which is mounted to a 3″ x 5″ x 3/4″ aluminum heat sink. The socket is copper and uses 28 mils thick alumina substrates (195 mils x 250 mils) with 62 mils thick copper tabs (125 mils x 250 mils) on the input and output. These components are soldered together using high temperature solder.

A comparison of the data in Table A1 shows the relative performance of the two mounting techniques. IR Scan II of the alumina/copper mounting technique clearly shows its superior thermal performance. Comparing the data at $P_D \approx 1.9$ watts for IR Scan I (G-10 PC board mounting) and IR Scan II (alumina/copper mounting) demonstrate the better thermal interface using alumina/copper. θ_{JS} for the alumina/copper mounting is 30.7°C/W while θ_{JS} for the G-10 PC board is 39°C/W.

As expected, the θ_{JL} is approximately the same for the two mounting techniques. The difference in θ_{JS} is dependent on the mounting technique used. The resulting θ_{CS} is calculated from the IR scan data by:

$$\theta_{CS} = \theta_{JS} - \theta_{JL}$$

Thus for IR Scan I (G-10 mounting):

$$\theta_{CS} = (39–23.2)\ °C/W = 15.8°C/W$$

Whereas, for Scan II (alumina/copper mounting):

$$\theta_{CS} = (30.7–24.4)\ °C/W = 6.3°C/W$$

Therefore, the IR scan results show a marked improvement in thermal performance when using the alumina/copper.

The heat spreading effects of the epoxy mold compound are also analyzed by IR scan of a molded device and an unmolded device. The molded device was chemically etched to expose the surface of the transistor die while maintaining the maximum epoxy compound around the transistor leads. The unmolded device was soldered into the RF circuit in leadframe form and then the lead interconnects were trimmed to make the part functional.

A comparison of RF Scan I and RF Scan III shows that the epoxy mold compound aids in spreading the heat from the collector lead to the other three leads. For example, at $P_D \approx 1.9$ watts, the junction temperature, T_J, of the molded device is only 106.2°C versus 154.3°C for the unmolded device. Thus, the heat transfer ability of the epoxy mold compound is significant.

Additional heat transfer can be realized by applying a small amount of heat sink compound to the heat sink side of the PowerMacro package and by mounting the device so that the package body contacts the heat sink. The thermal conductivity of the heat sink compound (K = 0.0018) is close to that of the epoxy mold compound (K = 0.0026) and it is 3 times better than G-10 (K = 0.0056). Table A2 in the Appendix lists and defines the thermal conductivity K, the specific heat S and mass density P of various materials.

SUMMARY

This application note utilizes the IR scan results in Table A1 to quantify the tradeoffs in performance of the two mounting techniques. A more rigorous analysis should be made by the designer when considering a particular application of a PowerMacro device. In a particular application, there usually are certain constraints, such as:

(1) Ambient and operating conditions
(2) Available heat sink size
(3) Available circuit layout space
(4) PC board material choice
(5) Assembly manufacturing techniques that are available and cost effective

These constraints may limit the designer's available options in providing the best interface and heat sink for the PowerMacro transistor.

The PowerMacro package is an excellent RF low power package. With proper mounting and applications of device specifications, the transistor will function reliably. The data sheet specifications for θ_{JL}, T_L, and P_D are based on mounting the device to G-10 PC board or equivalent at $T_A = 25°C$.

APPENDIX

Table A1 lists the IR scan results of the MRF553 PowerMacro transistor comparing two PC board materials. The mounting and RF circuit techniques are shown in Figures A1, A2 and A3.

TABLE A1. IR Scan Results for MRF553 PowerMacro

Mounting Technique	P_{out} (W) f = 175 MHz	P_{in} (mW) / P_R (mW)	V_{CC} (Vdc) / I_C (A)	P_D (W)	Die Temp. T_J (°C) Hot Spot	Die Temp. T_J (°C) Aver.	Collector Lead Temp. T_L (°C)	θ_{JL} Aver. (°C/W)	θ_{JL} Hot Spot (°C/W)	Ckt. Heatsink Temp. T_S (°C)	θ_{JS} Aver. (°C/W)	θ_{JS} Hot Spot (°C/W)	T_A (°C) Ambient Temp.
IR Scan I:	1.0	55 / 3.8	12.5 / 0.20	1.55	96.62	99.5	55.3	25.3	26.65	32	40.3	41.7	25
G-10 PC Board with Epoxy (Case Material)	1.5	88 / 8.4	12.5 / 0.25	1.70	101.40	99.1	59.7	23.2	24.5	32	39.5	40.8	25
	2.0	140 / 14	12.5 / 0.30	1.88	108.9	106.2	62.7	23.2	24.6	33	38.95	40.4	25
	2.5	222 / 21.5	12.5 / 0.35	2.08	120	116.9	67.35	23.8	25.3	35	39.4	40.9	25
	3.0	380 / 40	12.5 / 0.41	2.46	138.35	134.8	74.2	224.6	26.1	37	39.75	41.2	25
IR Scan II:	1.5	75 / 3.7	12.5 / 0.200	1.07	68	66.7	33.8	24.5	26.7	28	36.2	37.4	25
Alumina/ Copper Board with Epoxy (Case Material)	2.0	135 / 13	12.5 / 0.252	1.27	73.8	71.9	35.3	24.3	25.8	29	33.8	35.3	25
	2.5	350 / 60	12.5 / 0.33	1.92	90	88	41.1	24.4	25.5	29	30.7	31.8	25
	3.0	710 / 165	12.5 / 0.430	3.0	120.5	117.7	48.8	23.4	24.3	29	29.7	30.7	25
	3.2	1000 / 300	12.5 / 0.473	3.4	136.8	131.3	49	24.2	25.8	29	30.1	31.7	25
IR Scan III:	1.0	52 / 7.6	12.5 / 0.20	1.54	138.99	137.1	91.9	29.2	30.5	28	70.8	72.1	25
G-10 PC Board with No Epoxy (Case Material)	1.5	84 / 11	12.5 / 0.25	1.69	146.28	143.5	95.6	28.2	29.8	28	68	69.7	25
	2.0	140 / 16	12.5 / 0.30	1.87	156.64	154.3	101.35	28.35	29.6	28	67.4	68.6	25

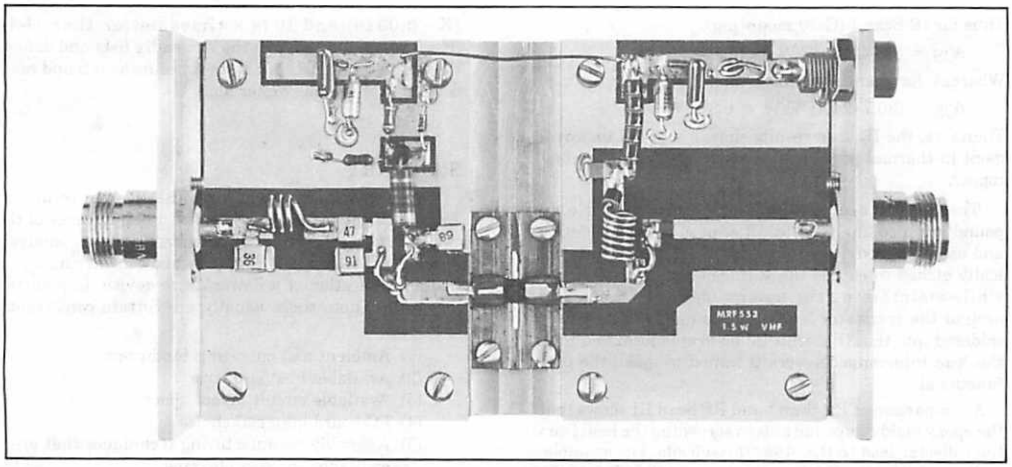


FIGURE A1 — Circuit Using G-10 PC Board

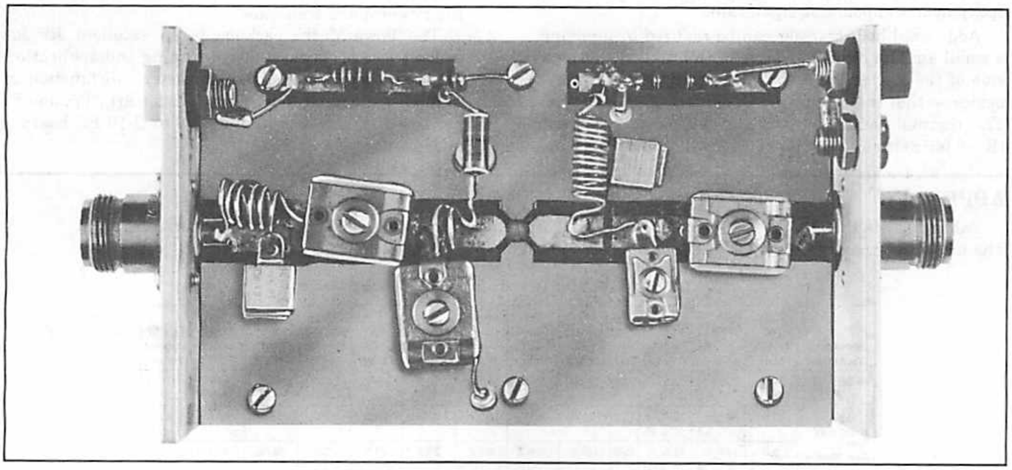


FIGURE A2 — Circuit Using Alumina/
Copper Socket

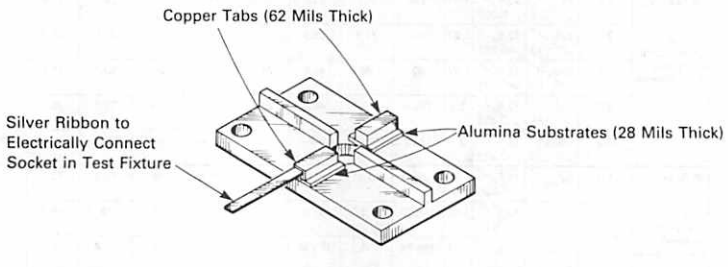


FIGURE A3 — Alumina/Copper Socket

The IR scans were made using a Barnes radiometric scope (Model No. RM2). The transistor's active area was IR measured at 6 points to adequately map the junction temperature. Also, the collector lead was IR measured immediately adjacent to the body of the package to obtain the case temperature, T_L of the device (see Figure A4).

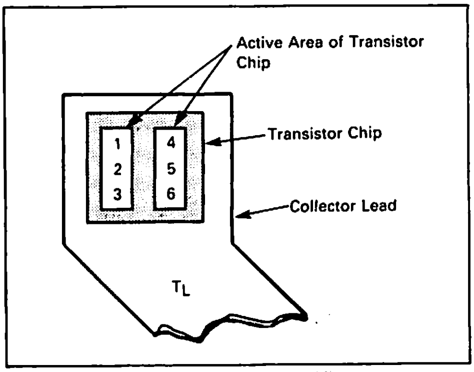


FIGURE A4 — IR Scan Map

Each operating condition chosen was allowed to reach steady state before the IR scan measurements were made.

In order to aid in heat sinking and mounting designs a table of thermal properties of common materials is presented. Three important thermal properties of common heat sink materials are given in Table A2. These properties should be considered in order to properly evaluate the choice of materials used in heat sinking/mounting of a PowerMacro for a given application.

Thermal Conductivity is a measure of the ability of a material of known cross sectional area to transfer heat a given distance in a given time with a given temperature difference. Generally metals are good thermal conductors.

Specific Heat is a measure of the amount of heat a given mass of material can accept for a given rise in temperature. The scale is normalized to the heat capacity of water (H_2O = 1.0).

Mass Density is simply the mass per unit volume of a material. This parameter is important in heat sink design in as much as large heat sinks of dense materials are undesirable.

The devices were decapsulated using a machine called a "Jet Etch." This machine is manufactured by:

B & G Enterprises
62B Hanger Way
Watsonville, California 95076-2486

The jet etch machine uses hot sulfuric acid to decapsulate the molded device. The device can be decapsulated so that there is no mechanical damage, no corrosive damage, and no loosening of external leads. Thus, the device is fully RF functional.

TABLE A2. Typical Thermal Properties of Materials

Material	Thermal Conductivity K (Cal/Sec-cm-°C)*	Specific Heat S (Cal/gm-°C)	Mass Density, P (gm/cm-°C)
Copper	0.94	0.093	8.9
Beryllia Ceramic	0.55	0.31	2.8
Aluminum	0.49	0.22	2.7
Brass	0.26	0.094	8.6
Silicon	0.20	0.18	2.4
Steel	0.12	0.12	7.8
Solder	0.09	0.04	8.7
Kovar	0.046	0.11	8.2
Alumina Ceramic	0.04	0.21	3.7
Plastic Epoxy	0.0026	0.2	2.0
Glass	0.0026	0.2	2.0
Mica	0.0018	0.2	3.2
Teflon	0.00056	0.25	2.2
Heatsink Compound	0.0018	—	—

*Conversion Factor: 1 watt/m = 2.39 x 10^{-3} Cal/Sec. cm. The thermochemical calorie = 4.184 joules. The absolute joule per second or watt is thus related in terms of calorie per second.

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A Cost Effective VHF Amplifier For Land Mobile Radios

By Ken Dufour
Motorola Power Products Division

INTRODUCTION

This application note describes a two stage, 30 watt VHF amplifier featuring high-gain, broad bandwidth and outstanding ruggedness to load mismatch, achieved by use of the new MRF1946A power transistor. It uses a die geometry intended for RF power devices operating in the UHF region. The emitter periphery (EP) to base area (BA) ratio of this die is 4.9, up from the normal EP/BA range of 1.5 to 3.5 for VHF devices. Power sharing and current sharing in the chip are controlled with diffused emitter resistors. The end result is a VHF transistor with very high power gain (10 + dB), sufficient so that processing steps can be taken to provide tolerance to load mismatch while still maintaining excellent performance. By mounting this die in the 0.380 flange or stud package and providing characterization data that spans 136 to 220 MHz, Motorola has provided a very versatile component for the RF designer.

CIRCUIT DESCRIPTION

Smith chart techniques were used to develop the two stage amplifier shown pictorially in Figure 1 and schematically in Figure 2. The end result is an amplifier that can produce 20 dB overall gain in the specified band (150 to 175 MHz), with a midband efficiency of 50 percent. The Motorola MRF237 was selected for the driver stage. This

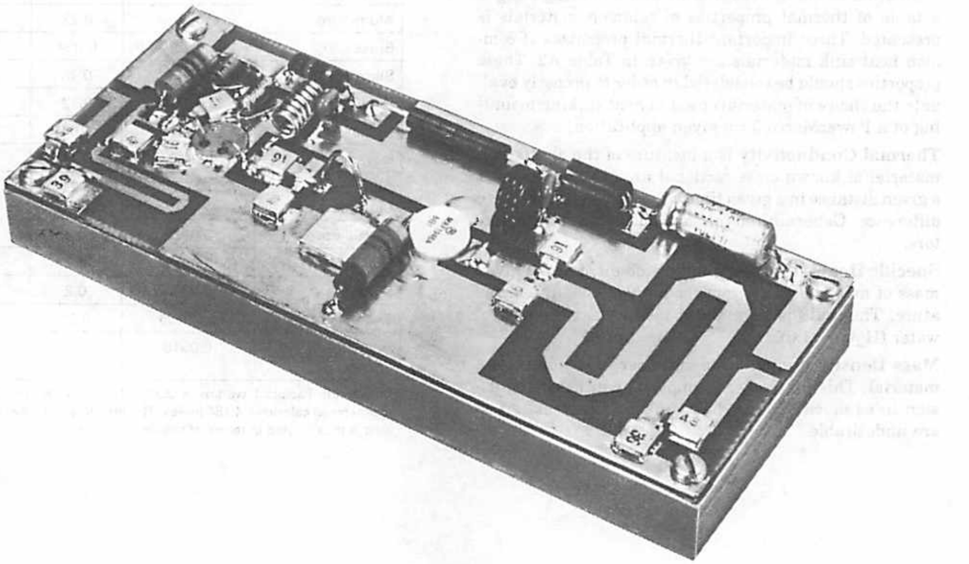
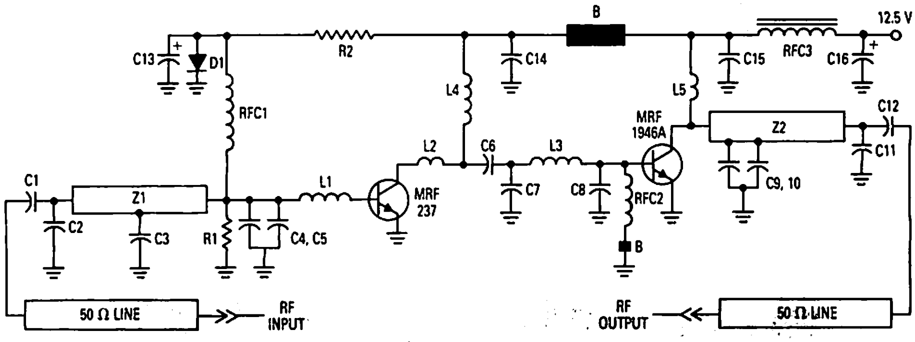


Figure 1. Engineering Model of MRF1946A Wideband Amplifier

common emitter (TO-39) RF power transistor produces high-gain, is easy to mount and is cost effective. In this design, the MRF237 is inserted into a hole in the circuit board and soldered to the ground plane for heat sinking, as shown in Figures 1 and 3. This method of attachment also provides a very effective emitter ground connection. By introducing a small amount of forward bias (5–15 mA) to the MRF237, it will track low drive levels and help maintain stability in the input stage. The amplifier is constructed on 1/16", double sided G-10 board with 2 ounce copper cladding. A photomaster of the printed circuit board is shown in Figure 4. The top and bottom ground planes of the board are connected by wrapping the board edges with thin copper foil (0.002") and then soldering it in place. Figures 1 and 3 illustrate how and where the board edges are wrapped in the prototype amplifier. No eyelets or plated-through-holes are required to achieve the level of performance noted here. Printed lines are used to match the devices' input and output impedance to 50 ohms, and an inductor and two capacitors form the interstage match. This allows some flexibility in shaping the overall frequency response and helps conserve board area. The MRF1946A stage is operated in Class C and is mounted to the heatsink using conventional methods, i.e.; an 8–32 stud inserted into an appropriately prepared heatsink. An alternate packaging arrangement, the 0.380 flange, allows one to attach the transistor to the topside of the heatsink with two screws. A Motorola Application Note on mounting techniques for various semiconductors is available and provides detailed information on installing either of these package styles (see reference 1). Additional information on thermal considerations can be found in reference 2. Performance of the amplifier is illustrated in Figures 5, 6 and 7. Figure 5 is a plot of P_{out} versus P_{in} at 160 MHz, 12.5 volts; Figure 6 shows output power, input VSWR and collector efficiency as functions of frequency; while Figure 7 demonstrates harmonic content for 30 watts output power.



C1 = 56 pF Dura Mica
C2 = 39 pF Mini-Unelco
C3, C7 = 68 pF Mini-Unelco
C4, C5, C6, C9, C10 = 91 pF Mini-Unelco
C8 = 250 pF Unelco J101
C11 = 36 pF Mini-Unelco
C12 = 43 pF Mini-Unelco
C13 = 1 μF, 25 V Tantalum
C14, C15 = 0.1 μF Mono-Block
C16 = 10 μF 25 V Electrolytic
D1 = Diode, 1N4933 or Equivalent
L1 = Base Lead Cut to 0.4", Formed Into Loop
L2 = Collector Lead Cut To 0.35", Formed Into Loop
L3 = 0.7" #18 AWG Into Loop
L4 = 7 Turns #18 AWG, 1/8" ID
L5 = 3 Turns #16 Enam, 3/16" ID
R1 = 10 Ω, 1/4 W Carbon
R2 = 1500 Ω, 1/2 W (Select For Most Appropriate ICQ)
RFC1 = 10 μH Molded Choke
RFC2 = 0.15 μH Molded Choke
RFC3 = VK200-4B Choke
Z1, Z2 = Printed Line
Z3 = 50 Ohm Printed Line
B = Ferroxcube Ferrite Bead 56-590-65-3B

Figure 2. Schematic Diagram of MRF1946A Wideband Amplifier

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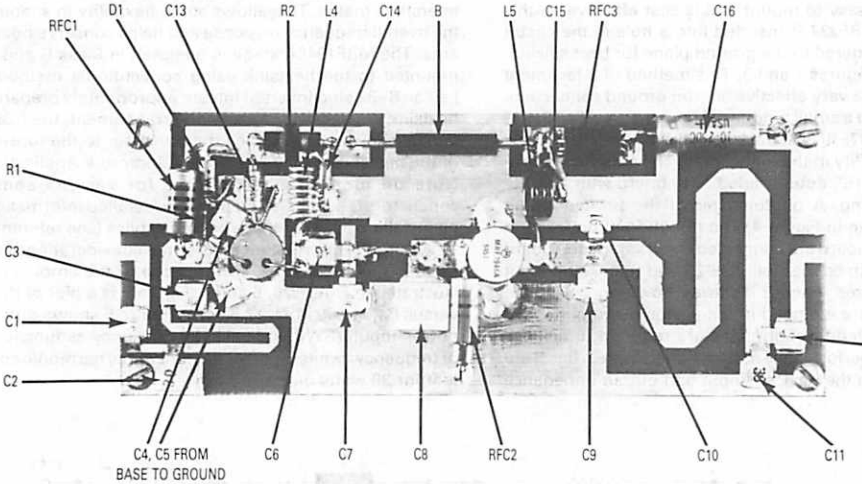
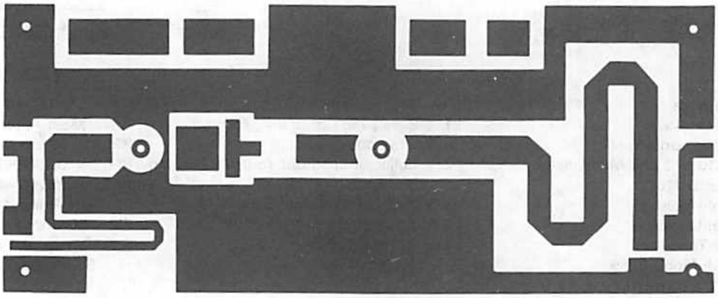


Figure 3. Parts Placement



NOTE: The Printed Circuit Board shown is 75% of the original.

Figure 4. PCB Photomaster

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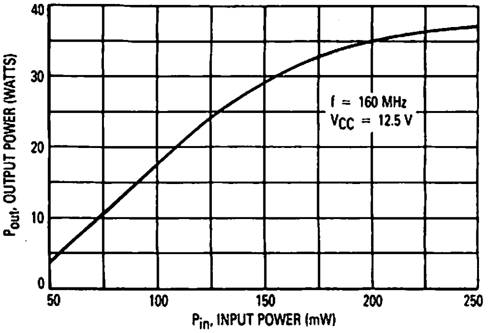

Figure 5. Output Power versus Input Power

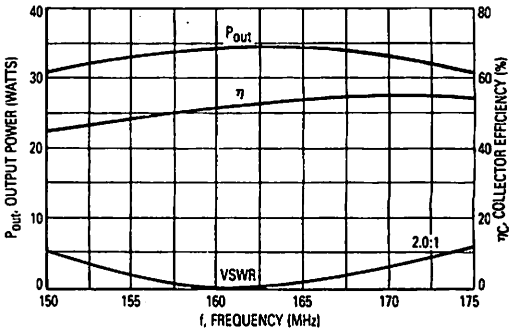

Figure 6. Output Power, Efficiency, and Input VSWR versus Frequency

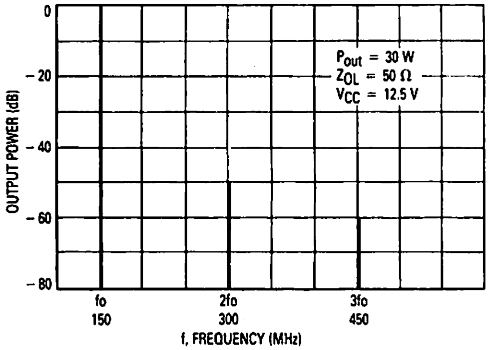

Figure 7. Output Spectrum

CONCLUSIONS

The two-stage amplifier described produces greater than 20 dB gain with 30 watts of output power over the frequency range of 150 to 175 MHz. Ruggedness and stability are achieved by use of the new MRF1946/A power transistor. The amplifier illustrates that relatively unsophisticated construction techniques properly implemented with the appropriate high gain devices can provide a cost effective 30 watt VHF amplifier for land mobile applications.

REFERENCES

1. Roehr, Bill: Mounting Techniques for Power Semiconductors, AN778. Motorola Semiconductor Products, Inc.
2. Johnsen, Robert J.: Thermal Rating of RF Power Transistors, AN790. Motorola Semiconductor Products, Inc.

7

A HIGH-PERFORMANCE VIDEO AMPLIFIER FOR HIGH RESOLUTION CRT APPLICATIONS

I. INTRODUCTION

This application note describes the superior performance characteristics of Motorola CRT driver transistors in a state-of-the-art video amplifier. In particular, the high speed obtainable with low DC power consumption is shown. A circuit which is insensitive to load variations and interconnect methods is given.

II. APPROACH

The performance requirements for the amplifier are these:

Voltage Gain	20
Rise and fall times	3 nS
Output	40 V p-p min.
Overshoot	5% max.
Load capacitance	8 pF min.
Power supplies	60 V, 5 V, −5 V

The voltage gain is obtained in a transconductance amplifier in the form of a common-emitter, common-base cascode circuit. In this circuit the load capacitance is isolated from the cascode by a set of complementary emitter-followers. Thus, the capacitive loading on the cascode is low, which allows operation at a moderate dissipation level.

The emitter followers are biased at a Class "B" operating point. They conduct only during voltage transitions, while charging or discharging the CRT capacitance. This operation is similar to the way highly efficient C-MOS logic ICs function.

The emitter followers provide a combined output signal from a low impedance, or "stiff" source. This stiff source makes the entire circuit insensitive to load variations and to different methods of connecting the video amplifier to the CRT.

III. THE CIRCUIT

A. The Input Circuit

Refer to the circuit diagram in Figure 1. A fast pulse generator is required for accurate performance data. The Tektronix Model PG502 is a good example of a pulse generator for optimum performance, versatility and price considerations. The pulse generator has a rise time in the range of .8 ns and an output impedance of 50 ohms. A minimum-loss L-pad is used between the generator and the base of the driver transistor, Q_1. The impedance level at this point is designed to be 75 ohms. The voltage attenuation of the matching circuit is 0.64.

B. The Cascode Circuit

1. The Common-emitter stage uses an LT1001 transistor in a TO-39 package. The emitter current of 70 mA is supplied from a −5 V source via resistors R_4, and R_5. For ac, only R_4 at 15 ohms is operative. R_4 and the built-in emitter-ballast resistor of 1.6 ohms, determine the transconductance of Q_1, which is then 60 mA/V.

Both the emitter current and the collector current of this stage follow the base voltage almost instantaneously. Computer simulation has shown that the transition times are less than 1 ns. The transconductance may be increased during the transition times by adding the "peaking-network" R_6, C_2, C_3. Adding this network is very much like adjusting the rise time in the probes of fast oscilloscopes. In the cascade circuit under discussion the "peaking" network compensates rise time deterioration at the collector by speeding up the emitter current of Q_1. This procedure must be applied with moderation since it may affect the large-signal swing capability. The resistor, R_6, should be equal to or larger than R_4. The capacitor, C_2, determines the length of time during which "peaking" occurs. The product of R_6 and C_2 is typically a few nanoseconds. The trimmer, C_3, can be used for fine-tuning, but is usually not important and may be omitted. If there is lead inductance associated with the path from the emitter of Q_1 through C_3 to ground, use of C_3 may cause ringing at high frequencies.

2. The common-base stage uses an LT1817 transistor in a TO-117 package. Since the transistor must dissipate continuously some two Watts of DC power, good heatsinking is mandatory. The TO-117 package provides a high-conductance thermal path to a heatsink or chassis. At the same time, it adds only minimal capacitance to the circuit.

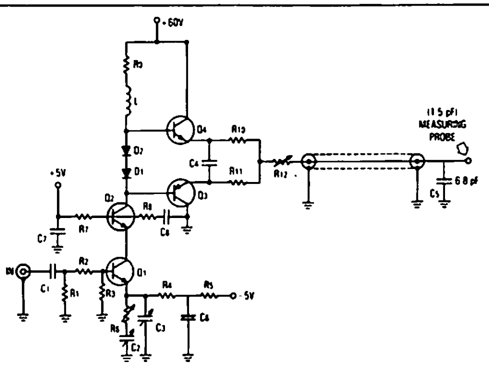

Figure 1. Circuit Diagram of Video Amplifier

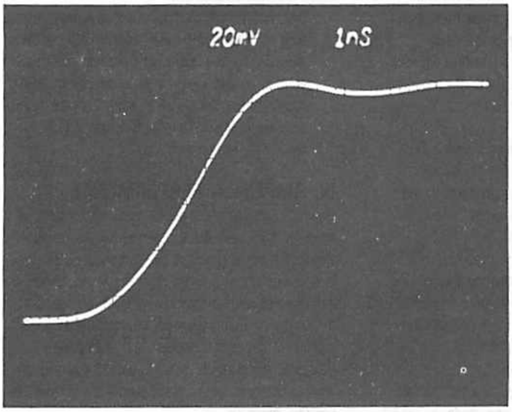

Figure 2A. Rise Time at 10 V p-p

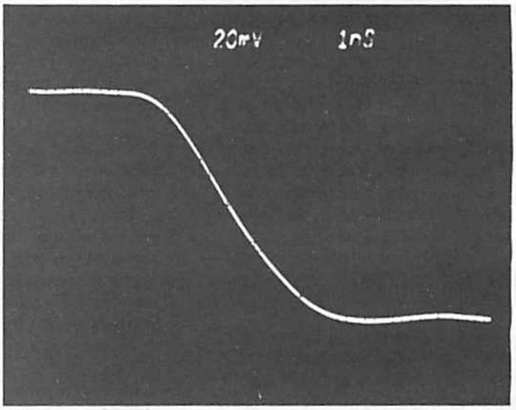

Figure 2B. Fall Time at 10 V p-p

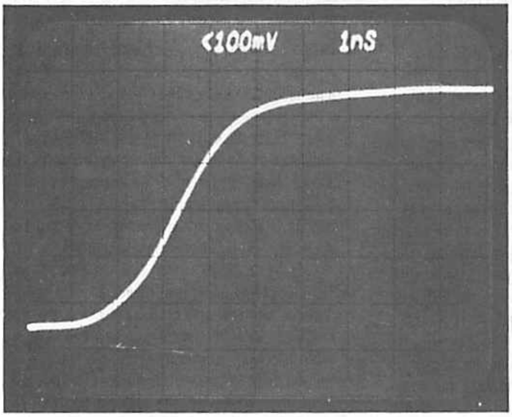

Figure 2C. Rise Time at 40 V p-p

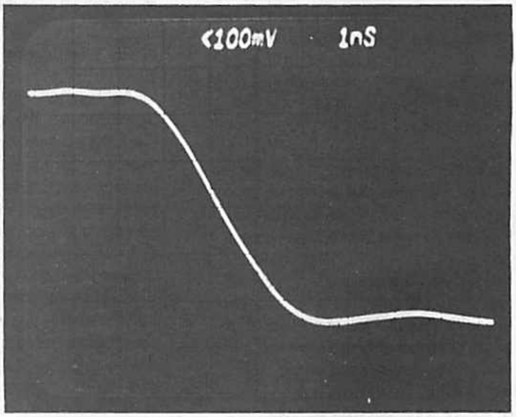

Figure 2D. Fall Time at 40 V p-p

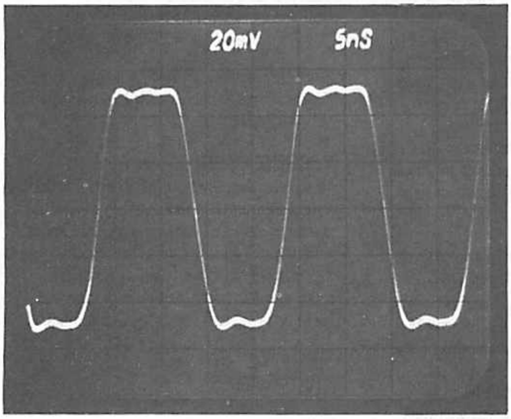

Figure 2E. 10 nsec Pixels 10 V p-p

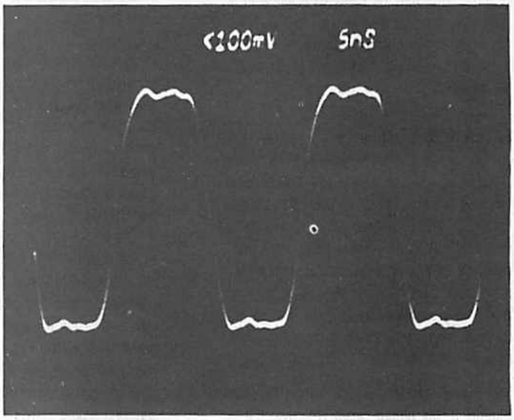

Figure 2F. 10 nsec Pixels 40 V p-p

The common-base stage has near unity current gain and acts as an impedance transformer, providing a current source at its collector. This current charges the combined collector capacitances of Q_2, and the emitter-followers, Q_3 and Q_4, which add up to about 5 pF at the operating point. To this total one must add about one pF of stray capacitance. A load- or "pull-up" resistor of 430 ohms is used at the collector of the common-base transistor, Q_2. The rise time at this point may be calculated to be:

$$t_r = .35 \cdot 2 \cdot \pi \cdot 430 \cdot 6\ \text{pF} = 5.7\ \text{nS}$$

This value is improved by the addition of a peaking coil of .22μH. Theoretically, the rise time could be reduced by up to 40% (without overshoot) by optimizing the inductance. Due to the non-linear nature of the capacitances to be compensated for here, different effects result for rise and fall times. This situation requires a compromise resulting in a practical improvement of less than the theoretical transition time. Nevertheless, 3 ns transition times are obtained at the collector of Q_2 by means of the emitter peaking discussed earlier.

The LT1817 is packaged in a common-base configuration. This means that the transistor base is connected to two symmetrical low-inductance base leads. As is well known, base-lead inductance may cause instabilities in common-base configurations. To prevent this from happening, base damping resistors, R_7 and R_8, have been added. The value of these resistors depends on the device bias point and the circuit layout. If oscillations occur, they would be near a Gigahertz or higher, and therefore may not be seen on anything but a sampling oscilloscope. They will affect rise times and output swing capability. Instabilities may be easily detected with a spectrum analyzer connected to the input jack of the video amplifier. Enough signal will feed back through the collector capacitance of Q_1 to reach the analyzer.

3. The emitter-followers, Q_3 and Q_4, are a complementary pair of transistors, LT1829 and LT5839, in TO-39 packages. The transistors are biased to the threshhold of conduction by two diodes, D_1 and D_2. These diodes should be relatively large, slow rectifier types, each providing no more than 0.6V of bias with a forward diode current of 70mA. The diodes have low, largely capacitive impedances at high frequencies, and should be connected with short leads between the bases of Q_3 and Q_4.

The emitter followers provide temporary charging currents to the output circuit whenever the voltage across the load is changed. In case of a display with high contrast and many transitions, the current in Q_3 and Q_4 may become appreciable, causing the transistors to heat up. The elevated junction temperature shifts the bias point from Class "B" in the direction of "AB."

If the emitters of these transistors were connected directly, a DC component of current would flow from the 60 V supply through the devices to ground. This "pole-current" would further heat up the junctions and might lead to thermal runaway. In the circuit described, this situation is prevented from occurring through the use of the emitter stabilizing resistors R_{10} and R_{11}. Using capacitor, C_4, prevents deterioration of the dynamic operation of the circuit.

A simpler, more primitive way to avoid thermal problems, is to use only one bias diode, or none at all. Doing this, however, has serious effects on the gray scale linearity at mid-range.

4. The output circuit. The LT1839 and LT5839 transistors have excellent peak current handling capabilities. Their emitter currents react virtually instantaneously to the base voltage. Even when supplying several hundred milliamperes of peak charging current, the base-to-emitter gain holds up well. It is therefore possible to drive more elaborate load configurations than a bare capacitance. This ability may ease interconnect problems. The circuit described in Figure 1 is powerful enough to accommodate a piece of shielded cable between the CRT and the video amplifier. A twin-lead line or a single wire connection may also be used instead of the shielded cable. The circuit is not only able to drive elaborate interconnect networks, but also to handle substantially larger CRT capacitances without significant penalties in rise and fall times. For instance, this circuit is capable of driving 15 pF with 3.8 ns transition times.

In all cases, the presence of additional reactive circuit elements causes the output circuit to have resonances which will cause ringing or overshoots, if the output circuit is not properly damped. To this end, a variable resistor, R_{12}, is included in the circuit. When adjusted for critical damping, the waveform will look smooth across the load capacitance.

In the demonstration circuit, (Fig. 1), a 6.5 pf chip capacitor simulates the CRT cathode capacitance. It is connected across a special jack, which has been designed for the Tektronix FET probe, Type 6201. Probe, jack and chip have a combined capacitance of 8pF. The FET probe may be used in conjunction with Tektronix sampling scopes or real-time scopes with bandwidths of 300 MHz or more.

One may be tempted to use slower instruments, such as a 200 MHz type, and correct mathematically for the additional transition time contributed by the scope. We do not recommend this approach since slower scopes appear to produce wave shape distortions which lead to misleading rise-time values.

IV. AMPLIFIER PERFORMANCE

Figure 2 contains photographs showing rise and fall times at 10 V and 40 V peak-to-peak swing. Also shown are some response curves generated by the well-known circuit analysis program SPICE. Careful modelling of the semiconductors used, according to the theory of Gummel and Poon, resulted in good agreement between computer and laboratory-generated performance data. In addition, computer analysis offers insights, which cannot be obtained by practical measurements.

Shown in Figure 3 are the superimposed plots of the input voltage at the base of Q_1 and the output voltage across the CRT capacitance. The second set of plots, Figure 4, displays the collector-current wave form of Q_1 and the combined emitter circuits of the complementary set of emitter followers. The collector current of Q_1 shows clearly the effect of "peaking," introduced by the emitter circuit components, R_6, C_2 and C_3. Note that under full swing conditions (40 V p-p output), the waveforms are not quite symmetrical. The effect on the transition times of the output voltage, however, is minimal.

The example shown in both Figures 3 and 4 corresponds to a pixel-time of 10 ns, which is the practical minimum for a system with 3 ns transitions. When operating continuously at this rate, approximately 25mA of average current flows in each one of the emitter-followers. This causes a significant rise in case temperature for these devices. It is therefore recommended that clip-on heat radiators be used. There is no electrical penalty for this measure, since the collectors are on ground potential.

Heatsinking becomes absolutely mandatory if one explores the limits of the amplifier by operating at 100 MHz and beyond.

V. CONCLUSION

An amplifier was developed which meets all needs of a high-resolution CRT monitor. While practical considerations played an important part in the circuit realization, the primary purpose was to demonstrate transistor capability. It is hoped that enough background information was given to allow the reader to tailor his circuit to his specific needs.

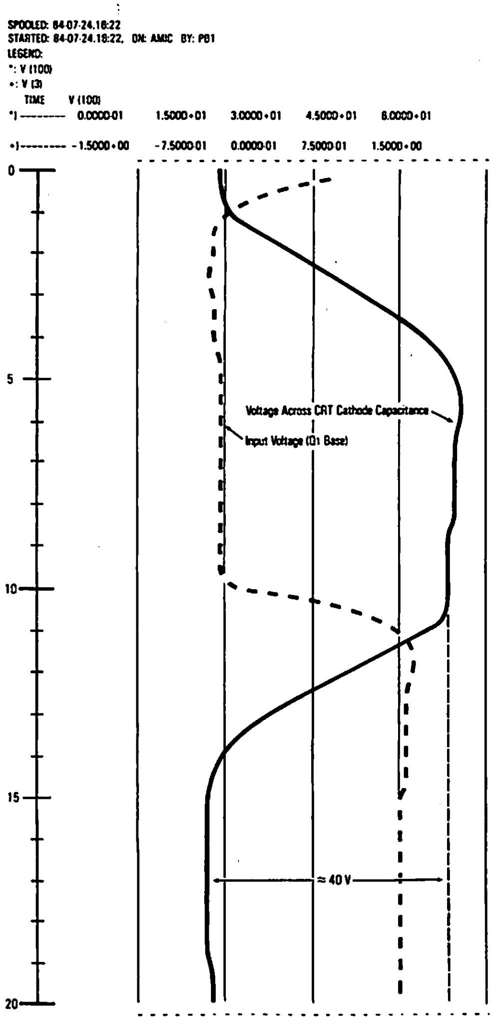

Figure 3. Computer Generated Voltage Plots

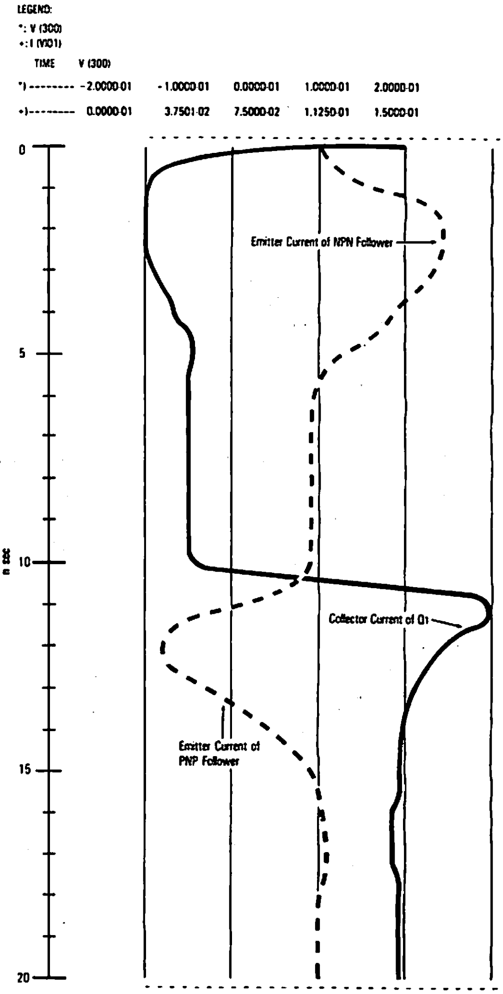

Figure 4. Computer Generated Current Waveforms

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A HYBRID VIDEO AMPLIFIER FOR HIGH RESOLUTION CRT APPLICATIONS

Motorola RF Devices has used their unique high frequency RF semiconductor capabilities and thin film hybrid expertise to produce a hybrid video amplifier with less than 2.9 ns rise and fall time for a 40 V output swing. This video amplifier provides a low power dissipation solution to a problem that has been limiting the performance of ultra high resolution CRT monitors: video amplifier speed. Many of the 1024 x 1024 and 1280 x 1024 pixel, 64 kHz horizontal sweep rate CRTs that are used in CAD/CAM and high resolution graphics applications have not realized their potential performance because of the speed of their video amplifiers. Video amplifiers with 3.5-4 ns rise and fall times often found in these high resolution CRTs do not provide optimum picture quality when the CRT has approximately *10 ns to energize* each pixel. A slow video amp will produce dimmer vertical lines than horizontal lines or may force monitor designers to other compromises such as a slower sweep rate which may produce flicker, or lower cathode voltage which will produce a dimmer picture. The hybrid described here solves these problems.

SUMMARY

The Video Amplifiers, CR2424 and CR2425, are hybrid integrated circuits designed for high resolution CRT Video Amplifier applications. They are capable of delivering 40 volts peak-to-peak output with overshoot typically less than 5% into an 8.5pf load. Typical 10-90% transition times are 2.6 nsec with a bandwidth of better than 130MHz. They have excellent gray-scale linearity, are dc coupled and do not require an external load-resistor.

CONSTRUCTION

A. Mechanical

The amplifier is housed in a proven package, which consists of a plastic housing, attached to an aluminum heatsink. Dimensions and pin configurations are shown on the attached specification sheets. The circuit uses special silicon transistors mounted on heat spreaders on an alumina substrate with thin-film resistors and gold metalization. The substrate is soldered to the heatsink.

The heatsink is supplied in two versions, CA Low Profile which is designated CR2424, and a taller heatsink version, CR2425. These two package styles are shown in Figure 1. The electrical characteristics of these two amplifiers are identical. The heatsink style choice should be based on ease of mechanical/electrical interface. In both cases, the heatsink is at ground potential and should be attached directly to the chassis or external heatsink for mechanical stability and heat conduction to ambient.

This CR2424 hybrid driver can also be supplied in a hermetically sealed package. The hermetic version is designated CR2424H and can be screened to Mil Std 883 method 5008.

B. Electrical

The circuit uses bipolar silicon transistors in a two-stage feed-back amplifier configuration. The output is supplied by emitter-followers. Because of the complementary circuitry employed, there is no need for a load (or pull-up) resistor.

The power consumption is typically 3.0 watts for average picture content and a maximum of 6.0W for 10ns continuous black to white transitions or worst case situations. The electrical pin connections are shown in Figure 2.

C. Thermal

Thermal analysis of an amplifier design is a very essential issue to ensure amplifier reliability. Heat is one of the most critical factors that determines how long the amplifier operates.

The ability to examine the CRT circuit thermally under operating conditions is absolutely necessary. The infrared microscanner was used for evaluation of the CRT hybrid amplifier from the standpoint of thermal resistance and operating temperature.

With the heatsink temperature stabilized at 60°C, the maximum transistor junction temperature was measured at 108°C. This is a very safe value, especially for devices with all gold metalization as used here. The maximum temperature occurs when the output voltage is either at its lower or upper extreme. Under this condition the maximum power dissipation on the die will be approximately 1.6W. Thus, the thermal resistance can be calculated to be 30°C/W.

Under normal operating conditions (normal operating conditions means an average picture content) the hottest transistor will dissipate approximately 1W. Again, with the heatsink temperature stabilized at 60°C, the transistor junction temperature will be 60°C + 30°C/W x 1W = 90°C. This is a very safe value for this kind of amplifier for a long life time.

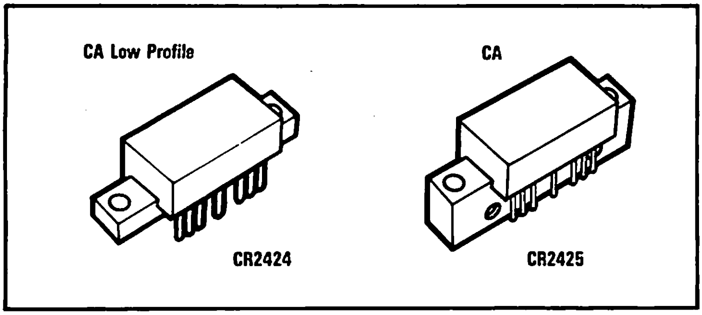
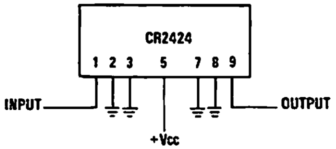


Figure 1. Package Types



(CASE 714G-01, STYLE 1)

Figure 2. Pin Configuration P/N CR2424

7

APPLICATIONS

A. Output Characteristics

The hybrid is intended to be used as the final stage of very fast video circuits. Properly driven, it can produce continuously alternating 10 nsec pixels with 40 volts swing and excellent brightness. The nominal load-capacitance is 8.5pf. Other values may be accommodated, since the output voltage is supplied by a pair of emitter followers, and is fairly insensitive to changes in load capacitance.

Often a wire connection of some length between the output of the module and the CRT cathode cannot be avoided. In this case a resonant circuit is formed, which may cause objectionable ringing or overshoot at its resonant frequency. To avoid this condition a damping resistor must be used in series with the lead inductance. For critical damping the value of this resistor becomes

$$R = 2 \cdot \sqrt{\frac{L}{C}} \quad (1)$$

A resistor is often desired at this position also for protection against arcing. In practice, the optimum value of resistance may be determined experimentally during the bread-boarding stage. Typical values are 50 to 100 ohms. The lead-inductance may be artificially increased by a few tenths of a microhenry to obtain a desired peaking effect. Any change in inductance will require readjustment of the damping resistance, as stated by Equation (1).

A short piece of cable (75 or 93 ohm) or 300 ohm twin-lead, terminated by a capacitance, will act similar to an inductance in the frequency range involved. In this case a damping resistor must also be used.

The output terminal of the hybrid is not short-circuit proof. Any resistance from this point to either ground or B+ should not be less than 600 ohms.

B. Input and Transfer Characteristics

The dc transfer characteristics of the module are shown in Figures 3, 4 and 5.

It is seen from Figure 3 that, at dc, an input current swing of ±6.25mA causes the output voltage to change by ± 20 volts. The next plot (see Figure 4) relates the input voltage, as measured at RF input port to the output voltage. The amplifier is phase-inverting. The ratio between these voltages is approximately 13.5. From the above values, one may calculate a low frequency input impedance of ~240 ohms at the RF input port.

Figure 5 is a plot that relates the input voltage, as measured immediately at module terminal 1, to the output voltage. The ratio between these voltages is approximately 230. From the above values, one may calculate a low-frequency input impedance of ~15 ohms at Pin 1.

Pin 1 is an internal dc feedback node and thus, as we can see, has a low impedance looking in from the outside. Pin 1 must be fed from a series network made up of a resistor with a shunt capacitor for high frequency pre-emphasis. An appropriate input network is shown in Figure 7 and is included as part of the standard test fixturing.

With the input terminal open, a dc level of approximately 1.4 volt exists at this point. Under this condition the module output voltage is approximately one-half of the supply voltage applied.

GENERAL CONSIDERATIONS

A. Test Circuit

The test circuit used to evaluate the hybrid module is shown in Figure 7.

The input is driven from a fast pulse generator, such as the Tektronix model PG502. It is important that the internal generator impedance is 50 ohms. It is also advisable to keep the cable length between the generator and the test circuit at a minimum; preferably only a barrel connector is used.

Since the module is dc coupled, the input drive voltage must be adjusted such that the driving wave form is centered around 1.4 volts. If the pulse generator used should not allow the setting of the dc level, a biasing current, injected at module terminal 1, through a resistor of more than 1 kiloohm, may be applied in order to adjust the desired quiescent point of the output voltage.

The output is taken from terminal 9 with an active FET oscilloscope probe fitted with a 100:1 voltage divider. This probe adds 1.5pf to the load capacitance, bringing the total load capacitance to 8.5 pf.

The input circuit contains a series resistor and capacitor in parallel, which is tuned for good response when driving with a 50 ohm pulse-generator. These components perform a RC "peaking" circuit.

B. Practical Circuits

The module is best driven from a low-impedance source, such as an emitter follower. The reader is invited to experiment with a circuit as shown in Figure 8.

The driver transistor can be an LT2001, biased at about 30mA. The collector lead must be by-passed for RF as close to the transistor as possible. For all common-collector (or common-base) circuits, a base resistor of ~20 ohms is recommended. It helps suppress spurious oscillations, which may occur in the GHz range and are difficult to detect. Resistors R_1, R_2 and R_3, and capacitor C_1 and coil L_1 are adjustable for desired circuit gain and response. Typical values may be:

$R_1 \approx 50\Omega$
$R_2 \approx 215\Omega$
$C_1 \approx 90pF$
$R_3 \approx 50\Omega$
$L_1 \approx 50nH$

The pulse generator used should allow changing the dc level in order to set a quiescent bias point of about 1.4V at the input of the module.

C. Frequency Response

In the literature and in many equipment specifications frequency response and rise-times are often treated as having a fixed relationship. The equation frequently quoted is

$$t_{r(10\text{-}90\%)} = .35 \; f_{3dB} \quad (2)$$

It can be shown that (2) indeed applies for the simple case of a single-pole R-C network. In reality, video amplifiers have much more complicated transfer functions, and the above equation holds true only in a very general way.

In addition to the proper gain response, another amplifier characteristic is of great importance. Since a symmetrical square wave consists of a fundamental frequency and odd harmonics thereof, the preservation of the phase-relationship between all frequency components, while passing through the amplifier, must be guaranteed. This requirement is tantamount to specifying a "linear-phase" response or, in other terms, a uniform delay. Amplifiers having constant group delay exhibit smooth, monotonically decreasing frequency-response curves. One must be wary of responses which show ripple or peaking at high frequencies. Although sometimes impressive in terms of bandwidth, such amplifiers often have poor transient response. Shown in Figure 6 is the sine-wave frequency response of the CR2424 in its test fixture with the input variables previously adjusted for best rise and fall times. The output voltage is 20V peak-to-peak. The sine-wave signal generator has a 50 ohm internal impedance. The −3dB point occurs at about 200MHz. For 40V output swings the −3dB bandwidth is typically 145MHz. Actual photographs of CR2424 output waveforms driving a 8.5 pf load are shown in Figure 9.

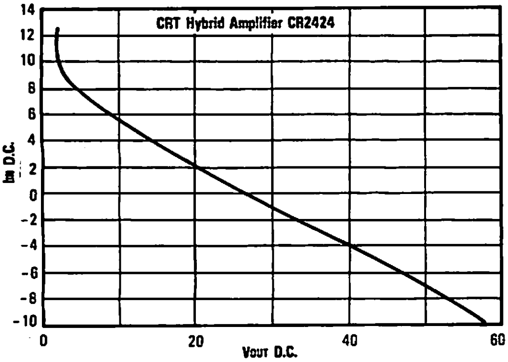


Figure 3. Output Voltage versus Input Current

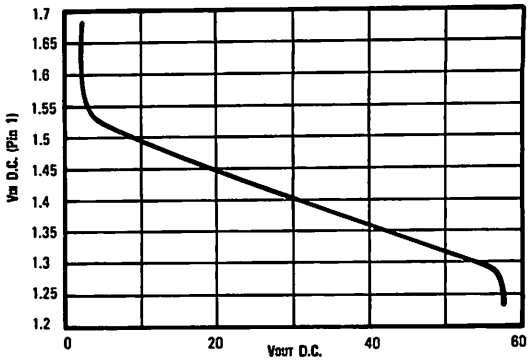


Figure 5. Voltage Ratio at Port 1

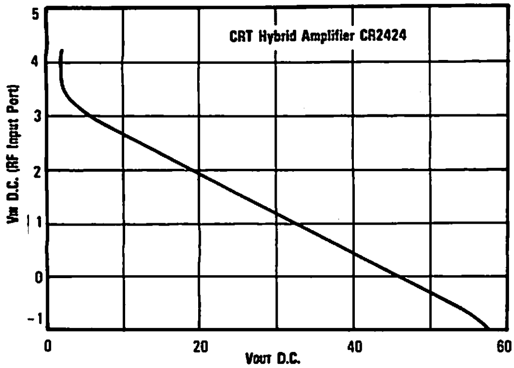


Figure 4. Voltage Ratio at RF Input Port

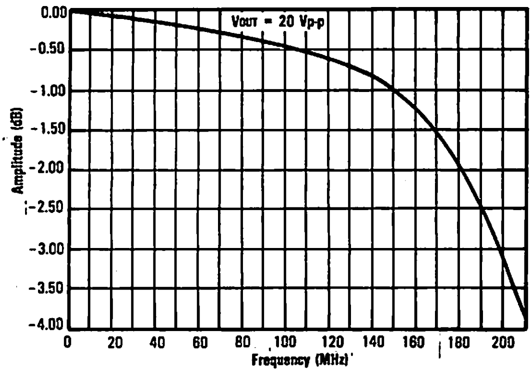


Figure 6. Frequency Response of CR2424

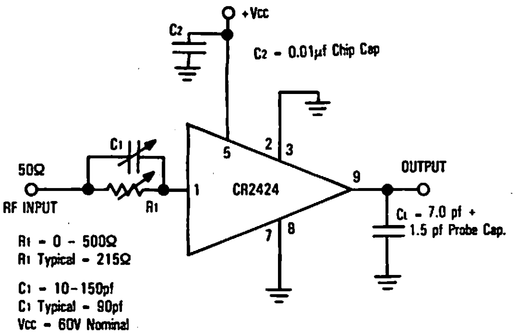


Figure 7. Test Circuit

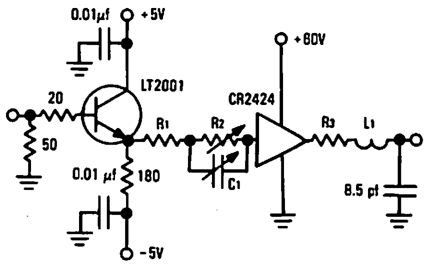


Figure 8. Experimental Circuit

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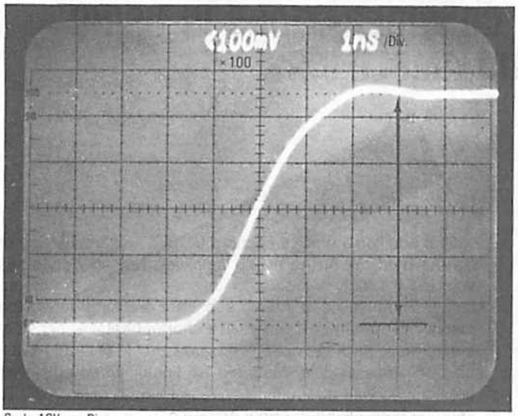
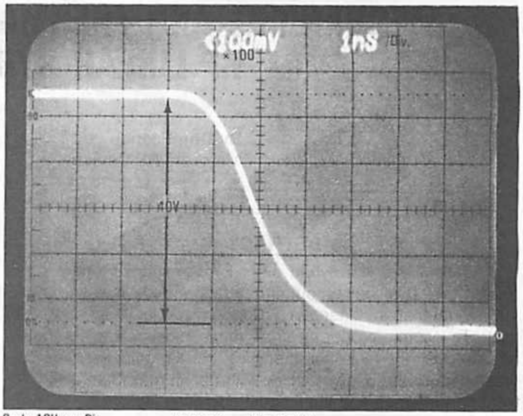


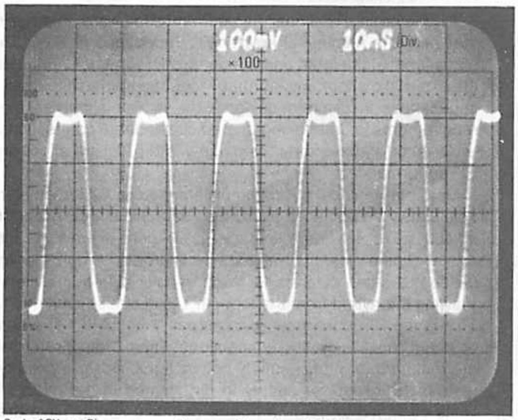
Scale 10V per Div.

Rise Time (10-90%)
t_r = 2.2nsec t_r typical = 2.5nsec



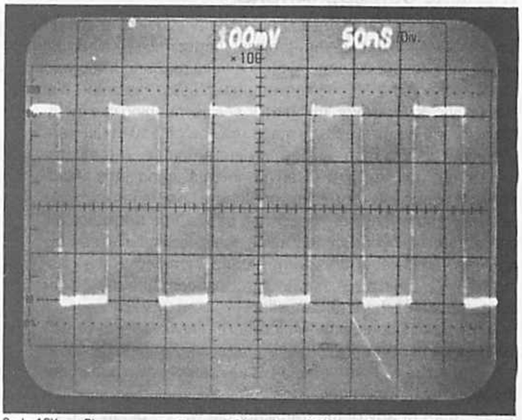
Scale 10V per Div.

Fall Time (10-90%)
t_f = 2.2nsec t_f typical = 2.5nsec



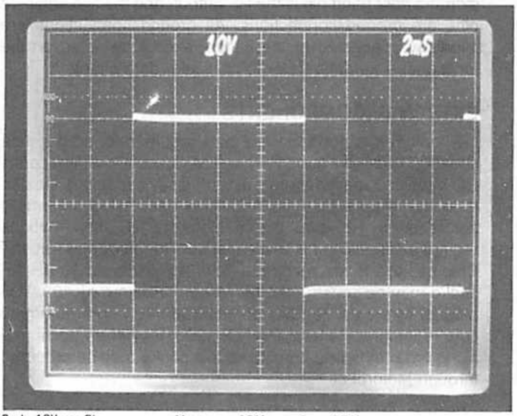
Scale 10V per Div.

Output Signal at 40V p-p
f = 50MHz (10nsec Pixels)



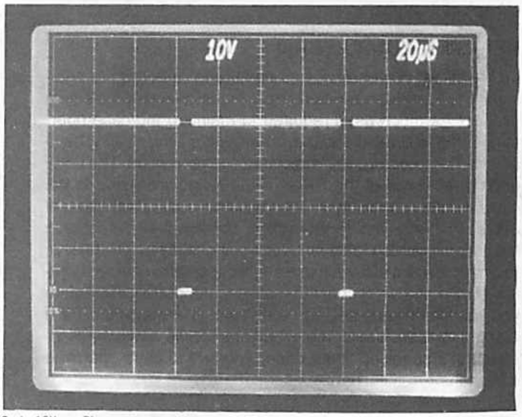
Scale 10V per Div.

Output Signal at 40V p-p f = 10MHz



Scale 10V per Div.

V_{OUT} = 40V p-p f = 67Hz



Scale 10V per Div.

V_{OUT} = 40r p-p

Figure 9. CR2424/2425 Output Waveforms Across 8.5 pF Load

MECHANICAL AND THERMAL CONSIDERATIONS IN USING RF LINEAR HYBRID AMPLIFIERS

By Don Feeney
Motorola RF Devices

ABSTRACT

Motorola's thin film hybrid amplifiers are medium power (0.2 W to 2.0 W power output) broadband devices (1 to 1000 MHz) that are biased in a class A mode for linear operation. To insure a proper electrical/mechanical interface with adequate RF/thermal characteristics, certain guidelines are presented for the design engineer to obtain maximum electrical performance and the longest operating life.

THERMAL CONSIDERATIONS

A question that often arises from engineers using our hybrid amplifiers is "What is the thermal impedance?" Thermal impedance (expressed as θ_{JC}) is a very real and important parameter for the RF design engineer using discrete solid state devices. However, this term loses its meaning in a multistage hybrid amplifier. Each stage may be biased at different quiescent conditions resulting in different junction temperatures under a given set of environmental conditions. Additionally, hybrid circuit design engineers may speak of θ_{JC} referring to the thermal impedance of a single transistor die mounted on a hybrid circuit using their particular assembly processes. However, this term has no meaning to the customer using their product who can only compute the power consumption of the total amplifier.

To avoid this confusion, Motorola RF Devices simply rates the maximum operating case temperature for their RF linear hybrid amplifiers. These amplifiers are designed so that under the worst case operating conditions, the maximum junction temperature of any of the transistor die will be below 150°C. This junction temperature correlates with our two years of accumulated reliability data which predicts an MTBF in excess of 142 years.

HEATSINK YOUR HYBRID

Like all RF power devices, hybrid amplifiers require heatsinking for proper operation. How much heatsinking is necessary? As much as is required to maintain the case operating temperature at the maximum value under worst case ambient temperature and maximum supply voltage. The presence or absence of the RF signal is insignificant due to the class A bias conditions. Reducing the supply voltage will decrease the power consumption, but it will also decrease the linearity. Attach the hybrid amplifier directly to the chassis, to a module card sidewall, to a small baseplate, or to a mounting bracket that is connected to one of the above. But before you complete your design, verify that the maximum case (flange) temperature for the hybrid amplifier is within the manufacturer's specified limits under your worst case operating conditions.

One additional note of caution. DO NOT attempt to lap or file the heatsink of the hybrid amplifier. Not only does this void the warranty (considered "mishandling" by the manufacturer), but you can induce substrate cracking during the machining operation. If you need a shorter heatsink, consider the hermetic package option or the low profile package available on some models. Motorola RF linear hybrid amplifiers are shipped with a mounting surface flatness of ±.002". To improve heatsinking, thermal grease can be used.

PRINTED CIRCUIT BOARD INTERFACE

All Motorola RF linear hybrid amplifiers are internally matched to a nominal characteristic impedance of 50 or 75 ohms, both at the input and the output. This not only reduces the external components normally required to match to these impedances in discrete designs, but it also simplifies the requirements for interfacing printed circuit board connections — for short path lengths, strip line width has little effect on RF performance.

Motorola RF linear hybrid amplifiers feature .020" diameter gold plated pins[1] spaced at .100" centers. Nominal pin length is .460" (.375" for hermetic package).[2] There is provision for a total of nine pins, but unused pins will be missing (refer to pin configuration diagram for the particular hybrid amplifier). Viewing the hybrid from the top, pin 1 is identified on the left. This is the RF input, usually transformer coupled.[3] The two adjacent pins are ground connections. The middle three pins are reserved for power supply connections. Positive polarity units have the power supply in pin located in the middle.[4] Units designed to operate from a negative supply have the power supply connection offset one pin to the left to guard against inadvertent installation in an improper test fixture. The extreme right hand pin is the RF output, and the two adjacent pins are ground connections. All ground connections are internally connected to the flange, except as noted on the functional schematic (refer to particular data sheets).

EXTERNAL COMPONENTS

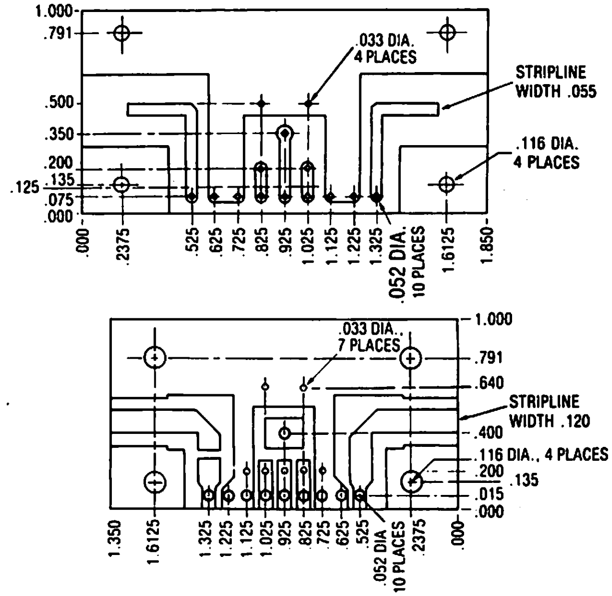
Although it is not specified as a requirement on the data sheets, it is usually good RF practice to add a low impedance RF bypass capacitor (e.g., 0.1 μF chip capacitor) located near the power supply pin. Additional decoupling is normally not required. However, some Motorola RF linear hybrids require external chokes and capacitors for proper operation.[5] Chip capacitors are recommended. A broadband 30 μH RF choke may be constructed by winding 30 turns of #36AWG magnet wire on a Ferroxcube 891 T050/4C4 core (alternate core is Indiana General P/N CF 12001). With an accompanying order of hybrid amplifiers, this choke may be procured through Motorola.

For Motorola hybrid amplifier model CA2820, the external chokes isolate the transistor from the power supply. Positioning of these chokes will have an effect on the high frequency end of the amplitude response.

TEST FIXTURES

Figures 1 through 10 detail the assembly of standard test fixtures for Motorola's line of RF linear hybrid amplifiers. Much of this mechanical information will prove useful to the engineer who is designing one of these units into his equipment. The details of the test fixture assembly for the CA2820 presented in Figure 7 apply to most of the standard RF linear hybrid amplifiers (just substitute PC boards, adjust pin spacing, and remove external components as required). Special provisions for adapting this same test fixture for the low profile package, the bent pin option, and the hermetic package option are presented in Figures 8, 9, and 10.

[1] Pin diameter for hermetic package is .018".
[2] These pins will mate with sockets manufactured by Amphenol (P/N 502-20071-572) and Barnes (P/N 027-018-02).
[3] Except for CA2820, which has an internal DC blocking capacitor at the input.
[4] Except for CA2820 and CA2870. Refer to individual data sheets.
[5] e.g. CA2820, CA2870



NOTES:
1. All dimensions in inches, tolerance ±.005.
2. Material is double sided glass epoxy (G10), 1/16" thickness, 1 oz. cooper, solder plated.
3. TF-06 used for CA2820 only. All other models use TF-03.

Figure 1. PC Board Construction for Hybrid Amplifier Test Fixtures

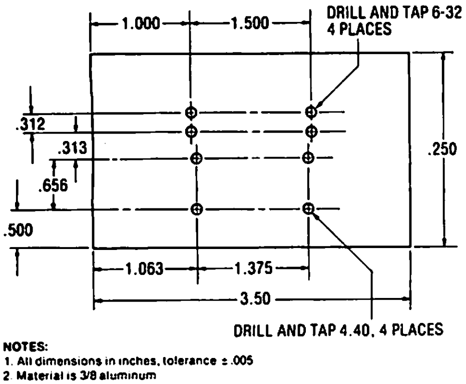


Figure 2. Heatsink Base Plate Construction for Hybrid Amplifier Test Fixture

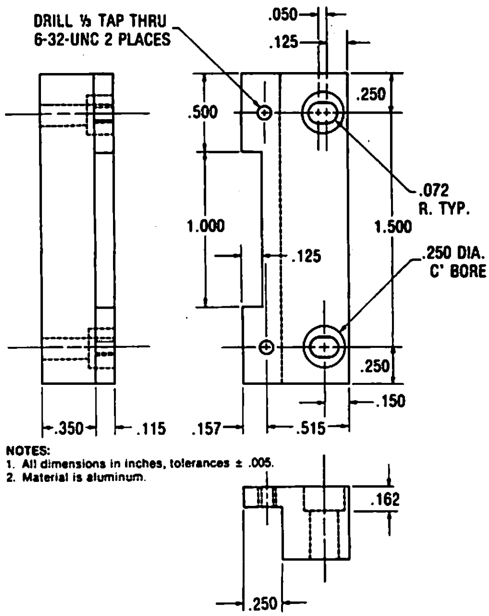


Figure 3. Adapter for Hermetic Package to Standard Hybrid Amplifier Test Fixtures

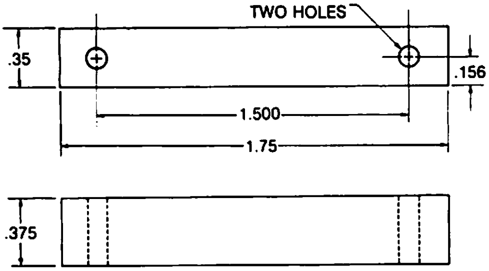
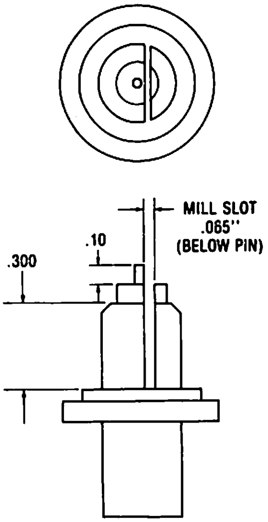


Figure 4. Adapter for Low Profile Package to Standard Hybrid Amplifier Test Fixtures



AMPHENOL P/N US-625/U (50Ω)
TROPOMETER P/N UBJ-20 (75Ω)

Figure 6. Modifications to BNC Connector

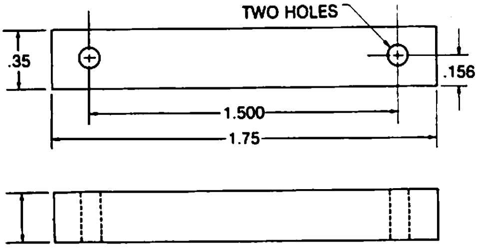


Figure 5. Spacer for Bent Pin Package Option to Standard Hybrid Amplifier Test Fixtures

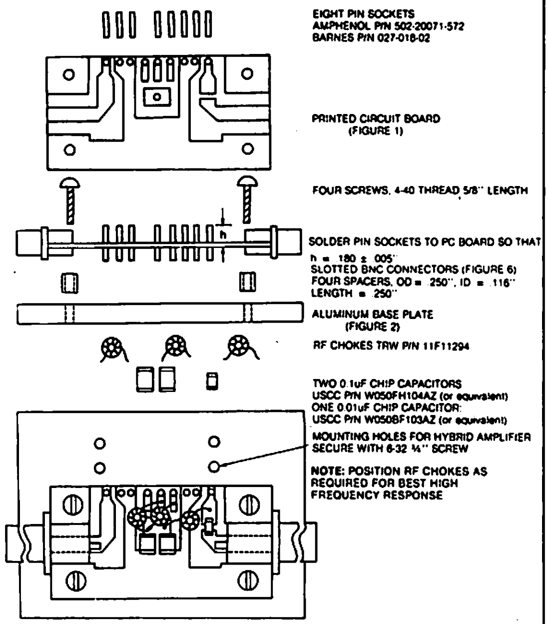


Figure 7. CA2820 Test Fixture Assembly (Case 714F-01)

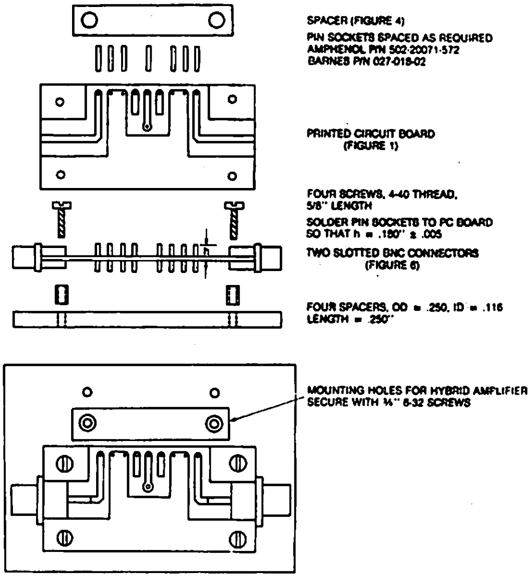


Figure 8. Text Fixture Assembly for Hybrid Amplifiers in Low Profile Package (Case 714G-01)

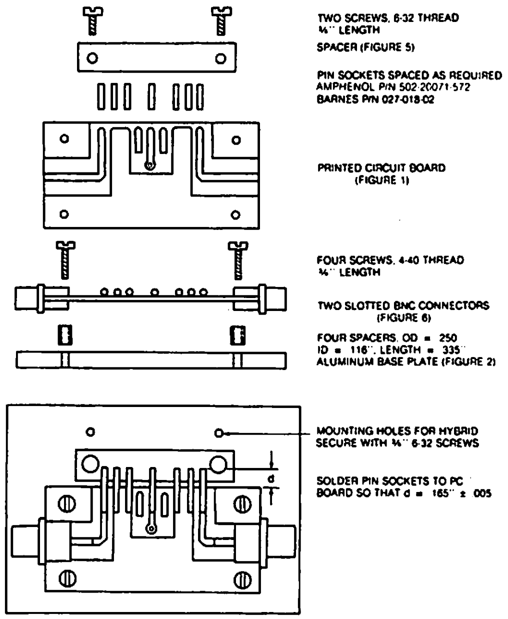


Figure 9. Text Fixture Assembly for Hybrid Amplifiers with Bent Pin Option (Case 714J-01)

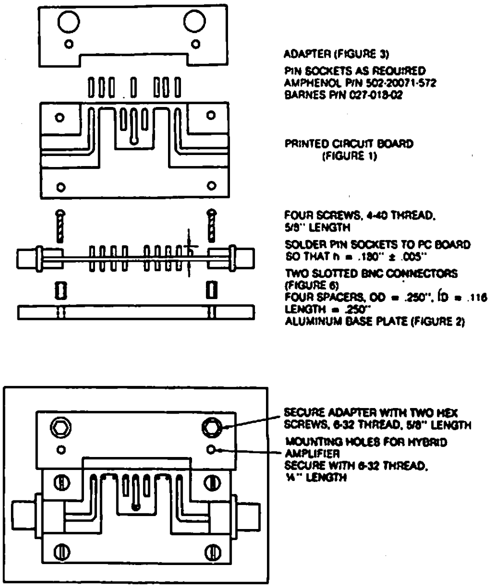


Figure 10. Test Fixture Assembly for Hybrid Amplifiers in Hermetic Package (Case 826-01)

7

MOUNTING TECHNIQUES FOR RF HERMETIC PACKAGES

ABSTRACT

Motorola RF Linear Hybrid Amplifiers are available in three package types; the plastic "CA" package, the low profile "CA" package, and the hermetic SINGLE-IN-LINE-PACKAGE (S.I.P.). The two "CA" type packages are discussed at length in applications note AN1022, "MECHANICAL AND THERMAL CONSIDERATIONS IN USING MOTOROLA RF LINEAR HYBRID AMPLIFIERS." The hermetically sealed package will be dealt with in this note. Guidelines for obtaining suitable interface between these packages and the printed circuit board are presented as well as Hi-Rel screening capabilities for military applications. Proper attention to mechanical details will insure long operating lifetime with optimum electrical performance.

THERMAL CONSIDERATIONS

A question that often arises from engineers using our hybrid amplifiers is "What is the thermal impedance?" Thermal impedance (expressed as θ_{JC}) is a very real and important parameter for the RF design engineering using discrete solid state devices. However, this term loses its meaning in a multi-stage hybrid amplifier. Each stage may be biased at different quiescent conditions resulting in different junction temperatures under a given set of environmental conditions. Additionally, hybrid circuit design engineers may speak of θ_{JC} referring to the thermal impedance of a single transistor die mounted on a hybrid circuit using their particular assembly processes. However, this term has no meaning to the customer using their product who can only compute the power consumption of the total amplifier.

To avoid this confusion, Motorola RF Devices simply rates the maximum operating case temperature for their RF linear hybrid amplifiers. This information is given in Table 1 under Case Burn-In temperature. These amplifiers are designed so that under the worst case operating conditions, the maximum junction temperature of any of the transistor die will be below 150°C. This junction temperature correlates with our two years of accumulated reliability data which predicts an MTBF in excess of 142 years.

HEATSINKING

The RF S.I.P. outline is shown in Figure 1. This package is used for medium power amplifiers with up to 15 watt of D.C. power dissipation. The RF SIP package is mounted on the groundplane side of the printed circuit board, with the pins soldered on the circuit side of the board. This mounting technique is compatible with the technique used on lower power TO-8 packages. Due to the large amount of power dissipated in the package, the P.C. board groundplane may not provide adequate heatsinking. Additional heatsinking will generally be required to insure that the case temperature is kept below the maximum rating.

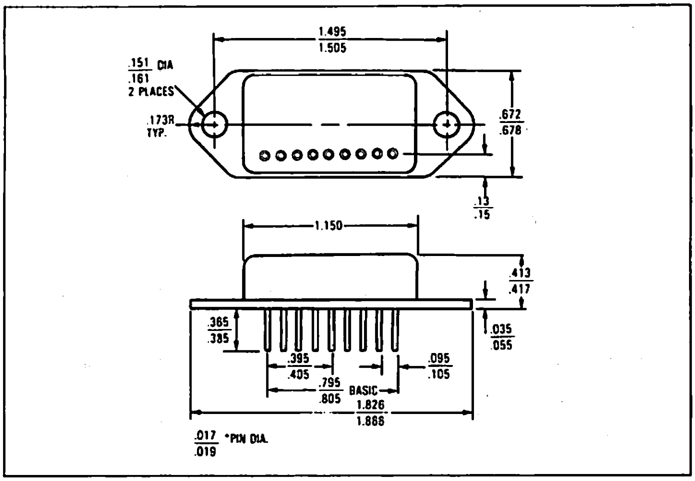


Figure 1. RF SIP Option (Case 826-01)

This additional heatsinking can be easily provided by a commercial heatsink sandwiched between the amplifier case and the P.C. board as shown in Figure 2. How do we determine which heatsink will work best for a given application? In order to answer this question, two important heatsink characteristics must be examined. The first characteristic is the thickness of the heatsink plate. Short lead lengths are a must for optimum RF performance. Since the amplifier leads must pass through both the heatsink plate and the P.C. board before making electrical contact, the minimum lead length is determined by the total thickness of the board and plate. As a rule of thumb, this combined thickness should be less than 0.190" for operation to 500 MHz and less than 0.165" for operation to 1000 MHz. The second important heatsink characteristic is the thermal efficiency. The heatsink must provide a low thermal impedance path from the amplifier case to ambient. Heatsink manufacturers refer to this impedance as θ_{CA} and they specify it in °C per watt. Low values of θ_{CA} correspond to high heatsinking efficiency. We will now examine several heatsinks which have both thin mounting surfaces and high efficiency.

For applications where air flow around the heatsink is available, low cost finned heatsinks can be used. The heatsinks shown in Figures 3 and 4 are of this variety. The heatsink shown in Figure 3 (AAVID[1] #6070) has a mounting surface thickness of 0.091" and a θ_{CA} of 7.2°C per watt for a 4" section. If this heatsink were

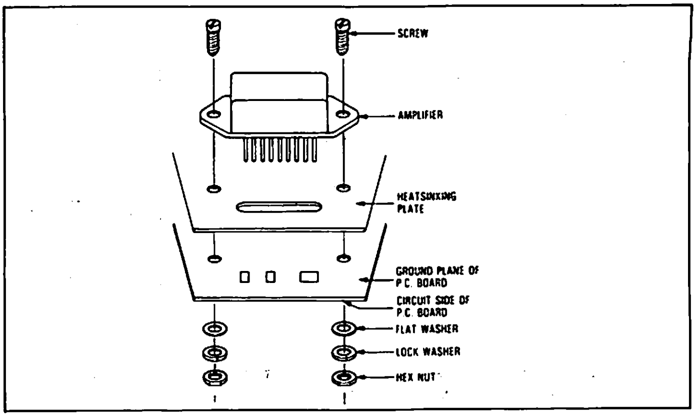


Figure 2.

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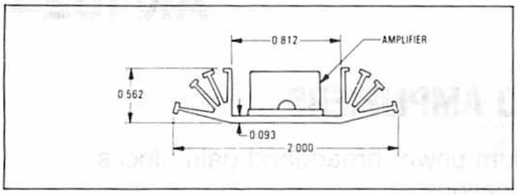


Figure 3.

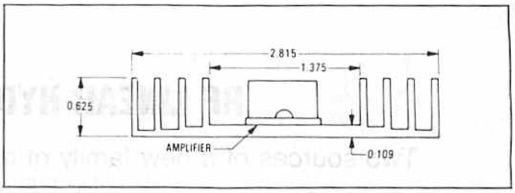


Figure 4.

used with a common glass-epoxy P.C. board, 0.062″ thick, the total thickness of the board and heatsink would be 0.152″. This combination would allow amplifier operation to 1 GHz. Also, for each watt of D.C. power dissipated in the hybrid, the case temperature will rise 7.2°C above ambient. The heatsink shown in Figure 4 (AAVID[1] #60235) has a flange thickness of 0.109″ and a θ_{CA} of 6.0°C per watt for a 4″ section. For applications where air flow is not available, the configuration shown in Figure 5 can be used. Here, a custom heatsink was built out of aluminum and bolted to a chassis (infinite heatsink). The mounting surface thickness for this heatsink is 0.062″ and the θ_{CA} was measured at 1.8°C per watt.

In order to demonstrate this mounting technique, an amplifier was built using the heatsink shown in Figure 3, and 0.062″ G-10 circuit board. The amplifier (see photo) consists of a TO-8 hybrid driving an RF SIP hybrid. The overall gain is 29 dB from 10 MHz to 700 MHz, with a third order intercept point of 41 dBm. Total D.C. power dissipation on the board is 6.8 watts resulting in a temperature rise of 50°C from case to ambient. Since both hybrids are rated at 100°C maximum case operating temperature, the maximum ambient temperature will be limited to 50°C.

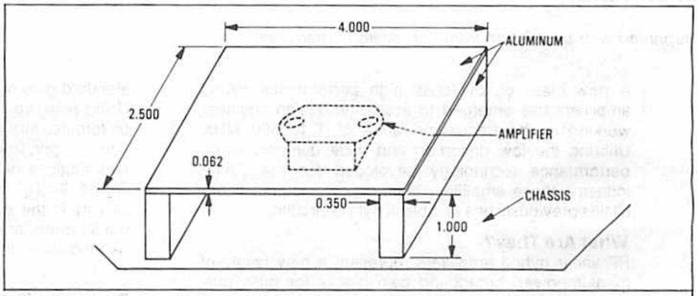
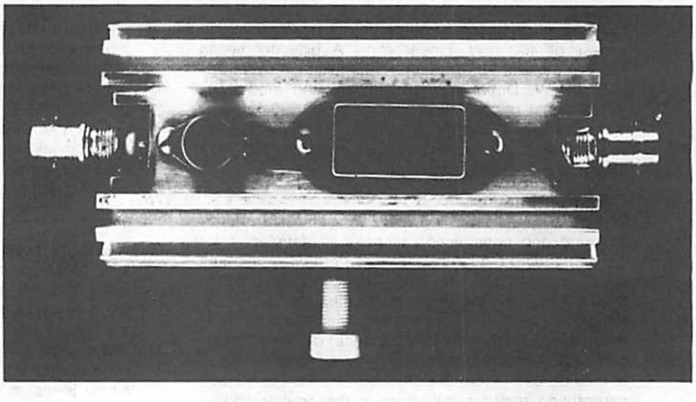


Figure 5.



HI-REL SCREENING

Motorola RF Linear Hybrids in the RF S.I.P. package are available with Hi-Rel screening to Military Standard 883C Method 5008 with the following exceptions:

- Substitute Motorola internal visual specificaiton for Method 2017.
- Substitute case burn-in temperature listed in Table 1 for temperature in Method 1015.
- Substitute constant acceleration level in Table 1 for level in Method 2001.

Consult the factory for specific requirements.

Table 1.

PART #	CASE BURN-IN TEMP. (°C) @ Vcc	CONSTANT ACCELERATION LEVEL (METHOD 2001)
CA2800H	100°C @ 24V	CONDITION A
CA2810H	100°C @ 24V	2.5Kg
CA2812H	100°C @ 24V	CONDITION B
CA2813H	100°C @ 24V	2.5Kg
CA2818H	100°C @ 24V	CONDITION A
CA2820H	80°C @ 24V	CONDITION B
CA2830H	100°C 24V	2.5Kg
CA2832H	60°C @ 28V	2.5Kg
CA2840H	90°C @ 24V	CONDITION A
CA2842H	90°C @ 24V	CONDITION A
CA2850RH	100°C @ 19V	CONDITION A
CA2870H	100°C @ 24V	2.5Kg
CA2875RH	100°C @ −19V	CONDITION A
CA2876RH	100°C @ −19V	CONDITION A
CA4800H	100°C @ 24V	CONDITION A
CA4812H	100°C @ 12V	CONDITION A
CA4815H	100°C @ 15V	CONDITION A
CA5800H	100°C @ 28V	CONDITION A
CA5815H	100°C @ 15V	CONDITION A

7

RF LINEAR HYBRID AMPLIFIERS

Two sources of a new family of medium power broadband gain blocks for RF applications.

By Don Feeney

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A new class of low cost, high performance hybrid amplifiers has emerged to assist the design engineer working in the frequency range of 1 to 500 MHz. Utilizing the low distortion and wide dynamic range performance technology developed for the CATV industry, these amplifiers feature power output capabilities previously unavailable in hybrid circuits.

What Are They?

RF linear hybrid amplifiers represent a new family of mediumpower, broadband gain blocks for multi purpose RF applications. Internally matched at both the input and the output for either 50 ohm or 75 ohm systems, these devices cover gains ranging from 17 to 35 dB, and can accommodate output power levels in excess of 400 mW. Linear class A bias conditions accommodate third order intercept values in excess of +45 dBmV. Depending on quantity and model selected, most prices fall in the range of \$30. to \$60. If you've been using transistors like the 2N3866, 2N5109, or stud mounted devices, read on. You may save a lot more than just design time.

Construction

RF linear hybrid amplifiers utilize the thin film manufacturing and construction techniques developed for the demanding CATV industry. All ceramic substrates are alumina (A1203) with gold conducting paths. Resistors are either cermet or nichrome, and are laser trimmed to better than one percent tolerance. For maximum MTBF, gold metallized transistor die are used incorporating resistive ballasting in the emitter fingers to provide even thermal distribution across the surface corporating resistive ballasting in the emitter fingers to provide even thermal distribution across the surface of the die and to eliminate "hot spotting." These transistor die are subjected to rigorous testing through an extensive wafer qualification program before being mounted on the circuit. The hybrid manufacturer must insure that the transistors used will meet the exacting requirements for gain, distortion, and noise figure.

Basic Circuit

To meet the stringent performance requirements of low distortion and low noise figure, the basic parallel cascade circuit shown in Figure 1 has emerged as the standard gain block used in CATV repeater amplifiers. Using resistive feedback techniques to assure product uniformity, this basic circuit accomplishes gain functions ranging from 17 to 25 dB. For higher gain models, two sections of this circuit are cascaded as shown in Figure 2. To accommodate the increased package density in the same form factor, the transmission line transformers are mounted on a bridge assembly suspended above the substrate.

Packaging Technique

The form factor standardized by the CATV industry allows the hybrid amplifier to be bolted directly to the chassis frame for maximum power dissipation. The pins are located on 0.100" centers for easy connection to a printed circuit board. Mating sockets are manufactured Amphenol (P/N 502-20071-572) and Barnes (P/N 027-018-02).

One note of caution. DO NOT attempt to lap or file the heatsink of the hybrid amplifier. Not only does this void the warranty (considered "mishandling" by the manufacturer), but you can induce substrate cracking during the machining operation.

Heatsink Your Hybrid

Like all RF power devices, hybrid amplifiers require heatsinking for proper operation. How much heatsinking is necessary? As much as is required to maintain the case operating temperature at the maximum value under worst case ambient temperature and maximum supply voltage. The presence or absence of the RF signal is insignificant due to the class A bias conditions. Reducing the supply voltage will decrease the power consumption, but it will also decrease the linearity. Attach the hybrid amplifier directly to the chassis, to a module card sidewall, to a small baseplate, or to a mounting bracket that is connected to one of the above. But before you complete your design, verify that the maximum case (flange) temperature for the hybrid amplifier is within the manufacturer's specified limits under your worst case operating conditions. This will insure that the maximum junction temperatures of the individual transistor die will not be exceeded (usually 140 C).

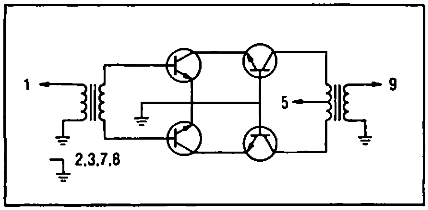

Figure 1. Single Parallel/Cascade Circuit

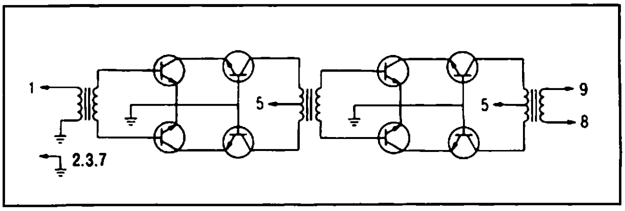

Figure 2. Double Parallel/Cascade Circuit

Electrical Performance Features

Gain — RF linear hybrid amplifiers are fixed gain devices (17 to 35 dB) which are fully cascadable for additional gain. If adjustable gain (AGC) is required for a particular application, it must be added externally (as with a conventional pin diode attenuator).

Frequency Range — These hybrid amplifiers utilize broadband transmission line transformers and 5 GHz fT transistor die to achieve wide bandwidths and linear phase response. Although some models may be optimized over a particular frequency range to fit a certain market, these hybrid amplifiers will often deliver satisfactory performance beyond the frequency ranges specified by the manufacturer.

Impedance — All hybrids are internally matched at both the input and the output for either 50 or 75 ohms. This not only reduces the external components normally required to match to these impedances in discrete designs, but it also simplifies the requirements for interfacing printed circuit board connections. For short path lengths, strip line width has little effect on RF performance.

Output Power — RF linear hybrids are often operated at power levels well below their maximum output capability (for example, in receiver applications). In such cases, operation at a reduced power supply voltage is recommended to reduce power consumption (assuming the full dynamic range is not required).

The maximum power capability for linear class A operation of these circuits may be restricted by several factors:

a) The operating supply voltage, which limits the maximum AC peak to peak swing.
b) The quiescent bias conditions, which limit the maximum current swing across the transformed load impedance.
c) Core saturation in the output transformer, a condition aggravated by high permeability ferrites operating at high ambient temperatures.

Changes in Performance with Supply Voltage — Simply as a point of reference, most RF linear hybrid amplifiers are characterized at a supply voltage of 24V. However, a design engineer may operate above (to increase available output power) or below (to reduce DC power consumption) the rated supply voltage and observe little or no change in gain or frequency response. However, certain specifications are directly affected by the supply voltage:

a) Current consumption. These hybrid amplifiers are biased (quiescent operating point) in a linear mode for class A operation. The higher the supply voltage, the more current they draw. The lower the supply voltage, the lower the current consumption. There is a 1:1 linear relationship between supply voltage and current consumption. Therefore, power consumption varies as the squre of the supply voltage.
b) Output power capability. As the supply voltage increases, so does the maximum available output power (higher peak to peak AC swing is possible across a given load).
c) Linearity. Third order intercept, a measure of linearity, is directly related to supply voltage. In many applications, however, these RF hybrid amplifiers offer more linearity than required. In these cases operation at a lower supply voltage is recommended to reduce power consumption.
d) Noise Figure. Just like a low noise transistor, the lower the bias current (or supply voltage, for these hybrid amplifiers), the lower the noise figure.

Reliability Screening, Military Applications

Since reliability is a mafor factor in the profitability of CATV systems, the component manufacturers who are supplying hybrid cirucits in volume to this competitive industry have developed extensive data bases to insure the reliability of their product. Additional reliability screens uncommon to commercial products are often added at the manufacturer's expense to insure against field failures. Reliability is a major consideration, but these hybrid devices were not designed to qualify to MIL-STD-883, level B.

For example, the caps are sealed with epoxy (non hermetic). The physical mass of the ferrite transmission line transformers prohibits excessive levels of mechanical shock and variable frequency vibration. However the manufacturers should be consulted for specific applications, because hybrid amplifiers of this generic type have qualified for certain military programs.

Why Use a Hybrid Circuit?

Many engineers can design a circuit with discrete components to do exactly what they want. Selecting a hybrid amplifier from a standard product line results in some compromise, but usually offers several advantages:

Who Uses Them?

Because of their wide bandwidth and linear operation, RF linear hybrids are effective for digital (or pulse) applications as well as for analog waveforms. Their unique combination of hgh performance over a broad frequency range and low cost make them the ideal choice for a broad spectrum of major markets:

Markets	Applications	Key Features
Communications Networks	Antenna Distribution	Linear Phase Response
Long Haul or Data Bus	Cable Drivers (50Ω or 75Ω)	Wide Bandwidth, Low Distortion
Coaxial or Fiber Cable	CCD Drivers	High Power Output Capability
Communications Radios	IF Amplifiers	Unconditional Stability and Linear
HF, VHF, UHF	Local Oscillator Buffers	Operation into Highly Reactive Loads
Commercial or Military	Repeater Amplifiers	Infinite VSWR Protection
Satellite Ground Stations	SAW Filter Amplifiers	High Third Order Intercept
High Speed Facsimile	Signal Processing Equipment	Excellent Impedance Match
Telemetry	Swept Measurement Testing	Low Noise Figure, Wide Dynamic
Radar	Transmitter Drivers	Range
ECM		
Instrumentation		

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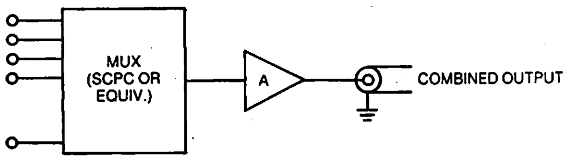
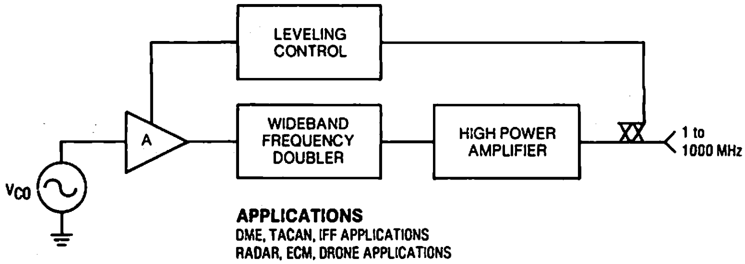
SATELLITE COMMUNICATIONS EQUIPMENT

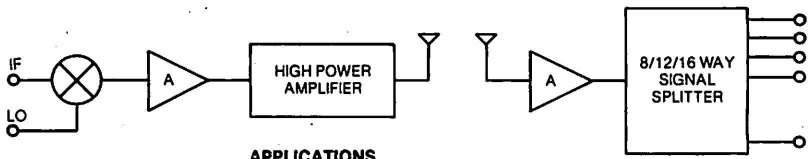


APPLICATIONS
LINEAR POWER AMPLIFIER FOR FM, DIGITAL, DATA, OR VOICE CHANNELS

DRIVER FOR EXTENDED LENGTHS OF COAX



APPLICATIONS
DME, TACAN, IFF APPLICATIONS
RADAR, ECM, DRONE APPLICATIONS
BROADBAND SWEPT INSTRUMENTATION
HF THROUGH UHF TRANSMITTER DRIVERS



TRANSMITTER DRIVER

APPLICATIONS
HF, VHF, UHF FREQUENCY RANGE
AM OR FM TRANSMISSION
COMMERCIAL OR MILITARY EQUIPMENT
N-WAY POWER SPLITTER

ANTENNA DISTRIBUTOR

Performance — The product of years of research, the RF linear hybrid offers the design engineer low distortion levels, wide dynamic range, and noise performance that are difficult to achieve in discrete form. This "extra margin" of performance may enhance the overall equipment design or allow more competitive specifications.

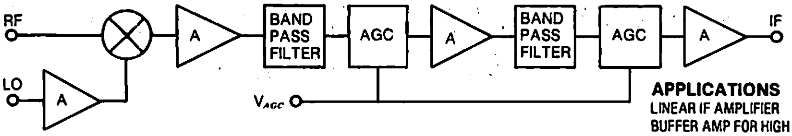
Size — If space is a consideration in the equipment design, the added real estate required for discrete circuitry may be prohibitive.

Reliability — The high degree of reliability demanded by the CATV industry has already been discussed. But given equivalent manufacturing and screening methods, hybrid cirucits offer improved system reliability over a circuit comprised of multiple discrete components. This reliability improvement is a result of reduced package count, fewer solder interconnects (each interconnect is a potential failure point), and system level testing and screening performed by the hybrid manufacturer. Consequently the hybrid manufacturer. Consequently the hybrid manufacturer is accepting a larger responsibility for reliability. The delivered product is a combination of many discrete components tested as a complete system. Losses due to individual component interaction or failure are isolated during the manufacturing cycle.

Cost — The raw cost of materials to build a replacement discrete circuit for a particular application is usually less than the initial price of a hybrid. However, the following factors are often overlooked in many equipment designs:

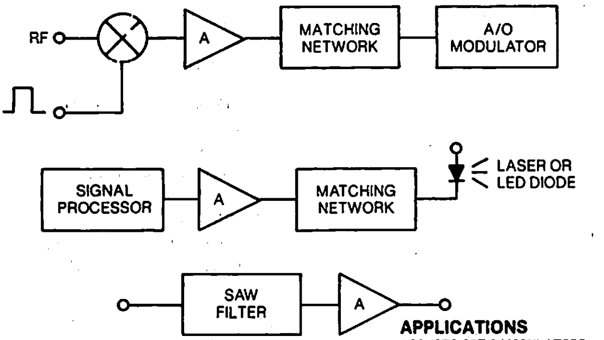
a) The hybrid manufacturer is absorbing the costs of incoming inspection, assembly, and test on the circuit he is providing. Manufacturing costs for equipment using discrete circuitry are always higher than equivalent equipment utilizing commercially available hybrid circuits. This is especially true if any tuning or tweaking of the circuit is required.
b) An equipment manufacturer's cost of procurement and cost of stocking are higher for a multicomponent discrete circuit than for a single thin film hybrid amplifier. These higher costs apply not only during the production build cycle, but throughout the lifetime of the equipment (spare parts inventory).
c) Engineering costs to design reliable replacement circuit. Don't forget to include the time spent in debugging and optimizing the circuit, and the time spent in productions support. The manufacturers of these RF linear hybrid amplifiers have spread their development costs over more than 1,000,000 units operating in the field.

HIGH PERFORMANCE RECEIVER APPLICATIONS



APPLICATIONS
LINEAR IF AMPLIFIER
BUFFER AMP FOR HIGH LEVEL MIXER
REPEATER AMPLIFIER FOR FIBER OR COAXIAL CABLE COMMUNICATIONS
HIGH DENSITY PACKAGING

ELECTRO/OPTICAL EQUIPMENT, SAW APPLICATIONS FIBER OPTIC APPLICTIONS



APPLICATIONS
ACOUSTO-OPTIC MODULATORS
FIBER OPTIC LASER/LED DRIVERS
SAW FILTER AMPLIFIERS
DRIVERS FOR CHARGE COUPLED DEVICES
SUITABLE FOR ANALOG OR DIGITAL MODULATION, ALL TYPES OF WAVEFORMS

Is the RF Linear Hybrid The Right Choice For My Design?

In the end, the choice between a standard hybrid amplifier and a discrete circuit must be made by the design engineer. Find out what's available from the various manufactureres, what their prices are, and what it costs your company to implement a discrete design. One thing you can be sure of: the thin film hybrid amplifiers described in this article have been proven in production and will be around for a long, long time. Probably longer than the discrete transistors they are replacing.

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RELIABILITY CONSIDERATIONS IN DESIGN AND USE OF RF INTEGRATED CIRCUITS

By
James Humphrey and George Luettgenau

ABSTRACT

Reliability is a major factor in the profitability of CATV Systems.

In spite of its proportionally low cost, the RF integrated circuit figures prominently in the overall reliability picture. This complex and important function is located at strategic points in the system.

Fortunately, modern design and manufacturing technology, which draws extensively from resources generated by military and space activities, assures a degree of reliability which is compatible with the most stringent requirements.

Transistor chips are the most vital elements of the RF integrated circuit. Low noise and distortion require state-of-the-art transistor structures. Gold metallization, thermal equilibrium by means of diffused balancing resistors, as well as automated process control have resulted in transistor lifetimes of over 100 years.

One of the inherent reliability advantages of IC's is the reduced number of interconnects. The full benefit of this characteristic is achieved through the use of gold conduction paths in conjunction with gold wire bonding. Perhaps the single most dangerous enemy of high reliability is excessive heat. Careful, computer-aided circuit design coupled with thermally sound, stress-free mechanical construction guarantee structural integrity and safe operating temperatures under all practical conditions. Infrared scanning helps verify the achievement of design goals.

Abuse or abnormal stresses may counteract the best of reliability. In order to avoid problems, the user must control the electrical, thermal, and mechanical environment surrounding the RF IC. Much progress in this respect has been made by the equipment industry.

INTRODUCTION

Reliability considerations are becoming increasingly important in the operation of CATV Systems, requiring an absorption of military and aerospace reliability technology into the CATV business. Market surveys show a large number of MSO's and consultants consider reliability as a major item in equipment selection.

A definition of major reliability terms is important along with an introduction to microcircuit reliability tools (both hardware and software).

An overview discussion of Physics of Construction involved with the die and interconnects must be presented.

DEFINITIONS

R = Reliability

Reliability is related to the probability that an item will perform a defined task satisfactorily for a specified length of time, when used for the purpose intended, and under conditions for which it was designed to operate.

Failure

Failure is a detected cessation of ability to perform a specified function within previously established limits in the area of interest.

(a) Dead on arrival
(b) Infant mortalities
(c) Lifetime failure rates (random)
(d) End of life (wearout)

MTBF (Mean Time Between Failures)

The total measured operating time of a population of equipment, divided by the total number of failures within the population during the measured period of time.

Average Life

The mean value for a normal distribution of lives, and generally, it applies to failures resulting from wearout.

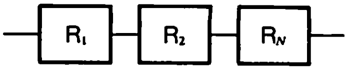
BASIC RELIABILITY EQUATION

$$R = e^{-t/m} = e^{-\lambda t}$$

Where: R = Reliability or probability of success
t = Mission time in hours
m = MTBF in hours $= \dfrac{\text{hours}}{\text{failures}}$
λ = Failure rate $= \dfrac{1}{\text{MTBF}} = \dfrac{\text{failures}}{\text{hours}}$

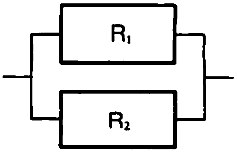
SYSTEM RELIABILITY

1. When components are in series, failure of any one of the components will result in failure of the system.



Then: $R_{SYSTEM} = R_1 \times R_2 \times R_3 \times \text{---} R_N$
$\lambda_{SYSTEM} = \lambda_1 + \lambda_2 + \lambda_3 + \text{---} \lambda_N$

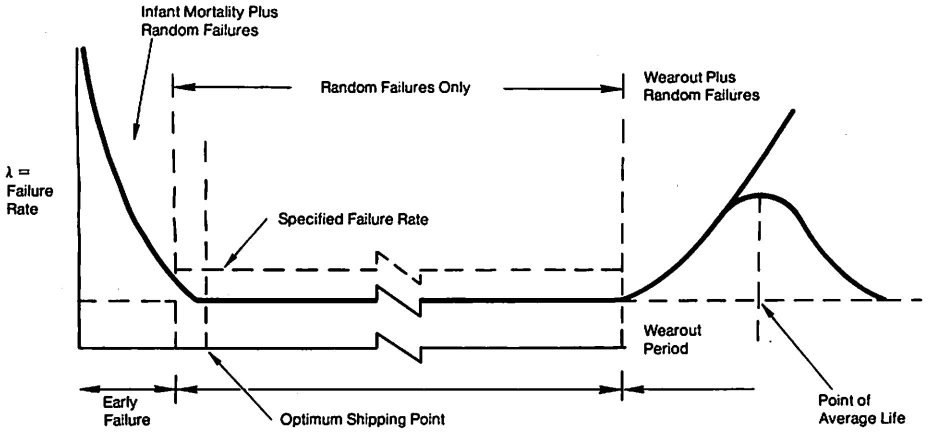
2. When the same components are in parallel (redundancy) neglecting, for simplicity, the decision-making device, the switchover function and the fail safe requirements:



$$R_{SYSTEM} = R_1 + R_2 - (R_1 R_2)$$

RELIABILITY CURVE

The following curve represents the typical condition of operational reliability.



RELIABILITY PREDICTION ALGORITHM

The military has put considerable money and time into the study of reliability. One very useful military document is Military Handbook 217B, *Reliability Prediction of Electronic Equipment*. This handbook shows how to develop failure rate predictions by the use of mathematical models based on years of data collection by military agencies. A discussion of the interaction of components in the model is very useful in gaining an understanding of the overall subject.

PART FAILURE RATE MODEL λ_p

$\lambda_p = \lambda_b (\pi_T \times \pi_E \times \pi_Q \times \pi_F \times \pi_M)$

Where:
- λ_p = Part failures in failures per 10^6 hrs.
- λ_b = Base failure rate
- π_T = Temperature adjustment factor
- π_E = Environmental adjustment factor
- π_Q = Adjustment factor based on quality
- π_F = Adjustment factor for circuit function
  - = 0.8 for digital hybrids
  - = 1.0 for linear hybrids
  - = 1.1 for combination hybrids
- π_M = Adjustment factor for maturity of product

BASE FAILURE RATE MODEL λ_b

$\lambda_b = \lambda_S + A_s\lambda_c + \Sigma\lambda_{RT}N_{RT}$ (Substrate contribution)
$+ \Sigma\lambda_{DC}N_{DC}$ (Attached components contributions)
$+ \lambda_{PF}\pi_{PF}$ (Package contributions)

Where:
- λ_b = Base failure rate in failures/10^6 hr.
- λ_S = Failure rate due to the substrate and film processing
- $A_s\lambda_c$ = Failure rate contributions due to network complexity and substrate area which includes:
  - (a) Number of lead terminations
  - (b) Number of film resistors
  - (c) Number of discrete chip devices
  - (d) Type of film (thin versus thick)
- $\Sigma\lambda_{RT}N_{RT}$ = The sum of the failure rates for each resistor as a function of the required resistance tolerance
- $\Sigma\lambda_{DC}N_{DC}$ = The sum of the attached device failure rates for semiconductors and capacitors
- $\lambda_{PF}\pi_{PF}$ = The hybrid package failure adjusted to include material and style

PHYSICS OF CONSTRUCTION

Following the enumeration and identification of symbols used in reliability algorithms, a discussion of the major microelectronic components with respect to their reliability contributions is in order:

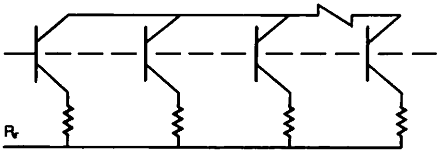
TRANSISTORS

The transistor die is the heart of the hybrid amplifier. With four to eight devices per circuit, the transistor determines performance and is most critical to proper circuit operation.

During the last few years users have witnessed major advances in the performance of linear broadband transistors. Often, efforts to improve one characteristic have adverse effects on other desirable features. For instance, distortion may be bettered by thinning the epitaxial collector region. This, however, leads to sensitivity to voltage transients and other abnormal operating conditions. Therefore, devices with outstanding performance in one area are prone to weakness in others. Computer-aided device design coupled with volume production and tight process controls have resulted in transistors in which all essential features are in proper balance.

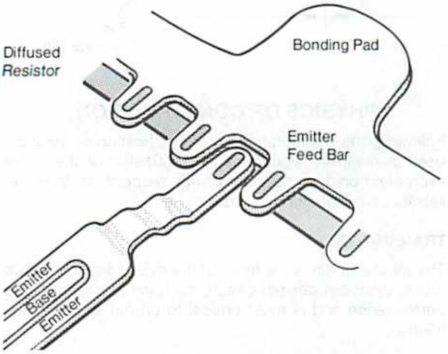
High f_T is generally recognized as an important factor in achieving wide bandwidth and uniform distortion characteristics. Gigahertz transistors, which are now being used, have very delicate patterns, involving micron and submicron tolerances. They also occupy sizable areas on the silicon wafer, since watt-sized powers have to be handled. It is only realistic to expect that all parts of the overall transistor structure are not perfectly alike, but rather resemble the parallel configuration of many, slightly differing, small devices, as shown in the figure.

Ballast Resistors

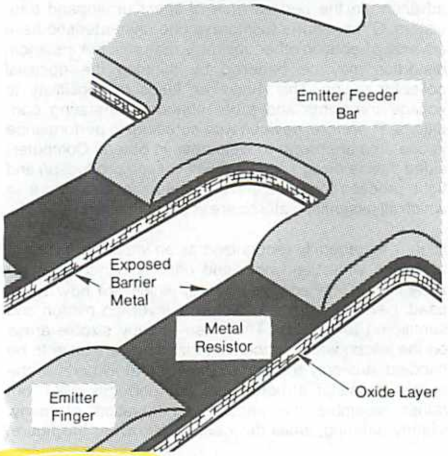


It is also apparent that the entire transistor geometry cannot be tightly thermally coupled within itself, therefore giving rise to the possibility of small sub-areas of the transistor assuming different values of temperature than others. This possible problem can be effectively combatted by adding emitter balancing resistors to the device. Ideally each emitter-site or finger should have its own resistor. This goal is easily realized in interdigitated structures. Film or diffused monolithic resistors may be used. From a process and reliability point of view, diffused resistors are preferred because they avoid the silicon-oxide barrier which has a very high thermal resistance.

Diffused Ballasting System (Only one emitter contact shown)



Metal Film Ballast Resistor



METAL MIGRATION

Some time ago a serious failure mechanism, associated with GHz transistors, was discovered. The metallization stripes of such devices, as mentioned earlier, are only a few microns wide. The metal thickness is, because of fabrication limitations, of similar dimensions. Consequently, the current density in these stripes is quite high, often reading hundreds of thousands of amperes per cm² of cross-section. Under these circumstances, metal migration may occur. With such large numbers of electrons flowing in such crowded space, the probability of collisions with thermally activated metal ions is great. The ions are propelled in the direction of electron current flow causing, in the long run, the metal to move, forming hillocks, whiskers and voids. The lifetime of a transistor is a function of three things: the current density, the temperature, and the type and consistency of metallization.

Not much leeway exists in reducing the current density (unless f_T is sacrificed). Changing from aluminum to gold extends the life at least by an order of magnitude. At high temperatures the difference is even more pronounced. At 150°C, the time to metal failure for gold metallization microwave transistors is in excess of 10^6 hours = 114 years. While this number is quite comforting, one is not at liberty to treat the subject of transistor chip heatsinking too lightly. A proven method for removing heat while at the same time obtaining a solid mechanical mount, has been to employ a heatspreader between the silicon chip and the IC substrate. Automatic mounting stations are used to eutectic collet mount the chip to indexed leadframes. Tight control of pressure and scrub sequence result in defect free attachment. Although one may employ other methods of heatsinking, e.g. beryllium oxide substrates for part of the circuit, the added mechanical complexity and the reduced freedom of optimal circuit layout presently outweight the minor advantages resulting from a reduction in transistor temperature.

INTERCONNECTS

One of the most important parts of hybrid circuits is the interconnect system. The ability to reduce the number, control the quality, and test them by screening complete functions, is one of the major advantages of hybrid circuits over more conventional approaches. Constant improvement in the mechanical and metallurgical systems have drastically improved reliability.

An analysis of the schematic on the standard 33dB Hybrid Amplifier will illustrate the point:

Comparing hybrid versus discrete techniques, one can show the following:

1. For each transistor used, a *minimum of three* interconnects corresponding to the solder joints at the PC board are eliminated.
2. For each capacitor used, a minimum of two interconnects are eliminated.
3. For each film resistor used, a minimum of four interconnects are eliminated corresponding to the connection to the resistor body and the connection to the PC board.
4. Transformer interconnects will be the same for hybrid or discrete.

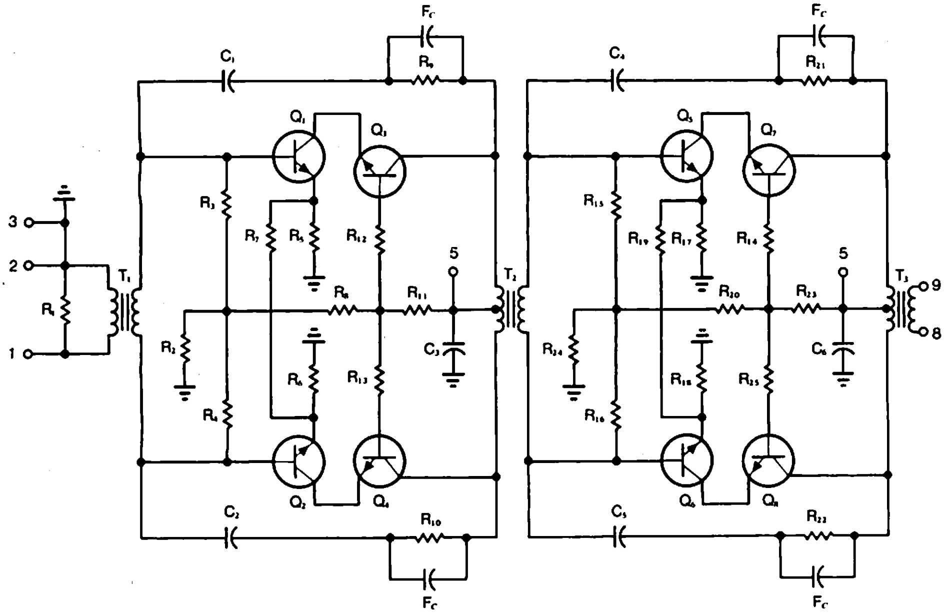
The increase in interconnects in building 33dB of gain in discrete form over the same circuit in hybrid form is:

Add due to transistors	=	24
Add due to chip capacitors	=	12
Add due to resistors	=	100
Add due to transformers	=	0
Less due to hybrid jumpers	=	−4
Less due to active pins	=	−5
		127 Additional interconnects per 33dB function

MIL Handbook 217B also discusses the reduction in reliability of printed circuit boards as a direct multiple of the holes required. Eighty-one additional holes are involved in making one discrete amplifier.

7

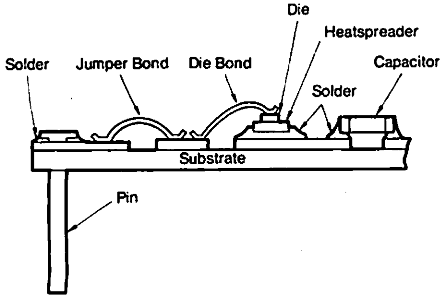
33dB Gain Block



Having the interconnects made early in the manufacturing sequence, before the subsequent series of tests and inspections, has beneficial influence on end equipment reliability.

The complete functional system including interconnects is tested, screened and Q.C. sampled many times before it even meets up with the PC board in the manufacturers subsystem.

Interconnects



COMPONENT MOUNT

The transistor heatspreaders, chip capacitors and pin connections are soldered to the metallization pattern on the substrate surface. This process is completed in a tightly controlled solder reflow furnace.

Due to the fact that the units are processed in an inert atmosphere and thoroughly cleaned and inspected early in the production process, workmanship problems are greatly reduced.

BONDS

Wire bonding was a major reliability issue for years.

Aluminum has been one of the most widely used bonding systems in the hybrid industry for many years. The main reason for this is that ultrasonic aluminum systems bond at room temperature and, hence, do not interfere with other hybrid assembly processes.

Gold thermal compression ball bonding has been a reliable standard process in the semiconductor industry for years. However, the requirement for 300°C bonding temperatures have kept this technique out of most hybrids. The recent changeover to all gold hybrids prompted the development of a compatible low temperature gold wire bonding system which by far out-performs aluminum.

Advantages of Aluminum Bonds

- Low temperature process
- Compatible with Al die metal
- Low cost
- High speed
- Easy to loop (stiff)

Disadvantages of Aluminum Bonds

- Degrades with time/temperature
- Kirkendall voiding
- Intermetallic formation with gold
- Brittle and subject to cracks
- Difficult to screen
- Difficult to control

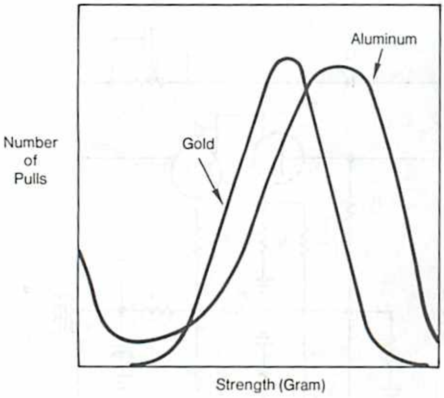
Advantages of Gold Bonding

- Compatible with gold die and substrate
- Strength stable with time/temperature
- Malleable — not subject to cracking
- Easier to control process

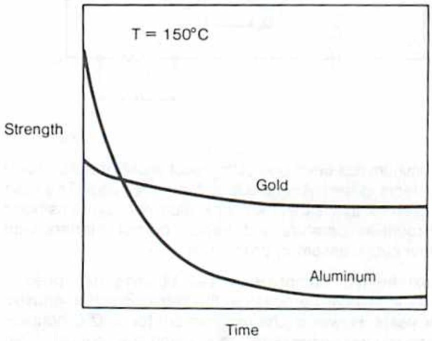
Disadvantages of Gold Bonding

- More expensive
- More deformation at bond foot
- Hard to form loops

Histogram of Gold Versus Aluminum Bond Strengths



Strength Versus Time on Gold Versus Aluminum Wire



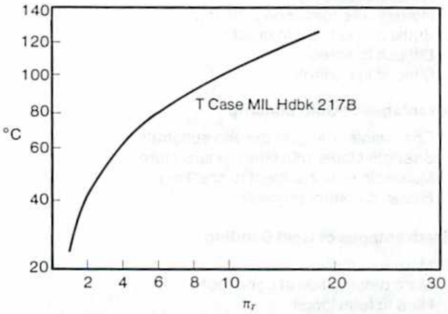
RELIABILITY ADJUSTMENT FACTORS

Following is a discussion of the "π adjustment factors" in MIL Handbook 217B. These relate to the external influences on hybrid circuit reliability.

TEMPERATURE ADJUSTMENT FACTOR π_T

Operating temperature is one of the most important factors in reliability. As can be seen by the curve shown, great reliability improvements can be obtained by lowering the case temperature.

Failure Rate Multiplier Due to Temperature



This curve shows that a hybrid circuit, operating at a case temperature of 100°C, has four times the failure rate as the same circuit run at 50°C.

ENVIRONMENTAL ADJUSTMENT FACTOR π_E

This adjustment factor is based on the service environmental conditions that the part will be exposed to during operation.

π_E, Environmental Factor Based on Environmental Service Conditions

Environment	Symbol	π_E
Ground, Benign	G_B	0.2
Space Flight	S_F	0.2
Ground Fixed	G_F	1.0
Airborne, Inhabited	A_I	4.0
Naval, Sheltered	N_S	4.0
Ground, Mobile	G_M	4.0
Naval, Unsheltered	N_U	5.0
Airborne, Uninhabited	A_U	6.0
Missile, Launch	M_L	10.0

MATURITY ADJUSTMENT FACTOR π_M

The failure rate predicted by this mechanical model can be expected to increase by a factor of (π_M = 10) under any one of the following conditions:

(a) New device in initial production.
(b) Where major changes in design or processes have occurred.
(c) Where there has been an extended interruption in production or a change in line personnel (radical expansion).

The factor of 10 can be expected to apply until conditions and controls have stabilized. This period can extend for as much as 6 months of continuous production.

This maturity factor is extremely important. The industry has used over 400,000 CATV modules since the first module was shipped in 1970. Since that time we have constantly improved and refined the IC. Optimum reliability is an evolutionary process depending on time, volume, defect analysis and feedback to fine tune the product and eliminate defects.

The question is where does CATV fit into this table. Mechanical and thermal casting designs are extremely important in protecting the RF IC from the external environment conditions. Still, wide variations in system placement introduce a swing factor for environmental effects, which will cause π_E for CATV to fall between 1.0 and 5.0.

The user must strive to keep the components as close to laboratory zero as possible.

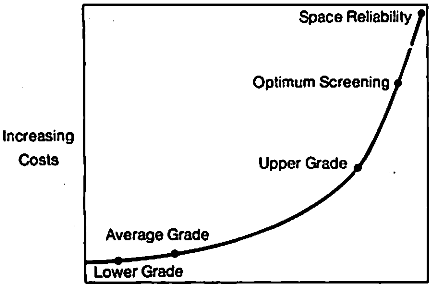
QUALITY ADJUSTMENT FACTOR π_Q

This is the adjustment factor based on the quality grade of the product. This factor modifies the reliability levels by the different quality levels specified in MIL STD 883, *Test Methods and Procedures for Microelectronics.* These levels take into account different screening levels, qualification levels and quality conformance inspection requirements for the specified class.

	π_Q
MIL STD 883 Class A	0.5
MIL STD 883 Class B	1.0
Vendor Equivalent Class B	5.0
MIL STD 883 Class C	30.0
Commercial with Screening	50.0
Commercial (No Screening)	75.0

A study of the MIL STD 883 Quality Requirements allow a very important discussion of cost versus reliability. As could be expected the test, manpower, equipment, time and paperwork go up rapidly as the MIL STD Grade is increased. A relative plot of this relationship is shown below:

Cost Versus Reliability



Many of the MIL Standard Military requirements seem unimportant in influencing CATV reliability. However, the cost versus reliability curve is real and the equipment supplier can make choices as to the type of reliability he is willing to pay for.

EQUIPMENT

It takes a massive capital investment in order to meet the manufacturing requirements for the CATV industry. The volume, quality and performance standards required have caused us to constantly reinvest for the future. Many of the invested dollars are for equipments for which the return on investment is subjective.

SCANNING ELECTRON MICROSCOPE

This instrument allows very high magnification of surface conditions not available with optical methods. Magnifications up to 100,000 times are possible with the SEM.

DISPERSIVE X-RAY ANALYSIS

This capability, which is a feature of the SEM, allows us to make a microprobe to determine the chemical composition of a sample. This is accomplished by detection of secondary emission x-rays which possess characteristic energies. The relative quantity and location of elements may then be displayed on the CRT.

VARIABLE FREQUENCY VIBRATION

This is a destructive test which is performed for the purpose of determining the effect on component parts of vibration in the specified frequency range.

X-RAY

This is a very valuable tool for detecting voids in solder or eutectic bonds.

INFRARED MICROSCOPY

The ability to examine a circuit thermally under operating conditions is absolutely necessary when designing a new product or testing a new process. The infrared microscanner is used for evaluation of new products from the standpoint of thermal resistance and operating temperature. Resolution of 0.0005 inch can be achieved.

CONCLUSIONS

- Many reliability tools are available today both in equipments for evaluation of reliability and in analytical tools such as MIL Handbook 217B for predictions of reliability.
- Hybrid circuits offer massive reliability leverage due to:
  (a) Reduction of Interconnects
  (b) Ability to control quality by screening
  (c) Large volume of complex standard functions are easier to control
- Case temperature is very important for reliability
- A monometallic system, i.e., gold die metallization and gold wire bonding are optimum for reliability.
- Reliability can be improved by adding quality cost to the module process. This increased cost may easily be returned due to the lower failure rate.

ACKNOWLEDGEMENTS

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EXTENDING THE RANGE OF AN INTERMODULATION DISTORTION TEST

More often than not, a system's intermodulation distortion is characterized by its third-order intercept value, the most widely accepted figure of merit for indicating the linearity of a system. Even though IMD is extremely difficult to measure accurately and with repeatability when low signal levels are introduced into the device under test, precise measurements can be made at levels as low as 100 decibels below the desired carrier (input-signal) point. The secret is to add a tunable bandpass filter to the measuring system and to reduce the nonlinearities inherent in the test system, thus making it possible to determine third-order intercept values of up to +50dBm, which is more than 20dB above that of most measuring systems now in use.

Third-order intermodulation products are generated as shown in part (a) of the figure. Consider two signals, f_1 and f_2, that are applied to the input of a device that has a non-linear transfer function. If the output power is equally distributed at both frequencies and the frequencies are close together, equal power-distortion products will occur at $2f_1-f_2$ and $2f_2-f_1$.

The magnitude of these unwanted products, expressed in decibels below the output Po, is defined as the system IMD. The third-order intercept may then be found by its defining equation:

$$I = P(dBm) + IMD(dB)/2 \qquad (1)$$

where IMD is the third-order product produced by the I intercept value, measured in decibels.

An IMD setup having wide dynamic range is shown in (b). In this case, measurements are performed at 30 to 500 MHz, although the guidelines set forth here will allow accurate measurements at any frequency.

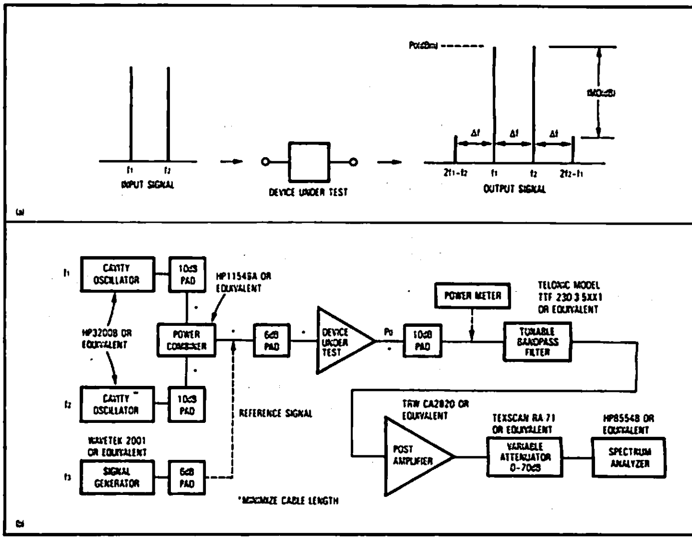
The first step in measuring IMD and thus securing the third-order intercept of a device is frequently the most difficult to attain — that of combining two input tones to the device under test without introducing distortion or spurious responses. For fixed-input-frequency setups, filters can be employed to eliminate harmonics generated by f_1 and f_2. If the input frequencies are variable, cavity oscillators should be used instead of sweep generators, because the latter's harmonic content is too high.

The best method for combining the two signals linearly is to use a resistive power combiner as shown, so that the composite signal generated will be virtually clean (no nonlinearities). To reduce third-harmonic distortion between the f_1 and f_2 generators, 10-dB attenuator pads should be used between the cavity oscillators and the power combiner. Using both the pads and the combiner guarantees a broadband input source with constant characteristic impedance facing the device under test. As the requirement for a broadband resistive source of constant impedance also applies to the load for the test device, it is wise to use a 10-dB attenuator here, as well.

The system's measuring range is improved by placing a five-pole bandpass filter in the postamplifier chain. Having a bandwidth of less than $\Delta\phi$, this filter rejects unwanted signals f_1, f_2, thus eliminating strong but unwanted signal responses that tend to limit the dynamic range of (that is, desensitize) the test system.

For those not familiar with the procedure, IMD and third-order intercept are found as follows:

- Set channel spacing to the desired Δf (6 megahertz for the system shown in the figure).
- Set reference signal f_3 to $2f_1-f_2$.
- Using a power meter, set Po to the desired output power level for each of the three sources independently. Connect only one source at a time.
- With f_3 connected, tune the bandpass filter to f_3. With the variable attenuation at 30 to 50 dB, set a reference level on the spectrum analyzer. Make sure the postamplifier is not in compression by inserting 30 to 50 dB of additional attenuation. One should then observe 30 to 50 dB of signal reduction on the spectrum analyzer.
- Apply f_1 and f_2. Decrease attenuation in the variable attenuator to bring the signal within range of the analyzer. Add the change in attenuation to the value of suppression as read on the analyzer to obtain IMD.
- Adjust f_3 and filter to $2f_2-f_1$ and repeat all steps. IMD should be within 3 dB of the first measurement.
- Calculate the third-order intercept from Eq. 1.



Wide range. Intermodulation distortion is created if two input frequencies pass through a nonlinear device (a). System measures IMD over wider range than standard setups by using cavity oscillators to reduce harmonic generation, tunable bandpass filter for rejection of IM components not measured against f_1, or f_2 ($2f_2-f_1$ or $2f_1-f_2$, respectively), and power-splitter for linear combiner of f_1 and f_2. Pads (6dB and 10dB) offer isolation between system elements. With setup, measurements of IMD can be made at levels 100dB below carrier.

RELIABILITY/PERFORMANCE ASPECTS OF CATV AMPLIFIER DESIGN

By
Michael D. McCombs

ABSTRACT

The reliability advantages to be offered by the RF hybrid amplifier as used in CATV applications are discussed. The active part of the hybrid amplifier is the transistor. Metallization, ballasting and ruggedness are reliability related factors that must be considered by the device engineer when designing a high performance CATV transistor. Vertical and horizontal geometry and device distortion mechanisms are performance related factors that must also be taken into account. The interrelation between these factors is examined. Life test data is then presented to illustrate the advantages to be gained by careful device design.

I. INTRODUCTION

The cable television system operator buys equipment which he knows has demonstrated a certain minimum level of performance, or in other words, equipment that meets his specifications. If he questions this performance he can run various electrical tests to check it.

Another question that we would like to be able to answer is, how long will his equipment operate before it fails, costing him downtime and repair. This is the question of reliability and to understand this it is necessary to understand the factors that go into designing for reliability.

The primary building block of a reliable CATV amplifier is the RF integrated circuit. This concept possesses many advantages over the PC board discrete design including a reduced number of interconnects and the ability of the manufacturer to effectively test the system before delivery to the equipment manufacturer.

Going one step further, the basic constituent of the integrated circuit is the transistor itself. It is in the design of this transistor that the ideals of high performance with reliability can be effectively realized.

The ultimate test is to see how long a part operates in the field without failing. The best way to simulate this is by means of a life test. Life test data is included as a means of demonstrating the results of a careful design.

II. WHAT IS RELIABILITY

One definition could be that reliability is something that can cost you money if you don't have it. The dictionary defines reliability as "the quality describing that which is dependable or honest." To build honest transistors and amplifiers is a noble concept but one which may be difficult to measure. So in the everyday sense, reliability is a somewhat abstract idea that is difficult to describe quantitatively. In engineering, however, reliability has an exact meaning.

> "Reliability is the probability of a device performing its purpose adequately for the period of time intended under the operating conditions encountered."[5]

When an amplifier is designed for a certain level of gain, it may happen in practice that the gain is less than that called out in the specification. In certain cases this may be acceptable if the amplifier turns out to be very reliable. However, another amplifier, which supplies the full gain with ease, may breakdown in operation because its components are being taxed to their limits. This is where reliability enters the picture. It is possible to achieve full performance and still have state-of-the-art reliability.[5]

We said that *reliability* is the capability of equipment not to break down in operation. The measure of an equipment's reliability, then, is the frequency at which failures occur in time. A failure is a malfunction which causes the component to violate the requirement for adequate performance. The frequency of such failures is called the failure rate. The reciprocal of the failure rate is called the mean time between failures or MTBF.

$$\lambda = \text{Failure Rate}$$

$$\frac{1}{\lambda} = \text{MTBF}$$

Referring to Figure 1, it is seen that there are three basic types of failures; early, chance and wearout failures.[2]

Early failures occur early in the life of a component and result usually from poor manufacturing. These can be eliminated by a 'burn-in' process.

Wearout failures are a symptom of component aging. These types of failures can be eliminated by either replacing at regular intervals or by designing for longer life than the intended life of the equipment if the components are inaccessible.

Chance failures occur at random intervals and are due to sudden stress accumulations beyond the design strength of the component. Since the other failure types are relatively easy to eliminate, performance reliability should be determined by the chance failures.

For chance failures only, reliability may be expressed by the exponential relationship

$$R(t) = e^{-\lambda t}$$

where λ is the failure rate and t is a given operating time; t must never exceed the 'useful life' of the device. The derivation of this reliability expression is found in the Appendix.

System failures are caused by component failures. When components can fail only because of chance, the system will fail only because of chance. The design engineer is responsible for the reliability which is characteristic of his equipment. If he desires to reduce the number of chance failures which occur during the useful life period of his equipment, he must keep several key points in mind.[5]

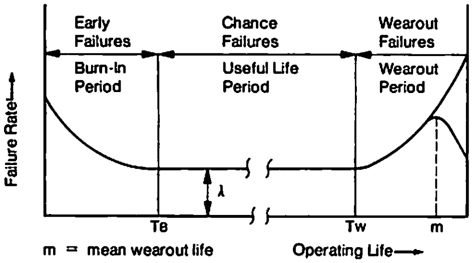


Figure 1. Component Failure Rate as a Function of Age

1. Design components to accept overstress; the normal operating point *should* be well below rated values, including temperature.
2. Provide good packaging with adequate heat sinking.
3. Design with as few components and interconnects as possible.

III. HYBRID CIRCUIT RELIABILITY ADVANTAGES

The hybrid circuit is the heart of the CATV amplifier. This assembly must perform its duty while experiencing a variety of electrical and environmental extremes. If the hybrid circuit should fail, then the cost to the system operator is high. For this reason the hybrid circuit should be an extremely reliable piece of equipment.

There are certain qualities of a hybrid circuit which make it an inherently reliable assembly.

One subtle advantage relates to the wear out life of components. Replacement of a hybrid circuit means replacing every amplifier component which resets the clock on the entire amplifier as far as mean life is concerned. Replacing a component in a discrete amplifier does not. All of the other discrete components continue to approach their wear out life.

The metallization system of the hybrid is another advantage. The gold metallization which is used for interconnects on the hybrid circuit allows the designer to have the high conductivity of gold for use in tying together the various components of the circuit, while having the additional reliability advantage of a mono-metallic gold system in wire bonding from the transistor to the hybrid. Even though the hybrid circuit utilizes heat sinking to reduce heat buildup, any bi-metallic interface will be susceptible to failure due to intermetallic formation. These gold-aluminum intermetallics are more brittle than the parent metals, and they also are susceptible to void formation due to the faster diffusion of aluminum into gold compared with gold into aluminum (Kirkendall Effect). If a hybrid circuit is manufactured using die with aluminum metallization, it is certainly preferable to use aluminum for bonding. This is because the gold-aluminum interface will then occur on the substrate, away from the heat of the transistor. This is important since the formation of intermetallics, $AuAl_2$ or Au_5Al_2, is accelerated by temperature. However, *these interfaces*, even though they occur on the substrate, are nonetheless sensitive to weakening. Which intermetallic compound is formed depends on the amount of gold available in the bonding area. If the *gold* is thin then Au_5Al_2 will be formed. If the gold is thicker then Au_5Al_2 will be formed. The end result is the same; voiding and a weak bond which eventually lifts. The entire process can be accelerated by thermal cycling whereby cracks are formed in the brittle intermetallics.[3] Data presented later illustrates the comparison between failure rates due to bond lifts in aluminum and gold systems.

Another advantage which hybrids enjoy over discrete designs is the reduction of the number of interconnects.

7

An interconnect is a potential failure point. Reduction of the number of these points will result in a more reliable system. A calculation of the additional interconnects required in a typical discrete amplifier over the hybrid equivalent shows an increase of 127 interconnects in the discrete version.[2] Figure 2 summarizes hybrid life test data.

So it is apparent that the hybrid structure is inherently more reliable than a discrete assembly. But the heart of the amplifier, be it hybrid or discrete, is the transistor.

Reliability Data at 95°C Case Temperature

Part Description	Unit Hours Accumulated	# Fail	MTBF With 90% Confidence	MTBF — Gain Product
Transistor Chip	7,398,000	3	141 Years	—
CA2200 Hybrid	984,000	4	13 Years	221dB — Yrs
CA2600 Hybrid	577,000	4	8 Years	264dB — Yrs

Figure 2. Hybrid Circuit Life Test Data

IV. RF TRANSISTOR DESIGN CONSIDERATIONS

The performance which can be obtained from the amplifier is determined, in the end, by the transistor. Not only must the transistor provide performance, however, it must provide this performance for a reasonable length of time. If the transistor fails, then the hybrid fails and cost to the system operator is the result.

When the transistor engineer begins to design a device for use in CATV amplifiers, then, he is faced with two main requirements. The device must offer a certain level of performance and it must do its job reliably. We will now investigate the RF transistor and the considerations that go into its design.

1. Starting Material

Modern transistors are built using what is called the planar technology. This name arises from the fact that all areas of the transistor are found on the planar surface of the silicon wafer. Figure 3 illustrates a cross-section of a typical transistor structure as built using the planar technology. The first job of the designer is to decide what starting material he wishes to use for his transistor. The starting material consists of a wafer of silicon, approximately 10 mils thick and typically 2 inches in diameter. This silicon has been grown in crystal form while introducing a large concentration of impurities. This substrate silicon, then, is very heavily 'doped' so that the resistivity is very low. On the surface of this low resistivity silicon wafer is then grown a layer of silicon which is not so heavily doped so that the resistivity of this layer is higher than that of the substrate. It is the configuration of this 'epitaxial layer' that is very important to the performance of the device. It is this layer that will form the collector of the transistor. There are two parameters of the epi layer that can be specified by the engineer. One is the thickness and the other is the resistivity. The resistivity is chosen from operating voltage considerations. The transistor is intended for a specific purpose and presumably the voltage at which it will be operating is known. If the device will be biased at 20 volts in an amplifier, then the collector breakdown voltage of the transistor, BV_{CBO}, should be higher than 20 volts to provide a safety cushion. The phenomenon that occurs in a well-designed transistor at breakdown is called avalanche. This occurs when a sufficiently high reverse voltage is placed across a p-n junction. A field is formed across this junction and carriers are accelerated across the field. When the applied voltage equals the avalanche voltage a multiplication effect occurs in which atomic bonds are broken and the junction breaks down. This is the collector breakdown voltage and it is proportional inversely to the doping level of the collector or epi layer. By specifying epi material, then, the designer sets his voltage operating limit.

The other epi parameter of interest is the thickness of the layer. It has been found that epi thickness is closely tied in to both device reliability and performance. One parameter that is commonly used to describe high-frequency transistors is f_T. This is the gain-bandwidth product of the device or the frequency at which the common-emitter, short circuit current gain, h_{21}, equals unity. A high f_T means to the circuit designer better wide band gain performance. The f_T frequency can be related to the physical device in terms of the various delay times throughout the transistor. If the delay that a carrier sees

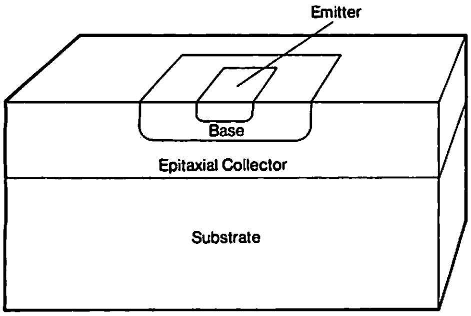


Figure 3. Planar-Epitaxial Technology

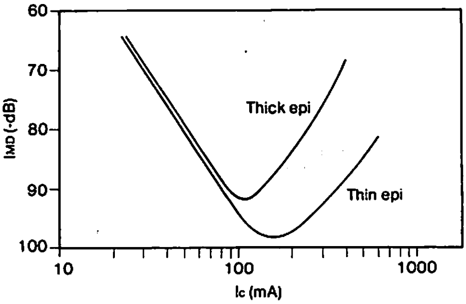


Figure 4. IMD Distortion Performance as a Function of EPI Thickness

in traveling through a device is less than in another device, then the f_t for the device with the least delay is higher. The thickness of the epitaxial region is related directly to one of these delay times; namely the $r_{sc}C_{Tc}$ time constant in the collector. The r_{sc} is the collector series resistance and to reduce this value for a given resistivity, we must reduce the epi thickness. There is another advantage to be gained from reducing the epi thickness which relates to distortion performance. Figure 4 shows a comparison of intermodulation distortion performance between two CATV transistors. The transistors are identical in all respects except that one device was built on epi material which was 50% thicker than the other. It is seen that the device which was built on thin epi material offers better distortion performance at higher current levels. The reason for this performance gain with thin epi is the fact that the maximum current density available in a device increases as the epi thickness is decreased. This occurs because of debiasing of the collector-base depletion region by the resistive epi region. The thin epi device, then, acts like a larger device at higher currents, resulting in better distortion performance at these higher levels.

Thin epitaxial material appears to yield very good transistors for CATV applications. Unfortunately there is a negative side to the story. The fact is that as the epi material is made thinner and thinner to achieve good performance the transistor becomes more and more sensitive to voltage variations. With thin epi the ballasting effect of the collector resistor is lost and the transistor loses ruggedness. The designer, then, wants to choose an epitaxial material which is as thin as possible for performance yet which is thick enough to avoid complete depletion and provide some collector ballasting.

2. Vertical Geometry

Once the starting material is decided upon, then it must be insured that a process is available which will yield a high performance vertical geometry. The importance of high f_T in the CATV transistor has been discussed. Another time constant which can be reduced in order to increase f_T is the delay due to carrier movement through the base region. The relationship for this delay is

$$t_b = \frac{W_b^2}{2.43\, D_{eb/n}\,(N_B'/N_{BC})}$$

This relationship describes the time required for carrier transit across the base region in terms of base width, W_b; diffusion co-efficient, D_{eb}; and doping gradient, N_B' and N_{BC}. The point here is that this delay time varies directly as the square of the base width. A desirable goal then is to produce a transistor which has a narrow base width. The well understood diffusion process can be used to control this parameter to a point. However, as narrower base widths are sought, device yields go down due to non-uniformities which are inherent in the diffusion process. State-of-the-art base widths with good uniformity are possible, though, by taking advantage of ion implant technology for the formation of the device junctions. Another advantage of implantation is that it makes possible steeper gradients in the emitter and base regions resulting in higher fields and shorter transit times in those areas.

3. Horizontal Geometry

One more item must be considered before the CATV transistor is ready to be built. A mask set must be designed, or, in other words, it must be determined what the device will look like, physically.

First, the basic device configuration must be decided upon. There are three transistor contact geometries in use; these are interdigitated, overlay, and mesh. The overlay and mesh configurations are used primarily for modern power transistors. High frequency devices are sensitive to parasitic capacitances and this favors the interdigitated design.

Figure 5 is a representation of typical transistor configurations. The base area is dictated by the power

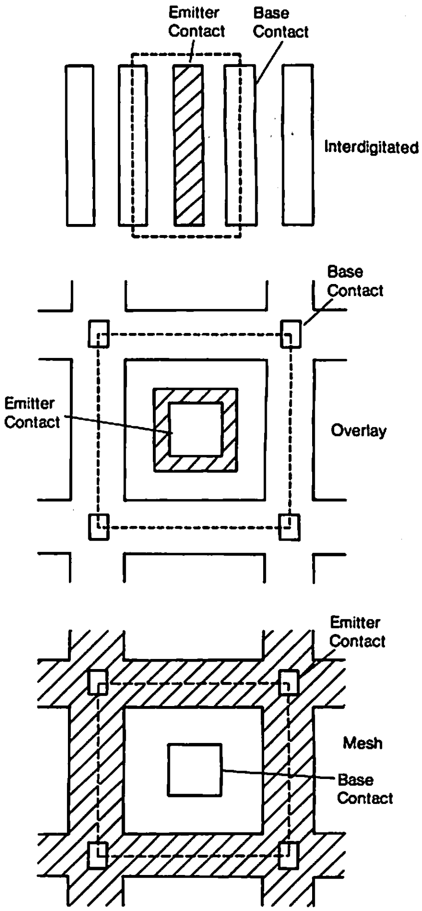


Figure 5. Typical Transistor Configurations

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handling requirements of the transistor. There must be enough area available to dissipate the heat which is generated. The amount of current to be handled by the device will determine what the minimum emitter periphery is. This is because at higher bias levels and frequencies a large transverse voltage drop occurs in the active base region under the emitter. This will have a de-biasing effect on the central portion of the emitter-base junction causing most of the current to pass at the emitter edges. Since it is known how much current the device will be required to handle, it is possible to calculate the amount of emitter periphery necessary to safely handle this current. The task now is to pack this amount of emitter periphery into the smallest base area possible, thereby reducing collector-base junction capacitance. Two examples of possible interdigitated designs having equal emitter peripheries are shown in Figure 6. It is seen

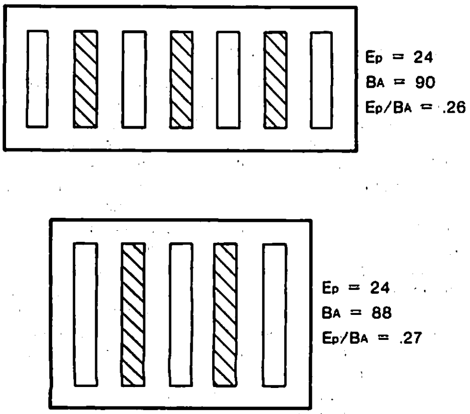

Figure 6. E_p/B_A Comparison for Square vs Rectangular Base Configuration

that slightly higher E_p/B_A ratios are possible with a design which is square compared to one with a higher aspect ratio. The problem with the square configuration is that the long emitter fingers required will result in considerable voltage drop along their length. The result is that part of the device is not being used and hot spots will develop. Not only will device performance be reduced, but it will soon fail because of overheating. The design with the higher aspect-ratio is desirable since the voltage drop problem is eliminated. Another advantage of this configuration is that it is inherently better able to dissipate heat since the cells are not so closely coupled as in the square configuration. This design also has a problem, however. Although the emitter fingers are now short enough, the active area of the device is now quite long. The middle portion of the device will tend to draw more current which is not efficient. The solution to this problem is to add ballast resistors between the emitter feeder arm and the emitter fingers. (See Figure 7.) The ballast resistors are thus in series with the emitter contact metallization. If an emitter-base junction site begins

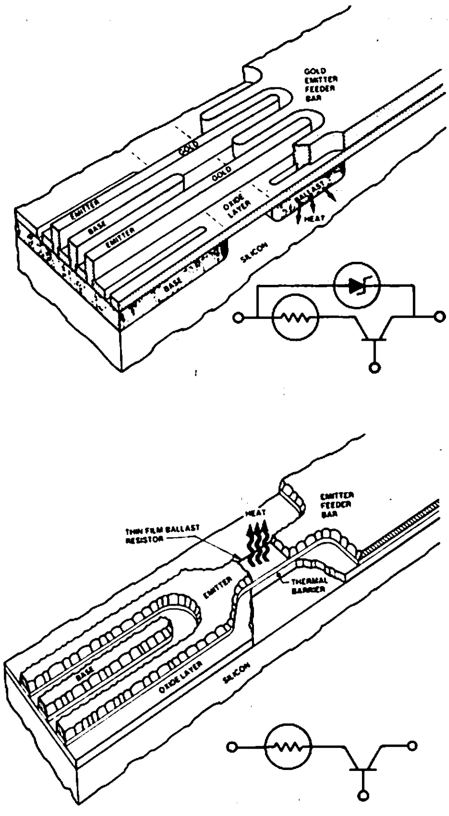

Figure 7. Ballast Resistor Configurations

pulling more than its share of current the series resistance will cause a proportionate drop in the input voltage for that site, thus limiting the current and preventing failure. An important point is the type of ballast resistor used. Two types of resistor are popular, thin film or diffused. Thin film resistors are susceptible to microcracking and they also are faced with a high thermal barrier since they sit on top of the silicon dioxide barrier. Diffused resistors are more reliable since they avoid the oxide barrier and are not susceptible to cracking.

It is also desirable to reduce the contact spacing and the emitter contact widths of the transistor for two important reasons.[1] A narrow contact spacing will allow more emitter periphery to be placed within a given base area. This is good since we have seen that gain performance depends directly on the amount of periphery available for current handling. A narrow emitter stripe is desirable since the resistance of the base region, r_b', varies directly as the emitter contact width and it is necessary to reduce the parasitic r_b' as much as possible for gain purposes. Incidentally, reduction of r_b' is good for noise figure too. Figure 8 illustrates the impact of emitter width on base resistance.

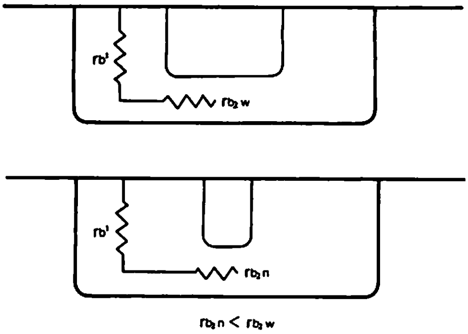

Figure 8. Effect of Emitter Stripe Width on Base Resistance

The last step in the construction of the transistor is the deposition of metallization so that contact can be made to the emitter and base regions. (See Figure 9.) The type

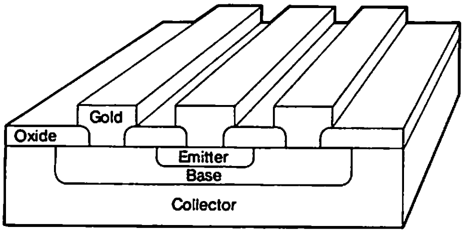

Figure 9. Transistor Metallization

of metal to be used is an important decision. The two metals that are low enough in conductivity that can be used for transistor metallization are gold and aluminum. Aluminum metallization has been used for years as a conductor for transistors. Its advantages are that it is a well-understood process, it offers a good silicon contact without any barrier metallization, and it is inexpensive. However, considering the micron contact geometry of the RF transistor and the fact that it will be mounted on a gold hybrid circuit, then the decision is considerably easier to make. For a CATV transistor, gold provides the following advantages over aluminum.[4]

1. Monometallic wire bonding system.
2. Electromigration resistance.
3. Low contact resistance with elimination of shorts due to silicon-metal alloying.
4. Corrosion resistance.
5. Oxide step coverage.

Allows use of tighter contact geometries.

Monometallic Wire Bonding System

As has been described, it is desirable to have an all-gold metal system for reasons of reliability. A monometallic system eliminates the formation of gold-aluminum intermetallics and the wire bond failures that result. Figure 10 illustrates life test data that shows an increased failure rate due to bond failures in the aluminum-gold system.

Life Test at 95°C Case Temperature

Part Description	Unit Hours Accumulated	Wire Bond Failure No's	Wire Bond Failure Rate %
601B, 200 Hybrids With Aluminum 3070 Die	1,162,000	24	4.1
2200, 2600 Hybrids With Gold 3040 Die	1,188,000	0	0

Figure 10. Wire Bond Failure Rates in Aluminum/Gold Life Test

Electromigration Resistance

It was shown earlier that it was desirable to achieve a high E_P/B_A ratio so as to obtain maximum performance from a device. This was achieved by placing the transistor contacts as close together as possible. The use of such tight contact geometry forces the use of very narrow metal fingers. The resulting high current densities can lead to reliability problems as a result of electromigration. Electromigration is a phenomenon which occurs in metal films as a function of time, temperature, and current density. For any given temperature, a certain equilibrium concentration of vacancies exists in all metal films. Self diffusion of metal ions throughout the film arise due to the metal ions being thermally activated into adjacent vacancies. In the absence of any external forces, the metal ion diffusion will be isotropic and will result in no net accumulation or depletion of mass in any given site. In the presence of an electric field, however, the metal ions experience a force due to their charge, inducing an ionic flux toward the cathode end of the film. In addition, the conduction flow of electrons in the metal due to the electric field will cause electron scattering off the activated ions and impart momentum to them inducing an ionic flux toward the anodic end of the film. In good conductors, the momentum exchange force dominates the electrostatic force and results in a net mass transport toward the anodic end of the film. The result is an open circuit in the metallization strip. This void formation is accelerated by high temperatures and current density.[5]

Aluminum has exhibited a high susceptibility to electromigration for current densities above 10^{-6} A/cm². Such a current density is easily realized in state-of-the-art RF devices. For a given device geometry there are only two alternatives to allow reduction of the current density in a device. Either the operating level can be reduced or a metal can be selected which has a higher mass and activation energy. The operating level cannot be reduced without a sacrifice in performance. We can still keep high performance and reduce the current density by using gold metallization. At 200°C, experiments conducted on identical transistors with gold vs. aluminum metallization showed an improvement in mean life time of two orders of magnitude using gold.

Contact Resistance

Gold cannot be used as a single layer metallization because of its relatively low silicon eutectic temperature and its poor adhesion to silicon and silicon dioxide. A barrier layer must be employed to prevent gold diffusion into the silicon and this barrier metal must offer good adhesion to silicon, silicon dioxide, and gold. Such a barrier is offered by a system utilizing platinum silicide, titanium and tungsten. The platinum silicide forms a good ohmic contact with the silicon; the Ti/W provides the necessary diffusion barrier and offers good adhesion to SiO_2 and silicon.

Aluminum has historically offered good ohmic contact without the need for barrier metals. In RF devices, however, at current densities well below electromigration densities, a problem of formation of silicon/aluminum alloy is ever present resulting in emitter-base shorts. Any hot spot formation will result in an increased alloying rate and early failure.

Corrosion Resistance

Under biased conditions, in a humid atmosphere, gold has demonstrated a lifetime more than 3 times that of aluminum. The failure mode in aluminum is electromechanical corrosion and gold is insensitive to this phenomenon.

Step Coverage

Gold offers tremendous improvements over aluminum in its ability to cover oxide steps without decrease in metal thickness or cracking. (See Figure 11.) Aluminum is deposited by means of evaporation in a vacuum where the mean free path of the aluminum particle is long. This means that equal coverage of all surfaces is impossible even if the target is rotated during evaporation. The plate-up gold system reduces step coverage problems to insignificance.

Narrow Contact Geometries

The RF transistor must have very fine horizontal geometry to achieve the performance required in a CATV system. With aluminum metallization these narrow finger widths are achieved by etching the aluminum to remove it. Such a process, if done very carefully, will at best result in fingers of uneven width which are susceptible to high current densities and the associated reliability problems. The gold system is capable of providing microwave geometries with insignificant variations in line widths. In fact, the geometry on present gold CATV devices is narrower than some low-noise microwave devices which are on the market today.

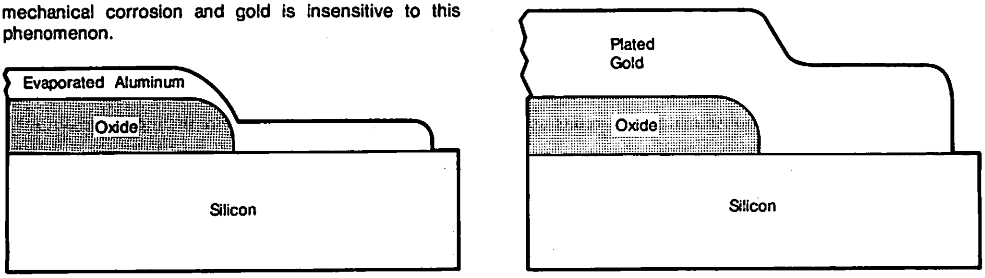

Figure 11. Oxide Step Coverage

V. SUMMARY

1. The CATV system operator is interested in performance with reliability in the amplifier equipment he uses.
2. The basic building block of the CATV amplifier is the hybrid circuit. The hybrid amplifier offers reliability advantages over discrete designs including gold circuit metallization and a reduced number of interconnects.
3. The heart of the hybrid circuit is the RF transistor.
4. The design of a reliable transistor for use in CATV amplifiers requires a knowledge of basic design values plus the availability of state-of-the-art processing. Points to be considered include:
   - starting material
   - vertical geometry
   - horizontal geometry
   - configuration
   - metallization.
5. Life tests show the improvements in reliability to be gained by careful transistor design.

APPENDIX

Derivation of reliability expression for chance failures[1]

$$R(t) = e^{-\lambda t}$$

If an original population of X_o items is continuously decaying so that there are X items at time t, the change of population in one interval dt is dX/dt. Divided by the total population X at t, this gives the negative rate at which the population changes at time t:

$$-\lambda = \frac{dX/dt}{X} = \frac{dX}{X}\,\frac{1}{dt}$$

then, $-\lambda dt = dX/X$

Integrating over the time period being considered,

$$-\int_0^t \lambda dt = \ln X/C = \ln X - \ln C$$

for $t = 0$, $X = X_o$

Then $C = X_o$

And $X/X_o = \exp\left(-\int_0^t \lambda dt\right)$

If the rate of decay, λ, is constant, then

$$X/X_o = \exp(-\lambda t)$$

Since X/X_o is probability of survival for a decaying population then

$$R(t) = X/X_o = \exp(-\lambda t)$$

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35/50 WATT BROADBAND (160–240 MHz) PUSH-PULL TV AMPLIFIER BAND III

This note describes the performance of a broadband ultra linear push pull amplifier designed for service in band III TV transposers and transmitters.

Devices used : two TPV 375.

Basic amplifier specifications :

IMD (1) = — 51 dB	at	P_o = 35 W	P_{gain}	= 10 dB
IMD (1) = — 48 dB	at	P_o = 50 W	input VSWR	: < 1.6
V_{cc} = 28 volts;		Total = 4.4 A	output VSWR	: < 1.5

(1) vision carrier — 8 dB, sound carrier — 7 dB, sideband signal — 16 dB.

General design Consideration

The principal aims were :

— employ a relatively simple solution permitting us to obtain the optimal performances from TWO TPV 375.

— simplify the design and reduce the cost.

The main consideration was to obtain the maximum output power with the best IMD over the band. To obtain this requirement the output match and losses must be the best possible in all the band.

The second consideration was to obtain the maximum gain by reducing the input matching circuit losses to a minimum.

These factors led us to choose matching circuits using quarter-wavelength transformers at the input and output which permit us to :

— reduce the load and source impedances to low values with low losses

— couple two transistors in a push pull configuration.

Because the output and input transistor impedances are in series, due to the push-pull configuration, the required transformation ratio is one half of that required for a single ended stage.

The first approach for the circuit calculation was made from the input and output impedances given in the TPV375 data sheet and matched to the proper impedance levels using a Smith Chart. The element values were then optimized with the aid of «COMPACT» program.

Amplifier Design

The basic block diagram for the amplifier is shown in Figure 1 and the circuit schematic is shown in Figure 2.

The input and output circuits are each composed of two networks : a quarter-wavelength transformer-balun and a matching network.

The quarter-wavelength transformer impedances have been chosen to be easily built using microstrip technology.

Input circuit

The input circuit is shown in Figure 3 and the input impedances are shown in Smith Chart 1.

The low transistor input impedances are transformed into higher impedances near the real axis by Capacitors FF.

The (EE, DD) series elements and (CC, BB) parallel elements collapse the amplifier input impedances around 8.5 Ω.

Since the devices can be considered in series at this point the impedance is doubled to 17 Ω. The quarter-wavelength transformer balun (AA) completes the match to 50 Ω.

The transformation ratio is 2.8 : 1.

The maximum theoritical input VSWR is 1.80 : 1 and the maximum experimental VSWR is 1.60 : 1.

Output circuit

The output circuit is shown in Figure 4 and the output impedances on Smith Chart. II. Since the output impedances are higher than the input impedances, the output matching network is simpler and the quarter-wavelength transformer ratio is lower.

The inductors aid the matching but primarily provide for good stability at the low frequencies, and are used for collector bias. The output quarter-wave-length transformer ratio is 1.6 : 1.

The maximum theoretical VSWR is 1.16:1 and the maximum experimental VSWR is 1.44:1.

Amplifier Performances

— IMD versus output power : Figure 5
— Input and output return loss and VSWR = Figure 6
— Gain versus frequency : see Figure 7
— 1 dB gain point compression : 70 W
— Bias conditions : V_{ce} = 28 V ; Total = 4.4 A.

Technology and layout considerations

The epoxy-Glass 1/16 inch (ε_r = 4.1) is used as board material except for the input and ouput transformers.
The glass - Teflon 1/50 inch (ε_r = 2.55) is used for the transformers (see the details Figure 8).
We have considered for a microstrip line that after W (Width) from the conductor strip edge the fields are negligible and we can size the ground conductor to be 3 W without perturbing the propagation. This kind of transformer has the following characteristics :
— We can have any impedance values within realizable min-max limits.
— The vertical dimensions are small and the mechanical realibility is good.
— Good repeatibility.

The bias circuits are included with RF circuits in order to give a compact amplifier : Figures 10 and 11 show the layouts and the Figure 12 the physical layout of the push-pull amplifier.

Combined pairs of push-pull Amplifiers

— In general several push-pull amplifiers are used for the final stage of the TV transmitter amplifiers.
They can be combined by pair with quadrature combiners (see block diagram Figure 9).
The advantage of using this kind of coupler is that the input and output VSWR become good (> 20 dB rtn. loss) in comparison with the relatively high original VSWR of the push-pull amplifier.

General Conclusions

— Pushpull techniques simplify the required circuitry and associated losses.
— The problems associated with 3 dB hybrids in cascade — insertion loss and imbalance — when four devices in parallel are required are minimized.
— With additional effort both the input and output VSWR could be improved to 1.2 : 1.
— Good repeatability in production without variable components being required.

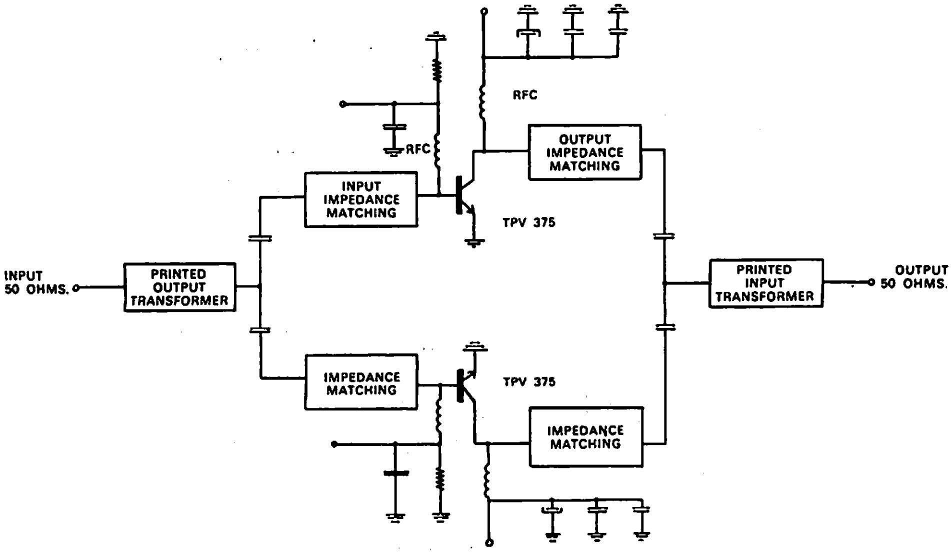

Figure 1. Push-Pull Circuit

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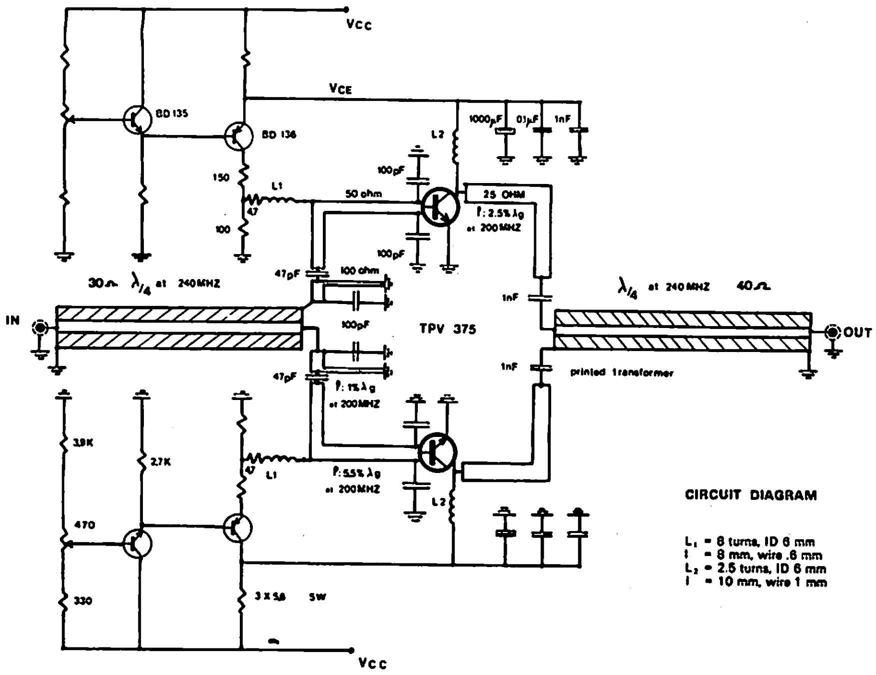
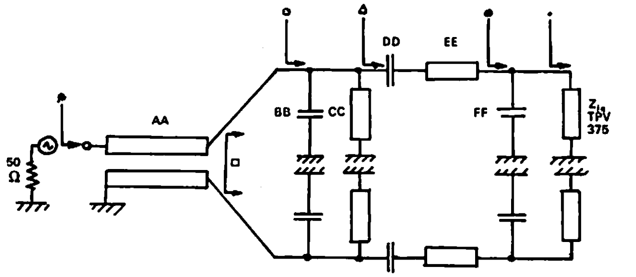


Figure 2. Circuit Diagram

On the smith chart the impedances are represented by :



	AA		BB	CC		DD	EE		FF
	Z_o (Ω)	L* (mm)	(pF)	Z_o (Ω)	L* (mm)	(pF)	Z_o (Ω)	L* (mm)	(pF)
Calc. value	30	313	139	100	11.3	47	50	80.8	238
Empirical value	30	313	100	100	15.0	47	50	82.5	200

* L is given for $\varepsilon_r = 1$

Figure 3. Input Circuit

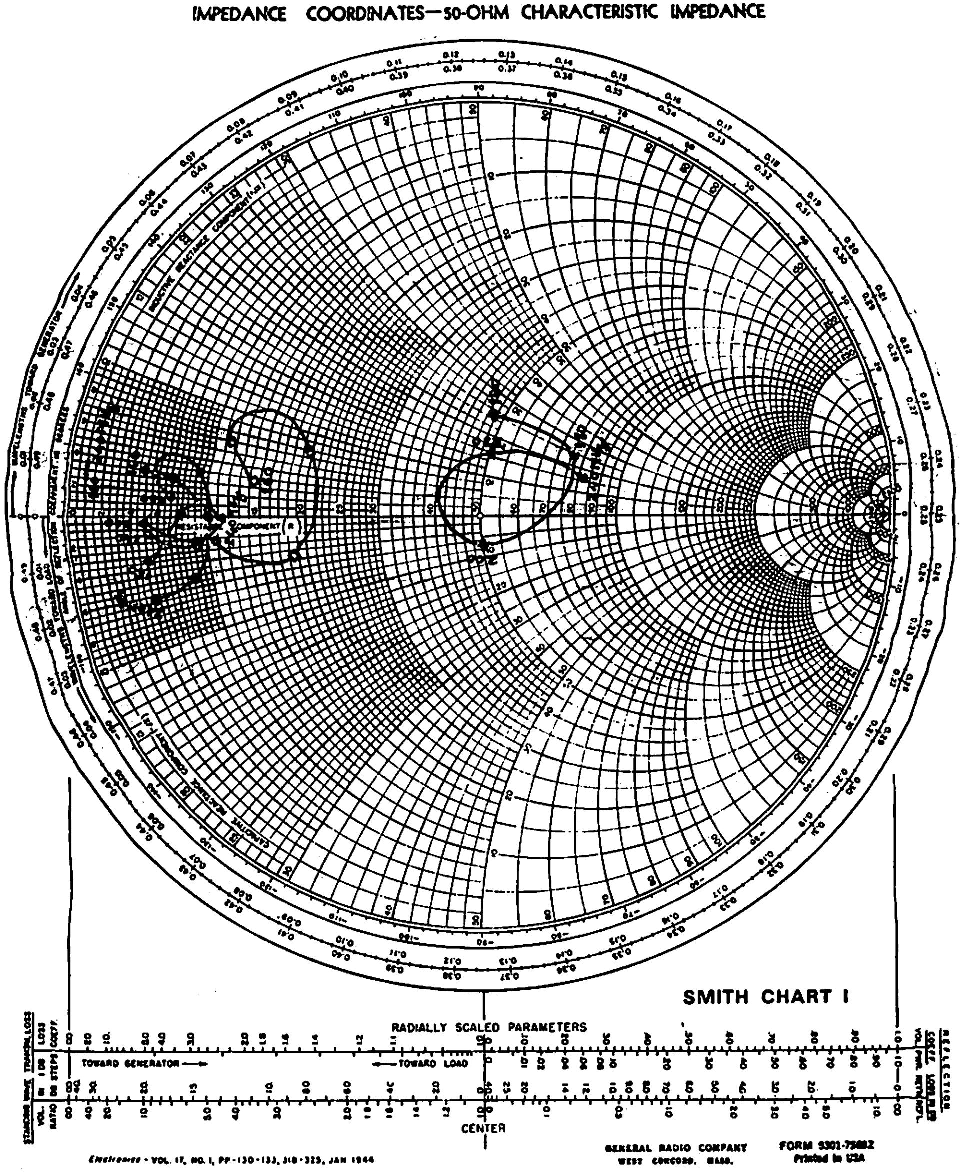


Figure 4A. Input Circuit

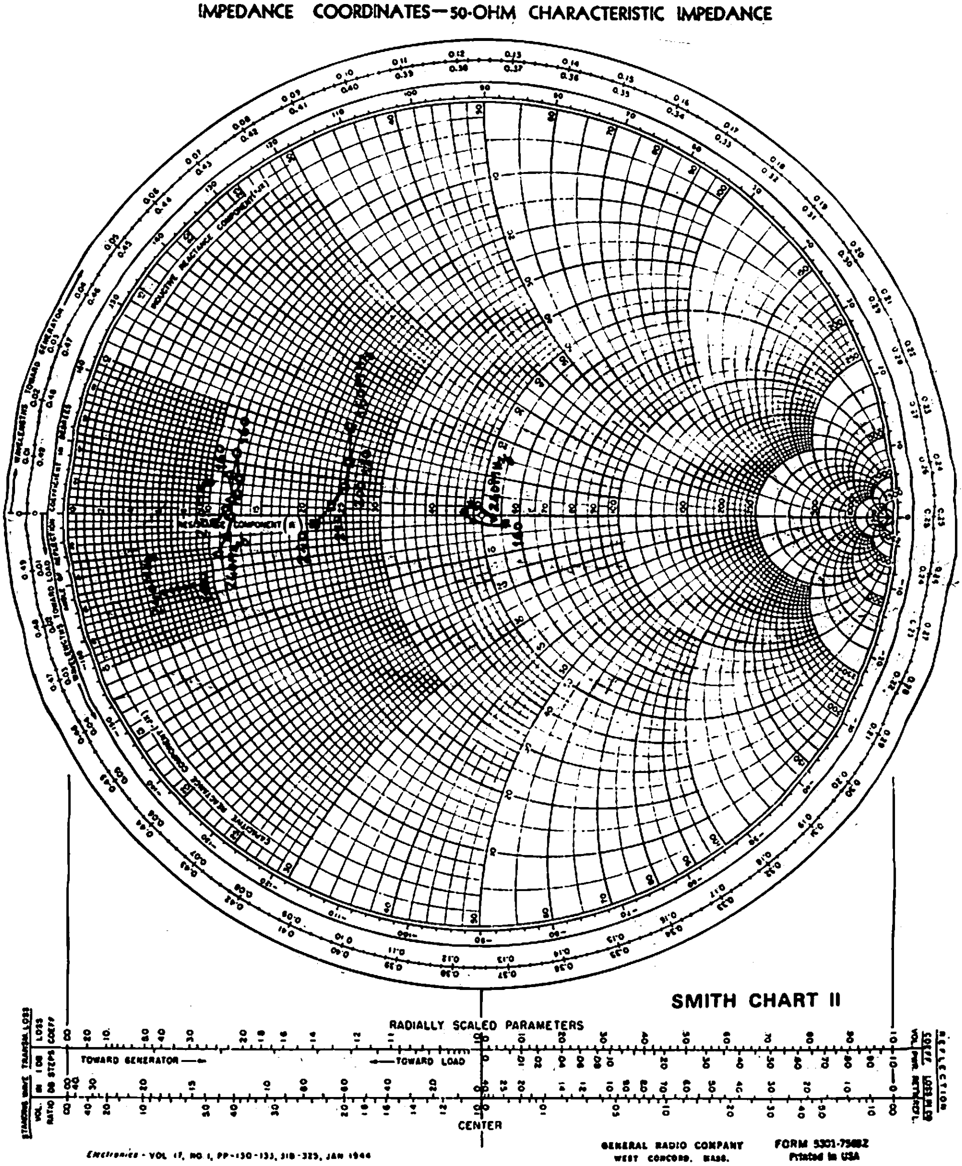


Figure 4B. Output Circuit

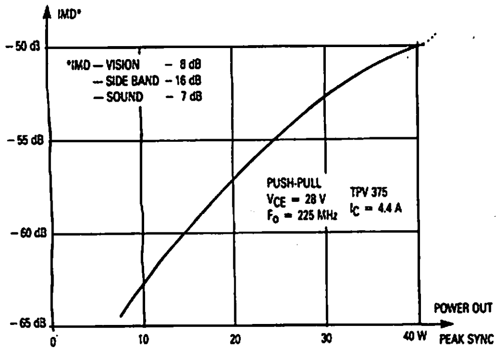


Figure 5. IMD versus Output Power

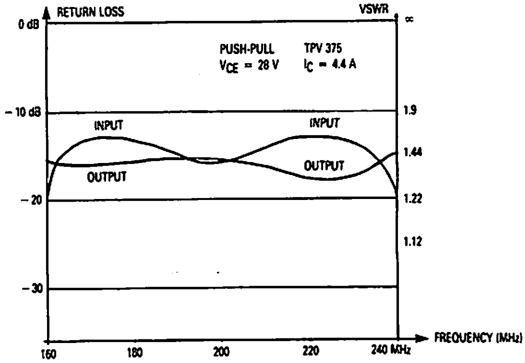


Figure 6. Input and Output Return Loss versus Frequency

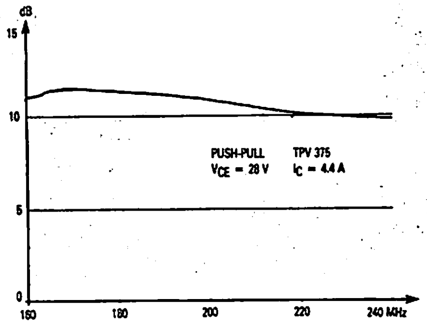
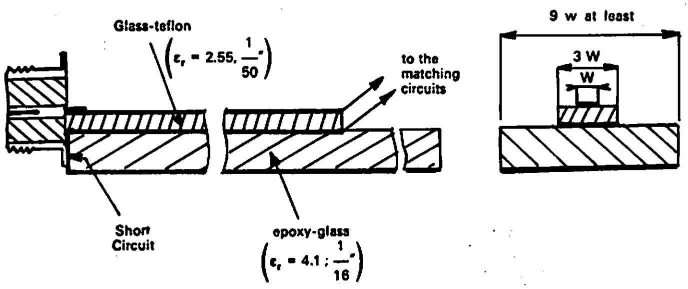
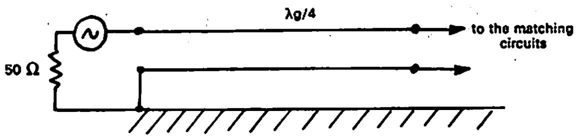


Figure 7. Low Level Gain versus Frequency



a.) Quater Wavelength Balun



b.) Equivalent Circuit

Figure 8.

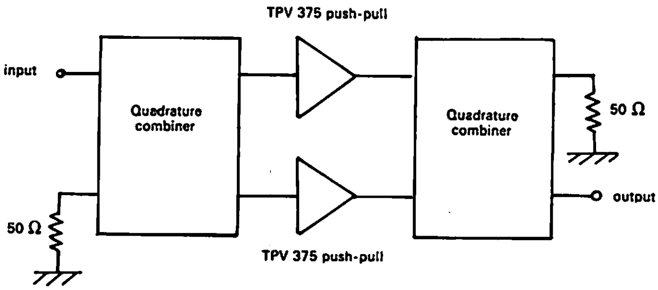


Figure 9. Combined Pair of Push-Pull Amplifiers

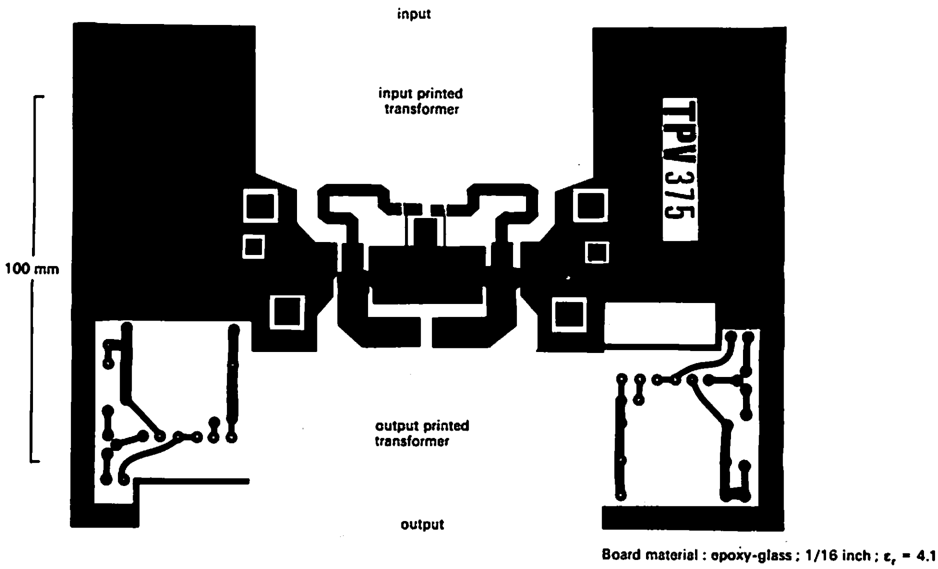


Figure 10. PC Board Layout (Not to Scale)

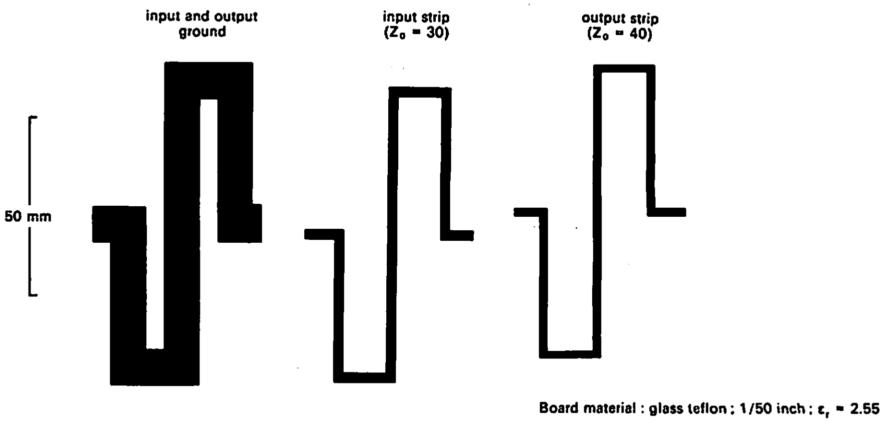


Figure 11. PC Board Layout for Input and Output Quater-Wavelength Transformer (Not to Scale)

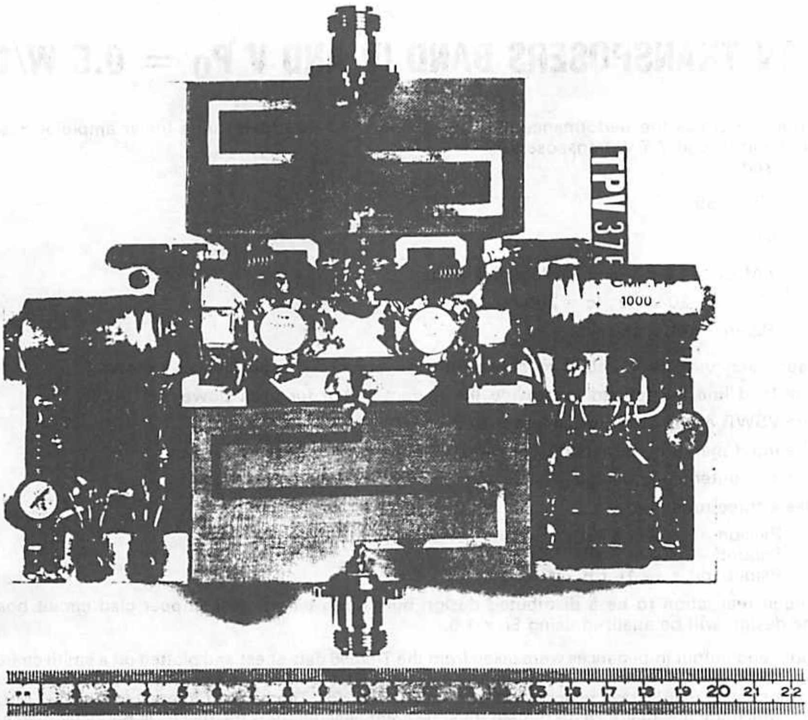
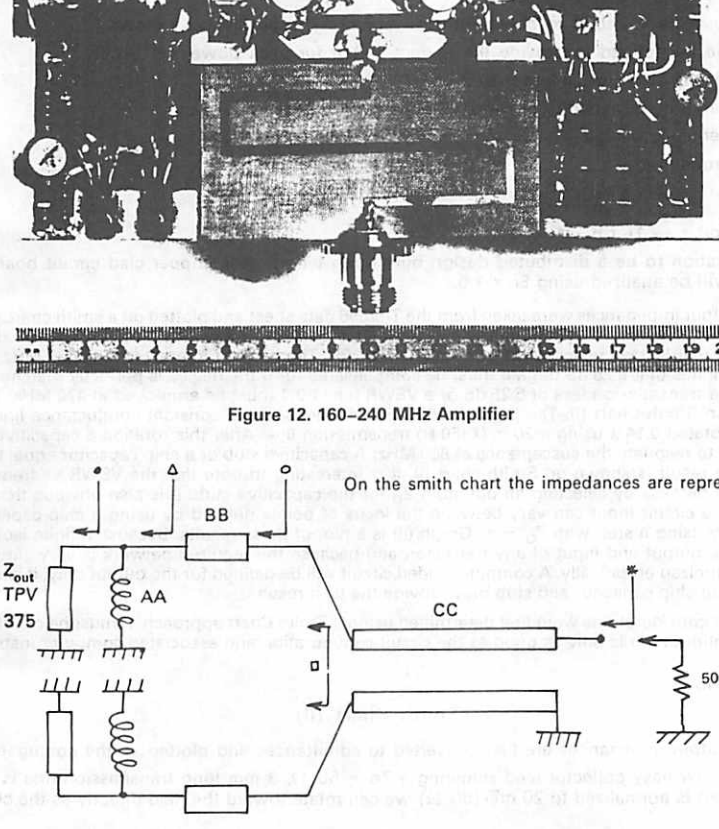


Figure 12. 160–240 MHz Amplifier

On the smith chart the impedances are represented by :



	AA	BB		CC	
	(nH)	Z_o (Ω)	L* (mm)	Z_o (Ω)	L* (mm)
Calc. value	11.7	21.6	37.5	33	312.5
Empirical value	53.1	25.0	37.5	40	312.5

* L is given for $\varepsilon_r = 1$

Figure 13. Output Circuit

TV TRANSPOSERS BAND IV AND V P_0 = 0.5 W/1.0 W

This note describes the performance of a broadband (470-860 MHz) ultra linear amplifier designed for service in band IV and V T V transposers.
Device used :

TPV 596.

Basic specs :

I.M.D. — 60 dB max. at Po = 0.5 watts
Vce = 20 volts ; Ic = 200 mA
Pgain = 11.5 dB min.

The approach used is intended to be straight forward and inexpensive as follows.

1) The load line be defined to provide the correct match for peak power (P. sync).
2) The VSWR at the collector be less than 2 : 1.
3) The input match be designed to provide flat gain with decreasing frequency.
4) Use computer aided design.
5) Use a three tone norm
   Pvision = — 8 dB
   Psound = — 7 dB
   Psideband = — 16 dB
6) Circuit realization to be a distributed design built upon teflon glass copper clad circuit boards. However the design will be analized using Er = 1.0.

The input and output impedances were taken from the TPV596 data sheet and plotted on a smith chart. First consider the input. To have flat gain with an optimum collector load, the basic physics of a class «A» biased device defines a gain slope of −6 dB/octave which must be compensated for. The band of interest is 470–860 MHz which is .915 octaves which implies that 5.25 dB of gain must be compensated for if the device is perfectly matched at 860 MHz. This means that a transmission less of 5.25 dB or a VSWR for 11.0:1 must be employed at 470 MHz. The input Z is converted to Y on Smith Chart (I). The point at 860 MHz will intersect the constant conductance line equal to 1.0 (20 m℧) if it is rotated 0.14 λ using a 20 m℧ (50 Ω) transmission line. After this rotation a capacitive stub or chip capacitor is used to resonate the susceptance at 860 MHz; A capacitive stub or a chip capacitor equal to 16.7 pF can be used, and the result is shown on Smith chart (I). It is interesting to note that the VSWR vs frequency can be adjusted for gain flatness by selecting an optimum Z_0 for the capacitive stub. It is also obvious that the locus of impedances at the circuit input can vary between the locus of points defined by using a chip capacitor, and the imaginary axis by using a stub with $Z_0 = \infty$. Graph (II) is a plot of these results. Because infinite isolation doesn't exist between the output and input of any transistor, and because the required network is very simple, the input circuit will be optimized empirically. A computed aided circuit will be defined for the output only. It is also indicated that a combination chip capacitor and stub may provide the best results.

The output circuit considerations were first determined using a Smith Chart approach. It must be clearly understood that computer optimization is only as good as the circuit configuration and associated computer instructions.

The approach follows :

Smith Chart (II)

1) The device output impedances are first converted to admittances and plotted as the conjugate (Y load).
2) In order to allow easy collector lead soldering a Zo = 50 Ω, 3 mm long transmission line is used. Since the Smith chart is normalized to 20 m℧ (50 Ω) we can rotate toward the load directly as the chart is configured.
3) Since the balance of the circuit used Yo = 10 m℧ (100 Ω) we next normalize the chart to 10 m℧. 100 Ω transmission line was chosen as a good compromise between physical length requirements and ease of realization on Teflon Glass.
4) The next element, a shorted shunt transmission line less than $\lambda/4$ in length reduces the imaginary part by moving each point of admittance along a line of constant conductance. The length was chosen to locate the lowest frequency point (400 MHz) near the real axis so that the locus of points would be more equally distributed about a 2.0 : 1 VSWR circle.
5) The resultant locus of points are then rotated with a 10 m℧ (100 Ω) transmission line to a degree which locates the admittance point of 860 MHz near the line of constant conductance equal to 2.0 on Smith Chart (II). This conductance is exactly equal to 20 m℧ since the chart is normalized to 10 m℧.

6) The final step is to use a parallel resonant circuit which will reduce the imaginary pacts at both the upper and lower frequencies.

The following approach was used to calculate the element values for the antiresonant circuit.

By observation of the smith chart it was decided to place the 460 and 860 MHz points on or just inside the 2.0 : 1 VSWR circle.

It then follows that

$$\text{at } f_1 = 460\text{ MHz} \qquad W_1C - \frac{1}{W_1L} = -0.4$$

$$\text{at } f_2 = 860\text{ MHz} \qquad W_2C - \frac{1}{W_2L} = 1{,}7$$

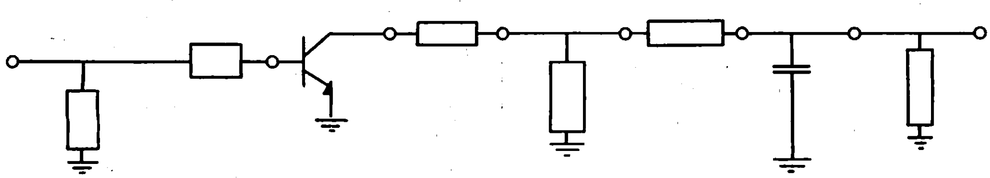
The 2 equations with 2 unknows are solved with the following result.

L = 0,189 nHy
C = 496.11 pFd

since we are normalized to 10 m℧

Lactual = 0.189/.01 nH = 18.9 nHy
Cactual = 496.11 × 0.1 pF = 4.96 pFd

7) The result is normalized to 20 m℧ with the final result shown.



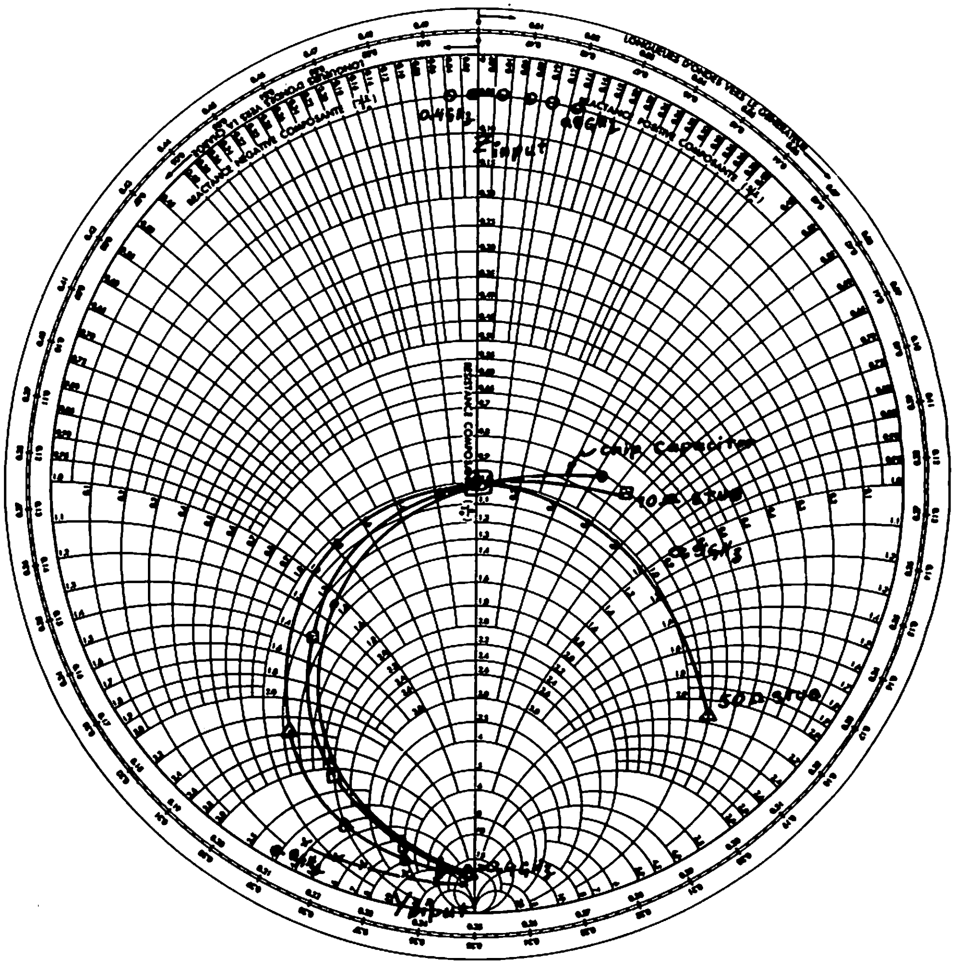
Zo	10 Ω	50 Ω	TPV 596	50 Ω	100 Ω	100 Ω		100 Ω
Calc. Value	45.7 mm	3.78 mm		3 mm	76.1 mm	29,3 mm	4.9 pF	50.4 mm
Empirical Value	8.5 48.8 mm	1.5 mm	Opti- mized Value	3 mm	98.8 mm	39.62	5.5 pF	61.6 mm

Graph (III) shows the various VSWR calculated compared to the theoretical best curve and the actual VSWR measured.

Graph (IV) shows the collector load VSWR for the calculated, optimized, and actual result.

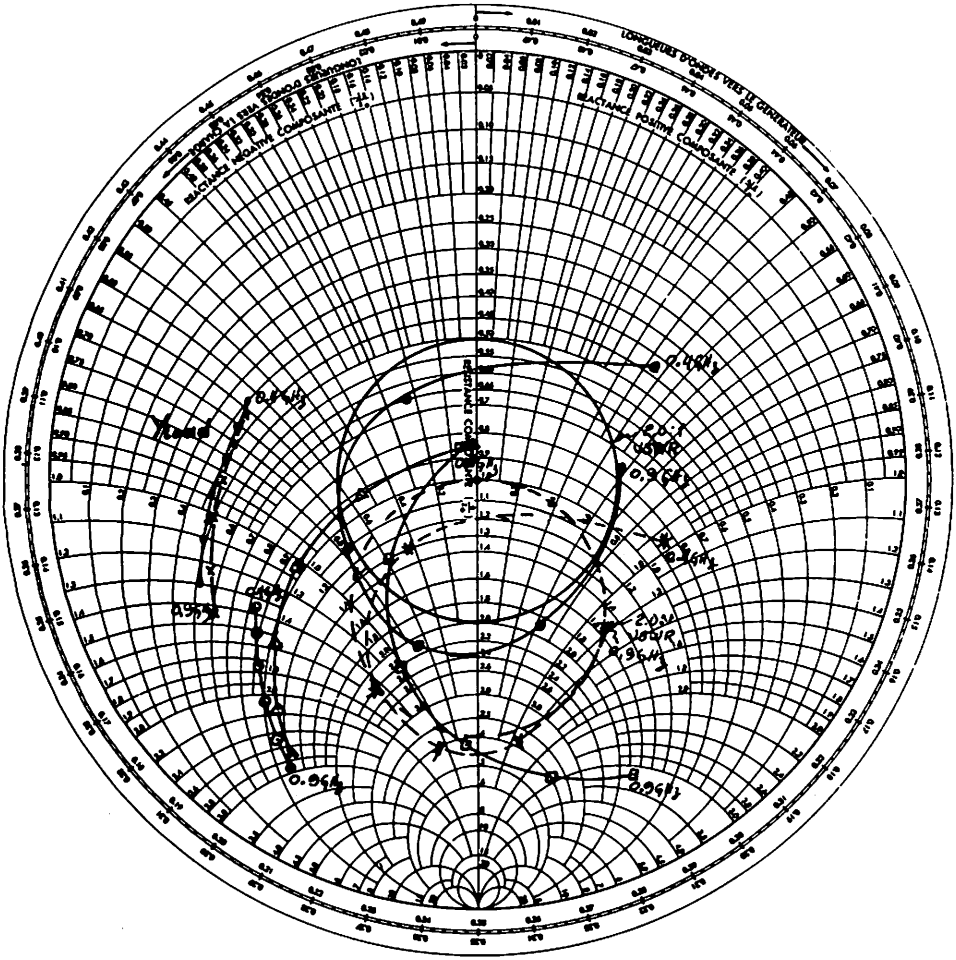
Graph (V) is a plot of the single ended amplifier results taken with a network analyzer. No component losses were considered for the theoretical and optimized analysis. The final circuit was also optimized empirically from 470–860 MHz using a network analyzer.

The following results are a summary of performance, bias conditions circuit configuration and recommended hybrid adaptation.



starting Imp.	⊙———⊙
rotated Adm.	×———×
final Adm. ω/Chip Cap.	●———●
final Adm. ω/10 Ω Stub	▫———▫
final Adm. ω/50 Ω Stub	△———△

Figure 1. Smith Chart (I)



starting Adm.
50 Ω rotation
100 Ω translation
equiv. shunt Ind.
100 Ω rotation
parallel L-C
final Adm. 50 Ω translation

Figure 2. Smith Chart (II)

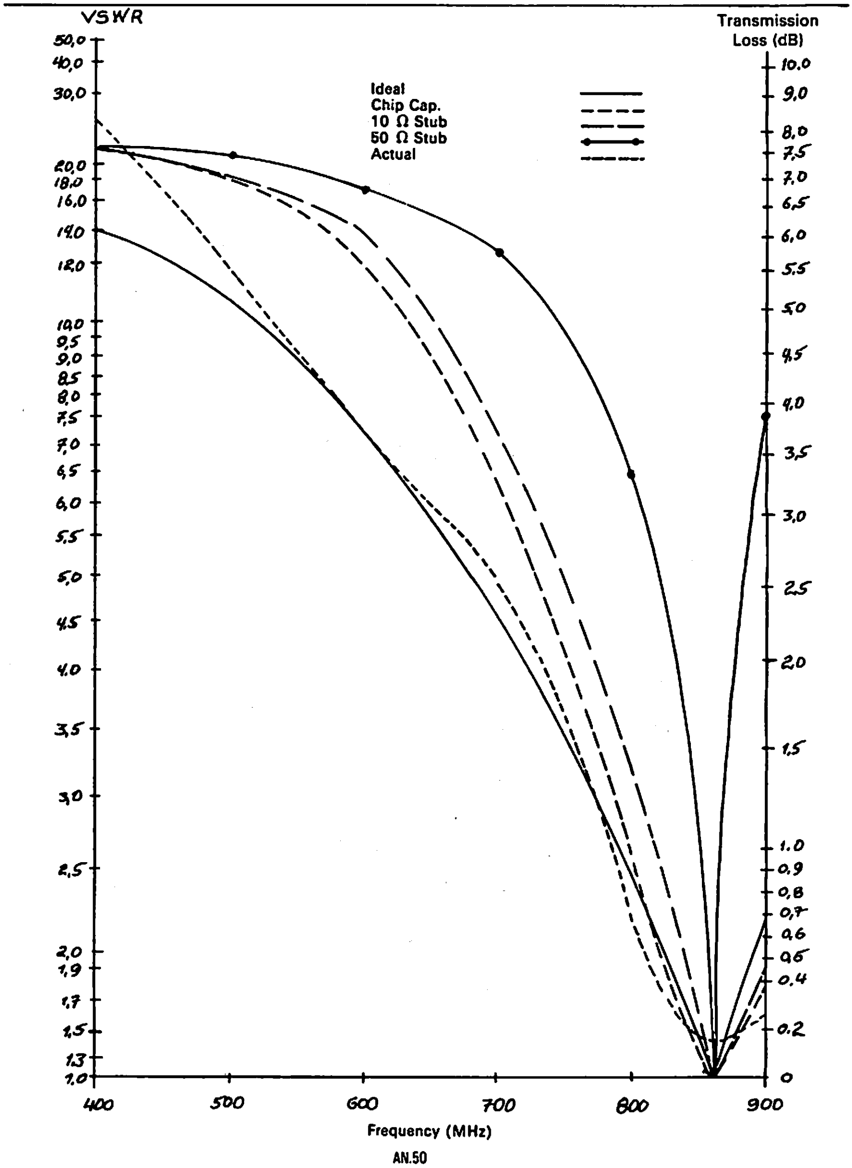


Figure 3. Graph III — VSWR versus Frequency

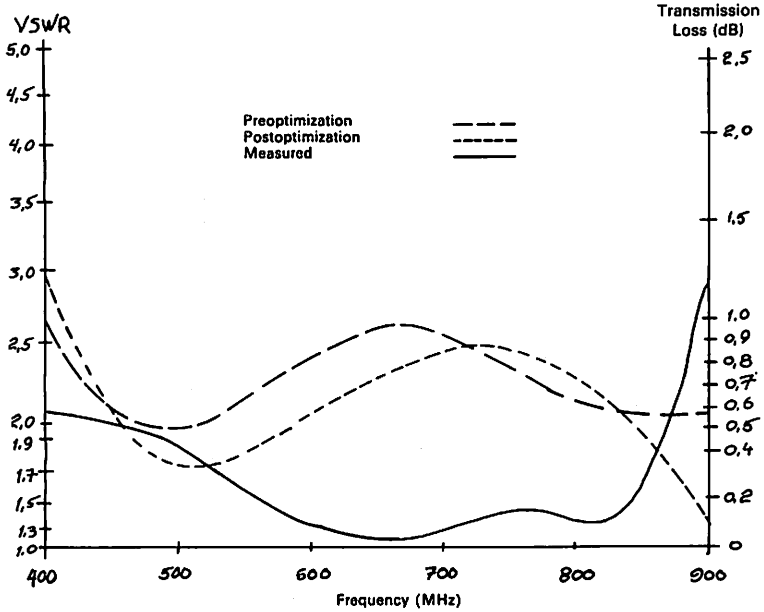


Figure 4. Graph IV — VSWR versus Frequency

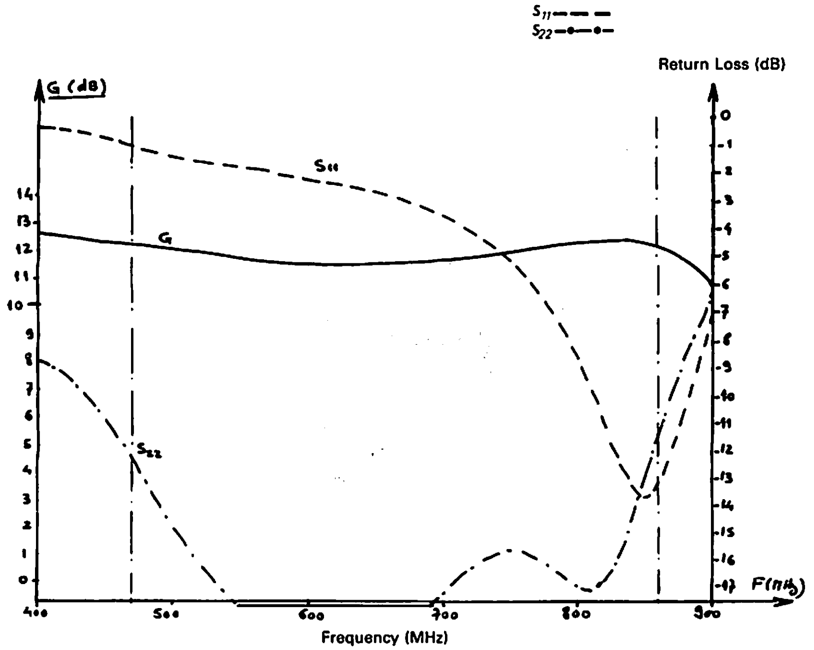
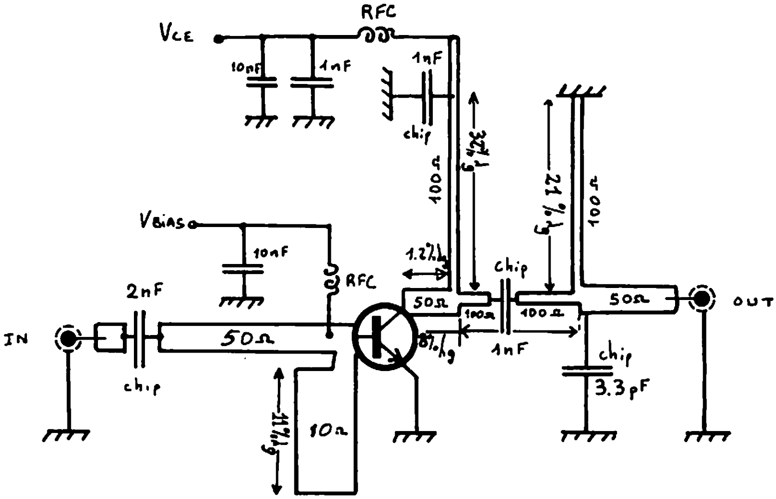


Figure 5. Graph V — TPV596 Amplifier Performance versus Frequency

7



Class A
V_{CE} = 20 V — I_C = 220 mA
f_0 = 860 MHz — WAVELENGTH (λg) at 860 MHz
(material: Glass teflon ϵ_r = 2.55 — 1/16")
Transistor — TPV596

Figure 6. Circuit Diagram for 470–860 MHz Amplifier

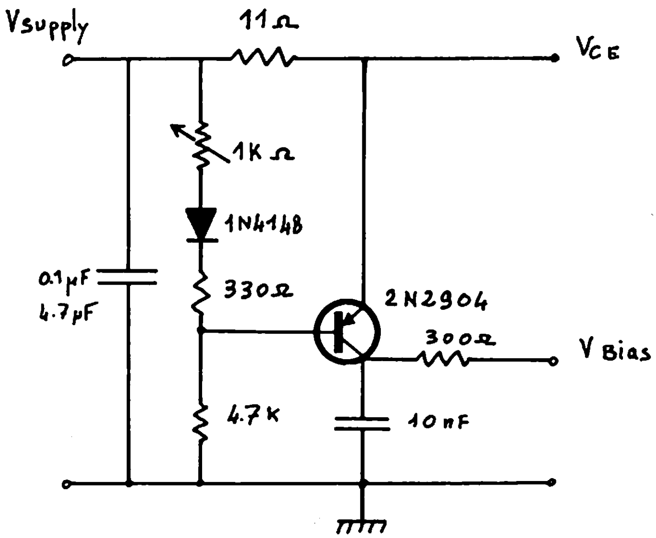


Figure 7. Class A Bias Circuit

7

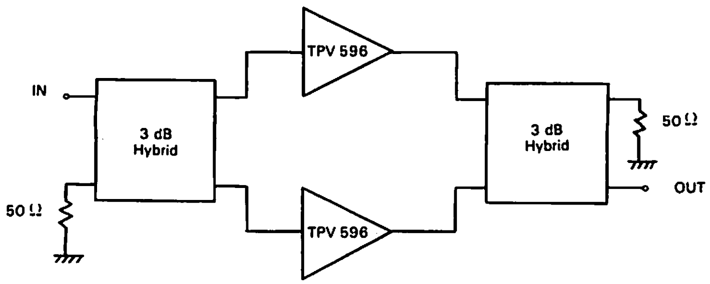
TPV 596 BROADBAND AMPLIFIER

FREQUENCY RANGE	: 470 MHz-860 MHz
POWER OUTPUT AT	: — 60 dB IMD* ⩾ 0.5 W
POWER GAIN	: 11.5 ⩽ G ⩽ 12.7 dB
INPUT RETURN LOSS*	: < — 1 dB
OUTPUT RETURN LOSS	: < — 11 dB
VOLTAGE SUPPLY	: ~ 23 V (V_{CE} = 20 V)
TOTAL CURRENT	: 220 mA

*IMD : Vision : — 8 dB ; Sound carried : — 7 dB ; Side band : — 16 dB

RECOMMENDED CONFIGURATION

*INPUT RETURN LOSS : This amplifier must be used by two connected together with two 3 dB quadrature hybrids to have a balance amplifier with a good input VSWR.



*3 dB - 90° Hybrid coupler from

- — ANAREN 10 264-3
- — SAGE wireline 3 dB Hybrid 4450 900

IMD VS OUTPUT FOR A SINGLE STAGE
VCE = 20 V-220 mA

F = 860 MHz ; Vision = — 8 dB ; Sound Carrier = — 7 dB ; Sideband = — 16 dB

Pout (W)	0.25 W	0.5 W	1 W
IMD (dB)	— 67 dB	— 61 dB	— 55 dB

F = 860 MHz ; IMD DIN 45004/B
RL = 75 ohms

1.5 V/75 ohms	IMD = — 66 dB
2 V/75 ohms	IMD = — 60 dB

1 W/2 W BROADBAND TV AMPLIFIER BAND IV AND V

This note describes the performance of a broadband (470-860 MHz) ultra linear amplifier designed for service in band IV and V TV transposers.

Device used : TPV 597

Basic specifications

IMD (1) = — 60 dB at P_o = 1 W
V_{ce} = 20 V ; I_c = 440 mA
P_{gain} = 11.5 dB.

(1) Vision carrier — 8 dB, sound carrier — 7 dB, sideband signal — 16 dB.

General design considerations

In general to obtain a flat gain for broadband amplifiers which use transistors with about — 6 dB power gain variation per octave we can use two techniques :

— feedback technique (eg emitter resistor and a negative feedback with a selective circuit between the collector and the base),

— or reflect the input or the output power selectivly to have an insertion loss of 6 dB per octave with 0 dB for the highest frequency.
(There is also another technique which uses a selective attenuator).

With the feedback technique we can have a good input and output match. With the second technique we need to reflect the input power and have a good output match in order to obtain a good IMD. It means the input VSWR is very high for the low frequencies.

The second solution is simpler than the first and if we use two amplifiers connected together with 3 dB quadrature hybrids to have a balanced amplifier this inconvenience disappears. We have chosen for this amplifier this second solution. For the larger broadband amplifier (eg 170-860 MHz) this solution must be rejected and the only acceptable solution is to use the feedback technique.

Amplifier design

The first approach fcr the circuit calculation was made by using the Smith Chart from the input and output impedances given in the TPV 597 data sheet to have, at the input, a reflected power so that the gain will be flat and at the output to obtain the best match possible.

INPUT VSWR VERSUS FREQUENCY TO OBTAIN A FLAT GAIN :

The power gain can be approximated by :

$$G \simeq \left(\frac{F_{max}}{F}\right)^2$$

F_{max} is the frequency for which power gain drops to unity.

The transmission loss due to the input reflection is :

$$\alpha = 1 - |\rho|^2$$

ρ is the reflection coefficient.

To have $G\alpha$ constant we must have :

$$G\alpha \simeq \left(\frac{F_{max}}{F}\right)^2 [1 - |\rho|^2] = G_H = \left(\frac{F_{max}}{F_H}\right)^2$$

G_H is the gain at the highest frequency used (F_H)

or

$$|\rho| \simeq \left[1 - \left(\frac{F}{F_H}\right)^2\right]^{1/2}$$

$$VSWR = \frac{1 + |\rho|}{1 - |\rho|} \simeq \frac{1 + \left[1 - \left(\frac{F}{F_H}\right)^2\right]^{1/2}}{1 - \left[1 - \left(\frac{F}{F_H}\right)^2\right]^{1/2}}$$

7

Figure 1 shows the theoretical VSWR versus frequency with an insertion loss of 0 dB (implies $\rho = 0$) for 860 MHz. We have defined the input circuit from the TPV597 input impedance to have an input VSWR as close as possible to this curve, and have assumed that output circuit losses versus frequency is negligible.

After we have calculated separately the input and the output circuits, we optimized some of the parameters by means of the global amplifier and the TPV597 S-parameters, with the COMPACT Program.

- — RF equivalent circuit : Figure 2
- — Program : Figure 3
- — Calculated gain and empirical gain : Figure 4
- — Calculated and empirical input VSWR : Figure 5
- — Calculated and empirical output VSWR : Figure 6

Amplifier Performance

- — IMD versus output power: Figure 7A
- — IMD versus frequency: Figure 7B
- — Input return loss and VSWR : Figure 5
- — Output return loss and VSWR : Figure 6
- — Gain versus frequency : Figure 4
- — Bias conditions : V_{ce} = 20 V; I_c = 440 mA

Technology and layout considerations

— The glass Teflon 1/16 inch (ϵ_r = 2.55) is used as board material. This substrate is soldered to the heatsink to have a good contact and repeatable results.

Figure 8 shows the circuit diagram and the bias circuit; Figure 9 shows the PC board layout.

Combined - Transistor Stage

In many instance the power output requirements of transposers exceed the capability of a single transistor, which forces the designer to use combinations of transistors. They can be combined by pair with quadrature combiners (See figure 10). Since quadrature combiners have the ability to channel the reflected power from the amplifier into the fourth port of the combiner it means the input and output VSWR become very low (VSWR < 1.2). The power gain is reduced due to the couplers insertion loss by 0.6 dB. Coupler imbalance should also be taken into account as causing some IMD degradation.

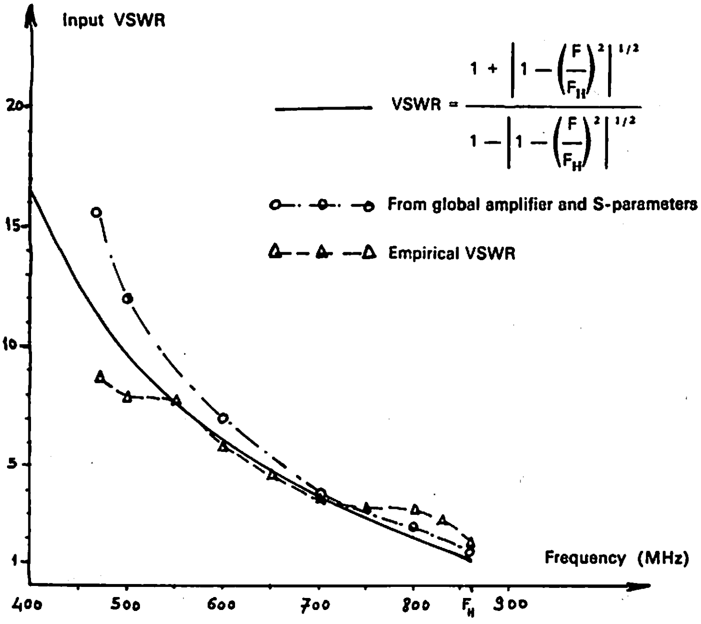
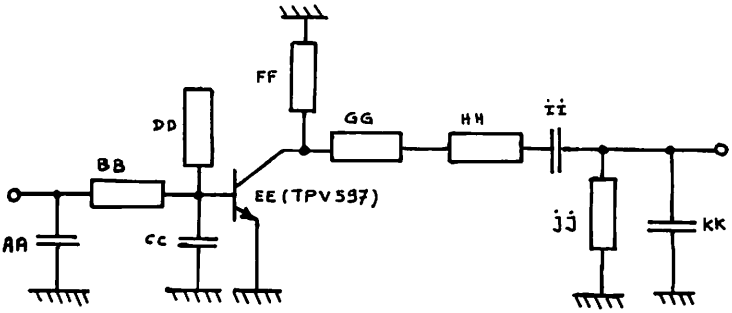


Figure 1. Input VSWR



	AA	BB		CC	DD		FF	
	pF	Z_0 (Ω)	L (mm)	pF	Z_0 (Ω)	L (mm)	Z_0 (Ω)	L (mm)
Calc. value	4.5	50	32.0	29.3	25	14	50	72.2
Empirical value	4.7	50	45.4	10.0	25	14	50	34.9

	GG		HH		II	JJ		KK
	Z_0 (Ω)	L (mm)	Z_0 (Ω)	L (mm)	pF	Z_0 (Ω)	L (mm)	pF
Calc. value	110	28.4	45	14	5.1	75	50	3.5
Empirical value	110	27.9	45	14	3.9	75	38.4	3.3

L are given for $\varepsilon_r = 1$.

Figure 2. RF Equivalent Circuit for Compact Program

```
MET  AA  ZZ
CAP  AA  PA   —4.61
TRL  BB  SE   50  —41.64  1
CAP  CC  PA   —25.39
ØST  DD  PA   25  14  1
TWØ  EE  S1   50
SST  FF  PA   50  —63.43  1
TRL  GG  SE   110  28.44  1
TRL  HH  SE   45  14  1
CAP  II  SE   —5.134
SST  JJ  PA   75  49.98  1
CAP  KK  PA   —4.129
CAX  AA  KK
PRI  AA  SI   50
END
```

CIRCUIT DEFINITION

```
470  500  600  700
800  860
END
```

FREQUENCY (MHz)

```
.92  176  2.38  72  .033  31  .55  —166
.91  175  2.21  71  .034  33  .54  —167
.93  171  1.80  63  .037  34  .56  —170
.93  170  1.57  59  .039  36  .59  —168
.92  169  1.40  54  .043  38  .58  —165
.91  167  1.30  52  .045  40  .58  —166
END
```

POLAR S PARAMETERS FOR TWØ EE (TPV 597)

```
.5
0  100  1  12
100  100  2  12
END
```

OPTIMIZATION DATA

Figure 3. Compact Program

VARIABLES (—)	GRADIENTS
(1) : 4.51899	(1) : —.894864
(2) : 32.0136	(2) : .704452E-01
(3) : 29.2938	(3) : 2.69282
(4) : 72.2399	(4) : .287748
(5) : 5.16145	(5) : 1.68585
(6) : 3.53445	(6) : —.267730
ERR. F. = 7.809	

HOW MANY ITERATIONS BEFORE NEXT STOP?, O ' RESULTS IN FINAL ANALYSIS.
WANT INTERMEDIATE PRINTS (YES = 1' NO = 0)? TYPE TWO NUMBERS : (I, J) : 0
SEARCH INTERRUPTED, FINAL ANALYSIS FOLLOWS :

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN <ANGL)	S21 (MAGN <ANGL)	S12 (MAGN <ANGL)	S22 (MAGN <ANGL)	S21 DB	K FACT.
470.00	0.88 < 134	3.53 < 86.3	0.049 < 45.3	0.11 < 105	10.97	0.75
500.00	0.85 < 128	3.46 < 68.4	0.053 < 30.4	0.12 < 109	10.79	0.90
600.00	0.75 < 92	4.19 < 12.2	0.086 <— 16.8	0.05 < 5	12.45	0.78
700.00	0.59 < 55	4.48 <— 39.2	0.111 <— 62.2	0.19 <—127	13.02	0.78
800.00	0.43 < 11	4.34 <— 93.2	0.133 <—109.2	0.26 < 180	12.75	0.86
860.00	0.20 <— 44	4.08 <—135.2	0.141 <—147.2	0.26 < 114	12.22	1.01

COMPACT PROGRAM

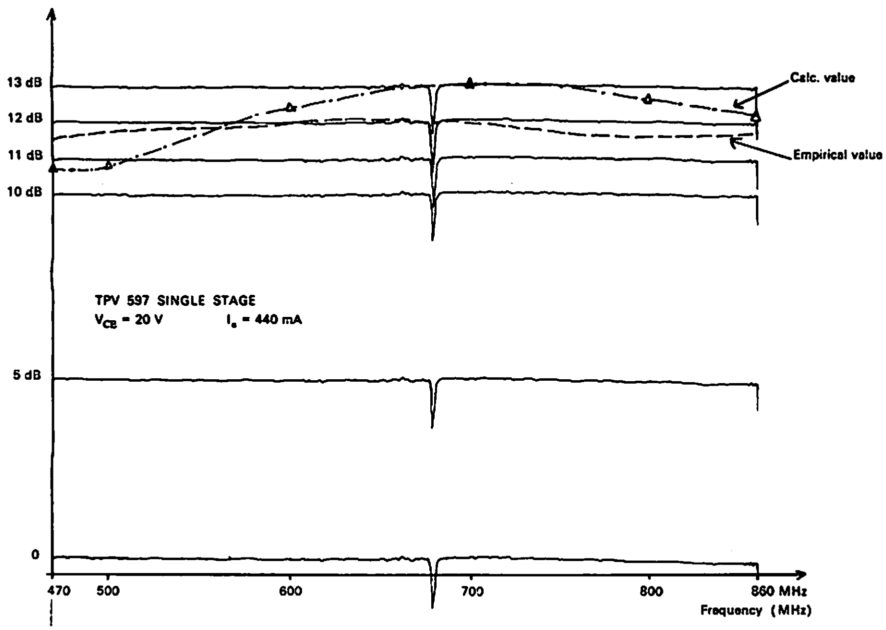


Figure 4. Gain versus Frequency

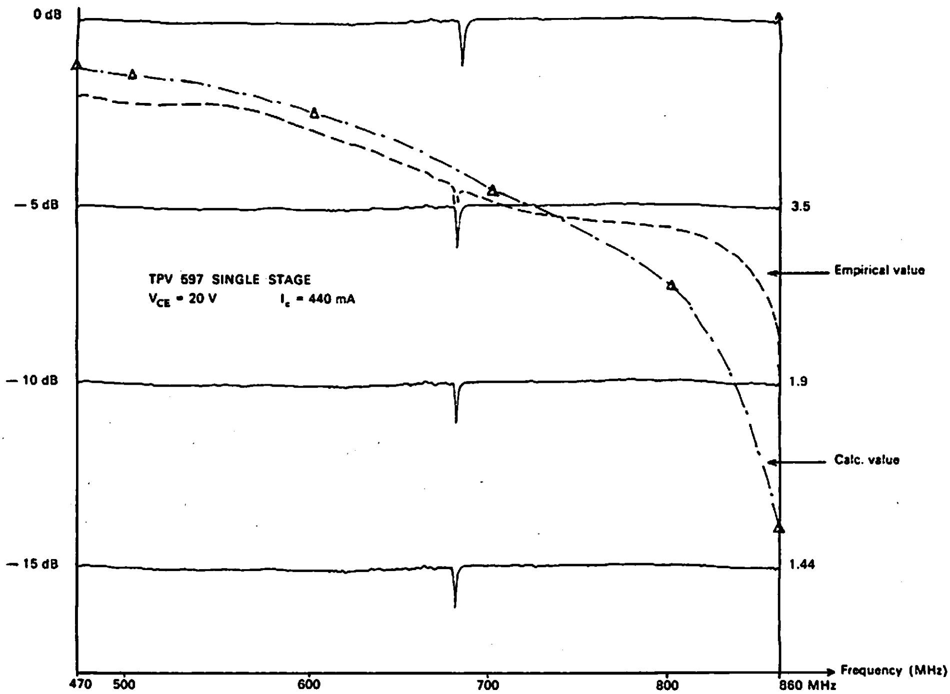


Figure 5. Calculated and Empirical Input Return Loss

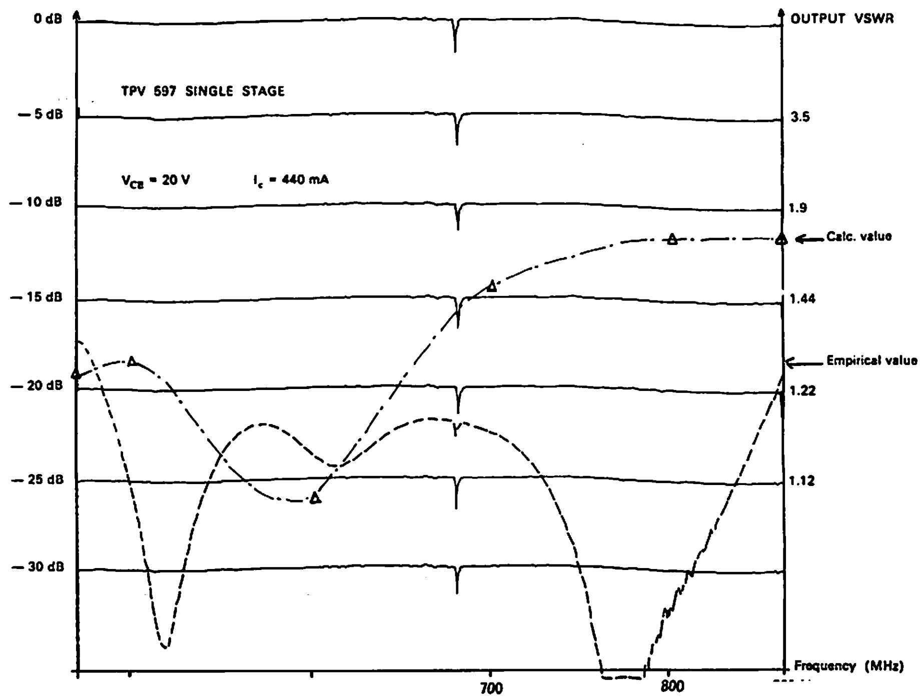


Figure 6. Calculated and Empirical Output Return Loss

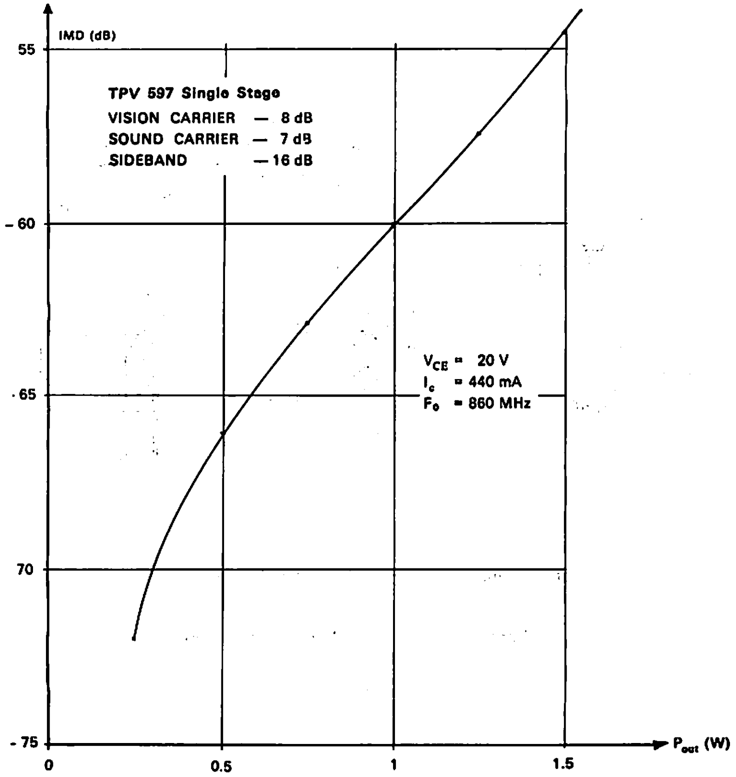


Figure 7a. IMD versus Peak Synch Output

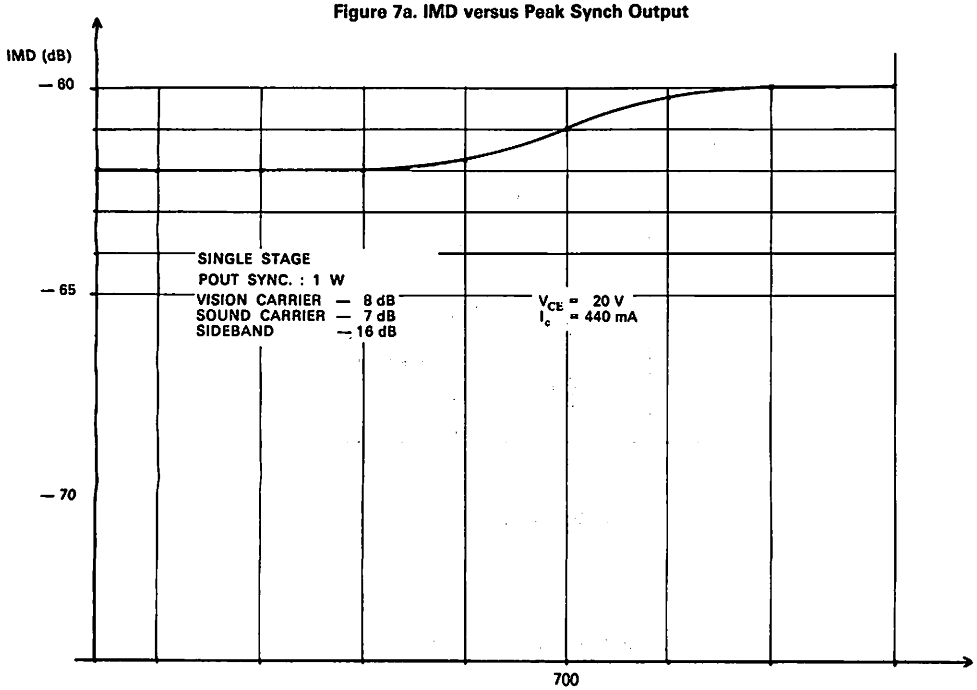
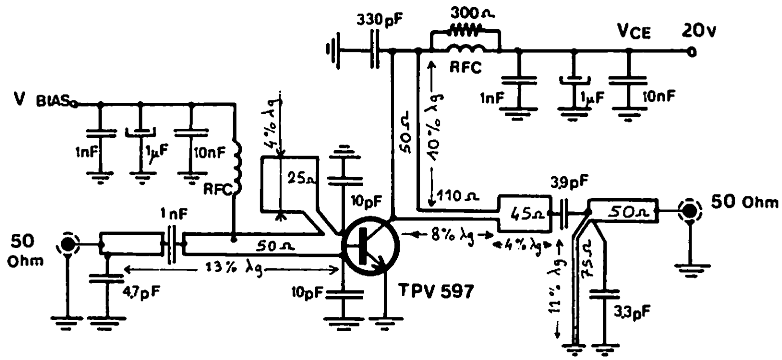


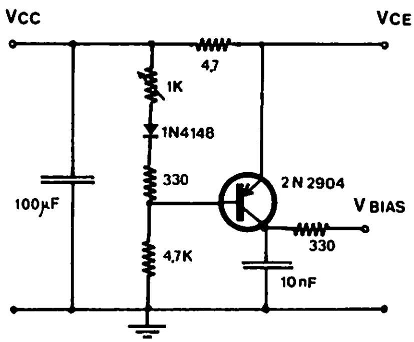
Figure 7b. IMD versus Frequency



Lengths are given at F_0 = 860 MHz $\left(\lambda g = \dfrac{3.10^8}{F_0 \sqrt{\varepsilon_{eff}}}\right)$

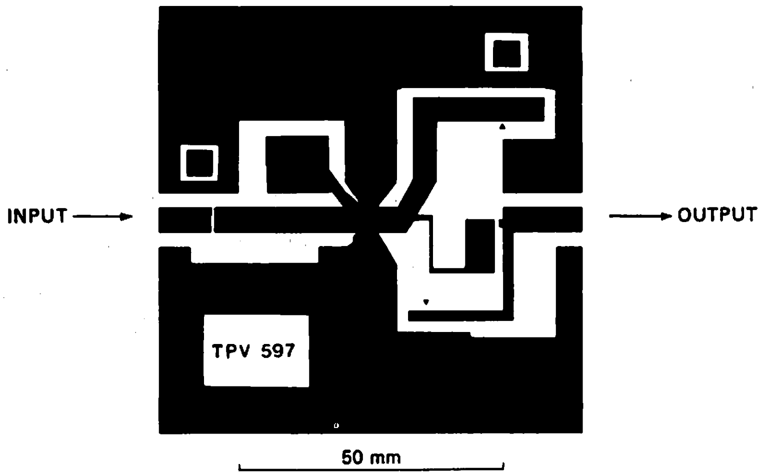
Glass teflon ϵ_r = 2.55, 1/16" board material.

a) Circuit Diagram



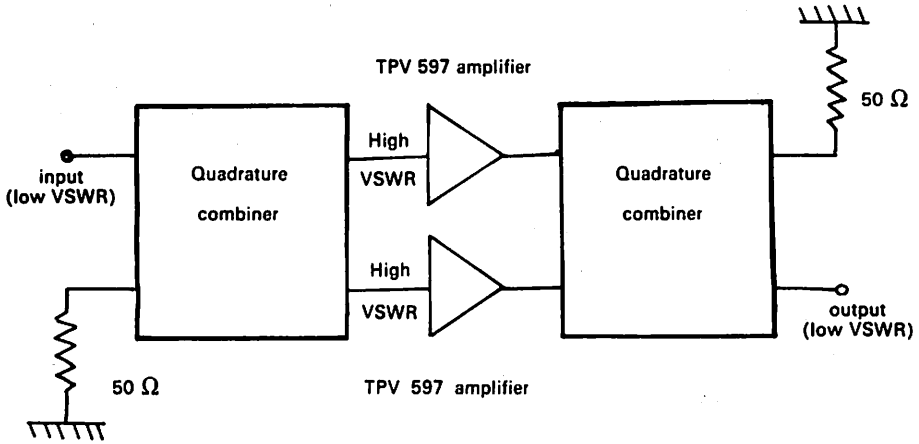
b) Class A Bias Circuit

Figure 8. Circuit Diagram and Bias Circuit



Board material : Glass Teflon ; 1/16 inch ; ε_r = 2.55

Figure 9. PC Board Layout (Not to Scale)



The 3 dB quadrature combiners can be supplied by :
- ANAREN (10 264-3)
- SAGE wireline (4450900)

Figure 10. Two Broadband Amplifiers Combined with Quadrature Combiners

HOW LOAD VSWR AFFECTS NON-LINEAR CIRCUITS

By Don Murray
RF Devices Division
Lawndale, Calif.

Reprinted from RF Design Magazine

If your amplifiers test out fine in the lab but fail QC testing, the testing environment – not the product – is likely at fault.

Consider the following scenario: You're designing and implementing into production a broadband Class C power amplifier. During your design phase, you follow all the rules of science and also dig into your bag of electronic tricks to meet the design specification. Your design is fabricated and tested successfully in the lab. Twenty-five more units are built in the lab and they, too, test out fine.

Confident that both design and production procedures are satisfactory, you begin series production. But when the first units reach RF test, not one meets specification. Yet when you retrieve the units, they test OK in the lab.

What's wrong with these amps? Probably nothing. This scenario, in one form or another, is all too common in the design and manufacture of non-linear RF circuitry. The culprit is correlation of test systems. A difference of .5 dB is enough to fail units that are perfectly good, resulting in unnecessary and expensive retesting or even reworking. Still worse, a half dB error will pass units that don't meet specs and never should be shipped.

Such correlation errors will disrupt an even more important function, that of maintaining product continuity. A device built in 1982 should perform the same as an identical model number device built in 1976. Another way of saying this is that a device tested in a 1982 test system should produce the same results when tested in a 1976 system. The key, of course, is RF correlation.

What is RF correlation? Simply put, RF correlation occurs when target error limits are established and adhered to on a continuous basis among two or more testing stations. Such correlation is essential to cost-effect production of non-linear RF and microwave power amplifiers, whose circuits are extremely sensitive to the impedance of their loads, either in test systems or equipment environments. It is easy to compensate for the insertion loss errors in an attenuator, but it is much more difficult to compensate for variations in the input impedance difference between attenuator pads, that is, the load VSWR.

Let's examine RF correlation on both an empirical and theoretical level.

EMPIRICAL APPROACH

The empirical approach is shown in Table I, where several test circuit loads (consisting of series attenuators, directional couplers and RF switches) were assembled. The insertion loss and input impedance of each load string was measured. Following this, the individual loads were connected to a given test circuit containing a common base microwave power transistor. The power meter used was also a constant.

Table I shows insertion loss, insertion loss corrections, indicated RF power, and actual power data of each load string. A maximum error of 0.52 dB was detected with a standard deviation of .19 dB. All these loads had a VSWR less than 1.1:1 at the frequency tested. A VSWR of 1.1:1 is better than the published specifications of commercially available attenuators, directional couplers, and RF switches from most leading manufacturers. A VSWR of 1.5:1 is a typical VSWR specification limit at 1.4 GHz. It must be noted that many users will gladly pay an additional nominal charge for components meeting a tighter VSWR spec.

THEORETICAL APPROACH

The vehicle for the theoretical discussion is the well known expression:

$$P_O = \frac{(V_{CC} - V_{CESAT})^2}{2R_L}$$

Where: P_O = Power output
V_{CC} = Collector supply voltage
V_{CESAT} = Collector-Emitter saturation voltage
R_L = Load resistance.

This expression is valid for a narrow range of R_L (10% range maximum). Over a wider range of R_L, significant changes in V_{CESAT} occur as a function of R_L. Output power varies with the square of V_{CESAT}. V_{CESAT} is a very strong function of collector current and transistor die temperature.

The theoretical approach will evaluate the changes in amplifier output power (P_O) for a given change in load resistance (R_L).

For simplicity, let us assume the following hypothetical conditions, which are typical of today's RF power transistors.

Hypothetical conditions:
V_{CC} = 28V
V_{CESAT} = 1.5V
P_{OUT} = 50W
Frequency = 1.0 GHz

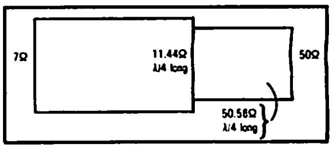
Solving for load resistance:

$$R_L = \frac{(V_{CC} - V_{CESAT})^2}{2P_O} = \frac{702.25}{100} = 7.02\Omega$$

Additionally, assume that a simple two-section impedance matching network matches the 7Ω to 50Ω. Let this two-section match consist of two λ/4 wave transformers.

Given the conditions we have hypothesized, the R_L of 7.02Ω represents the collector load that will yield the best simultaneous satisfaction of device efficiency, device gain, gain transfer characteristics, and saturated power.

For minimum Q, with a 2 section match, the transformation ratio of each section is



$$\sqrt{\frac{50}{7}} = 2.67.$$

$$Z_O \text{ 1st section} = \sqrt{(7)(2.67)(7)} = 11.44\Omega$$

$$Z_O \text{ 2nd section} = \sqrt{(7)(2.67)(50)} = 30.58\Omega$$

λ/4 @ 1 GHz = 2.95" = .075m

Table II shows the transformed impedance at the input of the matching network as a function of

Table I. Microwave Load Substitution Study

The vehicle used for this test was a production test fixture and correlation sample #2 for the TRW MRA1417-6 broadband, high-gain transistor. Measurements were taken at 1400 MHz with input power of 1.1W.

Load #	Measured Power Level	Circuit Return Loss	Collector Current	Measured Insertion Loss	Calibration Error	Actual Power	Delta from Reference	Load Input Return Loss	Impedance Angle	Real	Imaginary
1	1.1W	35 dB	—	30.03 dB	+.03 dB	thru	calibration	−40.2	99.1	49.8	+1.0
1	7.7W	16 dB	.51 A	30.03 dB	+.03 dB	7.75W	reference	−40.2	99.1	49.8	+1.0
2	7.6W	15.5 dB	.5 A	39.66 dB	−.44 dB	6.87W	−30.5		−77.5	50.6	−3.0
3	7.65W	15.5 dB	.51 A	39.68 dB	−.32 dB	7.10W	+.38 dB	−34.1	−171.5	50.4	−2.0
4	8.0W	15.5 dB	.51 A	39.8 dB	−.20 dB	7.63W	−.07 dB	−34.1	68.1	50.7	−1.9
5	7.2W	16 dB	.505 A	30.16 dB	+.16 dB	7.47W	−.16 dB	−30.1	−128.0	51.1	−3.0
6	8.3W	15.2 dB	.51 A	39.78 dB	+.22 dB	7.89W	+.08 dB	−31.7	−144.6	47.9	−1.5
7	7.75W	16.2 dB	.505 A	39.73 dB	−.27 dB	7.28W	−.27 dB	−32.7	11.9	49.0	−2.4
8	7.78W	16.8 dB	.503 A	39.7 dB	−.30 dB	7.26W	−.28 dB	−35.4	−111.9	49.1	−1.5

Largest Delta after calibration correction is 0.52 dB.
Mean value of the measured power = 7.41W.
Standard Deviation = .34W = .19 dB.

Note: −30 dB RETURN LOSS = ρ of 0.03 and VSWR of 1.06:1.

Table II. RL Effects on Output Power

Load Resistance (Ω)	Transformed Load Resistance (Ω)	Output Power (W)	ΔdB	Cumulative ΔdB
45	6.30	55.73		
			.095	.095
46	6.44	54.52		
			.093	.189
47	6.58	53.36		
			.091	.280
48	6.72	52.25		
			.090	.370
49	6.86	51.18		
			.087	.457
50	7.00	50.16		
			.086	.543
51	7.14	49.18		
			.085	.628
52	7.28	48.23		
			.083	.710
53	7.42	47.32		
			.081	.791
54	7.56	46.45		
			.080	.871
55	7.70	45.60		

Maximum Delta dB Vs. VSWR

VSWR	Maximum ΔdB
1.02	.17 (±.085)
1.04	.34 (±.17)
1.06	.51 (±.255)
1.08	.68 (±.34)
1.10	.87 (±.435)

various load impedances. Our example utilizes a real-to-real impedance match for convenience. The analysis also is appropriate for an imaginary-to-real match in that center of the VSWR circle at the input to the matching network will be rotated but won't change in magnitude from the data presented.

CONCLUSION

The data presented in table represents the power variation into a load with a VSWR of 1.1:1 relative to 50Ω. The result is a power output of 50W ± 5.3W (±.435 dB). The total Delta is 10.3W (.87 dB). This is enough to:

A) Make a good circuit look bad, or. . .

B) Make a bad circuit look good.

This analysis was done for a single frequency. The problem is compounded in a broadband environment by requirements for a good broadband load impedance.

TEST EQUIPMENT ACCURACY

Test equipment manufacturers have produced some very impressive equipment in recent years; however, the accuracy of a well constructed system using the latest equipment available is generally considered to be no better than ±3%. Considering the number of variables in RF testing and the magnitude of the task faced by the test equipment manufacturers, ±3% is no small achievement. However, ±3% is ±.13 dB. This ±.13 dB added to the ±.435 dB indicated earlier yields a total possible error magnitude of ±.565 dB. This adds up to a total possible error of ±14% into a load with 1.1:1 VSWR. The output power range of our amplifier is now 50W ± 7.05W.

Now we see how bad things can be, a few comments on reality are in order.

The author believes that the correlation target for the test of RF power devices should be ±0.2 dB, which we believe is the optimum tolerance for combining strict quality standards and the need for easy repeatability under series production conditions. If more than an occasional device fails this test, do not assume that the devices are at fault. Instead, first analyze the test circuit and then the test system to determine the reason for the additional error. Some suggestions on how to maintain a ±0.2 dB correlation are shown in Table III.

Table III. Notes

Suggestions to the Maintenance of Correlation

1. Serialize and document all components (attenuators, directional couplers, power meters, detectors, etc.) of the test system. Do not disturb the system once calibration has been performed. Calibrate the system once a month.

2. Require that loads have a calibration return loss ⩾ −35 dB (VSWR of 1.05:1) in frequency band of interest.

3. Dedicate test systems to specific circuits or products. This is necessary for both correlation and product continuity.

4. The placement of transistors in the test fixtures must be uniform. For instance, flanged transistors should be placed in the test fixtures with the device pushed towards collector load circuitry.

5. Be selective when using cables in test systems. For example, the MIL-C-17 specification for "RG" cable types says that RG-58 can have a characteristic impedance from 48 to 52Ω (maximu VSWR of 1.04:1) when terminated in a "perfect" 50Ω load.

6. Be very selective when choosing RF switches. The VSWR of a mechanical switch will vary with time.

7. If possible, terminate the system with a 50Ω load rather than an attenuator. Load manufacturers need only consider the VSWR of a load. However, for attenuator, tradeoffs must be made between VSWR and frequency response. Measure power and other performance parameters via calibrated directional couplers.

The 0.2 dB target is an achievable target in broadband test systems. However, a constant awareness of the test system capabilities and potential problem areas is mandatory. RF correlation problems will never go away, but they can be made easier to handle.

MATCH IMPEDANCES IN MICROWAVE AMPLIFIERS

and you're on the way to successful solid-state designs. Here's how to analyze input/output factors and to create a practical design.

By Roger DeBloois

The key to successful solid-state microwave power-amplifier design is impedance matching.

In any high-frequency power-amplifier design, improper impedance matching will degrade stability and reduce circuit efficiency. At microwave frequencies, this consideration is even more critical, since the transistor's bond-wire inductance and base-to-collector capacitance become significant elements in input/output impedance network design.

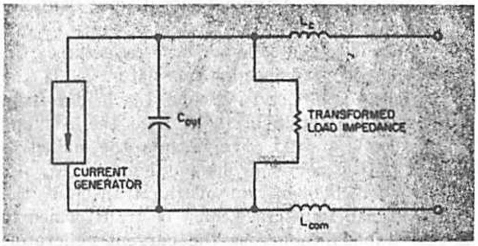
In selecting a suitable transistor, therefore, keep in mind that the input and output impedances are critical along with power output, gain and efficiency.

Unless the selected transistor is used at frequencies that are much lower than the maximum operating frequency, the input impedance is largely inductive with a small real part. The large inductance is due to bond wires that connect the transistor chip to the input lead of the package and to the common-element bond wires. The small real part of the input impedance is due to the large geometries required to generate high power at high frequencies; the base bulk resistance may be the predominant part of the real input impedance.

Use microstrip stubs at input network

The first and most important step in designing the input matching network for the selected device is to provide a shunt capacitance that will resonate the inductive component of the input impedance. This step forms the low-pass matching section of the network and should provide the smallest possible transformed impedance. To minimize the inductive component, the input and common-element lead lengths must be kept short.

The resonating capacitance is generally best provided by a microstrip stub. In some cases the stub producing the required capacitance is so large that a practical circuit size cannot be realized. It is best then to distribute as much of this capacitance as is physically practical and to provide the balance with high-quality chip capacitors.



1. In this output equivalent circuit, capacitance C_{OUT} is almost equal to the selected transistor's collector-to-base capacitance C_{ob}.

The first section of the impedance matching network is extremely important because it can degrade the stability of the amplifier if it is not well designed. Depending on the design frequency of the amplifier and the transistor selected, the resonated real impedance can range from less than 50 Ω to much higher. When it is below 50 Ω, an additional low-pass matching section can be conveniently added to achieve the required 50-Ω impedance at the input.

The higher-impedance case presents a special problem if microstrip techniques are used to build the matching network. The problem occurs because the resonated impedance may be as high as 300 Ω. Reducing this to 50 Ω by use of a low-pass network configuration requires a series-transmission line that will behave as an inductor. The rule of thumb is that the characteristic impedance of the transmission line must be at least twice the higher impedance before such behavior results. Examination of the accompanying table shows that characteristic impedance lines of greater than 100 Ω are very narrow. Narrow transmission lines (less than 0.01-inch wide) should be avoided wherever possible, because repeatability of width dimensions is poor. Also, the loss in a narrow line may become excessive. A better solution is to use a quarter-wave transmission-line transformer with a characteristic impedance

7

equal to the square root of the 50-Ω impedance product: $Z_o = \sqrt{50\,Z_R}$.

Make output bandwidth wider than input

The output impedance of a microwave power transistor is usually defined as the conjugate of the load impedance required to achieve the device performance. A typical output equivalent circuit is shown in Fig. 1. The capacitance C_{out} is nearly equal to the collector-base capacitance C_{ob} specified for the selected transistor. L_c is the inductance of the bond wires used to bridge from the collector metallization area to the package output lead, and L_{com} represents the inductive effects of the common element bond wires.

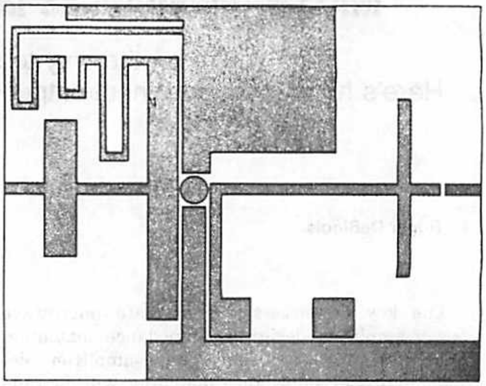
For correct operation of the transistor, the ultimate load impedance must be transformed to a real impedance across the current generator. This real impedance is determined by

$$R_L = \frac{[V_{cc} - V_{ce}\,(sat)]^2}{2P_{out}}.$$

The load impedance presented to the package terminals will contain the real impedance at the current generator, transformed to a lower value by the low-pass L section formed by C_{out} and the parasitic inductances L_c and L_{com}. Usually the reactive part of the load impedance is made inductive to tune out the residual capacitance of the device.

The output matching network should be designed so it has greater bandwidth than the input matching network. Providing a good collector match, both above and below the design frequency, ensures that the input power will be reflected before the collector VSWR rises to values that endanger the transistor. In this way the transistor is protected from off-frequency operation. The amount of additional bandwidth required for protection of the transistor depends on the ruggedness of the transistor used. The manufacturer's specifications for VSWR tolerance and input Q can be a guide for determining the bandwidth requirements of the input matching network.

One technique for obtaining the required bandwidth is to resonate a portion of the capacitive



2. **With this typical microwave amplifier breadboard layout,** the entire board can be soldered to a metal plate to provide a path for thermal cooling.

reactance of the transistor output impedance with a shunt inductor. The shunt inductor can also be used to feed the collector supply voltage to the transistor. Additional transformation may be obtained from a low-pass matching section. By adjusting the amount of shunt inductance and rematching with the low-pass section, the designer can create a truly broadband output match.

Don't overlook base and collector paths

In addition to matching the device impedances, direct-current paths must be provided to the base and collector of the transistor. The collector path is provided by the shorted stub in the impedance-matching network. The base path requires the addition of a choke from the base to ground. The choke can be a lumped element or a distributed shorted stub of sufficient impedance to be negligible in the circuit. A quarter-wavelength stub is ideal. The narrowest practical line should be selected. In addition a dc blocking capacitor is required in the collector circuit. Also needed is a bypass capacitor to provide the proper ac shorting point for the inductive stub in the col-

Microstrip Z_0 and velocity factor vs width-to-height (W/H) ratio.

(Prepared by Don Schulz, Applications Engineer)

W/H	Air K = 1.0 Z_o	Air V_P	Teflon K = 2.55 Z_o	Teflon V_P	Epoxy K = 4.25 Z_o	Epoxy V_P	Alumina K = 9.6 Z_o	Alumina V_P
0.630	168.425	1.000	110.683	0.657	87.986	0.522	60.977	0.362
0.695	161.878	1.000	106.258	0.656	84.414	0.521	58.441	0.361
0.766	155.370	1.000	101.865	0.656	80.870	0.521	55.927	0.360
0.844	148.909	1.000	97.509	0.655	77.360	0.520	53.440	0.359
0.931	142.506	1.000	93.199	0.654	73.888	0.518	50.985	0.358
1.026	136.171	1.000	88.941	0.653	70.463	0.517	48.566	0.357
1.131	129.916	1.000	84.745	0.652	67.090	0.516	46.187	0.356
1.247	123.753	1.000	80.616	0.651	63.775	0.515	43.853	0.354
1.375	117.692	1.000	76.565	0.651	60.524	0.514	41.568	0.353
1.516	111.746	1.000	72.597	0.650	57.345	0.513	39.337	0.352
1.672	105.926	1.000	68.721	0.649	54.243	0.512	37.164	0.351
1.843	100.242	1.000	64.944	0.648	51.223	0.511	35.053	0.350
2.032	94.706	1.000	61.273	0.647	48.291	0.510	33.007	0.349
2.240	89.327	1.000	57.714	0.646	45.451	0.509	31.030	0.347
2.470	84.115	1.000	54.271	0.645	42.709	0.508	29.123	0.346
2.723	79.076	1.000	50.951	0.644	40.066	0.507	27.289	0.345
3.002	74.218	1.000	47.757	0.643	37.527	0.506	25.531	0.344
3.310	69.546	1.000	44.692	0.643	35.094	0.505	23.849	0.343
3.649	65.065	1.000	41.759	0.642	32.768	0.504	22.244	0.342
4.023	60.779	1.000	38.959	0.641	30.550	0.503	20.716	0.341
4.435	56.689	1.000	36.292	0.640	28.440	0.502	19.266	0.340
4.890	52.796	1.000	33.760	0.639	26.439	0.501	17.892	0.339
5.391	49.100	1.000	31.360	0.639	24.544	0.500	16.594	0.338
5.944	45.600	1.000	29.091	0.638	22.755	0.499	15.370	0.337
6.553	42.291	1.000	26.952	0.637	21.069	0.498	14.218	0.336
7.224	39.173	1.000	24.938	0.637	19.485	0.497	13.138	0.335
7.965	36.233	1.000	23.047	0.636	17.998	0.497	12.125	0.335
8.781	33.484	1.000	21.275	0.635	16.606	0.496	11.179	0.334
9.681	30.904	1.000	19.618	0.635	15.305	0.495	10.295	0.333
10.674	28.491	1.000	18.071	0.634	14.091	0.495	9.472	0.332
11.768	26.240	1.000	16.629	0.634	12.961	0.494	8.707	0.332
12.974	24.143	1.000	15.288	0.633	11.911	0.493	7.996	0.331
14.304	22.192	1.000	14.043	0.633	10.937	0.493	7.338	0.331
15.770	20.381	1.000	12.888	0.632	10.033	0.492	6.728	0.330
17.387	18.702	1.000	11.818	0.632	9.198	0.492	6.164	0.330
19.169	17.148	1.000	10.830	0.632	8.425	0.491	5.644	0.329
21.133	15.172	1.000	9.917	0.631	7.713	0.491	5.164	0.329
23.300	14.385	1.000	9.074	0.631	7.056	0.490	4.722	0.328
25.688	13.162	1.000	8.299	0.630	6.451	0.490	4.315	0.328

Table continued

W/H	Air K = 1.0 Z_o	V_p	Teflon K = 2.55 Z_o	V_p	Epoxy K = 4.25 Z_o	V_p	Alumina K = 9.6 Z_o	V_p
28.321	12.036	1.000	7.585	0.630	5.894	0.490	3.942	0.327
31.224	10.999	1.000	6.929	0.630	5.383	0.489	3.598	0.327
34.424	10.047	1.000	6.326	0.630	4.914	0.489	3.284	0.327
37.953	9.172	1.000	5.773	0.629	4.483	0.489	2.995	0.327
41.843	8.370	1.000	5.266	0.629	4.089	0.489	2.731	0.326
46.132	7.634	1.000	4.801	0.629	3.727	0.488	2.489	0.326
50.860	6.960	1.000	4.376	0.629	3.397	0.488	2.267	0.326
56.073	6.343	1.000	3.987	0.629	3.094	0.488	2.065	0.326
61.821	5.779	1.000	3.632	0.628	2.818	0.488	1.880	0.325
68.157	5.264	1.000	3.307	0.628	2.566	0.487	1.711	0.325
75.144	4.792	1.000	3.010	0.628	2.335	0.487	1.557	0.325
82.846	4.362	1.000	2.739	0.628	2.125	0.487	1.417	0.325
91.337	3.969	1.000	2.492	0.628	1.933	0.487	1.289	0.325
100.700	3.611	1.000	2.267	0.628	1.758	0.487	1.172	0.324

lector-matching network.

Selection of a blocking capacitor is relatively straightforward. The capacitor should be chosen to provide low loss at the operating frequency while maintaining the capacitance at a value that inhibits low-frequency oscillation. The latter is caused by the series capacitor's tendency to display rising reactance with decreasing frequency.

Blocking capacitors must be large enough to preserve coupling characteristics down to a frequency where the shunt-feed chokes can effectively short the respective port to ground. Coupling capacitors should not be excessively large, or they may produce as much as 1-dB loss in gain with a corresponding decrease in efficiency in the case of collector coupling capacitors. The Q of the coupling capacitor determines the acceptable range of capacitance values and is generally inversely related to capacitance.

Bypass capacitors are selected by analysis of the same considerations as those for blocking capacitors. A large bypass capacitor (tantalum or electrolytic), placed from the dc feedpoint to ground, prevents tendencies toward low-frequency oscillation in the circuit. Also, it may be necessary to add smaller bypass capacitors to preserve stability over a wide range of frequencies.

Adjust for bandwidth and physical dimensions

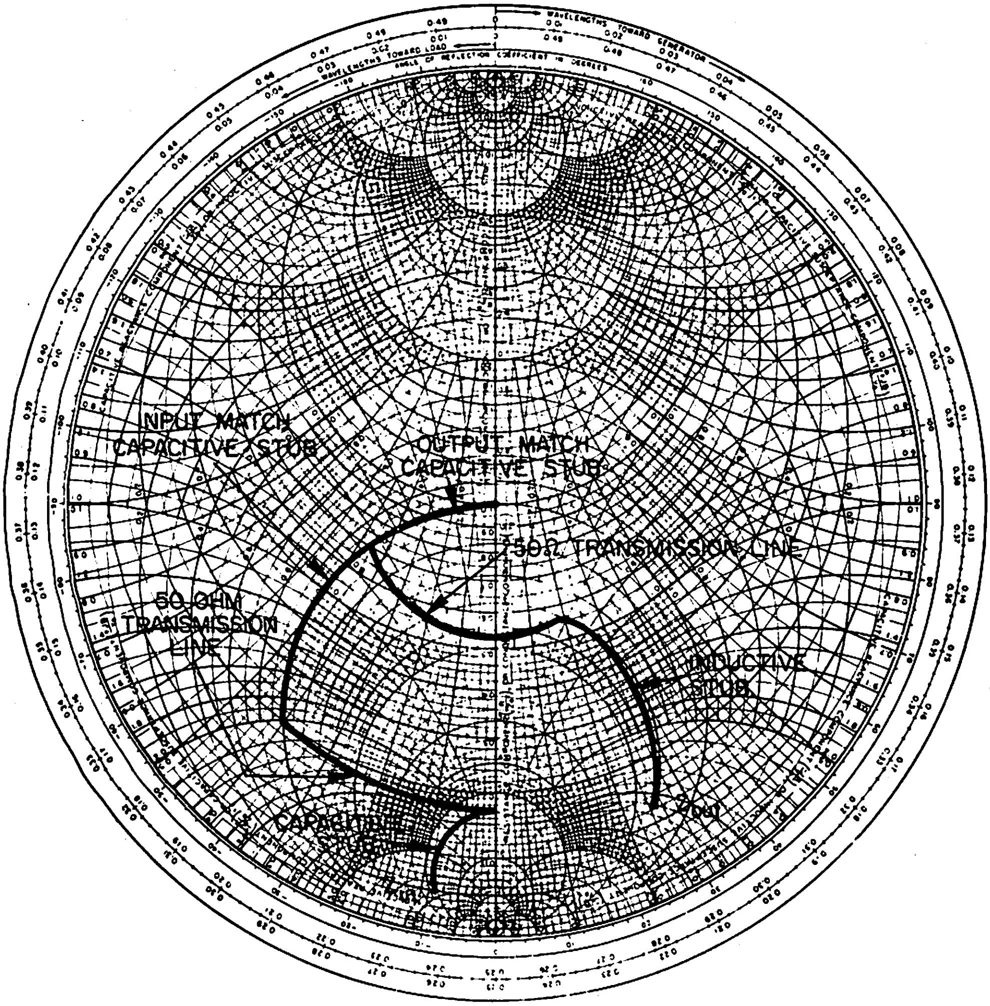
The circuit design may be adjusted quickly for bandwidth requirements through use of a computer optimization program such as Magic, offered by University Computing of Dallas, Tex. When that step is finished, electrical dimensions must be converted to physical dimensions.

At this point in the design sequence, the dielectric material must be chosen. Three commonly used materials are Teflon fiberglass, epoxy fiberglass and alumina. Above 500 MHz, epoxy fiberglass exhibits too many losses to be a good choice. Teflon fiberglass can be used up to several gigahertz; it has reasonable dielectric losses and is easy to process. Alumina, a ceramic, offers a high dielectric constant, good dimensional consistency and small circuit geometry.

When plastic materials are used, it's a good practice to measure the material thickness and dielectric constant, because variations are common. In a recent test the dielectric constant of a sheet of epoxy fiberglass material was measured at 4.55 at 1 MHz and 4.25 at 500 MHz. If the manufacturer's value of 5.5 had been used for the design of matching networks, considerable error would have resulted.

The physical dimensions of the matching circuitry may be calculated from the data in the table. The line lengths are scaled by the velocity factor, which is equal to $Z_o/Z_{o(air)}$ in air for a constant width-to-height ratio, W/H.

The final design of a typical breadboard microwave amplifier is shown in Fig. 2. The ground areas on the top of the board are connected to the microstrip ground plane by 2-mil-thick foil wrapped around the edges of the board and the areas directly under the emitter leads of the transistor. The foil is secured to the top and bot-



3. **The immittance chart,** with values specified for the design example, indicates the necessary inductive and capacitive stubs. Impedance transformations are achieved by 50-Ω series-transmission lines.

tom surfaces with solder. Plating may be used for production units. The entire board can be soldered to a metal plate to allow connector mounting and to provide a thermal path for the heat generated by the transistor.

The initial tune-up of the amplifier matching circuits can be expedited by use of a network analyzer and a precision load on the input or output connector. The circuit can be adjusted to match the nominal impedances supplied by the transistor manufacturer. Distributed stubs are purposely made longer than necessary and are adjusted to the correct length by trimming of the foil on the capacitive stubs. The inductive stub in the output network is adjusted by positioning of the bypass capacitor along the stub and the adjacent ground plane.

This procedure results in a load line that is fairly close to optimum. A transistor can now be inserted in the circuit and the collector matching network readjusted for maximum collector efficiency. Stub tuners are used to match the amplifier input impedance, so that only one variable at a time need be considered. Initially it may be necessary to operate the transistor at reduced collector voltage and power output to avoid excessive stress. When maximum efficiency is obtained, the stub tuner is removed and the input network adjusted for minimum input VSWR.

Now let's design an impedance-matching circuit

Let's consider a practical example of a procedure for the design of impedance-matching circuitry. The sample circuit uses a TRW 2N5596 at 700 MHz as the active device.

Specifications for the completed amplifier are:

$$Z_{in} = 50\ \Omega,$$
$$Z_{out} = 50\ \Omega,$$
$$P_{out} = 20\ W,$$
$$G_p = 7\ dB,$$
$$\eta = 55\%\ \text{minimum.}$$

Specifications for the TRW 2N5596 are:

$$P_{out} = 20\ W \text{ at } 1\ GHz,$$
$$\eta = 55\%\ \text{minimum at } 1\ GHz,$$
$$G_p = 5\ dB\ \text{minimum at } 1\ GHz,$$
$$Z_{in} = 2.5 + J4.0 \text{ at } 700\ MHz,$$
$$Z_{out} = 6.0 - J12.5 \text{ at } 700\ MHz.$$

In practice, the gain of a common-emitter amplifier decreases at a rate of 4 to 5 dB per octave. The 2N5596 at 700 MHz produces about 7 dB of gain. Therefore approximately 4 W of drive will be required to produce 20 W of output power. The collector efficiency can be expected to increase at the lower frequency, but it is difficult to estimate because it is a complex phenomenon. Manufacturers' curves of typical behavior are useful. Output power will not increase significantly with the decreased frequency.

The efficiency-frequency relationship depends on device f_T and ballasting. Heavily ballasted transistors tend to give increased efficiency as frequency is decreased. However, they level out at a lower efficiency than a nonballasted part because of I^2R losses in ballast resistors. The average increase in efficiency as a result of decreasing frequency is about 20% per octave. Values from 10 to 40% per octave have been measured.

The initial phase of the design is best accomplished on an immittance chart. The chart with appropriate values indicated for the sample design is shown in Fig. 3. The input match is achieved when the input impedance is resonated with a capacitive susceptance of 0.18 mhos. This susceptance is realized by use of a pair of capacitive microstrip stubs. Each stub must exhibit a reactance of 2 × 1/0.18 mhos, or 11.1 Ω. The length of the stub may be calculated by

$$\tan\theta = \frac{Z_o}{X_c}.$$

For ease of adjustment, the length of the stubs should be less than 60 degrees. Because capacitive reactance is a tangential function, the reactive variations per unit length become increasingly severe past 60 degrees. It is better to decrease Z_o rather than to use longer stubs to achieve higher capacitance. Therefore $Z_o \leqq 1.732\ X_c \leqq 19.24\ \Omega$. Because it is easier to shorten a microstrip stub than to lengthen it, the Z_o of 15 Ω, for example, provides sufficient adjustment range to accommodate device variations.

The next step is to transform the resonated impedance to 50 Ω. This is accomplished by a series-transmission line with a characteristic impedance of 50 Ω. From Fig. 3, we see that the length of this line can be directly determined to be 0.062 wavelengths, or 22.3 degrees, long. A capacitive susceptance of 0.040 mhos completes the transformation. Again, a pair of capacitive stubs will provide the susceptance. For ease of converting the design to microstrip dimensions, it is convenient to choose a Z_o for the second stub that is equal to that selected for the first. Therefore:

$$\tan\theta = \frac{Z_o}{X_c} = \frac{15}{50} = 0.3,$$
$$\text{or } \theta = 16.7 \text{ degrees.}$$

In this case the length chosen is 20 degrees to allow for some adjustment.

The output match is achieved by partial resonating of the device's output impedance with an inductive susceptance. While the amount of susceptance chosen is arbitrary at this point, the output network bandwidth is affected by the value. From Fig. 3, we can determine that 0.05 mhos is required for the first matching element. This susceptance is achieved by use of a shorted microstrip stub. The length of the stub may be calculated from the equation

$$\tan\theta = \frac{X_L}{Z_o}.$$

If Z_o of the stub is arbitrarily chosen to be 50 Ω,

$$\tan\theta = \frac{20}{50} = 0.4,$$
$$\theta = 21.8 \text{ degrees.}$$

Again, the stub is made somewhat longer because it can be adjusted by *sliding* the chip capacitor (ac short) up or down the line length. The remaining transformation is achieved by a 50-Ω series-transmission line of 0.15 wavelengths (54 degrees long) and a capacitive susceptance of 0.014 mhos. Selecting a pair of 50-ohm microstrip lines to provide the susceptance requires a stub length of

$$X_c = 2 \times \frac{1}{0.014} = 143\ \Omega.$$

$$\tan = \frac{Z_o}{X_c} = \frac{50}{143} = 0.350 = 19.3 \text{ degrees.}$$

A stub length of 25 degrees will provide an adequate allowance for adjustment of the circuit. ■■

THREE BALUN DESIGNS FOR PUSH-PULL AMPLIFIERS

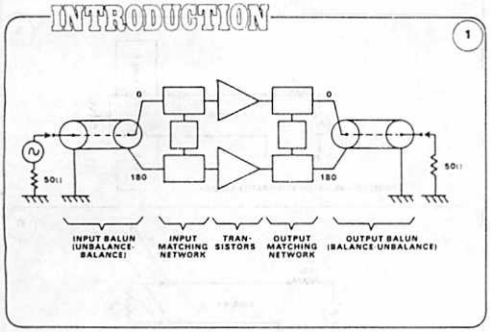
SINGLE RF power transistors seldom satisfy today's design criteria; several devices in separate packages[1] or in the same package (balanced, push-pull or dual transistors), must be coupled to obtain the required amplifier output power. Since high-power transistors have very low impedance, designers are challenged to match combined devices to a load. They often choose the push-pull technique because it allows the input and output impedances of transistors to be connected in series for RF operation.

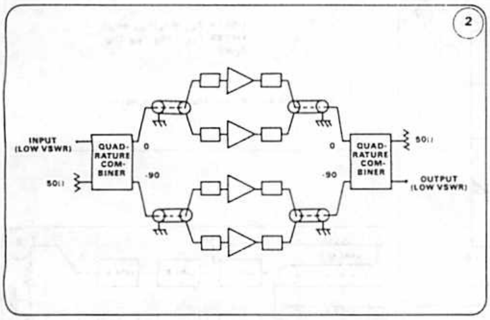
Balun-transformers provide the key to push-pull design, but they have not been as conspicuous in microwave circuits as at lower frequencies. Ferrite baluns[2] have been applied up to 30 MHz; others incorporating coaxial transmission lines operate in the 30-to-400-MHz range.[3]

The success of these two balun types should prompt the microwave designer to ask if balun-transformers can be included in circuits for frequencies above 400 MHz. Theory and experimental results lead to the emphatic answer: yes! Not only will baluns function at microwave frequencies, but a special balun can be designed in microstrip form that avoids the inherent connection problems of coax.

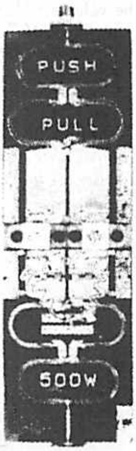
On the next six pages, you will observe the development of three balun-transformers—culminating with the microstrip version. None of the baluns was tuned nor were the parasitic elements compensated. In this way, the deviation of the experimental baluns from their theoretical performance could be evaluated more easily. The frequency limitations imposed by the parasitic elements also were observed more clearly.

INTRODUCTION





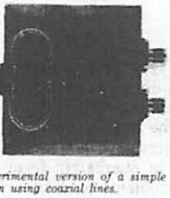
1. A balun transforms a balanced system that is symmetrical (with respect to ground) to an unbalanced system with one side grounded. Without balun-transformers, the minimum device impedance (real) that can be matched to 50 ohms with acceptable bandwidth and loss is approximately 0.5 ohms. The key to increasing the transistors' output power is reducing this impedance ratio. Although 3-dB hybrid combiners can double the maximum power output, they lower the matching ratio to only 50:1. Balun transformers can reduce the original 100:1 ratio to 6.25:1 or less. The design offers other advantages: the baluns and associated matching circuits have greater bandwidth, lower losses, and reduced even-harmonic levels.



A 500-W push-pull amplifier for DME band.

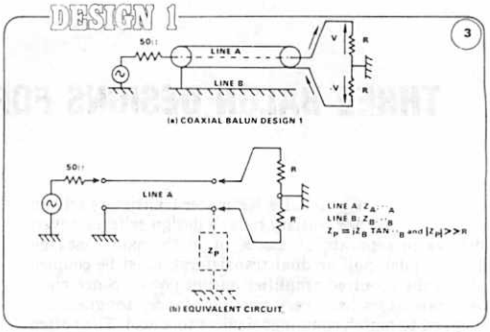
2. Baluns are not free of disadvantages. Coupling a pair of push-pull amplifiers with 3-dB hybrids avoids (for four-transistor circuits) one of these: the higher broadband VSWRs of balun-transformers. A second disadvantage, the lack of isolation between the two transistors in each push-pull configuration, is outweighed by the advantages of the balun design in reducing the critical impedance ratio.

3. In this simple balun that uses a coaxial transmission line, the grounded outer conductor makes an unbalanced termination, and the floating end makes a balanced termination. Charge conservation requires that the currents on the center and the outer conductors maintain equal magnitudes and a 180-degree phase relationship at any point along the line. By properly choosing the length and characteristic impedance, this balun can be designed to match devices to their loads. In the case shown, if $\theta_A = 90$ degrees, the matching condition is:

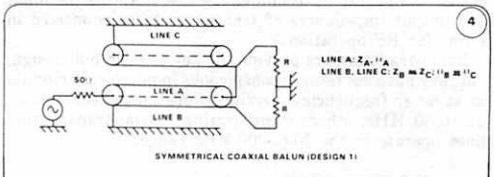


Experimental version of a simple balun using coaxial lines.

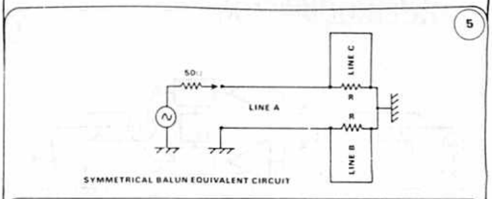
$$Z_A^2 = 2xRx50.$$



4. By adding a second coaxial line, the basic balun can be made perfectly symmetrical. In this symmetrical coaxial balun, the bandwidth (in terms of the input VSWR) is limited by the transformation ratio, 50/2R, and the leakages, which are represented by lines B and C. If Z_A = 50 ohms and R = 25 ohms, the bandwidth is constrained only by the leakages.

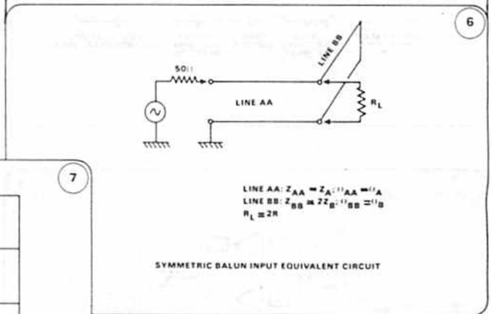


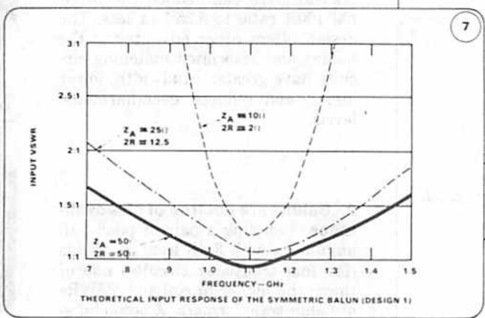
5. The equivalent circuit for the symmetrical balun shows the effect of the leakages (lines B and C) on its performance. A broadband balun can be obtained by using a relatively high characteristic impedance for these leakage lines. In theory, the construction of the baluns insures perfect balance.



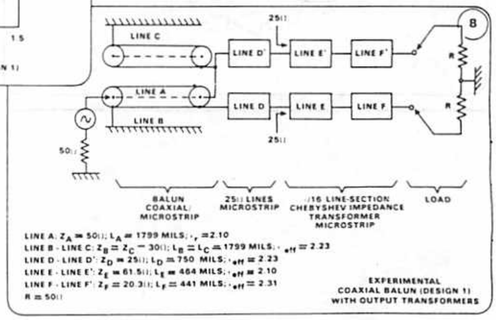
6. The symmetric balun's input equivalent circuit further simplifies its configuration and allows the input VSWR to be calculated.[4] In this design, line A has a characteristic impedance of Z_A=50 ohms, a length of L_A=1799 mils, and a dielectric constant (relative) of ϵ_r=2.10. For lines B and C, Z_o=30 ohms, L=1799 mils, and ϵ_{eff}=2.23.

L=1799

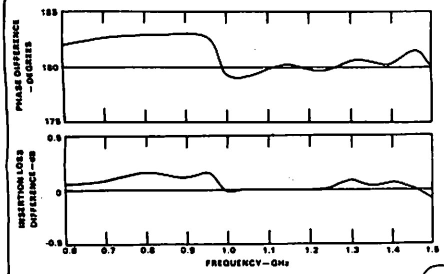




7. The theoretical input VSWR has been calculated for 50-ohm values of Z_A and 2R, and for two other sets of values for these parameters. The performance of an experimental balun will be compared with these theoretical results.



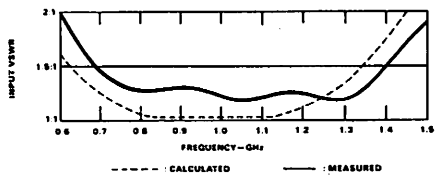
8. Two λ/16 line-section Chebyshev impedance transformers match the experimental balun to a 50-ohm measurement system. The balun was tested from 0.6 to 1.5 GHz.



DESIGN 1 BALUN MEASURED PERFORMANCE

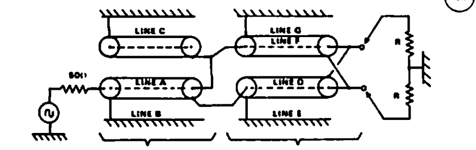
9. The measured phase difference and insertion loss difference, which indicate the maximum unbalance for the Design 1 experimental balun, are 3 degrees and 0.2 dB, respectively.

10. The maximum VSWR measured for the first design is 1.5:1. Note the comparison between the calculated and measured response. The performance shown can be considered valid for amplifier applications up to an octave range.



DESIGN 1 BALUN PERFORMANCE

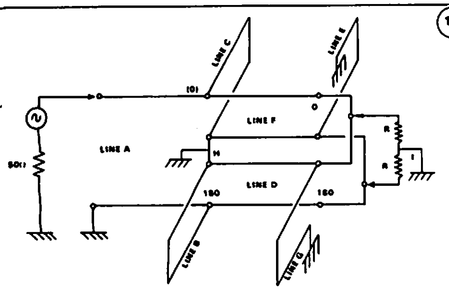
DESIGN 2



LINE B AND LINE C: IDENTICAL LINE D AND LINE F: IDENTICAL LINE E AND LINE G: IDENTICAL

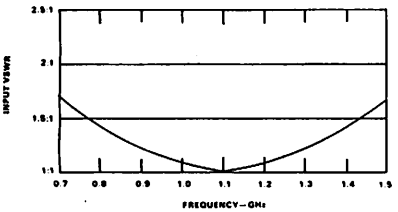
COAXIAL BALUN DESIGN 2

11. The second balun design adds two identical coax lines to the simple balun just described. The inputs of the identical lines are connected in series to the output of the first balun. By putting their outputs in parallel, the final output becomes symmetrical. The output impedance is halved.



DESIGN 2 BALUN EQUIVALENT CIRCUIT

12. The equivalent circuit for the Design 2 balun indicates that its bandwidth, in terms of input VSWR, is limited by the transformation ratios of the first and second sections and the leakages represented by lines B, C, E, and G. If the balun is designed with Z_A = 50 ohms, and $Z_D = Z_F$ = 25 ohms, and if the load, 2R, is set at 2×6.25 ohms, all of the transmission lines will be connected to their characteristic impedances. In this case, the bandwidth will be limited by the leakage alone, and a broadband balun can be obtained by choosing lines B, C, E, and G with relatively high impedance and $\lambda/4$ length for the center frequency. The balun achieves a transformation from 50 ohms to twice 6.25 ohms without causing a standing wave in the coaxial cables.

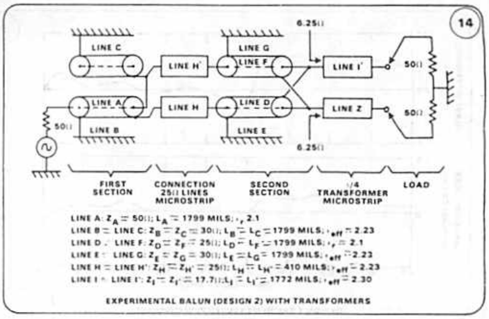


THEORETICAL INPUT RESPONSE OF THE COAXIAL BALUN (DESIGN 2)

13. The performance of the Design 2 balun can be calculated using its equivalent circuit. The calculated VSWR shows a response very close to the simple coaxial balun (Fig. 10) because the new second section has four times the bandwidth of the first section. This design and its two companions are intended to have octave bandwidths centered at 1.1 GHz, the central frequency used in distance measuring equipment (DME, 1.025 to 1.150 GHz) and tactical air navigation (TACAN, 0.960 to 1.215 GHz). For line A: Z_A = 50 ohms, L_A = 1799 mils, ϵ_r = 2.10; lines B, C, E, and G: Z_o = 30 ohms, L = 1799 mils, ϵ_{eff} = 2.23; lines E and F: Z_o = 25 ohms, L = 1799 mils, ϵ_r = 2.10.

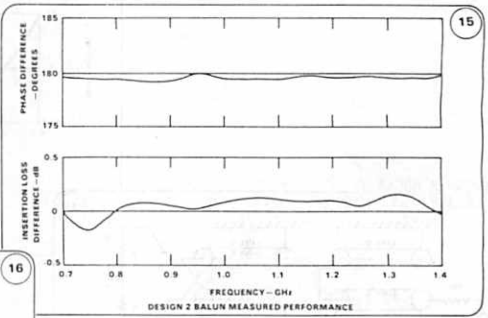
Two-section balun often used in the 100-to-400 MHz range.

14. Two λ/4 transformers match the experimental two-section coaxial balun's 6.26-ohm impedance to the 50-ohm load. Although these transformers drastically reduce the bandwidth (in terms of the VSWR), they don't affect the balance.



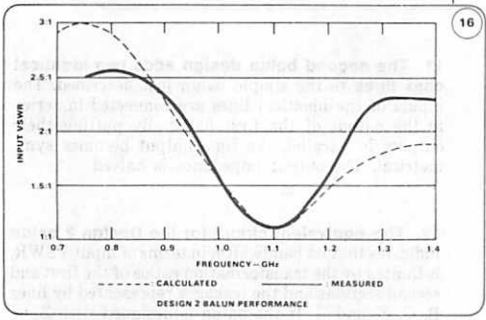
EXPERIMENTAL BALUN (DESIGN 2) WITH TRANSFORMERS

15. The measured phase difference and measured insertion loss difference are plotted for the two-section coaxial balun (Design 2). The maximum unbalances for these two measurements over the octave bandwidth are 1 degree and 0.2 dB.



DESIGN 2 BALUN MEASURED PERFORMANCE

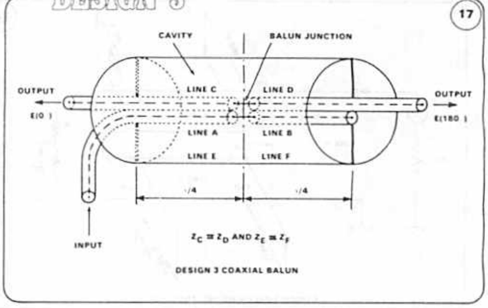
16. The calculated and measured values for the input VSWR for the Design 2 balun show close agreement between the experimental and predicted performances. This indicates that the parasitic inductors at the connections are negligible to at least 1.4 GHz. Moreover, the balun has excellent balance to 1.4 GHz and achieves the 4:1 transformation without causing a standing wave in the coaxial line. Despite the many excellent qualities of the Design 1 and Design 2 baluns, the necessary coaxial line connection limits them to approximately 2 GHz.



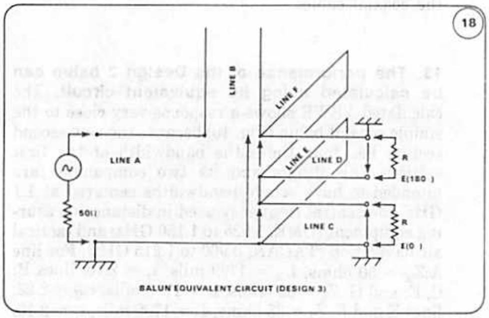
DESIGN 2 BALUN PERFORMANCE

17. The problems associated with the previous coaxial baluns can be reduced or eliminated by using a balun that allows a microstrip coplanar arrangement of the input and output lines, which greatly simplifies the connections to the amplifier. This balun[5] consists of an input line, A, connected in series to three elements in the center of the half-wavelength cavity: a reactive open-circuit stub, B, and the λ/4 output lines, C and D.

DESIGN 3



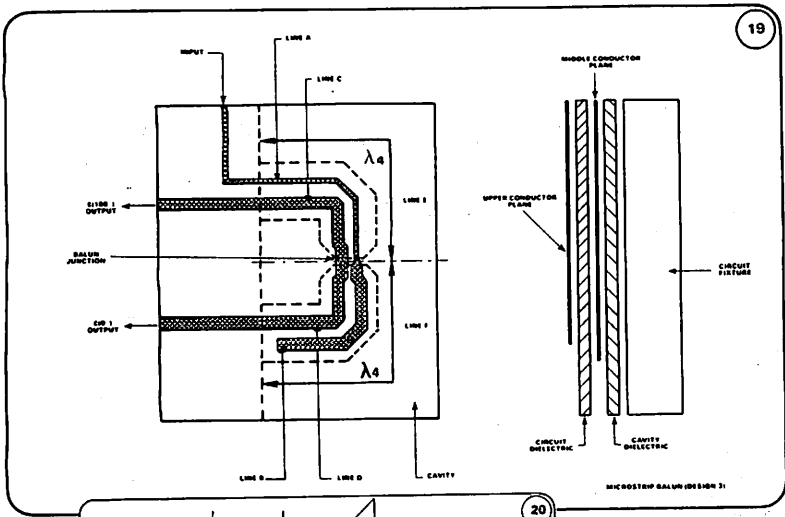
DESIGN 3 COAXIAL BALUN

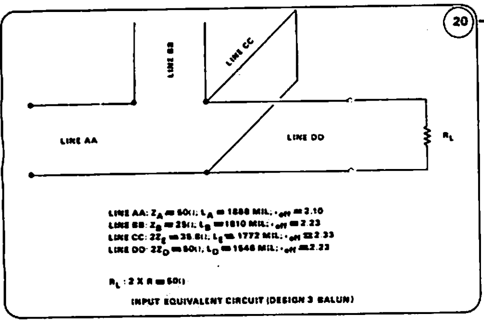


BALUN EQUIVALENT CIRCUIT (DESIGN 3)

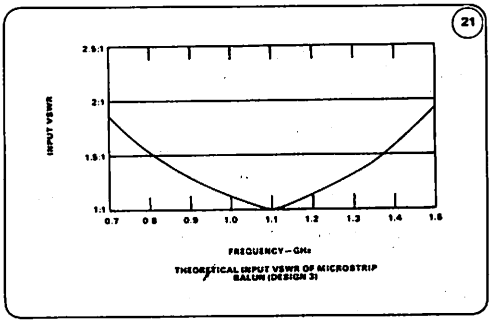
18. The equivalent circuit of the Design 3 coaxial version balun shows lines C and D connected to place their input signals in antiphase, thereby producing two antiphase signals at their outputs. Transmission line impedances and lengths are optimized to achieve the correct input/output transformation ratio and a good match across the desired bandwidth. If only one frequency or a narrow bandwidth is desired, and all lengths are λ/4, the matching condition $Z_A^2/50 = 2Z_C^2/R$, will occur. In this case, Z_E ($Z_E = Z_F$) and Z_B have no significance except for loss.

19. The coplanar arrangement of input and output lines can be accomplished with microstrip technology. The uppermost conductor plane contains input line A, output lines C and D, and the open stub B. Coupling between these lines is avoided by separating them by at least one line width. The middle conductor carries the ground plane for the lines. To avoid radiation loss, the center conductor must extend at least one line width to either side of the upper plane circuit line. The balun resonant cavity is formed by the region between the middle and the lower conductor planes. A hole for the cavity is cut in the circuit fixture, filled with dielectric, and covered with the middle conductor plane. The end-to-end length of the cavity is nominally a half-wavelength at midband. To avoid disturbance of the field distribution, the cavity width must be at least three times the width of the middle conductor plane. The arms of the balun cavity are folded to produce two parallel and proximate output transmission lines. This configuration is more suited to coupling two transistors than the original layout in which the two outputs were on opposite sides (Fig. 17).





20. The input equivalent circuit for the microstrip version of the Design 3 balun allows its theoretical performance to be calculated. The design parameters shown provide a microstrip circuit that can be compared with the coaxial baluns of Design 1 and Design 2. Transmission line A and lines C and D are loaded by their characteristic impedances—in this case, 50 and 25 ohms. The cavity and the stub impose the principal frequency limitation. The impedances of these elements are dictated by the properties of the available dielectric substrates (glass-Teflon 0.020 and 0.0625 inches thick).



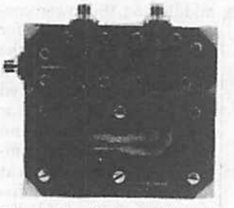
References

1. "35/50 Watt Broadband (160-240 MHz) Push-Pull TV Amplifier Band III," TRW Application Note, TRW RF Semiconductors Catalog No. 97, p. 84AN.
2. "150 W Linear Amplifier 2 to 28 MHz, 13.5 Volt DC," TRW Application Note, TRW RF Semiconductors Catalog No. 97, p. 108AN.
3. TRW Application Notes on the TPM-4100 (100 W, 100 - 400 MHz); the TPM-4040 (40 W, 100 - 400 MHz); the TPV-3100 (110 W, Band III); and the TPV-5050 (50 W, UHF), available from TRW RF Semiconductors.
4. The program used for the circuit calculation was COMPACT (Computerized Optimization of Microwave Passive and Active Circuits).
5. Gordon J. Laughlin, "New Impedance-Matched Wideband Balun and Magic Tee," *IEEE Transactions: Microwave Theory and Technology*, Vol. MTT-24, No. 3, (March 1976).

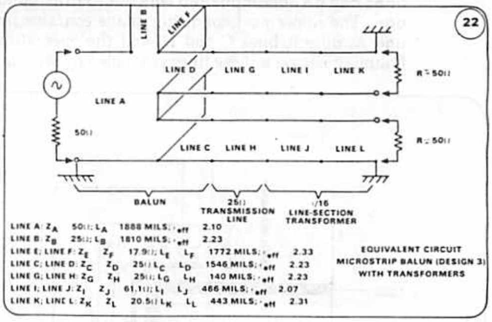
21. The input VSWR can be calculated based on the equivalent circuit for the microstrip balun. For a one-octave bandwidth, the input VSWR is lower than 1.75:1. This calculated performance is similar to that of the two previous balun designs. The design of the microstrip has theoretically perfect balance.

7

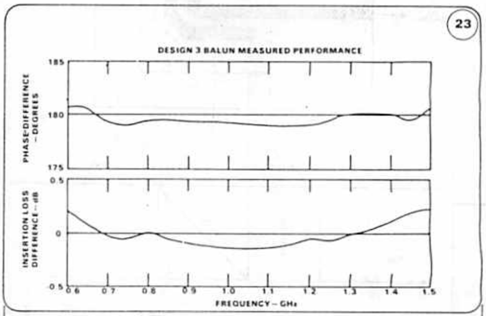
22. The equivalent circuit of the microstrip balun shows it during performance measurements with $\lambda/16$ matching lines. The experimental model uses 18-mil glass-Teflon (ϵ_r = 2.55) for the tap circuits and 62.5 mil glass-Teflon for the cavity. Balance properties were measured with a 50-ohm system, which was transformed to 25 ohms by the $\lambda/16$ line-section Chebyshev impedance transformers, which have a bandwidth from 0.960 to 1.215 GHz.



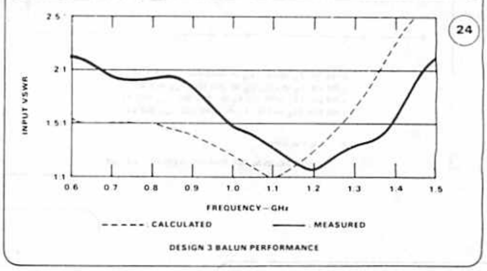
The experimental microstrip balun showing the uppermost conductor plane.



23. The unbalance between output ports for a one-octave bandwidth is shown in the measured 1.5-degree maximum phase difference and 0.15-dB maximum insertion loss difference.



24. The central frequency is 10 percent higher than expected, but response is close to the calculated values if relative frequency is considered. If the output transformers and their effect on input VSWR are disregarded, an octave bandwidth with a maximum input VSWR of around 2.0:1 can be obtained. The 100-MHz shift between the two curves may be caused by the improper determination of the folded cavity's electrical length. Similar calculation inaccuracies may arise from effects at the balun junction and from the electrical length of the stub. As in the calculated response, the experimental microstrip balun performs comparably to the two coaxial designs.



25. The similarity in the performance of the three balun designs within the considered frequency bands indicates that the parasitic elements do not significantly affect the theoretical properties. The frequency limit is higher than 1.5 GHz for all three. In the 0.960-to-1.215-GHz bandwidth (TACAN and DME applications), each performed with satisfactory balance. The table compares the main characteristics of the balun designs.

The phase differences ($\pm$1.5 degrees) for all three baluns are similar to those experienced with the miniature 3-dB hybrid couplers that are normally used to combine transistors for microwave balanced amplifiers. But the insertion loss differences of the baluns are better—0.2 dB for a one-octave bandwidth compared with 0.5 dB.

The physically simple microstrip balun eliminates the connection problem inherent in coaxial designs: physical variances that breed standing waves and unbalance. Microstripping the transmission lines allows a designer to choose any value of characteristic impedance of the lines. Consequently, the microstrip balun is both more manageable and more controllable.

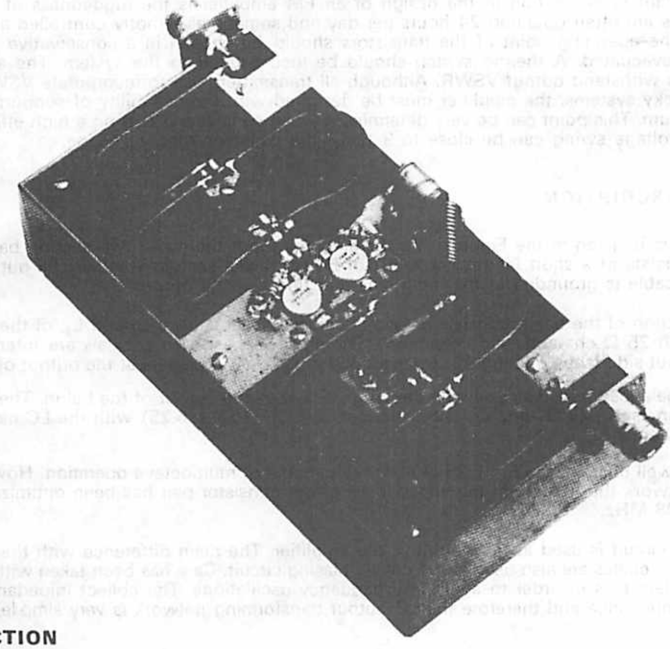
Since the balun load impedance will vary with frequency, the best results will be obtained by simultaneously optimizing the balun parameters with those of the matching network. The transistor's internal prematching network must be considered.••

SUMMARY

Performance of the Three Balun Designs

Type of balun	Balun loads, R (ohms)	Maximum experimental unbalance for one-octave bandwidth		Theoretical input VSWR for:	
		$\Delta\phi$(°)	ΔMAG (dB)	960-1215 MHz	One-octave bandwidth
Coaxial I (Design 1)	25	3	0.2	1.15:1	1.6:1
Coaxial II (Design 2)	6.25	1	0.2	1.15:1	1.6:1
Microstrip (Design 3)	25	1.5	0.2	1.20:1	1.8:1

SOLID STATE POWER AMPLIFIER
300 W FM
88–108 MHz



INTRODUCTION

High efficiency multikilowat FM transmitters with full solid state amplifiers are possible today. The power amplifier of these transmitters should be made by multiparalleling of a basic building block amplifier. This building block should have a high output power and a high gain, a good collector efficiency, broad-band (88-108 MHz) frequency response and a simple, reproducible and reliable circuit design. This application note describes an FM building block amplifier that meets the requirements mentioned above and that can be successfully incorporated to a number of amplifier architectures.

The amplifier has been developed with a pair of TP 9383 transistors in push-pull configuration. TP 9383 is a double diffused silicon epitaxial transistor that makes use of gold metallization and diffused ballast resistors for long operationg life and ruggedness. Its basic specifications are :

V_{CC} = 28 V ; η = 75 % at 108 MHz and 150 W output power

G = 9 dB   Po = 150 W

DESIGN CONSIDERATIONS

When designing an FM amplifier the total efficiency must be the first goal.

Overall efficiency is the combination of good collect efficiency and high gain. To get a good collector efficiency the transistors must be operated in class C and the load impedance should match the transistors output impedance at the operation power level. Class C amplifiers are non-linear units. The harmonic content of the output signal of this type of amplifiers can be very high and their power wasted with an important reduction in the efficiency.

This fact made advantageous the use of balanced amplifiers. In such circuit arrangement all the even harmonic are largely suppressed and the waste of power minimized. Push-pull amplifiers have also the additional advantages of connecting in series for RF operation the input and output impedance of the 2 transistors. That makes considerably easier to match the input and output impedances of the transistor pair. However, as the impedance transformation is lower, the RF power losses are smaller and the gain and efficiency higher.

Another important consideration in the design of an FM amplifier is the ruggedness of the amplifier. FM transmitters are often operated 24 hours per day and sometimes remotly controlled and in difficult access sites. The operating point of the transistors should be chosen in a conservative way and the heat properly evacuated. A thermo switch should be incorporated to the system. The amplifier must also be able to withstand output VSWR. Although all transmitters use to incorporate VSWR protection in their interlocky systems, the amplifier must be designed with the capability of supporting VSWR of 3.1 as a minimum. This point can be very determinent when considering that on a high efficiency circuit the collector voltage swing can be close to 3 times the collector supply voltage.

CIRCUIT DESCRIPTION

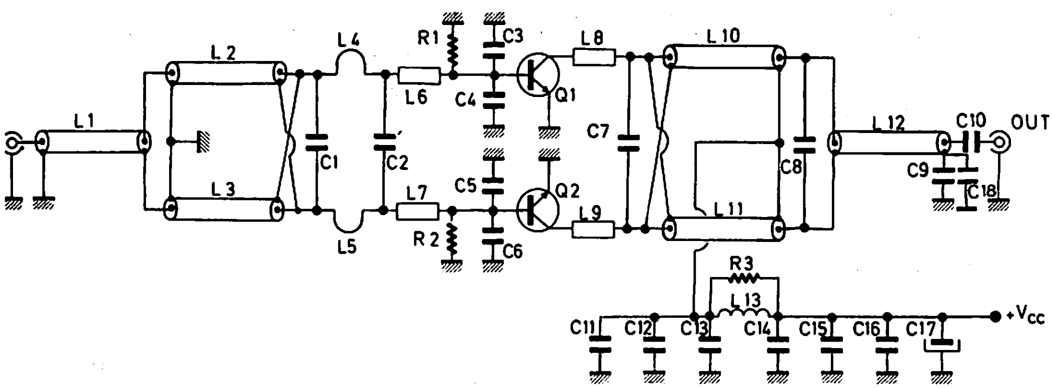
Circuit schematic is given in the Figure 1. At the amplifier input there is a two section balun. The first section, L_1, consists of a short lenght ($\simeq \lambda/20$) of 50 Ω coaxial semirigid cable. The outer conductor of the coaxial cable is grounded at the input side and floats at the output.

The second section of the balun consists of two identical coaxial cables, L_2 and L_3, of the same length that L_1 but with 25 Ω characteristic impedance. The ends of these two coaxials are interconnected in series at the input side (thus offering 50 Ω impedance to L_1) and in parallel at the output of the section.

The combined balanced impedance will be therefore 12.5 Ω at the output of the balun. The input impedance of the transistor pair Q_1 and Q_2 is transformed to 12.5 Ω (2 × 6.25) with the LC network represented in the schematic.

If this balun is well charged by 2 × 6.25 Ω it is well capable of multioctave operation. However in this case the LC network that transform the impedances of the transistor pair has been optimized only between 88 and 108 MHz.

A similar balun circuit is used at the output of the amplifier. The main difference with the input balun is that the coaxial cables are also used in the collect biasing circuit. Care has been taken with the decoupling of the collect bias in order to avoid low frequency oscillations. The collect impedance is higher than the base impedance and therefore the LC output transforming network is very simp le, only L_8, L_9 and C_7.



88-108 MHz; 300 W 28 V

Figure 1. FM Broadband Power Amplifier

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COMPONENTS LIST

C_1	= 120 + 80 pF Chip capacitor ATC 100 B
C_2	= 220 pF Chip capacitor ATC 100 B
C_3, C_4, C_5, C_6	= 470 pF Chip capacitor ATC 100 B
C_7	= 100 pF Chip capacitor ATC 100 B
C_8	= 27 pF Chip capacitor ATC 100 B
C_9, C_{10}, C_{11}, C_{14}	= 1 000 pF Disc capacitor
C_{12}, C_{15}	= 10 nF
C_{13}, C_{16}, C_{18}	= 0,1 µF
C_{17}	= 1 000 µF/63 V Electrolytic

L_1	= 50 Ω coaxial cable ⌀ 3,2 mm (Teflon) L = 110 mm
L_2, L_3	= 25 Ω coaxial cable ⌀ 3,2 mm (Teflon) L = 110 mm
L_4 L_5	= Hair pin : copper foil 18 × 3 mm 0,3 mm thickness
L_6, L_7	= Line on substrate : 15 × 5 mm
L_8, L_9	= Line on substrate : 10 × 5 mm
L_{10}, L_{11}	= 25 Ω coaxial cable ⌀ 5 mm (Teflon) L = 110 mm
L_{12}	= 50 Ω coaxial cable ⌀ 5 mm (Teflon) L = 110 mm
L_{13}	= 15 turns ⌀ 8 mm 1,4 mm wire

R_1, R_2	= 22 Ω 1/2 W
R_3	= 47 Ω 2 W

Q_1, Q_2	= TP 9383

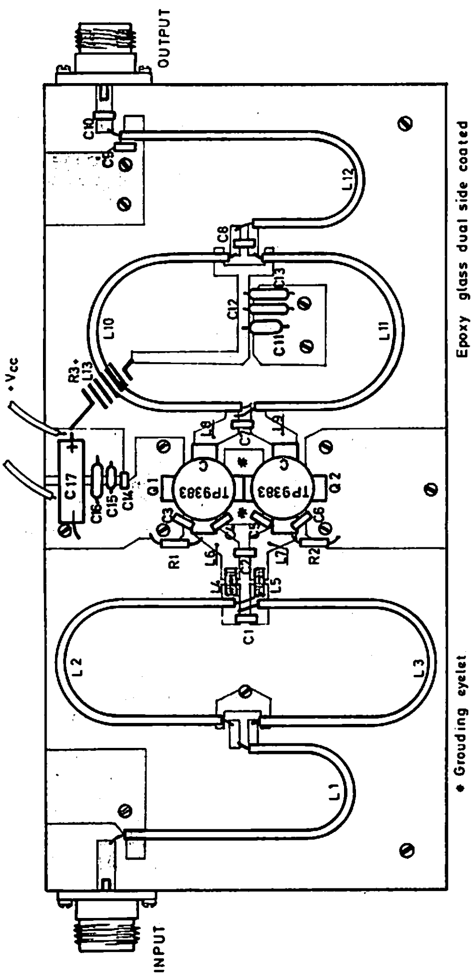

Figure 2. Component Layout

300 W PUSH-PULL FM TP 9383

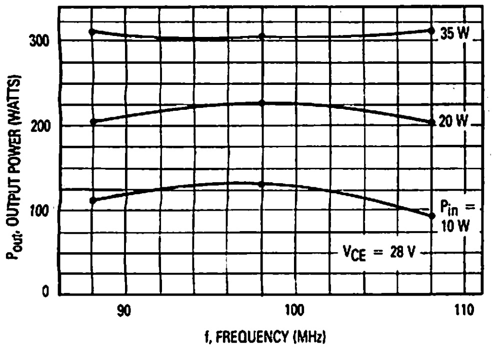

Figure 3. Output Power versus Input Power and Frequency

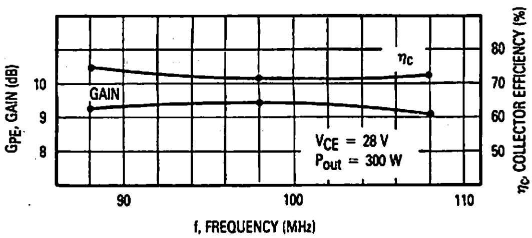

Figure 4. Gain and Efficiency versus Frequency

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1.2 V, 40–900 MHz BROADBAND AMPLIFIER WITH THE TP 3400 TRANSISTOR

INTRODUCTION

This application note describes a single stage broadband amplifier incorporating the TP 3400 transistor. The amplifier will deliver 1.2 V output signal from 40 to 900 MHz at an intermodulation level* of — 60 dB or less. The gain is 9.5 dB ± 0.5 dB. Although the amplifier has been designed for MATV use, its simplicity and versatility makes it suitable for use in many other applications. The circuit construction is straight forward and only standard components have been used.

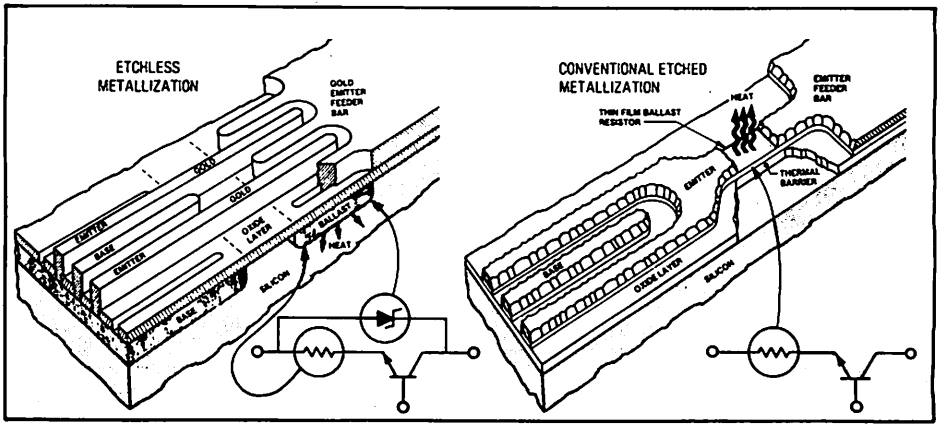
TP 3400

The TP 3400 is a NPN gold metallized transistor with a transition frequency of more than 3 GHz. The transistor is housed in a SOE 200 package.

The gold metallization process used on the manufacture of this transistor is etchless, providing exact finger definition with submicron resolution and avoids the finger scalloping characteristic of all etching processes, which eliminates therefore current crowding where metal fingers are necked down. Moreover this gold process improves on all the benefits of gold over aluminium regarding electromigration.

The TP 3400 also incorporates diffused ballast resistors. High resistance ballast resistors are diffused directly into the silicon avoiding therefore all the reliability problem associated with conventional thin film, metal ballast resistors. In addition the P-N diode of the ballast resistor is diffused to avalanche at a lower voltage than the transistor, thus protecting effectively the transistor against VSWR or transient damage. A diagram illustrating the above mentioned technological characteristic is given in fig. 1.

DIFFUSED BALLAST RESISTORS WITH ETCHLESS GOLD METALLIZATION VS. **CONVENTIONAL THIN FILM BALLAST RESISTORS WITH ETCHED METALLIZATION**



(*) Intermodulation measured with a test procedure in accordance with DIN 45004/B.

Figure 1. Types of Ballast Resistors

AMPLIFIER DESIGN

a) Calculations

The amplifier configuration chosen is given in figure 2. A combination of series and shunt feedback compensates the frequency gain slope of the transistor. Transmission line inductors are used on the shunt feedback network. The resistor in series with the base will improve the input VSWR at the cost of some gain, but this gain decrease is partially compensated by the fact that less series feed-back is necessary in this way.

The calculation and optimization of the circuit was carried out with the aid of a computer using the COMPACT program. The program, the optimization data and the final expected results are given in table. 1. The expected gain is 9.5 dB plus/minus 0.5 dB, the amplifier is unconditionally stable over the required frequency range and input and output impedance matchings could be considered correct.

b) Amplifier assembly

Final amplifier is shown in fig. 3. The component values are given in table 2. The amplifier was built on standard Epoxy glass double clad printed circuit board and all the components are commonly used types. The resistors are carbon-composition type. Care was taken with all ground returns, made by wrapping copper foil between both planes. Plated trough holes may also be used. PC board and component layouts are given in figures 4 and 5 respectively.

RESULTS

Several TP 3400 transistors, covering all the accepted production spread, were used and no significant differences in the amplifier performance were recorded.

Input and output matching are given in figures 6 and 7. Gain versus frequency is given in figure 8. It is similar to that calculated.

Figure 9 shows its behabiour as an MATV amplifier, measured according to the DIN 45004B test procedure. The — 60 dB IMD level is attained at 1.2 volt, 75 output.

INTERMODULATION MEASUREMENT ACCORDING DIN 45004/B

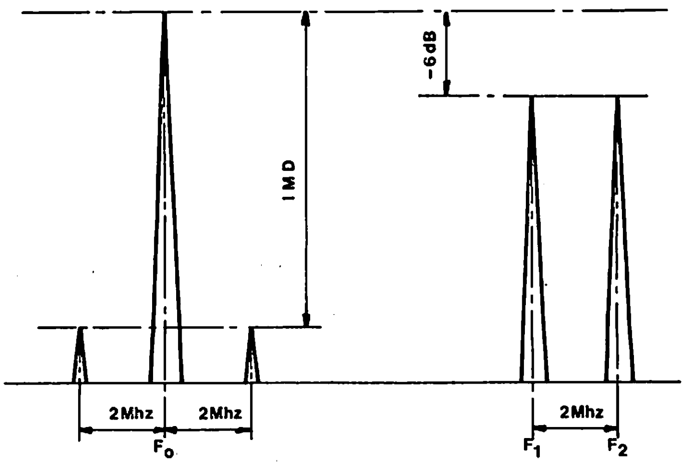


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Table 1. Compact Program

CIRCUIT DEFINITION

```
MET  AA  ZZ
CAP  AA  PA  —2.078
TRL  BB  SE   65.00   —19.96   1.000
RES  CC  SE  —12.44
TRL  DD  SE   65.00   —18.35   1.000
CAP  EE  PA  —2.101
TWO  HH  SI   50.00
CAS  EE  HH
RES  II  PA  —6.759
SER  EE  II
CAP  JJ  PA  —.8989
SRL  KK  PA   35.00    1000.
TRL  LL  SE   65.00   —10.15   1.000
CAX  JJ  LL
CAS  EE  JJ
RES  MM  SE  —204.7
TRL  NN  SE   65.00   —7.229   1.000
CAS  MM  NN
PAR  EE  MM
TRL  FF  SE   65.00   —14.60   1.000
CAP  GG  PA  —.9557
CAX  AA  GG
PRI  AA  SI   50.00
END
```

FREQUENCY (MHz)

```
100  200  300  400  500  600  700  800  900
END
```

POLAR S PARAMETERS FOR TWO HH (TP 3400)

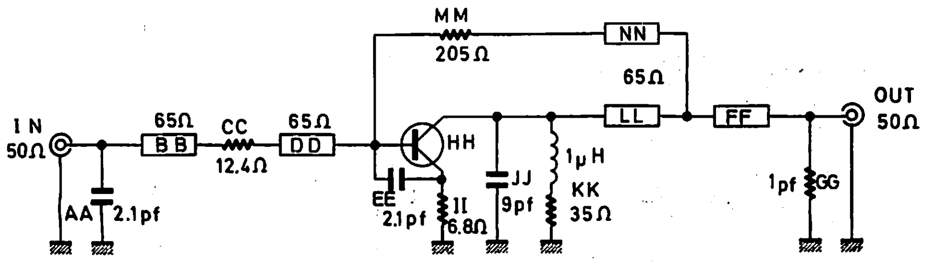
```
.61  226  17.8  126  .0200  35  .53  320
.73  203  12.9  103  .0282  33  .32  305
.77  192  9.23   93  .0299  33  .27  297
.75  185  6.92   84  .0335  33  .27  295
.75  179  5.15   79  .0335  38  .27  300
.78  174  4.68   72  .0355  42  .24  300
.77  167  3.34   61  .0447  44  .27  285
.77  163  3.16   56  .0473  44  .24  290
END
```

OPTIMIZATION DATA

```
.5
10  10  1  10
END
```

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN	ANGL)	S21 (MAGN	ANGL)	S12 (MAGN	ANGL)	S22 (MAGN	ANGL)	S21 dB	K FACT.
100.00	0.09	—132	2.99	157.1	0.139	—10.7	0.16	149	9.52	1.38
200.00	0.11	—140	3.14	135.2	0.139	—21.5	0.16	141	9.94	1.33
300.00	0.13	—152	3.13	113.4	0.136	—32.7	0.11	128	9.91	1.36
400.00	0.15	—166	3.14	89.7	0.133	—43.6	0.03	86	9.94	1.38
500.00	0.15	166	2.94	64.2	0.128	—53.5	0.07	— 52	9.37	1.49
600.00	0.15	140	3.15	43.9	0.126	—63.6	0.10	— 68	9.96	1.42
700.00	0.15	99	3.18	20.0	0.127	—72.3	0.16	— 99	10.05	1.37
800.00	0.20	51	2.95	— 6.8	0.128	—80.8	0.25	—120	9.38	1.34
900.00	0.26	18	3.06	—29.3	0.128	—93.0	0.25	—125	9.78	1.22



$9.4 \leqslant G \leqslant 10.1$ dB INPUT VSWR $\leqslant$ 1.8 : 1
OUTPUT VSWR $\leqslant$ 1.7 : 1

Figure 2. TP 3400 Amplifier 40–900 MHz

Table 2. List of Components

C_1	= capacitor ceramic 2.8 pF 632 RTC
C_2	= capacitor chip 10 nF Eurofarad
C_3	= capacitor chip 8.2 pF Vitramon
C_4	= capacitor chip 2.2 pF Vitramon
C_5, C_7	= capacitor chip 1 nF Eurofarad
C_6, C_8	= capacitor chip 10 nF Eurofarad
C_9	= capacitor chip 22 pF Vitramon
C_{10}	= capacitor chip 10 nF Eurofarad
C_{11}	= capacitor electrolytic 25 MF 25 V
L_1	= 8 turns 5/10 mm Cu ID 2.5 mm
L_2	= printed 5 nH
L_3	= printed stripline 75 ohms 11.5 mm
L_4	= printed stripline 75 ohms 11 mm
L_5	= printed stripline 75 ohms 25 mm
F_1	= ferrite bead 1200082 TRW
R_1	= resistor 12 ohms 1/4 W carbon composition
R_2	= resistor 4.7 ohms 1/4 W carbon composition
R_3, R_4	= resistor 10 ohms 1/4 W carbon composition
R_5	= resistor 8.2 kohms 1/4 W carbon composition
R_6	= resistor 240 ohms 1/4 W carbon composition
R_7	= resistor 12 ohms 1/2 W carbon composition
T	= transistor TP 3400

Board Material

Epoxy glass (G 10) 1/16 inch $E_R = 4.2$

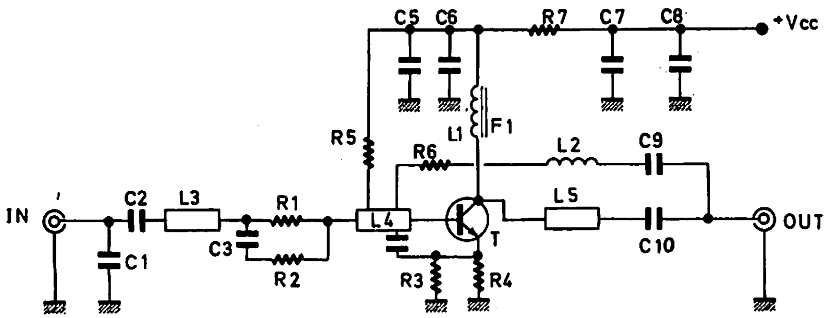


Figure 3. Circuit Schematic

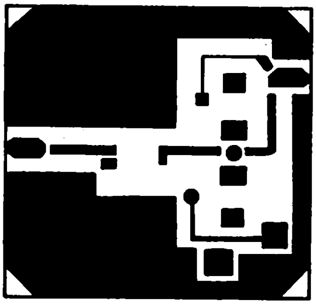


Figure 4. PC Board Layout (Not to Scale)

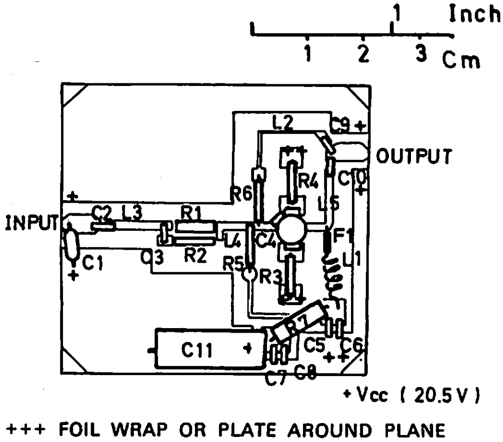


Figure 5. Component Layout

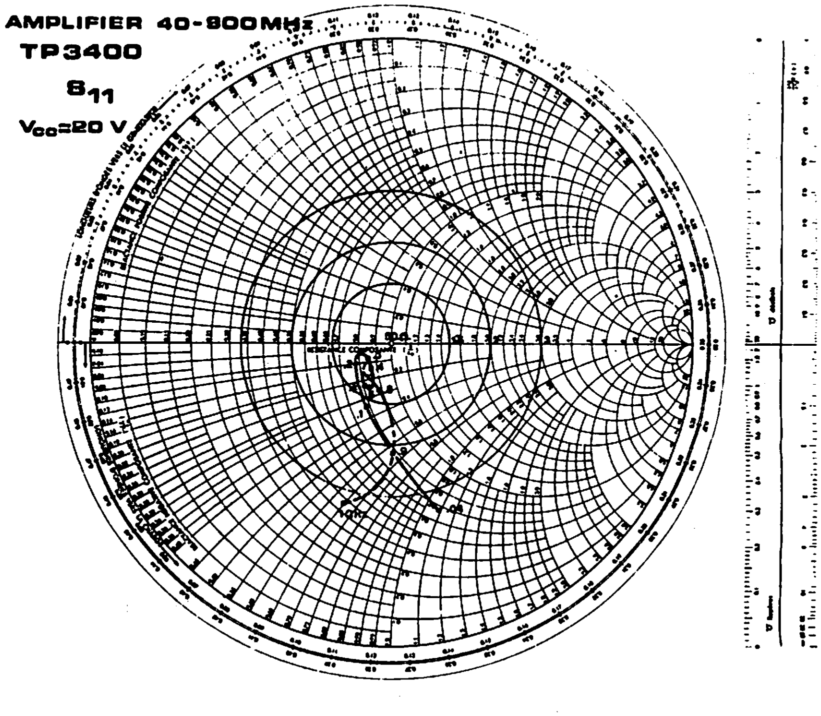


Figure 6. S_{11} versus Frequency

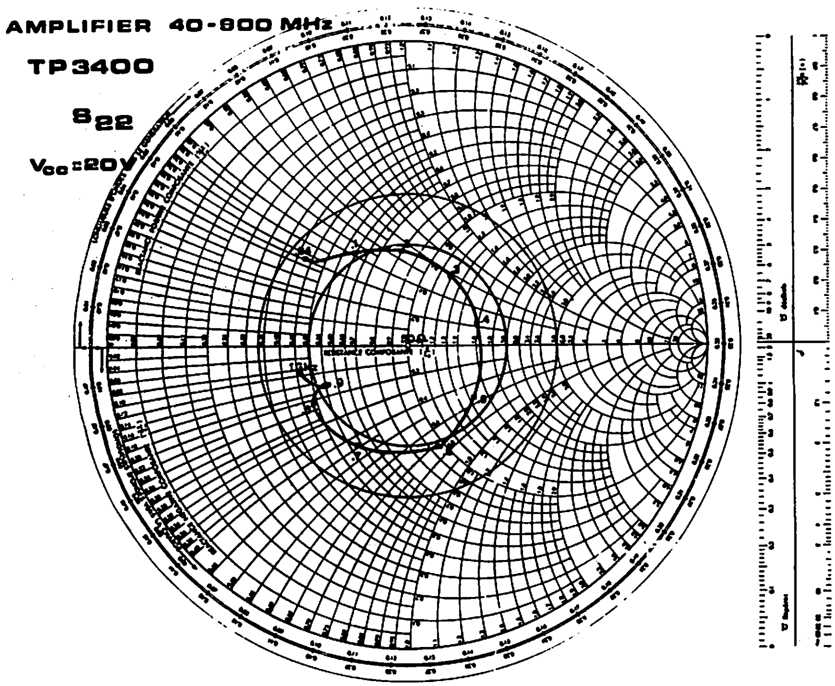


Figure 7. S_{22} versus Frequency

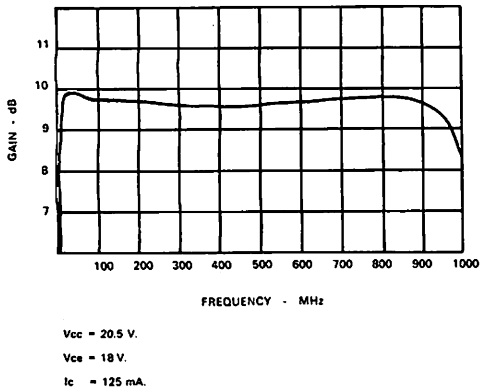


Figure 8. Gain versus Frequency

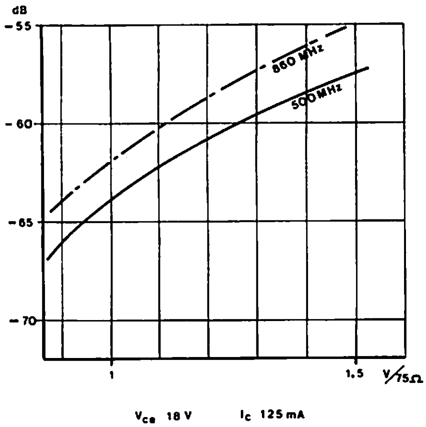
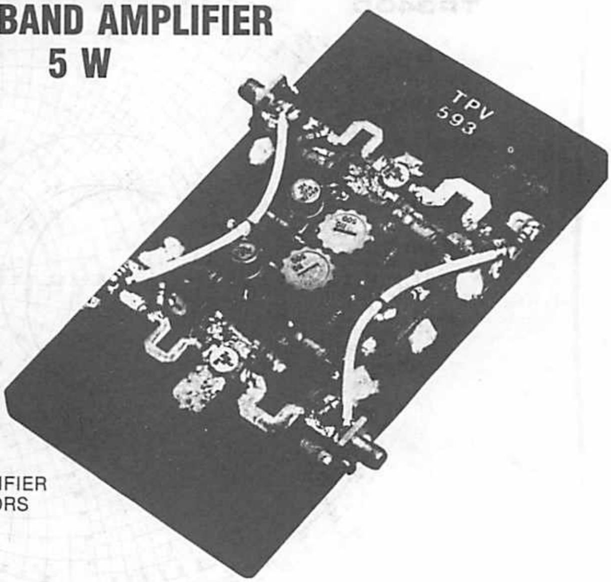


Figure 9. IMD (Din 45004 B) versus Output Voltage

470–860 MHz BROADBAND AMPLIFIER 5 W



5 W UHF TV TRANSPOSER AMPLIFIER
WITH TWO TPV 593 TRANSISTORS

INTRODUCTION

This application note describes an ultralinear broadband (470-860 MHz) amplifier, developed for TV transposer applications. The amplifier incorporates two TPV 593 transistors.

Each transistor is used to build a separate broadband amplifier. The two identical amplifiers are later combined with 3 dB hybrids.

The TPV 593 transistor has been developed for TV class A application. It incorporates gold metallization and diffused ballast resistors for ruggedness and linearity. Its DC current consumption is very low and makes it a good candidate for solar cell powered systems. Its basic specifications are :

V_{CC} = 25 V $\qquad$ I_C = 450 mA

G = 9 dB at 860 MHz

IMD = — 60 dB at 860 MHz and 2 W output

The S parameters of the TPV 593 are given in the table below.

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN	ANGL)	S21 (MAGN	ANGL)	S12 (MAGN	ANGL)	S22 (MAGN	ANGL)	S21 dB	K FACT·
470.00	0.93	170	1.50	63.0	0.040	50.0	0.55	— 166	3.52	1.01
650.00	0.93	165	1.06	50.0	0.050	54.0	0.60	— 169	0.51	1.04
860.00	0.92	162	0.79	38.0	0.056	54.0	0.65	— 169	— 2.00	1.15

POLAR COORDINATES OF SIMULTANEOUS CONJUGATE MATCH

F MHz	SOURCE REFL. COEFF. MAGN.	ANGLE	LOAD REFL. COEFF. MAGN.	ANGLE	Gmax dB
470.0	0.99	−173	0.91	124	15.23
650.0	0.97	−168	0.83	134	12.01
860.0	0.95	−165	0.79	146	9.16

DESIGN CONSIDERATIONS

Two identical single transistor class A amplifiers will be combined with 3 dB couplers. First the design of a single amplifier will be considered.

From the analysis of the variation of the TPV 593 S21 parameter with the frequency it may be seen that there is a difference of 5.52 dB between 470 and 860 MHz. If a flat gain is required this gain slope has to be compensated. The compensation can be implemented in two ways :

a) By placing a selective attenuator at the input of the transistor amplifier, with an insertion loss minimum at 860 MHz and which increases to 5.52 dB at 470 MHz. The insertion loss increase should compensate the transistor gain slope.

b) By selective mismatch at the input of the transistor. The input circuit will provide impedance matching at 860 MHz, in order to get a gain as close as possible to the GA max. Frequency dependent mismatch will compensate the gain slope. At 470 MHz a VSWR as high as 11:1 will be necessary. It has been proved that impedance mismatch at the base terminal of a transistor power amplifier does not modify the linearity behavior of the device.

As it was decided to combine two amplifiers with 3 dB couplers the method b) was selected. 50 ohms 3 dB hybrid couplers when used with two identical loads provide a good VSWR at the common terminal even if the loads differ from 50 ohms. The reflected energy is dissipated as the 50 ohms load connected to the fourth terminal of the coupler. The coupler behaves as a selective attenuator. Figure 1 shows the amplifier arrangement. The use of a 3 dB coupler to split the input signal makes almost compulsory the use of the same type of circuit at the output.

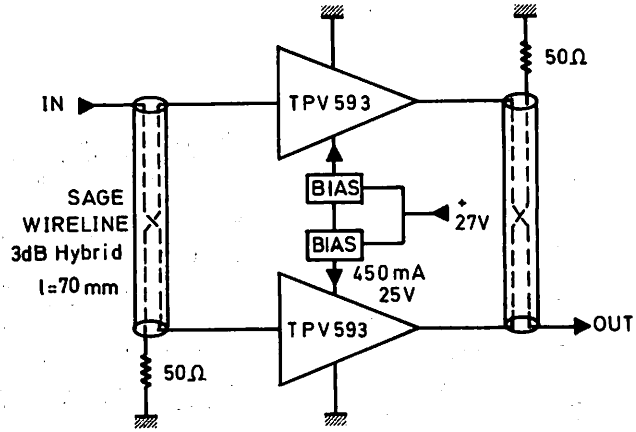


Figure 1. Block Diagram of Amplifier

The amplifier must be as linear as possible over the complete UHF band. A transistor power amplifier usually requires impedance matching at the collector side for optimum intermodulation. Therefore the output circuitry has been designed for impedance matching all over the bands IV and V.

COMPONENTS PART LIST

L_1 = 65 line 11 % g at 860 MHz
L_2 = 50 line 1.5 % g at 860 MHz
L_3 = 50 line 17 % g at 860 MHz
L_4 = 7 turns ID 2 mm - Closely Wound - wire 5 mm
L_5 = 10 mm : 5 mm wire 1 mm

C_1-C_5 = Variable Airtronic AT 7275, .8-4.5 pF
C_2 = 6.8 pF ATC 100A
C_3-C_4 = 10 pF ATC 100A
C_6-C_7 = 1 nF + 10 nF + 1μ + 10 μF

Board Material: 1/16" Teflon Fiberglass

CIRCUIT DESCRIPTION

The circuit of a simple amplifier is given in Figure 2.

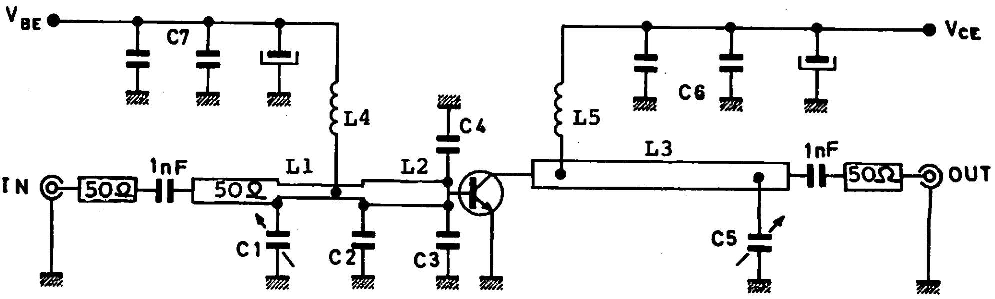


Figure 2. Circuit Schematic

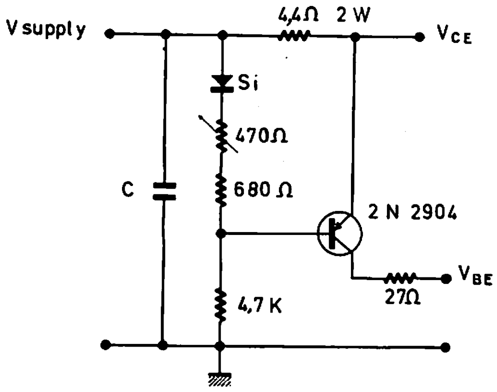


Figure 3. Class A Bias Circuit

The input circuit consist of a three section low pass type matching network. To minimize power losses all the impedance transformations are made at a low Q level. Variable capacitor C_1 is adjusted for optimum VSWR at 860 MHz. The tuning is straight forward and only a small retouch is necessary after the collector tuning.

The very constant S22 of the TPV 593 transistor makes extremely simple to match the collector to a 50 ohms load. L_8 tunes the output capacitance of the device and is determined for good matching at the low end of the band. Only one low pass section is necessary. Capacitor C_5, variable, allows a good shaping of the output VSWR. Collector tuning should be done after tuning the input.

The bias control circuitry is classical and is given in Figure 3.

CONSTRUCTIONAL DETAILS

The printed circuit board lay-out of the complete amplifier is given in Figure 4. Considerate attention should be paid to the ground returns. Plated through holes have been used to ensure low emitter inductance. Wrapped foils ensure proper grounding of parallel capacitors and connectors.

The couplers have been made with parallel wire cable.

This solution is as inexpensive as a straight forward.

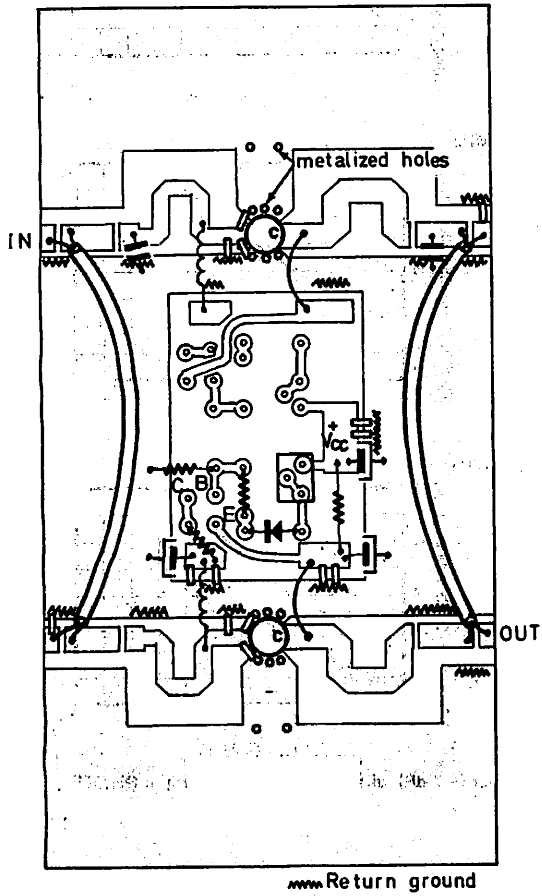


Figure 4. Printed Circuit Board Layout

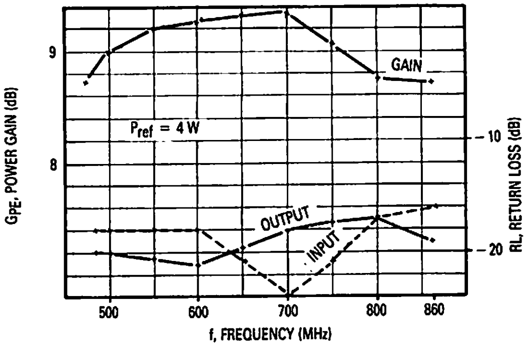


Figure 5. Gain and Return Loss versus Frequency

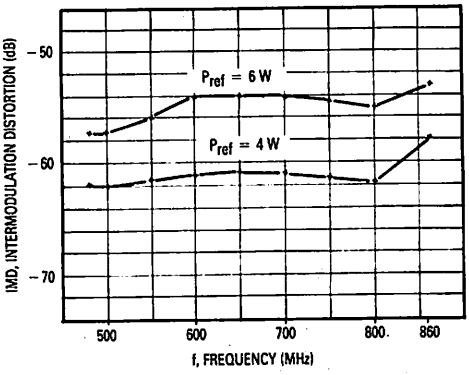


Figure 6. Intermodulation Distortion versus Frequency

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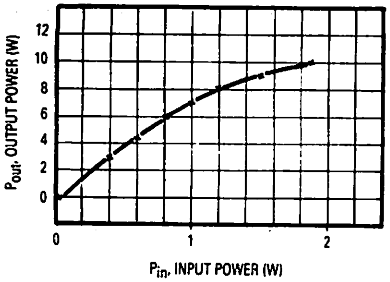
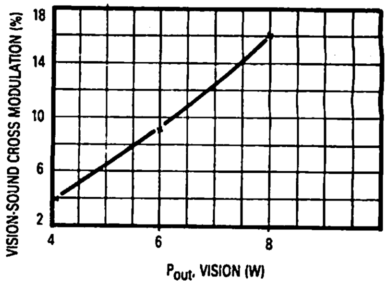
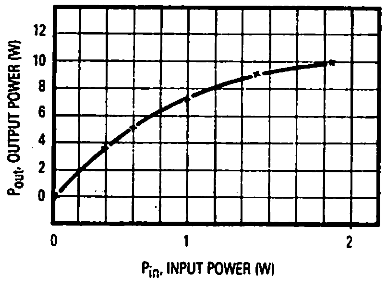
Figure 7. Output Power versus Input Power | **Figure 8. Vision to Sound Cross Modulation**

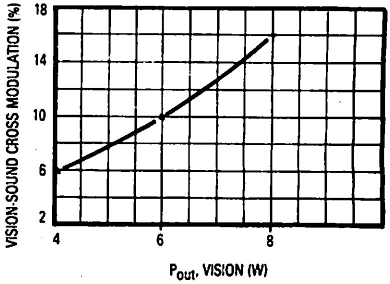
f = 470 MHz



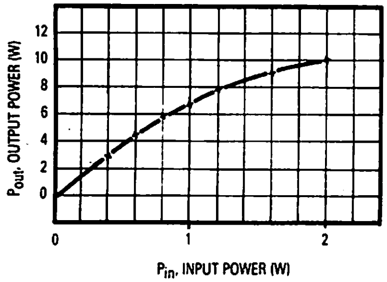


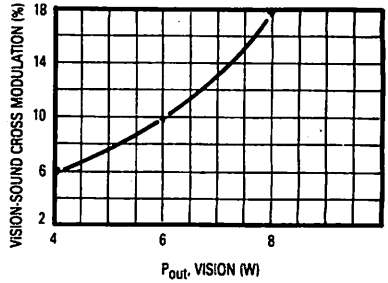
f = 650 MHz





f = 860 MHz





NOTE: Δ% of sound carrier (−7 dB) when vision carrier is switch ON/OFF

MEASUREMENTS

The measurements results have been summarized in Table 2.

Figure 5 shows the frequency response of the amplifier as well as the input and output match. Figure 6 displays the linearity (IMD test; −8, −16, −7 dB) of the amplifier. Static transfer curves are given in the Figures 7 and 8 that show also the vision to sound cross modulation of the amplifier.

Table 2

TYPICAL RESULTS

BANDWIDTH	: 470 - 860 MHz	* IMD :	SOUND	= REF. — 7 dB
GAIN	: 8.7 dB min.		VISION	= REF. — 8 dB
IMD* at — 4 W	: — 58 dB		SIDEBAND	= REF. — 16 dB
— 5 W	: — 56 dB			
INPUT RETURN LOSS	: — 16 dB			
OUTPUT RETURN LOSS	: — 17 dB			
BIAS CONDITIONS	: V_{CE} = 25 V ; I_C = 2 × 450 mA			

CONCLUSION

A high performance amplifier has been described as an example of the possibilities offered to the designer by the TPV 593. In particular the amplifier combines excellent frequency response and linearity with high efficient use of the DC power. This circuit may be of interest for output stages of low power TV transposers or drivers of higher power units.

AN1040

Mounting Considerations for Power Semiconductors

Prepared by Bill Roehr
Staff Consultant, Motorola Semiconductor Sector

TABLE OF CONTENTS

INTRODUCTION

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one-half for a decrease in junction temperature from 160°C to 135°C.(1) Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.(2) Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic-packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

(1) MIL-HANDBOOK — 217B, SECTION 2.2.
(2) "Navy Power Supply Reliability — Design and Manufacturing Guidelines" NAVMAT P4855-1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.

Figure 1 shows an example of doing nearly everything wrong. A tab mount TO-220 package is shown being used as a replacement for a TO-213AA (TO-66) part which was socket mounted. To use the socket, the leads are bent — an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet-metal screw through a 1/4″ hole containing a fiber-insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.

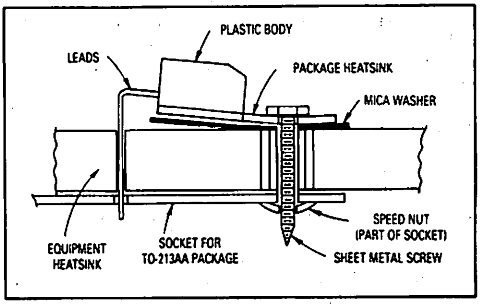


Figure 1. Extreme Case of Improperly Mounting A Semiconductor (Distortion Exaggerated)

In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc-over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

Stud Mount
Flange Mount
Pressfit
Plastic Body Mount
Tab Mount
Surface Mount

Appendix A contains a brief review of thermal resistance concepts. Appendix B discusses measurement difficulties with interface thermal resistance tests. Appendix C indicates the type of accessories supplied by a number of manufacturers.

MOUNTING SURFACE PREPARATION

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high-power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e. Δh/TIR, if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory; a finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy using a copper TO-204 (TO-3) package with a typical 32-microinch finish, showed that heatsink finishes between 16 and 64 μ-in caused less than ±2.5% difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.[3] Most commercially available cast or extruded heatsinks will require spotfacing when used in high-power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

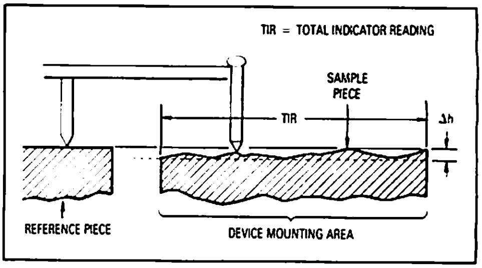


Figure 2. Surface Flatness Measurement

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO-3, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat-dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine-edge blanking or sheared-through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four-post die sets equipped with proper pressure pads and holding fixtures.

(3) Catalog #87-HS-9 (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381-0839.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black-anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromate-acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 volts.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

INTERFACE DECISIONS

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pock-marked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section.

To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic-encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

The silicone oil used in most greases has been found to evaporate from hot surfaces with time and become deposited on other cooler surfaces. Consequently, manufacturers must determine whether a microscopically thin coating of silicone oil on the entire assembly will pose any problems. It may be necessary to enclose components using grease. The newer synthetic base greases show far less tendency to migrate or creep than those made with a silicone oil base. However, their currently observed working temperature range are less, they are slightly poorer on thermal conductivity and dielectric strength and their cost is higher.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil, a dry graphite compound, is shown in the data of Figure 3. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from Aavid is called KON-DUX. It is made with a unique, grain oriented, flake-like structure (patent pending). Highly compressible, it becomes

Table 1
Approximate Values for Interface Thermal Resistance Data from Measurements Performed in Motorola Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data			Interface Thermal Resistance (°C/W)					
JEDEC Outlines	Description	Test Torque In-Lb	Metal-to-Metal		With Insulator			See Note
			Dry	Lubed	Dry	Lubed	Type	
DO-203AA, TO-210AA TO-208AB	10-32 Stud 7/16" Hex	15	0.3	0.2	1.6	0.8	3 mil Mica	
DO-203AB, TO-210AC TO-208	1/4-28 Stud 11/16" Hex	25	0.2	0.1	0.8	0.6	5 mil Mica	
DO-208AA	Pressfit, 1/2"	—	0.15	0.1	—	—	—	
TO-204AA (TO-3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO-213AA (TO-66)	Diamond Flange	6	1.5	0.5	2.3	0.9	2 mil Mica	
TO-126	Thermopad 1/4" x 3/8"	6	2.0	1.3	4.3	3.3	2 mil Mica	
TO-220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figures 3 and 4 for additional data on TO-3 and TO-220 packages.
2. Screw not insulated. See Figure 12.

formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

INSULATION CONSIDERATIONS

Since most power semiconductors use are vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non-isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Newer packages, such as the Motorola Full Pak and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal-to-metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO-204 (TO-3) and TO-220 packages, are shown in Figure 3, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case).

Referring to Figure 3, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraided, as the dust is highly toxic.) Thermafilm is a filled polyimide material which is used for isolation (variation of Kapton). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high breakdown voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease.

Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut-through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By

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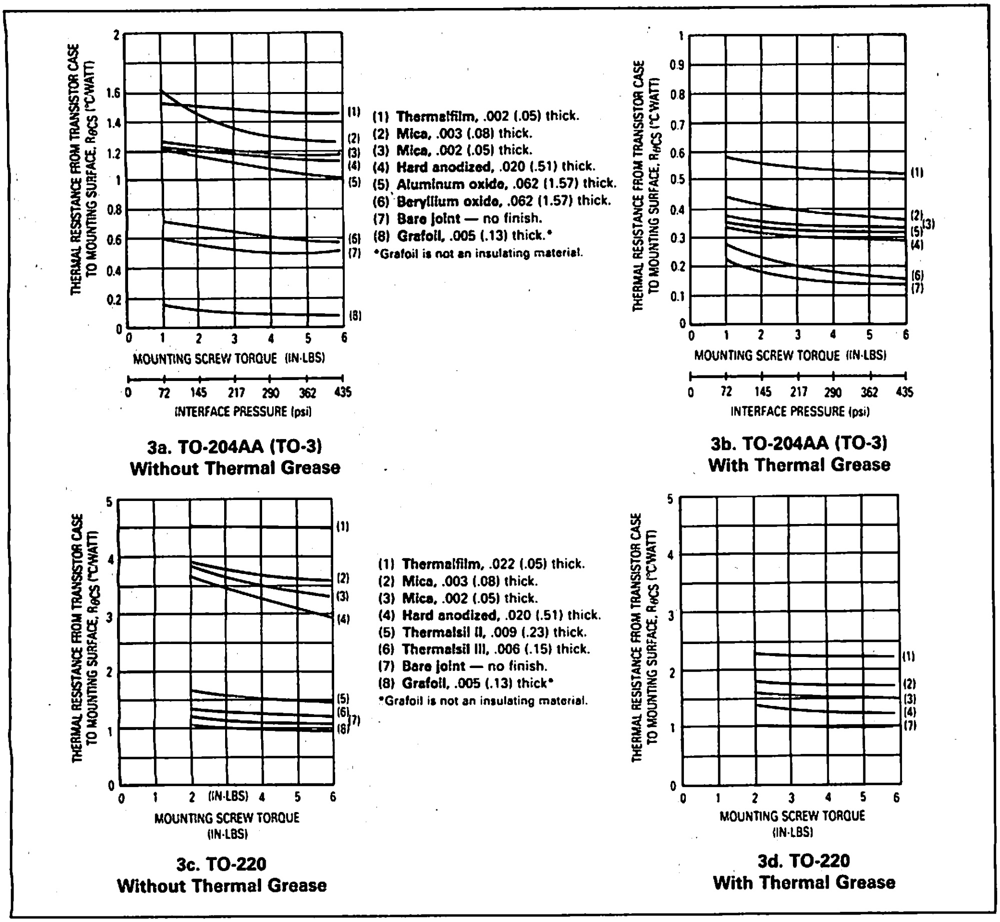

Figure 3. Interface Thermal Resistance for TO-204, TO-3 and TO-220 Packages using Different Insulating Materials as a Function of Mounting Screw Torque (Data Courtesy Thermalloy)

comparing Figures 3c and 3d, it can be noted that Thermasil, a filled silicone rubber, without grease, has about the same interface thermal resistance as greased mica *for the TO-220 package.*

A number of manufacturers offer silicone rubber insulators. Table 2 shows measured performance of a number of these insulators under carefully controlled, nearly *identical* conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out-of-flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K-10 pad, for example, is described as having about 2/3 the interface resistance of the Sil Pad 1000 which would place its performance close to the Chomerics 1671 pad. AAVID also offers an isolated pad called

Table 2. Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	$R_{\theta CS}$ @ 3 Mils*	$R_{\theta CS}$ @ 7.5 Mils*
Wakefield	Delta Pad 173-7	.790	1.175
Bergquist	Sil Pad K-4	.752	1.470
Stockwell Rubber	1867	.742	1.015
Bergquist	Sil Pad 400-9	.735	1.205
Thermalloy	Thermalsil II	.680	1.045
Shin-Etsu	TC-30AG	.664	1.260
Bergquist	Sil Pad 400-7	.633	1.060
Chomerics	1674	.592	1.190
Wakefield	Delta Pad 174-9	.574	.765
Bergquist	Sil Pad 1000	.529	.935
Ablestik	Thermal Wafers	.500	.990
Thermalloy	Thermalsil III	.440	1.035
Chomerics	1671	.367	.655

*Test Fixture Deviation from flat from Thermalloy EIR86-1010.

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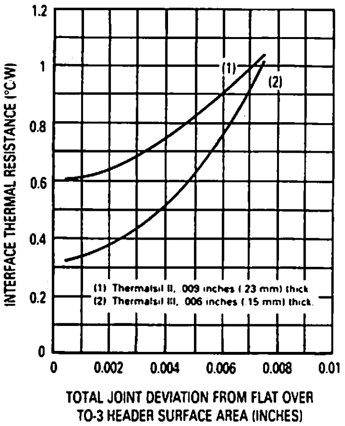
Rubber-Duc, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from AAVID shows $R_{\theta CS}$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO-204AA (TO-3) package insulated with Thermasil is shown on Figure 4. Observe that the "worst case" encountered (7.5 mils) yields results having about twice the thermal resistance of the "typical case" (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.



Data courtesy of Thermalloy

Figure 4. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho-Therm 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R_{\theta CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in-lb from an initial 6 in-lb. With nonconformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly; so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi-pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost-effective insulated packages since the 1950's. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The EMS (Energy Management Series) Modules, *shown on Figure* 8, Case 806 (ICePAK) and Case 388A (TO-258AA) (see Figure 11) are examples of parts in this category. The second category contains parts which have a plastic overmold covering the metal mounting base. The *Full Pak,*

Table 3. Performance of Silicon Rubber Insulators Tested per MIL-I-49456

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data(1)	Berquist Data(2)
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	—
Cho-Therm, 1617	0.233	—
Q Pad (non-insulated)	—	0.009
Sil-Pad, K-10	0.263	0.200
Thermasil III	0.267	—
Mica, greased	0.329	0.400
Sil-Pad 1000	0.400	0.300
Cho-therm 1674	0.433	—
Thermasil II	0.500	—
Sil-Pad 400	0.533	0.440
Sil-Pad K-4	0.583	0.440

(1) From Thermalloy EIR 87-1030
(2) From Berquist Data Sheet

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Case 221C, illustrated in Figure 13, is an example of parts in the second category.

Parts in the first category — those with an exposed metal flange or tab — are mounted the same as their non-insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 5, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection — generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a Sync Nut, the patented device can be soldered to a PC board and the semiconductor mounted with a 6-32 machine screw.(4)

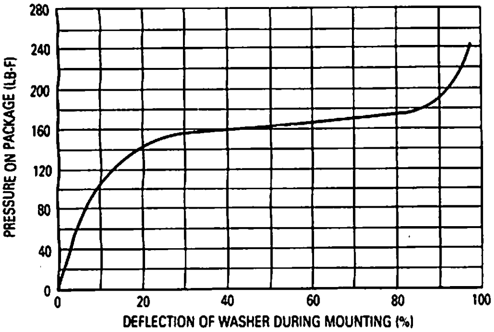


Figure 5. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors

(4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board-mounted or free-standing heat dissipators with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO-220 and TO-126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO-220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or sync-nuts) can form a trouble-free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self-Tapping Screws

Under carefully controlled conditions, sheet-metal screws are acceptable. However, during the tapping-process with a standard screw, a volcano-like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speed-nut. If a self tapping process is desired, the screw type must be used which roll-forms machine screw threads.

Rivets

Rivets are not a recommended fastener for any of the plastic packages. When a rugged metal flange-mount package or EMS module is being mounted directly to a heatsink, rivets can be used provided press-riveting is used. Crimping force must be applied slowly and evenly. Pop-riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional beltfurnace, irons, vapor-phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.[5] Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non-field-servicable systems or low strength types for field-serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

FASTENING TECHNIQUES

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel- or gold-plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper based part is rigidly mounted to an aluminum heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws the semiconductor chip could be damaged. Bending can be minimized by:

1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

Stud Mount

Parts which fall into the stud-mount classification are shown in Figure 6. Mounting errors with non-insulated stud-mounted parts are generally confined to application

(5) Robert Batson, Elliot Fraunglass and James P. Moran, "Heat Dissipation Through Thermalloy Conductive Adhesives," EMTAS '83. Conference, February 1-3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.

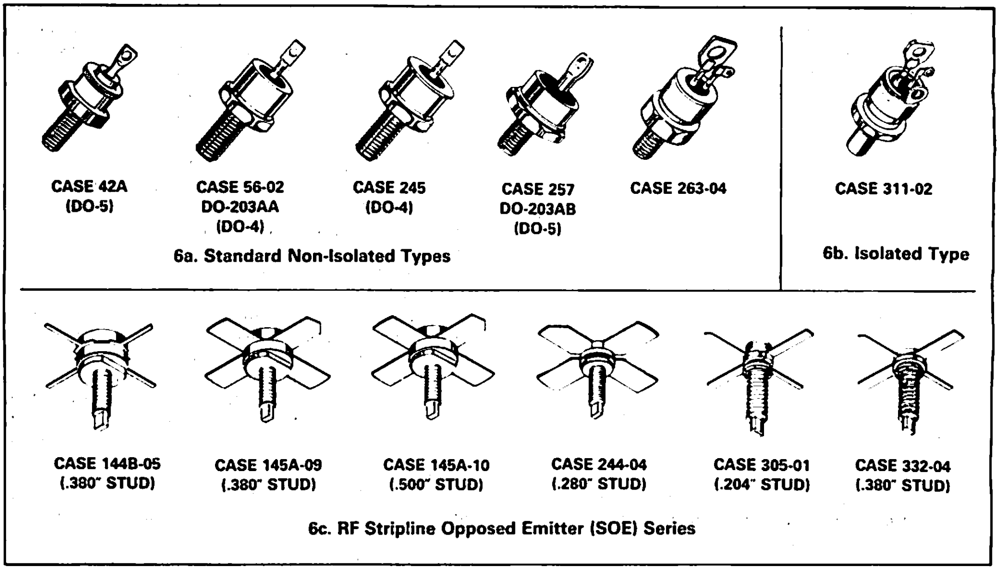


Figure 6. A Variety of Stud-Mount Parts

of excessive torque or tapping the stud into a threaded heatsink hole. Both these practices may cause a warpage of the hex base which may crack the semiconductor die. The only recommended fastening method is to use a nut and washer; the details are shown in Figure 7.

Insulated electrode packages on a stud mount base require less hardware. They are mounted the same as their non-insulated counterparts, but care must be exercised to avoid applying a shear or tension stress to the insulation layer, usually a berrylium oxide (BeO) ceramic. This requirement dictates that the leads must be attached to the circuit with flexible wire. In addition, the stud hex should be used to hold the part while the nut is torqued.

R.F. transistors in the stud-mount stripline opposed emitter (SOE) package impose some additional constraints because of the unique construction of the package. Special techniques to make connections to the stripline leads and to mount the part so no tension or shear forces are applied to any ceramic — metal interface are discussed in the section entitled "Connecting and Handling Terminals."

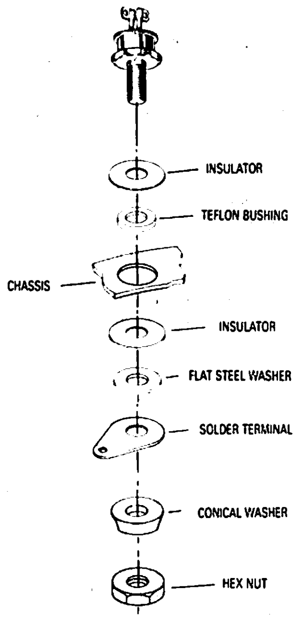
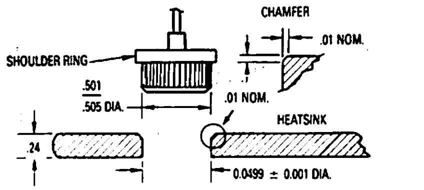


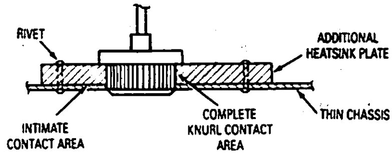
Figure 7. Isolating Hardware Used for a Non-Isolated Stud-Mount Package

Press Fit

For most applications, the press-fit case should be mounted according to the instructions shown in Figure 8. A special fixture meeting the necessary requirements must be used.



Heat Sink Mounting



Thin-Chassis Mounting

The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the case during press-in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heatsink material. Recommended hardnesses are: copper-less than 50 on the Rockwell F scale; aluminum-less than 65 on the Brinell scale. A heatsink as thin as 1/8" may be used, but the interface thermal resistance will increase in direct proportion to the contact area. A thin chassis requires the addition of a backup plate.

Figure 8. Press-Fit Package

Flange Mount

A large variety of parts fit into the flange mount category as shown in Figure 9. Few known mounting difficulties exist with the smaller flange mount packages, such as the TO-204 (TO-3). The rugged base and distance between die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is therefore good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger-tight the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 10. Machine screws (preferred) self-tapping screws, eyelets, or rivets may be used to secure the package using guidelines in the previous section. "Fastener and Hardware Characteristics."

The copper flange of the Energy Management Series (EMS) Modules is very thick. Consequently, the parts are rugged and indestructible for all practical purposes. No

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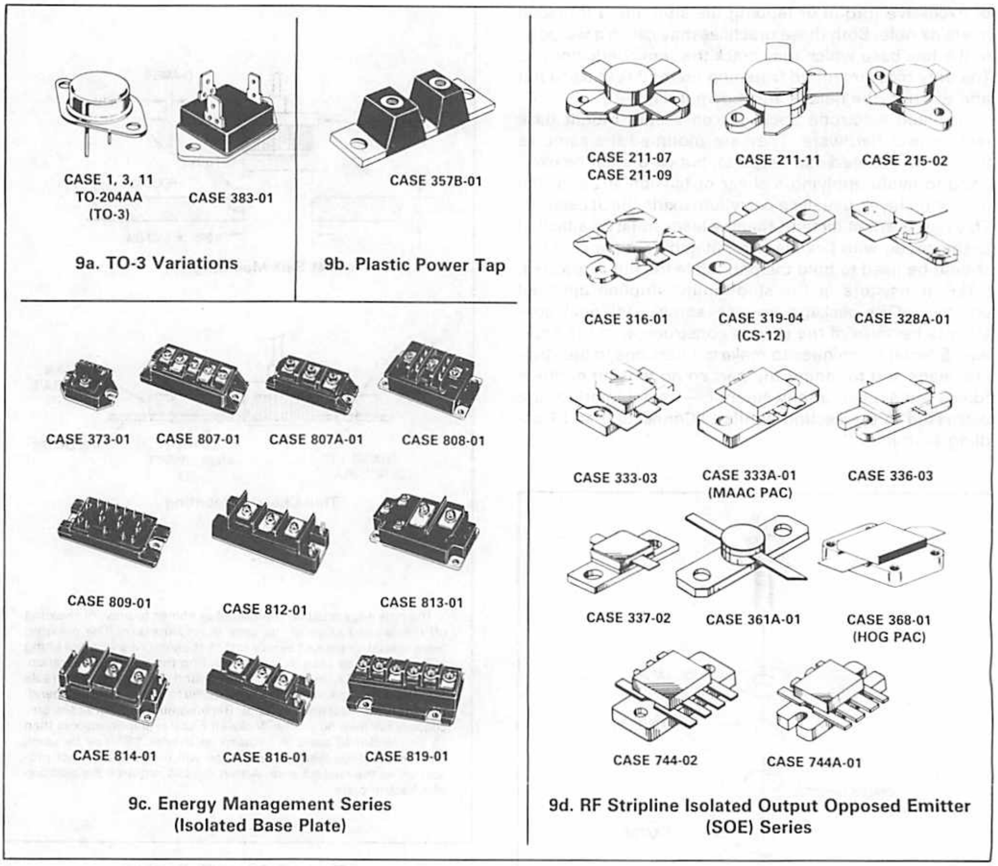


Figure 9. A Large Array of Parts Fit into the Flange-Mount Classification

special precautions are necessary when fastening these parts to a heatsink.

Some packages specify a tightening procedure. For example, with the Power Tap package, Figure 9b, final torque should be applied first to the center position.

The RF power modules (MHW series) are more sensitive to the flatness of the heatsink than other packages because a ceramic (BeO) substrate is attached to a relatively thin, fairly long, flange. The maximum allowable flange bending to avoid mechanical damage has been determined and presented in detail in EB107 "Mounting Considerations for Motorola RF Power Modules." Many of the parts can handle a combined heatsink and flange deviation from flat of 7 to 8 mils which is commonly available. Others must be held to 1.5 mils, which requires that the heatsink have nearly perfect flatness.

Specific mounting recommendations are critical to RF devices in isolated packages because of the internal ceramic substrate. The large area Case 368-1 (HOG PAC) will be used to illustrate problem areas. It is more sensitive to proper mounting techniques than most other RF power devices.

Although the data sheets contain information on recommended mounting procedures, experience indicates that they are often ignored. For example, the recommended maximum torque on the 4–40 mounting screws is 5 in/lbs. Spring and flat washers are recommended. Over torquing is a common problem. In some parts returned for failure analysis, indentions up to 10 mils deep in the mounting screw areas have been observed.

Calculations indicate that the length of the flange increases in excess of two mils with a temperature change of 75°C. In such cases, if the mounting screw torque is excessive, the flange is prevented from expanding in length, instead it bends upwards in the mid-section, cracking the BeO and the die. A similar result can also occur during the initial mounting of the device if an excessive amount of thermal compound is applied. With sufficient torque, the thermal compound will squeeze out of the mounting hole areas, but will remain under the center

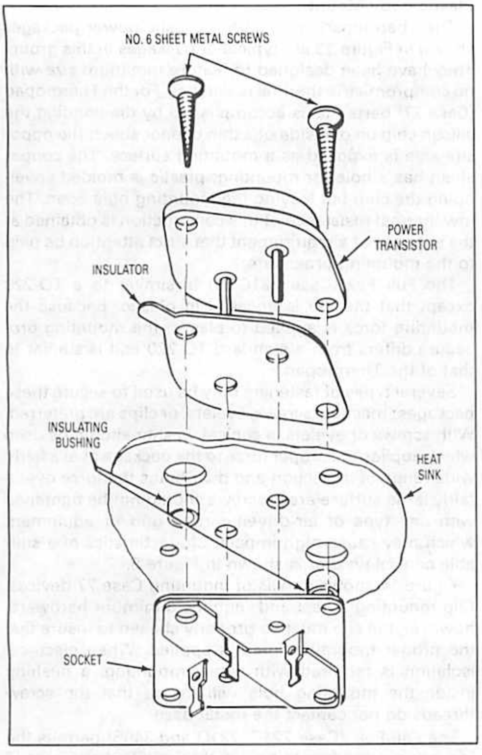


Figure 10. Hardware Used for a TO-204AA (TO-3) Flange Mount Part

of the flange, deforming it. Deformations of 2–3 mils have been measured between the center and the ends under such conditions (enough to crack internal ceramic).

Another problem arises because the thickness of the flange changes with temperature. For the 75°C temperature excursion mentioned, the increased amount is around 0.25 mils which results in further tightening of the mounting screws, thus increasing the effective torque from the initial value. With a decrease in temperature, the opposite effect occurs. Therefore thermal cycling not only causes risk of structural damage but often causes the assembly to loosen which raises the interface resistance. Use of compression hardware can eliminate this problem.

Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 11. Mounting considerations for all varieties are similar to that for the popular TO-220 package, whose suggested mounting arrangements and hardware are shown in Figure 12. The rectangular washer shown in Figure 12a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6–32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is suggested when using a 6–32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO-220 packages have a chamfer on one end. TO-220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

The popular TO-220 Package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure B1.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.[6] In addition, it separates

(6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.

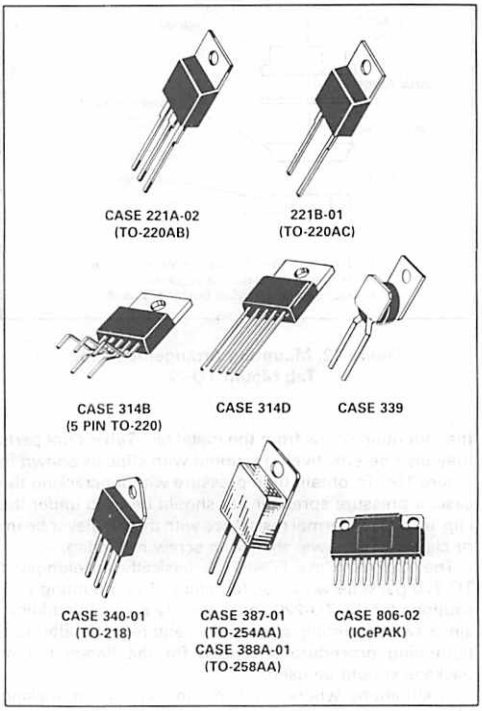


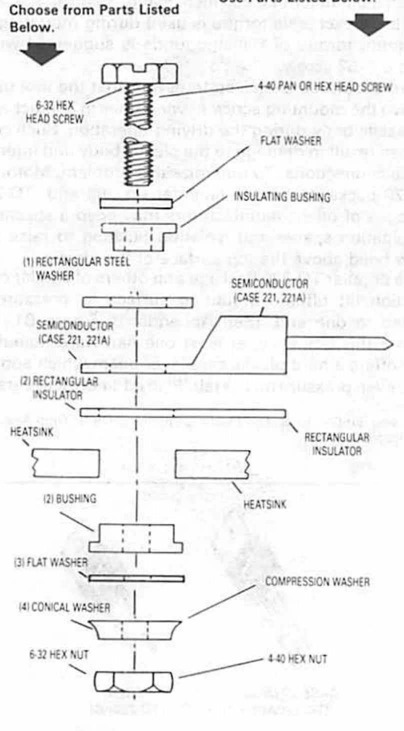
Figure 11. Several Types of Tab-Mount Parts

a) Preferred Arrangement for Isolated or Non-isolated Mounting. Screw is at Semiconductor Case Potential. 6-32 Hardware is Used.

Choose from Parts Listed Below.

b) Alternate Arrangement for Isolated Mounting when Screw must be at Heatsink Potential. 4-40 Hardware is Used.

Use Parts Listed Below.



(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing is used.

Figure 12. Mounting Arrangements for Tab Mount TO-220

the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 15c. To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

The ICePAK (Case 806-02) is basically an elongated TO-220 package with isolated chips. The mounting precautions for the TO-220 consequently apply. In addition, since two mounting screws are required, the alternate tightening procedure described for the flange mount package should be used.

In situations where a tab mount package is making direct contact with the heatsink, an eyelet may be used, provided sharp blows or impact shock is avoided.

Plastic Body Mount

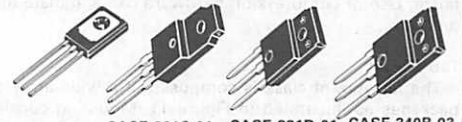
The Thermopad and Full Pak plastic power packages shown in Figure 13 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance. For the Thermopad (Case 77) parts this is accomplished by die-bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting; plastic is molded enveloping the chip but leaving the mounting hole open. The low thermal resistance of this construction is obtained at the expense of a requirement that strict attention be paid to the mounting procedure.

The Full Pak (Case 221C-01) is similar to a TO-220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO-220 and is similar to that of the Thermopad.

Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air-driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 5.

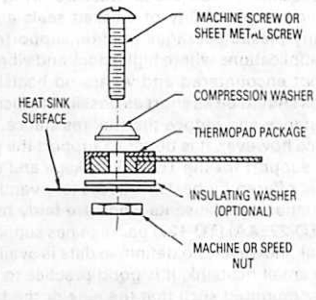
Figure 14 shows details of mounting Case 77 devices. Clip mounting is fast and requires minimum hardware, however, the clip must be properly chosen to insure that the proper mounting force is applied. When electrical isolation is required with screw mounting, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

The Full Pak, (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO-220. As shown in Figure 15c, one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure B1 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 15b may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO-220 package which is shown in Figure 15a.

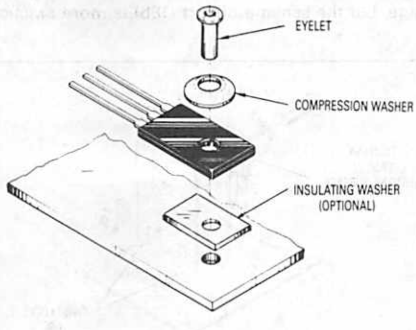


CASE 77 (TO-225AA/ TO-126) (THERMOPAD) | **CASE 221C-01 (Full Pak)** | **CASE 221D-01 (Full Pak)** | **CASE 340B-03 (Full Pak)**

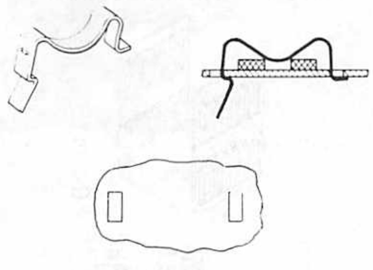
Figure 13. Plastic Body-Mount Packages



14a. Machine Screw Mounting

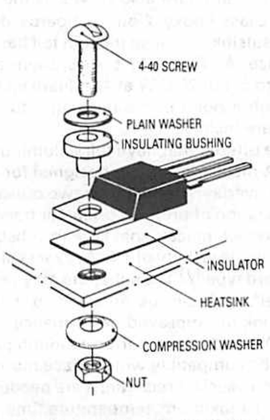


14b. Eyelet Mounting

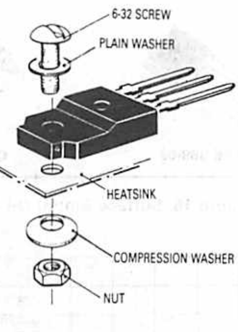


14c. Clips

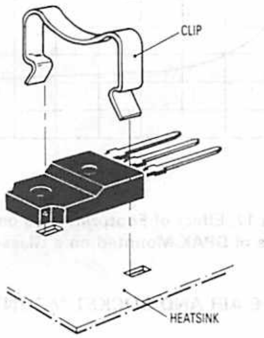
Figure 14. Recommended Mounting Arrangements for TO-225AA (TO-126) Thermopad Packages



15a. Screw-Mounted TO-220



15b. Screw-Mounted Full Pak



15c. Clip-Mounted Full Pak

Figure 15. Mounting Arrangements for the Full Pak as Compared to a Conventional TO-220

Surface Mount

Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 16, for example, will accommodate a die up to 112 mils x 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.

Standard Glass-Epoxy 2-ounce boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 17 shows, thermal resistance assymtotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlayed with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.[7] The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

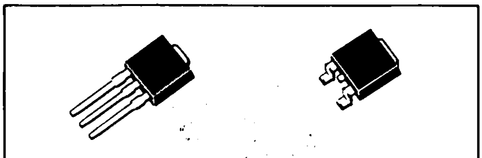


Figure 16. Surface Mount D-PAK Parts

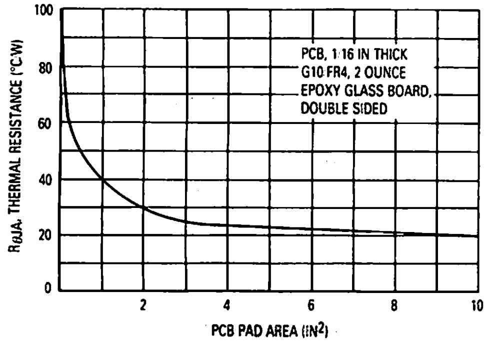
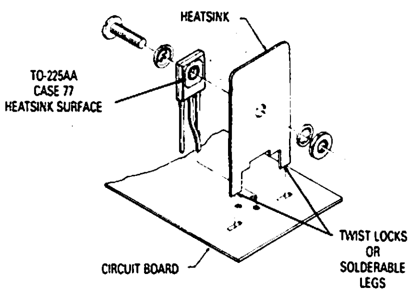


Figure 17. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass-Epoxy Board

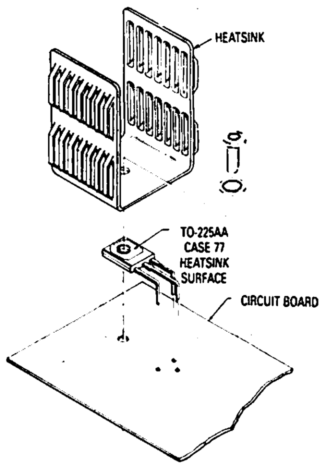
FREE AIR AND SOCKET MOUNTING

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO-220 Package and other similar types is offered by heatsink accessory vendors.

In many situations, because its leads are fairly heavy, the CASE 77 (TO-225AA) (TO-127) package has supported a small heatsink; however, no definitive data is available. When using a small heatsink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 18. The arrangement of part (a) could be used with any plastic package, but the scheme of part (18b) is more practical



18a. Simple Plate, Vertically Mounted



18b. Commercial Sink, Horizontally Mounted

Figure 18. Methods of Using Small Heatsinks With Plastic Semiconductor Packages

(7) Herb Fick, "Thermal Management of Surface Mount Power Devices," Powerconversion and Intelligent Motion, August 1987.

with Case 77 Thermopad devices. With the other package types, mounting the transistor on top of the heatsink is more practical.

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

CONNECTING AND HANDLING TERMINALS

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

Metal Packages

The pins and lugs of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

EMS Modules

The screw terminals of the EMS modules look deceptively rugged. Since the flange base is mounted to a rigid heatsink, the connection to the terminals must allow some flexibility. A rigid buss bar should not be bolted to terminals. Lugs with braid are preferred.

Plastic Packages

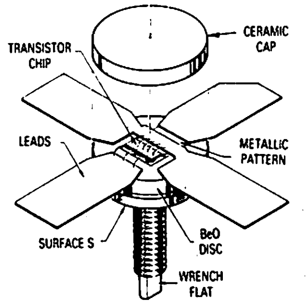
The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead-bending unnecessary. Numerous lead- and tab-forming options are available from Motorola on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead-bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

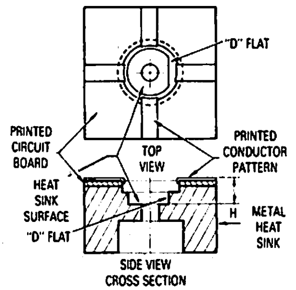
The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/16 inch is advisable for TO-225AA (CASE 77) and 1/32 inch for TO-220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

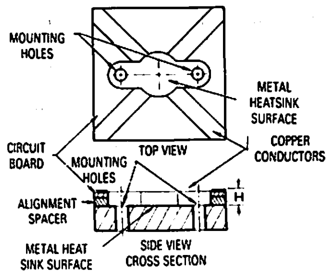
The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be



19a. Component Parts of a Stud Mount Stripline Package. Flange Mounted Packages are Similarly Constructed



19b. Typical Stud Type SOE Transistor Mounting Method



19c. Flange Type SOE Transistor Mounting Method

Figure 19. Mounting Details for SOE Transistors

exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire-wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

Stripline Packages

The leads of stripline packages normally are soldered into a board while the case is recessed to contact a heatsink as shown in Figure 19. The following rules should be observed:

1. The device should never be mounted in such a manner as to place ceramic-to-metal joints in tension.
2. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.
3. When the device is mounted in a printed circuit board with the copper stud and BeO portion of the header passing through a hole in the circuit boards, adequate clearance must be provided for the BeO to prevent shear forces from being applied to the leads.
4. Some clearance must be allowed between the leads and the circuit board when the device is secured to the heatsink.
5. The device should be properly secured into the heatsinks before its leads are attached into the circuit.
6. The leads on stud type devices must not be used to prevent device rotation during stud torque application. A wrench flat is provided for this purpose.

Figure 19b shows a cross-section of a printed circuit board and heatsink assembly for mounting a stud type stripline device. H is the distance from the top surface of the printed circuit board to the D-flat heatsink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the package, there is no possibility of tensile forces in the copper stud — BeO ceramic joint. If, however, H is greater than the package dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurrences are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead-soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heatsink surface will occur as the differences between H and the package dimension become larger, this may result in device failure as power is applied.

Figure 19c shows a typical mounting technique for flange-type stripline transistors. Again, H is defined as the distance from the top of the printed circuit board to the heatsink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur.

CLEANING CIRCUIT BOARDS

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated Freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free-standing without support.

THERMAL SYSTEM EVALUATION

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN569.

Other applications, notably RF power amplifiers or switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where
- T_J = junction temperature (°C)
- T_C = case temperature (°C)
- $R_{\theta JC}$ = thermal resistance junction-to-case as specified on the data sheet (°C/W)
- P_D = power dissipated in the device (W)

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

APPENDIX A
THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady-state conditions is generally written as:

$$q = hA\Delta T \tag{1}$$

where
q = rate of heat transfer or power dissipation (P_D)
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, R_θ, is

$$R_\theta = \Delta T/q = 1/hA \tag{2}$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A1.

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \tag{3}$$

where
T_J = junction temperature,
P_D = power dissipation
$R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
$R_{\theta CS}$ = interface thermal resistance (case to heatsink),
$R_{\theta SA}$ = heatsink thermal resistance (heatsink to ambient),
T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance, $R_{\theta CS}$, may be significant compared to the other thermal-resistance terms. A proper mounting procedure can minimize $R_{\theta CS}$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short-pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

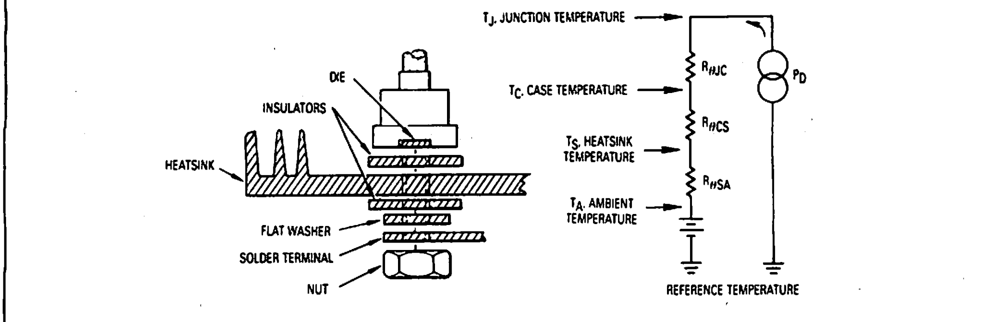


Figure A1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor

APPENDIX B
MEASUREMENT OF INTERFACE THERMAL RESISTANCE

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring DC power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO-3 package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL-I-49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented."

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The Motorola fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO-220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15 to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure

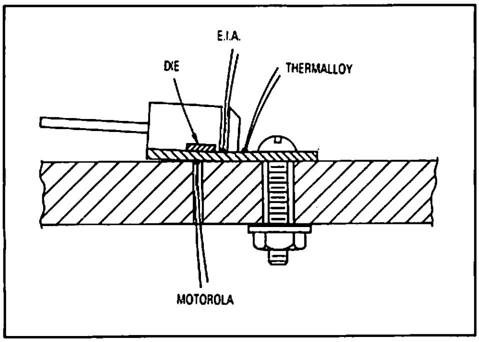


Figure B1. JEDEC TO-220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End

the semiconductor case temperature. Consider the TO-220 package shown in Figure B1. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly. To improve contact, Motorola TO-220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure. Three thermocouple locations are shown:

a. The Motorola location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b. The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction-to-sink thermal resistance must be constant for a given test setup, the calculated junction-to-case thermal resistance values decrease and case-to-sink values increase as the "case" temperature thermocouple readings become warmer. Thus the choice of reference point for the "case" temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The Motorola location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO-220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction-to-case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1 mil/inch, has a finish better than 63 μ-inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application-oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction-to-case thermal resistance while testing for interface thermal resistance. If the junction-to-case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

APPENDIX C
Sources of Accessories

Manufacturer	Joint Compound	Adhesives	Insulators						Heatsinks
			BeO	AlO_2	Anodize	Mica	Plastic Film	Silicone Rubber	
Aavid Eng.	X	X	—	—	—	—	—	X	X
AHAM-TOR	—	—	—	—	—	—	—	—	X
Astrodynamis	X	—	—	—	—	—	—	—	X
Delbert Blinn	—	—	X	—	X	X	X	X	X
IERC	X	—	—	—	—	—	—	—	X
Staver	—	—	—	—	—	—	—	—	X
Thermalloy	X	X	X	X	X	X	X	X	X
Tran-tec	—	—	X	X	X	X	—	X	X
Wakefield Eng.	X	X	X	—	X	—	—	X	X

Other sources for silicone rubber pads: Chomerics, Berquist

Suppliers Addresses

Aavid Engineering, Inc., 30 Cook Court, Laconia, New Hampshire 03246 (603) 524-4443

AHAM-TOR Heatsinks, 27901 Front Street, Rancho, California 92390 (714) 676-4151

Astro Dynamics, Inc., 2 Gill St., Woburn, Massachusetts 01801 (617) 935-4944

Berquist, 5300 Edina Industrial Blvd., Minneapolis, Minnesota 55435 (612) 835-2322

Chomerics, Inc., 16 Flagstone Drive, Hudson, New Hampshire 03051 1-800-633-8800

Delbert Blinn Company, P.O. Box 2007, Pomona, California 91769 (714) 629-3900

International Electronic Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502 (213) 849-2481

The Staver Company, Inc., 41-51 Saxon Avenue, Bay Shore, Long Island, New York 11706 (516) 666-8000

Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243-4321

Tran-tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564-2748

Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245-5900

PACKAGE INDEX

PREFACE

When the JEDEC registration system for package outlines started in 1957, numbers were assigned sequentially whenever manufacturers wished to establish a package as an industry standard. As minor variations developed from these industry standards, either a new, non-related number was issued by JEDEC or manufacturers would attempt to relate the part to an industry standard via some appended description.

In an attempt to ease confusion, JEDEC established the present system in late 1968 in which new packages are assigned into a category, based on their general physical appearance. Differences between specific packages in a category are denoted by suffix letters. The older package designations were re-registered to the new system as time permitted.

For example the venerable TO-3 has many variations. Can heights differ and it is available with 30, 40, 50, and 60 mil pins, with and without lugs. It is now classified in the TO-204 family. The TO-204AA conforms to the original outline for the TO-3 having 40 mil pins while the TO-204AE has 60 mil pins, for example.

The new numbers for the old parts really haven't caught on very well. It seems that the DO-4, DO-5 and TO-3 still convey sufficient meaning for general verbal communication.

Motorola Case Number	JEDEC Outline		Notes	Mounting Class	See Page
	Original System	Revised System			
001	TO-3	TO-204AA		Flange	9
003	TO-3		2	Flange	9
009	TO-61	TO-210AC		Stud	8
011	TO-3	TO-204AA	—	Flange	9
011A	TO-3	—	2	Flange	9
012	TO-3	—	2	Flange	9
036	TO-60	TO-210AB	—	Stud	8
042A	DO-5	DO-203AB	—	Stud	8
044	DO-4	DO-203AA	—	Stud	8
054	TO-3	—	2	Flange	9
056	DO-4	—	—	Stud	8
058	DO-5	—	2	Stud	8
61-03				Flange	9
63-02	TO-64	TO-208AB		Stud	8
63-03	TO-64	TO-208BAB		Stud	8
077	TO-126	TO-225AA	—	Plastic	12
080	TO-66	TO-213AA	—	Flange	9
086	—	TO-208	1	Stud	8
086L	—	TO-298	1	Stud	8
144B-05				Stud	8
145A-09				Stud	8
145A-10				Stud	8
145C	TO-232		1	Stud	8
157	—	DO-203	1	Stud	8
160-03	TO-59	TO-210AA	—	Stud	8
167	—	DO-203	1	Stud	8
174-04				Pressfit	9
175-03				Stud	8
197	—	TO-204AE	—	Flange	9
211-07				Flange	9
211-09				Flange	9

Notes: 1. Would fit within this family outline if registered with JEDEC.
2. Not within all JEDEC dimensions.

Motorola Case Number	JEDEC Outline		Notes	Mounting Class	See Page
	Original System	Revised System			
211-11				Flange	9
215-02				Flange	9
221	—	TO-220AB	—	Tab	11
221C-02				Plastic	12
221D-01	—	—	Isolated TO-220	Plastic	12
235	—	TO-208	1	Stud	8
235-03				Stud	8
238	—	TO-208	1	Stud	8
239	—	TO-208	—	Stud	8
244-04				Stud	8
245	DO-4	—	—	Stud	8
257-01	DO-5	—	—	Stud	8
263	—	TO-208	—	Stud	8
263-04				Stud	8
283	DO-4	—	—	Stud	8
289	—	TO-209	1	Stud	8
305-01				Stud	8
310-02				Pressfit	9
311-01			Isolated	Stud	8
311-02				Pressfit	9
311-02				Stud	8
314B-01				Tab	11
314D-01				Tab	11
316-01				Flange	9
319-04				Flange	9
328A-01				Flange	9
332-04				Stud	8
333-03				Flange	9
333A-01				Flange	9
336-03				Flange	9

Motorola Case Number	JEDEC Outline		Notes	Mounting Class	See Page
	Original System	Revised System			
337-02				Flange	9
340		TO-218AC		Tab	11
340A-02				Plastic	12
340B-03			Isolated TO-218	Plastic	12
342-01				Flange	9
357B-01				Flange	9
361-01				Flange	9
368-01				Flange	9
369-03		TO-251		Insertion	14
369A-04		TO-252		Surface	13
373-01			Isolated	Flange	9
383-01			Isolated	Flange	10
387-01		TO-254AA	Isolated 2	Tab	11
388A-01		TO-258AA	Isolated 2	Tab	11
744-02				Flange	9
744A-01				Flange	9
806-02			Isolated	Flange	9
807-01			Isolated	Flange	9
807-02			Isolated	Flange	9
807A-01			Isolated	Flange	9
808-01			Isolated	Flange	9
809-01			Isolated	Flange	9
812-01			Isolated	Flange	9
813-01			Isolated	Flange	9
814-01			Isolated	Flange	9
814A-01			Isolated	Flange	9
084B-01			Isolated	Flange	9
816-01			Isolated	Flange	9
819-01			Isolated	Flange	9
043-02	DO-21	DO-208AA		Pressfit	9

AN1041

Mounting Procedures for Very High Power RF Transistors

Prepared by
Helge O. Granberg
RF Engineering
Advanced Products Group

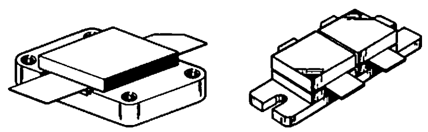
RF power semiconductors such as MRF153, MRF154, MRF155, MRF156 and MRF430 are housed in Case 368-01, whereas MRF141G, MRF151G, MRF175G and MRF176G use Case 375-01 (both shown below). All of these are high power devices (200–600 W), which results in an abnormally large amount of heat dissipated within a small physical area. For such high power transistors, special attention must be paid to the heat sink material as well as the finish and flatness of the mounting surface. The material should have at least a thermal conductivity equal to or better than copper and for the mounting surface flatness ±0.0005" can be considered sufficient. The heat sink can be made of material with lower thermal conductivity such as aluminum, but in that case a copper heat spreader should be used. The heat spreader should have a minimum thickness of 0.25" for case 375-01 and 0.375" for 368-01 and should extend at least 0.5" to 1.0" beyond the flange edges, depending on the device type and the amount of dissipation involved. For die temperature calculations of devices in case 368-01, the Δ temperature between the mounting screw areas and the bottom center of the flange is approximately 5°C and 10°C under normal operating conditions and dissipations of 150 W and 300 W respectively.

Although the data sheets contain information on the subject above as well as the mounting procedures of these devices, very few designers actually follow them. The maximum recommended torque on the #4 size mounting screws is 4–5 in.-lbs. along with split lock- and *flat*-washers, of which the latter should be in immediate contact with the flange's top surface. Experiments have shown that merely compressing the split lock washer to its full flatness produces enough torque for sufficient pressure against the heat sink. The split lock washers are available with various spring tensions. Bell type compression washers would be an even better choice if found with 5 in.-lbs. or lower torque specifications.

Calculations indicate that the length of the case 368-01 copper flange increases in excess of two thousands of an inch with a temperature change of 75°C. In such case, if the mounting screws are torqued too tight, the flange cannot expand in length but will bend upwards in the mid section, cracking the Beryllium Oxide insulators as well as the dice. It must also be noted that the thickness of the flange increases with temperature. For the excursion mentioned above, the amount is around 0.25 mils, which results in further tightening of the mounting screws, thus increasing the effective torque from the initial value. However the amount of increase is difficult to measure and depends on the exact type of mounting hardware used. The copper-tungsten flange of case 375-01 has a much lower expansion coefficient than copper, but if mounted on a copper or aluminum heat sink, it can be similarly bent during a cooling cycle as the heat sink material contracts.

Deformation can also occur during the initial mounting of the device if an excessive amount of thermal compound is applied along with sufficient screw torque. The thermal compound will squeeze out of the mounting hole areas, but will remain under the center of the flange, deforming it in a similar manner. Depending on the amount of thermal compound and its type, deflections of 2–3 mils have been measured between the flange center and corners created by such conditions. The same can happen with all flange mounted RF devices, but with thicker Beryllium Oxide insulators and lower dissipation levels the problem is less severe.

The maximum operating junction temperature and the total dissipation are usually given in the data sheets. It should be able for the device to be operated within these limits if the case temperature can be kept at 25°C or the derating factor is taken into account. The 150°C storage temperature indicated implies that the device can be operated at that case temperature, which is true but at a much derated dissipation rating. However good engineering practices would limit the case temperature to 70–80°C and the die temperature to not higher than twice that.



CASE 368-01 CASE 375-01

7

Applying Power MOSFETs in Class D/E RF Power Amplifier Design

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By H.O. Granberg
Motorola Semiconductor Products, Inc.

Class D and E are variations of switching mode amplifiers which are designated in the literature at least up to Class S. Switching means that the amplifying devices are either conducting or "open" during each half cycle and the switching from one state to the other is done as fast as possible. In some systems the switching is done at other than the carrier frequencies for modulation or other purposes. Class D and E usually refer to carrier switched amplifiers and are best suited for high frequency applications where the rise and fall times of the switching waveform are of main importance. They are directly adaptable to CW or FM, but other types of modulation are also possible by pulse width or amplitude modulation (1, 2, 3, 4, 5). The theoretical aspects have been well covered by F.H. Raab and N. Sokal in numerous publications over the years, and practical low power designs have also been shown. The author feels that since the evolution of the RF power FET, high power switching amplifiers can be designed at least up to 30 MHz and possibly 50 MHz.

Currently, Class D or E transmitters are marketed at up to 10kW power levels for the broadcast band (.55 MHz-1.6 MHz) and at 1 kW for shortwave (up to 15 MHz). All use power FETs as the switches and advertise high efficiency and reliability. When the efficiency is higher, the reliability is better since the transistor (FET) die operates at a lower temperature. Efficiencies of at least 70 percent to 80 percent in Class D and 80 percent to 90 percent in Class E are possible with the present RF power FETs at moderate power levels. Efficiency in Class D is limited mainly by the saturation resistance of the devices and the output capacitance. The objective in Class E is to use the device output capacitance as part of a tuned circuit, thus eliminating its effect as a load capacitance. In an ideal form it also ensures that the switching voltage and current waveforms are not overlapping (6, 7).

An obvious advantage of high efficiency is the smaller amount of heat generated compared to power output. This results in a smaller heat sink and more compact design, leading to smaller output devices and reduced cost. An important application of high efficiency amplifiers is in battery powered transmitters, where battery lifetimes 25 percent to 30 percent longer than Class C should be possible. Another advantage is simplified circuit design, since interstage matching networks are not required, as they are with Class A, B and C, where the amplifying devices act as current sources rather than switches. From the low level limiter to the P.A. the power gain can be as high as 40 dB to 50 dB and the system bandwidth is limited only by the response of the output transformer or matching network. Assuming a constant pulse width from the limiter on, extremely wide-band amplifiers can be designed with no variation in power gain. Figure 1 shows an estimated power level vs. frequency curve of Class D/E feasibility with today's technology.

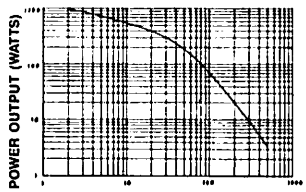

FIGURE 1. Estimated maximum power levels with a push-pull or single ended Class D/E amplifier based on present technology.

Preparing the Carrier Input Signal

Since the emphasis here is on relatively high power levels (up to 300W-400W per push-pull pair), the signal processing circuitry is only designed to operate up to 50 MHz. At higher frequencies it may be desirable to employ single ended designs in order to avoid any possible phase errors, which become exponentially more difficult to control with increasing frequency. The phase errors can be minimized in a push-pull circuit by providing the P.A. input drive through a transformer with bandwidth characteristics that will not affect the input rise and fall times considerably. Due to the difficulty in designing such transformers, which would require a bandwidth of one to several hundred MHz for a 2 MHz to 50 MHz carrier, it was decided to create the required 180 degree out-of-phase signals with ECL integrated circuits (*Fig. 2*).

The RF drive is first limited in a pair of cross coupled hot carrier diodes and then in three sections of ECL line receivers (MC 10H116). The limiter has approximately 50 dB dynamic range for amplitude modulated signals such as SSB. A peak detector circuit, shown at the upper left, was included, although the scope of this article is not to describe a modulated system.

The detector was designed to operate at audio frequencies, 300 Hz to 3 kHz, with an RF carrier down to 2 MHz. The detector output with two-tone RF input is shown in Figure 3.

The output audio envelope can be fed to an audio amplifier which can drive an emitter-follower or switchmode regulator that supplies the V_{DD} to the Class D P.A. The principle is to provide the amplitude information through this audio chain and the phase information through the RF chain. They are then combined in the output stage to provide a restored AM or SSB signal. This technique is called Envelope

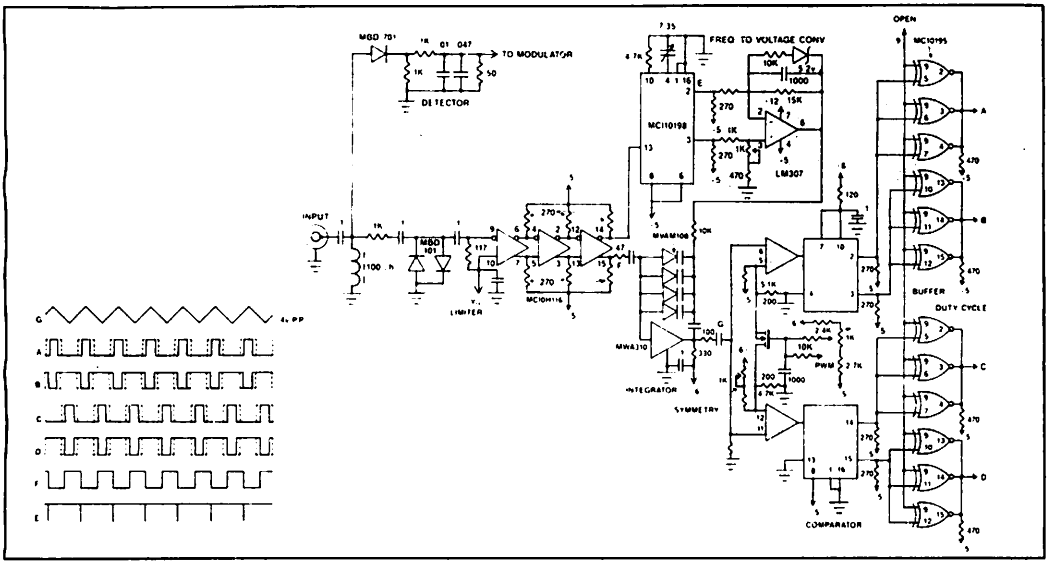

FIGURE 2. Schematic of the signal processor used in all the Class D experiments described. If the input is in sine wave, the amplitude can vary from .5 to 100 peak to peak. The output duty cycle is independent of the frequency.

Elimination and Restoration (EER) (2, 3, 4, 5). Pulsewidth modulation techniques can also be used to amplify AM and SSB signals with a Class D amplifier (1); however, the technique involves generating an inverse sine reference signal at the carrier frequency, and the distortion would be directly reflected to the output. The finite switching speeds also limit the dynamic range in this system. Both problems make the pulse width modulation technique practical only up to a few MHz. In contrast, distortion in an EER system is generated only by phase errors between the audio and RF chains (4, 5).

Although the circuit in Figure 2 is not intended for pulse width modulation, a provision was made to adjust the pulse width manually to allow the power output to be varied and to ensure that the P.A. drive signals would not be overlapping. The objective was to provide a constant duty cycle with frequencies anywhere between 2 MHz and 50 MHz. This was difficult to achieve, and the final result was that the frequency was split into two segments: 2-25 MHz and 25-50 MHz. Adjustments in the MC10198 (one shot) timing as well as the LM307 and the comparator biases were necessary to cover each band. The problem was mainly with the limited capacitance range of the MVAM108 tuning diodes in the integrator. Their capacitance should track the frequency in order to provide a constant amplitude triangular wave output from the integrator. It must be pointed out that the physical circuit layout of the integrator is critical for low distortion output. All lead lengths should be minimized and elsewhere proper ECL wiring techniques should be followed.

The circuit of Figure 2 was intended to be used with a number of Class D P.A.s studied. It is remotely located from the driver and the P.A. assembly, and the signals between the two are connected by twisted wire lines. The pull down resistors in the MC10195 outputs are provided only for testing purposes, while the terminations are located at the driver and P.A. assembly.

The Driver

Because of direct coupling between the stages, each side of the push-pull circuit requires its own driver and pre-driver. This has the advantage that the high peak current requirement from the driver is divided between two circuits, which will be discussed later in detail. For this reason also the push-pull configuration was chosen. A single ended design would require an output FET twice as large, having proportionally higher gate input capacitance.

The ECL level limited signal must be converted first to a voltage swing of at least 2 to 3 volts above ground to feed the driver, which may have a FET or bipolar input. The circuit shown in Figure 4E can be used for this, or 4F, if the ECL is operated between ground and +5 volts. Alternatively, integrated circuits, such as the MC10G125 ECL to TTL converter or MC10177 MOS clock driver, can be used for this function, as shown in Figure 5. These ICs can be operated with single phase inputs as well as two phase. The voltage swing must be increased to 8 to 10 volts above ground to ensure that the P.A. FETs will be fully "turned on."

Figure 4 gives examples of drivers that are fairly simple and can drive heavy capacitance loads. Figure 4A is the most complex, but it performs well providing the devices are correctly selected and the gate threshold voltages of Q3 and Q5 are equal. Without a load no current should flow through Q2 and Q3. The last statement applies to 4B also, if Q2 and Q3 are switched correctly. This basic circuit is used in the output stages of many TTL gates and buffers, and in integrated form the transistor base-emitter forward and saturation voltages can be controlled closely. In a discrete form the value of Q1 emitter resistor must be adjusted according to the parameters above. In addition, Q3, which is in common emitter configuration, must be of a fine geometry, high frequency design to minimize the base-emitter junction stored charge effect. Such devices in the NPN polarity are currently available in many package configurations.

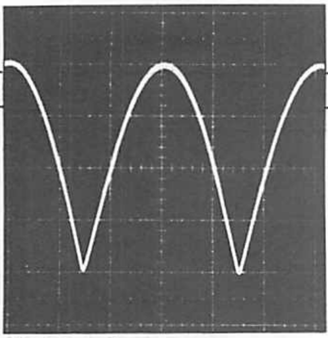

FIGURE 3. The peak detector output waveform (Fig. 2) with a two tone SSB drive signal. This can be used to control the P.A. supply voltage for amplitude modulation.

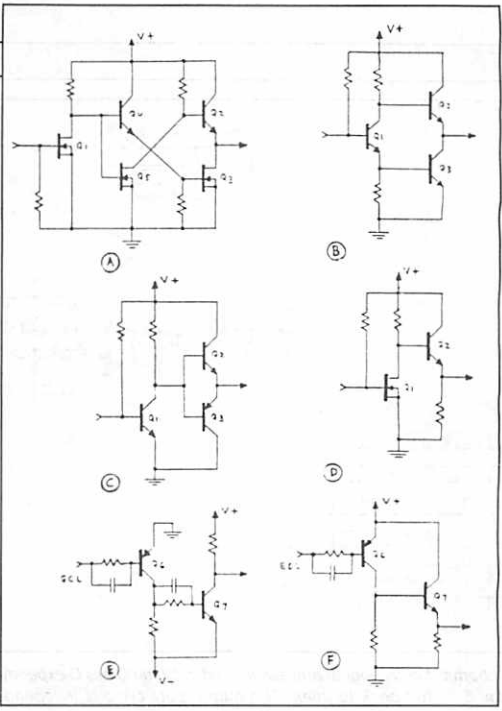

FIGURE 4. Various Class D driver configurations. E and F are intended for ECL to positive level conversion, while A, B, C and D are designed to operate from higher voltage inputs to drive capacitive loads, such as the FET fates.

Circuits in 4C and 4D are the simplest and least critical, although both have some drawbacks. 4D uses a passive pull down, where the resistor value can be calculated for the desired turn off time when the voltage and FET input capacitances are known. A typical value for a 50W FET operating at 50 MHz would be around 3 to 4 ohms. The resistor current will be added to the input capacitance (C_{iss}) charge current, requiring a doubled current capability from the emitter follower (Q_2), although the average power dissipated is equal to that of circuits with active pull down. The complementary emitter follower in 4C is probably the most efficient driver, considering its simplicity. It is tolerant against variations in device parameters and has the lowest output impedance if the transistors are properly selected. The only disadvantage is the scarcity of high frequency PNP transistors with sufficient current capabilities. In all Figure 4 circuits the pre-driver (Q_1) can be a bipolar transistor or a FET depending on the exact requirements and the input signal amplitude.

Power MOSFET HF Switching Characteristics

At low frequencies the MOSFET gate should present a purely capacitive load to the driver. In switching applications, however, the rise and fall times represent a much higher frequency component than the fundamental. For example, if at 30 MHz carrier 4 nanosecond switching times can be tolerated, at 80 percent amplitude the 4 ns represents roughly a 100 MHz sine wave. Examining the MRF150 Smith Chart (data sheet) and converting the information into parallel form we find that the input capacitance remains a constant 800 pF up to 150 MHz. This is an average value under biased and linear operating conditions, but it indicates that the wire bond and package inductances have a minimal effect at that frequency. For switching applications, where the FET goes into saturation, the input capacitance is more difficult to define.

As shown in Figure 5, the C_{iss} varies with gate and drain voltages. At left (zero gate voltage) we can see the value under the conditions where the parameter is normally specified. At increased gate voltage the capacitance goes down to its lowest value, just before reaching the threshold voltage. When the FET begins to draw drain current, there is a point where the device gain is at its highest value. At that time the drain voltage is also lowered, resulting in reduction of the depletion area and causing an overlap between the gate and the bulk material. This in turn increases the value of drain to gate capacitance (C_{rss}), which will be multiplied further by the gain and reflected back to the gate. As a result, a sharp peak in the C_{iss} will occur. When the FET is fully saturated, the C_{iss} settles to its value under zero drain voltage and positive gate conditions. A similar effect is present with all power MOSFETs to some extent depending on their exact parameters. The data was taken at 1 MHz but is not expected to change considerably at higher frequencies.

Figure 6 shows two input drive waveforms superimposed at 25 MHz repetition rate: the driver waveform without a load (A) and when loaded by the FET gate (B).

The notches in B are the result of the C_{iss} peak in both turn on and turn off. In low frequency switching applications this may not be directly noticeable due to the much slower transition times involved. For HF, the peak value of the C_{iss} must definitely be taken into consideration when designing the driver. Assuming the driver pulse amplitude is 8 volts, the driver has a relatively easy task in turning the FET on. The C_{iss} is low up to the threshold point, approximately 3.5 volts, increasing to 4.5 volts. After this, the voltage only has to increase another 3.5 volts, loaded by the high capacitance. Since this period falls within the "on" cycle of the FET, a slower rise time is of lesser importance. In turning the FET off the driver must supply the highest current at the beginning of the cycle. Its dissipation is also at the peak at this point and high until the first 3.5 volts of discharge is completed, the load capacitance lowered and the voltage across the driver gradually reduced. This is the most critical part of the cycle since it can result in a

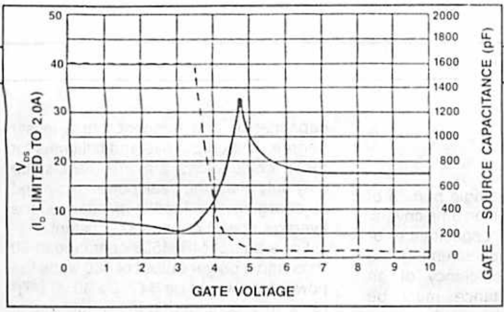

FIGURE 5. Typical TMOS (MRF-150) gate-source capacitance versus gate and drain voltages. All power MOSFETs behave more or less similarly, depending on their die structures, geometries and electrical parameters.

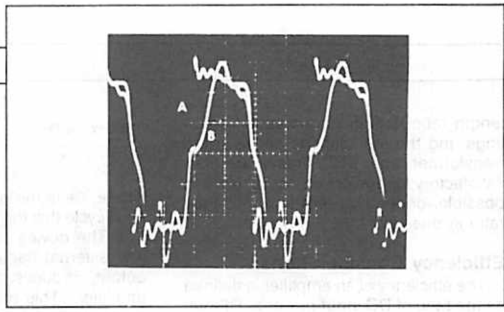

FIGURE 6. Driver output waveform at 25 MHz. A without a load. B loaded by the P.A. FET gate. Results of the uneven gate capacitance distribution versus gate and drain voltage can be noticed in B. 10 nS and 2v/div.

delay in the turn off of the FET, causing both sides of a push-pull circuit to draw current simultaneously for a part of the cycle. The delay can be prevented or minimized by adjusting the driver voltage amplitude only to a level necessary to switch the output FETs to a full saturation and completely off. Any excess voltage swing increases the delay and also the dissipation in the driver.

Considering the complex nature of the FET C_{iss}, a most realistic figure for the required driver output impedance can be obtained if it is calculated for the peak capacitance value and the gate voltage swing between saturation and threshold:

$$\frac{-t}{C \times L_n(1 - \frac{V_2}{V_1})}$$

where:

$-t$ = required switching time (4ns).
C = FET input capacitance at the peak (1300 pF).
V_1 = gate voltage at saturation (8V).
V_2 = gate voltage between saturation and threshold (4.5V).

then:

$$\frac{-4x10^{-9}}{1.3 \times 10^{-9}(-.82)} = \frac{-4}{1.3 \times (-.82)}$$

= 3.74 ohms

This translates to 1.2 amperes up to where the driver transistors (NPN and PNP) must have a linear h_{FE}. As stated earlier, the 4 ns transition times represent about a 100 MHz sine wave, which means that an HF beta of 10 would require an f_t of 1000 MHz for the driver transistors according to the 6 dB/octave slope (8). The DC beta (h_{FE}) is not critical but must be greater than 10.

For the complementary emitter follower, the PNP half may be difficult to find with the above specifications. In fact, some special units were built for experimental purposes using a multiple die similar to the 2N5583. The NPN counterpart was an MRF630. This combination worked well except that heat sinking of the TO-39 packages was difficult because of the close proximity of the pair, which is necessary to minimize all inductances.

Output Impedance Matching

In low voltage Class A, B and C designs the output impedance matching becomes difficult due to the low impedance levels involved at 100 W and higher output levels, if broadband operation is required at HF. The matching is usually done with broadband transformers, of which the transmission line types offer the best broadband performance. For many applications, however, they are considered impractical and bulky in higher than 9:1 or 16:1 impedance ratios (9). There are other transformer types that are more convenient in physical aspects but lack the bandwidth characteristics. This poses a real problem, especially for Class D where bandwidths from 1 MHz to 100 MHz or higher may be required. A transformer type which is fairly good for impedance ratios to 25:1 and higher is one where the low impedance winding is formed by metal tubes inside ferrite sleeves and the high impedance widing is threaded through the tubes (7, 9). Such a transformer was used in the design of Figure 7, where the power output specification was 100 W, requiring the closest integer of 16:1 impedance ratio.

Two points in its behavior must be noted.

1. The high leakage inductance of this type transformer requires an unusually large capacitance for compensation limiting the bandwidths. These capacitances, of which the device output capacitance will be a part, are normally located across the primary or secondary windings, or both (Figure 7, C_1 and C_2). The required compensation can be calculated from the measured leakage inductance, and the maximum frequency will be limited by the device output and stray capacitances. At the resonant frequency the transformer VSWR will be 1.2:1, increasing to approximately 6:1 an octave higher (10). The leakage inductance can be measured across the secondary with the primary shorted. The connection inductances must be added to this and the maximum tolerable value is:

$$L_1 = \frac{R_L}{2\pi f}$$

where:

L_1 = Leakage inductance (μH)
R_L =Load impedance (50 ohms)
f = Maximum frequency (Mhz)

In Class D, the limited bandwidth will slow down the output rise and fall times. Since the transformer acts as a low Q resonant circuit, this can be used to place the amplifier in Class E mode of operation by moving the resonance down to the carrier frequency, although the Q cannot be properly controlled and the system may not be optimized.

2. The coupling between the two halves of the low impedance primary winding is only provided through the secondary and is very poor at higher frequencies due to the leakage inductances. If the amplifier is designed for voltage switching configuration, the transformer center tap is bypassed to ground. Due to the decreasing coupling the effect of the center tap is lost and at higher frequencies the amplifier will turn into current switching mode. With these two configurations the drain voltage and current waveforms are reversed (7), resulting in unpredictable waveshapes at the between frequencies. This will not affect the amplifier's efficiency, which theoretically should be equal for voltage and current switching modes, but makes its operation more difficult to analyze. If the transformer is properly designed, e.g., the tube diameter to

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length ratio is high for increased couplings and the inductances between the transformer and FET drains are low, satisfactory operation up to 50 MHz is possible, depending on the impedance ratio in question.

Efficiency Considerations

The efficiency of an amplifier is defined as the ratio of DC input power to RF output power and is usually expressed in percentage. There are three main device parameters that affect the efficiency of a Class D amplifier:

1. Saturation voltage, in some data sheets given as saturation resistance, is directly proportional to the current and more linear with FETs than with bipolar transistors due to the latter's nonlinear diode characteristics. In contrast to the bipolar the FET has a highly positive temperature coefficient slope (saturation voltage increases with temperature), approximately 1 percent/°C. The DC value starts higher with FETs than with comparable devices. At RF the saturation voltage is further increased by the package and wire bond inductances and is more noticeable with low voltage devices due to the low impedances and high current levels involved. The RF saturation voltage can be more accurately measured than calculated. Typical values for MRF140 and MRF150, for example, are 1.7 volts and 3.0 volts, respectively, at 10 amperes and 30 MHz. From these numbers the efficiency can be calculated simply as:

$$\frac{V_{DD}-V_{sat}}{V_{DD}}$$

2. The switching speed of a transistor or a FET is mainly related to its high frequency characteristics, as discussed earlier in the driver paragraph. The internal capacitances have a large effect, but they in turn are a function of f_t, except for small differences between various FET structures such as interdigitated and overlay or TMOS and VMOS. For comparable geometries the FET has about three times higher f_t than the BPT. This means that some of the low frequency switching FETs can be used as RF switches up to 20 MHz to 30 MHz if a low output impedance driver is provided. In case of a sine-wave driving signal (7) the switching speed relies totally on the device high frequency gain and the input signal amplitude, whereas with a square-wave drive, it is affected by the input rise and fall times as well. Assuming a linear ramp with no distortion, the effect of transition times on efficiency can be calculated as:

$$\frac{360 \times \sin\Theta s}{2\pi \times \Theta s}$$

where: Θs is the phase angle portion of a full cycle that the transition time covers.

3. The device output capacitance, or any external capacitance shunting the output, reduces the efficiency of an amplifier. This capacitance must be charged to nearly twice the supply voltage during each cycle, and the power used is dissipated in the amplifying device. In narrowband designs and Class E switching it can be tuned out but not completely since its value varies with the output voltage swing. With power transistors and power FETs, the C_{ob} or C_{oss} is usually dominant and stray capacitances can be disregarded for practical purposes. Their values in data sheets are specified at DC and at the recommended supply voltage for RF, or mostly at 25 volts for LF switching. For example, the C_{oss} for the MRF150 is given as 250 pF at 50 volts but is higher at lower voltage and increases sharply at voltages below 5; thus, for accurate calculations a higher C_{oss} value should be used for an average, but it can only be obtained from a C_{oss} vs voltage curve. According to the formula in Reference 7, (p.446) the power loss for a push-pull amplifier is:

$P_s = C_s(2\ V_{eff})^2(2f) = 8\ C_s\ V_{eff}{}^2 f$ where:
P_s = Power loss
C_s = Device output capacitance
$V_{eff} = V_{DD} - V_{sat}$
f = Frequency

From this we can see that power loss depends mostly on supply voltage and on capacitance and frequency to a lesser degree. The output rise and fall times for these calculations are irrelevant since they only affect the peak power dissipated in charging the load capacitance, the average power remaining constant.

For a pair of MRF150s operating at 50 volts and a power output of 300 watts the power loss would be 8 (250×10^{-12}) $(47)^2$ (30×10^6), considering the worst case at 30 MHz. (2×10^{-3}) (2200) (30) = 132 watts and the efficiency is:

$$\frac{300}{132 + 300}$$

= 69 percent.

If the same die (MRF140), with its 450 pF output capacitance, were used in a similar 28 volt system, the efficiency would be (3.6×10^{-3}) (692) (30) = 75 percent. This is in contrast to the belief that a higher supply voltage automatically results in higher efficiency except when the circuit losses become high at very low output impedances. Considering this, it would seem that Class D efficiency is not much better than Class B or Class C, at least at higher supply voltages. If we calculate the total efficiency, taking all the above factors into account, it is only about 60 percent, However, efficiencies up to 80 percent have been demonstrated in practice in similar systems, using the MRF150s or comparable devices.

It is obvious that load capacitance is the one factor that limits amplifier efficiency most seriously, unless it can be compensated for. Assuming a perfect output transformer in a Class D push-pull amplifier,

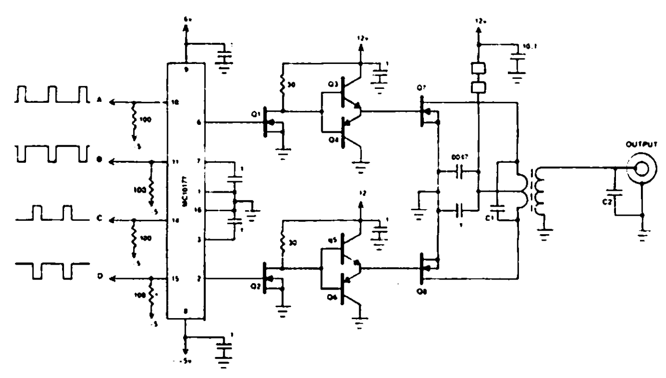

FIGURE 7. Schematic of Class D push-pull amplifier. ECL integrated circuits are used to provide the 180 out of phase input signal (see Fig. 12). This makes the pulse width easy to control compared to transformer coupling.

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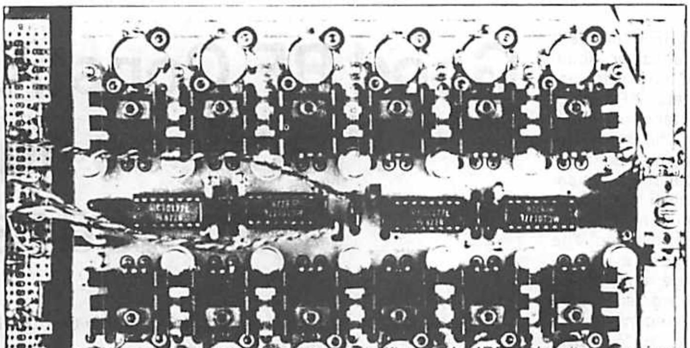

FIGURE 8. An experimental 2 kW Class D amplifier. Each MRF[illegible] has its own driver, while the drains are directly paralleled. The amplifier operates up to 15 MHz with an efficiency of [illegible] (see text).

the compensation could be done by inserting a required amount of series inductance between the drains and the transformer primary. This would form a resonant circuit with the device C_{oss}, limiting the bandwidth to some extent, and the advantage of the perfect transformer would be lost. This inductance can be used and sometimes is used unintentionally to tune out the device output capacitance, but since the effective C_{oss} varies within the RF cycle, total compensation can hardly be achieved. Thus, in practical amplifier circuits of this type, there is a tradeoff between efficiency and bandwidth, which also applies to Classes B and C.

Conclusion

Commercial Class D and E transmitters up to 1 kW and 10 to 15 MHz are on the market. The author demonstrated a 1 kW, 10 MHz amplifier in 1981 (11), which was later evaluated by the National Bureau of Standards. Other designs since then include an 800 W amplifier at 13.54 MHz with four MRF150 FETs, a 100W unit for 25 to 50 MHz operating at 12 volts and a 2 kW, 50 volt system (Fig. 8) which did not function as expected at frequencies above 15 MHz. The main problem was increasing inductance in the power FET drain connections to the output transformer. The component physical size undoubtedly places a limit for high power designs of this type, unless multidimensional constructions can be made feasible.

The importance of the physical layout must be emphasized, since it is the key to a properly operating system no matter how good the electrical design is. We must remember that we are dealing with frequency components of 100 MHz and higher in a 30 to 50 MHz carrier system, where even a nanosecond difference in delays between each side of a push-pull circuit drive signal will noticeably affect efficiency.

Since high power Class D and E designs up to 15 MHz with efficiencies far exceeding those at Class B have been shown, the author feels that the frequency range can be extended to at least 30 MHz with proper physical design, leading to high efficiency linear and other applications.

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Good RF Construction Practices and Techniques

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Categories considered include Device Selection; Emitter Inductance; Amplifier Instability; Single, Parallel or Push-Pull Configurations and Thermal Design.

Many designers of RF equipment with vacuum tubes or solid-state small signal equipment are not familiar with solid-state RF power design, and the importance of many aspects in developing the hardware. It is true that the same rules apply in each case, but the physical construction of RF power circuits is much more critical due to the low input impedance levels involved. The importance of these aspects are frequency, supply voltage and power level dependency. For a given supply voltage the input impedances are about equal for UHF at 10-15 watts, VHF at 35-40 watts and HF at around 100 watts. This means that the impedance levels of properly selected devices for each application (except the output) are nearly equal, but the RF currents are a function of the power level. Thus, it can be deduced for example that equal emitter inductances, in common emitter operation, can be tolerated in each case.

Selecting The Device

RF power transistors are being made for three basic supply voltages: 12.5V (12-15.5V) for land mobile and marine applications: 28V (24-32V) and 50V (40-50V) for aircraft, military and base stations. The high voltage devices have higher collector resistivities than the ones designed for low voltage operation, and the emitter ballast resistors have higher values. Devices designed for high voltage operation can be used at lower voltages, but not vice-versa. This would result in saturation at a lower power level than normal, but will give a rugged design. An example of this is a high level AM modulated amplifier, where the breakdown voltages must be high enough not to be exceeded by the modulation peaks.

UHF devices have a thinner epitaxial layer than parts designed for VHF and the same is true from VHF to HF. The higher frequency devices also use much finer geometries than the lower frequency devices, resulting in higher f_T and higher power gain. It is not recommended in general, that a UHF or VHF device be used at HF frequencies, except at reduced supply voltages and reduced power levels. Even then, stability problems may be encountered due to the high power gain. A 2N3866 is a popular low level driver at HF, but some power gain must be sacrificed by heavy emitter feedback. Going the opposite way, HF devices are often used at VHF and VHF devices at UHF in applications where a low gain stage (3-6 dB) is required. Most newer RF power transistors are specified to withstand infinite load mismatches under a variety of operating conditions. However, this is providing that the maximum total dissipation rating is not exceeded. This can happen if the device goes into self oscillation, usually a circuit oriented problem. The total dissipation is specified under RF conditions, and does not mean that the device can be DC biased up to that point at the operating voltage, although some devices could survive it. All transistors can be used for linear operation providing the power output is kept low to avoid the saturation knee. Devices specified for linear operation employ a much larger die for this reason, and have been specially processed to improve the linearity of the transfer curve.

Other important factors to consider are the input Q and matching of devices for push-pull or parallel systems. The input Q determines the broadband performance of the device, especially at the higher frequencies. For broadband application a low Q device should be selected. The Q is primarily determined by the ratio of the reactive and resistive components (X_S/R_S). The output Q is usually much lower and is not the limiting factor in most cases. Device matching should be done on power gain for class B and C, and in addition on h_{FE} and V_{BE} forward voltage for class A and AB. The power gain follows the h_{FE} to a great extent as long as the device is not saturated, and in most instances, at lower frequencies 10-15 percent h_{FE} matching is considered sufficient.

The Emitter Inductance

For simplicity we will only discuss the common emitter amplifier configuration. It should be realized that in a common base circuit, the base inductance is equally critical. To obtain the maximum power gain of a given device, the emitter-to-ground inductance must be kept as small as possible. This inductance outside the transistor consists of the transistor lead inductance to ground and the impedance of the circuit board ground plane. In most good designs it is necessary to employ a double-sided circuit board where a continuous ground plane is provided at the bottom side of the board. This is electrically accessible by feed-through eyelets or plated-through holes around the transistor mount opening, near the emitter area. For even better performance, the transistor mount opening in the board can be wrapped around with straps of metal foil, connecting areas on the top of the board to the ground plane. To minimize the lead inductance, the transistor mount opening in the circuit board, which is necessary to allow the device to be attached to a heat sink, should not be made larger than necessary for a given package type. If the lead inductance is converted to reactance at the frequency of operation, its effect can be compared to that of an equal value resistance between the emitter and ground. This will allow us to calculate the actual gain loss in each case.

The transistor wire bond and lead frame inductance are fixed parameters, and can only be changed by selecting a device in the physically smallest package that will do the job. Sometimes the same transistor die is available in various package styles such as the standard .380 SOE,* .500 SOE, or plastic TO-220. For a given die, it would be possible to obtain the highest power gain out of the .380 style since the internal package inductance is lower than in the two other cases. Also, the stud-mounted packages, although not as good thermally as a flange type, allows closer access to the ground plane, since openings for the flange ears in the circuit board are not required.

In a push-pull configuration the emitter-to-ground inductance becomes non-important, and this path only provides the DC supply to the devices. Analyzing the push-pull operation reveals that the RF current is now flowing from emitter to emitter. For this reason, the devices should be physically mounted as close to each other as possible. If this cannot be done due to an existing circuit layout or other reasons, some improvement can be obtained by connecting all the emitters together with a *wide metal strip over the* transistor caps. With flange-mounted parts, each emitter can be connected to the flange using solder lugs or wire loops under the mounting screws, enabling the heat sink to provide a low inductance connection between the emitters. For push-pull operation at UHF, special eight lead packages have been developed, where the two transistor die are attached next to each other, thus limiting the emitter to emitter inductance to that of the bonding wires. This is probably the only practical approach to UHF push-pull techniques at higher power levels.

Amplifier Instability

There are many reasons for an amplifier stage to reach conditions of instability. Sometimes it is device oriented, depending upon the amount of feedback capacitance compared to the electrical size of the device, and the phase angle of the feedback. Somewhere higher than the operating frequency the feedback phase angle will be 360°, and if the device F_T is high enough, it will oscillate. The oscillations may occur only at reduced drive levels or reduced supply voltage. In most cases it can be remedied by lowering the Q of the input circuit or making the tank circuit Q higher.

The so called half F_0 instability is fairly common with VHF and UHF amplifiers. It is more or less device oriented and is caused by a varactor effect in the base-collector junction diode or a combination of it and the base-emitter junction diode. The half F_0 usually occurs at reduced supply voltages in 12.5V systems, at some specific drive level, which indicates that when the diode DC bias is reduced, the junction capacitance will be increased, and the RF voltage swing will drive it into a parametric mode. The amplitude of the half F_0 can be reduced or sometimes totally eliminated by narrowing the system bandwidth.

Another possible cure for both problems above is de-Q'ing the base bias choke (Class B, C). This can be done with a high μ ferrite bead in line with the choke or an external low value resistor in parallel with it.

Low frequency instability is probably the most troublesome mode of self-oscillation. It usually occurs at audio frequencies or VLF, where the device has extremely high power gain. Since its oscillation is broadband in nature, it results in high collector currents, and often the device is destroyed by overdissipation. Causes for the low frequency instability are usually inadequate collector DC feed by-passing or an extremely poor ground in that area. Two or three RF chokes together with various values of by-pass capacitors from 1000 pF to several μF may be required in the DC line to stabilize the circuit. (See examples in Reference 1.)

Negative feedback through an RLC network from the collector to the base will reduce the device gain at low frequencies, and is found to be helpful on many occasions. The above modes of instability can be present when the amplifier is operated into a proper load. In addition, instabilities usually occur when operated into a mismatched or reactive load. The general rule is: The higher the stage gain, the less stable it can be under these conditions. This naturally assumes, that the amplifier is not unstable for reasons discussed earlier. A reactive load can be present in the form of a low-pass filter, and if not properly designed, will cause amplifier instabilities. A good solution to analyze the stability is presented in Reference 2. An amplifier can be tested for stability using a load mismatch simulator. (Figure 1).

L and C values will of course depend on the frequency of operation. Typically C_1 and C_2 are equal and L_1 has twice the value of L_2. The circuit should have a point, which presents a complete short and a complete open circuit and all phase angles between, which can be verified using a vector impedance meter. Attenuators can be connected between the simulator and the amplifier to limit the maximum mismatch. For example: A 3 dB attenuator would represent 6 dB return loss, limiting the VSWR to 3:1. Similarly a 2 dB attenuator would give about 4.5:1 maximum mismatch. A directional coupler and a spectrum analyzer can be used to monitor the amplifier behavior. Stability under a 3:1 mismatch is usually considered sufficient for most purposes.

Single-Ended, Parallel or Push-Pull

Each of the above configurations has its own application with regards to frequency spectrum, bandwidth and power level. A single-ended narrow-band amplifier design usually produces optimum performance of the device. These circuits are employed when power gain or other information is compiled for a device data sheet, or if an amplifier for single frequency operation is required. Lump constant matching networks can be used up to about 200 MHz and stripline designs are common at 150 MHz and up, and in fact are the most practical design concepts at UHF and microwave. With proper techniques, it is possible to achieve bandwidths of one octave or more. Tapered line or step line approach, where the line impedance varies exponentially per unit length, or a number of quarter wave lines in series, having various characteristic impedances, is widely used for this purpose. A disadvantage is that the physical layouts become rather bulky at frequencies below 500 MHz, unless substrate material with a high dielectric constant is used. (Reference 3.)

At lower frequencies, up to 100 MHz, broadband transformer matching

*Stripline Opposed Emitter

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techniques are only practical at 40-50W power levels at 12.5V or 90-100W levels at higher supply voltages. The low impedance levels and the high RF currents involved, make it difficult to adequately by-pass the transformer ground returns.

Between 100 and 200 MHz, broadband designs are difficult to implement. Lumped constant matching networks can be used, but since several sections in the input and output are required, production repeatibility may be poor. The etched air line inductors described in Reference 4 may be the best solution to this problem.

In the past it was considered poor practice to directly parallel transistors in order to obtain higher power levels. This was mainly because of uneven current sharing

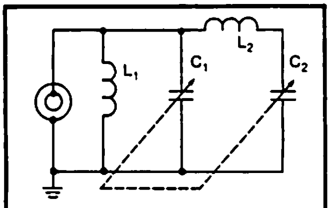

Figure 1.

between the devices, which usually led to thermal runaway and destruction of one device. However, most RF power transistors are now emitter ballasted with a built-in resistor for each emitter site. This minimizes the problem, but it is also difficult to design low loss matching networks for the reduced input and output impedance levels. Thus, the direct paralleling of transistors is not recommended in general. Paralleling may be done in such manner, that the input and output impedance of each unit are first transformed to some intermediate level or directly to 100 ohms, where the inputs and outputs are then paralleled. The best way to generate higher power levels with low power transistors is to use 50 ohm in-out "building blocks" of which any number can be combined by in-phase, quadrature or hybrid couplers. (References 5, 6, 7, 8.) This also provides isolation between the individual amplifier units.

Push-pull configuration has several advantages over single-ended amplifiers:

1. Even harmonic suppression.

2. Easier input-output matching due to higher impedance levels.

3. Emitter grounding and collector DC feed by-passing less critical.

4. Automatically combines the powers of two devices.

A push-pull circuit can be designed as a narrow-band system using lumped constant elements, or using stripline techniques at higher frequencies. These circuits are rather critical however, and require extreme symmetry between each side. A broadband circuit, using RF transformers is much more tolerable in this respect due to the tight coupling possible between the transformer windings. Push-pull circuits of this type have been designed up to 150 MHz or higher, depending on the power level and supply voltage. With proper transformer design, several octave bandwidths can be achieved. Other means of designing push-pull circuits include: a) A quarter-wave balun to provide the unbalanced to balanced function and 180° phase shift for two single-ended amplifiers. b) Two single-ended amplifiers, of which one is fed directly, while the other one is fed through a delay line, providing a 180° lag in phase at the frequency of interest. The same must be done at the output. Quarter-wave lines are commonly used for this purpose. Both a) and b) operate only within a narrow bandwidth, since the phase angle varies with frequency. The latter method is especially adaptable to UHF and higher frequencies, where the lines will be of moderate length. a) and b) also differ from conventional push-pull designs, discussed earlier, in that the phase shifting is done at the 50 ohm impedance levels rather than at the base and collector directly.

Thermal Considerations

On the reliability viewpoint it is important that the transistor die temperature is kept below a certain limit. This varies slightly with different geometries, but 160-165°C is usually considered the maximum recommended. Take the MRF422 as an example, which has a junction-to-case thermal resistance ($R_{\theta JC}$) of 0.6°C/W. If the transistor is operated at 150W dissipation, the case temperature should not exceed: $(T_J - (P_D R_{\theta JC}) = 165 - (150 \times 0.6) = 75°C$. The $R_{\theta JC}$ number published in data sheets is an average, and actually varies with power dissipation (Reference 9). Considering the thermal resistance of the heat sink, which most manufacturers specify as from the mounting surface to ambient, but do not specify the mounting suface area, the heat sink ambient temperature must be considerably cooler than 75°C. Thus, the $R_{\theta JC}$ of a heat sink actually depends on the transistor package style. An aluminum heat sink with surface thickness of 0.25" was tested. Its temperature was measured three inches from the transistor, which was mounted directly on the surface. The temperature was kept at 25°C with forced air cooling. With the 150W dissipation the transistor case temperature rose to 72°C. The case to ambient temperature then is:

$$\frac{\Delta T_{SA}}{Pd} = \frac{72\text{-}25}{150} = 0.31\,°C/W.$$

The die temperature is $T_J - (T_C - T_{C'}) = 165 - (75 - 72) = 162°C$. The same measurement was done using a copper block of 2" x 2" x 0.125" as a heat spreader under the transistor. The case temperature was measured at 58°C, and the thermal resistance decreased to (58 − 25)/150 = 0.22°C/W, and the die temperature was lowered to 148°C. The 150W dissipation is hardly realistic under normal operating conditions, but can be reached during a load mismatch. *Regarding the above* data, more attention should be paid to the heat sink material and not only its size. □

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RF power MOSFETs

While switching type MOSFETs gather all the acclaim, RF types are quietly starting to find their niche

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Since their introduction in the mid-70s, power MOSFETs have found major use in switching power supplies and in motor control circuits. More recently, however, they are being considered more and more for use as RF power amplifiers because they offer certain advantages over bipolar transistors. These advantages include higher input *impedance* (in all circuit configurations), gain control by varying the DC gate voltage bias, and immunity to thermal runaway. They do have some disadvantages, though — probably the biggest is their higher cost. Other disadvantages of MOSFETs include a higher saturation voltage than bipolars and their susceptibility to gate punch-through.

RF and switching MOSFETs differ

Power MOSFETs made for RF applications differ in a number of ways from those made for switching applications. For example, RF power MOSFETs usually have much finer die geometries than switching MOSFETs. Also, their die metallization pattern is divided into a number of segments, with each segment having separate gate and source bonding wires. This reduces wire bonding inductances and lowers the MOS capacitances within the die, greatly increasing their operating frequency capabilities.

RF power MOSFETs are generally n-channel, enhancement-mode devices, which means that the drain is positive with respect to the source and the gate must be biased to a positive voltage with respect to the source for drain-source current to flow. Some other RF devices, such as GaAs FETs, are depletion-mode devices and must be turned off by a negative bias like electron tubes.

While most designers are very familiar with bipolar transistor parameters, this isn't so for power MOSFET types. The table, *"Comparison of bipolar and power MOSFET DC parameters,"* explains the various MOSFET parameters and their importance to the designer, and relates them to bipolar parameters.

One important DC parameter not listed in the table is thermal stability. A MOSFET is almost always biased to some level of idle current, while the bipolar must be biased for linear operation. The forward voltage variations in a base-emitter junction are 1 to 2 mV/°C, and always have a negative temperature coefficient. Gate threshold voltage must be measured against a constant drain current and also has a negative coefficient at low current levels. However, the material bulk resistance of an FET has a positive coefficient, which becomes dominant at higher current levels. Thus, an FET's g_{FS} goes down as temperature goes up.

Stabilizing RF transistors

Looking at bipolar collector and MOSFET drain currents versus temperature at constant base and gate voltages (Fig. 2), it can be seen that the bipolar transistor has a negative coefficient up to high current levels but the FET "turns around" before the device dissipation rating is exceeded. Since these parameters are h_{FE}, g_{FS}, and current dependent, it is not easy to provide temperature stabilization for biased devices. For the bipolars, a forward-biased diode with suitable

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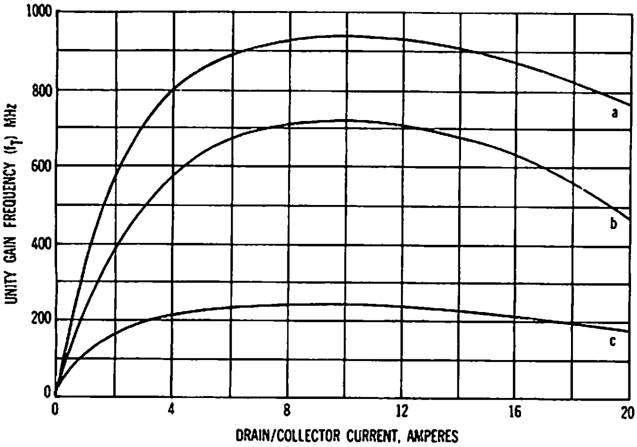

Fig. 1. Unity gain frequency versus I_c or I_b. Curve (a) represents a 150-W RF power MOSFET. Curve (c) is a bipolar having the same basic die geometry. Curve (b) is a standard switching power MOSFET with approximately equal gate periphery for comparison purposes.

characteristics kept at or near the transistor case temperature is usually considered a sufficient bias voltage source. In MOSFETs the required voltage can vary by several volts and the rate of change can be several times that of a bipolar at low drain currents. Thus, the FETs require more sophisticated methods for their temperature compensation. Resistor-thermistor combinations, together with regulators or op amps, are typical of these methods.

Despite the power MOSFET's parameter and cost-related drawbacks, its advantages still make it the choice over bipolars in certain applications. At VHF and UHF, the high gate-input impedance and the high power gain of the MOSFET make it possible to design broadband amplifiers with simpler input matching networks. Since the gate-source impedance remains capacitive to much higher frequencies, it makes internal matching networks unnecessary at least up to VHF even for devices of 100 to 150 W power ratings. On the other hand, VHF bipolar transistors with power ratings of 50 W and higher commonly employ internal matching networks, which means that the first section of the total network is built inside the device to transform the die impedance up to practical levels.

In general, at frequencies below VHF, the input and output matching for power FETs and bipolars are very similar. Only the network element values differ in most cases. At high frequency (2 to 90 MHz), where the configuration is mostly push-pull, ferrite broadband transformers or lumped-constant balanced LC transformers can be used depending on the exact requirements.

Amplifier circuit configurations such as common base (bipolar) and common drain (MOSFET) are also possible and practical. The common base circuit may be useful where more constant input impedance-versus-frequency or wider gain control range with gate voltage is required.

The MOSFETs common drain circuit configuration represents an emitter follower in bipolar circuits. Its specific merits are exceptional stability and linearity. However, these are attained at the cost of low power gain and at the danger of exceeding the V_g.

A MOSFET source follower cannot be considered as having current gain like an emitter follower. Rather, the amplification is achieved through impedance transformation. Note that the FET gate, which consists mostly of MOS capacitance, normally presents a high Q input to any matching network. This will impair the broadband performance and stability of the amplifier unless the Q is lowered by artificial means. A

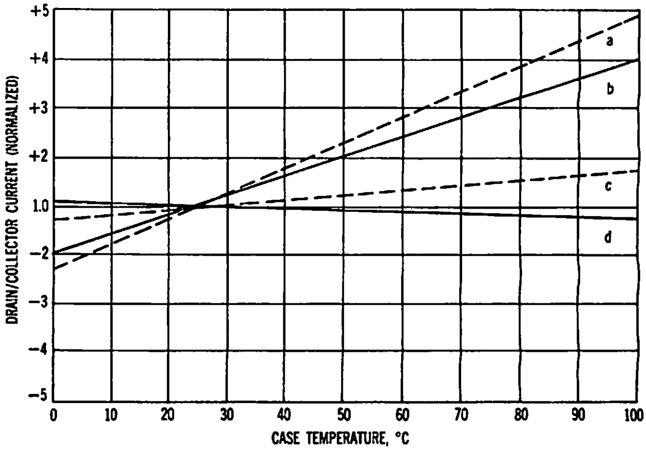

Fig. 2. Collector and drain idle current versus temperature at constant base or gate voltages. (a) and (c) represent a bipolar device at collector currents of 100 mA and 10 A respectively. (b) and (d) is a power MOSFET at drain currents of 100 mA and 10 A respectively.

gate shunt resistor, which can be part of the biasing circuit, serves this purpose.

A more sophisticated method of achieving broadband performance and stability is to employ negative feedback, which can be easily implemented only in the common source configuration. The feedback can be brought to the gate through an RLC network which, in combination with the shunt resistor, allows easier tailoring of the gain slope. In each case some power gain will be sacrificed, but this can be minimized at the high frequency end of the band (where the power gain is the lowest to begin with) by proper choice of component values in the feedback network.

The FET gate should never be connected to only inductive reactances in an attempt to use the inductance to control the gate Q. The C_{ISS} is highly drain-source voltage dependent and under certain conditions the total Q may be high enough to allow transients to exceed the V_g, thereby causing instant device failure.

Compare linearity and noise

It's commonly believed that power MOSFETs have more linear transfer characteristics than bipolars. This is only true if the FET is operated at a reduced power level and high bias (near or in class A). Based on two-tone linearity tests, the low order distortion products (3rd, 5th and 7th) fall faster with MOSFETs than with bipolars at reduced amplifier power outputs. However, FCC specifications are relaxed on low order distortion — −31 dB below the transmitter peak power — a figure easy to achieve with both types of transistors. It's when it comes to high-order distortion — 9th order and up — that MOSFETs are superior to bipolars (see Fig. 3).

High-order distortion causes disturbances to adjacent communication channels, whereas low-order distortion only relates to the quality of the modulation. High-order distortion results from phase nonlinearities between the input and output, from amplitude nonlinearities at low drive levels, and from

Comparison of bipolar and power MOSFET DC parameters

"Equivalent" Parameters

Bipolar	MOSFET	Description
BV_{CEO}	BV_{DSO}	Not specified or measurable with MOSFETs. In case of low gate-source leakage, the gate can charge to voltages exceeding the punch-through.
BV_{CES}	BV_{DSS}	Normal method of measuring the MOSFET breakdown voltage. It refers to the maximum drain to source voltage the FET is allowed with the gate DC biased or in the same potential as the source.
BV_{CBO}	BV_{DGO}	Not specified or measurable with MOSFETs. Gate-source rupture voltage would be exceeded in case of any drain-source leakage present.
BV_{EBO}	Vg	Not specified or measurable with MOSFETs unless done carefully at low current levels. Gate rupture can be compared to exceeding a capacitor's maximum voltage rating.
V_B (forward)	Vg(th)	Not specfied or necessary in most cases for BPTs. For a MOSFET, this parameter determines the turn-on gate voltage and must be known for biasing the device.
I_{CES}	I_{DSS}	Drain-source leakage current with gate shorted to source. BPT and FET parameters equal and normally only refer to wasted DC power and reliability.
I_{EBO}	I_{gt}	Normally not given in BPT data sheets, but important for MOSFETs for biasing purposes. Both affect their associated device's long term reliability.
$V_{CE(SAT)}$	$V_{DS(SAT)}$ or $R_{DS(ON)}$	Not usually given in BPT data sheets but important in certain applications. With power MOSFETs this parameter is of main importance. The numbers are assumably higher than with BPTs, and are material and die geometry dependent.
h_{FE}	g_{FS}	These are parameters for low frequency current and voltage gain, respectively. In a MOSFET the g_{FS} is more an indication of device electrical size and to a certain extent depends on processing.
f_T	(f_T)	Unity current or voltage gain frequency. Not given in many of the BPT or MOSFET data sheets. The figure can be two to five times higher for the MOSFET for an equivalent basic geometry and electrical size (see Fig. 1). The figure of merit of a MOSFET is usually considered as the ratio of the gate-source capacitance to the G_{FS}, but other parameters such as the R_{DS} (on) have some effect on the figure of merit.
G_{PE}	G_{PS}	Power gain in common emitter or common source configuration. This parameter is equal for both types of devices, except normally regarded as current gain for the BPT and voltage gain for the FET. At lower frequencies, where the FET gain is extremely high, the number may be merely an indication of how much stable and useable gain is available.
C_{IB}	C_{ISS}	Base to emitter or gate to source capacitance. Rarely given for BPTs. In RF power FETs the C_{ISS} has a larger effect on the gate-source impedance. In fact, if stray inductances from the die metal pattern, wire bonds, and package were absent, the gate impedance would be a pure capacitive reactance. The C_{ISS} consists mostly of die MOS capacitance, whereas the C_{IB} of BPT is a combination of MOS and diode junction capacitance. Since the diode(s) are forward biased during one half cycle and reverse biased during the other, it is obvious that the base impedance is largely drive level dependent.
C_{OB}	C_{OSS}	Collector to emitter or drain to source capacitance. Both are usually specified and are approximately equal in value for a given device rating and voltage Both are combinations of MOS and diode capacitances. Each effect the device efficiency since this capacitance must be charged and discharged at the rate of the operating frequency.
C_{RB}	C_{RSS}	Collector to base or drain to gate capacitance. Rarely specified for BPTs. Normally referred to as the feedback capacitance and very important for MOSFETs considering their lower gate-source capacitance and superior high frequency performance. At low frequencies C_{RSS} provides a 180° out of phase feedback to the gate, but can turn to positive feedback at high frequencies depending on stray inductances and the C_{ISS}. The results will be noticed as parasitic oscillations, unless C_{RSS} is low or the resonances fall outside the device's frequency capabilities.

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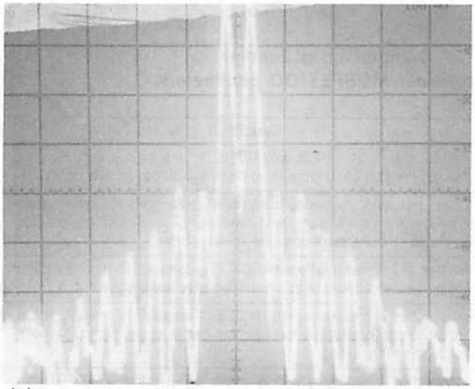

(a)

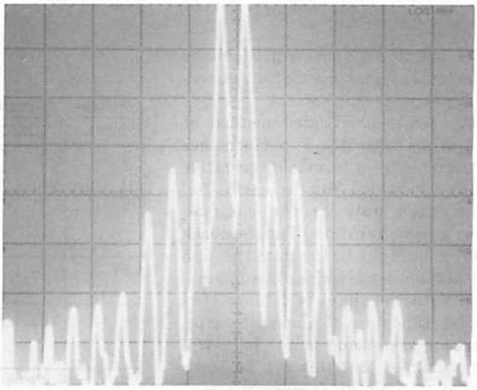

(b)

Fig. 3. Typical intermodulation distortion for a bipolar RF transistor (a) and for an RF power MOSFET (b). For the bipolar transistor, distortion products are visible up to the 15th order; for the MOSFET, 9th order and higher products are down in the noise.

nonlinear feedback. Most of the nonlinear phase and amplitude feedback in the bipolars is delivered through the emitters, which are coupled to the collectors through diodes and MOS capacitance. The emitter ballast resistors, although very low in value, allow enough feedback to the emitters to cause distortion. These ballast resistors in FETs are unnecessary, and the source is directly grounded. Thus, high-order distortion in a MOSFET is only possible through the C_{RSS}, which is very, very low.

Much like the high-order distortion in SSB communications, the broadband noise generated in any transmitter causes adjacent channel interference. The noise can be generated by the signal source, mixers, or any stage in the amplifier chain. The noise generated in the low level stages is amplified in all succeeding stages, and is of most concern. In linear amplifiers, where all stages are biased, the bias current alone can generate sufficient noise to block a nearby receiver. Both MOSFETs and bipolars generate thermal noise, which comes from the moving electrons. In addition, the forward-biased diode(s) in bipolars generate white noise, which is not present in MOSFETs. The two types of noise is usually measured together, and since a bipolar typically has about three times higher noise figure than a comparable FET, it appears that a majority of the noise generated comes from the base-emitter junction.

When higher current levels or higher amplifier power outputs are required than one semiconductor device can provide, paralleling devices is often the first thing that comes to mind. Bipolars are often paralleled at DC and low frequencies, where their balance can be assured with external ballast resistors. At RF, however, this technique can not be used due to excessive losses in power gain. Instead the devices must be closely matched. At VHF and UHF, where the base impedance is very low and mostly inductive in reactance, added inductance in the form of the interconnections would make the design of matching networks difficult. So, in practical designs, the low impedance of each device is transformed to a higher level, before the point where the parallel connection is made.

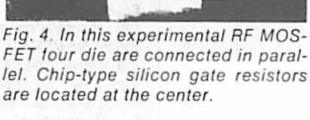


Fig. 4. In this experimental RF MOSFET four die are connected in parallel. Chip-type silicon gate resistors are located at the center.

The above problem is present with MOSFETs also, but they are more tolerant of gain mismatches because of the large amount of drain ballasting inherent in their structure. The MOSFET's higher, and capacitive, input impedance allows direct paralleling of higher power devices up to 150 to 200 MHz. However, a new problem arises when the MOSFETs are paralleled. When MOSFETs are paralleled directly, a multivibrator type oscillator is formed, in which the feedback is derived through the C_{RSS} and the time constant is the cross-coupled C_{ISS} plus wire bond and interconnect inductances in series. This may also occur when individual die are paralleled in the same package unless the C_{ISS} is low and the resonances fall outside the device limits. A commonly used cure for these parasitic oscillations is to de-Q all gates with series resistors (see Fig. 4) but this lowers the frequency response, making this technique impractical for truly high frequency applications. □

7

rf design feature

New MOSFETs Simplify High Power RF Amplifier Design

By H.O. Granberg
Motorola Semiconductor Products Inc.

There are many applications for high power solid state RF amplifiers in the 1 to 120 MHz range. Past designs have consisted of a number of 200-300 watt modules combined to produce power outputs in the multikilowatt level. Power combiners and splitters are expensive and difficult to design for extremely wide bandwidths, and at low frequencies are bulky as well. It is always desirable to combine as few modules for a given power output as possible, although system cooling becomes more difficult with thermal energy concentrated in a smaller area. There is obviously a practical limit to the point where this philosophy is valid.

Motorola has recently introduced high power MOSFETs MRF153 and MRF154, which are rated for 300 watt and 600 watt power output, respectively. A 600 watt bipolar transistor (MRF430) is also in this family of RF power devices. The MRF154, which is the subject of this article, is usable up to 100 MHz with a power gain of 8-10 dB. Special design techniques result in a junction to ambient thermal resistance as low as 0.13°C/w. The transistor housing is designed for conduction cooling, and has 1.4 square inch flange surface area. A mounting surface of high conductivity material such as copper is recommended, since up to 900 watts of power may be dissipated in each device. The heat dissipator itself can be forced air or liquid cooled.

The 1 kW push-pull amplifier described here is designed to cover a frequency range of 10 to 90 MHz. Its applications include military communications, jammer, low channel TV, etc. Although the point of saturation is well over 1000 watts, the amplifier was tested for linearity at 800 watts. The available output transformer impedance ratios (9:1 or 16:1) are the limiting factor: the 16:1 impedance ratio would be optimum at around 1500 watts power output, but the 9:1 was chosen in order to achieve a better overall CW efficiency at the 1 kW level. In pulsed applications such as Nuclear Magnetic Resonance, linear operation is possible up to 1000 watts per device due to the low average dissipation and lowered thermal limits. In such case the output impedance matching can be modified accordingly.

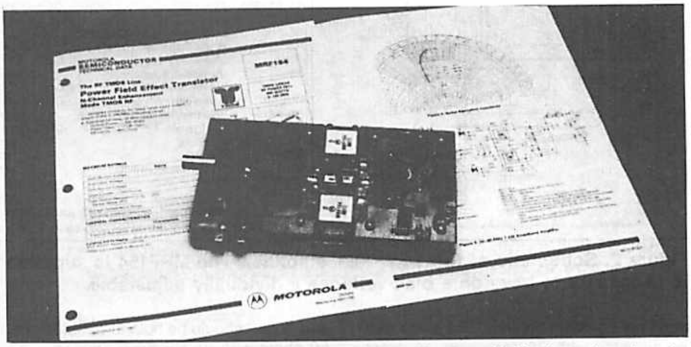
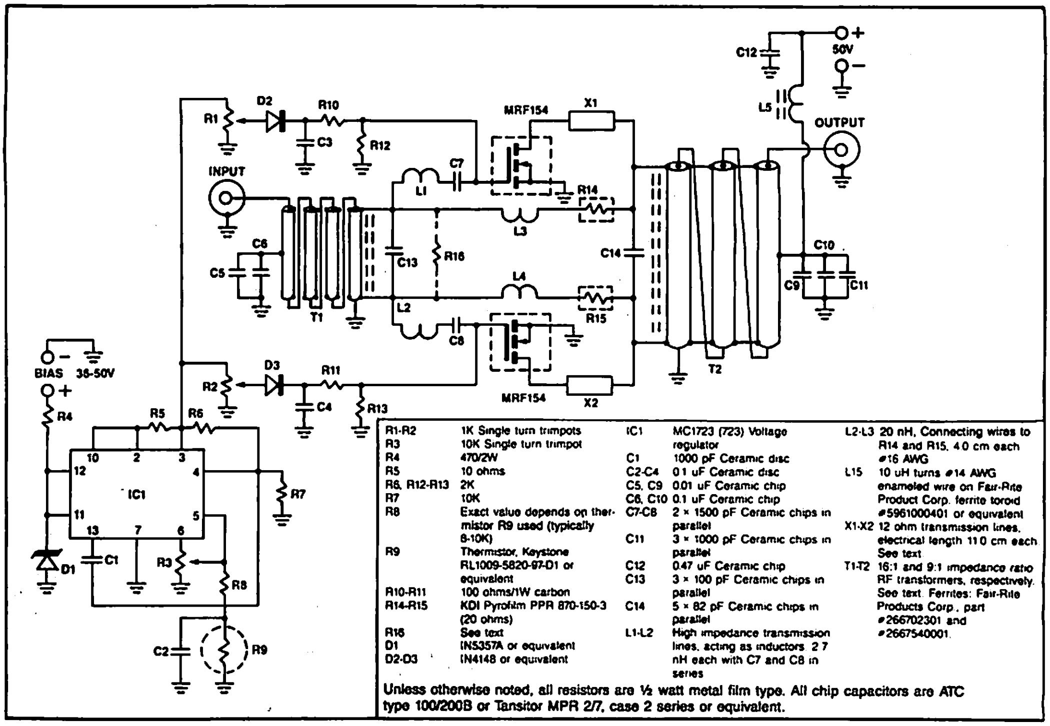


Figure 1. One kilowatt 10-90 MHz amplifier. The two FETs, input and output boards are mounted to a copper plate, which is then attached to the main heat sink.

Circuit Description

In contrast to a single ended amplifier circuit, in a push-pull configuration only the device mutual inductance (source to source in this case) is critical, and must be as low as possible for good high frequency performance. The common mode inductance (from each source to ground) is less important, reducing the requirement for low inductance grounding between the input and the output circuits. Input and output sections of the circuit board can be split and grounded only through metal spacers to the heat sink. The source of the MRF154 is internally connected to the mounting flange, which is also grounded to the heat sink. This provides a good, low inductance path between the two sources. The arrangement (Figure 1) results in a convenient and compact mechanical layout and makes the unit easily serviceable, since each board can be removed separately.

In addition to the matching network, the input circuit board includes the FET bias regulator, making the bias current insensitive to supply voltage variations. With the component values shown in Figure 2, excursions of 30 to 50 volts result in less than 1 percent changes in the bias current. The regulator also provides a convenient point for connecting a thermistor for bias current temperature tracking purposes. The thermistor must be of NTC type, and can be thermally connected to one of the FETs or to any central location at the heat sink, depending on the ther-



R1-R2	1K Single turn trimpots	IC1	MC1723 (723) Voltage regulator	L2-L3	20 nH, Connecting wires to R14 and R15, 4.0 cm each #16 AWG
R3	10K Single turn trimpot	C1	1000 pF Ceramic disc	L15	10 uH turns #14 AWG enameled wire on Fair-Rite Product Corp. ferrite toroid #5961000401 or equivalent
R4	470/2W	C2-C4	0.1 uF Ceramic disc	X1-X2	12 ohm transmission lines, electrical length 11.0 cm each. See text
R5	10 ohms	C5, C9	0.01 uF Ceramic chip	T1-T2	16:1 and 9:1 impedance ratio RF transformers, respectively. See text. Ferrites: Fair-Rite Products Corp., part #266702301 and #2667540001.
R6, R12-R13	2K	C6, C10	0.1 uF Ceramic chip		
R7	10K	C7-C8	2 × 1500 pF Ceramic chips in parallel		
R8	Exact value depends on thermistor R9 used (typically 8-10K)	C11	3 × 1000 pF Ceramic chips in parallel		
R9	Thermistor, Keystone RL1009-5820-97-D1 or equivalent	C12	0.47 uF Ceramic chip		
R10-R11	100 ohms/1W carbon	C13	3 × 100 pF Ceramic chips in parallel		
R14-R15	KDI Pyrofilm PPR 870-150-3 (20 ohms)	C14	5 × 82 pF Ceramic chips in parallel		
R16	See text	L1-L2	High impedance transmission lines, acting as inductors 2.7 nH each with C7 and C8 in series		
D1	IN5357A or equivalent				
D2-D3	IN4148 or equivalent				

Unless otherwise noted, all resistors are ½ watt metal film type. All chip capacitors are ATC type 100/200B or Tansitor MPR 2/7, case 2 series or equivalent.

Figure 2. Schematic of the 1 kW FET amplifier. The MRF154 is supplied in matched pairs for g_{FS} and gain. It is necessary to have gate bias voltages individually adjustable.

mal time constant desired. The slope can be adjusted with R8, for which the exact value is determined by the FET g_{FS}. The value shown typically results in bias current tracking of less than 20 percent for 25° to 75°C. The bias can be turned completely off by grounding R8. However, this cannot be used for high speed switching of the amplifier due to the limiting time constant of the FET input capacitances and the bias voltage source path. Since the bias voltages are individually adjustable with R1 and R2 in addition to a common adjustment R3, the FET gate threshold voltages do not need to be matched. The power gain of an FET is mainly dictated by the g_{FS} and not by the V_g(th).

The bias setting procedure is as follows: 1) adjust R1 and R2 to minimum; 2) adjust R3 for a voltage higher than the device V_g(th) at pin 3 of IC1. This should be typically 7-9 volts in order to place the R1 and R2 settings in the middle of the tuning range; 3) measure current at 50 volt supply point; 4) with power supply connected, advance R1 for desired current reading; 5) advance R2 until the current reading is doubled; 6) R1 and R2 need no adjustment after this, and the bias currents of both FETs can now be set with R3. During this operation (1-6) the input and output should be both terminated into 50 ohms with no RF drive applied.

On the output side of the circuit board design, the DC paths must be able to handle current levels of *50 amperes* and more, and the maximum RF currents are in the order of 15 amperes RMS at the low impedance points. The DC current would require almost 10^4 mils² for the conductor cross sectional area in free air, but since the conductor will be heat sunk to the circuit board surface, a number about one fourth of this is adequate. Even then, circuit board material with at least 2 ounces of copper is required, and should be solder plated for added conductor thickness. In regards to the skin effect, a certain foil thickness is also necessary for the conductors carrying the RF currents. The skin depth at the high frequency end (90 MHz) is about 0.40 mils, and the foil thickness in the RF conducting paths should be at least five times that, or 2.0 mils, according to a rule of thumb. Since the skin depth varies as an inverse function of the frequency, it is really only meaningful at high frequencies, where the dimensional conditions can be met. It is then desirable to have a conductor with a large surface area and a thickness that meets the minimum requirement. Normally this will also be sufficient for low frequencies, where the conductor losses become nearly purely resistive.

Input-Output Impedance Matching

Since the output impedance matching and transformer design are far more critical than the input side, they will be discussed first. According to (1) and (2) dips in transmission line transformer response will occur when the physical line length reaches ¼ wavelength, if the Z_o differs from the optimum required value or if the terminating impedances are incorrect. These dips, which actually are changes in the transformer impedance characteristics, have been noticed with ⅛ and 1/16 wavelength increments as well. Their magnitude also strongly relates to the amount of leakage inductance present, which has the same effect as an incorrect line impedance. Standard practice is to keep the line lengths as short as possible to reduce the IR losses, preferably shorter than ⅛ wavelength at the highest operating frequency. Although operation between the incremental frequencies is possible, the bandwidth would be limited to less than one octave.

The effective line length varies with the transformer configuration. In a balanced

4:1 as shown in Figure 3B, the two lines are electrically in series, making the effective line length twice the actual. Cascading these for 16:1 impedance ratio further doubles the effective line length, making the total four times the length of one line. In a 9:1 impedance ratio transformer (Figure 3A) the two lines *a* and *b* are electrically in parallel, making the effective line length equal to the length of one line. However, since a balun is required for the balanced to unbalanced function, its length must be added to the total.

In high power solid state RF amplifiers it is desirable to eliminate the need for output DC blocking capacitors. Even if they are located at the 50 ohm points, they must be able to handle large RF currents (4.5A at 1 kW) and should be chip type to minimize the series inductance. This can be done either by replacing the typical autotransformer configuration with a design as in Figure 3C, or replacing the balun with a 1:1 isolating transformer (Figure 3Ad and 3Dh). A disadvantage with 3D is that an impractically low characteristic impedance may be required for line *h*, but its high frequency performance is excellent due to the equal delay unbalanced 9:1 section.

The design shown in Figure 3C is probably the most practical one for its simplicity and ease of manufacture. It lends itself to high impedance ratios such as 16:1 and up, which would be difficult to implement with other types. The impedance transformation is achieved by parallel connection of one conductor of the lines and series connection of the other. In principle it resembles the multifilar type transformers described in references (3) and (4), and must be considered a conventional (non-transmission line) transformer, although the low impedance line provides most of the coupling between the primary and secondary at high frequencies. The line impedance is not defined in the same manner as in transmission line transformers, and is not as critical. For increased coupling and low IR losses it can be lowered to a point where the resonance of the line capacitance and the leakage inductance falls outside the highest frequency of operation.

As discussed earlier, the high frequency limit of an RF transformer is set by the physical length of the line or the winding on the high impedance side. Considering the ⅛ wavelength rule, mentioned in several of the references, the maximum total line length at 90 MHz would be:

$$\frac{\lambda}{8} \times V_p = \frac{333}{8} \times 0.63 = 26.2 \text{ cm.}$$

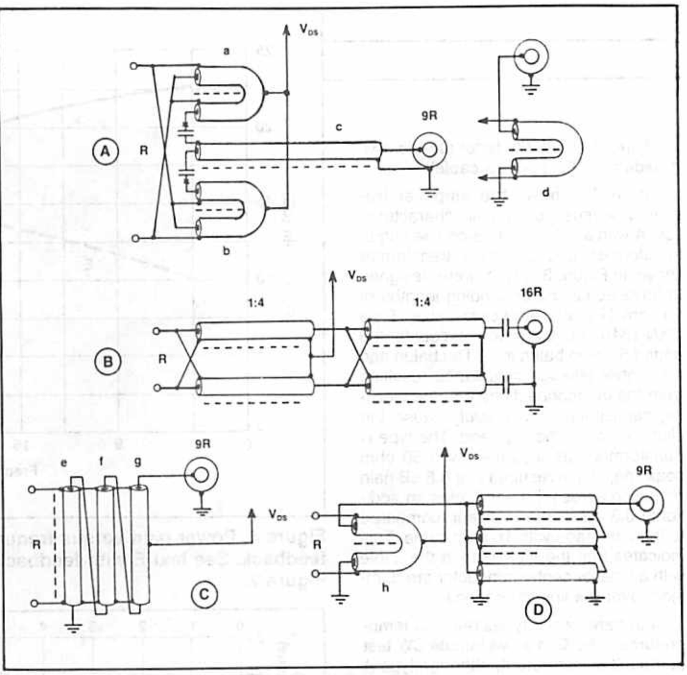


Figure 3. Wideband RF transformer configurations for balanced to unbalanced impedance matching at high power levels. Coaxial transmission lines are most convenient for compact physical designs.

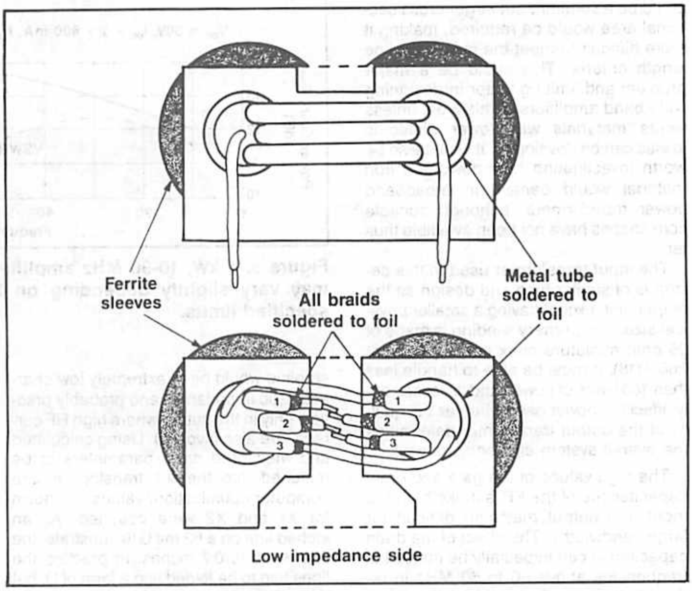


Figure 3E. Physical construction of RF transformers used in the amplifier. The electrical details are shown in Figure 3C.

Where: V_p = velocity factor (0.63 for low impedance TFE co-axial cable).

Figure 3E shows the amplifier frequency versus power gain characteristics, *A* with a 9:1 transmission line output transformer, and *C* with a transformer shown in Figure 3C. Both were designed to have equal line or winding lengths of 16 ohm TFE insulated coax cable (Type CXN 1848 W.L. Gore Co.), except for the added 50 ohm balun in *A*. The balun and the higher leakage inductance resulting from the interconnections and the blocking capacitors in *A* possibly cause the slight roll-off at the high end. The type *C* transformer was also tried with 50 ohm coax line, which resulted in a 0.8 dB gain reduction across the band, plus an additional 0.3 dB at the high end compared to the unit made with 16 ohm cable. This indicates that the IR losses in the cable with a smaller center conductor are dominant over the line impedance.

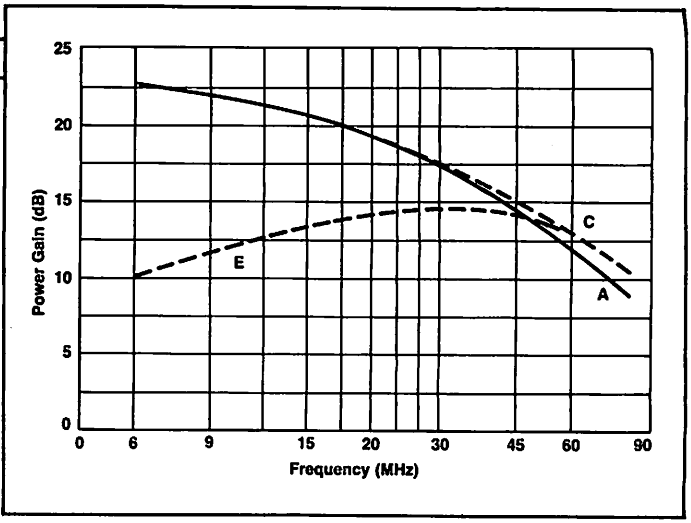


Figure 4. Power gain versus frequency A and C without negative feedback. See text E with feedback, component values as shown in Figure 2.

Both transformer types reached temperatures of 80°C in a five minute CW test at the full power output, although type *A* had twice the ferrite cross sectional area. This leads us to determine that the ferrite dielectric losses are a problem in high power and high frequency applications such as this. Lower permeability material could be a solution, but larger cross sectional area would be required, making it more difficult to meet the maximum line length criteria. This could be a major problem and limiting factor in designing wide band amplifiers of this type, unless ferrite materials with lower dielectric losses can be developed. It would also be worth investigating how powdered iron material would behave in broadband power transformers, although suitable core shapes have not been available thus far.

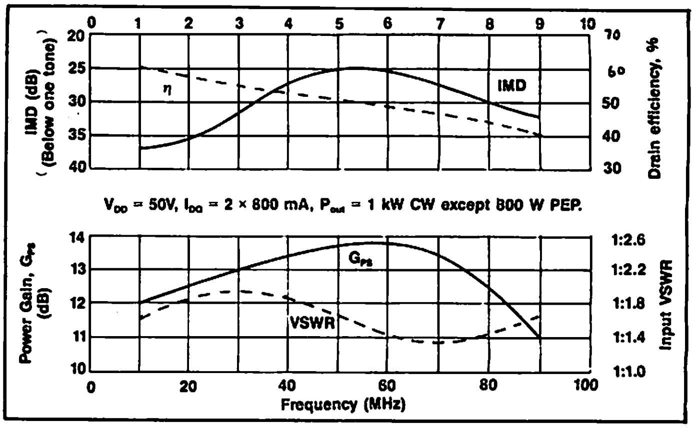


Figure 5. 1 kW, 10-90 MHz amplifier typical performance. The numbers may vary slightly depending on the exact device parameters within specified limits.

The input transformer used in this design is of similar type and design as the output unit, except having a smaller physical size. The primary winding is made of 25 ohm miniature coax cable (Microdot 260-4118). It must be able to handle less than 100 watts of power, and its losses only affect the power gain, whereas the quality of the output transformer determines the overall system efficiency as well.

The high values of the gate and drain capacitances of the FETs make both the input and output matching difficult for large bandwidths. The effect of the drain capacitance can especially be noticed at frequencies above 50 to 60 MHz in reduced efficiency. Part of this capacitance can be compensated for with small values of series inductance or stripline. The stripline would be of extremely low characteristic impedance, and probably practical only in the output where high RF currents are also involved. Using calculated and measured drain parameters to be matched into the 9:1 transformer and computer optimization, values as shown for X1 and X2 were obtained. As an etched line on a 62 mil G10 substrate, the line width is 0.7 inches. In practice the lines had to be folded into a form of U, but this allows part of the line to be conveniently shorted for adjustment purposes. The effect of the output lines can be noticed in increased efficiency at 90 MHz (6% to 8%), but at a cost of reduced power gain by approximately 0.5 dB.

Similarly, using the data sheet numbers converted to parallel form, indicated values for input lines L1 and L2 were obtained. They are high impedance etched lines on similar G10 substrate. They act as inductors and their values are also adjustable by shorting part of the line or by moving the input transformer connection points. The values of L1 and L2 will finally depend on the amount of negative feedback necessary for the desired gain slope.

Although not adapted to this design, a dummy resistor (R16) can be used to make the input look more resistive and improve the input VSWR. A suitable amount of L in series with it, combined with negative feedback, is a common technique in applications requiring extremely large bandwidths.

Gain Leveling with Negative Feedback

The negative feedback term usually refers to a condition where part of the output power (voltage) is fed back to the input out of phase. Out of phase generally means 180° phase difference, although in practical systems the voltage fed back usually lags the input voltage due to delays in the circuitry. Any inductance in the feedback path causes a delay and a phase error, but seldom has effects large enough to cause instability. Sometimes an amount of inductance is intentionally included in the feedback circuit in order to prevent the feedback from affecting the high end. In most circuit configurations the phase shift is close to 180° between the input and the output, in which case the feedback is easy to implement. Otherwise a phase reversing component, such as a transformer must be employed.

Here the series inductances L3 and L4 are limited to their minimum values of 20-25 nH by the physical distance between the input and the output, although they can be controlled to a degree by varying the conductor diameter. Their reactances are about 8 ohms at the mid-band, where lower values would result in increased feedback and a flatter gain response than shown in Figure 5. It must be noted that the reactances at 10 MHz may be also significant, and should be deducted from the values of R_{fb} to be calculated.

In addition to gain reduction, negative feedback lowers the effective input impedance. Ideally the amount of feedback voltage should be inversely proportional to the frequency in such amplitude that *the gain would be reduced just the correct* amount at all frequencies below the high end. This is not possible with simple feedback networks consisting only of L and R. Even with more sophisticated networks the feedback voltage source should be adjustable in some manner. Such a system is described in (6), but due to the high frequencies and higher power level involved it would be difficult to implement in this design. Here the feedback voltage is derived directly from the FET drains, which will limit the optimization of the system in this respect.

The MRF 154 data sheet shows a power gain of 22 dB for the device at 10 MHz, and a one to four difference in the gate input impedance from 10 to 90 MHz, or 12 ohms and 3 ohms composite parallel, respectively, from gate to gate. The 22 dB

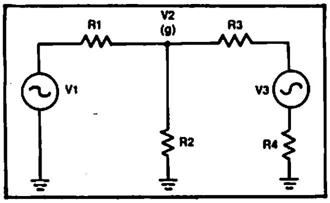


Figure 6. A simplified model of the negative feedback network can be used to figure the loop parameters with sufficient accuracy.

can be considered typical, and can vary as much as 3 dB at 30 MHz. However, the devices are supplied in matched pairs for operation in push-pull systems. The 22 dB translates to a power input of 6.5 watts for two devices at 1 kW output. Assuming a 10 dB gain reduction, the power input then would be 65 watts. Since the device power gain is not affected by the feedback and part of the input power is cancelled by the feedback voltage, the difference power must be dissipated somewhere. Most of this occurs in the feedback resistors, which also control the amount of feedback.

A 16:1 impedance ratio input transformer was selected with an idea in mind that the feedback would bring the low frequency gate to gate impedance down to the 90 MHz value (3 ohms). Because of the reasons discussed ahead, the gain slope cannot be controlled, and since no loss of gain in the high end can be afforded the feedback is limited to an amount that results in a low VSWR at 10 MHz. The computer analysis of the input matching mentioned earlier assumed a constant 3 ohm impedance, but this will deviate considerably at the mid-band. A computer program with all these variables would be very complex, and since the system could not be totally optimized anyway it was decided to discard the effort at this point.

Since an FET is a voltage-controlled device, the feedback loop can be modeled at low frequencies or DC as shown in Figure 6, where:

R1 = Transformer source impedance
R2 = FET gate to gate impedance
R3 = Feedback resistor. (Divided into two equal values in the amplifier.)
V1 = input voltage
V2 = FET gate to gate voltage
V3 = Drain to drain output voltage across R4

For a given level of power output, the values of R1, V2 and V3 will remain virtually unchanged regardless of the amount of feedback.

It is assumed for simplification, that the value of R2 will be reduced by the feedback from 12 ohms to equal R1. Then:

R1, R2 = 3.12 ohms.
V1 = 14.23 volts (−10 dB)
V2 = 4.5 volts (22 dB)
V3 = −74.2 volts (R4 = 5.5 ohms)

$$R3 = \frac{(V2 + V3)}{\left(\frac{V1 - V2}{R1}\right) - \left(\frac{V2}{R2}\right)} - R4 =$$

$$\frac{(4.5 + 74.2)}{\left(\frac{14.23 - 4.5}{3.12}\right) - \left(\frac{4.5}{3.12}\right)} - 5.5 =$$

$$\frac{78.7}{1.70} - 5.5 = 40.8 \text{ ohms}$$

or 20.4 ohms each.

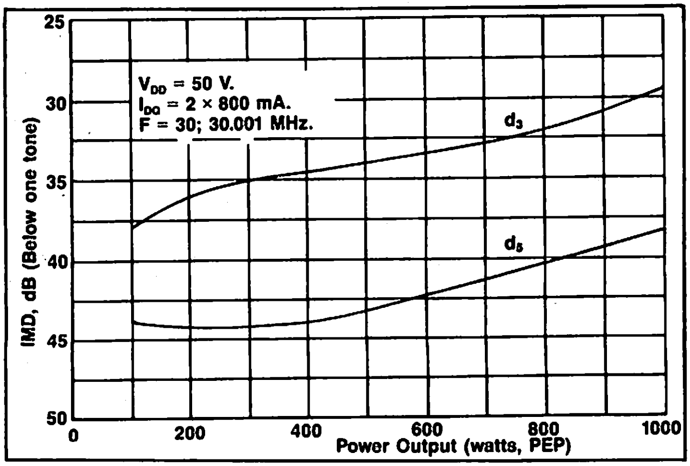


Figure 7. Intermodulation distortion versus power output of 1 kW amplifier. Output impedance matching is optimum only at 800 watts with the transformer impedance ratio employed.

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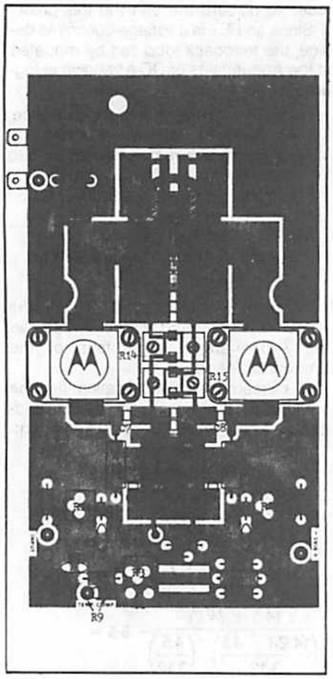

Figure 8a. Component layout.

The feedback resistors then must be able to dissipate 65-6.5 watts plus any excess power resulting from the non-optimum voltage source. In this case the dissipation is $78.7 \times 1.70 = 133.8$ watts, or 66.9 watts per resistor. It is obvious that they must be of a type with a provision for heat sinking, and with low parasitic inductance (8).

Design and Construction Summary

The amplifier performance, shown in Figures 5 and 7 can be affected by circuit parameters such as type of components, their values and exact locations. In this respect, it can be compared to a low power UHF design if the impedance levels are scaled down with frequency. Although the layout resembles that of a typical 2 to 30 MHz amplifier, considerable differences in the construction techniques are essential to ensure proper operation, especially at the high frequencies.

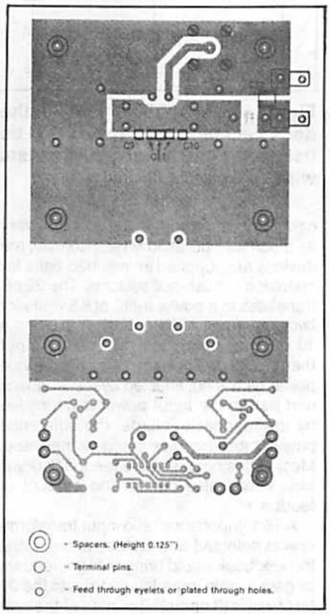

Figure 8(b). Underside of p.c. board.

Due to the high gate capacitance (C_{iss}) of the devices, the input matching is critical for good broadband performance. The values of L1 and L2, as well as the physical locations of T1 and C13, have a dominant effect in the input VSWR. The above is also true concerning the output matching, where these variables affect the power gain, efficiency, saturated power, and the IM distortion. Special attention must be paid to the location and quality of C14, which is essential to the amplifier operation above 50 MHz. Once all these criteria have been established, duplication of the system should not be a problem, although it is not possible to give physical details with sufficient accuracy in an article of this proportion to guarantee the exact results without minor adjustments.

The RF currents associated with the high power level and low impedances also introduce new problems to the designer in the form of passive components. The weakest link probably is the capacitors, which in certain locations must be composed of several paralleled smaller values in order to achieve the current carrying capability required and reduce the series inductance. Other limitations associated with the passive components have been discussed earlier. One of these is the circuit board itself, where the DC currents and the skin effect place a minimum limit to the foil thickness.

The low impedance levels are not new to a solid state power designer, but their association with a kW power level in a single amplifier is unique at these frequencies. This places new requirements on all passive components and presents challenges in thermal design.

Finally, it must be pointed out that the component values given or the mechanical design may not be exactly optimum for the specific goals described. The intent was to make the circuit board layout, including the output section, as universal as possible to allow its use for designs with other devices and frequency ranges. rf

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About the Author

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DESIGN FEATURE

BUILDING PUSH-PULL, MULTIOCTAVE, VHF POWER AMPLIFIERS

By choosing the right feedback network and wide-band transformers, users will have a powerful amp.

TWIN FET packages are the heart of a unique, push-pull 300-W power amplifier. With a 50-V power supply, this broadband amplifier is easy to implement, and has excellent impedance-matching characteristics and low DC-current levels.

Applications include low-band and VHF communications base stations, FM broadcast, low-band TV, and certain medical uses. For these uses, a frequency coverage of at least 10 to 175 MHz is required. However, for a particular application, the required bandwidth can be narrowed for increased circuit efficiency.

The development of high-power VHF/UHF power FETs make the amplifier possible. These FETs have recently become available in a push-pull package configuration—commonly called the Gemini. A push-pull Gemini package is a flange-mounted transistor header capable of accommodating two individual transistors—either FETs or bipolars. One of the three transistor electrodes is connected to the normally grounded flange.

On first observation, it seems that a push-pull header would not be as advantageous as separate headers for each transistor. Separate headers provide better thermal distribution, improved circuit design and layout versatility, and higher production yields. The result is lower cost per watt of output power.

In addition, operating parameters of the two transistors in a push-pull header must be closely matched before assembly. If there is even the slightest mismatch in any of the several DC parameters, the device must be rejected. Another drawback of the push-pull header is that the adjacent-transistor configuration results in reduced thermal ratings, leading to a decrease in electrical ruggedness.

But there are important advan-

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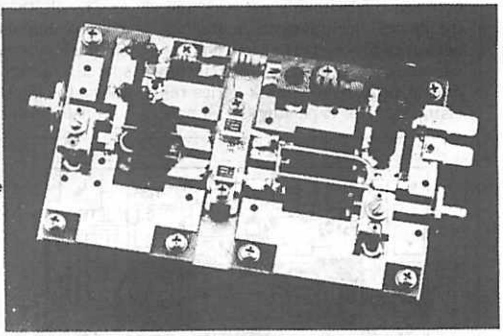
Transformer characteristics

Frequency (MHz)	R_P (Ω)	X_P (Ω)
10	12.85	+J30
30	12.20	+J58
50	11.90	+J95
100	10.20	+J150
175	8.70	+J9.60



1. For this high-power VHF amplifier, separate circuit boards are used for the input and output. The magnetic core has been removed from the output transformer for clarity. Note the thermistor (upper middle) attached to one end of the transistor flange.

DESIGN FEATURE

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tages to the push-pull design. For example, the power gain performance of this design is difficult to duplicate in single-ended configurations because power gain is directly related to the emitter- or source-to-ground inductance. Also, in push-pull designs, the common-mode inductance is completely insignificant; mutual inductance between each emitter, or source, becomes the critical factor. This mutual inductance is much easier to control and minimize.

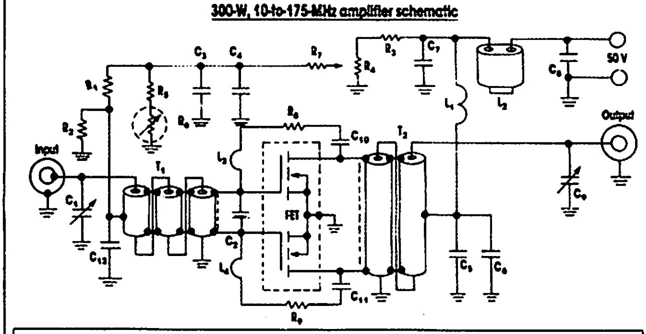
There are several different design approaches that can be used for solid-state power amplifiers. A transformer-based push-pull design is the best approach for multioctave devices, but such circuits are not easily implemented for frequency ranges higher than 50 to 100 MHz. If transformers are used, their locations and connecting points, as well as the locations of any associated capacitances, are extremely critical. These parameters must be tightly controlled.

Control of input and output impedances to the matching networks is also required. These impedances must be kept constant over the entire operating range. Internal impedances—which are directly proportional to the frequency—cannot be easily adjusted. However, some designs mitigate the effect of this frequency-dependent internal impedance. These practices include inserting special correcting elements between the matching network and the device, designing the matching networks for the proper impedance-versus-frequency slope, and introducing negative-feedback series resistor-inductor-capacitor (RLC) networks for controlling the feedback over the desired frequency band. Often, the negative-feedback technique is used with special, correcting-element techniques.

Negative feedback is the output voltage returned to the input at 180 deg. out of phase. In series RLC networks, the series resistor limits the overall amount of feedback voltage and also lowers the Q of the inductor. The capacitance is mostly used for DC blocking.

With these networks, the series inductive reactance results in phase lag. This phase lag is maximum at high frequencies, where the effect of the negative feedback is the least. As a result, the out-of-phase voltage must be obtained from either side of the push-pull circuit—or through a specially designed network—which allows the impedance of the voltage source to be optimized.

300-W, 10-to-175-MHz amplifier schematic



R_1 = 1 kΩ—1/2 W
R_2 = 1.5 kΩ—1/2 W
R_3 = 1.5 kΩ—2 W
R_4 = 1-kΩ trimpot
R_5 = 6.8 - 8.2 kΩ—1/4 W (depends on FET g_{FS})
R_6 = Thermistor—10 kΩ at 25°C; 2.5 kΩ at 75°C
R_7 = 2 kΩ—1/2 W
R_8, R_9 = 50-Ω power resistor—EMC Technology type 5310, or KDI Pyrofilm type PPR 515-20-3
C_1, C_9 = 8 - 60 pF, ARCO 404 or the equivalent
C_2 = 150-pF ceramic chip
C_3, C_{10}, C_{11} = 0.1-μF ceramic chip
C_4, C_5, C_{12} = 1000-pF ceramic chip
C_6, C_7 = 5000-pF ceramic chip
C_8 = 0.47-μF ceramic chip, or lower values in parallel to reach the value indicated
L_1 = 10 turn, AWG #16 gage enameled wire, 5-mm inside diameter
L_2 = Ferrite beads, 1.5-μH total
L_3, L_4 = Lead lengths of R_8 and R_9, 20-mm total
T_1 = 9:1 RF transformer—25 Ω, 0.062-in. outside diameter, semirigid coax
T_2 = 1:4 RF transformer—25 Ω, 0.090-in. outside diameter, semirigid coax
FET = MRF151G
Notes: For T_1, two type 75-26 E and I Micrometals powdered iron cores are required.
For T_2, three type 100-8 E and I Micrometals powdered iron cores are required.
All chip capacitors of 5000 pF or less are ATC type 100 or equivalent.

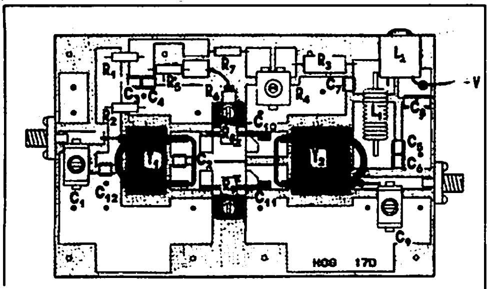
2. At the heart of the 300-W amplifier is the Gemini push-pull transistor configuration. This broadband amplifier operates in the 10-to-175-MHz range.

A resistive network eliminates the reduced efficiency of the feedback power. This power is dissipated in the series resistor. Power loss can be considerable—up to 15 percent at the low end of the spectrum—where the feedback is highest.

Another factor in negative-feedback system design is that the out-of-phase feedback voltage must be injected after the input-matching network. This will not affect the device input impedance, but will lower the load impedance to the input-matching network. Also, there will be an additional load to the device output at low frequencies, where the output impedance is higher and less reactive.

In addition to the correct use of negative feedback, the basis for good, multioctave, RF power-amplifier design is well-designed wideband transformers and correct matching elements. With proper design, this combination yields a low-input circuit VSWR over many octaves and results in a system with level power output.

Proper push-pull design requires a noncritical, source-to-ground inductance that provides a DC current path. This allows the circuit board to be split into two sections: an input



3. Building the amplifier is easy using this component layout.

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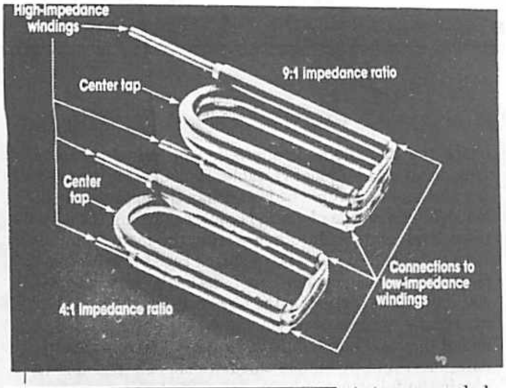

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and an output board (Fig. 1). The input section carries the input-matching network and part of the gate-bias circuit.

The first parts of the bias circuit—the output matching network and the drain-source voltage (V_{DS}) filtering and bypassing components—are mounted on the output board. This configuration allows each board to be changed independently for matching-network modifications or for other purposes. Furthermore, the input matching is almost identical for a 28-V power-supply counterpart, requiring the change of only one chip capacitor and the output board (Fig. 2).

Component locations can be seen in Fig. 3. The board material is G10, which is adequate for frequency ranges as high as 200 to 250 MHz, especially since no high-Q elements are incorporated. For a two-sided board, the lower side is a continuous ground plane, although not necessarily in all locations. This means that no through-holes are provided for components such as resistors, trimpots, and inductors. These components—as well as chip capacitors and wideband transformers—must be surface-mountable. The total number of feedthroughs to the bottom ground plane is 16.

Gate-bias voltage is obtained from the main DC supply voltage through two voltage dividers. The first divider includes a trimpot for the bias adjustment. The second divider accommodates a thermistor-resistor combination (R_5, R_6) for temperature stabilization of FET biases. Without this stabilization, the drain idle current would have an approximate temperature coefficient of +15 mA/°C. With this temperature coefficient, idle current would increase by a factor of three if the case temperature was doubled.

The FET and circuit boards are mounted on a milled copper plate, measuring 115 × 75 × 6 mm. Input/output SMA-type connectors are mounted at the end of this plate. The result is a self-contained, single structure that can be fastened to a properly cooled heatsink. In laboratory tests, the copper plate—called the heat spreader—was pressed against an air-cooled heatsink by its own weight with a thermal compound interface. The V_{DS} feed circuitry consists of standard high- and low-frequency filtering and bypassing. In Fig. 2, it is clear that components L_1 and C_7 handle the high-frequency end; the low-frequency end is handled by the L_2, C_8 components.

Normally it is desirable to filter down to very low frequencies to prevent any RF energy from feeding back to the power supply, in case of load mismatches and instabilities. But this type of filtering applies primarily to single-ended circuits. In push-pull circuits, the DC feed is usually at a balanced point, with no RF potential. In this push-pull circuit, such an elaborate filtering network is not necessary, except when partially damaged devices cause excessive unbalances between the two sides.

4. Correct construction of the wideband transformers makes the amplifier work properly.

IMPEDANCE MATCHING

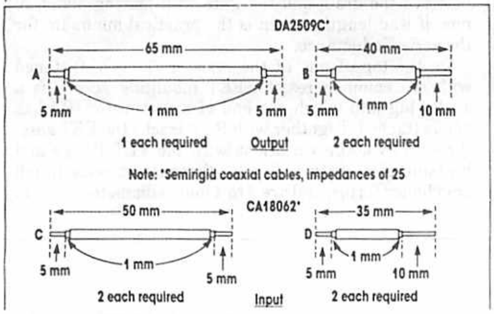
Input- and output-impedance matching is done with unique wideband transformers (Figs. 4 and 5).[1] Advantages of using these transformers include DC isolation between the primary and secondary turns, automatic balanced-to-unbalanced functions, and compact size vis-a-vis the power-handling capability. The principle is the same as in ordinary low-frequency transformers. However, the tight coupling coefficient is achieved between the transformers' windings by the use of a low-impedance transmission line, in this case, semirigid coaxial cable.

The low-impedance side always has one turn, and consists of parallel, connected segments of the coax outer conductor. The high-impedance side has inner conductor segments that are connected in series. This arrangement permits only integer impedance ratios that are perfect squares, such as 1, 4, 9, and 16. The coupling coefficient between the primary and secondary turns can be controlled by varying the coax impedance. The optimum line impedance formula, Eq. 1, also applies to the transmission-line transformers:

$$Z_0 = \sqrt{R_L(R)}^{1/2} \quad (1)$$

High line impedance results in loss of high frequency response, whereas a very low impedance would further lower the R_P at the middle frequencies (see table).

There is a trade-off between the cable diameter and the length of the board. Depending on where the lines



5. Semirigid coaxial cables are bent and formed to produce the wideband transformers. The outer conductors are soldered together. The inner conductor of all segments are sharply bent inwards against each other.

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are stacked, using large-diameter cable results in less-definable connection points to the low-impedance winding. This results in an increased leakage inductance. The areas of the coax inner conductor—where the winding series connections are made—are uncontrollable and contribute to the leakage inductance.

In an optimum configuration, the low-impedance winding connection points should be brought together as close as possible. This minimizes the lengths of the uncovered inner-conductor segments, but the physical format would be difficult to accomplish.

The optimum value for the R_P would be exactly 12.5 Ω, with a high value for the X_P. In fact, if X_P is equal to, or greater than, the high-impedance termination, it can be omitted. Then, only the R_P becomes the determining factor. The worst case is at 100 MHz, at which the R_P is low and the X_P is high (see table).

This means the transformer ratio is greater than 1:4 at that frequency, resulting in a dip in the drain efficiency. It is the result of the leakage inductance and can be observed at frequencies as low as 50 MHz. The compensation capacitor, C_9, is optimized at 175 MHz, but its influence diminishes at 130 to 150 MHz. Despite all of this, the overall performance of the transformer was considered satisfactory.

Variations of the output impedance with frequency, compared to those of the input, are usually several times smaller. Therefore, impedance-sloping networks are rarely seen. Such networks should be able to handle high RF currents and voltages and would be difficult to design with low losses. Negative feedback, however, tends to present an artificial load to the device output and it can be designed to decrease with frequency.

The parallel, equivalent gate-to-gate input impedance of the push-pull network is 1.28 – J 3.12 Ω at 175 MHz, making the normalized impedance value equal to 3.37 Ω. At 10 MHz, the normalized impedance would be 15.7 Ω. At 175 MHz, a 16:1 impedance ratio would result in a closer input-impedance match, but it was decided that a 9:1 ratio would provide a closer match at lower frequencies. The high end can be corrected with an adjustment of C_1 and C_2. At 10 MHz, the input transformer would see a 15.7 Ω load, which represents a VSWR of almost 5:1.

Therefore, if no correction network or feedback is employed, negative feedback will level the power gain as well. But, with simple RLC networks, only the high- and low-frequency ends can be equalized, leaving a "hump" at the middle frequencies. In most cases, this hump is only 2 to 3 dB—tolerable for most applications. The series resistor should lower the Q of the inductor. But real optimization requires a variable source for the feedback voltage.[1] The feedback resistor values can also be calculated.[2]

A simplified model of the feedback network can be seen in Fig. 6. Only the series inductor, which is used to shape the gain slope, is omitted. This inductor can be treated as an additional variable. Its value for the spectrum in question would be lower than the minimum limit achievable with the physical layout, regarding the minimum lead lengths. In other words, the model only allows the calculation of the feedback resistor values at a single frequency. In most instances, the minimum series inductor is limited by the physical size of the circuitry. Ideally, its reactance should be infinite at the high end of the band and should be zero at 10 MHz. From the data sheet and by simple calculations, it is possible to obtain the following values:

- G_{PS} at 10 MHz = 26 dB.
- G_{PS} at 175 MHz = 16 dB (lowered to 15 dB with feedback).
- P_{in} 1 (f = 10 MHz, P_{out} = 300 W) = 0.75 W, V_{in} (RMS) = 2.03V (V_2).
- P_{in} 2 (f = 175 MHz, P_{out} = 300 W) = 9.50 W, V_{in} (RMS) = 7.23V (V_1).
- V_3 = RMS output voltage (drain to drain) = –61.25 V.
- R_1, R_2 (transformer source and gate-to-gate impedances) = 5.5 Ω.
- R_3 = feedback resistor.
- R_4 (output load) = 12.5 Ω.

The value of the feedback resistor is given by:

$$R_3 = \frac{V_2 + V_3}{\left[\left(\frac{V_1 - V_2}{R_1}\right) - \left(\frac{V_2}{R_2}\right)\right]} - R_4$$

$$= 48.3\ \Omega \text{ (each resistor)} \qquad (2)$$

Total power dissipated (R_8 and R_9) = 63.28 × 0.58 = 36.70 W, or 18.35 W per resistor. The values can be rounded to 50 Ω, allowing the use of stock resistors. The resistors used here are rated for 25 W. They have a one-sided flange for heatsinking purposes, which is mounted on 6.35-×-6.35-×-4-mm-high copper blocks in each end of the FET. Holes are provided through the blocks, and common screws are used to mount the resistors and the FET.

The purpose of the copper blocks is to conduct the heat away from the resistors to the heatsink through the ends of the FET flange and to raise their height to more than the top surface of the ceramic lids of the FET, allowing the resistors to be mounted directly on top of each lid. This design provides the shortest path between the drain and the gate, still leaving about 20 mm of lead length, which is the practical minimum for the series inductance.

On the top of one of the resistor flanges, fastened with the common resistor-FET mounting screw, is a solder lug into which one end of a thermistor (R_6) has been attached. Together with R_5, it tracks the FET gate-threshold voltage variations with the FET flange and heatsink temperature. Similar thermistors come in pill or cylinder forms, and are 3 to 4 mm in diameter and 4 to

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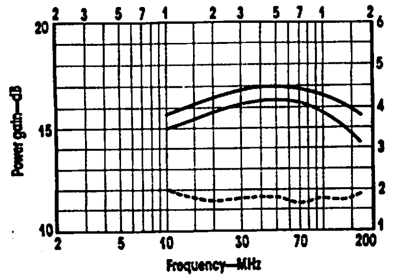
5 mm long. Normally they have wires soldered to each end, of which one was removed and replaced with the solder lug. The lug is the electrical contact to the ground and the thermal contact to the heatsink. Thermistors with similar mounting may be commercially available.

Since the output-load impedance is fixed and set for a nominal 12.5 Ω, the optimum supply voltage would be approximately 45 V for the best combination of drain efficiency and saturated power. If good linearity is required, higher voltage will give better results. In most applications, such as single sideband (where the duty cycle is low), the efficiency is less important. Other factors that affect efficiency are the amount and type of magnetic material in the output transformer, the amount of negative feedback introduced, and the magnitude of drain idle current.

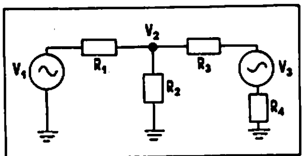
It would be difficult to design an amplifier covering the 1-to-175-MHz range in one segment, since highly permeable magnetic material is excessively lossy at VHF. Transmission-line transformers would allow multiturn windings and the use of material with lower permeability, but could easily lead to excessive *physical line length.* For extremely broadband designs, a low overall efficiency must be accepted, as well as reduced power output from the specified device values. In such cases, efficiencies of 40 to 45 percent are typical.

However, if the band is split into segments such as 1 to 75 MHz and 75 to 175 MHz, magnetic material in the output transformer is not required for the high segment, resulting in 10-to-15-percent higher efficiency. Amplifiers, for even narrower bandwidths such as the 88-to-108-MHz FM broadcast band, have been designed with efficiencies up to 70 percent using the same devices and design technique.

Some power is absorbed by the feedback networks at the high end of the band as a result of the finite reactance of the series inductances.



7. Input VSWR is effectively constant. However, the choice of transformer core material can change VSWR performance.



6. A negative-feedback network plays an important role in the amplifier's operation. Design of this DC model is based on a series RLC circuit.

The reactance decreases in proportion with the frequency and reaches its minimum value at the lowest frequency of operation, which is where maximum power loss due to feedback occurs. The numbers previously determined from the feedback resistor calculations permits a determination: The power loss is P_{in} 2 − P_{in} 1 + 36.7 W = 45.45 W, which converts to 7.5 percent, assuming 50-percent initial efficiency.

Linear amplifiers usually operate at a lower efficiency than amplifiers designed for CW or FM service. For good linearity, the output-matching network is designed for a higher transform ratio than that which is optimum for efficiency, which also results in higher saturated power output. Linearity is affected by the amount of quiescent idle current as well, of which a certain amount is always required. In a FET amplifier, going from class B to class C has a larger effect on efficiency than in a bipolar design, since the gate-threshold voltage is usually higher than the base-emitter forward voltage. Zero gate voltage would lower the amplifier's power gain, but would also increase its efficiency by more than that accounted for by the idle current, and could actually be thought of as setting the operating point closer to class D.

Stability is a concern with all solid-state amplifiers. It is easier to achieve with FETs than bipolar transistors, mainly due to a higher ratio of feedback capacitance to input impedance. The "half f_0 oscillation" phenomenon is unknown with FETs, since the nonlinear diode junctions are not present. However, at low frequencies the FET input impedance is almost a pure capacitance with high reactance, resulting in extremely high power gain. If the FET gate is not properly terminated due to input mismatches, low-frequency instabilities may take place—especially if the frequency response of the input circuit is low enough to sustain the activity.

For push-pull RF FET amplifiers, the two gates must have sufficient isolation between each other at the frequency at which the device internal capacitances, wirebond inductances, and external inductances resonate. If the gate inductance is low compared to the device's internal inductances, oscillations at the resonant frequency will occur.[3-5]

Depending on the exact conditions and device type, relatively low-level parasitic oscillations can occur; in worst-case scenarios, a latching-type condition will destroy the FET instantly. This can be prevented by lowering the Q of the resonant circuit with series resistance or inductance at the gates. Unfortunately, this seriously affects the high frequency performance of the amplifier. A more practical solution is simply to load the input transformer itself with magnetic material, which in this design is required to extend the frequency response down to 10 MHz in any case, and would be required for any amplifier of this type regardless of the frequency range.

The input VSWR can be optimized for lower frequencies by increasing the value of C_2 and adjusting C_1 (Fig. 2). The optimum value for C_2 at 150 MHz is approximately 180 pF.

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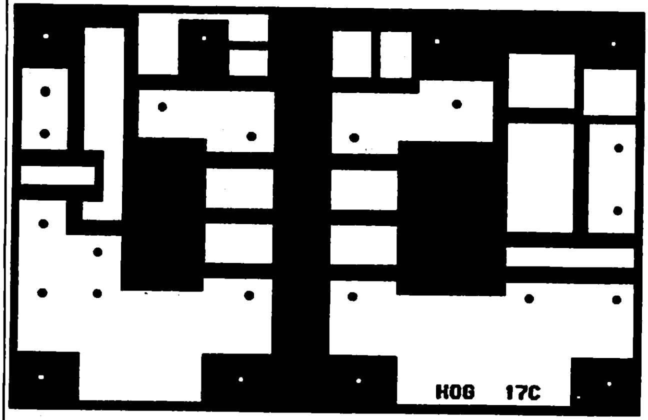
Its location, which is critical, should be inside T_1 (Fig. 3). The C_2 capacitor should be soldered in place before the mounting of T_1. Some designers allow a fair amount of input reflected power at low frequencies to compensate for excessive power gain. However, this may result in instabilities with the driver, unless biased into class A.

In this design, the input and output magnetic cores are heatsunk to the copper heat spreader. In the case of E- and I-type cores, the I section is pressed flat against the heat spreader, and the E section is cemented to it through a rectangular opening in the circuit board. Since the cemented joints have high thermal resistance, this is not a perfect way to remove the heat from the core, but it lowers the temperature by 20 to 30°C from no cooling at all. Cooling is only necessary for certain types of ferrites with low Curie points. The powdered iron transformer core does not have a Curie point in that sense and can be operated at high temperatures without changes in its magnetic properties.

The efficiency is lowest with full bandwidth and high supply voltage. Although the data was taken under CW conditions, continuous operation of the unit is not recommended, except with reduced duty cycle such as SSB or linear pulse. For applications above 50 to 70 MHz, it is recommended that no magnetic material is inserted in T_2 (Fig. 6). This applies especially to FM and other CW modes, at which the unit should be run at reduced power levels and voltages. At full power output (Fig. 7) and worst-case efficiency, power dissipation gets dangerously close to the derated limit, assuming a 60-to-70°C flange temperature.

Overtightening the device mounting screws will bow the relatively thin and long flange. Split lockwashers should be used, with enough mounting torque to fully compress the washer. Silicone thermal compound must be applied to the flange/heat-spreader interface. A thin layer wiped only to the flange bottom is sufficient and will spread evenly under the pressure. This interface, the mounting torque, and the flatness and type of mounting surface are some of the most important aspects in high-power transistor amplifier design because heat is the number one enemy of any solid-state device. ••



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rf featured technology

Wideband RF Power Amplifier

This Amplifier Operates Over A Wide Range Of Supply Voltages.

By H.O. Granberg
Motorola Semiconductor Products

A single amplifier covering frequencies from HF to VHF at a power output level of 300 watts would have been considered impossible or impractical a few years ago. This would still be true if not for the advances in power FET technology.

This article covers the design aspects of a 300 watt unit with a frequency range of 10 to 150 MHz.

The MRF141G, used in this design, is housed in a special push-pull header commonly known as "Gemini" (twins), meaning that there are two identical transistors mounted next to each other on a common carrier or a flange. There are transistors (mainly FETs) available in the Gemini type packages rated from 20 watts to 300 watts. The lower power units can be used to frequencies of 1 GHz and higher, while the 100-150 watt units are designed to operate up to 500-600 MHz.

The advantages of a push-pull package such as the Gemini become apparent at higher frequencies, where the normal push-pull configuration with discrete devices would be impractical. In the push-pull circuit configuration the critical factor is the mutual inductance between the two push-pull halves, and not the device to ground inductance, as is the case in single ended designs. The Gemini or any other push-pull transistor housing permits the minimization of the mutual inductance to a level that approaches the ultimate in physical terms.

There are a couple of penalties we must pay for all this. One is a slightly higher cost when compared to two discrete units due to matching procedures involved and lower production yields resulting from double the possible reject rate. Another one is the reduced thermal characteristics. Twice as much dissipated power is concentrated virtually in the same area as in the case of a discrete design, leading to special cooling requirements.

About Power FETs

There have been designs of high power HF amplifiers using the T0-3 packages,

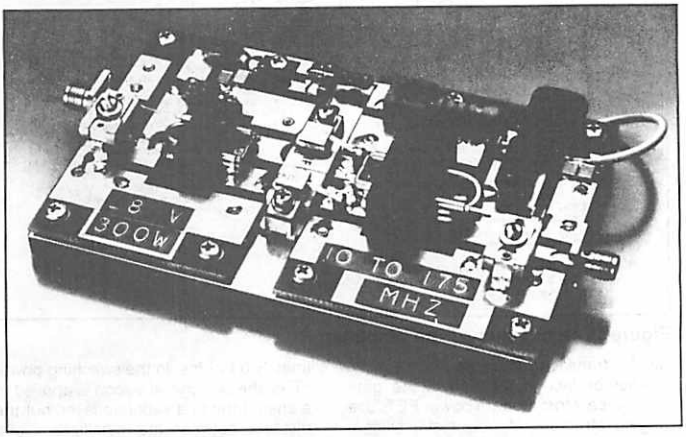
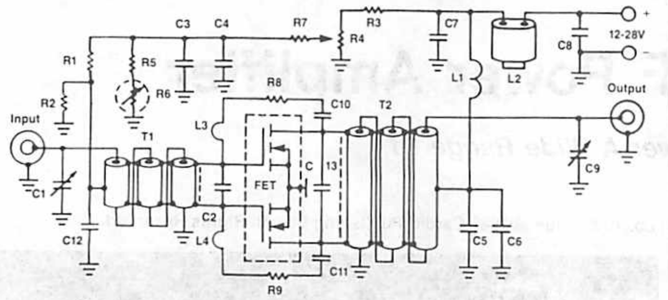


Figure 1. Overall view of the 300 watt, 10-150 MHz amplifier. Separate circuit boards are used for the input (left) and the output.

and lower power versions with the T0-220 plastic units. With a given die geometry, a FET has approximately four times higher unity gain frequency than a bipolar transistor. This explains the fact that even the larger low frequency power FETs may have 10 dB or more power gain at 30 MHz, where a similar bipolar counterpart would be totally unusable. The difference is mostly in the figure of merit of the die itself, which is the ratio of feedback capacitance to the input capacitance or impedance. (This should not be confused with the more common base area/emitter periphery figure of merit die design formula.) With bipolar transistors the feedback capacitance (collector to base) is not usually specified, but it is 15-20 times higher than the drain to gate capacitance of a comparable FET, while the base/gate input impedances become about equal at increased frequencies. This feedback capacitance normally produces feedback within the device itself, whose exact phase angle depends on the capacitance values and other parameters.

In FETs designed specifically for RF, the die geometry is usually finer (larger ratio of the gate periphery to the channel area) than in the switching power FETs. This reduces the device capacitances automatically. Further reduction is achieved by splitting the die into a multiple of cells (groups of source sites and gate fingers) where the gates and sources are connected in groups of two or four by individual bonding wires to the common package terminals. For example, in the MRF141G one of the two die consists of 36 cells each having around 70 individual small FETs, making the total about 2,500.

In switching power FETs, the connections to the numerous source sites and gates are made with metal pattern on the die surface which allows the use of single large diameter bonding wires for the source and gate contacts. The increased metal area results in increased MOS capacitance and reflects to the device input (C_{ISS}), feedback (C_{RSS}) and output (C_{OSS}) capacitances. The transconductance of a MOSFET g_{fs} is a measure of its electrical size. Thus, a good indication of the high frequency performance can be obtained by comparing the capacitance values (especially C_{RSS}) of devices with



R1 — 1K/½W
R2 — 10K/½W
R3 — 330 Ohms/2W
R4 — 1K Trimpot
R5 — 6.8K/¼W
R6 — Thermistor, 10K at 25°C/2.5K at 75°C
R7 — 2K/½W
R8, R9 — EMC Technology Type 5310 or KDI Pyrofilm Type PPR 515-20-3 Power Resistors, 25 Ohms
C1, C9 — ARCO 402, 1.5-20pF Compression Mica or equivalent
C2 — 200pF Ceramic Chip
C3 — 0.1uF Ceramic Chip
C4, C5, C12 — 1000pF Ceramic Chip
C6, C7 — 0.01uF Ceramic Chip
C8 — 0.47uF Ceramic Chip or lower values in parallel for the value indicated
C13 — 300pF, 2x150pF or 100pF and 200pF Ceramic Chips in parallel

L1 — 10 Turns AWG #16 Enameled Wire, 5mm I.D.
L2 — Ferrite Beads over AWG #16 Wire, 1.5 uH total
L3, L4 — Lead Lengths of R8 and R9, 20mm total
FET — MRF141G
T1 — 9:1 RF Transformer (15-25 Ohm, 1.2-1.6mm O.D. semi rigid coax.) Magnetic Core Required: Fair-Rite Products Corp. #9461012002/9361021002 E and I (2 ea.) Types, Respectively, or Equivalent.
T2 — 1:9 RF Transformer (15-25 Ohm, 1.8-2.3mm O.D. semi rigid coax.) For Magnetic Core See Text

Note: All chip capacitors of 0.01uF and less in value are ATC type 100 or equivalent.

Figure 2. Schematic of the amplifier.

similar transconductances.

Another fact to mention is the gate resistance. Most modern power FETs use a gate structure of polycrystal silicon, which can have a bulk resistance comparable to carbon. It is also used as a conductor between the metal pattern and each individual gate. In the RF power FETs, each gate is fed through a separate contact having a resistance of approximately 0.1 ohms. In the switching power FETs, the polycrystal silicon is applied in a sheet form in a separate layer, but the distance between the metallization and the farthest gate still results in at least 30-40 times higher gate resistance with a die of comparable size.

In high frequency applications the high gate resistance permits a part of the drain-source RF voltage or transients to be fed back to the gate through C_{RSS} in amplitudes that can rupture the gate-source oxide layer. The rupture will first occur in the far end of the die, away from the gate terminal. Since the gate resistance is internal to the FET die, external limiting or clamping circuits at the gate are of no help. The gate of a MOSFET is the most sensitive part of the device, which can be permanently damaged even by static charges during the handling. Although the larger FETs (100-150 W), due to their higher gate capacitance, are not as vulnerable as the smaller ones, proper precautions should be exercised.

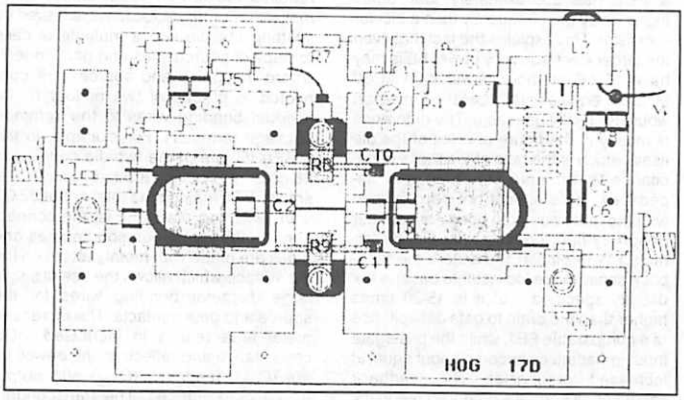


Figure 3. The component layout diagram. The only critical component locations are those of C2 and C13. They must be soldered in place (½ of C13) before the mounting of the input-output transformers.

Design and Construction

As discussed earlier, the common mode inductance in a push-pull circuit is not critical, and the ground path is only used for DC feed to the amplifier. The input and output impedance levels are established from gate to gate and drain to drain respectively. This allows the circuit board, which is made of the standard 1.6 mm G10 material, to be split into two sections. One carries the input matching network and part of the bias circuit, while the second section holds the output matching network, the bias set and the drain voltage feed and filtering circuitry. (See Figures 1 and 2). In addition to allowing wider design flexibility, this arrangement also simplifies the repair and maintenance of the unit, if required.

The two circuit boards including the space between them for the FET measures 115 × 75 mm. They are mounted on a copper plate with the same dimensions having a thickness of 6 mm. The input and output connectors (SMA) are mounted to the edges of the copper plate. They can also be placed at a remote location with coax connections to the amplifier utilizing any connectors that have good RF characteristics such as BNC.

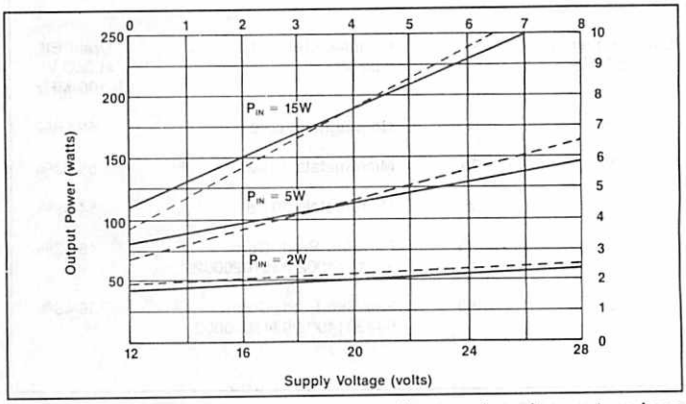
Due to the large amount of heat concentrated in a small area in the form of dissipated power, it is important that the copper plate be employed as a heat spreader unless the heat sink itself is made of copper. The heat spreader can then be bolted to a piece of aluminum extrusion with thermal resistance of 1° C/W or less for normal intermittent operation without forced air cooling. The heat spreader and the extrusion surfaces should be flat without any burrs, and silicone thermal compound must be applied to the interface. The same practices should be followed in mounting the FET into the heat spreader. If the FET gate and drain leads are bent sharply up along the package sides, they will be aligned along

7

the edges of the circuit boards. This makes the board spacing from the heat spreader less critical, which then can be anywhere from 1 to 3 mm. The FET lead lengths to the board connection points are variable by the same amount, but they have a minimal effect on the impedance matching and performance at these frequencies.

Details of the electrical design concepts of a similar amplifier are given in reference 1. The input-output transformers require a special low impedance semi-rigid coax cable making construction difficult in single quantities. The output transformer only requires a magnetic core if operation below 75 MHz is desired. In contrast, the input transformer always requires one regardless of the frequency of operation. In a push-pull FET amplifier design the gates of the two halves must be isolated by sufficient inductance or resistance (7,8). In order to prevent instabilities which will occur at the resonant frequency of the device capacitances, the internal wire bond inductances and the external inductances, sufficient isolation is required between the two gates which the magnetic core will provide. Without this, the two FETs of the push-pull circuit would see a parallel connection at some resonant frequency, which would result in serious instability problems.

The importance of the negative feedback (L3, L4-R8, R9-C10, C11) must be emphasized. Without it the power gain would exceed 30 dB at low frequencies, resulting in increased conditions for instabilities. The feedback is designed to lower the low frequency power gain close to the 150 MHz level it is at. L3 and L4, which consist of the lead lengths of R8 and R9 represent a reactance of 20 ohms each at 150 MHz. It also controls the frequency-amplitude slope. This in series with the 25 ohm resistor values lowers the power gain by one dB at 150 MHz but increases to as much as 15 dB at 10 MHz. C10 and C11 are only used for DC blocking and their values are not critical as long as their reactances are less than 10-15 percent of R8+R9. C10 and C11 are ceramic chip capacitor that are mounted vertically on the circuit board (Figure 1). Although unusual, it allows the feedback resistor leads to be soldered directly to the capacitor top terminals. This provides a much lower inductance path than the conventional mounting technique and saves board space. Since R8 and R9 must be able to dissipate up to 15 Watts each depending on the frequency of operation, they must be of a type that can be easily heat sunk. The type resistors designated



Fgure 4. Amplifier power output versus the supply voltage at various input levels. Solid lines represent 150 MHz and dashed lines 10 MHz.

have mounting lugs which are terminally connected to the copper heat spreader through 5 mm high spacers.

These are mounted on top of the ends of the FET flange, allowing the use of common screws for fastening the resistors and the FET. The spacers must be of material with low terminal resistance like aluminum, brass or copper, and must have a larger surface area than thin wall tubing. A couple of stacked brass nuts, one size larger than the mounting screws is a good solution. Although not very professional it works rather well. If the unit is used for other than intermittent modes of operation such as voice communication, a thermistor (R6) can be used for bias stabilization. Without it the drain idle current will approximately triple if the FET case temperature is doubled, and would result in decreased efficiency. The thermistor can be attached to a solder lug, which is fastened with one of the resistor-FET mounting screws.

The input and output impedance matching is achieved with unique wide-

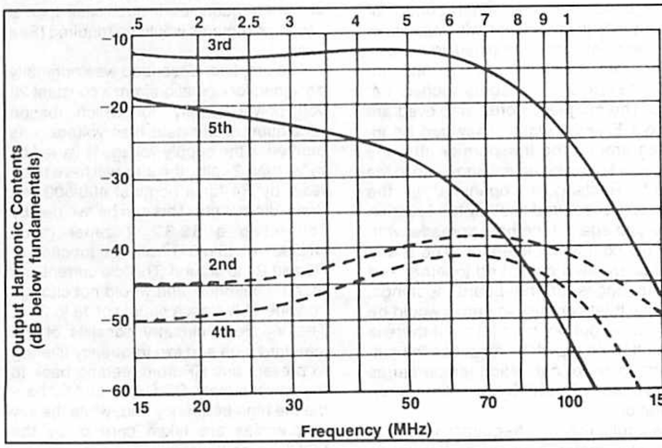


Figure 5. Output harmonic contents versus frequency. (V_{DS} = 28V, P_{OUT} = 300W.) The benefit of the push-pull configuration can be seen in the suppressed even order products. The data does not change considerably with varying the supply voltage or power output.

Low Frequency end MHz	μ1	Manufacturer and type #	Drain Eff. at 300 W, 75-100 MHz
75	1	No magnetic core	62-66%
25	20	Micrometals 101-2	59-63%
15	35	Micrometals 101-8	54-59%
7.5	125	Fair-Rite Prod. Corp. 9461014002/9361020002	46-52%
2	850	Fair-Rite Prod. Corp. 9443014002/9343020002	36-43%

Table 1. Effect of the output transformer magnetic core material on amplifier bandwidth and efficiency.

band transformers described in References 1 and 2. Some of their advantages are: DC isolation between the primary and the secondary, automatic balanced to unbalanced function and compact size in comparison to the power handling capability. Their principle is the same as in ordinary low frequency transformers, except that tight coupling between the windings is achieved through the use of low impedance transmission line, in this case semi-rigid coax cable. The low impedance side always has one turn and consists of parallel connected segments of the coax outer conductor. The inner conductor forms the high impedance winding, where the segments are connected in series.

This arrangement only permits impedance ratios with integers such as 1:4, 9, 16. The magnetic cores employed are the old E and I types. They can be inserted around the transformer after the windings are made up and mounted to the board. Rectangular openings in the boards are required to allow the I section to be laid against the heat spreader with thermal compound interface. The E and I cores are then cemented together and to the edges of the board openings. Special heat conductive epoxy would be preferable, but not mandatory. If there is no air flow on top of the amplifier, the output transformer can reach temperatures in excess of 100°C in continuous operation.

As a rule, the high frequency losses in magnetic material such as ferrite or powdered iron, are more or less directly related to its permeability, and appear as heat generated within the core. Since this part of the RF energy is not delivered to the output terminal, and the drain current is equal in each case, the result is lowered overall efficiency.

From the above we can conclude that the magnetic core material should be selected according to the lowest desired frequency of operation. For example, from 2 to 150 MHz, initial permeability (u_i) of over 600 and cross sectional area of about 1 cm² would be required. Ferrites in this category have Curie temperatures of 130-140°C, above which temperature they become paramagnetic and causes serious malfunctions in the operation of at lower frequencies. In such case special cooling structures would be required (See Table 1).

The amplifier described was originally designed for operation from a constant 28 volt power supply, for which reason regulation of the gate bias voltage was omitted. If the supply voltage is varied by more than 2 volts, the bias will have to be reset by R4 for a nominal 400-500 mA drain idle current. This can be avoided by connecting a 6.8-8.2 V zener diode (1N5921A-1N5923A) from the junction of R3 and R4 to ground. The idle current can then be set once, and would not change considerably from a supply of 12 to 28 V. The V_{DS} feed circuitry consists of the standard high and low frequency filtering to prevent any RF from feeding back to the power supply. C5, C6, L1 and C7 handle the high frequency end, while the low frequencies are taken care of by the L2-C8 combination.

Performance

With the 1:9 impedance ratio output transformer employed, the optimum power output at 12 and 28 V supplies would be only 50 and 265 watts respectively.

$$P_o = \frac{2V^2_{DS} - V_{DS_{ON}}}{50/9}$$

At these power levels the IM distortion is better than −30 dB at all frequencies, the worst case being at 50-100 MHz. From Figure 4 it can be seen that higher output levels are possible with increased drive power, but the amplifier will be close to saturation and can be only used for nonlinear applications such as FM or CW. For the best IMD, the idle current should be 500-800 mA total, but disregarding the linearity, it can be as low as 100-200 mA. Lower idle current will result in loss of power gain by 0.5-1.0 dB, while increasing the efficiency.

The stability of any RF power amplifier (especially solid state) under mismatched load conditions is always a concern. The power MOSFETs have been proven superior in this respect to the BJTs, although the stability is also circuit dependent to a great extent. The stability of the amplifier described here has been tested against load mismatches using a simulator of 30:1 at all phase angles and a 3 dB power attenuator to the amplifier output, which results in approximately 3:1 VSWR. Unconditional stability was shown at a combination of any power output level and supply voltage at 10, 50 and 150 MHz. Stability into a 3:1 mismatched load is almost considered a standard specification in the industry, meaning that the harmonic filter-antenna combination (if applicable) should have its input VSWR equal or lower. Normally 2:1 is easy to achieve over a fraction of an octave bandwidth, unless the filters are improperly designed. Figure 5 shows that at 150 MHz and beyond the output harmonics are well suppressed to start with, but a filter is still required to meet the FCC regulations. More elaborate filtering is necessary at lower frequencies, where the 3rd harmonic is only 12-13 dB below the fundamental. For most industrial applications, however, harmonic filtering may not be necessary. Although data is not shown, the amplifier can be used up to 175 MHz with a power gain of 10-11 dB. C1 should be adjusted for lowest input VSWR and C9 for the peak power output at the highest desired frequency of operation.

As the MRF 141G basically operates from a 28 V supply, lowering the voltage down to 20 or below would make the unit almost indestructible against load mismatches in case of an open coax or broken antenna. Figure 4 shows that the power output is still almost 200 watts at

20 V and 150 watts at 16 V. The ruggedness criterion does not apply against possible transients to the input from the signal source and assumes that the FET is properly mounted to the heat sink. A normal guideline is that a transistor should have its break down voltage (BV_{dss}) 2-25 times the operating voltage. The break down voltage is set by choosing the starting material (silicon) with proper resistivity or doping. If the break down voltage is too low, the output voltage swing may exceed it and cause an avalanche. If it is too high, the transistor will saturate at a low power level, but it will be harder to blow up since the device is less likely to exceed its dissipation limits. For the same reason, devices made for 50 V operation are often used at 30-40 V and at reduced power levels in applications like laser drivers and magnetic resonance imaging, where they must momentarily withstand a large output load mismatch. The circuit boards and other components for this design are available from Communication Concepts, Inc., 121 Brown Street, Dayton, OH 45402. rf

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HOW TO APPLY THE MHW709/MHW710 UHF POWER MODULES

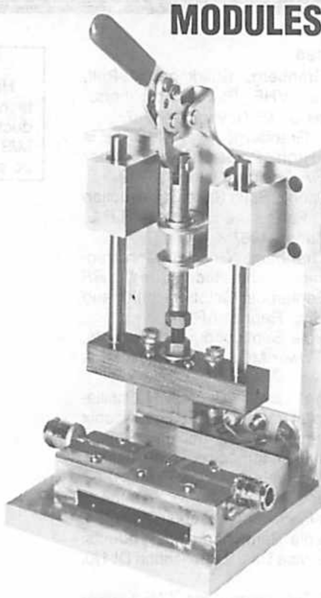


FIGURE 1 — UHF POWER MODULE TEST INFORMATION (MHW709 AND MHW710)

TEST CIRCUIT

Motorola's UHF Power Modules use thin film construction to minimize parasitics, and for manufacturing consistency. They're flange mount for easy, one-sided assembly. They reduce your system inventory, eliminate the need for special production equipment. But even though the MHW709/MHW710 are "complete" UHF power drivers and reduce RF design and production to a new level of ease, there are a few operation and testing considerations to follow for best results.

The modules are conservatively rated. Actual output power capability is 50 to 70% above rated power. However, the equipment designer should not design a product using the module above the rated output power. In some cases, if smaller margins are acceptable and certain other conditions are met, some of the reserve power output can be used. In this case, please contact your Motorola representative for specific recommendations.

When operated within published specifications, the maximum device current density seen in a limit module will be 1.5 x 10^5 A/cm^2. Maximum die temperature with a 100° C base plate temperature will be 165° C.

Nominal ratings are for a 12.5 Vdc supply (V_s at pin 5) and control (V_{sc} at pin 3) voltage. Specifications such as power gain, efficiency, and input VSWR are measured with the nominal 12.5 Vdc supply and an output power of 13 W (MHW710) and 7.5 W (MHW709).

Gain Control

The preferred method of operation is to apply 12.5 Vdc to both pin 3 and pin 5 through the recommended decoupling network. (In general, the *module output power* should be limited to 14 W, MHW710; 8.5 W, MHW709.) The output of the module is then set by adjusting the input drive level. Operation in this manner will result in the best performance with temperature variation.

Pin 5 supplies collector voltage to the input stage in the module. This pin is internally bypassed by a .018 μF chip capacitor effective for frequencies *from 5 MHz* through the operating frequency. Due to size limitations in the module, additional external low frequency decoupling effective below 5 MHz is required (as is required with discrete UHF transistors). If pin 5 is used to reduce the module output, two characteristics may cause an application problem.

One is that with the drive power appreciably above that required (+2 dB or so) for 13 watts output, the voltage on the first stage may be as low as four or five volts. This low voltage tends to increase the slump in output power with increasing temperature as opposed to the condition of pin 5 = pin 3 = 12.5 V and drive adjusted for desired power output. Second, if voltage to pin 5 is derived from a series dropping resistor and the value of the resistor is above 10 to 20 ohms, the output power will tend to rise with decreasing drive which could cause problems in an application using an automatic gain or output leveling circuit. If pin 5 is fed from a regulated voltage source, as opposed to a series dropping resistor, this problem does not arise, however, the temperature slump characteristic is still present.

Typically, the MHW710 slump at 80° C from rated output at 25° C with V3 = V5 = 12.5 Vdc is 9 to 12%. With pin 5 voltage set for rated output power and rated drive applied, the typical slump will be 10 to 16% at 80° C. Slump in the MHW709 under the same conditions is typically 5% less than the above figures.

Decoupling

As mentioned, size limitations in the module make it necessary to provide external coupling for frequencies below 5 or 10 MHz. This can take the form of a network as shown on the data sheet. All decoupling capacitors internal to the module are .018 μF chips. Output and interstage blocking capacitors are 39 pF NPO chips. This chip type has a nominal reactance to 9 ohms in the UHF band and was selected to decrease the module gain at frequencies below the pass band. Also, the base return chokes in all stages were selected to degrade gain slightly at UHF with greater effect at lower frequencies. The use of small coupling and blocking capacitors along with low impedance base returns reduces the loop gain at low frequencies to minimize low frequency problems from the increased device gains below the operating frequency.

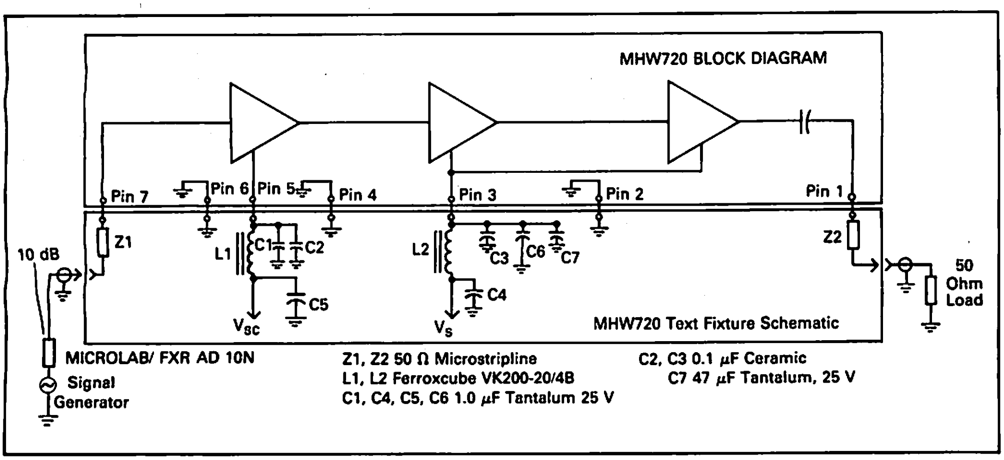
The decoupling network shown on the data sheet is used during final test of the module and has been found effective for our test setup. Differences in test circuit layout, ground current paths or other low frequency feedback circuits could require a modified decoupling network. Some applications may benefit from the use of a series R-C damping circuit connected to ground from pins 5 or 3. This can consist of a 5 to 10 ohm carbon resistor in series with a 1 to 10 μF, 25 volt electrolytic or tantalum capacitor.

Source and Load Impedances

The modules are designed for proper operation with source and load impedances of 50 ohms resistive. With proper decoupling, they will be stable with 2:1 VSWR source and load impedances, any phase angle and any combination of phase angles at nominal drive and power output. In addition, the rf drive and supply voltage can be varied over wide ranges. Typically, during this test, no spurious outputs are seen except with drive powers above 300 mW taken simultaneously with supply voltages below 4 or 5 volts. This condition of simultaneous high drive and low voltage will most likely never be seen in actual applications.

Most problems with module instabilities are a function of poor source impedance or poor decoupling. If a tendency is seen for the module to "snap on" or have hysteresis in the output power versus input power curve, the problem is most likely due to a source VSWR above 2:1 relative to 50 ohms. To check this, put a 3 dB or 6 dB

FIGURE 2 — UHF POWER MODULE TEST SETUP



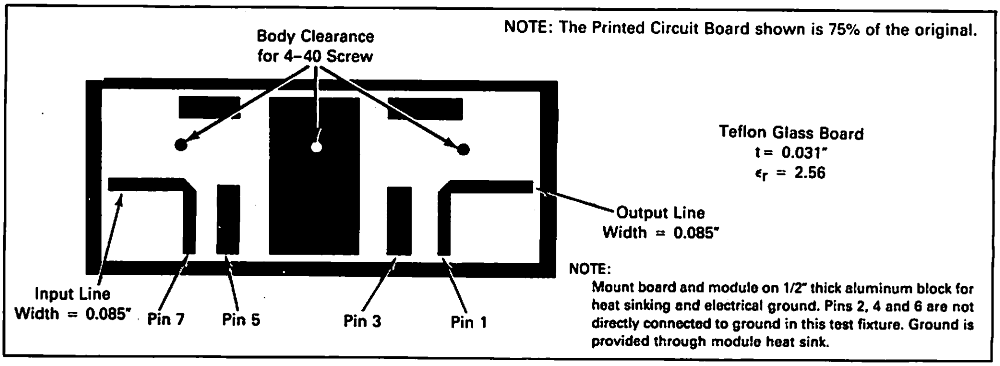
NOTE: No Internal D.C. blocking on input pin.

matched pad between the source and the module. The hysteresis or "snap" should disappear if the problem is source impedance. If "jumps" are noticed during varying input power conditions, the problem is most likely low frequency breakup due to insufficient low frequency decoupling—this can be seen on a spectrum analyzer sampling the output power. If a spectrum analyzer is not available, an ac-coupled 10 MHz oscilloscope on the dc feed pins at the module will usually detect low frequency breakup.

a spectrum analyzer. It has been found that at least 90 percent of semiconductor failures during load mismatch tests are due to spurious breakup during the test. When the spurious problems are solved, the burnout problems are also solved.

The MHW modules are 100% tested for burnout and spurious breakup two times during the production process. One test is performed after the module is com-

FIGURE 3 — UHF POWER MODULE TEST FIXTURE
PRINTED CIRCUIT BOARD



pleted and on the heatsink, another is performed after the module is capped and marked. The 13 watt modules are tested at 17 to 20 watts output into a load with a return loss of less than 0.7 dB at all phase angles (greater than 25:1 VSWR) and the 7.5 watt modules are tested at 10 to 12 watts into the same load.

When using the module as a drop-in for other modules, it has been found that circuit "tweaks" made to compensate for antenna switching and output filter VSWR to provide optimum performance with a particular type module may degrade the performance of the MHW series modules. The output circuit in this module is a low-pass Chebyshev impedance transforming network. It is carefully designed to provide a 50 ohm source impedance with a VSWR of less than 1.3:1 at 13 watts power output and 12.5 V supply. The power available to the load (forward power as measured by a directional coupler) with this module will not degrade more than 20% from the power set into a 50 ohm load when a load with a VSWR of 2:1 is placed on the output and varied through all phase angles. This characteristic holds true throughout the rated frequency range of the module.

Load Mismatch

When performing a load mismatch capability test with any semiconductor device, especially in a new environment where all sources of regeneration are not yet identified, one should monitor the output of the device with a directional sampling scheme and display this output on

In summary, it is recommended that the MHW709/710 series modules be operated under the following conditions:

1. Source and load VSWR <2:1 with respect to 50 ohms.
2. Proper low frequency decoupling.
3. Supply voltage of 12.5 volts applied to both pin 5 and pin 3 with driver power adjusted for desired output power.
4. Sufficient heatsinking so that module flange does not exceed 100° C (preferably 80° C).
5. Flange at rf ground potential. The "ground" pins 2, 4, and 6 are not sufficient to establish a good rf ground at UHF by themselves.

When these rules are followed, the MHW709/710 series modules will provide the performance you expect.

CONTROLLED — Q RF TECHNOLOGY — WHAT IT MEANS, HOW ITS DONE

The difficult transfer of high frequency energy from a signal source to the control element of an RF power transistor is efficiently achieved by a new design philosophy. Both monolithic and hybrid IC techniques are used to include a matching network in the transistor package and overcome this tough design problem.

The insertion of a matching network into an RF power transistor package has cured many evils encountered in high frequency circuit design. Devices using such an internal impedance matching network have been dubbed Controlled Q because that is exactly what the added package circuitry does — it gives the power transistor a consistent and highly controlled electrical quality (Q) factor. In a nutshell controlled Q increases guaranteed gains from previously available 4 dB to 5 or 6 dB in the 470 MHz region at 12.5 V. The controlled Q means that these devices are easier to match into circuit networks, and offer better consistency of high frequency parameters than other, non-controlled Q RF power devices.

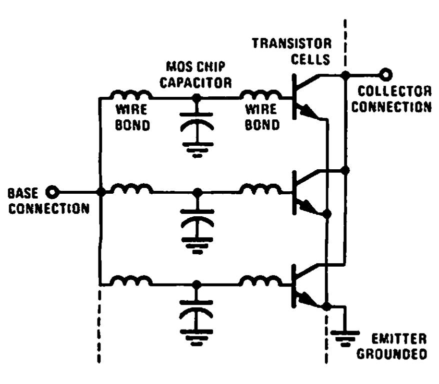


FIGURE 1 — Each base region has an internal matching network included in the CQ package.

The Old and the New

There are no panaceas for the complexities of broadband RF circuit design. With or without controlled Q, circuit networks must be designed to impedance-match the different stages. Gain and power output has to be optimized for the particular application, while maintaining a specified overall circuit bandwidth.

With older RF power devices, such as the 2N6136, a complete interstage matching network had to be provided using discrete passive components external to the transistor package. Not only did the circuit take up a lot of space, but its overall series component reactance limited design capability — especially in bandwidth. In addition, parasitic elements caused by the extra components, and package geometries interfered with establishing a solid signal ground.

With newer controlled Q devices, "inside-the-package" construction of some of the network matching elements brings the network closer to the active transistor die. Not only does this eliminate the number of required external components, but it also means that a small amount of capacitance can minimize the imaginary part of the input impedance for maximum bandwidth. Internal construction techniques help establish a better signal ground by removing most parasitic reactance.

A Closer Look

Controlled Q transistors use both monolithic and hybrid techniques in their construction. The active transistor die is fabricated using monolithic integrated circuit methods. A small MOS chip capacitor is wire bonded to the active transistor die thus incorporating hybrid technology. The resulting total transistor package can be thought of as an active transmission line element for high frequency (to 500 MHz) amplifier design. Figure 1 shows a portion of the device circuit.

To meet the high power handling requirements the controlled Q transistors are specially constructed with each of its multiple emitters having its own ballast resistor. These nichrome (NiCr) resistors, shown in the close-up of Figure 2, have different resistance values to compensate for thermal differences of various portions of the transistor chip. This prevents overloading of some emitters due to temperature difference. This Isothermal* resistor design technique assures balanced current distribution throughout the transistor for more consistent operation at various power levels.

Emitter inductance and its undesirable gain reducing negative feedback are minimized in controlled Q devices, by establishing a solid ground for the transistor emitters. This is accomplished by using the lead frame to extend the ground plane completely around the device. Emitter wires are then attached to this ground plane. Such an emitter bonding technique has been shown to contribute more than 50% of the gain increase of a controlled Q device in the 470 MHz region. Its total gain of 5.22 dB is significantly higher than a non-CQ device of the same 25 W version that gives around 4.0 dB gain.

Controlled Q transistors also have bonding wires extending from each transistor base region to the MOS capacitor chip and then out to the package base lead. These bonding wires and the MOS capacitor interconnect one half of an input impedance matching network as in Figure 3.

**Trademark of Motorola Inc.*

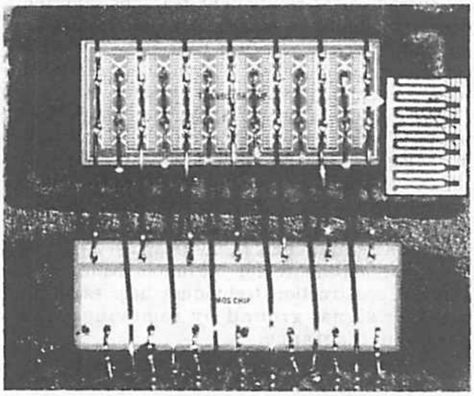


FIGURE 2— A close-up view of the emitter ballasting resistors.

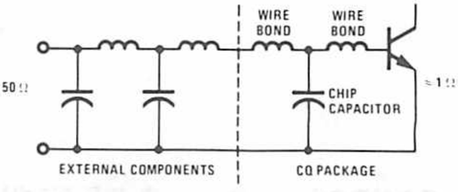


FIGURE 3 – Part of the transmission network inductance and capacitance is provided in CQ transistor packages.

Controlled Q production methods not only increase device yield, but also allow all final factory testing to be done in fixed-tuned test equipment. This means ease of final test for the semiconductor manufacturer, but more importantly, insures the consistency of controlled Q transistors from device to device. To the RF equipment manufacturer, this means that once a piece of communications gear has been designed, controlled Q devices can be dropped into amplifier modules with a minimum of circuit adjustment and tuning.

What's Available

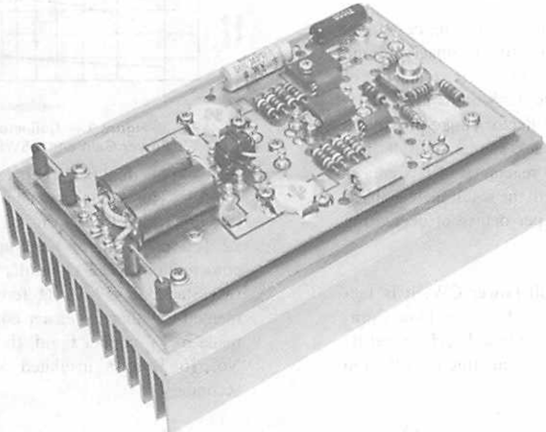
Motorola's MRF series of high frequency power devices are available in stripline opposed emitter packages which offer excellent thermal characteristics along with controlled Q operation. Available in both 12.5 V and 28 V devices, these transistors listed in Table I are capable of operating at frequencies to 900 MHz with power outputs to 50 watts.

TABLE I – Controlled Q RF Power Transistors

Device	Operation Voltage	Output Power	Frequency	Comment
MFR243	12.5 V	60 W	to 175 MHz	For VHF Large Signal Application
MRF245		80 W		
MRF316	28 V	80 W	to 200 MHz	For VHF MIL Aircraft and Mobile Operation
MRF317		100 W		
MRF641	12.5 V	15 W	to 512 MHz	For UHF FM Mobile Applications
MRF644		25 W		
MRF646		40 W		
MRF648		60 W		
MRF325	28 V	30 W	to 500 MHz	For 225-400 MHz Aircraft and Mobile Operation
MRF326		40 W		
2N6439		60 W		
MRF327		80 W		
MRF338		80 W		
MRF329		100 W		
MRF840		7 W	to 900 MHz	For 900 MHz Land Mobile
MRF842		20 W		
MRF844		30 W		
MRF846		40 W		

GET 300 WATTS PEP LINEAR ACROSS 2 TO 30 MHz FROM THIS PUSH-PULL AMPLIFIER

Prepared by
Helge Granberg
Circuits Engineer, SSB

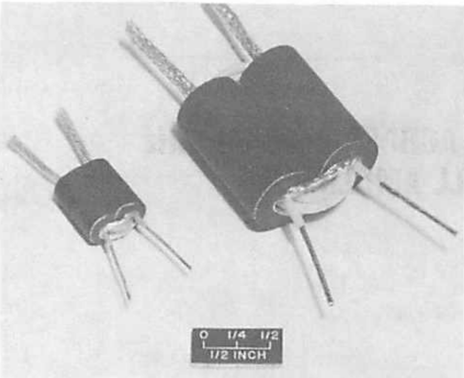


(The heat sink shown with amplifier is sufficient only for short test periods under forced air cooling.)

This bulletin supplies sufficient information to build a push-pull linear amplifier for 300 watts of PEP or CW output power across the 2- to 30-MHz band. One of Motorola's new high-power transistors developed for single-sideband, MRF422, is used in this application.

Like all transistors in its family of devices, MRF422 combines single-chip construction that is advancing the state-of-the-art, and improved packaging to accommodate the low collector efficiencies encountered in class B operation. Rated maximum output power is 150 watts *CW or PEP with intermodulation* distortion spec'd at −30 dB maximum, −33 dB typical. Although not recommended, a saturated power level of 240- to 250-W is achievable. Maximum allowable dissipation is 300 W at 25°C.

Because of its excellent load and line voltage regulating capabilities, an integrated circuit bias regulator is used in the amplifier. The MPC1000, originally described in this bulletin, consisted of a MC1723 chip and a built-in pass transistor. The manufacture of this device has been discontinued however, and the board lay-out was modified to incorporate the above two in separate packages. The load regulation typically measures less than 2% at current levels up to 0.5 A, which assumes an h_{FE} of 40 for the RF power devices. The board surface provides a sufficient heat sink for the 2N5990 pass transistor, but a separate heat dissipator, such as Thermalloy 6107 can be added if necessary. With the component values shown, the bias is adjustable from 0.4 to 0.8 volts.



Transformer Construction

Gain flatness over the band is achieved using base input networks R_1C_2 and R_2C_3 and negative feedback through R_3 and R_4. The networks represent a series reactance of 0.69 ohms at 30 MHz rising to 1.48 ohms at 2 MHz. A single-turn winding in the collector choke provides a low-impedance negative feedback source, thus R_3 and R_4 determine the amount. The reactance of C_4 reduces feedback at high frequencies with the result that feedback increases an average of 4 dB per octave at decreasing frequency.

For continuous operation at full power CW, it is recommended that heat sink compound, such as Dow Corning #340, be applied between the board surface and R_3 and R_4, and if possible have air circulating over the top of the circuit board as well.

The effective base-to-base impedance, increased by the RC networks is about 5 ohms at midband. As a result of this and the 9:1 impedance ratio in the input transformer T1, the input VSWR is limited to 1.9:1 or less across the band. Transformer T2, in addition to providing a source for the feedback and carrying the dc collector current, acts as the rf center tap of the output transformer. To construct T2, wind 5 turns of 2 twisted pairs of AWG No. 22 enameled wire on a Stackpole 57-9322 toroid (Indiana General F627-8Q1).

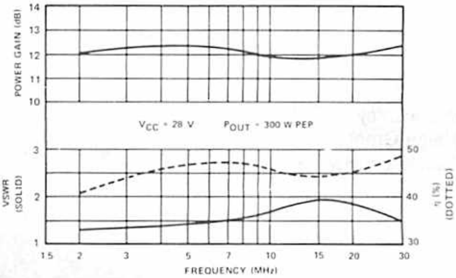
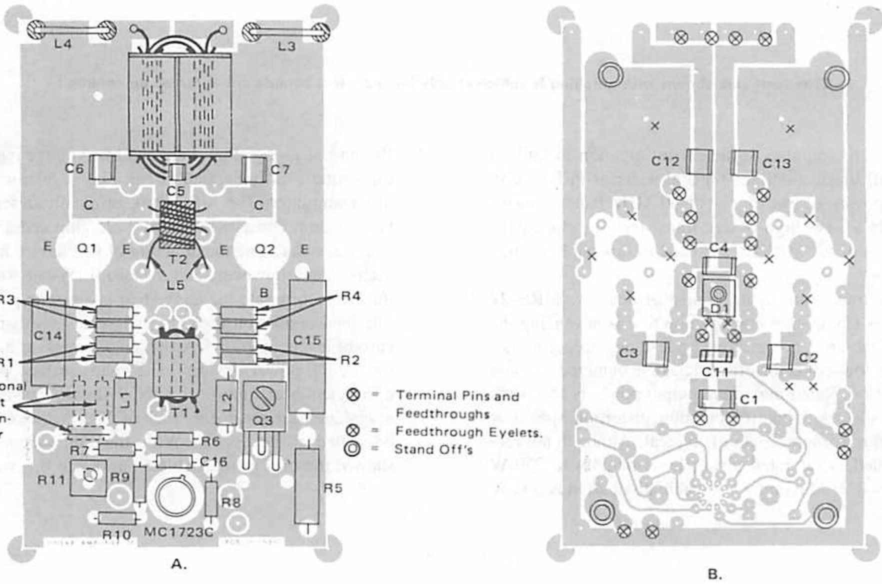


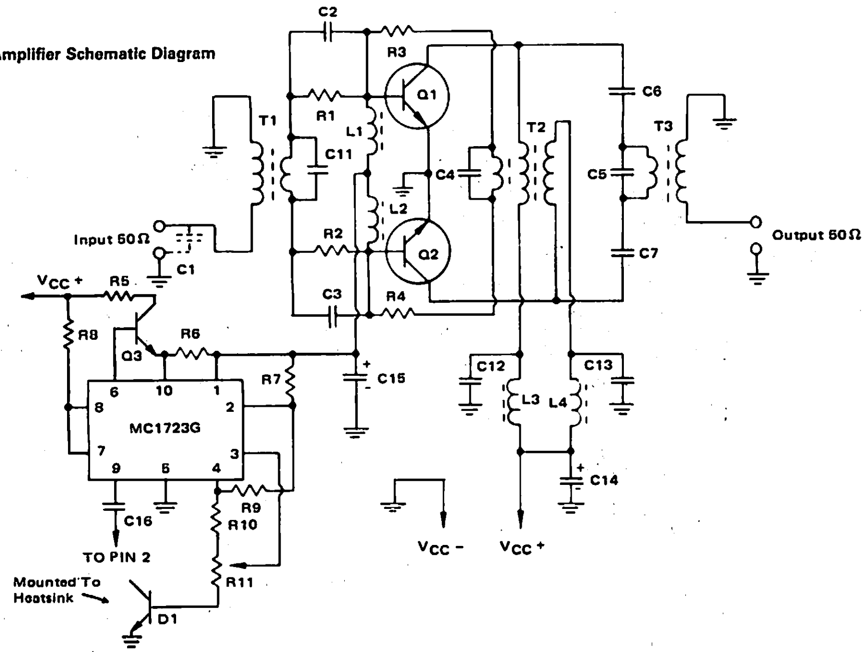
Figure 1 — Collector Efficiency, Power Gain and VSWR vs Frequency

A Stackpole dual balun ferrite core 57-1845-24B is used for T1. The secondary is made of ⅛″ copper braid, through which three turns of the primary winding (No. 22 Teflon® insulated hook-up wire) are threaded. The construction of T3 is similar to that of T1. It employs two Stackpole 57-3238* ferrite sleeves which are cemented together for easier construction. The primary is made of ¼″ copper braid, through which three turns of No. 16 Teflon® insulated wire are threaded for the secondary.



A. B.

300-Watt Linear Amplifier Schematic Diagram



C1 – 100 pF
C2, C3 – 5600 pF
C4, C5 – 680 pF
C6, C7 – 0.10 μF
C11 – 470 pF
C12, C13 – 0.33 μF
C14 – 10 μF – 50 V electrolytic
C15 – 500 μF – 3 V electrolytic
C16 – 1000 pF

R1, R2 – 2 X 3.3Ω, 1/2 W in parallel
R3, R4 – 2 X 3.9Ω, 1/2 W in parallel
R5 – 47Ω, 5 W
R6 – 1.0Ω, 1/2 W
R7, R8 – 1.0 k, 1/2 W
R9 – 18 k, 1/2 W
R10 – 8.2 k, 1/2 W
R11 – 1.0 k Trimpot
D1 – 2N5190
L1, L2 – Ferroxcube VK200 20/4B
L3, L4 – 6 ferrite beads each, Ferroxcube 56590 65/3B

Q1, Q2 – MRF422, Q3 – 2N5990
T1, T2, T3 – See text

All capacitors except electrolytics and C16 are chips –

Union Carbide type 1813 and 1225, or Varadyne size 18 or 14, or equivalent

For production quantities, the braid in T_3 may be made of brass or copper tubes with their ends soldered to pieces of PC board laminate. See cover picture and Motorola AN-749 for details.

The bandwidth characteristics of these transformers do not equal those of the transmission line type, but they're much easier to duplicate.

The measured performance of the amplifier is shown in figures 1, 2, and 3 and harmonic rejection data in table I.

Table I. Output harmonic contents, measured at 300-W CW (all test data taken using a tuned output, narrow band signal source).

	2nd	3rd	4th	5th
f (Mhz)	(dB below the carrier)			
30.0	−38	−25	−34	−48
20.0	−33	−13	−43	−45
15.0	−50	−10	−51	−47
7.50	−40	−30	−55	−47
4.0	−37	−22	−55	−37
2.0	−36	−18	−45	−37

*A similar product is available from Fair-Rite Products Corp., Wallkill, N.Y., 12589

®Registered trademark of DuPont

PCB, chips capacitors, transformers T_1, T_2, T_3, and ferrite beads are available from: COMMUNICATIONS CONCEPTS, 2648 N. Aragon Ave., Kettering, Ohio 45420. Telephone: (513) 294-8425.

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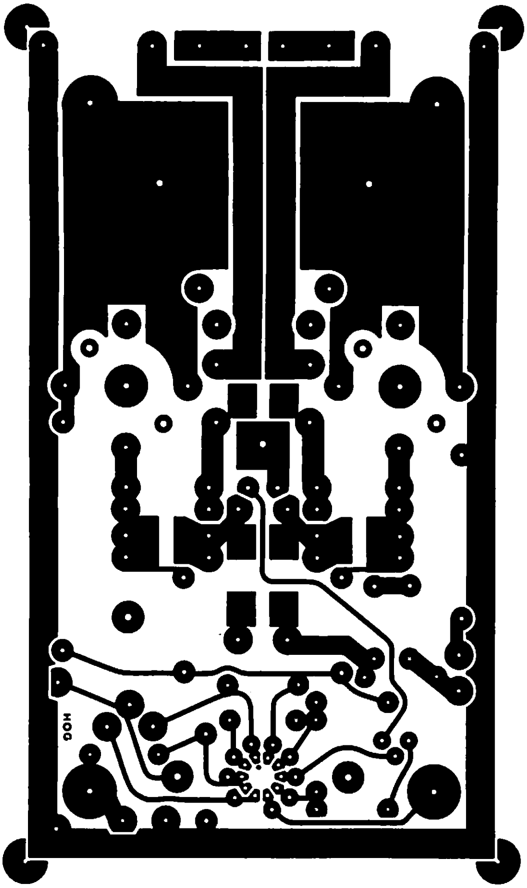
NOTE: The Printed Circuit Board shown is 75% of the original.



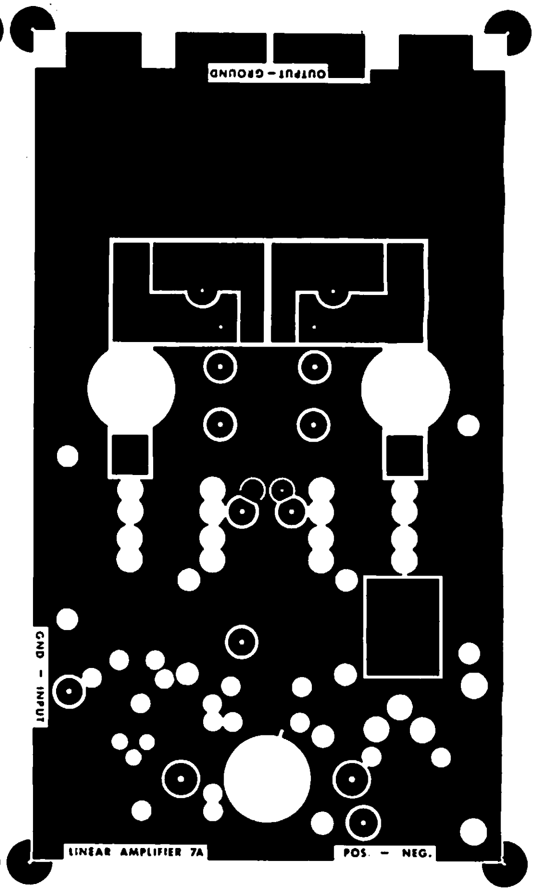


Figure 2 — IMD vs Frequency

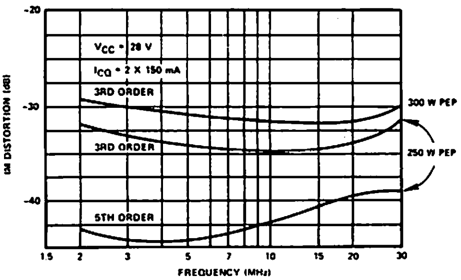
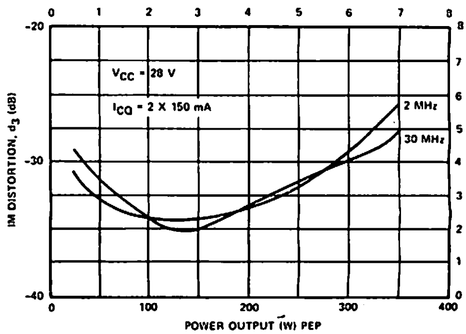
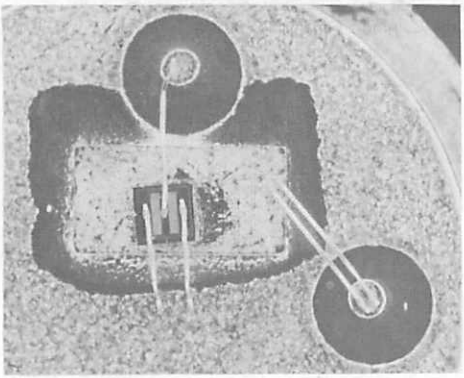


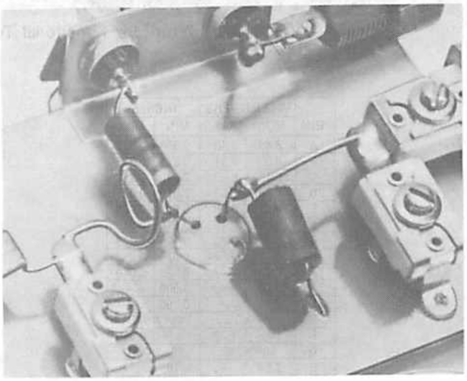
Figure 3 — IMD vs Power Output



THE COMMON EMITTER TO-39 AND ITS ADVANTAGES

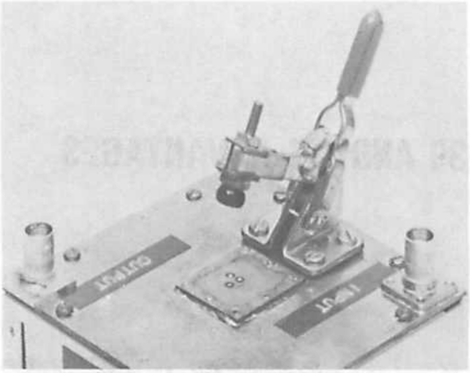
Prepared By Rich Potyka

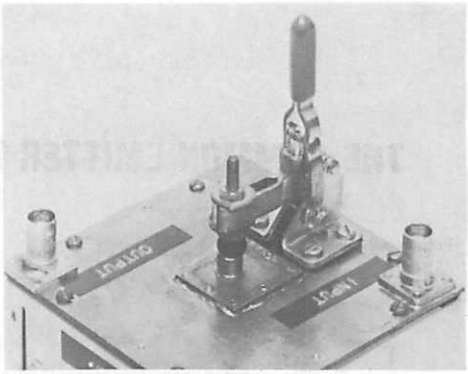




The common emitter TO-39 package is one of Motorola's latest innovations in low-cost rf packages. It differs from conventional TO-39's or TO-5's in that the emitter, not the collector, is connected to the metal case. To achieve this, a BeO insulating block metallized on top and bottom is brazed to the can bottom and the transistor chip brazed to the BeO insulator. Wires are then bonded from the chip and insulator block to the terminals and the can bottom as shown in the photo. With NPN transistors, this configuration permits direct connection of the can to rf and negative dc ground for many class B and C circuits.

Two important advantages can be derived from the common emitter TO-39: By connecting the case to the rf circuit ground, emitter inductance is reduced and gain increased by 3 to 5 dB over that of comparable, conventionally wired transistors. And the case may be directly pressed, clipped, or soldered to the heat sink with no effect on rf performance. This feature may eliminate the need for the heat radiating "coolers" because soldering the transistor bottom to the circuit, typically a PC board, improves dissipation by removing heat through the thick metal base rather than the thin can.



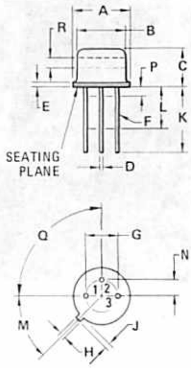


Fixture for Functional Testing of the Common Emitter TO-39

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39



STYLE 5:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

For example, the MRF227 was mounted in this manner and a θ_{jc} of 15°C/W was measured using a Barnes RM-2A Infrared Microscope. Compared to an MRF607 in a conventional package operating under identical conditions, this is greater than a 2:1 reduction in thermal resistance. And as side benefits, the lower θ_{jc} also reduces power slump and improves reliability.

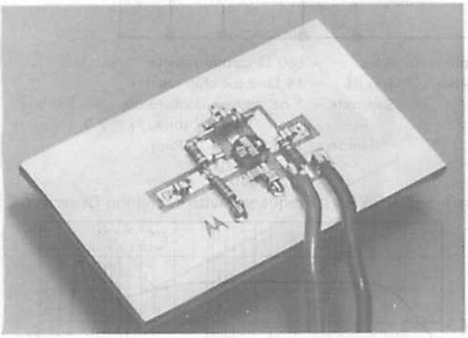
In many mobile radios CE-TO39 devices can replace stud or flange mounted stripline parts used for 1- to 4-watt drivers. This conversion should normally offer a significant savings in the cost of parts as well as the costs of mounting hardware and labor.

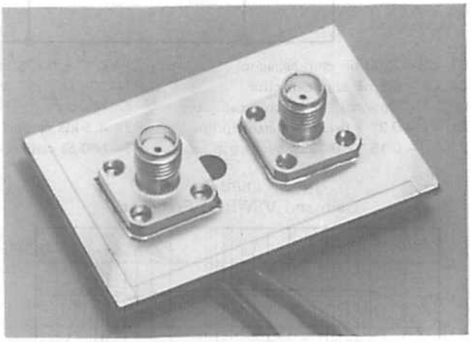
The designer of compact handheld radio equipment will find the CE-TO39 offers a real advantage from the elimination of interstage RFI or coupling because the can is at rf ground. Stability is usually improved and the higher available gain may reduce the number of transmitter stages. Simplified and improved cooling may also be obtained by connecting the can directly to the radio housing or chassis.

To sum it up: The emitter-to-can wired TO-39 known as the CE-TO39 offers the designer significant improvements in both gain and thermal performance. Because of its price, compared to SOE and TO-60 packages, the designer can use the CE-TO39 to reduce costs. And he can make his design easier to assemble with no loss in rf performance.

AMPLIFIER GAINS 10 dB OVER NINE OCTAVES

Prepared by:
Mike Hadley
Industrial Applications Engineer





The introduction of Motorola encapsulated transistors fabricated with ion-implanted arsenic emitters has made a reality of economical small-signal amplifiers with bandwidths exceeding 1 GHz. The recently developed MRF901, an example of this technology, has an f_T exceeding 4.5 GHz, and a maximum noise figure at 1 GHz of 2.5 dB. The device package (case 302) employs the Motorola dual emitter bonding concept to minimize parasitic inductance and enhance high-frequency performance.

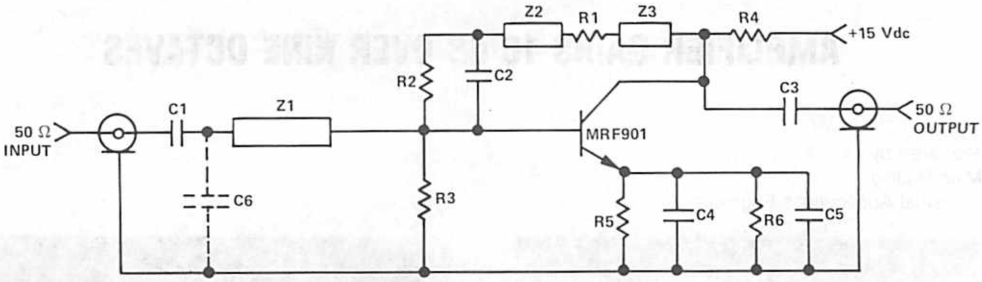
Using the MRF901, an amplifier has been developed which exhibits a nominal gain of 10 dB over nine octaves of bandwidth. The circuit design is a class A amplifier employing both ac and dc feedback. Bias is stabilized at 15 mA of collector current using dc feedback from the collector. The ac feedback from collector to base, and in each of the partially bypassed emitter circuits, compensates for the increase in device gain with decreasing frequency, yielding a flat response over a maximum bandwidth. Transistor S parameters, as provided by the MRF901 data sheet, and computer-aided circuit optimization techniques were used to choose component values for gain flatness, input VSWR and output VSWR. The described performance was achieved using common high-frequency amplifier construction techniques and a standard printed circuit board substrate. Even better results could be expected from the use of today's hybrid circuit technology.

Evaluation of the amplifier shows a nominal 10 dB power gain from 3 MHz to 1.4 GHz. With only a minimum matching network used at the amplifier input, the input VSWR remains less than 2.5:1 to approximately 1 GHz while the output VSWR stays under 2:1 to approximately 1.4 GHz (figure 2). If input impedance matching were of prime consideration, connecting a 2.1 pF capacitor from the junction of C1 and Z1 to ground (C6 in figure 1) would hold input VSWR below 2.2:1 over the complete frequency range (figure 3). Note that a slight degradation in gain flatness and output VSWR occurs with the addition of C6. A more elaborate network design would probably optimize impedance matching while maintaining gain flatness.

The amplifier was built on a glass Teflon® printed circuit board 1.8″ x 1.2″. A 2:1 reproduction of the circuit pattern is provided in figure 4. The type OSM215 50-ohm input and output connectors were mounted opposite the component side to facilitate laboratory measurements. Board size could be reduced to approximately half by reducing the ground plane around the circuit perimeter. A combination of chip capacitors, chip resistors and standard carbon resistors were used to obtain maximum performance at minimum cost.

Extra care was taken to keep all component lead lengths to an absolute minimum and to provide a good ground plane. In the interest of maintaining a good ground, copper foil was soldered at the board edges to connect the top and bottom circuit grounds, and an eyelet was inserted near each emitter lead.

Figure 1. Schematic Diagram



C1–C3 – 2200 pF chip capacitor
C4, C5 – 6.5 pF chip capacitor
C6 – Optional 2.1 pF chip capacitor
Z1 – 0.3" x 0.125" microstrip line
Z2 – 0.15" x 0.125" microstrip line
Z3 – 0.3" x 0.125" microstrip line
R1 – 200 Ω, 1/8" W, ±5% carbon resistor
R2 – 4.3 kΩ carbon resistor
R3 – 680 Ω carbon resistor
R4 – 560 Ω carbon resistor
R5, R6 – 15 Ω ±5% chip resistor
Substrate – 1 oz. copper, double-sided glass Teflon® board 0.0625" thick, $\epsilon_r \approx 2.5$

® Registered trademark of DuPont

Figure 2.
Gain and VSWR vs Frequency

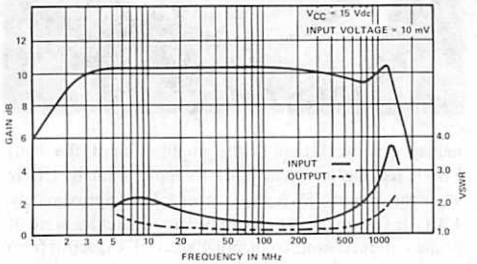


Figure 3.
Gain and VSWR vs Frequency with Matching Capacitor C6

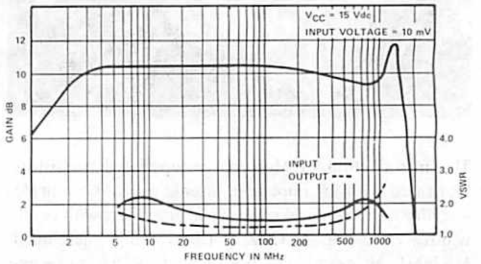


Figure 4. Amplifier PCB Artwork

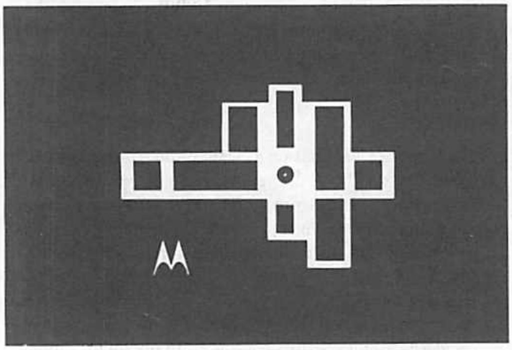
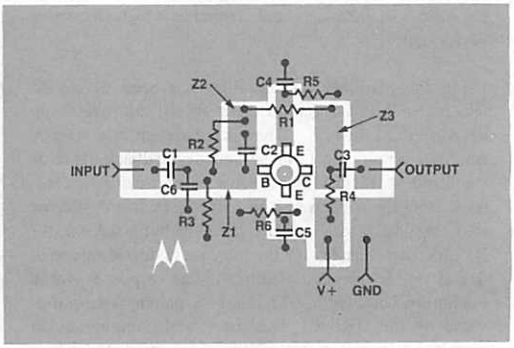


Figure 5. Parts Layout



MEASURING THE INTERMODULATION DISTORTION OF LINEAR AMPLIFIERS

Prepared by
Helge Granberg
Circuits Engineer, SSB

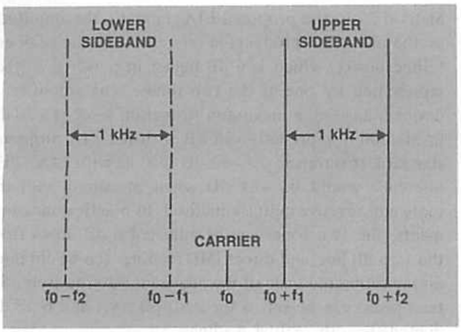
The measured distortion of a linear amplifier, normally called Intermodulation Distortion (IMD), is expressed as the power in decibels below the amplifier's peak power or below that of one of the tones employed to produce the complex test signal.

A signal of three or more tones is used in certain video IMD tests, but two tones are common for HF SSB. The two-tone test signal provides a standard, controlled test method, whereas the human voice contains an unknown number of frequencies of various amplitudes and couldn't be used for accurate power and linearity measurements. Separation of the two tones, for voice operation equipment, may be from 300 Hz to 3 kHz, 1 kHz being a standard adopted by the industry.

Generation of the Test Signal

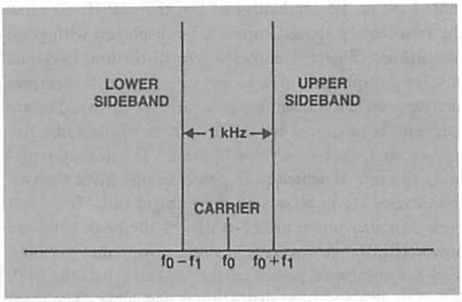
The two-tone IMD test signal can be generated by a number of means of which the following three are the most common:

System A–A two-tone audio signal is formed by algebraically adding two sine wave voltages of equal amplitude which are not harmonically related, e.g., 800 Hz and 1.8 kHz. This two-tone audio signal is fed into a balanced modulator together with an RF carrier, one sideband filtered out, and the resultant further mixed to the desired frequency and then amplified. The system is useful in testing complete SSB transmitters. A commercial transmitter can also be used as a signal source for testing linear amplifiers.



SYSTEM A

System B–In this method, a signal of approximately 500 Hz is fed into a balanced modulator together with an RF carrier and amplified to the required power level.



SYSTEM B

The resultant is a double-sideband signal that resembles a single-sideband signal generated under two-tone sine wave conditions. Viewed on a scope screen, the envelope produced by this method appears the same as a SSB two-tone pattern. However, unlike the System A test signal, there is a controlled and fixed phase relationship between the two output tones. This system is widely employed to generate the test signal for linearity measurements.

System C–Two equal amplitude RF signals, separated in frequency by 1 kHz, are algebraically added in a hybrid coupler. The isolation between input ports must be high enough to avoid interaction between the two RF signal generators. Short-term stability (jitter) should be

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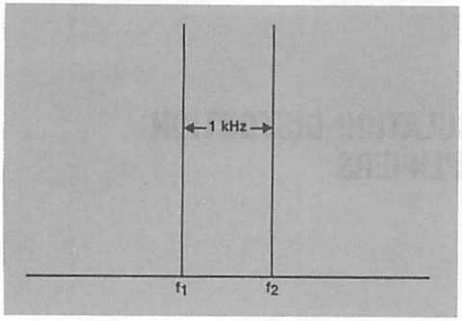


SYSTEM C

less than one part per million at 30 MHz. The carrier is nonexistent as compared to A and B, and the two-tone signal is generated as the RF voltages cancel or add at the rate of their difference frequency according to their instantaneous phase angles. Because no active components are involved, very low IM distortion is achievable. This system is useful in applications where low distortion and low power levels are required.

Except for the position of the carrier in respect to the two tones, displays of the signals produced by systems A, B and C appear identical on a spectrum analyzer screen. Sometimes, however, the suppressed carrier may remain below the noise level of the instrument. Any spectrum analyzer used for SSB linearity measurements must have an IF bandwidth of less than 50 Hz to allow the two closely spaced tones to be displayed with good resolution. Figure 1 shows a low distortion, two-tone envelope displayed on a scope screen. On a spectrum analyzer screen the same signal displays as two discrete frequencies separated by the difference of the audio frequency or frequencies. See figure 2. The display represents the rate at which peak power occurs when the two frequencies are in phase and the voltages add. Thus, one peak contains one-fourth (–6 dB) of the peak envelope power (PEP). An average reading power meter would read the combined power of the tones, or half the PEP, assuming the envelope distortion is negligible. The third order distortion products (d_3), fifth order (d_5), etc., can be seen on each side of the tones. The actual power (PEP) of each distortion product can be obtained by deducting the number of decibels indicated by the analyzer from the average power. This value may be useful in determining the linearity requirements of the signal source. While the maximum permissible distortion levels of the driver stages in a multi-stage amplifier may be difficult to specify, a 5- to 6-dB margin is usually considered sufficient.

Types of Distortion

The nonlinear transfer characteristics of active devices are the main cause of amplitude distortion, which is both device and circuit dependent. On the other hand, harmonic and phase distortion, also present in linear amplifiers, are predominantly circuit dependent. Even order harmonics, particularly noticeable in broadband designs, cause the harmonic distortion. Push-pull design will eliminate most of the even-order-caused harmonic distortion and the driver stages, where efficiency is of less concern, can be biased to class A.

Phase distortion can be caused by any amplitude or frequency sensitive components, such as ceramic capacitors or high-Q inductors, and is usually present in multi-stage amplifiers. This distortion may have a positive or negative sign, resulting in occasions where the level of some of the final IMD products (d_3 or d_5, or both) may be lower than that of the driving signal, due to cancelling effects of opposite phases. Actual levels depend on the relative magnitude of each distortion product present.

From the above it is apparent that the distortion figures presented by the spectrum analyzer represent a combination of amplitude, harmonic and phase distortion.

Measurement Standards

As indicated earlier, there are two standard methods of measuring the IM distortion:

Method 1–In military standard (1131 A-2204B), the distortion products are referenced to one of the two tones of the test signal. The maximum permissible IMD is not specified but, numbers like –35 dB are not uncommon in some equipment specifications. However, when this measuring system is employed in industrial applications, the IMD requirement (d_3) is usually relaxed to –30 dB. Figure 3 shows the frequency spectrum of IM distortion products and their relative amplitudes for a typical class AB linear amplifier. Biasing the amplifier more toward class B will cause the lower order distortion products to go down and the amplitudes of the higher order products to increase. There is a bias point where the d_3 and d_5 products become equal resulting in 2–5 dB improvement in the lower order IMD readings.

Method 2–In the proposed EIA standard, the amplitude of the distortion products is referenced to the peak envelope power, which is 6 dB higher in power than that represented by one of the two tones. The amplifier or device indicating a maximum distortion level of –30 dB in Method 1 represents –36 dB with the EIA proposed standard. Conversely, a –30 dB reading with EIA's PEP reference would be –24 dB when measured with the more conservative military method. In practical measurements, the two tones can be adjusted 6 dB down from the zero dB line, and direct IMD readings can be obtained on the calibrated scale of the analyzer. Alternatively, the tone peaks can be set to the zero dB level and 6 dB deducted from the actual reading.

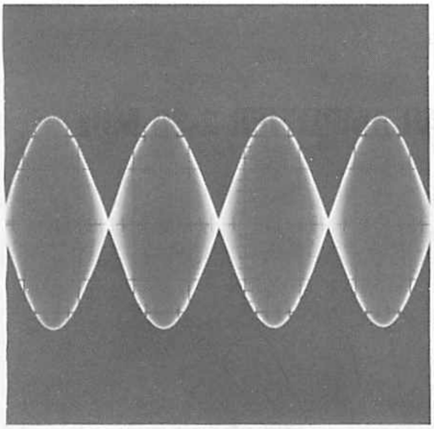


FIGURE 1. Two-tone test pattern generated by A, B or C.

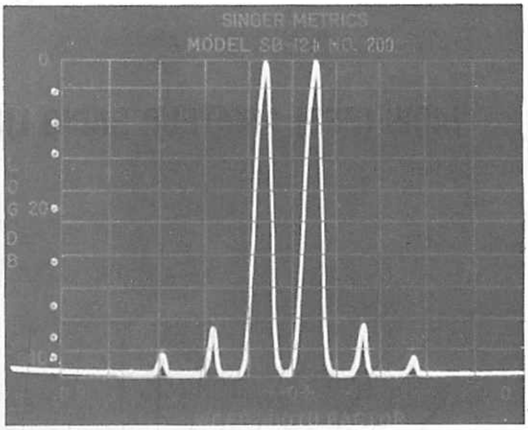


FIGURE 2. Test signal of figure 1 displayed by a spectrum analyzer. 3rd and 5th order distortion products are visible.

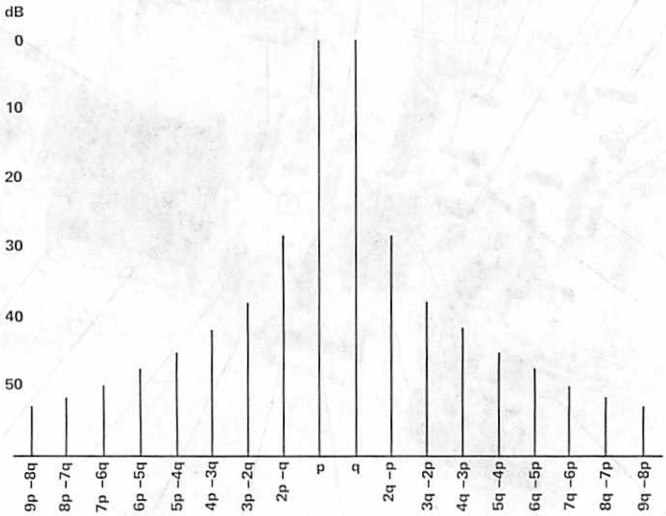


FIGURE 3. Typical distribution of distortion product amplitudes compared to the two fundamental frequency components.

The military standard, with the relaxed −30 dB IMD specification, is employed by most manufacturers of high power commercial transmitters and marine radio base stations. *The EIA measuring method is used by the majority of ham radio equipment and CB radio manufacturers. It is also used to measure IMD in various mobile radio applications operating from a 12.5-V nominal dc supply.

Because of the importance to your design, data sheets of the newer generation Motorola devices specify linearity tests appropriate to the expected application of the particular device and test conditions are always indicated.

*FCC specifications are now in effect covering maximum permissible distortion up to the 11th order products.

REFERENCES:

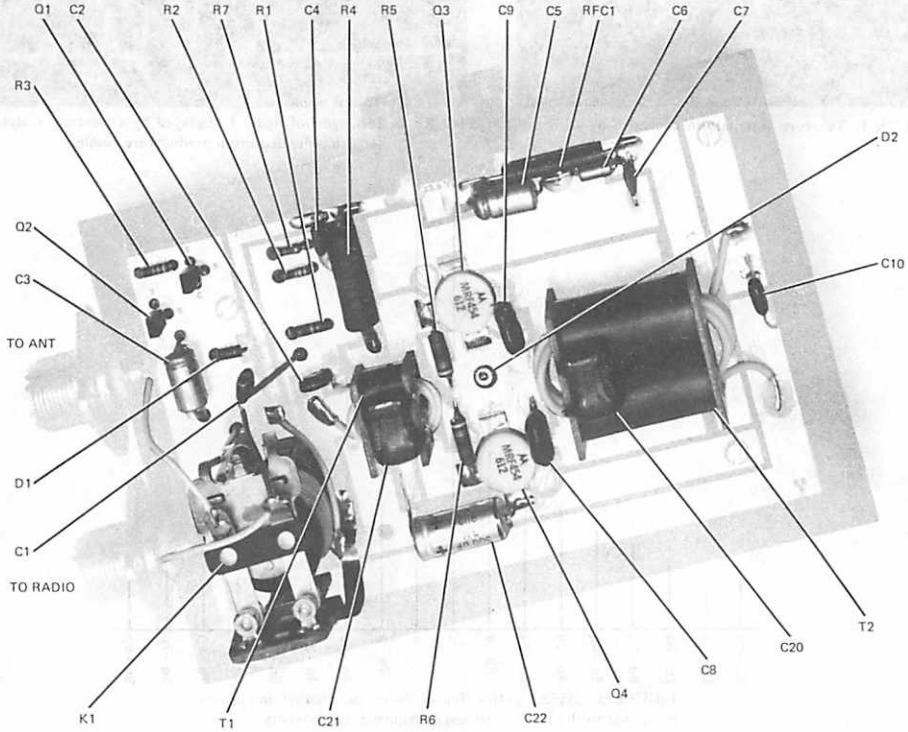
Pappenfus, Brueue & Schoenike, "Single-Sideband Principles and Circuits," McGraw-Hill.

William I. Orr, "Radio Handbook," 18th Edition, Editors and Engineers, Ltd.

Stoner, Goral, "Marine Single-Sideband," Editors and Engineers, Ltd.

Hooton, "Single-Sideband, Theory and Practice," Editors and Engineers, Ltd.

140W (PEP) AMATEUR RADIO LINEAR AMPLIFIER 2-30 MHz



The popularity of 2-30 MHz, SSB, Solid State, linear amplifiers is increasing in the amateur market. This EB describes an inexpensive, easy to construct amplifier and some pertinent performance information. The amplifier uses two MRF454 devices. These transistors are specified at 80 Watts power output with 5 Watts of input drive, 30 MHz, and 12.5 Vdc. The MRF454 is used because it is a readily available device and has the high saturation power and ruggedness desired for this application. This device is not characterized for SSB. However, IMD specs for the amplifier are shown in Figures 2 and 3.

THE AMPLIFIER

The performance of the amplifier can be seen in Figures 1, 2, 3, 5, 6, 7 and 8. The quiescent current is 500 mA on each device. This amount of bias was needed to prevent "cross over" at the higher output powers during SSB operation. The amplifier operates across the 2-30 MHz band with relatively flat gain response and reaches gain saturation at approximately 210 Watts of output power. Figure 5 depicts the amplitude modulated waveform with respect to a 100-Watt carrier. Figure 6 depicts the increased amplitude modulation at 50-Watt carrier. In both cases the peak output power is equal to approximately 210 Watts due to the saturation of the MRF454. The 50-Watt carrier is thus recommended in any amplitude modulated applications.

The bias diode D2 has been mounted in the heatsink for temperature tracking. The cathode is pressed into the heatsink and the anode extends through the circuit board. (See Figure 9.) Both input and output transformers are 4:1 turns ratio (16:1 impedance ratio) to achieve low input SWR across the specified band and a high saturation capability. T1* is made from FairRite Products, ferrite beads, material #77, .375" O.D. × .187/.200" I.D. × .44L". T2* is made from Stackpole Co. ferrite sleeves #57-3238-7D.

When using this design, it is important to interconnect the ground plane on the bottom of the board to the top; especially at the emitters of the MRF454s. Eyelets were used in this design, which are easier to apply, but #18 AWG wire can be used. On the photomask, (see Figure 10) ":" signifies where the ground plane has been interconnected. The letter "O" designates where the 4–40 screws are installed to fasten the board to the heatsink. 6–32 nuts are used as spacers on the 4–40 screws between the board and the heatsink to keep the board from touching the heatsink.

THE DESIGN

This amplifier was designed for simplicity. The design goal was to allow repeatability of assembly and reduce the number of components used. The amplifier will accept Single Side Band or Amplitude Modulation without external switching. A carrier operated relay circuit is on the same layout to make this an easy amplifier to add on to any suitable radio with an RF output of 1.0–5.0 Watts. All components used are readily available at most distributors and are relatively inexpensive.

*Ref: Application Notes
AN749 BroadBand Transformers and Power Combining Techniques for RF – H. Granberg
AN762 Linear Amplifiers for Mobile Operation – H. Granberg

NOTE: Parts and Kits for this amplifier are available from:

Communications Concepts
121 Brown St.
Dayton, Ohio 45402
(513) 220-9677

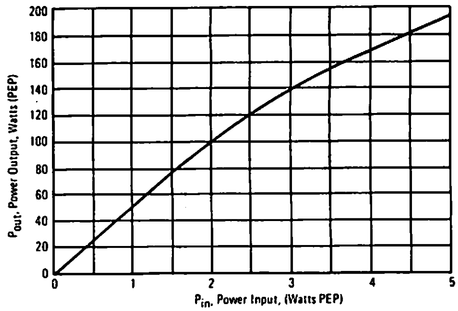


FIGURE 1–P_{out} vs. P_{in}, 30 MHz, 13.6 Vdc

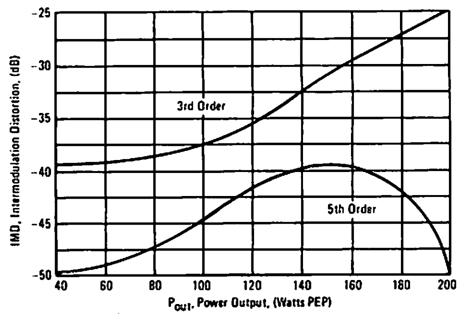


FIGURE 2–Intermodulation Distortion Versus P_{out}, 30 MHz, 13.6 Vdc

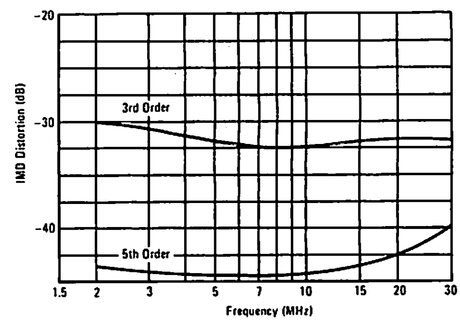
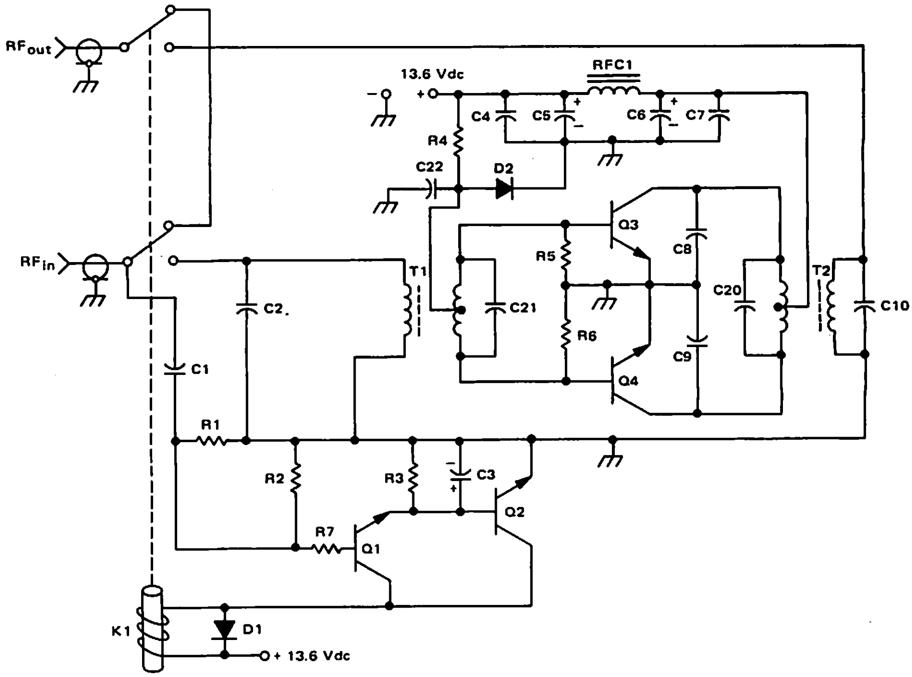


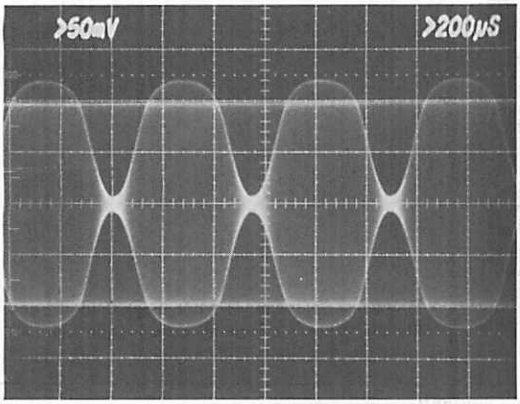
FIGURE 3–IMD vs. Frequency, P_{out} = 140 Watt PEP 13.6 Vdc



C1 = 33 pF Dipped Mica
C2 = 18 pF Dipped Mica
C3 = 10 μF 35 Vdc for AM operation,
100 μF 35 Vdc for SSB operation.
C4 = .1 μF Erie
C5 = 10 μF 35 Vdc Electrolytic
C6 = 1 μF Tantalum
C7 = .001 μF Erie Disc
C8, 9 = 330 pF Dipped Mica
R1 = 100 kΩ 1/4 W Resistor
R2, 3 = 10 kΩ 1/4 W Resistor
R4 = 33 Ω 5 W Wire Wound Resistor
R5, 6 = 10 Ω 1/2 W Resistor

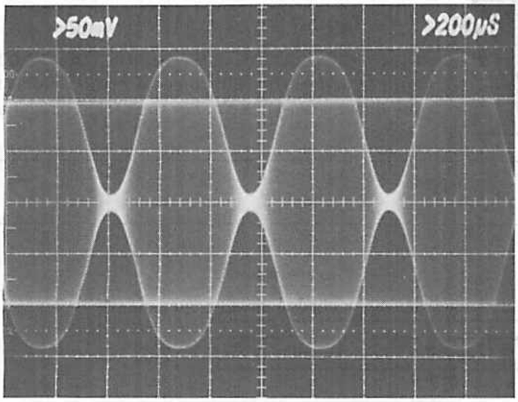
R7 = 100 Ω 1/4 W Resistor
RFC1 = 9 Ferroxcube Beads on #18 AWG Wire
D1 = 1N4001
D2 = 1N4997
Q1, Q2 = 2N4401
Q3, 4 = MRF454
T1, T2 = 16:1 Transformers
C20 = 910 pF Dipped Mica
C21 = 1100 pF Dipped Mica
C10 = 24 pF Dipped Mica
C22 = 500 μF 3 Vdc Electrolytic
K1 = Potter & Brumfield
KT11A 12 Vdc Relay or Equivalent

FIGURE 4—Schematic Diagram



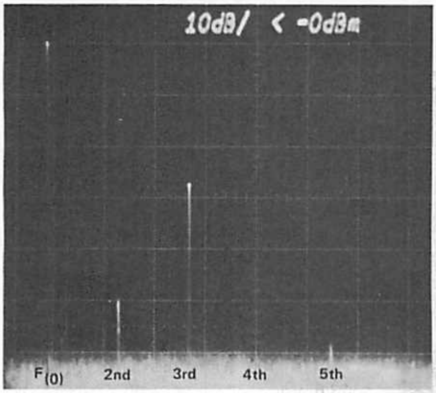
Amplitude Modulated Waveform with Superimposed Carrier. Carrier Conditions: $f = 30$ MHz; $P_{in} = 2.2$ Watts; $P_{out} = 100$ Watts (carrier); $V_{CC} = 13.6$ Vdc

FIGURE 5



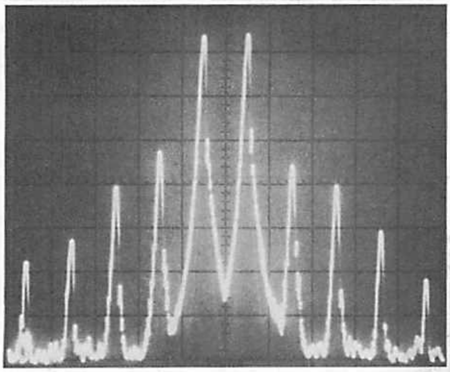
Amplitude Modulated Waveform with Superimposed Carrier. Carrier Conditions: $f = 30$ MHz; $P_{in} = 1.3$ Watt; $P_{out} = 50$ Watts; $V_{CC} = 13.6$ Vdc

FIGURE 6



Frequency Spectrum, 30 MHz ($F_{(0)}$, 2nd, 3rd, and 5th harmonics are visible). Vertical resolution: 10 dB/div. Horizontal 20MHz/div.

FIGURE 7



INTERMODULATION DISTORTION, 30, 30.001 MHz (3rd, 5th, 7th, 9th) order distortion products are visible. Vertical resolution: 10 dB/div. Horizontal: 1KHz/div.

FIGURE 8

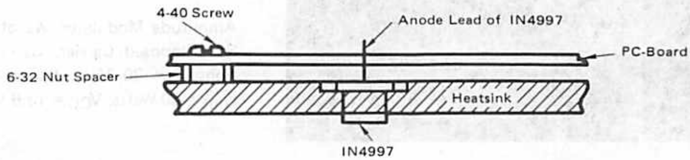
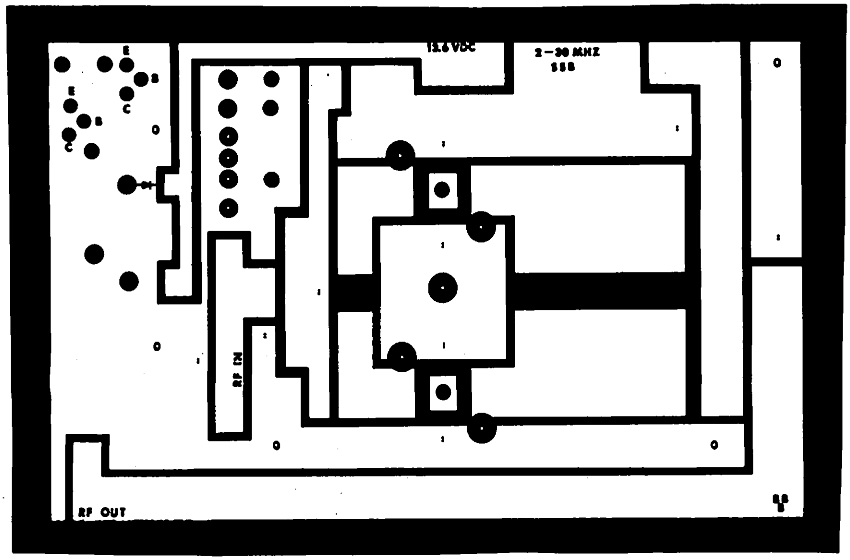


FIGURE 9 – Mounting Detail of IN4997 and 6-32 Nut (Spacer)



NOTE: The Printed Circuit Board shown is 75% of the original.

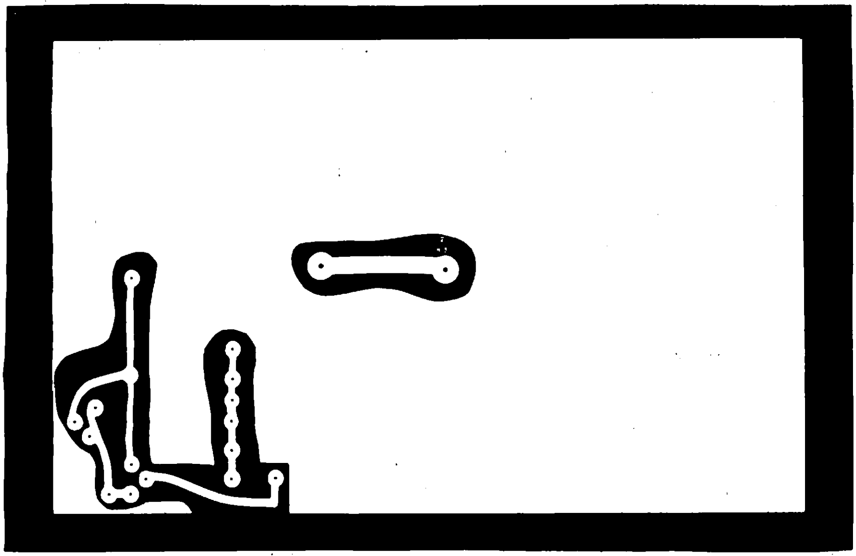


FIGURE 10— Photomaster (Positive)

Note: The use of this amplifier is illegal for Class D Citizen Band service.

A 10 WATT 225–400 MHz AMPLIFIER — MRF331

Prepared by
Dave Hollander
RF Power Engineering

This bulletin describes a broadband amplifier covering the 225–400 MHz military communications band producing 10 watt RF output power and operating from a 28 volt supply. The amplifier can be used as a driver for higher power devices such as 2N6439 and MRF327. Typical performance curves are shown in Figures 5, 6, and 7.

Circuit Description

The circuit is designed to be driven by a 50 ohm source and operate into a nominal 50 ohm load. The input matching network[1] consists of a π-section composed of C3, C4, Z2, C5 and C6. C2 is a dc blocking capacitor, and T1 is a 4:1 impedance ratio coaxial transformer. Z1 is a 50 ohm transmission line. A compensation network consisting of R1, C1, and L1 is used to improve the input VSWR and flatten the gain response of the amplifier. L2 and a small ferrite bead make up the base bias choke.

The output network is made up of a microstrip L-section consisting of Z3 and C7, and a high pass section consisting of C8 and L3. C8 also serves as a dc blocking capacitor.

Collector decoupling is accomplished through the use of L4, L5, C9, C10, C11, C12, and C13.

Construction

The circuit is constructed on a 3.375 × 2.5 inch (8.57 × 6.35 cm) double sided PC board. Board material is 3M Glass Teflon,* with a thickness of 0.031 inch (0.0787 cm). Glass Teflon was selected for its low loss and dielectric consistency. Figure 2 is a 1:1 scale photomaster print of the top side of the board. Eyelets are placed at the points marked by plus signs. The eyelets are soldered to both sides of the PCB to control ground current return paths. The edges of the transistor mounting hole beneath the emitter leads are also wrapped, using copper foil soldered in place to insure a solid emitter ground.[2,3] Due to a ground imbalance caused by the transformer, a component placement layout of the RF circuitry is shown in Figure 1. It is important that this layout is followed in order to duplicate performance. Construction details of the 4:1 transformer are shown in Figure 4.

*Registered Trademark of Dupont

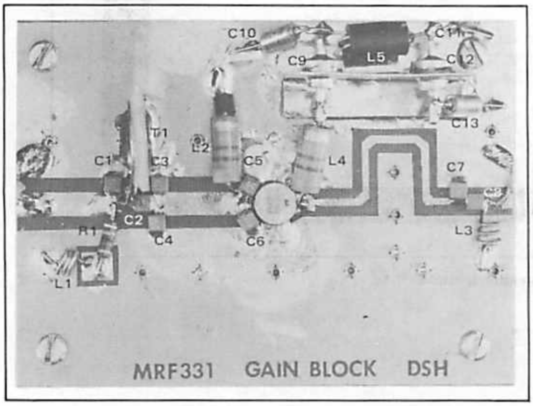
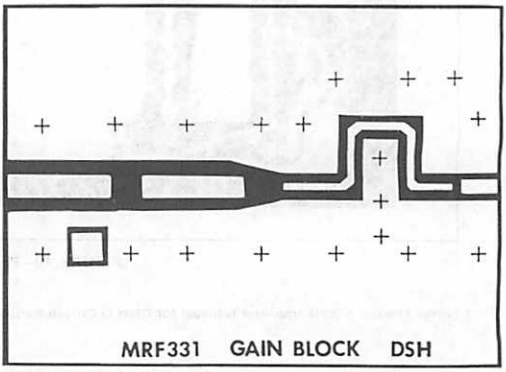


FIGURE 1 — Component Layout of the Amplifier



NOTE: The Printed Circuit Board shown is 75% of the original.
FIGURE 2 — Printed Circuit Board Layout

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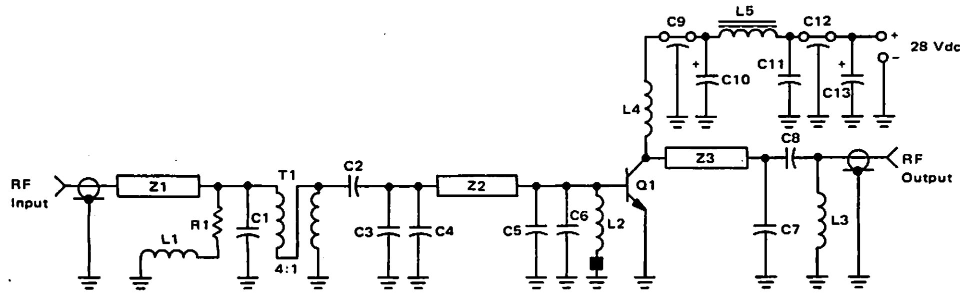

C1 – 8.2 pF Chip*
C2 – 270 pF Chip*
C3 – 36 pF Chip*
C4, C7 – 15 pF Chip*
C5, C6 – 50 pF Chip*
C8 – 82 pF Chip*
C9, C12 – 680 pF Feedthru
C10, C13 – 1.0 μF 50 V Tantalum
C11 – 0.1 μF Erie Redcap

L1, L3 – 3 Turns #22 AWG 1/8" (3.175 mm) ID
L2 – 0.15 μH Molded Choke
L4 – 0.15 μH Molded Choke with Ferroxcube Bead (Ferroxcube 56-590-65/4B on Ground End of Choke)
L5 – Ferroxcube VK200-19/4B

*100 mil A.C.I. Chip Capacitors

R1 – 36 Ω 1/4 Watt

T1 – 25 Ω Subminiature Coax (Type UT34-25) – 1.75 inches (44.45 mm) long

Z1 – Microstrip Line
720 mils L X 162 mils W
18.29 mm L X 4.115 mm W

Z2 – Microstrip Line
680 mils L X 162 mils W
17.27 mm L X 4.115 mm W

Z3 – Microstrip Line
2200 mils L X 50 mils W
55.88 mm L X 1.27 mm W

Board – 0.0625" (1.588 mm) Glass Teflon, ϵ_r = 2.56

Q1 – MRF331

FIGURE 3 — Schematic Diagram and Component List

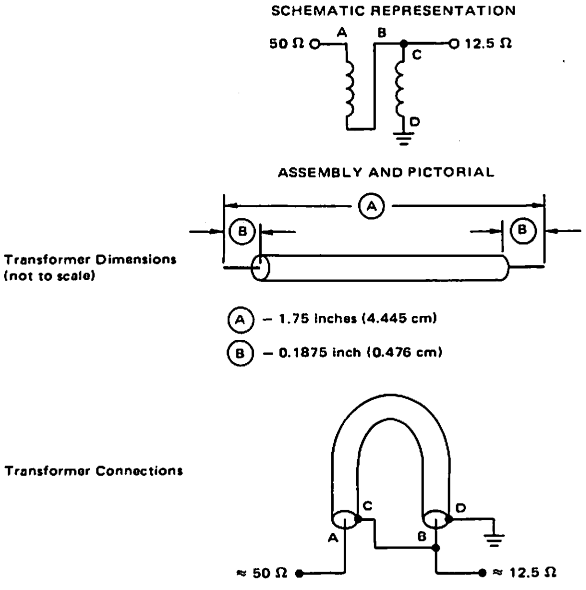

FIGURE 4 — Construction Details of 4:1 Impedance Ratio Transformer

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AMPLIFIER PERFORMANCE

FIGURE 5 — Power Gain and Efficiency versus Frequency

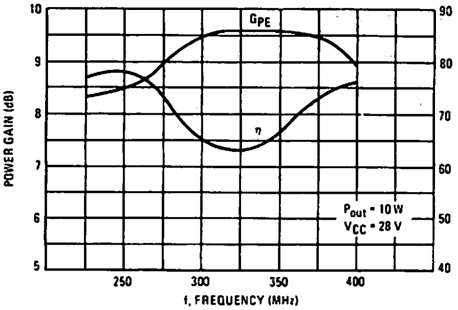


FIGURE 6 — Output Power versus Input Power

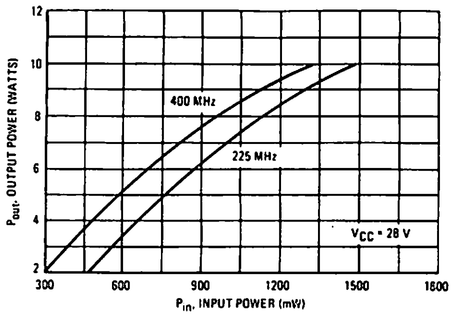
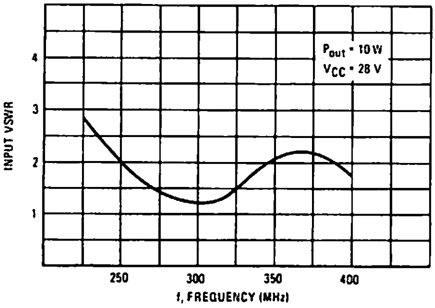


FIGURE 7 — Input VSWR versus Frequency



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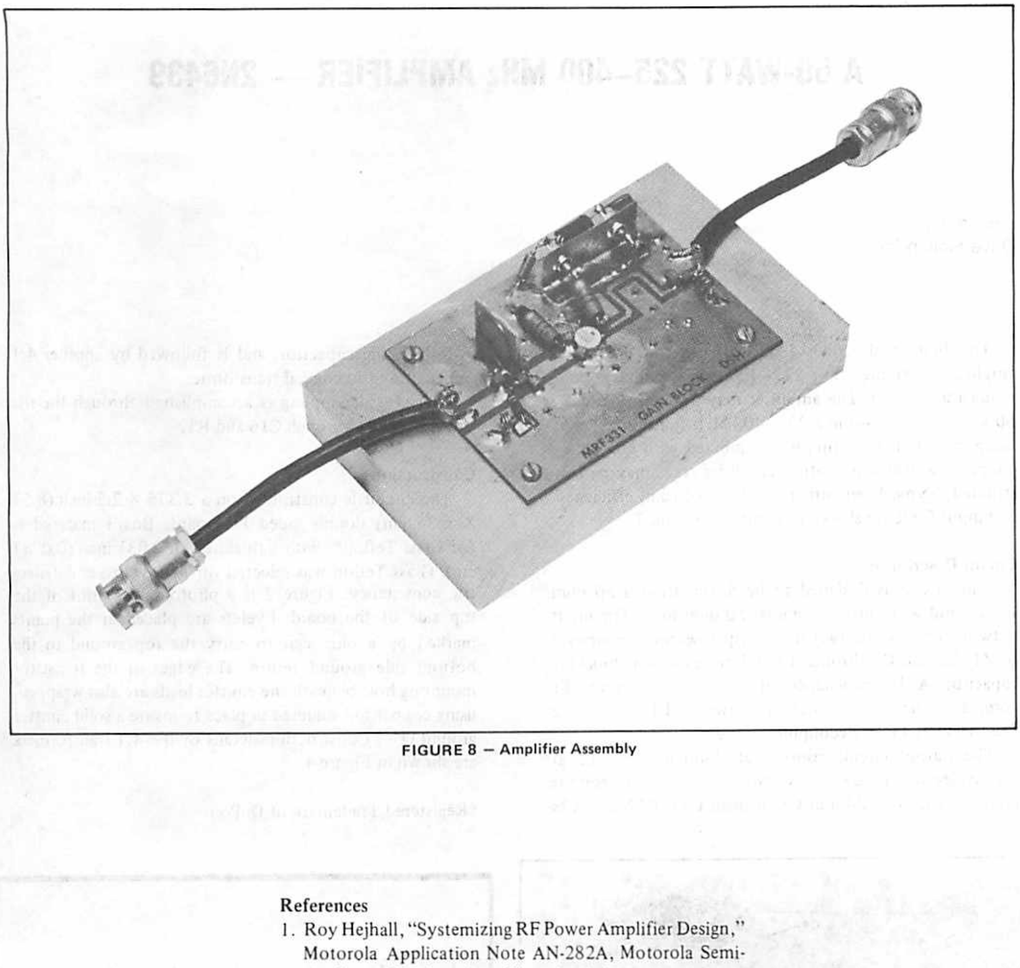


FIGURE 8 – Amplifier Assembly

References

1. Roy Hejhall, "Systemizing RF Power Amplifier Design," Motorola Application Note AN-282A, Motorola Semiconductor Products Inc., Phoenix, Arizona.
2. "Mounting Stripline – Opposed Emitter (SOE) Transistors," Motorola Application Note AN-555, Motorola Semiconductor Products Inc., Phoenix, Arizona.
3. Glenn Young, "Microstrip Design Techniques for UHF Amplifiers," Motorola Application Note AN-548A, Motorola Semiconductor Products Inc., Phoenix, Arizona.

A 60-WATT 225–400 MHz AMPLIFIER — 2N6439

Prepared by
Dave Hollander

This bulletin describes a 60 watt, 28 volt broadband amplifier covering the 225–400 MHz military communications band. The amplifier may be used singly as a 60 watt output stage in a 225–400 MHz transmitter, or by using two of these amplifiers combined with quadrature couplers, a 100 watt output amplifier stage may be constructed. Typical performance curves of gain, efficiency, and input SWR are shown in Figures 5, 6, and 7.

Circuit Description

This circuit is designed to be driven from a 50 ohm source and work into a nominal 50 ohm load. The input network consists of two microstrip L-sections composed of Z1, Z2 and C2 through C6. C1 serves as a dc blocking capacitor. A 4:1 impedance ratio coaxial transformer T1 completes the input matching network. L1 and ferrite bead serve as a base decoupling choke.

The output circuit consists of shunt inductor L2 at the collector, followed by two microstrip L-sections composed of Z3, Z4 and C8 through C11. C12 serves as a dc blocking capacitor, and is followed by another 4:1 impedance ratio coaxial transformer.

Collector decoupling is accomplished through the use of L3, L4, C14 through C16 and R1.

Construction

The circuit is constructed on a 3.375 × 2.5 inch (8.57 × 6.35 cm) double sided PC board. Board material is 3M Glass Teflon*, with a thickness of 0.031 inch (0.0787 cm). Glass Teflon was selected for its low loss and dielectric consistency. Figure 2 is a photomaster print of the top side of the board. Eyelets are placed at the points marked by a plus sign to carry the top ground to the bottom side ground return. The edges of the transistor mounting hole beneath the emitter leads are also wrapped, using copper foil soldered in place to insure a solid emitter ground.[1,2] Construction details of the 4:1 transformers are shown in Figure 4.

*Registered Trademark of DuPont

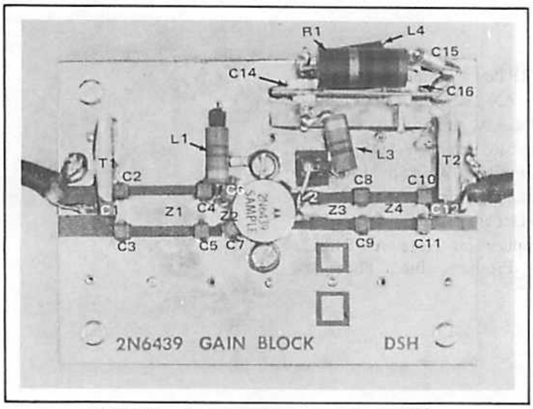
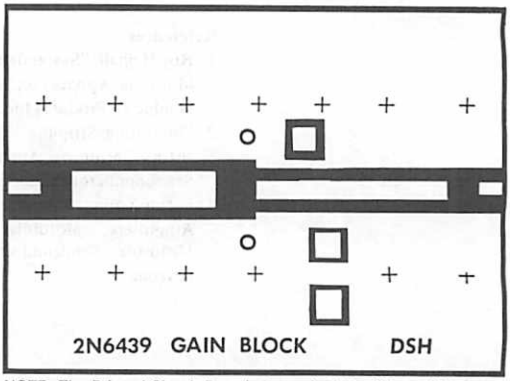
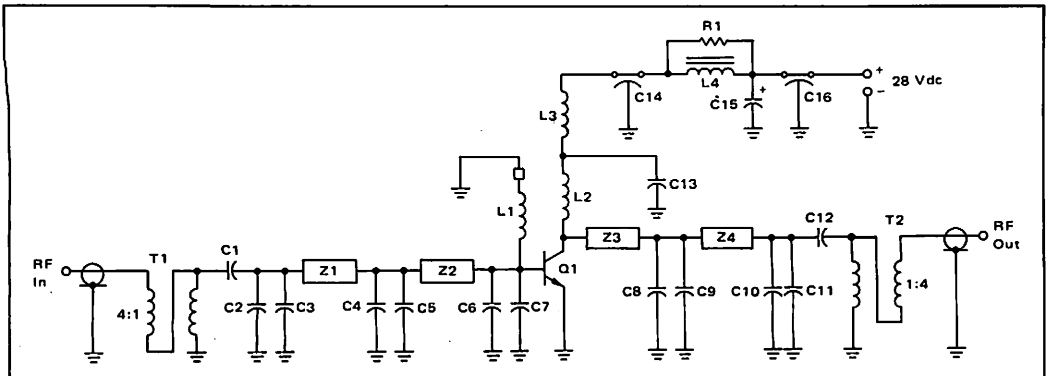


FIGURE 1 — Component Layout of the Amplifier



NOTE: The Printed Circuit Board shown is 75% of the original.
FIGURE 2 — Photomaster of Circuit Board



C1 – 63 pF Chip
C2, C8 – 27 pF Chip
C3 – 24 pF Chip
C4 – 15 pF Chip
C5, C9 – 30 pF Chip
C6, C7 – 50 pF Chip
C10 – 10 pF Chip
C11 – 5.1 pF Chip
C12 – 150 pF Chip
C13 – 270 pF Chip
C14, C16 – 680 pF Feedthru
C15 – 1.0 μF 50 V Tantalum

All Chip Capacitors are 100 mil TDK-ACI Co, Style FC282 BAG
L1 – 0.15 μH Molded Choke with Ferroxcube Bead #56-590-65/4B on ground end of coil
L2 – 1 Turn #22 AWG, 1/8" ID
L3 – 0.15 μH Molded Choke
L4 – Ferroxcube VK-200-19/4B
Q1 – 2N6439
R1 – 10 Ω 2 Watt
T1, T2 – 25 Ω Subminiature Coax (Type UT25) 2.25 inches (57.15 mm) long

Z1 – Microstrip Line
800 mils L X 225 mils W
20.32 mm L X 5.715 mm W
Z2 – Microstrip Line
200 mils L X 225 mils W
5.08 mm L X 5.715 mm W
Z3, Z4 – Microstrip Line
550 mils L X 125 mils W
13.97 mm L X 3.175 mm W
Board – 0.031" (0.787 mm) Glass Teflon
$\epsilon_r = 2.56$

FIGURE 3 – 2N6439 60 Watt Building Block 225–400 MHz

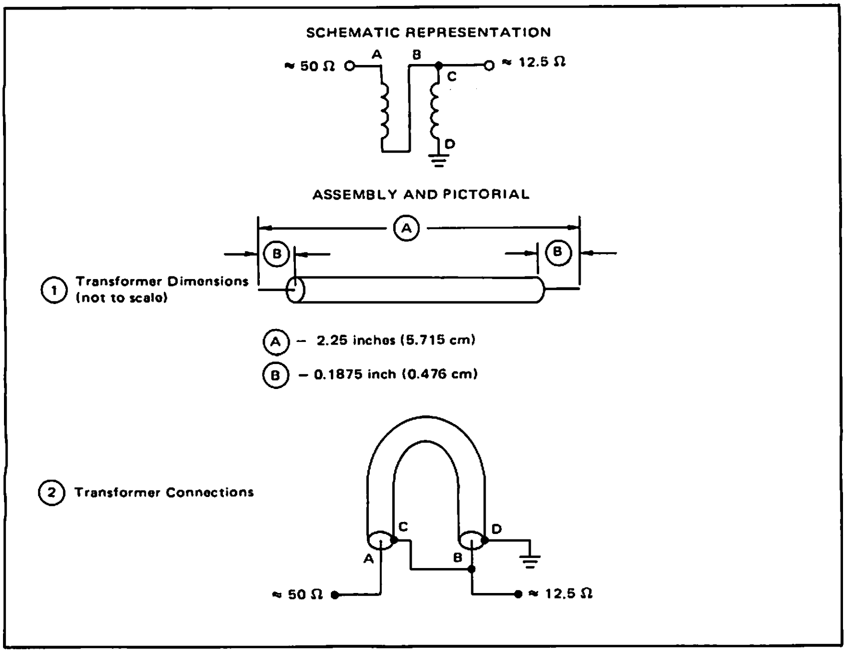


FIGURE 4 – Construction Details of the 4:1 Unbalanced to Unbalanced Transformers

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AMPLIFIER PERFORMANCE

FIGURE 5 — Power Gain versus Frequency
Efficiency versus Frequency

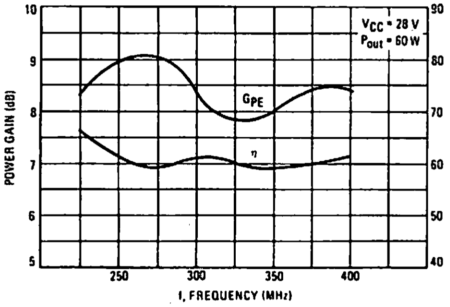


FIGURE 6 — Output Power versus Input Power

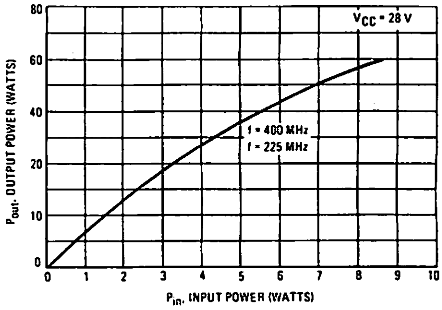
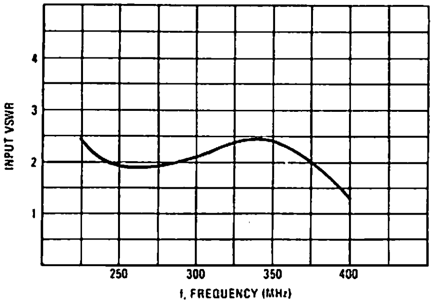


FIGURE 7 — Input VSWR versus Frequency



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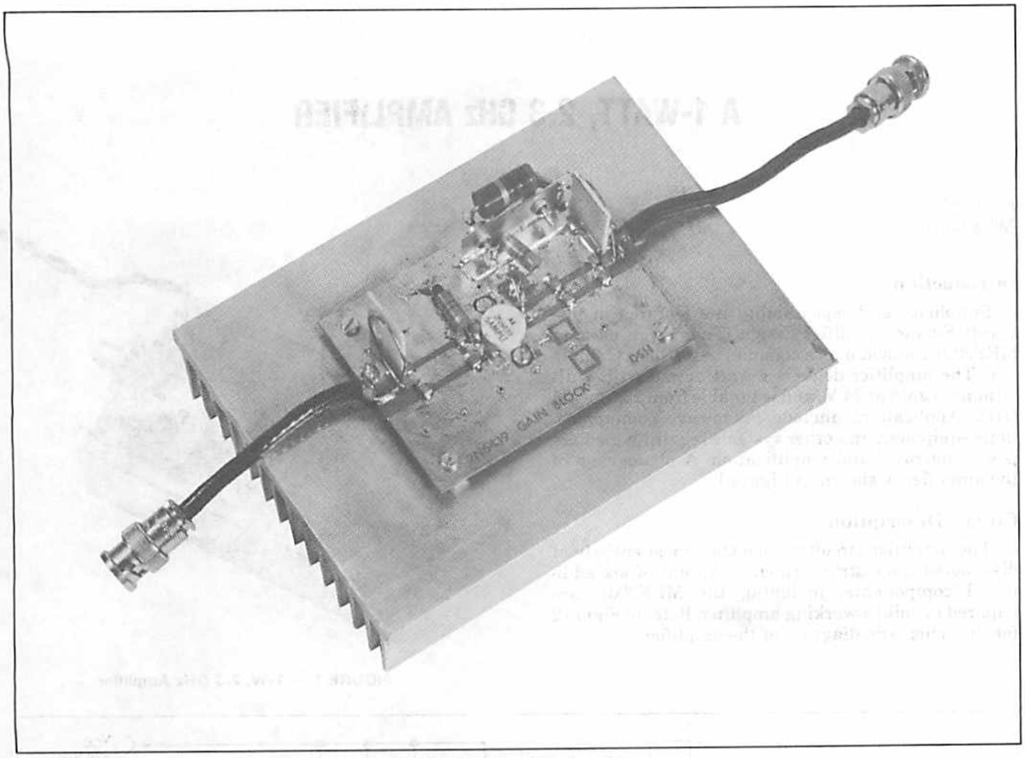


FIGURE 8 – Amplifier Assembly

Bibliography

1. "Mounting Stripline – Opposed Emitter (SOE) Transistors," Motorola Application Note AN-555, Motorola Semiconductor Products Inc., Phoenix, Arizona.

2. Glenn Young, "Microstrip Design Techniques for UHF Amplifiers," Motorola Application Note AN-548A, Motorola Semiconductor Products Inc., Phoenix, Arizona.

3. Roy Hejhall, "Systemizing RF Power Amplifier Design," Motorola Application Note AN-282A, Motorola Semiconductor Products Inc., Phoenix, Arizona.

NOTE: A 10 Watt 225–400 MHz Amplifier–MRF331 is described in Engineering Bulletin EB-74.

A 1-WATT, 2.3 GHz AMPLIFIER

Prepared by
Mike Miceli

Introduction

Simplicity and repeatability are featured in this 1-watt S-band amplifier design. The design uses an MRF2001 transistor as a common base, Class C amplifier. The amplifier delivers 1-watt output with 8 dB minimum gain at 24 V, and is tunable from 2.25 to 2.35 GHz. Applications include microwave communications equipment and other systems requiring medium power, narrow band amplification. A photograph of the amplifier is shown in Figure 1.

Circuit Description

The amplifier circuitry consists almost entirely of distributed microstrip elements. A total of six additional components, including the MRF2001, are required to build a working amplifier. Refer to Figure 2 for the schematic diagram of the amplifier.

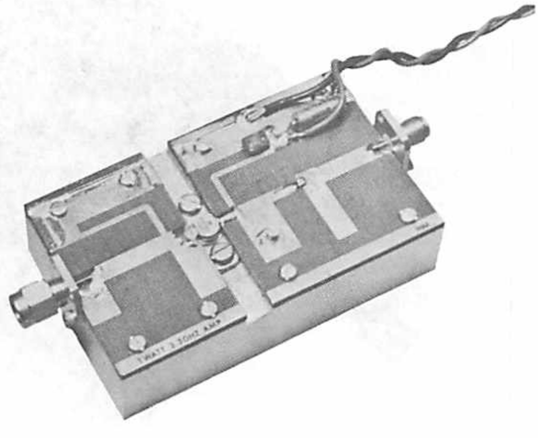
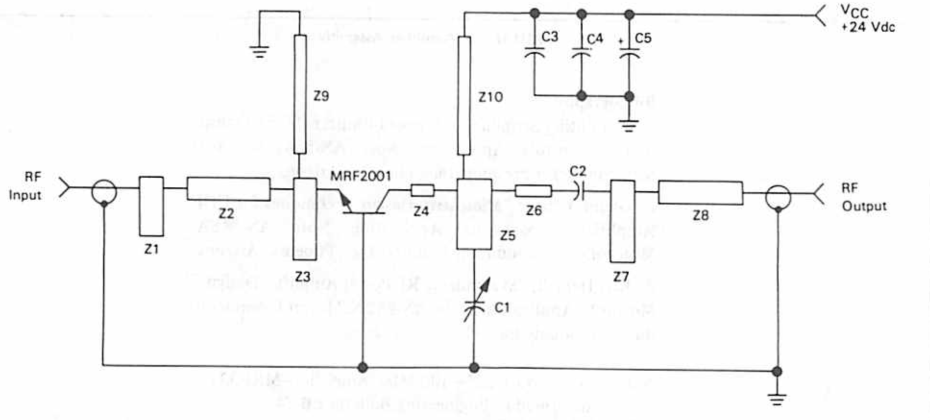


FIGURE 1 — 1-W, 2.3 GHz Amplifier

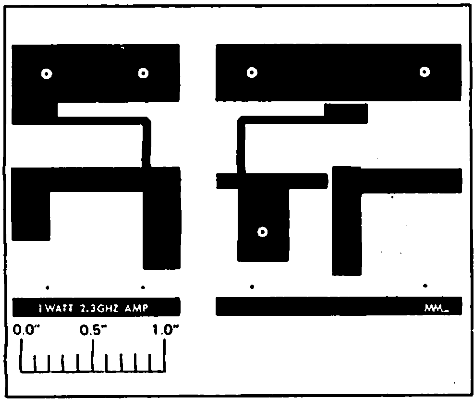


C1 — 0.4-2.5 pF Johanson 7285*
C2, C3 — 68 pF, 50 mil ATC**
C4 — 0.1 μF, 50 V
C5 — 4.7 μF, 50 V Tantalum
Z1-Z10 — Microstrip; see Photomaster, Figure 3

Board Material — 0.0625" 3M Glass Teflon,***
$\epsilon_r = 2.5 \pm 0.05$
*Johanson Manufacturing Corp., 400 Rockaway Valley Road, Boonton, NJ 07005
**American Technical Ceramics, One Norden Lane, Huntington Station, NY 11746
***Registered Trademark of Du Pont

FIGURE 2 — Schematic Diagram

The input and output impedances of the transistor are matched to 50 ohms by double section low pass networks. The networks are designed to provide about 3% 1 dB power bandwidth while maintaining a collector efficiency of approximately 30%. There is one tuning adjustment in the amplifier — C1 in the output network. Ceramic chip capacitors, C2 and C3, are used for DC blocking and power supply decoupling. Additional low frequency decoupling is provided by capacitors C4 and C5. Refer to Figure 3 for a 1:1 photomaster of the circuit boards.



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 3 — Circuit Photomaster

Amplifier Assembly

The circuit boards are mounted on a 3.125" × 1.875" × 0.750" aluminum block. A 0.062" deep and 0.260" wide slot is milled in the heat sink as shown in Figure 4.

The transistor mounts in the slot with two 4-40 screws. An alternate approach that would eliminate the need for milling is the laminated structure shown in Figure 5.

Using the laminated assembly, the transistor is mounted on the surface of the block and 0.062" aluminum shim stock is sandwiched between the block and the circuit boards. Connector mounting plates are required if SMA type connectors are used for the RF input and output. The SMA connectors can be fastened directly to the block if the milled approach is used. Either method results in the same performance for this 1-watt design. The laminated structure, however, may not be suitable for higher power designs. With higher power levels the transistor impedances are lower. The RF ground impedance through the laminated metal may be sufficiently high to impair gain and stability. This point emphasizes the fact that the successful design of RF amplifiers is dependent not only on attention to electrical considerations, but to the physical construction as well. While construction related parasitics cannot be totally ignored at medium frequencies, they can pose serious problems at microwave frequencies. It is recommended that the following construction techniques be followed when building this amplifier. Refer to Figure 6 for the component placement diagram.

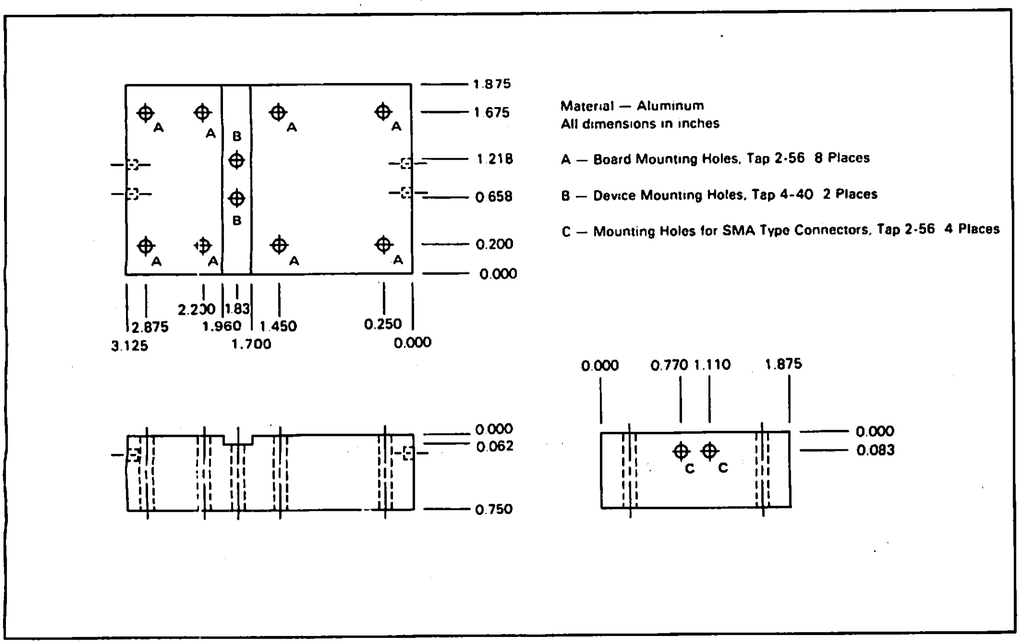


FIGURE 4 — Amplifier Heat Sink

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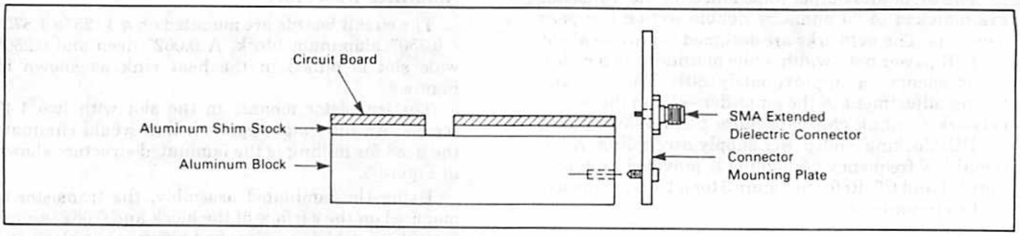

FIGURE 5 — Laminated Assembly

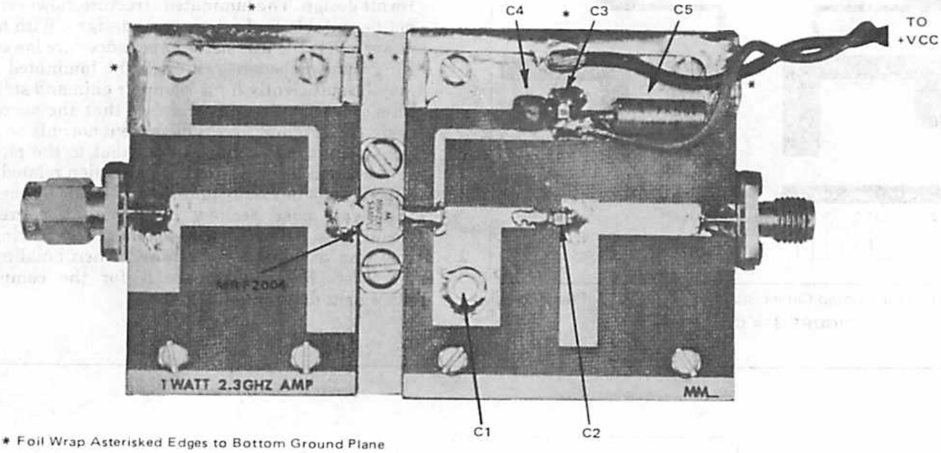

FIGURE 6 — Assembly Diagram

Construction Notes

1. The transistor is fastened to the heat sink with two 4-40 screws. The mounting surface should be flat and clean. Thermal compound should not be used on the underside of this device; the flange provides the transistor base connection and must make good electrical contact with the heat sink. The wide lead is the emitter and the narrow lead is the collector.

2. The edges of the boards marked with an asterisk (see Figure 6) must be foil wrapped to the bottom ground plane to provide a low impedance RF ground connection for C3, C4, C5 and the emitter choke, Z9. This is accomplished by soldering a 1/4″-wide strip of 1- to 5-mil thick copper foil to the top ground plane and then wrapping it around the edge of the board. The other edge of the foil is soldered to the bottom ground plane.

3. Use a #31 drill bit to drill the board mounting holes. With the transistor already mounted to the heat sink, slide the boards into position so they butt up against the transistor. This will insure that the excess lead inductance of the transistor is kept to a minimum. The boards can now be fastened to the heat sink and the remaining components mounted.

4. Use a minimum of heat when soldering C2 and C3. Excess heat could cause the end metal of the chip capacitor to separate from the ceramic.

5. C1 is a miniature variable capacitor whose high self-resonant frequency makes it ideal for use at microwave frequencies. The package design makes it very convenient to use wherever a shunt capacitive element is desired and is used here to vary the capacitance of microstrip stub, Z5. The capacitor is mounted by drilling a 0.120″ diameter hole (#31 drill bit) at the point indicated in Figure 6. Using the circuit board as a template, mark the point on the heat sink directly below the mounting hole. Since the capacitor is slightly longer than the thickness of the board, a clearance hole is needed at this point. The bottom of the capacitor is soldered to the ground plane on the bottom of the board. The flange of the capacitor is soldered to Z5. Avoid getting solder into the area above the flange as this will prevent the movement of the tuning piston.

Performance Data

Amplifier tune-up is accomplished by adjusting C1 for maximum output power with minimum collector current. The amplifier will tune from 2.25 to 2.35 GHz while maintaining an input VSWR of less than 2:1. Typical performance curves appear in Figure 7. Figures 7a and 7b show performance with the amplifier re-tuned for each frequency. Figure 7c shows performance without re-tuning. Note from Figure 7c that the instantaneous 1 dB bandwidth is approximately 70 MHz with the amplifier tuned to a center frequency of 2.3 GHz.

FIGURE 7 — Performance Curves

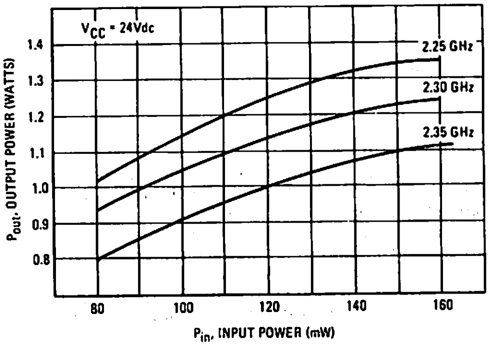

FIGURE 7a — Output Power versus Input Power

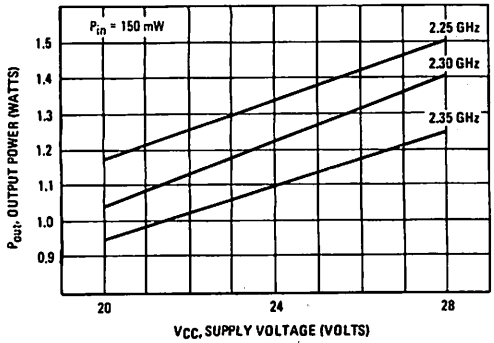

FIGURE 7b — Output Power versus Supply Voltage

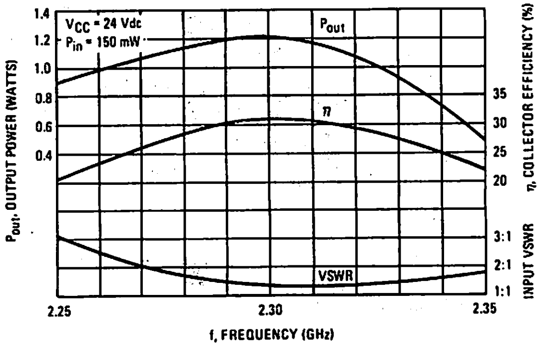

FIGURE 7c — Output Power, Efficiency and VSWR versus Frequency

NOTE: The MRF2001 is one of a family of 2 GHz power transistors with RF output powers as indicated below:

MRF2001	1 W	MRF2005	5 W
MRF2003	3 W	MRF2010	10 W

LOW-COST VHF AMPLIFIER HAS BROADBAND PERFORMANCE

Prepared by
Ken Dufour

Introduction

This bulletin presents two VHF amplifier designs intended for FM or CW service in the 136-174 MHz band. Both amplifiers feature the Motorola MRF260 and MRF262 plastic encased VHF transitors which are rated at 5.0 W and 15 W power output respectively. This new series is derived from a line of highly successful device types of similar capability, but packaged in a standard configuration, (i.e., stripline packages). The MRF260 and MRF262 are in a standard TO-220 silicone epoxy case with the emitter wired to the metal tab and center lead of the device. This common emitter configuration results in good RF performance, improved thermal conductivity, and ease of mounting in an RF amplifier, by connecting the transistor mounting flange to RF and DC ground.

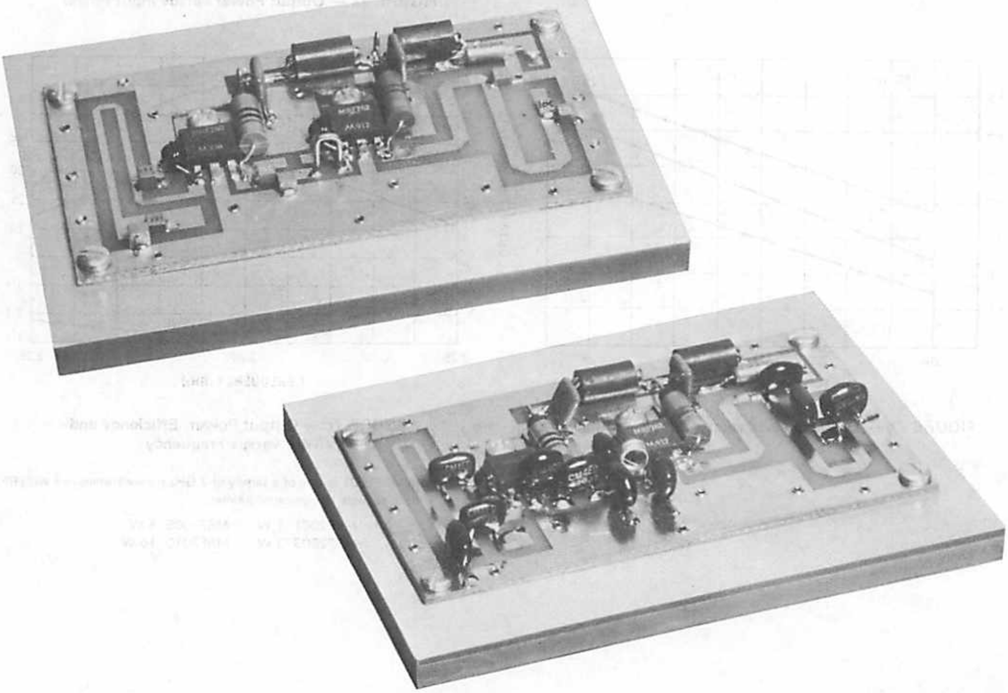

FIGURE 1 — Engineering Models. A Common Board Layout is Used for Both Versions

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1. Hatchett, John: 25 Watt and 10 Watt VHF Marine Band Transmitters, AN-595, Motorola Semiconductor Products, Inc.
2. Granberg, H: A Simplified Approach to VHF Power Amplifier Design, AN-791, Motorola Semiconductor Products, Inc.
3. Hollander, D: A 15 Watt AM Aircraft Transmitter Power Amplifier Using Low Cost Plastic Transistors, AN-793, Motorola Semiconductor Products, Inc.

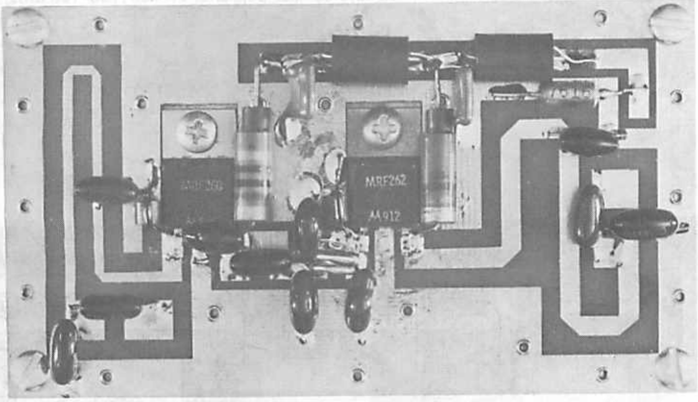


FIGURE 2 — 136-160 MHz Amplifier

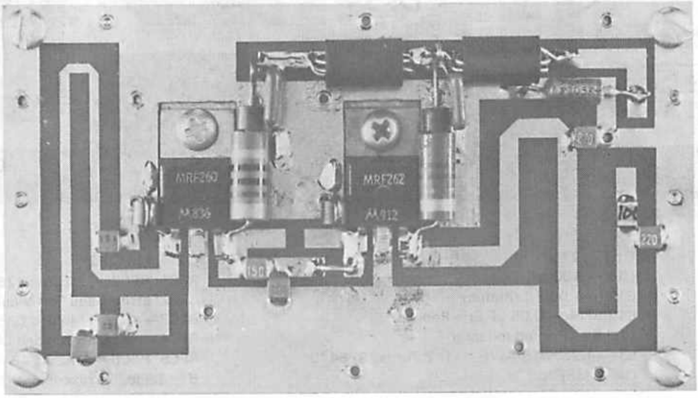


FIGURE 3 — 160-174 MHz Amplifier

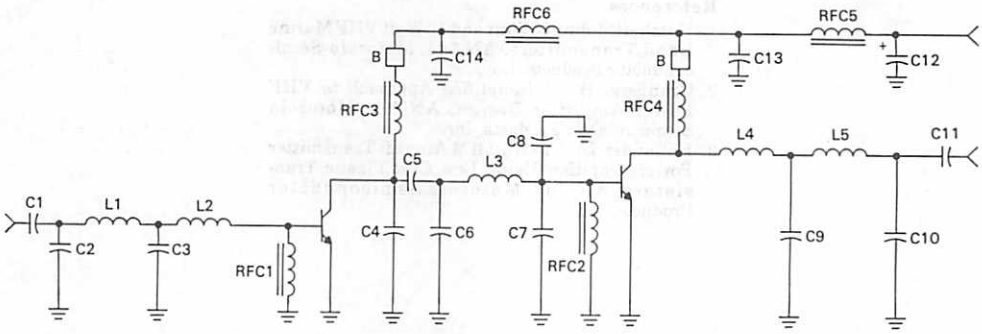
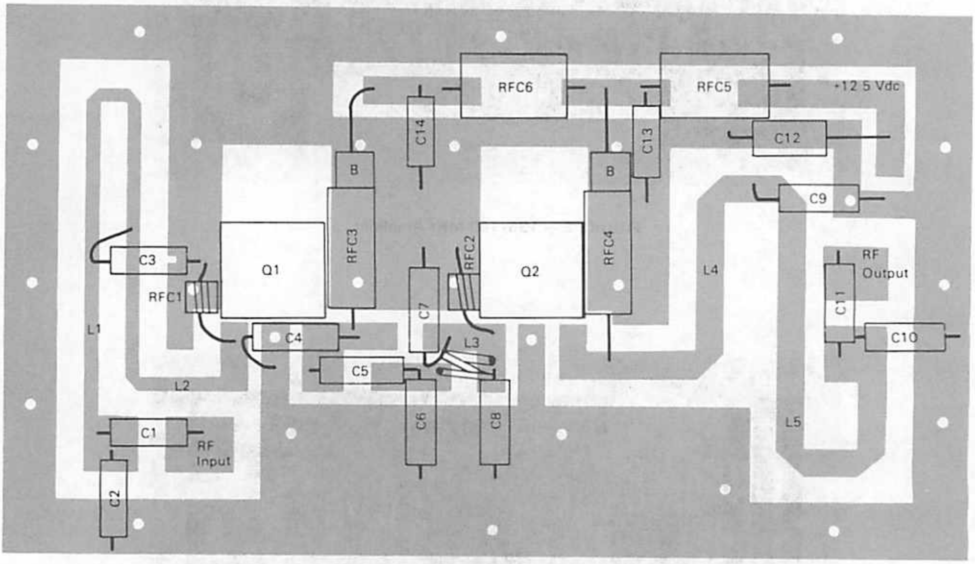


FIGURE 4 — Schematic Diagram of Dipped Silvered Mica Capacitor Version (136-160 MHz)



C1 — 200 pF
C2 — 33 pF
C3 — 47 pF
C4 — 18 pF
C5, C8 — 43 pF
C6 — 12 pF
C7, C9 — 50 pF
C10 — 22 pF
C11 — 100 pF
C12 — 1.0 μF Tantalum
C13, C14 — 0.05 μF Erie Redcap
L1-L5 — Printed Inductor
L3 — 1.25″ #18 AWG, 1-1/2 Turns, 9/64 ID
Q1 — MRF260
Q2 — MRF262
RFC1, RFC2 — 2 Turns #26 Enameled on Ferrite Bead Ferroxcube 56-590-65/3B
RFC3 — 10 μH Molded Choke
RFC4 — 0.15 μH Molded Choke
RFC5, RFC6 — VK200-4B
B — Bead, Ferroxcube 56-590-65/3B

FIGURE 5 — Component Placement, 136-160 MHz Amplifier

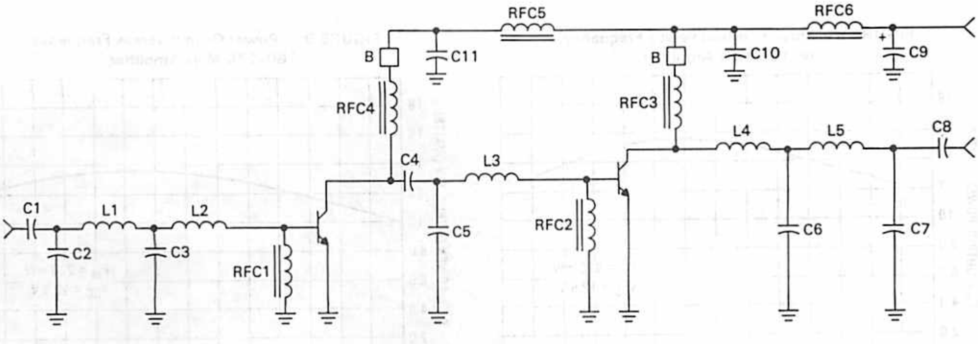
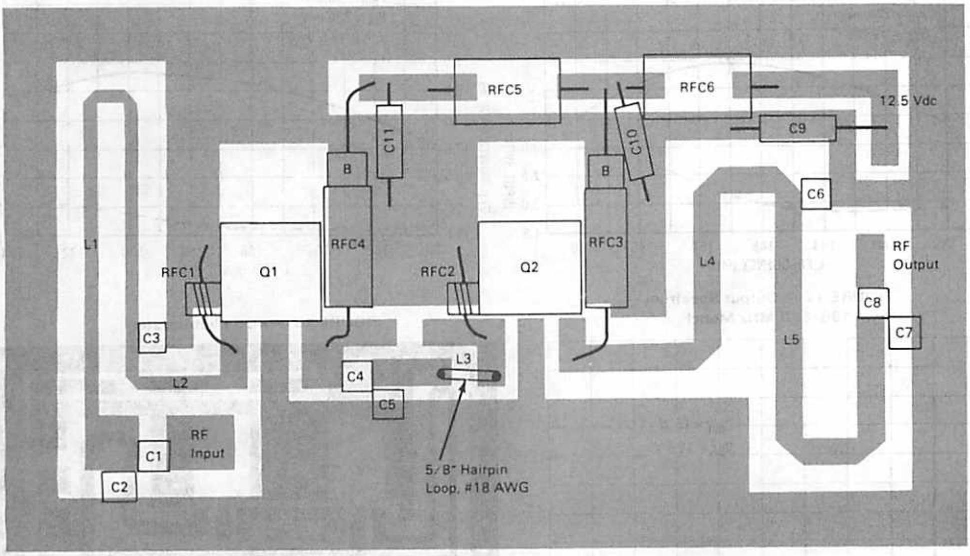


FIGURE 6 — Schematic Diagram of Chip Capacitor Version (160-174 MHz)



C1 — 220 pF, TDK 100 mil Chip Capacitor
C2 — 43 pF, TDK 100 mil Chip Capacitor
C3 — 150 pF, TDK 100 mil Chip Capacitor
C4 — 15 pF, TDK 100 mil Chip Capacitor
C5 — 63 pF, TDK 100 mil Chip Capacitor
C6 — 27 pF, TDK 100 mil Chip Capacitor
C7 — 22 pF, TDK 100 mil Chip Capacitor
C8 — 100 pF, TDK 100 mil Chip Capacitor
C9 — 1.0 μF Tantalum
C10 — 0.1 μF Erie Redcap, 100 V General Purpose
C11 — 0.05 μF Erie Redcap, 100 V General Purpose

L1-L5 — Printed Inductor
L3 — 5/8" #18 AWG Wire formed into hairpin loop
Q1 — MRF260
Q2 — MRF262
RFC1, RFC2 — 2 Turns #26 Enameled Wire through Ferrite Bead Ferroxcube 56-590-65/3B
RFC3 — 0.15 μH Molded Choke
RFC4 — 10 μH Molded Choke
RFC5, RFC6 — VK200-4B
B — Bead, Ferroxcube 56-590-65/3B

FIGURE 7 — Component Placement, 160-174 MHz Amplifier

FIGURE 8 — Power Output versus Frequency, 136-160 MHz Amplifier

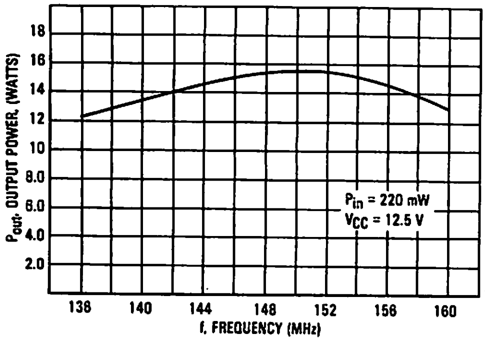


FIGURE 9 — Power Output versus Frequency, 160-174 MHz Amplifier

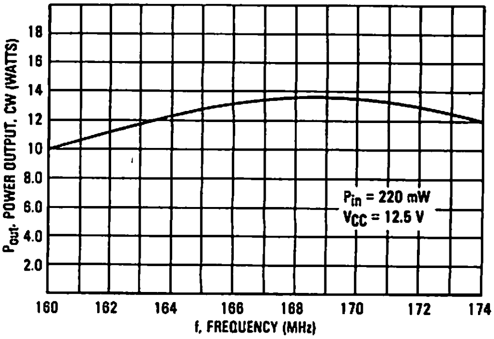


FIGURE 10 — Power Gain and Input VSWR versus Frequency, 136-160 MHz Amplifier

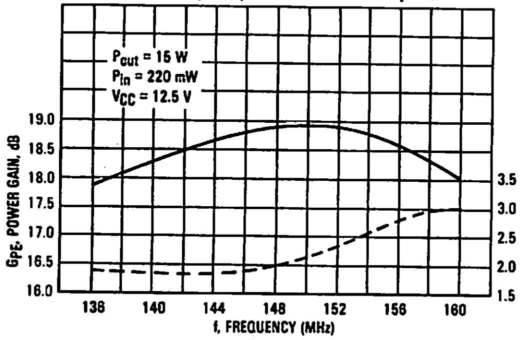


FIGURE 11 — Power Gain and Input VSWR, versus Frequency, 160-174 MHz Amplifier

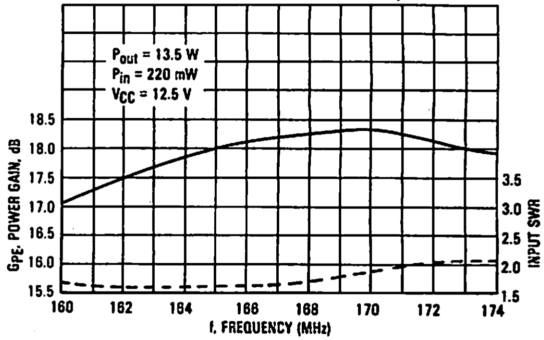


FIGURE 12 — Output Spectrum 136-160 MHz Model

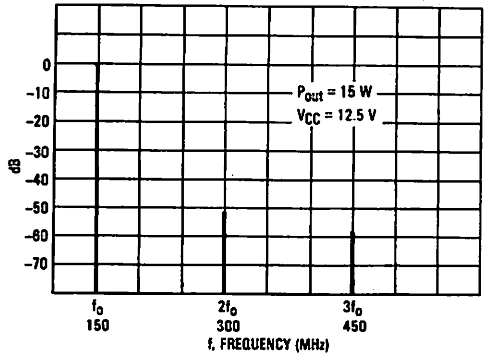
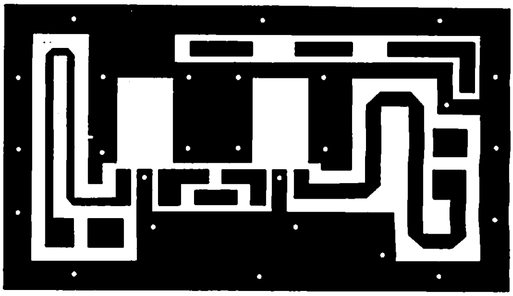


FIGURE 13 — PCB Photomaster



Note: Grounding eyelet locations are indicated by dots.

The Printed Circuit Board shown is 75% of the original.

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Design Considerations

The lower frequencies (136-160 MHz) are serviced by a design utilizing low-cost dipped silver mica capacitors. For a broadband response in the higher frequencies; (160-174 MHz), low inductance, ceramic chip capacitors are used.

Ease of assembly, repeatability and fast economical construction received the utmost consideration in the design of this amplifier. TO-220 devices result in a low profile circuit which minimizes the volume occupied by the amplifier. Additionally, the MRF262 transistor used in the output stage is a rugged device, able to tolerate high load SWR conditions. Maximum use of printed inductors assures good repeatability.

Both amplifiers utilize stagger tuned networks to enhance bandwidth. Additionally, each design retains excellent gain and stability characteristics when narrow banded. All of these merits are attributed to optimum device gain and the reasonably high inter-stage impedance levels incurred at these power levels.

Circuit Description

The amplifier has two stages and uses 5.0 W and 15 W rated transistors to accomplish the desired gain and power output. Two stage transmission line Chebyshev networks accomplish coupling and impedance transformation at the input and output. Nominal impedance levels are 50 ohms, while the interstage network transforms device impedances directly. Values for the reactive elements of these networks were almost entirely generated by computer aided design. Although the interstage network is straight forward in design, it required some modification and refinement of computer generated values to achieve the final results and accomodate available component values.

Construction

The amplifier is assembled on double-sided G-10 fiberglass board with 1 oz. copper cladding. The format is 2.0" × 3.5" and a photomask is provided (Figure 13). Some method of electrically connecting the upper and lower ground plane is required. Eyelets or plated through holes are recommended, but *alternative* measures such as short pieces of wire soldered to both planes can be used successfully. Failure to provide an adequate or consistent ground plane may result in poor RF performance, instability, and unpredictable tuning. The reverse side of the board retains all copper and forms the ground plane. Component placement and the recommended position of grounding eyelets is shown in Figures 13, 5, and 7. All component leads are positioned and soldered above the board. There are no through connections other than grounding points. This facilitates component positioning, replacement, and accessability. The transistors are fitted into a 0.4" by 0.65" opening in the board and are installed *directly against* the heat sink. A coating of heat sink compound such as Dow Corning 340 between each device and the heat sink improves thermal contact and helps prevent power slump.

At frequencies beyond 100 MHz, dipped silver mica capacitors generally become inductive, and do so with a high degree of unpredictability. This phenomenon is also dependent upon component value and becomes more pronounced with an increase in frequency. (Ref: 1, 2, 3). To maintain predictable performance beyond 160 MHz, a second layout featuring ceramic chip capacitors is offered (Figure 3, 6, 7). The design of these capacitors allows them to remain capacitive beyond the VHF frequencies. Maintaining the bandwidth of 160-174 MHz with this circuit board, the networks become lossy and power output suffers slightly. Variable capacitors may make this condition more tolerable and can be installed in the input and interstage networks. In some cases the ease of adjustment and added flexibility would justify the added cost of the variable capacitors.

Performance

Normally, this amplifier will not require tuning provided that components are as described and are positioned as shown on Figure 5 and 7. If an accurate method of measuring power is available, a quick check of amplifier performance can be accomplished by comparing its parameters with the performance data of Figures 8 through 11. Drive must be maintained at 220 mW (±20 mW) and V_{CC} held to 12.5 Vdc to accurately reproduce the overall response noted here. Allow some degree of tolerance (10%) in output power to account for differences inherent in component values and transistor performance. To assure broadband performance and tailored frequency response, the amplifier should be checked using a swept frequency generator capable of 200-300 mW output. Tuning for maximum power out and minimum reflected power at band centers will not necessarily provide a broadband response. Figures 8 through 11 graphically depict typical levels of performance achieved with this amplifier. Either version is stable into higher than 3:1 VSWR load mismatch at all phase angles. The output device is tolerant of short term operation into an open or short circuit load at full drive.

Harmonic content of a 150 MHz signal at the output of the dipped silver mica version is illustrated in Figure 12. The 2nd harmonic is approximately -50 dB with respect to the fundamental. This level of performance cannot be maintained across the entire band, therefore, some additional filtering of the output signal will be required to meet more stringent requirements.

With the amplifier mounted on aluminum stock, 2.0" × 8.5" and 0.090" thick, a 25% duty cycle (1 min on, 4 min off) produced a temperature of 50°C (122°F) after two hours of operation. A 50% duty cycle (1 min on, 1 min off) raised this temperature to 60°C (140°F) and full key down operation caused a stabilized temperature of 80°C (176°F). All temperatures were measured on the heat sink at the final device with output power maintained at 15 watts. One can safely assume that a panel on the outside edge (i.e., backside) of a transceiver could be successfully used as a heat sink for this amplifier.

60 WATT VHF AMPLIFIER USES SPLITTING/COMBINING TECHNIQUES

Prepared by
Ken Dufour
RF Product Group

Using proven combining techniques to obtain higher output power or added reliability at VHF can be accomplished with excellent results. Simple matching networks and power transistors featuring moderate gain capability can produce a level of performance comparable to that of a single-stage amplifier using a larger, more expensive device. Though not the ultimate answer in VHF amplifier design, the splitter/combiner method does have distinct advantages over designs that brute force the transistors into a parallel configuration. Current hogging and reduced impedance level problems associated with that technique are minimized. The exotic materials or expensive board layout required to produce a true push-pull design operating at VHF again makes combining techniques more appealing.

This 60 W amplifier operates from 150 to 175 MHz and features two, low-cost Motorola MRF264 transistors. These devices are designed for operation at VHF and individually produce 30 watts of rated output power and 6.0 dB of gain with a 12.5 volt supply. The amplifier design makes use of a modified Wilkinson combiner technique to produce 60 watts output with a drive level of 15 watts.

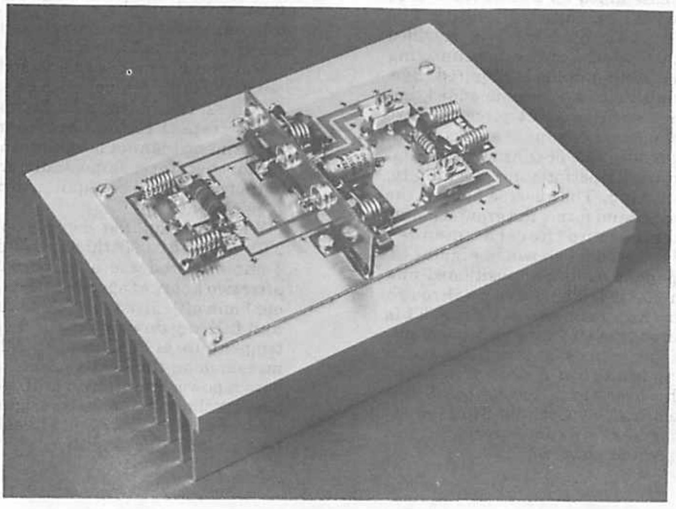


FIGURE 1 — Engineering Model

Design Considerations

Experimental work with 90° (quadrature) couplers proved unsuitable for this application. Generally, they are sensitive to mismatch and tend to create instability and loss of power when used in an amplifier. In-phase (Wilkinson) couplers provide an adequate solution to this problem. (Ref: 1) They are relatively insensitive to phase changes and offer good bandwidth characteristics.

Printed transmission lines for the frequency of interest can become somewhat cumbersome on standard circuit board material. Therefore, lumped reactances (L1, 2, 9, 10 and C1, 2, 3, 14, 15, 16, Figure 5) are used to simulate 70.7 ohm 1/4 wave transmission lines, the main element in the couplers. This approach not only conserves board space, but provides a means to compensate for small variations in associated component values.

Microstrip techniques are incorporated in the amplifier networks to balance RF performance and promote reproducibility. Because of the lower circulating currents and reduced component heating in the collector circuitry of low-powered stages, smaller capacitors can be used in the networks at that point than would be required for a single-ended 60 watt design. Separating the major heat producing devices to two areas on the heatsink produces a more even heat transfer to the ambient air. The combined amplifier presented here has good harmonic suppression (Figure 8). A low-pass filtering effect is noticeable with the Wilkinson combiners.

Construction and Alignment

A 1:1 photomask of the circuit is provided in Figure 9 and double-sided G-10 fiberglass board with two-ounce copper cladding is recommended for construction. The ground points are indicated on the PCB photomask.

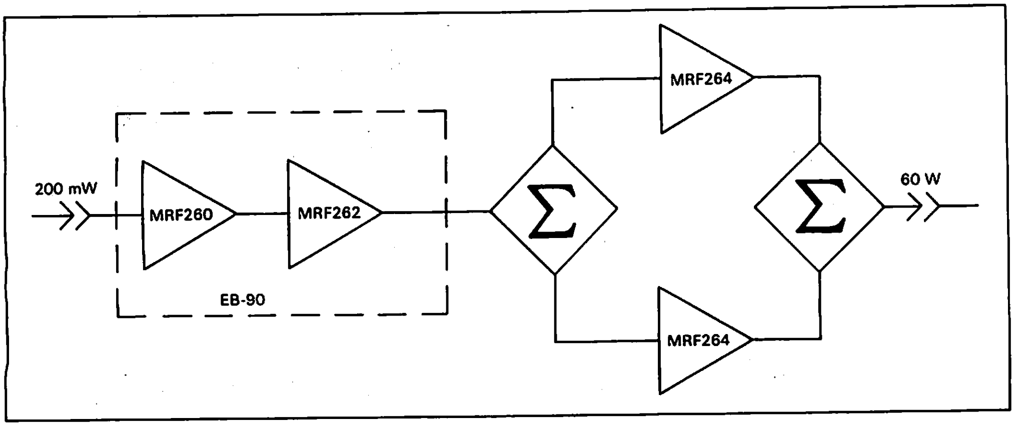
The inductors required for the splitter/combiner are constructed by winding the appropriate number of turns (closewound) on a temporary 1/8 inch form and then separating the individual turns by 0.020 inch. An Xacto number 11 knife blade was used for this purpose and provides the correct turns spacing. The 100-ohm isolation resistors, R1 and R2, must be noninductive and carbon composition resistors proved to be entirely adequate. In a properly tuned and balanced amplifier these resistors should remain fairly cool to the touch during normal operation. Each amplifier and coupler input and output port is designed to be terminated into 50-ohms to facilitate testing into a 50-ohm system.

A PCB bridge (Figures 3 and 9) is used to carry all of the dc feed circuitry. It acts as a continuation of the ground plane and enhances circuit stability. Solid copper (0.027 inch) and double-sided circuit board were used as a construction medium and no difference in performance was noted with either material.

Initial alignment is accomplished by driving the amplifier with a 5 watt CW source at approximately 160 MHz. The applied voltage is set at 12.5 volts and the variable capacitors, C4 and C5, are adjusted in an alternating manner to provide maximum output power. Full drive (15 watts) is then applied and the capacitor adjustments are repeated. At this point, the circuitry should be delivering 60 watts or more to the 50-ohm load with the 15 watts input. After the final adjustments are made, the isolation resistor temperature in either coupler should be relatively cool to the touch and the input VSWR should be at a minimum. Best results will be obtained if the transistors are beta matched (±10%) prior to installing them in the circuit.

Additional Comments

This amplifier has been extensively tested for ruggedness and reproducibility. The 15 watt input level makes it compatible with the EB-90 two-stage VHF amplifier as a driver. Together they form a chain requiring 200 mW of input power for a 60 watt or more output.



References

1. Lawrence R. Laveller; "Two Phased Transistors Shortchange Class C Amps," *Microwaves*, Pg. 48-54, February, 1978.
2. Ernest J. Wilkinson; "An N-Way Hybrid Power Divider," *PGM TT Transactions*, pg. 116-118, January, 1960.

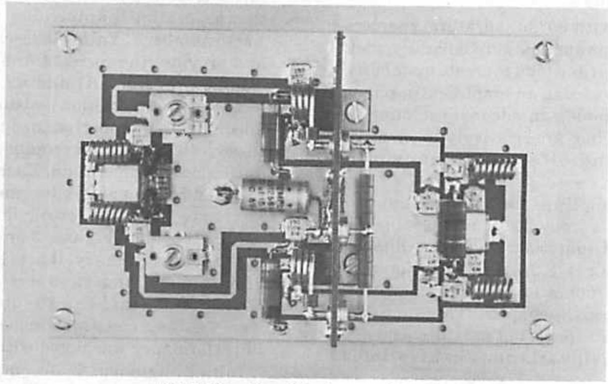


FIGURE 2 — Amplifier Layout - Top View

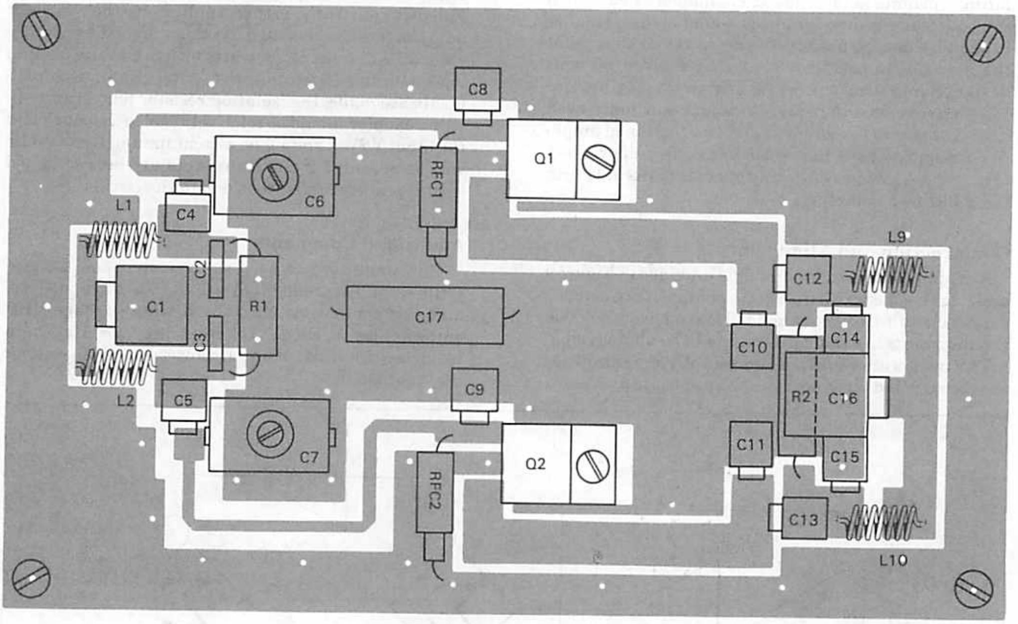
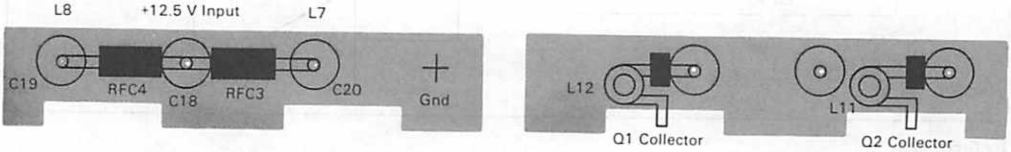


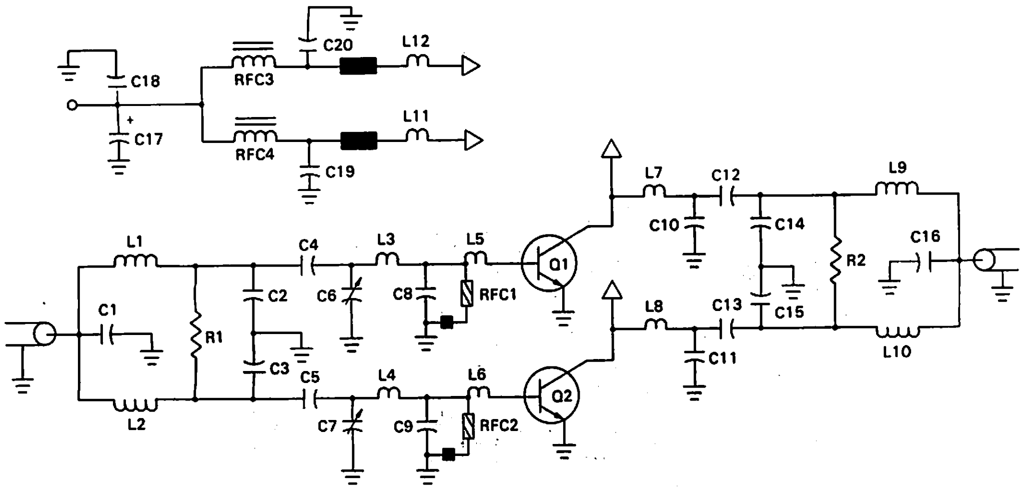
FIGURE 3 — Component Placement



a. Output Side

b. Base Side

FIGURE 4 — PCB Bridge Details



C1, C16 — 25 pF Unelco (J101)
C2, C3 — 15 pF CM04 Mica
C4, C5 — 68 pF Standex
C6, C7 — Arco 404 Variable
C8, C9 — 150 pF Standex
C10, C11 — 56 pF Standex
C12, C13 — 39 pF Standex
C14, C15 — 15 pF Standex
C17 — 100 μF @ 16 V Electrolytic
C18, C19, C20 — 680 pF Allen Bradley Feedthru

L1, L2 — 7 Turns #18, 0.125" ID
L3, L4, L5, L6 — Printed Inductors
L7, L8 — Printed Inductors
L9, L10 — 7 Turns #18 AWG, 0.125 ID
L11, L12 — 4 Turns #18 AWG, 0.250 ID w/Bead
Q1, Q2 — MRF264
RFC1, RFC2 — 0.15 μH Molded Choke w/Bead, Ferroxcube 56-590 65/3B
RFC3, RFC4 — 4 Ferrite Beads each on #18 AWG
R1 — 100 Ω 1/2 W Carbon
R2 — 100 Ω 2.0 W Carbon

FIGURE 5 — Schematic - 60 W Amplifier

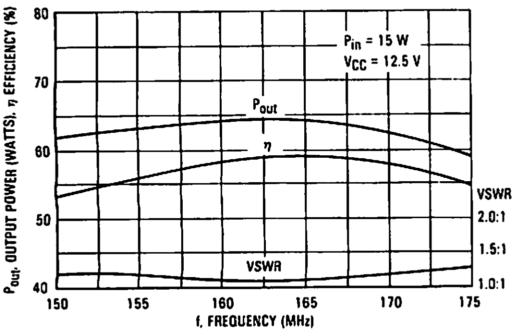


FIGURE 6 — Output Power, Efficiency, and Input VSWR versus Frequency

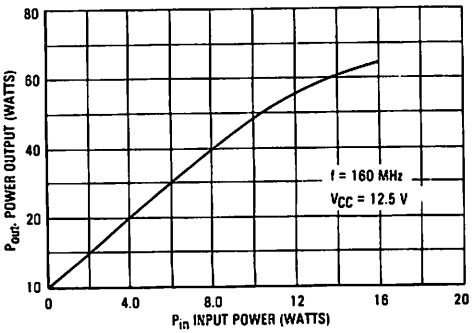
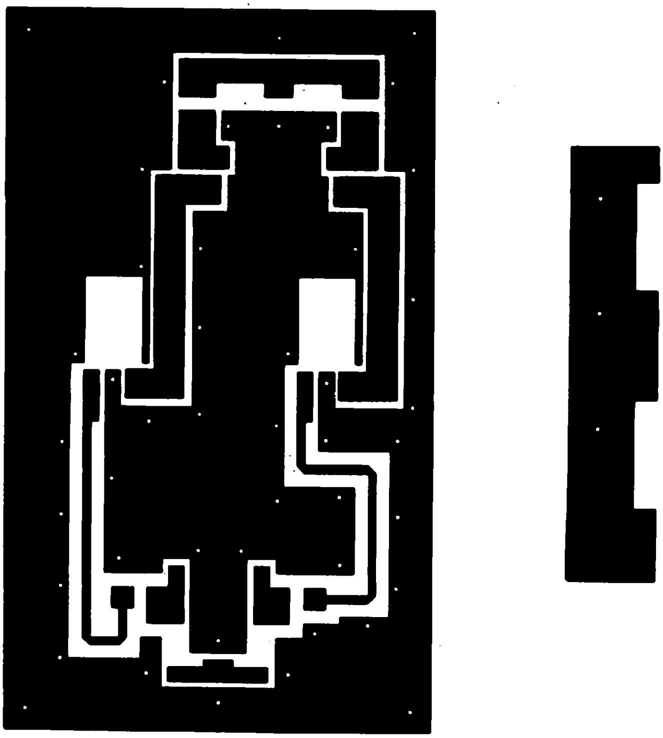


FIGURE 7 — Output Power versus Input Power



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 8 — PCB Photomaster

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GET 600 WATTS RF FROM FOUR POWER FETs

Prepared by
Helge Granberg
Circuits Engineer, SSB

This unique push-pull/parallel circuit produces a power output of four devices without the added loss and cost of power splitters and combiners. Motorola MRF150 RF power FET makes it possible to parallel two or more devices at relatively high power levels. This technique is considered impractical for bipolar transistors due to their low input impedance. In a common-source amplifier configuration, a power FET has approximately five to ten times higher input impedance than a comparable bipolar transistor in a common emitter circuit. The output impedance in both cases is determined by the dc supply voltage and power level. The limit to the number of FETs that can be paralleled is dictated by physical, rather than electrical restrictions, where the mutual inductance between the drains is the most critical aspect, limiting the upper frequency range of operation. The magnitude of these losses is relative to the impedance levels involved, and becomes more serious at lower supply voltages and higher power levels. Since the minimum mounting distance of the transistors is limited by the package size, the only real improvement would be a multiple die package. For higher frequency circuits, these mutual inductances could be used as a part of the matching network, but it would seriously limit the bandwidth of the amplifier. This technique is popular with many VHF bipolar designs.

In paralleling power FETs another important aspect must be considered: If the unity gain frequency (f_α) of the device is sufficiently high, an oscillator will be created, where the paralleling inductances together with the gate and drain capacitances will form resonant circuits. The feedback is obtained through the drain to gate capacitance (C_{rss}), which will result in 360° phase shift usually somewhere higher than the amplifier bandwidth. Thus, the oscillations may not be directly noticed in the amplifier output, but may have high amplitudes at the drains. This can be cured by isolating the paralleling inductance, which consists of the dc blocking capacitors (C7-C10, Figure 2) and their wiring inductance from the gates. Low value non-inductive resistors which do not appreciably affect the system gain can be used for this purpose.

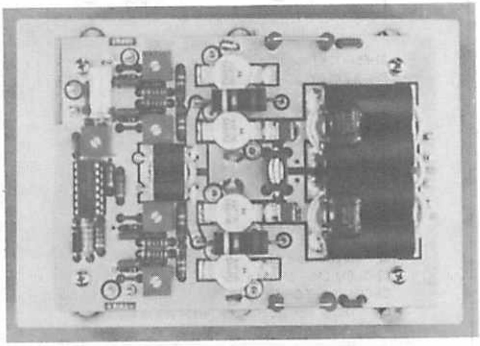

FIGURE 1 — Photograph of the 600 Watt 2.0-30 MHz MOSFET Linear Amplifier

CIRCUIT DESCRIPTION

Figure 2 shows a detailed schematic of the 600 W RF FET amplifier. It can be operated from supply voltages of 40 to 50 depending on linearity requirements. The bias for each device is independently adjustable, therefore no matching is required for the gate threshold voltages. Since the power gain of a MOSFET is largely dependent on the drain bias current, only g_m matching is required, and it can be only ± 10%.

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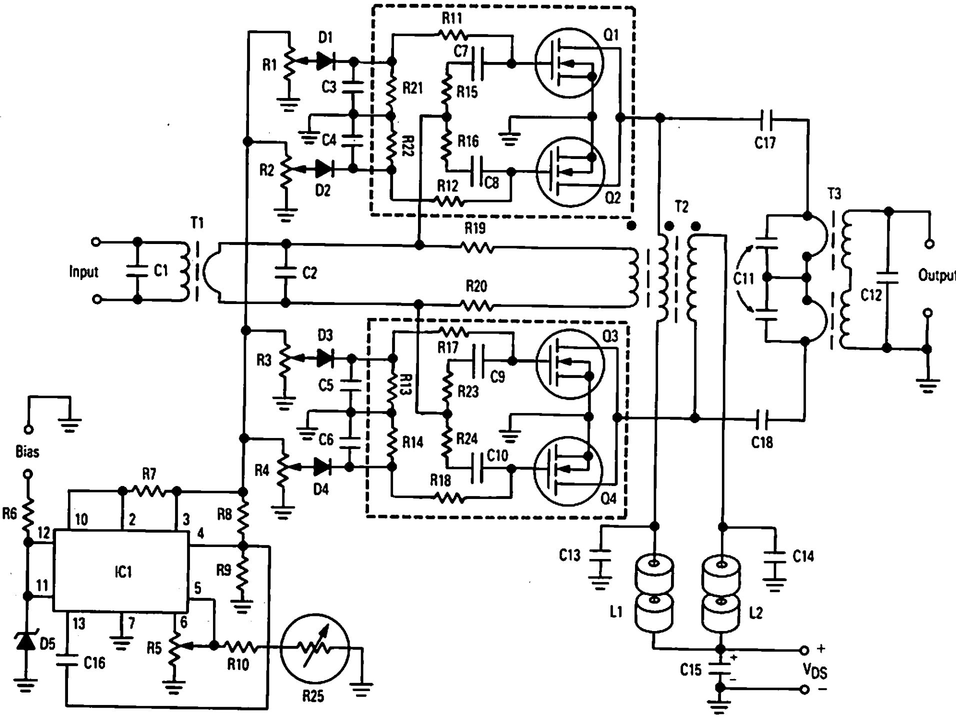
FIGURE 2 — Detailed Schematic

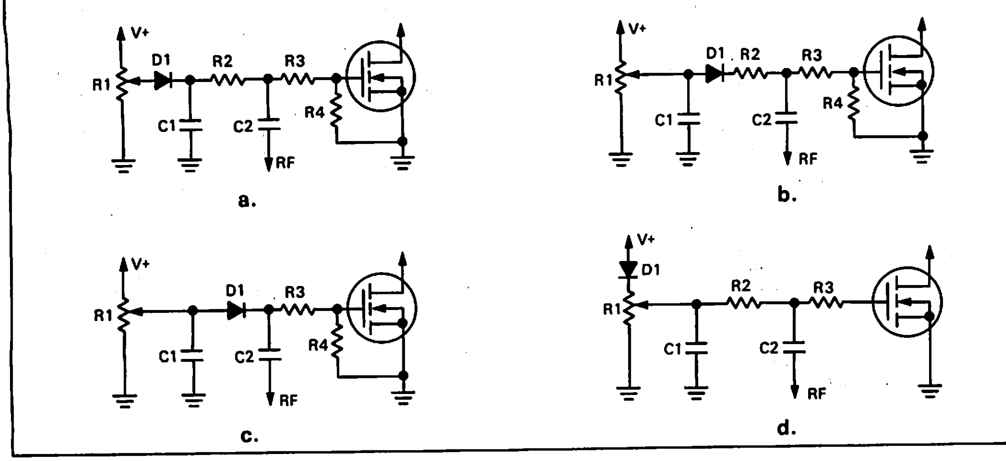


R1-R5 — 10 k Trimpot
R6 — 1.0 k/1.0 W
R7 — 10 Ohms
R8 — 2.0 k
R9, R21-R24 — 10 k
R10 — 8.2 k
R11-R14 — 100 Ohms
R15–R18 — 2.7 Ohms
R19–R20 — 10 Ohms/2.0 W Carbon
R25 — Thermistor, 10 k (25°C), 2.5 k (75°C)
C1 — Not used
C2 — 820 pF Ceramic chip
C3-C6, C13, C14 — 0.1 μF Ceramic
C7–C10 — 0.1 μF Ceramic chip
C11 — 1200 pF each, 680 pF mica in parallel with an Arco 469 variable or three or more smaller value mica capacitors in parallel
C12 — Not used
C15 — 10 μF, 100 V Electrolytic
C16 — 1000 pF Ceramic
C17, C18 — Two 0.1 μF, 100 V Ceramic each, (ATC 200 823 or equivalent)
D1–D4 — 1N4148
D5 — 28 V Zener, 1N5362 or equivalent
B1-B4 — Ferrite Beads
L1, L2 — Two Fair-Rite 2673021801 ferrite beads each or equivalent, 4.0 μH
T1-T3 — See text
Q1-Q4 — MRF150
IC1 — MC1723CP
All resistors 1/2 W carbon or metal film unless otherwise designated.

*Note: parts & kits for this amplifier are available from Communications Concepts, 121 Brown St., Dayton, Ohio 45402 (513) 220-9677

The circuit board was designed to allow several different gate biasing configurations (Figure 3). In circuit "a", which is used in the amplifier described here, D1 serves a purpose of preventing positive voltage from getting fed back to the bias source in case of a drain-gate short in a FET. This protects the other three devices from gate overvoltage. C1-R2 combination establishes an RF shunt from the gate to ground, which is necessary for stabilization. R4 could also be used for this purpose, but it would have to be a relatively low value, resulting in unnecessary high current drain from the bias supply. Normally R4 is only a dc return to ground, which is required with D1 preventing an open circuit in one direction. R3 is a low value resistor to prevent parasitic oscillations in a parallel FET circuit, as discussed earlier. Variations "b" and "c" are basically the same, except for R2, which can be used to control the amount of RF rectified by D1. In addition to blocking the dc in one direction, D1 can be used for proportional biasing, in which the bias voltage increases with RF drive. This allows the initial idle current to be set to a lower than normal value, increasing the system efficiency.

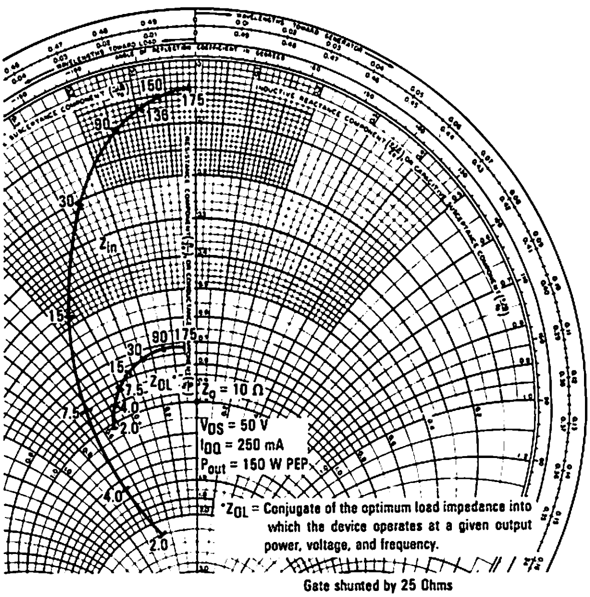
FIGURE 3 — Various Bias Configurations



The gate de-Qing in these circuits is done with R4. Circuit "d" is another variation, where D1 is moved in series with R1 eliminating R4. The value of R1 must be high to prevent destruction from a drain-gate short. The common bias is derived from IC1 (MC1723CP) which provides both line and load regulation. The line voltage regulation is defeated when the voltage to Pin 12 falls below 24 V, and the bias input can be used for Automatic Level Control (ALC) shut-down or linear ALC function. The regulator output voltage is adjustable from 0.5 to 9.0 volts with R5, which can be permanently set to 7.0-8.0 V. This voltage is also controlled by the combination of R10 and R25. R25 is a thermistor, and is tied to the heat sink for bias temperature compensation.

In Figure 2, the input from T1 is fed to the gates through C7-C10 and R15-R18. The input matching is initially done at the high end of the band (30 MHz). In contrast to a bipolar push-pull circuit, where the base-to-base impedance varies with class of operation, the gate-to-gate impedance of a common source FET circuit is always twice that from gate to ground. In this case, where two FETs are in parallel on each side, the gate-to-gate impedance equals the gate-to-ground impedance of one device. From the Smith chart information (Figure 4) this can be established as 3.45 ohms.

FIGURE 4 — Series Equivalent Impedance



The effect of R11-R14 and R21-R24 is minimal and can be disregarded. Considering the standard integers for T1 impedance ratio, 9:1 with its 5.55 ohms secondary appears to be the closest. This would set the values of R15-R18 at 2.0 ohms each, which would result in 3.5 dB gain loss, and about 1.0 W would be dissipated in each resistor. For this reason it was decided to reduce their values to 1.0 ohm, and trim the values of C1 and C2 for lowest input VSWR. As a trade-off, the VSWR will peak slightly at 15-20 MHz, but still remain below 2:1.

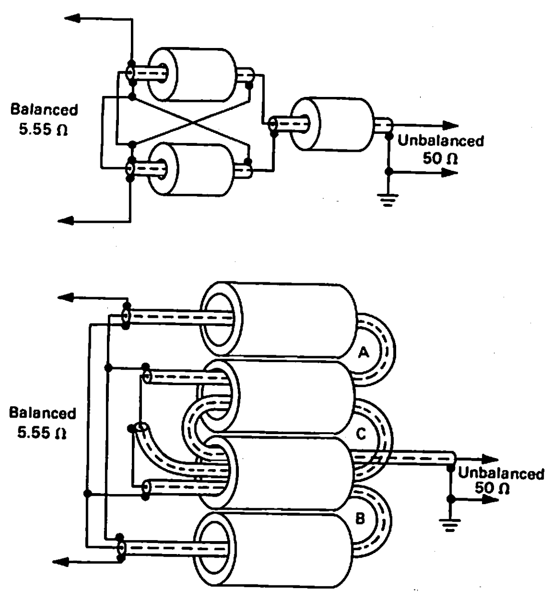
Negative feedback is derived from a winding in T2 through R19 and R20. Its purpose is to equalize the load impedance for T1 and reduce the amplifier gain at low frequencies. Since the gate to source capacitance of a MOSFET is fairly constant with frequency, the amount of feedback voltage is inversely proportional to its reactance. This function should be more or less linear, unless the inductive reactance of T1 is too low, or if resonances occur somewhere in the circuit. No computer analysis (as in Reference 2) was performed on the negative feedback system. Instead a simple approach described in Reference 1 was taken, where the gain difference between 2.0 and 30 MHz determines the feedback voltage required to equalize the voltages of the secondary of T1 at these frequencies. With an input impedance of 45 ohms at 2.0 MHz, and the feedback source delivering 15 $V_{(RMS)}$, (P_{out} = 600 W) the values of R19 and R20 will be around 10 ohms each.

A ferrite toroid or a two hole balun type core can be used for T2. Relatively low μi material with high curie temperature is recommended, since the minimum inductance requirement for the dc feed winding is less than 2.0 μH. Depending on the material, T2 can reach temperatures of 200-250°C, which the wire insulation must also be able to withstand. Several different output transformer configurations (T3) were tried, including a transmission line type in Figure 5. Although difficult to make, it has the advantage that low μi, low loss ferrite can be used with multiple turn windings. At this power level, heat in the output transformer was a major problem. High permeability materials, required in the metal tube and ferrite sleeve transformers could not be used because of their higher losses and low curie temperature. On the other hand, low μi cores with larger cross sectional areas were not readily available. To reach the minimum inductance required for 2.0 MHz, two of these transformers, with low permeability ferrite cores were connected in series. Both have 9:1 impedance ratios. Alternatively the secondaries can be connected in parallel with twice the number of turns (6) in each. C11 must withstand high RF currents, and must be soldered directly across the transformer primary connections. Regular mica or ceramic capacitors cannot be used, unless several smaller values are paralleled.

PERFORMANCE

Due to the mechanical proximity of the four MOS FET devices, the RF ground of the circuit board is poor, and results in 1.0-1.5 dB gain loss at 30 MHz, which can be seen in Figure 6. The ground plane can be improved by connecting all source leads together with a metal strap over the transistor caps. Another method is to place solder lugs under each transistor mounting screw, and solder each one to the nearest source lead. In this case, the heat sink will serve as the RF ground. Although the 3rd order IM distortion is not exceptionally good, (Figures 6, 7) the worst case 5th order

FIGURE 5 — Number of Turns Shown is not Actual



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products are better than -30 dB at all frequencies, and as can be expected with FETs, the 9th and higher order products are in the -50 to -60 dB level. It can also be noticed from Figure 6, that the IMD does not increase at reduced power levels, as common with bipolar amplifiers. The even order output harmonic content depends greatly on the device balance as in any push-pull circuit. The worst case is at the low frequencies, where numbers like *-30 to -40* dB for the 2nd harmonic is typical. The highest 3rd harmonic amplitude of -12 dB is at 6.0-8.0 MHz carrier frequency. Information on suitable harmonic filters is available in Reference 3. The stability of the amplifier has been tested into a 3:1 load mismatch at all phase angles. It was found to be completely stable, even at reduced supply voltages.

In a MOSFET (common source) the ratio of feedback capacitance to the input impedance is several times higher than that of a bipolar transistor (common emitter). As a result, a properly designed FET circuit should be inherently more stable, especially under varying load conditions.

It must be noted, that special attention must be given to the heat sink design for this unit. With the 200-300 watts of heat generated by the transistors in a small physical area, it must be conducted into a heat sink efficiently. This can be only done with high conductance material, such as copper. If aluminum heat sink is used, a copper heat spreader is recommended between the transistor flanges and the heat sink surface.

FIGURE 6

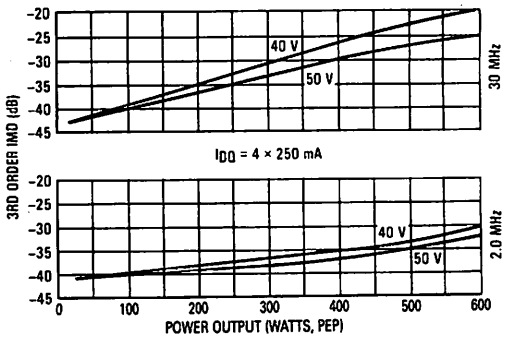
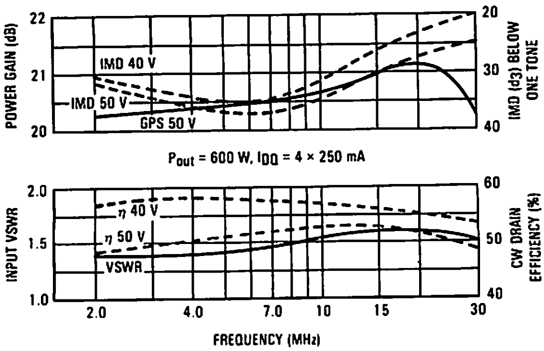
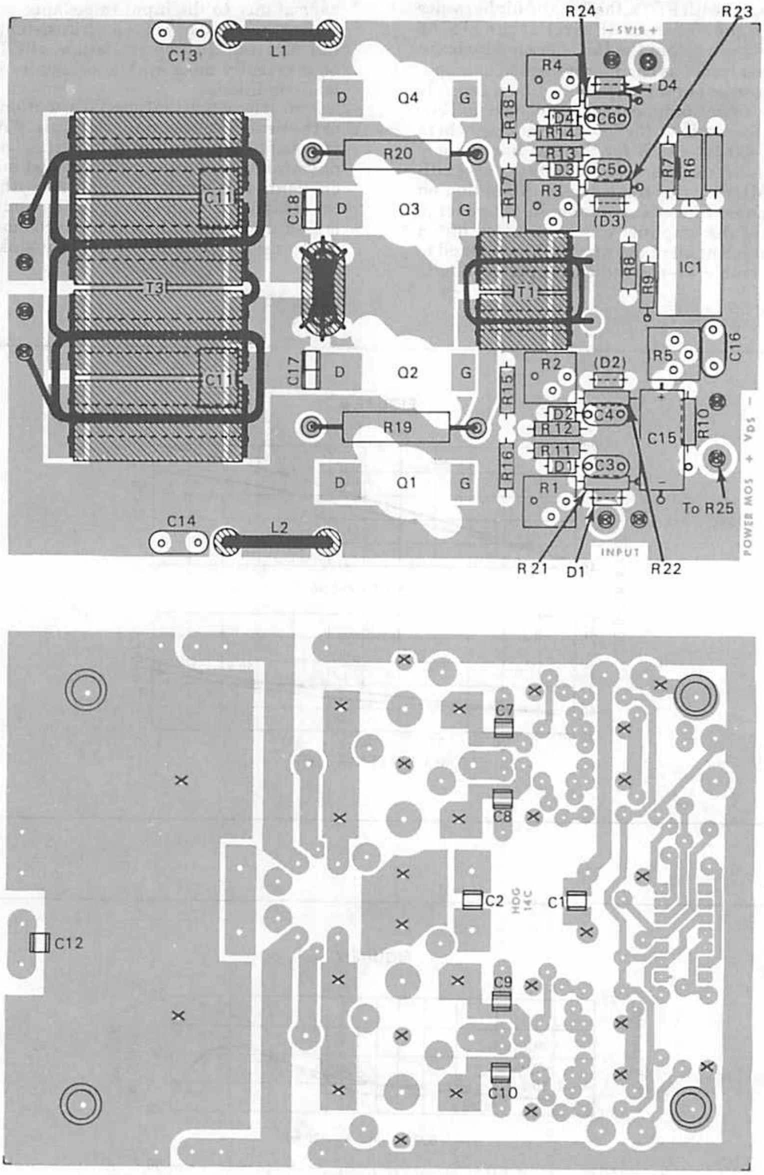


FIGURE 7



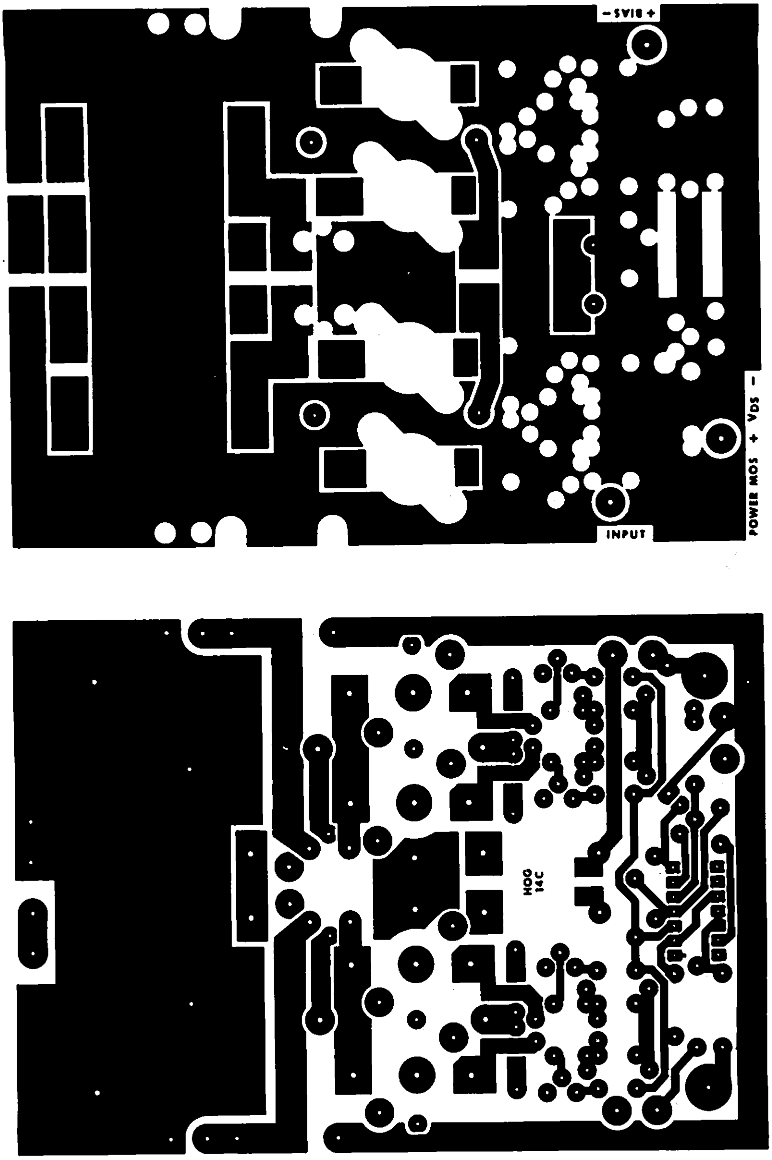


× denotes feed-through eyelets

⊗ denotes terminal pins

◎ denotes board spacers

FIGURE 8 — Component Locations



NOTE: The Printed Circuit Board shown is 75% of the original.

FIGURE 9 — Circuit Board Photo Master

REFERENCES

1. "A Two-Stage 1.0 kW Solid-State Linear Amplifier," AN-758, Motorola Semiconductor Products, Inc.
2. "Low-Distortion 1.6 to 30 MHz SSB Driver Designs," AN-779, Motorola Semiconductor Products, Inc.
3. H. Granberg, "MOS FET Power in the kW Level," QST, Dec., 1982, Jan., 1983

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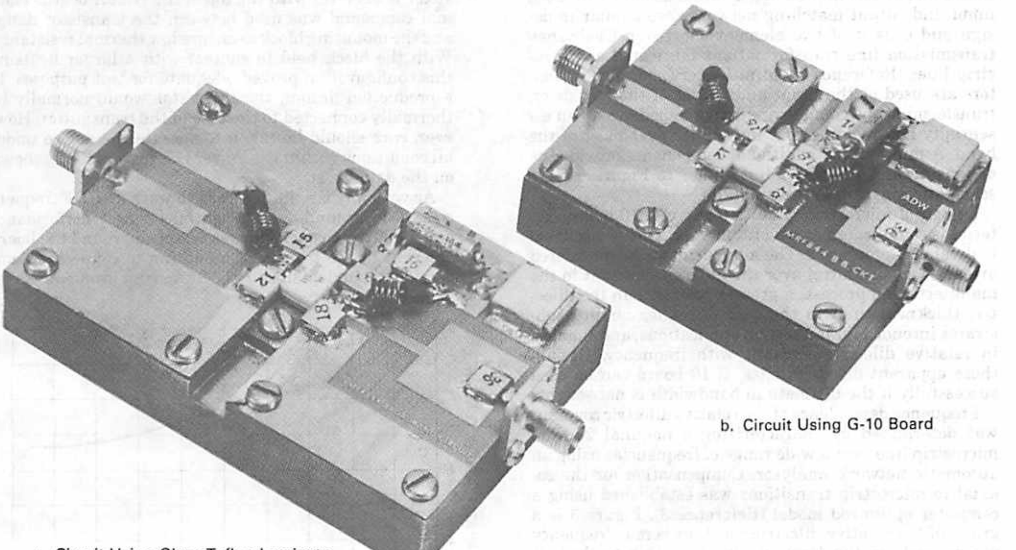
3. Granberg, *Power MOS FETs versus Bipolar Transistors*, RF Design, Nov. - Dec., 1981.
4. Hejhall, *VHF MOS Power Applications*, MIDCOM Paper, Dec., 1982
5. DeMaw, *Practical Class-A and Class-C Power — FET Applications at HF*, MIDCOM Paper, Dec., 1982

A 30 WATT, 800 MHz AMPLIFIER DESIGN

Prepared by
Alan Wood
Semiconductor Product Sector

INTRODUCTION

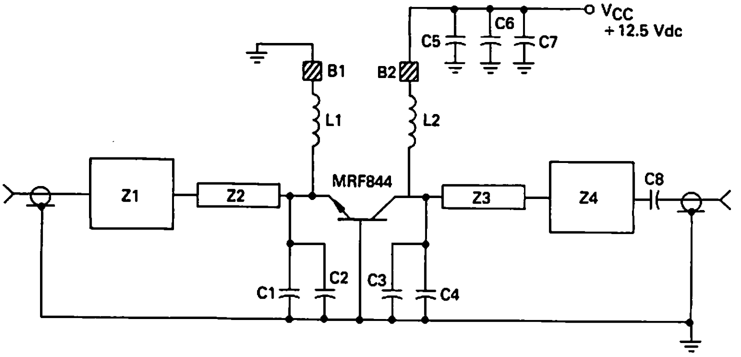
Simplicity and compactness mark the design of this 30 Watt amplifier designed for the 800 MHz mobile communications band. The amplifier uses the internally matched MRF844 transistor in a common base Class C configuration providing a minimum of 5.0 dB gain over a fixed tuned bandwidth of 800 to 870 MHz at 12.5 volts. Lower manufacturing costs are of prime concern to land mobile equipment suppliers and single-board, fixed tuned transmitter amplifier designs are becoming increasingly common. Two versions are therefore presented, one using glass teflon laminate and the second using less expensive G-10 board. (Figure 1).



b. Circuit Using G-10 Board

a. Circuit Using Glass Teflon Laminate

Figure 1 — Two Versions of MRF844 Broadband Circuit



B1, B2 —	Ferroxcube Bead 56-590-65/3B	L1, L2 —	4 Turns, #20 AWG Enameled Wire 0.15" ID
C1 — 15 pF	Mini-Underwood Mica	Z1 - Z4 —	Microstrip; See Photomasters
C2 — 12 pF	Mini-Underwood Mica	Board Material — See Text	
C3, C4 — 18 pF	Mini-Underwood Mica		
C5 — 91 pF	Mini-Underwood Mica		
C6 — 1000 pF	Unelco Mica		
C7 — 1.0 μF	Electrolytic		
C8 — 36 pF	Mini-Underwood Mica		

Figure 2 — Circuit Schematic of 30 Watt 806-870 MHz Amplifier

CIRCUIT DESCRIPTION

The circuit is designed to be driven from a 50 ohm source and be terminated in a nominal 50 ohm load. Both input and output matching networks are similar in design and consist of two element short-step Chebyshev transmission line transformations fabricated as microstrip lines (Reference 1). Mini-Underwood mica capacitors are used at the input and output of the transistor, transforming the complex inductive impedance to an essentially non-reactive real impedance over most of the band. A minimum of additional components provide the dc biasing and RF decoupling. Refer to Figure 2 for a schematic diagram of the amplifier.

Design of microstrip circuits using a G-10 board material is complicated by several factors. This is discussed in detail in Reference 2. The main points to be considered are, the lack of control over the dilectric constant in the manufacturing process; a greater tolerance in the dilectric thickness than in the case of higher quality substrates intended for microstrip applications, and changes in relative dilectric constant with frequency. Despite these apparent disadvantages, G-10 board can be used successfully if the ultimate in bandwidth is not sought.

Frequency dependence of the relative dilectric constant was determined by characterizing a nominal 25 ohm microstrip line over a wide range of frequencies using an automatic network analyser. Compensation for the coaxial to microstrip transitions was established using a computer optimized model (Reference 3). Figure 3 is a graph of the relative dilectric constant versus frequency determined for the laminate used by this method. It should be noted that differences in epoxy composition could affect both the low frequency dilectric constant and its frequency dependence.

CONSTRUCTION PROCEDURES

Both amplifiers were mounted on 0.5" thick copper blocks, 2.25" by 2" in the case of the G-10 board design and 3" by 2" for the glass teflon board. The blocks were slotted to a depth of 0.130" to enable mounting the transistor leads level with the top of the circuit board. Thermal compound was used between the transistor flange and the mounting block to ensure low thermal resistance. With the block held in contact with a larger heatsink this configuration proved adequate for test purposes. In a production design, the transistor would normally be thermally connected to the case of the transmitter. However, care should be taken to operate the device under all conditions within the Power Dissipation limits shown on the data sheet.

As with any circuit designed to work at UHF frequencies, good grounding is essential for best performance and stability. Copper foil was wrapped around the board adjacent to the transistor mounting to connect the underside ground plane to the transistor common leads.

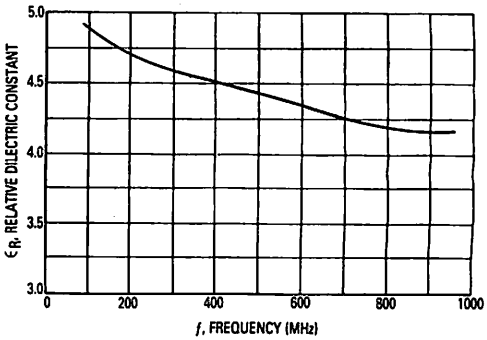


Figure 3 — Relative Dilectric Constant (G-10) versus Frequency

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Additional copper foil was wrapped around the board to connect the 1000 pF Unelco capacitor pad to the lower ground plane.

Positioning of the emitter and collector shunt capacitors is critical to the resulting amplifier performance. The capacitors should be mounted as close to the transistor case as possible. Minor tuning of the circuit can be achieved by lateral movement of these components. Larger tuning adjustments can be incorporated by replacing part of the fixed shunt capacitance by a variable trimmer.

Both circuits use 28 mil dilectric 2 ounce copper clad laminate. Refer to Figure 6 for a 1:1 Photomaster of the circuit boards.

PERFORMANCE DATA

Similar performance was measured for the same part soldered in either circuit. Typical performance curves for this broadband design are shown in Figures 4a, 4b, and 4c for the glass teflon design and Figures 5a, 5b, and 5c for the G-10 based circuit. Circuit losses in the G-10 board were less than expected and were certainly minimized by the short fractional wavelength transmission lines employed.

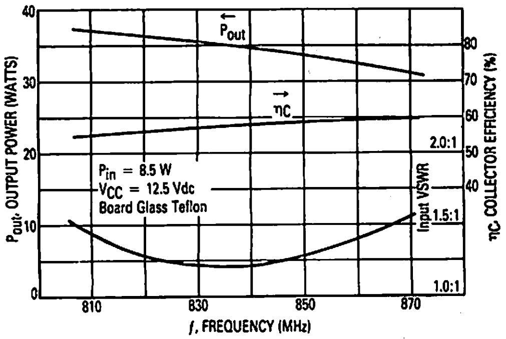

Figure 4a — Typical Performance in Broadband Circuit

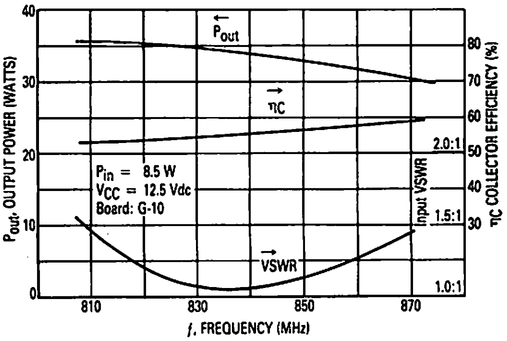

Figure 5a — Typical Performance in Broadband Circuit

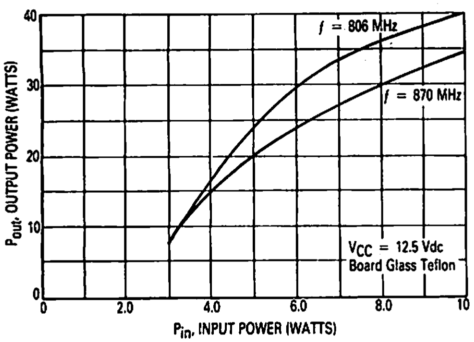

Figure 4b — Output Power versus Input Power

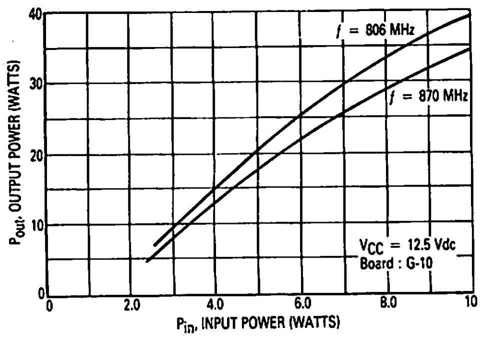

Figure 5b — Output Power versus Input Power

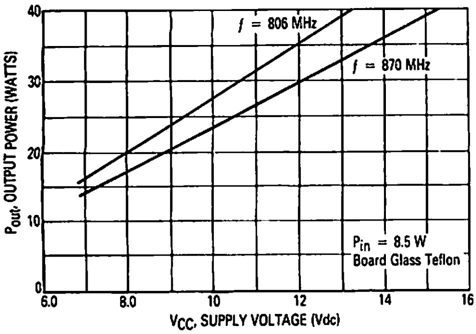

Figure 4c — Output Power versus Supply Voltage

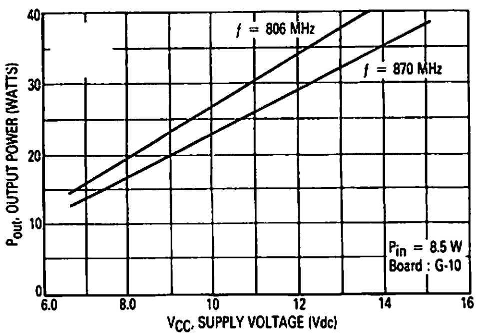

Figure 5c — Output Power versus Supply Voltage

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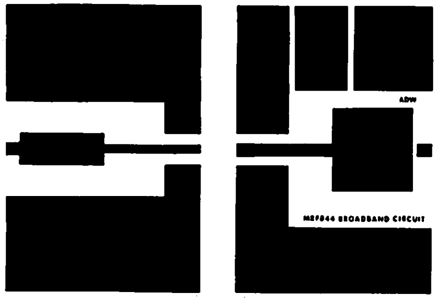
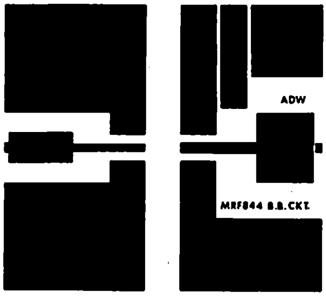
NOTE: The Printed Circuit Board shown is 75% of the original.



a. Photomaster Using Glass Teflon Laminate



b. Photomaster Using G-10 Board

Figure 6 — Two Photomaster Versions of MRF844 Broadband Circuit

REFERENCES

1. G. L. Mattheai. *Short-Step Impedance Transformers. IEEE Transactions on Microwave Theory and Techniques*. Vol. MTT-14 No 8 August 1966.

2. Glenn Young. *UHF Microstrip Amplifiers Utilizing G-10 Epoxy Glass Laminate*. Motorola Application Note AN-578.

3. M. L. Majewski. *Modeling and Characterization of Microstrip to Co-axial Transistions. IEEE Transactions on Microwave Theory and Techniques*. Vol. MTT-29 No 8 August 1981.

MOUNTING CONSIDERATIONS FOR MOTOROLA RF POWER MODULES

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RF Power Modules

INTRODUCTION

The packaging used for standard Motorola RF Power modules consists of a copper flange on which the substrates are soldered and a non-conductive cover which is either of a "snap-on" or epoxy attached design. The ceramic substrates are either 96% alumina (Al_2O_3), 99.5% alumina or 99% Beryllium oxide (BeO). These substrates are attached to the copper flange using either lead-tin or indium based soft solders. Typical liquidus temperatures of these solders are in the 149°C to 163°C range.

The purpose of this paper is to present the mechanical factors which should be considered in mounting these modules in equipment.

MAJOR MOUNTING FACTORS

There are three major considerations in mounting an RF power module. First, the flange is used for the RF electrical ground reference. Typical inductance of the connection pins used on these modules is about 18 nanohenries per inch or 1.8 nanohenries per 100 mils. Since at 800 MHz a nanohenry has about 5.0 ohms reactance, it is easy to see that it would be almost impossible to achieve a low reactance ground through the use of pins alone. Second, the copper flange provides the thermal path for the removal of the heat produced in the active devices present in the module. Thus, proper thermal handling must be considered in mounting the module. Finally, we must consider the mechanical stresses placed on the module by the mounting techniques used. Here we consider stresses placed on the leads and bending or twisting of the mounting flange which would cause ceramic fractures.

MODULE FLANGE FLATNESS

During the processing of the module, consideration has to be given to the various stresses produced. Through analysis of these stresses and the materials used we can arrive at the maximum allowable flange bending which can be tolerated from a mechanical standpoint. In determining the allowable flange flatness conditions, both analytical and empirical analyses were performed. Agreement between both of these analyses was very good. The theoretical analysis was performed by Motorola Government Electronics Group, Mechanical Engineering Laboratory. GEG was selected to do this work because they have done extensive work in the area of laminate stresses and have available several proven computer programs which apply directly to this problem. The assigned task was to provide an estimate of the maximum amount of initial bow (curvature) in the mounting flange which would not subsequently cause the ceramic substrate to fracture in the final assembled state. For the results of this analysis, see Table 1.

MOUNTING CONSIDERATIONS

The theoretical analysis shows that some of the responsibility for proper mounting rests on the user. Proper consideration should be given to the following items:

1. Flatness of the mounting area must be such that the final mounting of the module will not bend the flange beyond the limits given in Table 1.
2. Attention must be given to surface finish and cleanliness of the mounting surface. For instance, if one mounts the module with thermal compound and uses a dirty work area which allows 3 to 5 mil particles to be present in the compound, a failure mode can be produced.
3. Another consideration is the movement of material around tapped or punched holes. A tapped or punched hole which leaves a burr on the mounting surface can lead to failure modes.
4. In addition, rigidity of the mounting surface and its material should be considered. For instance, the copper flange on an aluminum heatsink will result in a bimetallic system which can create a bending problem. Consideration of the direction of ribs in a heatsink should be made to maximize stiffness in the direction of bending or adequate thickness of the heatsink must be provided to control bending.

It is not desirable to mechanically constrain the ends of the module so that no "slip" is possible between the module flange and its mounting surface. If the ends are constrained and the temperature differential between the module and the heatsink is significant, there can be enough bending of the module flange to break the ceramic. An example calculation is shown below to demonstrate this problem.

Assume that the ends of the flange are constrained at the centerline of the mounting holes. (2.4 inches for MHW612A/MHW710/MHW720 series modules). Assume that the module is mounted on a machined aluminum heatsink.

Thermal expansion coefficients in μinch/inch/°C

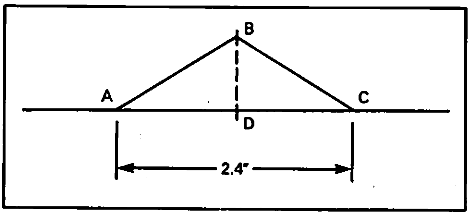
Aluminum 25×10^{-6}

Copper 17×10^{-6}

L = 2.4 inches

For a reasonable approximation assume the thermally induced bending creates an isosceles triangle as shown in Figure 1.

FIGURE 1



Assume that the module flange changes temperature from 25°C to 50°C and the heatsink changes temperature from 25°C to 30°C in the same time (obviously the heat input to the system comes from the copper flange — more on this later).

$$\text{Heatsink } \Delta \text{ L (aluminum)} = 2.4'' \times 5^\circ\text{C} \times 25 \times 10^{-6} = 0.0003''$$

$$\text{Flange } \Delta \text{ L (copper)} = 2.4 \times 25^\circ\text{C} \times 17 \times 10^{-6} = 0.00102''$$

So length ABC = 2.40102, AB = 1.20051"

length AC = 2.4003", AD = 1.20015

$$\text{And } AB^2 = AD^2 + BD^2$$

$$BD = \sqrt{AB^2 - AD^2}$$

So BD = 0.029397 inches which far exceeds the allowable flange bend.

This analysis also points out the advantage of keeping the heatsink and the flange at lowest possible temperature differential through the use of thermally conducting compounds between the surfaces.

For instance, in the example given above with an aluminum/copper system, the copper flange will remain in tension at any temperature *above* the temperature at which the system was constrained as long as the temperature ratio between the heatsink and flange is kept less than the ratio of the thermal expansion coefficients or 25/17. Incidentally, this assumes that the heat input source to the system originates in the copper flange. This situation points out the folly in some types of temperature cycling testing. For instance, if the aluminum/copper system is constrained at 25°C and is uniformly heated to say 125°C, the copper remains in tension — if the system is cooled below 25°C, the copper will go into compression. This is exactly the opposite situation obtained when the heat input to the system comes from the copper flange.

The above is a rather elementary analysis of the thermal effects on the module/heatsink system. Many other factors are involved such as relative strengths of the materials involved, bending of the mounting screws and so forth.

What should be derived from this discussion is that the design of the mounting for the module/heatsink system is not a simple one and should not be done in a casual manner.

Our recommendation is that a mock version of the system be constructed early in the equipment design and thermal cycling performed both with external heat input to the system and with heat input to the system from the module. This is a very effective "analog computer" and direct measurements of the flange/heatsink deflections can be made. In this manner the actual expected flange excursions can be compared to the recommended maximum flange bending to determine whether the design is adequate. Incidentally, the recommended maximum deflection values given in Table 1 have a safety factor of approximately 2. That is, the deflection required to crack the ceramic is approximately twice the value given. Table 1 includes data showing the empirical deflections required to fracture a ceramic board in the module.

5. We strongly recommend the use of a good thermal compound between the mounting surface. Sufficient material must be used to fill all gaps which may be present. We have not been able to create any mechanical problem with excess compound as long as there is a path for the excess material to escape as the module is tightened down with the mounting screws. At this point it should be pointed out that unless both the module flange and the heatsink were lapped to absolute gauge block flatness, there will always be a significant air gap between areas of the flange and the heatsink. Since it is obviously not practical to achieve a lapped surface of this quality, this portion of the mounting problem resolves to one of mechanical rather than thermal considerations. As an aside, some of the Motorola modules also have machined surfaces which may be oxidized to some degree. Infrared thermography of the active die was performed to see if there was any thermal degradation due to this oxide layer and no degradation could be found. This has also been found true on lapped discrete transistor flange mount parts.

Several manufacturers of thermally conductive heatsink compound exist. We have used products from Wakefield and Dow Corning with success.

MOUNTING HARDWARE

Obviously an ideal mounting hardware scheme would be one in which the clamping pressure remained constant with age. One way of achieving this is through the use of conical washers — one trade name is Belleville washers. Another possibility is "wavy" washers. Proper selection of mounting hardware and torque is also necessary. We recommend the following mounting hardware sizes and torques:

4–40	3 in/lb
6–32	5 in/lb
8–32	5 in/lb

TIGHTENING SEQUENCE

A very important factor to be considered in mounting the module is the proper torquing sequence. The personnel involved in mounting the modules should be given careful instruction and their procedures monitored at regular intervals. Since the flanges are punched from a

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roll of material, there can sometimes be a small "roll-up" at the end of the mounting flange. If one considers what can happen if the mounting hardware were tightened completely at one end first, it is easy to see that the other end could be "lifted" off the mounting surface well in excess of the allowable flange bending tolerance.

This should be avoided by first lightly alternately snubbing down the mounting hardware "finger-tight." Next, the hardware can be torqued to its final specification again in at least two sequential steps.

THE IMPORTANCE OF THIS TORQUING SEQUENCE CANNOT BE STRESSED TOO HIGHLY

LEADS

The leads used on the standard Motorola RF Power Modules are of either tinned copper, gold or silver plated KOVAR, or pure silver strap, typically 5 to 10 mils thick and 15 to 20 mils wide. The leads are intended for making electrical connections to the modules *only* and are not intended to support the module at any time in the assembly process. Consideration should be given to the stresses which may occur during mounting or testing. Poorly designed test fixtures can create lead stresses far above those encountered in the end-use equipment. It is recommended that the fixture be designed so the leads are always clamped after the flange is clamped and the tolerances be such that an upward force is never placed on the leads, even as the fixture wears. Motorola's specification for lead pull in shear and peel are 908 gm shear and 454 gm peel for BeO boards and 1500 gm shear and 750 gm peel for alumina boards. Modules from PC86, 90, and 91 product lines use BeO boards. Modules from the PC87, PC103 line use one alumina and one BeO board. PC41, PC64, and PC104 use alumina boards.

DEFLUXING

These modules are designed to be manually soldered into an assembly. The modules have a silicone die coat over the active die, MOS capacitors, and nichrome resistors. The die coat used will not withstand the normal flux removal fluids and severe reliability problems could be incurred if the flux removal fluids or solder fluxes penetrate the inside of the module. We recommend a flux activity of no more than R or RMA be used.

CONCLUSION

In mounting RF power modules, the following major areas should be considered:

1. Heatsink flatness.
2. Use thermal compound — eliminate dirt or grit in the compound or on mounting surfaces, use an adequate amount to fill gaps.
3. Tighten modules down in an alternate manner "finger-tight" before final torquing.
4. Be careful with defluxing operations.
5. Consider lead stresses, both in mounting and testing.

TABLE 1 — Maximum Deflection

DEVICES	THEORETICAL DEFLECTION TO BREAK		***EMPIRICAL DEFLECTION TO BREAK		MAXIMUM RECOMMENDED DEFLECTION COMBINED HEATSINK & FLANGE		OUTGOING QA SPEC. (MAX)	
	LINE		MIN	AVG	CONVEX	CONCAVE	CONVEX	CONCAVE
MHW709, 710	PC41	0.015	0.0190	0.0218	0.008	0.010	0.005	0.005
MHW720 *	PC64	0.015	0.0190	0.0206	0.008	0.010	0.005	0.005
MHW720 **	PC64	0.011	0.0075	0.0079	0.007	0.0085	0.003	0.005
MHW720A	PC104	—	0.0190	0.0206	0.008	0.010	0.005	0.005
MHW612, 613†	PC86	0.0025	0.0019	0.0028	0.0015	0.002	0.001	0.002
MHW612A, 613A†	PC87	0.011	0.0103	0.0108	0.007	0.0085	0.003	0.005
MHW808	PC90	—	0.0025	0.0034	0.0015	0.002	0.001	0.002
MHW808A	PC103	—	0.0065	0.0070	0.0035	0.004	0.0015	0.0025
MHW820	PC91	0.005	0.0073	0.0084	0.004	0.005	0.002	0.003

ALL UNITS IN INCHES

* PC64 was changed to alumina board — BeO carrier transistor construction similar to PC41 in February, 1983. All product with date code .883 and after has this construction.

** Old construction of PC64 with total BeO output board.

*** Measured deflection to break a substrate within 3 to 5 seconds of application of force.

† These devices will be obsolete on September 30, 1983. Contact Motorola for the current availability and recommended discrete transistor replacement lineup.

LOW COST UHF DEVICE GIVES BROADBAND PERFORMANCE AT 3.0 WATTS OUTPUT

Prepared by
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INTRODUCTION

The major cost element in low-to-medium power (1.0-5.0 W) RF transistors is the package. Several years ago Motorola took a major step in limiting cost increases by introducing the common emitter TO-39 package. Through the use of appropriate circuit design and construction techniques, use of the CE TO-39 can be extended to broadband UHF amplifiers producing up to 3.0 W output power.

This bulletin describes a broadband circuit application of the low cost MRF630 — an all gold metallized, emitter ballasted, high figure of merit transistor capable of 3.0 W output power with 10 dB gain at 512 MHz. A photo of the amplifier is shown in Figure 1. Emphasis is placed on mounting techniques which minimize parasitic inductances and maximize heat transfer.

CONSTRUCTION

TO-39's used as RF amplifiers are most commonly found in transmitter exciter chains mounted on printed circuit boards. The parts are seated on small disc shaped insulators and are heatsunk using press-fit "top hat" style radiators (Figure 2). Heat is inefficiently conducted upwards through the metal can (Figure 3) and radiated by commercially available heatsinks, called "top hats". As a result, the θ_{JA} is excessive, causing elevated junction temperatures and thermal slump problems. Because the TO-39 is situated above the PC board resulting in long leads, input Q's are also excessive and combine to limit broadband performance and device gain. In low power applications (<1.0 W) and VHF frequencies or lower, the problems mentioned above may not be noticeable. Higher power devices

FIGURE 1

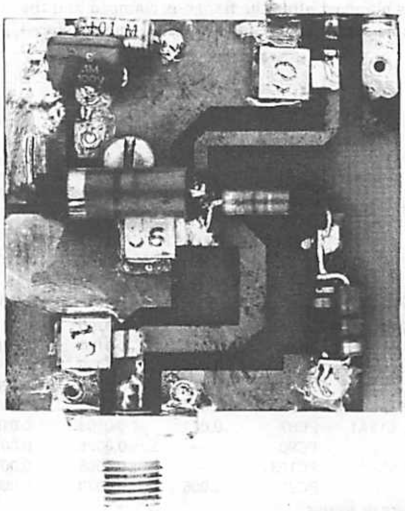

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FIGURE 2

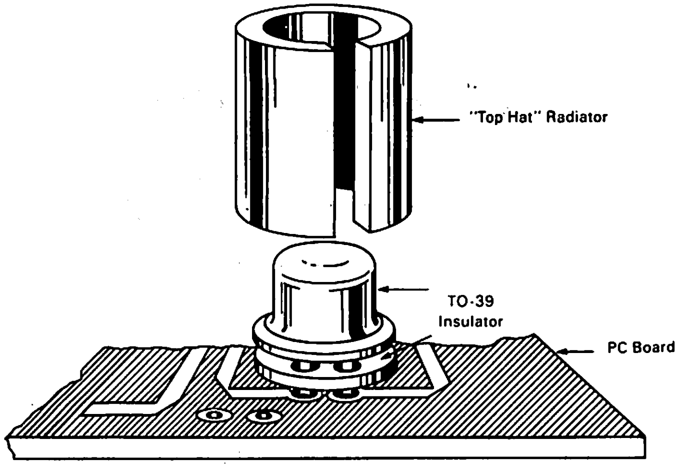
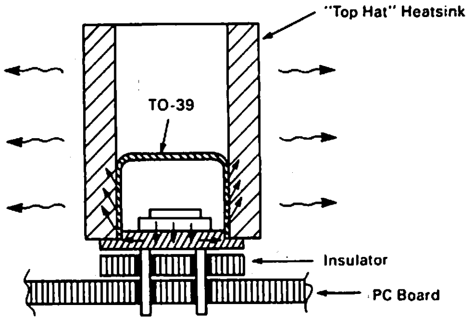


FIGURE 3



such as the MRF630, however, should be treated with the same considerations as any other RF power transistor (i.e., provisions for proper heatsinking and grounding).

When using an SOE power transistor, heatsinking is simplified with the inclusion of a stud or flange. Since TO-39's have neither, some modifications are required. Figure 4 depicts a means of heatsinking by soldering a "flange" to the bottom side of the TO-39 package, thus providing a path for heat flow directly beneath the transistor die. The "flange" is secured to the amplifier heatsink by one or two screws. With this arrangement, maximum heat dissipation can be provided with a minimum amount of space consumption. This method also creates better electrical grounding as the package is now mechanically connected to chassis ground. The attachment of this "flange" provides improvements in both grounding and heatsinking. Both are fundamental requirements to obtain the expected performance from an RF power TO-39 such as the MRF630.

CIRCUIT DESCRIPTION

The circuit, which was optimized for the MRF630, uses a distributed element design. Tight tolerance control is achieved by substituting transmission lines for inductors and specifying capacitor placement carefully. With this approach, good broadband performance is possible.

Since transmission line characteristics are dependent on line widths, dielectric properties and circuit board thickness, glass teflon circuit board is generally selected, as it offers the best tolerance control over the latter two variables. The major drawbacks of glass teflon circuit board are its low dielectric constant and relatively high price. A less expensive alternative, which was used in the construction of the MRF630 amplifier, is G10 printed circuit board. Its lower price coupled with its higher dielectric constant results in a smaller circuit and lower overall cost. The dielectric constant of G10 is not a controlled parameter, yet G10 is consistent enough to be useful for many applications at UHF frequencies.

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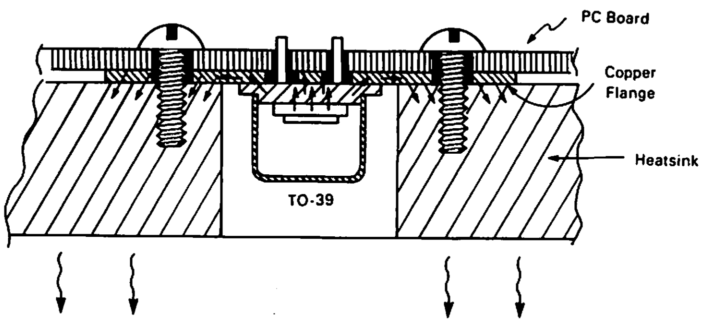
FIGURE 4



"Mini" clamped mica capacitors were chosen for the matching components in this amplifier design because of their low cost, availability and very high "Q". Mica is an extremely good dielectric and these capacitors, if carefully soldered (minimizing capacitor series lead inductance), boast a higher series reasonant frequency than some chip capacitors.

The use of G10 printed circuit board, "mini" clamped mica capacitors and the MRF630, enhance component repeatability, affordability, and availability.

PERFORMANCE

Broadband circuit performance is displayed in Figure 5 and a typical gain curve is shown in Figure 6. As can be seen, the MRF630 has excellent turn-on characteristics and saturated power capability. The normal gain roll-off above 490 MHz is expected but was minimized by optimizing both input and output impedance matching networks above that frequency. By adding additional matching sections, broadband performance down to 400 MHz could be achieved with respectable input VSWR's.

With the addition of the copper "flange" in the circuit assembly, average device θ_J-HS was limited to 12.3°C/W (dissipated power = 4.0 W, T_C = 60°C). The MRF630 was also mounted directly to the bottom of the printed circuit board, which was placed directly against the heatsink. The θ_J-HS degraded to only 15.6°C/W under the same conditions of power dissipation. If the PC board were "floating" using the same technique, higher θ_J-HS's would be observed. Assuming all circuit components were to be mounted in stripline fashion, allowing the PC board to be mounted directly to the heatsink, adequate heatsinking could be obtained without the addition of the "flange". The copper "flange" method of heatsinking is highly recommended for standard printed circuit boards which are isolated from the chassis heatsink.

An exploded view of the amplifier showing printed circuit board, flange and heatsink is shown in Figure 7. Figure 8 is a circuit schematic including parts list, while Figure 9 shows details of part location on the PC board. Finally, as an aid to duplication of the amplifier described herein, Figure 10 is a 1:1 photo master of the printed circuit board.

FIGURE 5 — Broadband Performance

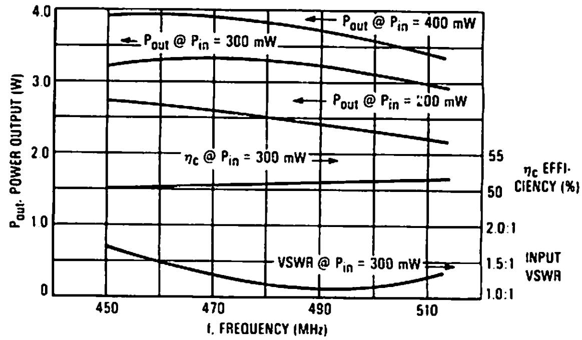
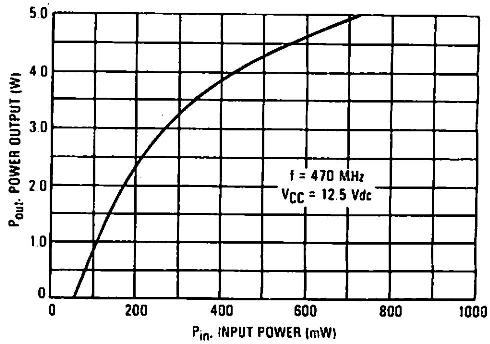


FIGURE 6 — Output Power versus Input Power



SUMMARY

Outlined in this article are methods of assuring the best possible performance from a low cost package; specifically, the MRF630 TO-39. If good construction practices are followed to ensure proper heatsinking and grounding, performance comparable to an SOE can be demonstrated, taking advantage of the cost benefits offered by a TO-39.

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FIGURE 7 — Exploded View of Amplifier Assembly

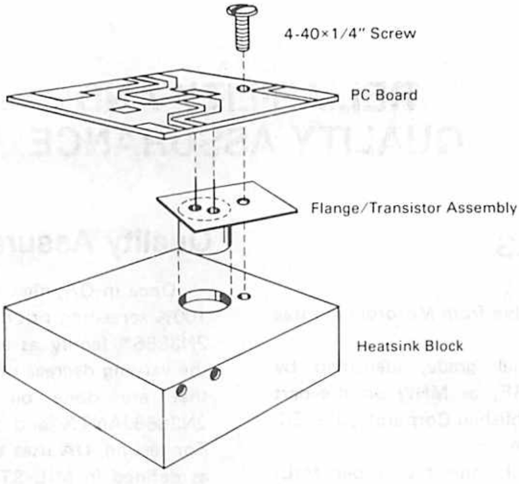
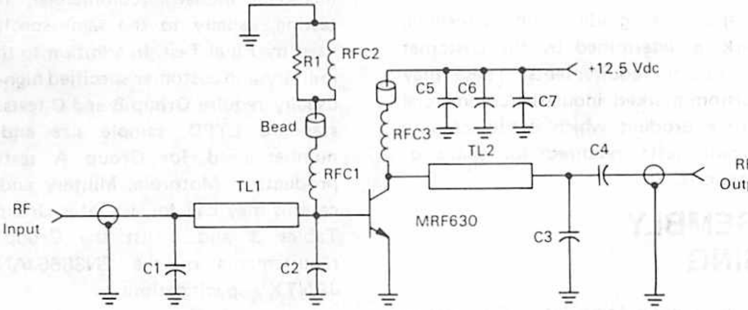


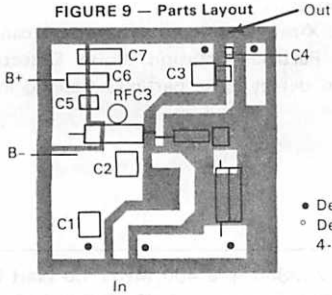
FIGURE 8 — Circuit Schematic and Parts List



C1, C3 — 10 pF Mini-Unelco
C2 — 36 pF Mini-Unelco
C4, C5 — 0.018 μF Chip Capacitor
C6 — 0.1 μF Dipped Capacitor
C7 — 1.0 μF Electrolytic
R1 — 12 Ω — 1/4 W Resistor

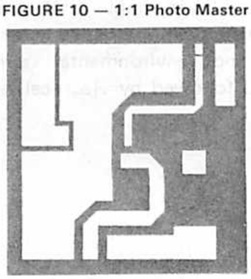
RFC1 — 0.15 μH Mini-Molded Choke
RFC2 — 1.0 μH Mini-Molded Choke
RFC3 — 0.15 μH Molded Choke
TL1 — Transmission Line 0.105 x 1.110" (W x L)
TL2 — Transmission Line 0.053 x 0.987" (W x L)
Board Material — 2 Oz. 0.0625" Epoxy Fiberglass (G-10)

FIGURE 9 — Parts Layout



• Denotes copper eyelets.
° Denotes 4-40 clearance for 4-40 screw mounting.

FIGURE 10 — 1:1 Photo Master



NOTE: The Printed Circuit Board shown is 75% of the original.

RELIABILITY AND QUALITY ASSURANCE

QUALITY LEVELS

RF Products are available from Motorola in three quality levels:

1. Industrial/commercial grade, identified by a prefix such as 2N, MRF, or MHW on the part number and tested to a published Corporate, JEDEC, or Proelectron specification.
2. Military grade, built and tested per MIL-S-19500 and identified by a 2N prefix and JAN, JTX, or JTXV suffix.
3. Customer-specified grade with screening, testing, and marking determined by the customer to meet his particular requirements. These may range from a custom-marked industrial/commercial grade product to a product which is subjected to the most stringent tests required for space or submarine applications.

POST-ASSEMBLY PROCESSING

After assembly, a production lot is first sent to Final Test, then is transferred to Quality Assurance.

Final Test Processing

In Final Test, 100% of a lot is processed. This processing may be as simple as electrical testing to a data sheet specification or as complex as a series of mechanical and environmental screening tests preceded and followed by electrical tests.

Quality Assurance Processing

Once in QA, high-rel lots may undergo additional 100% screening prior to testing. Using the popular 2N3866* family as an example, Table 1 compares the varying degrees of preconditioning and screening that are done on the 2N3866, 2N3866JAN, 2N3866JANTX and the 2N3866JTXV transistors. For testing, QA uses test sample groups A, B, and C as defined in MIL-STD 19500. Individual tests are defined in MIL-STD-202, 750, and 883. All lots, including industrial/commercial, receive Group A testing, usually to the same specification which is used by Final Test. In addition to the Group A tests, military and customer-specified high-rel specifications usually require Group B and C tests. Table 2 lists the standard LTPD, sample size and lot acceptance number used for Group A testing of standard products at Motorola. Military and high-rel specifications may call for a tighter Group A sample plan. Tables 3 and 4 list the Group B and C test requirements of the 2N3866JAN and 2N3866-JANTXV specifications.

Special Processing

Three additional tests that may be specified at extra cost by a high-rel customer are:

1. Scanning electron microscope inspection of a wafer.
2. X-ray examination of metal can transistors.
3. Particle Inclusion Noise Detection (PIND) test to detect loose particles trapped in a package.

*The 2N3866 is a 400 MHz, 1.0 Watt NPN silicon transistor mounted in a TO-39 metal can.

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TABLE 1 – 100% PRECONDITIONING AND SCREENING (2N3866 Family)

Test	MIL-S-750 Method	Condition	2N3866/JAN	2N3866JTX/V
Final Test				
1. Electrical Tests		Go/No Go		
(Same as Group A)		Remove Rejects	100%	100%
2. High Temperature Storage		200°C, 24 hours	Omit	100%
3. Temperature Cycling	1051	C, 10 cycles	Omit	100%
4. Constant Acceleration	2006	20,000 G Y_1	Omit	100%
5. Hermetic Seal	1071		Omit	100%
Fine Leak		G or H		
Gross Leak		A, B, C, D or F		
6. HT R B		150°C, 48 hr, 24 V	Omit	100%
7. Electrical Tests				
(Similar to Group A)			Omit	100%
QA				
8. Electrical Tests		Go/No Go	Omit	100%
9. Establish Identity			Omit	100%
10. Electrical Tests	I_{CBO} and h_{FE}		Omit	100%
11. Burn In	with	168 hr, 1.0 W	Omit	100%
12. Electrical Tests	Deltas	PDA = 10%	Omit	100%

TABLE 2 — STANDARD GROUP A SAMPLING PLANS (Discrete Products)

Characteristic (By Subgroup)	LTPD	Sample Size	Accept Number
Discrete Devices			
Visual and Mechanical	3.0	129	1
DC Parameters	3.0	129	1
AC and Temperature Parameters	7.0	55	1
Opens/Shorts	1.75	129	0
Discrete Wafers and Dice			
Visual and Mechanical			
Multipack and Decca Pack (100% Sorted)	10	38	1
Wafer Sales and Vial Package (no 100% Sort)	20	38	4
DC Parameters	10	38	1
AC and Temperature Parameters	15	25	1

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TABLE 3 — GROUP B TESTS (2N3866 Family)

Inspection or Test	MIL-S-750 Method	Condition	LT P D (Accept No.)	
			2N3866JAN	2N3866JTX/V
Subgroup B-1 Physical Dimensions	 2066		20(1)	20(1)
Subgroup B-2 Solderability Temperature Cycling Thermal Shock Hermeticity Fine Leak Gross Leak Moisture Resistance	 2026 1051 1056 1071 1021	 C B IIIa G, or H A, B, C, D or F 	15(1)	15(1)
Subgroup B-3 Shock Variable Freq. Vib Constant Acceleration	 2016 2056 2006	 1500 G 20,000 G	15(1)	15(1)
Subgroup B-4 Lead Fatigue	 2036	 E	20(1)	20(1)
Subgroup B-5 Salt Atmosphere	 1041		20(1)	20(1)
Subgroup B-6 High Temperature Storage Life	 1031	 200°C	7(1) (340 hours)	5(1) (1000 hours)
Subgroup B-7 Steady State Operating Life	 1026	 $T_A = 25°C$ $V_{CB} = 25$ V $P_T = 1$ W	7(1) (340 hours)	5(1) (1000 hours)

TABLE 4 — GROUP C TESTS (2N3866 Family)

Inspection or Test	MIL-S-750 Method	Condition	LTPD (Accept No.)	
			2N3866JAN	2N3866JTX/V
Subgroup C-1 Barometric Pressure Thermal Resistance	 1001 3151		10(1)	10(1)
Subgroup C-2 Burnout by Pulsing	 3005		10(1)	10(1)
Subgroup C-3 High Temperature Storage Life	 1031	Extension of B-6 to 1000 hrs	10(1)	–
Subgroup C-4 Steady State Operating Life	 1026	Extension of B-7 to 1000 hrs	10(1)	–

Test Descriptions

The following tests are frequently used for screening, acceptance and evaluation of semiconductor devices.

A. Steady State Operating Life (SSOL)

The purpose of this test is to evaluate the bulk stability of the die and to generate defects resulting from manufacturing aberrations that are manifested as time and stress-dependent failures.

Conditions: T_A = 25°C, PD = max rated power

B. Intermittent Operating Life (IOL)

The purpose of this test is the same as Operating Life in addition to checking the integrity of both the wire and die bonds by means of thermal stressing.

Conditions: T_A = 25°C, PD = max rated power. $T_{(on)}$ = $T_{(off)}$ = 1 min.

C. High Temperature Storage Life

The purpose of this test is to generate time/temperature failure mechanisms and to evaluate long-term storage stability.

Conditions: T_A = 150°C no bias applied

D. High Temperature Reverse Bias (HTRB)

The purpose of this test is to align mobile ions by means of temperature and voltage stresses to form a high-current leakage path between two or more terminals.

Conditions: T_A = 150°C, V_{CB} = 80% max rated V_{CB}.

E. High Temperature High Humidity Reverse Bias (H^3TRB)

The purpose of this test is to evaluate the moisture resistance of non-hermetic components. The addition of voltage bias accelerates the corrosive effect after moisture penetration has taken place. With time, this is a catastrophically destructive test.

Conditions: T_A = 85°C, RH = 85%, V_{CB} = 80% max rated V_{CB}.

F. Moisture Resistance

The purpose of this test is to evaluate the moisture resistance of components under temperature/humidity conditions typical of tropical environments.

Conditions: Mil-Std-750, Method 1021.

G. Pressure Cooker

The purpose of this test is to evaluate the moisture resistance of non-hermetic components under pressure/temperature conditions.

Conditions: T = 121°C, P = 1 atmosphere (15 psig)

H. Temperature Cycle (Air to Air)

The purpose of this test is to evaluate the ability of the device to withstand both exposure to extreme temperatures and the transition between temperature extremes, and to expose excessive thermal mismatch between materials.

Conditions: Mil-Std-750, Method 1051, –55°C to 150°C, 15 minutes dwell time at each temperature

I. Thermal Shock (Liquid to Liquid)

This test is an accelerated version of temperature cycle.

Conditions: Mil-Std-750, Method 1056, 0°C to 100°C, 15 seconds dwell time at each temperature

J. Terminal Strength

The purpose of this test is to evaluate the ability of the device terminals to withstand the lead forming and tension associated with component installation into a circuit.

Conditions: Mil-Std-750, Method 2036, Condition E.

K. Solderability

The purpose of this test is to determine the solderability of the device terminals.

Conditions: Mil-Std-750, Method 2026.

L. Salt Atmosphere (Corrosion)

The purpose of this test is to accelerate the corrosion effects of an environment in which salt (NaC1) is present.

Conditions: Mil-Std-750, Method 1041

M. Mechanical Stress Tests

Vibration, shock and constant acceleration tests are infrequently used since they rarely generate failures in small-signal transistors. However, they are still specified for acceptance of military product.

HIGH RELIABILITY PROCESSING OF RF TRANSISTORS

I WAFER PROCESSING

After wafers are processed, they are subjected to Motorola visual inspection specifications then probe tested to determine compliance with Group A specifications upon completion. Probe tests include the following: (1) Class Probe — performed to determine device type and yield; (2) Unit Probe each unit is subjected to Group A electrical tests — rejects are inked. Following the class and unit probe tests, the wafer is scribed and broken.

II ASSEMBLY

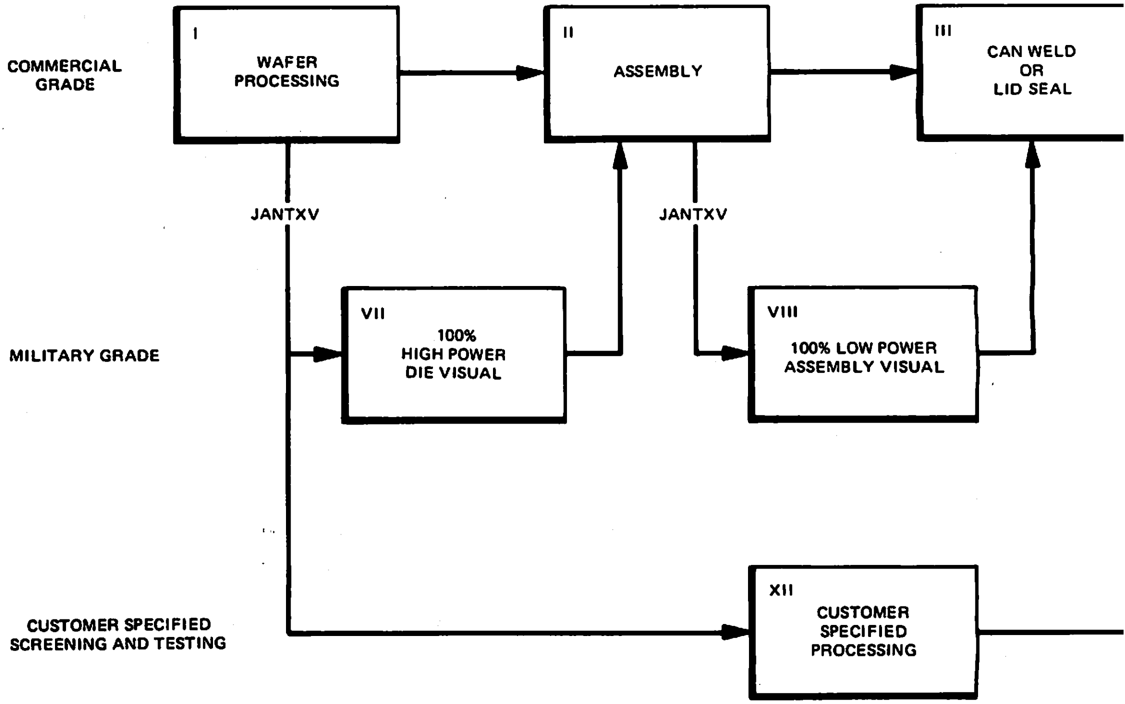
The die are attached to headers and then wire bonded. Wire pull tests are performed by Quality Control inspectors on a sample basis to ensure assembly process controls.

Units are stored in dry air until ready for capping.

III CAN WELD OR LID SEAL

Completed headers are loaded into a vacuum chamber for can weld or processed thru a furnace for metal top attachments on ceramic packages with solder preforms.

PROCESSING AND QUALITY CONTROL FLOW CHART



VII 100% HIGH POWER DIE VISUAL

The high power portion of the inspection is performed to assure good die construction and front metal conditions. Individual reject criteria includes the following: Metallization defects such as scratches, voids, corrosion, adherence, bridging and alignment. Poor die construction conditions such as oxide and diffusion faults are also rejected.

VIII 100% LOW POWER ASSEMBLY VISUAL

The low power visual inspection controls workmanship, i.e., die attachment, internal lead-wire attachment, and package defects. Die attachment inspection includes assuring good adherence, die placement and proper orientation. Internal lead wires must have proper arc and all attachment bonds must be properly placed and in good condition. Package defect inspection includes checking for foreign material, improper construction and cracked glass conditions.

IV FINAL ELECTRICAL TEST

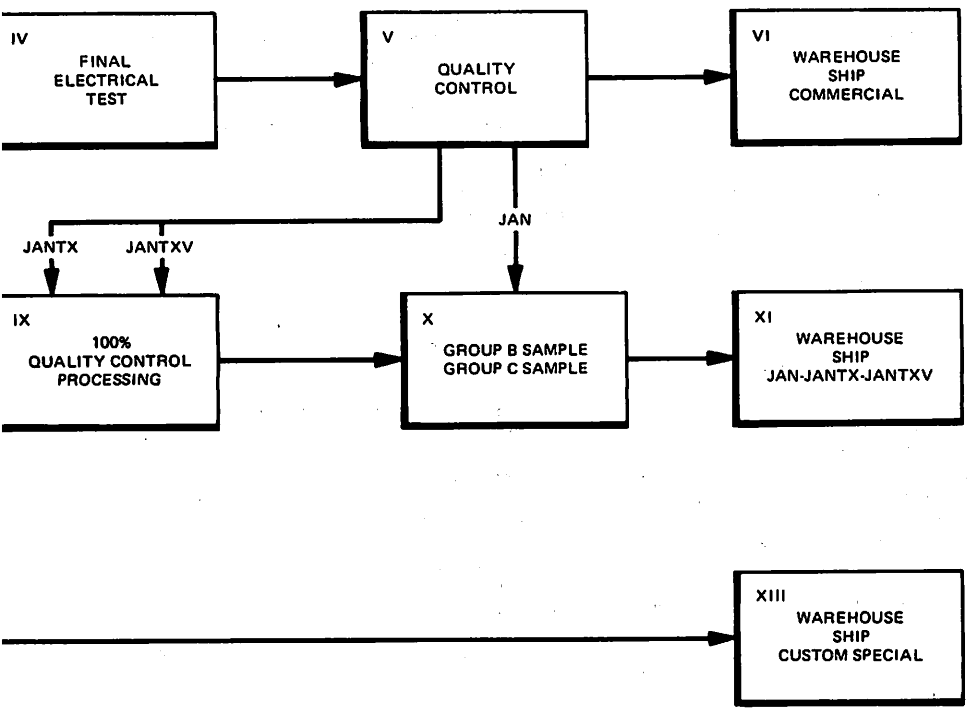
pleted units are selected for a Group A elec- test. Hand screening is performed where ssary. Electrical fallout units and over-runs ubject to future screening.

V QUALITY CONTROL

Samples are taken for complete electrical analysis of the lot. Group A and B tests are performed on JAN devices. Group A and B tests and 100% processing are performed on JANTX devices. Some devices also require Group C inspection tests.

VI WAREHOUSE

Upon completion, the finished product is ready for shipping. Purchase order requirements are carefully checked again prior to shipping. Overruns are kept for future orders. Warranty tests (Group A) are performed every 24 months on military devices.



IX 100% QUALITY CONTROL

a. High temperature storage
b. High temperature reverse bias
c. Temperature cycling
d. Thermal shock
e. Hermetic seal
f. Acceleration
g. Read & Record parameters
h. Room temperature burn-in

X GROUP B AND GROUP C INSPECTION

Typical Group B Processing (Sample Basis)

a. Physical dimensions
b. Moisture resistance
c. Terminal strength
d. Hermetic seal
e. Solderability
f. Vibration fatigue
g. 1000 hr. storage life
h. 1000 hr. operating life

Typical Group C Processing (Sample Basis)

a. ac parameters
b. Barometric pressure
c. Burn out pulsing
d. Resistance to solvents

Glossary of Reliability and Quality Terms

Acceptable Quality Level (AQL) — A measure of quality for which a given lot will be accepted most of the time. This is usually established at a probability of acceptance equal to 95%. It is referred to as the producer's risk because the probability of rejecting a good lot is 5%.

Acceptance Number (Ac) — The largest number of defectives in an inspection sample under consideration that will permit acceptance of the lot.

Acceptance Tests — Tests to determine conformance to specification requirements as a basis for lot acceptance.

Average Outgoing Quality (AOQ) — The average quality of outgoing product after 100% screening of rejected lots. This is usually measured in parts per million (PPM).

Average Outgoing Quality Limit (AOQL) — The maximum average outgoing quality that is possible for a given sampling plan.

Defect — Any deviation of a device that does not conform to specified requirements. One device may contain more than one defect.

Defective — A device which contains one or more defects.

Double Sampling — Sampling inspection in which the inspection of the first sample leads to a decision to accept, to reject, or to take a second sample. The inspection of a second sample, when required, always leads to a decision to accept or to reject.

Failure — The inability of a device to perform a specified function within previously-established limits.

Failure Rate — The statistical probability of a failure occurring within a stated period of time. For electronic components it is usually assumed that failures follow an exponential distribution, in which case the failure rate over any stated period of time is constant. The failure rate of semiconductor devices is generally given in percent per thousand hours.

Infant Mortality — Premature failures occurring at a failure rate substantially greater than that observed during subsequent life prior to wear-out.

Lot — A group of devices from which samples are drawn and inspected to determine compliance with acceptance criteria (inspection lot).

Lot Tolerance Percent Defective (LTPD) — A measure of quality for which a given lot will be rejected most of the time. This is usually established at a probability of acceptance equal to 10%. It is referred to as the consumer's risk because the probability of accepting a bad lot is 10%.

Mean Time Between Failures (MTBF) — The total measured operating time of a group of equipments divided by the total number of failures of a repairable equipment. In the case of an exponential failure distribution, this ratio is the reciprocal of failure rate.

Operating Characteristic Curve (OC curve) — A graph of the probability of acceptance as a function of the lot quality or process average quality, whichever is applicable.

Percent Defective — The number of defective devices in a lot divided by the total number of devices in that lot, multiplied by 100.

Probability of Acceptance (Pa) — The fractional probability that a lot will be accepted, usually expressed as a decimal.

Process Average Quality — The expected quality of product from a given process, usually estimated from first sample results of previous inspection lots.

Quality — A measure of the degree to which a product conforms to specification and workmanship requirements.

Rejection Number (Re) — The smallest number of defectives in an inspection sample under consideration that will prevent acceptance of the lot.

Reliability — A measure of the performance of a product over a specified period of time.

Sample — One or more devices selected at random from an inspection lot to represent that lot for acceptance purposes.

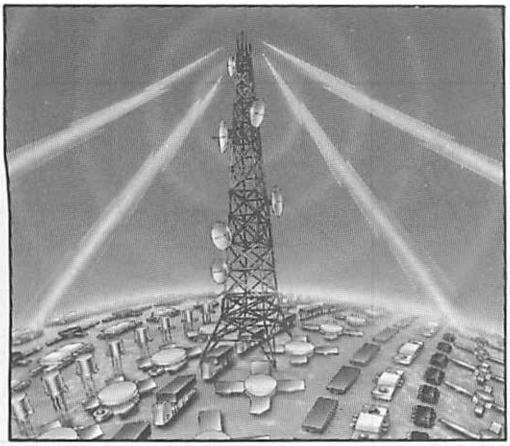
Sampling Plan — A specific plan which defines the sample size and the criteria for accepting or rejecting a lot.

Screening Tests — Tests employing nondestructive environmental, electrical, thermal and/or mechanical stresses, for the purpose of identifying anomalous devices.

Single Sampling — Sampling inspection in which a decision to accept or to reject is reached after the inspection of a single sample.

Wearout Failures — Those failures which occur as a result of deterioration processes and whose probability of occurrence increases with time.

100% Inspection — Inspection of every device, in which each device is accepted or rejected individually for the characteristic concerned, on the basis of its own inspection only.

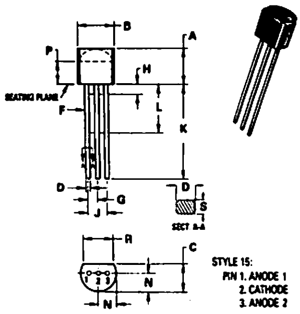


Volume II

Case Dimensions

8

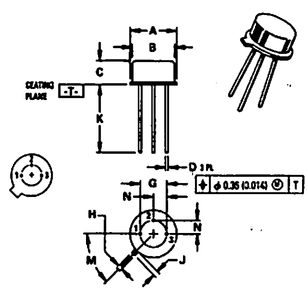
Case Dimensions



STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
H	—	2.54	—	0.100
J	2.42	2.66	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.04	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.39	0.50	0.015	0.020

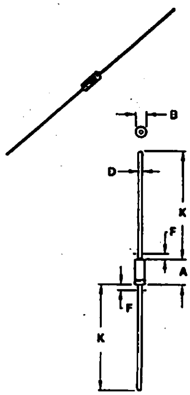
CASE 29-04
(TO-226AA)



STYLE 2:
PIN 1. INPUT
2. OUTPUT
3. GROUND

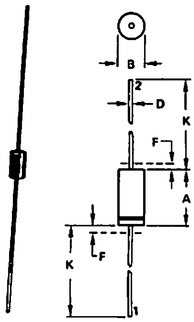
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.50	0.305	0.335
C	3.81	4.57	0.165	0.185
D	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	—	0.500	—
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	

CASE 31A-03
(TO-205AD)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.84	7.62	0.230	0.300
B	2.16	2.72	0.085	0.107
D	0.46	0.56	0.018	0.022
F	—	1.27	—	0.050
K	25.40	38.10	1.000	1.500

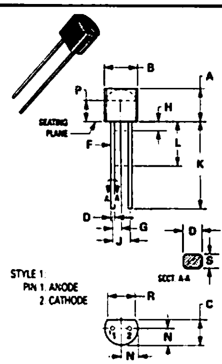
CASE 51-02



STYLE 1:
PIN 1. CATHODE
2. ANODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.84	7.62	0.230	0.300
B	2.74	3.56	0.108	0.140
D	0.46	0.56	0.018	0.022
F	—	1.27	—	0.050
K	25.40	—	1.000	—

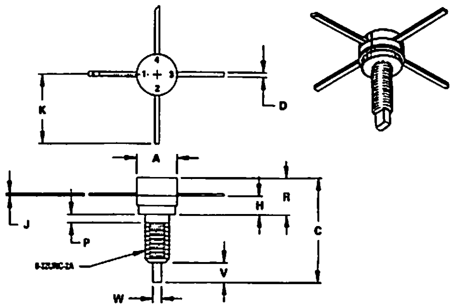
CASE 146-01



STYLE 1:
PIN 1. ANODE
2. CATHODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.407	0.482	0.016	0.019
G	1.27 BSC		0.050 BSC	
H	—	1.27	—	0.050
J	2.54 BSC		0.100 BSC	
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

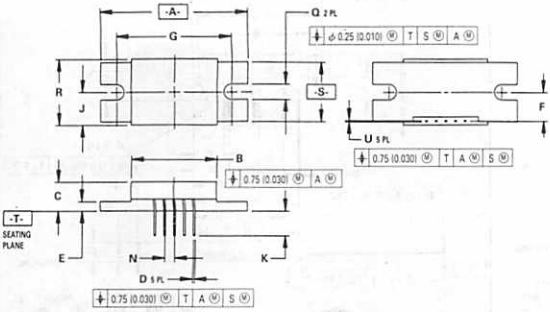
CASE 182-02



STYLE 1:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.74	7.23	0.265	0.285
C	14.94	16.23	0.588	0.639
D	0.64	0.89	0.025	0.035
H	2.65	3.40	0.104	0.134
J	0.11	0.15	0.004	0.006
K	11.18	11.68	0.440	0.460
P	1.40	1.65	0.055	0.065
R	5.21	6.35	0.205	0.250
V	2.93	3.68	0.115	0.145
W	1.40	1.65	0.055	0.065

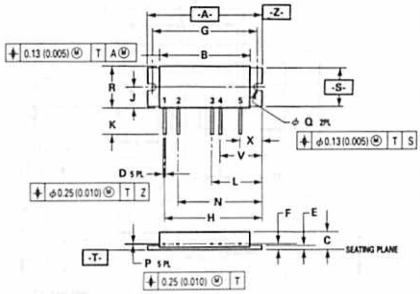
CASE 244D-01



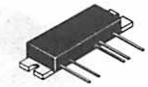
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	37.85	38.35	1.490	1.510
B	22.22	22.73	0.875	0.895
C	8.26	9.27	0.325	0.365
D	0.46	0.55	0.018	0.022
E	2.16	2.54	0.085	0.100
F	7.87 BSC		0.310 BSC	
G	29.72 BSC		1.170 BSC	
J	8.26	8.89	0.325	0.350
K	6.32	7.62	0.250	0.300
N	2.54 BSC		0.100 BSC	
Q	3.81	4.11	0.150	0.162
R	16.64	17.40	0.655	0.685
S	15.12	15.62	0.595	0.615
U	0.20	0.30	0.008	0.012

STYLE 1:
PIN 1. RF INPUT
2. V DRIVER
3. GROUND
4. V_{CC}
5. RF OUTPUT
CASE: GROUND

CASE 297C-02

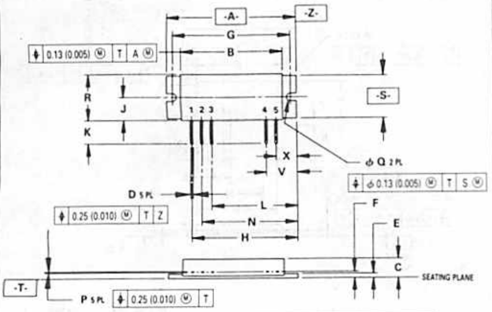


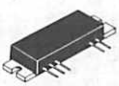
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	44.71	45.21	1.760	1.780
B	34.80	35.30	1.370	1.390
C	6.23	6.73	0.245	0.265
D	0.46	0.55	0.018	0.022
E	2.04	2.54	0.080	0.100
F	3.30 BSC		0.130 BSC	
G	41.91 BSC		1.650 BSC	
H	37.72 BSC		1.485 BSC	
J	6.79	7.06	0.267	0.278
K	5.85	7.62	0.230	0.300
L	19.94 BSC		0.785 BSC	
N	32.64 BSC		1.285 BSC	
P	0.21	0.30	0.008	0.012
Q	3.05	3.30	0.120	0.130
R	13.59	14.09	0.535	0.555
S	11.31	11.81	0.445	0.465
V	17.40 BSC		0.685 BSC	
X	9.78 BSC		0.385 BSC	



STYLE 1:
PIN 1. RF INPUT/V CONT
2. VS1
3. VS2
4. VS3
5. RF OUTPUT
CASE:

CASE 301E-04

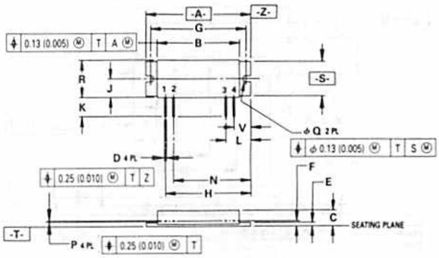


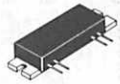


STYLE 1:
PIN 1. RF INPUT
2. + DC
3. + DC
4. + DC
5. RF OUTPUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	55.63	56.13	2.190	2.210
B	35.44	35.94	1.395	1.415
C	8.89	9.55	0.350	0.376
D	0.46	0.55	0.018	0.022
E	3.05	3.42	0.120	0.135
F	4.06 BSC		0.160 BSC	
G	48.26 BSC		1.900 BSC	
H	40.64 BSC		1.600 BSC	
J	8.77	9.77	0.345	0.385
K	5.72	—	0.225	—
L	35.56 BSC		1.400 BSC	
N	38.10 BSC		1.500 BSC	
P	0.21	0.30	0.008	0.012
Q	3.81	4.06	0.150	0.160
R	17.53	19.55	0.690	0.770
S	15.12	15.49	0.595	0.610
V	17.78 BSC		0.700 BSC	
X	12.70 BSC		0.500 BSC	

CASE 301G-03





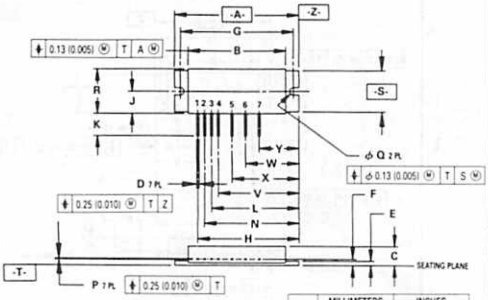
STYLE 2:
PIN 1. RF INPUT
2. + DC (CONTROL)
3. + DC (SUPPLY)
4. RF OUTPUT
CASE: GROUND

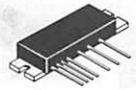
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	48.01	48.51	1.890	1.910
B	29.72	30.22	1.170	1.190
C	8.89	9.55	0.350	0.376
D	0.46	0.55	0.018	0.022
E	3.05	3.42	0.120	0.135
F	4.06 BSC		0.160 BSC	
G	40.64 BSC		1.600 BSC	
H	35.56 BSC		1.400 BSC	
J	8.77	9.77	0.345	0.385
K	5.72	—	0.225	—
L	17.78 BSC		0.700 BSC	
N	33.02 BSC		1.300 BSC	
P	0.21	0.30	0.008	0.012
Q	3.81	4.06	0.150	0.160
R	17.40	19.55	0.685	0.770
S	15.12	15.49	0.595	0.610
V	12.70 BSC		0.500 BSC	

CASE 301H-03

8

CASE DIMENSIONS (continued)

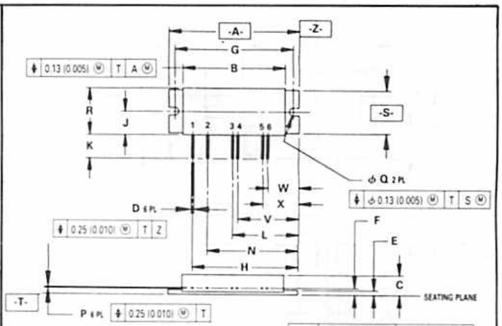


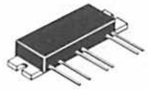


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	44.84	45.21	1.765	1.780
B	34.80	35.30	1.370	1.390
C	6.35	6.73	0.250	0.265
D	0.46	0.55	0.018	0.022
E	2.16	2.54	0.085	0.100
F	3.35 BSC		0.132 BSC	
G	42.02 BSC		1.654 BSC	
H	37.77 BSC		1.487 BSC	
J	6.79	7.06	0.267	0.278
K	3.81	11.43	0.150	0.450
L	32.69 BSC		1.287 BSC	
N	35.23 BSC		1.387 BSC	
P	0.21	0.30	0.008	0.012
Q	3.05	3.30	0.120	0.130
R	13.59	14.09	0.535	0.555
S	11.31	11.81	0.445	0.465
V	30.15 BSC		1.187 BSC	
W	19.99 BSC		0.787 BSC	
X	25.07 BSC		0.987 BSC	
Y	14.91 BSC		0.587 BSC	

STYLE 1:
PIN 1. RF INPUT
2. VS1
3. VCONT
4. VS2
5. VS3
6. VS4
7. RF OUTPUT

CASE 301J-02

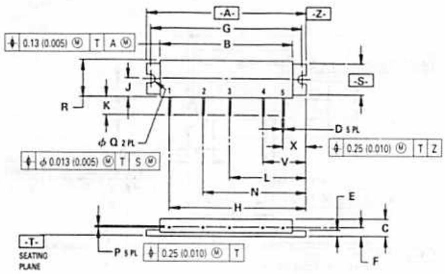


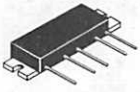


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	44.96	45.34	1.770	1.785
B	34.80	35.31	1.370	1.390
C	6.35	6.73	0.250	0.265
D	0.46	0.55	0.018	0.022
E	2.16	2.54	0.085	0.100
F	3.35 BSC		0.132 BSC	
G	42.04 BSC		1.655 BSC	
H	37.85 BSC		1.490 BSC	
J	6.78	7.06	0.267	0.278
K	5.85	7.62	0.230	0.300
L	25.15 BSC		0.990 BSC	
N	32.77 BSC		1.290 BSC	
P	0.21	0.30	0.008	0.012
Q	3.05	3.30	0.120	0.130
R	13.59	14.09	0.535	0.555
S	11.31	11.81	0.445	0.465
V	22.61 BSC		0.890 BSC	
W	7.24 BSC		0.285 BSC	
X	9.91 BSC		0.390 BSC	

STYLE 2:
PIN 1. RF INPUT
2. VSI
3. VCONT
4. VBIAS
5. VS2
6. RF OUTPUT
CASE:

CASE 301K-02

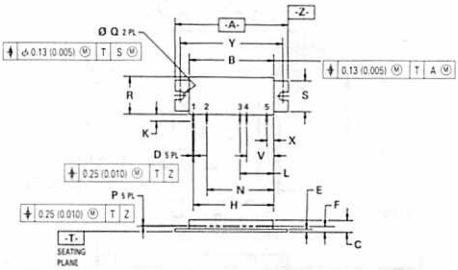




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	60.46	60.83	2.380	2.395
B	50.04	50.54	1.970	1.990
C	6.35	6.73	0.250	0.265
D	0.46	0.55	0.018	0.022
E	2.16	2.54	0.085	0.100
F	3.35 BSC		0.132 BSC	
G	57.40 BSC		2.260 BSC	
H	51.87 BSC		2.042 BSC	
J	6.78	7.06	0.267	0.278
K	4.49	5.51	0.177	0.217
L	29.01 BSC		1.142 BSC	
N	39.17 BSC		1.542 BSC	
P	0.21	0.30	0.008	0.012
Q	3.05	3.30	0.120	0.130
R	13.59	14.09	0.535	0.555
S	11.31	11.81	0.445	0.465
V	16.31 BSC		0.642 BSC	
X	8.60 BSC		0.342 BSC	

STYLE 2:
PIN 1. RF INPUT
2. VS1
3. VS2/V CONT
4. VS3
5. RF OUTPUT
CASE: GROUND

CASE 301L-02

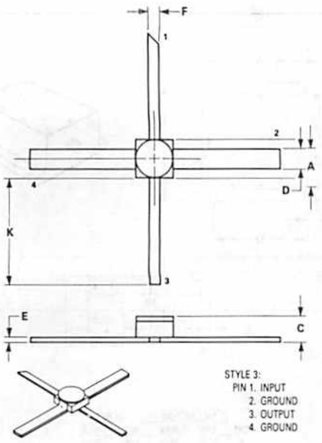


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	42.80	43.05	1.685	1.695
B	32.01	32.38	1.260	1.275
C	4.45	4.57	0.175	0.180
D	0.46	0.55	0.018	0.022
E	1.02	1.14	0.040	0.045
F	1.96	2.41	0.077	0.095
H	30.61 BSC		1.205 BSC	
K	2.54	—	0.100	—
L	12.83 BSC		0.505 BSC	
N	25.53 BSC		1.005 BSC	
P	0.21	0.30	0.008	0.012
Q	3.05	3.30	0.120	0.130
R	13.85	14.22	0.545	0.560
S	11.43	11.68	0.450	0.460
V	10.29 BSC		0.405 BSC	
X	2.67 BSC		0.105 BSC	
Y	38.99 BSC		1.535 BSC	

STYLE 1:
PIN 1. RF INPUT/V CONT
2. VS1
3. VS2
4. VS3
5. RF OUTPUT
CASE: GROUND

CASE 301N-01

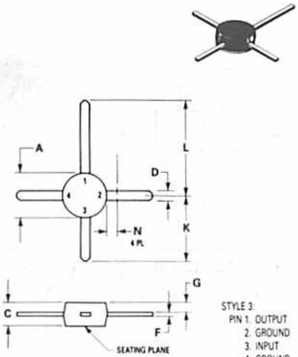
8



STYLE 3:
PIN 1. INPUT
2. GROUND
3. OUTPUT
4. GROUND

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	1.58	1.98	0.062	0.078
C	0.77	1.19	0.030	0.047
D	0.84	1.19	0.033	0.047
E	0.08	0.15	0.003	0.006
F	0.41	0.60	0.016	0.024
K	5.01	5.89	0.197	0.232

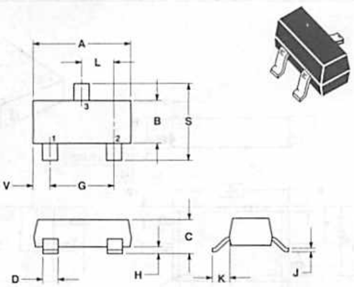
CASE 303A-01
(.070" CERAMIC)



STYLE 3:
PIN 1. OUTPUT
2. GROUND
3. INPUT
4. GROUND

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.44	5.21	0.175	0.205
C	1.90	2.54	0.075	0.100
D	0.84	0.99	0.033	0.039
F	0.20	0.30	0.008	0.012
G	0.76	1.14	0.030	0.045
K	7.24	8.13	0.285	0.320
L	10.54	11.43	0.415	0.450
N	—	1.65	—	0.065

CASE 317-01
(MACRO-X)



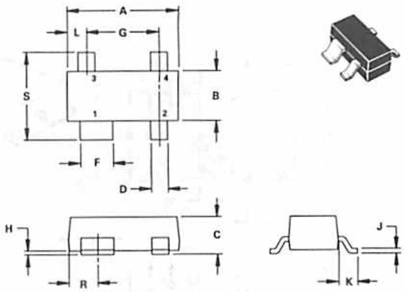
STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE-ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.89	1.11	0.0350	0.0440
D	0.37	0.50	0.0150	0.0200
G	1.78	2.04	0.0701	0.0807
H	0.013	0.100	0.0005	0.0040
J	0.085	0.177	0.0034	0.0070
K	0.45	0.60	0.0180	0.0236
L	0.89	1.02	0.0350	0.0401
S	2.10	2.50	0.0830	0.0984
V	0.45	0.60	0.0177	0.0236

CASE 318-07
LOW PROFILE
(TO-236AB)

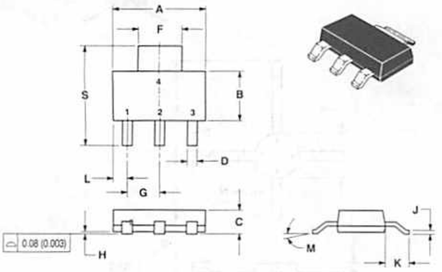


STYLE 4:
PIN 1. OUTPUT
2. GROUND
3. GROUND
4. INPUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.110	0.120
B	1.20	1.39	0.047	0.055
C	0.84	1.14	0.033	0.045
D	0.39	0.50	0.015	0.020
F	0.79	0.93	0.031	0.037
G	1.78	2.03	0.070	0.080
H	0.013	0.10	0.0005	0.004
J	0.08	0.15	0.003	0.006
K	0.46	0.60	0.018	0.024
L	0.445	0.60	0.0175	0.024
R	0.72	0.83	0.028	0.033
S	2.11	2.48	0.083	0.098

CASE 318A-05
LOW PROFILE
(SOT-143)

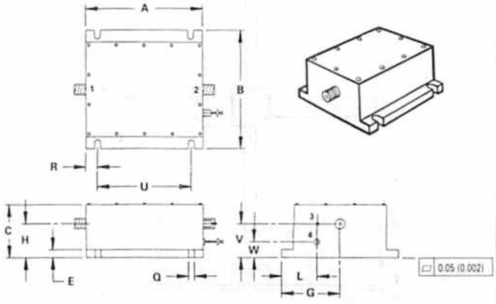
8



STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.30	6.70	0.249	0.263
B	3.30	3.70	0.130	0.145
C	1.50	1.75	0.060	0.068
D	0.60	0.89	0.024	0.035
F	2.90	3.20	0.115	0.126
G	2.20	2.40	0.087	0.094
H	0.020	0.100	0.0008	0.0040
J	0.24	0.35	0.009	0.014
K	1.50	2.00	0.060	0.078
L	0.85	1.05	0.033	0.041
M	0°	10°	0°	10°
S	6.70	7.30	0.264	0.287

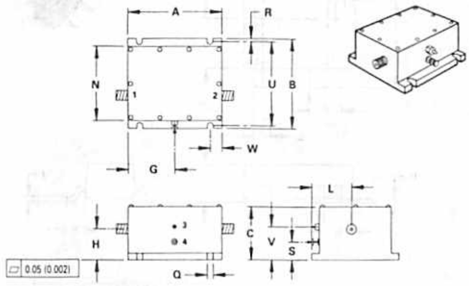
CASE 318E-04



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	75.82	76.58	2.985	3.015
B	74.55	75.31	2.935	2.965
C	33.28	34.03	1.310	1.340
E	4.83	5.33	0.190	0.210
G	37.22	37.72	1.465	1.485
H	20.83	21.33	0.820	0.840
L	22.61	23.11	0.890	0.910
Q	3.56	4.06	0.140	0.160
R	7.37	7.87	0.290	0.310
U	60.58	61.34	2.385	2.415
V	21.34	21.84	0.840	0.860
W	9.91	10.41	0.390	0.410

STYLE 1:
PIN 1. RF INPUT
2. RF OUTPUT
3. +28V
4. GROUND

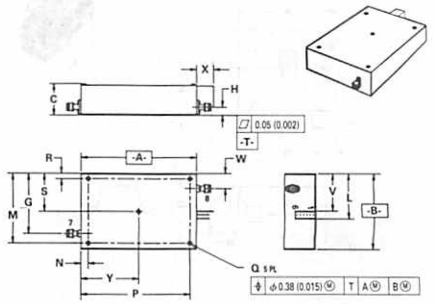
CASE 389-01
(DHP)



STYLE 1:
PIN 1. RF INPUT
2. RF OUTPUT
3. +28V
4. GROUND

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	60.71	61.21	2.390	2.410
B	56.90	57.40	2.240	2.260
C	33.41	33.90	1.315	1.335
G	30.23	30.73	1.190	1.210
H	19.56	19.68	0.770	0.775
L	20.71	21.20	0.815	0.835
N	41.53	42.29	1.635	1.665
Q	3.56	4.06	0.140	0.160
R	3.56	4.06	0.140	0.160
S	11.18	11.68	0.440	0.460
U	49.15	49.91	1.935	1.965
V	20.83	21.33	0.820	0.840
W	7.37	7.87	0.290	0.310

CASE 389A-01
(SHP)



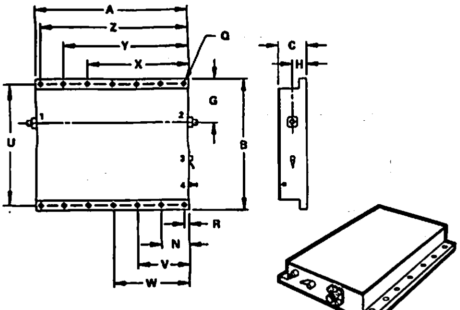
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	133.7	134.2	5.26	5.28
B	—	86.0	—	3.38
C	—	36.2	—	1.42
G	68.1	68.3	2.68	2.70
H	9.1	9.7	0.36	0.38
L	51.2	51.5	2.02	2.03
M	79.6 BSC		3.13 BSC	
N	8.5 BSC		0.33 BSC	
P	125.5 BSC		4.94 BSC	
Q	4.4	4.6	0.17	0.18
R	6.2 BSC		0.24 BSC	
S	35.2 BSC		1.38 BSC	
V	42.1	42.6	1.66	1.68
W	17.5	17.9	0.69	0.70
X	—	13.5	—	0.53
Y	67.0 BSC		2.64 BSC	

STYLE 1:
PIN 1. +V SUPPLY 26.5V
2. DO NOT USE
3. GROUND
4. TEST POINT (Ic1)
5. TEST POINT (Ic2)
6. OPTION
7. RF INPUT
8. RF OUTPUT

STYLE 2:
PIN 1. +V SUPPLY
2. FREE
3. GROUND
4. GROUND
5. GROUND
6. GROUND
7. RF INPUT
8. RF OUTPUT

CASE 389B-02
(ABC/ACR/AMR/ATV)

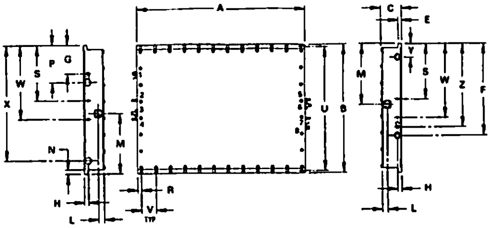
8



STYLE 1:
PIN 1. RF OUTPUT
2. RF INPUT
3. GROUND
4. DC POWER

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	159.01	159.51	6.260	6.280
B	134.37	134.87	5.290	5.310
C	29.04	30.04	1.143	1.183
G	34.04	34.54	1.340	1.360
H	14.61	15.11	0.575	0.595
N	28.96	29.46	1.140	1.160
Q	3.92	4.16	0.154	0.164
R	4.96	5.20	0.195	0.205
U	124.21	124.71	4.890	4.910
V	53.85	54.35	2.120	2.140
W	79.39	79.89	3.125	3.145
X	104.91	105.41	4.130	4.150
Y	129.80	130.30	5.110	5.130
Z	153.93	154.43	6.060	6.080

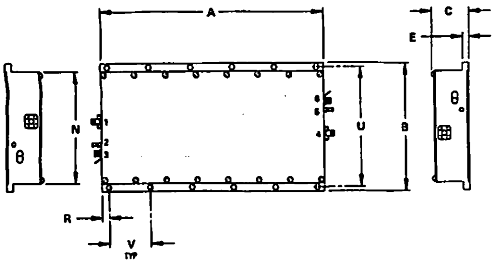
CASE 389C-01
(PAM)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	291.34	291.84	11.470	11.430
B	219.71	220.21	8.650	8.670
C	36.58	37.08	1.440	1.460
E	6.10	6.60	0.240	0.260
F	156.60	157.09	6.165	6.185
G	48.01	48.51	1.890	1.910
H	6.86	7.36	0.270	0.290
L	9.53	10.03	0.375	0.395
M	103.38	103.88	4.070	4.090
N	7.37	7.87	0.290	0.310
P	62.87	63.37	2.475	2.495
R	5.85	6.35	0.230	0.250
S	93.73	94.23	3.690	3.710
U	212.09	212.59	8.350	8.370
V	25.15	25.65	0.990	1.010
W	125.73	126.23	4.950	4.970
X	196.47	196.97	7.735	7.755
Y	22.99	23.49	0.905	0.925
Z	141.99	142.49	5.590	5.610

STYLE 1:
PIN 1. GROUND
2. DC IN
3. RF OUT
4. DC IN
5. DC IN
6. RF IN
7. DC IN
8. GROUND

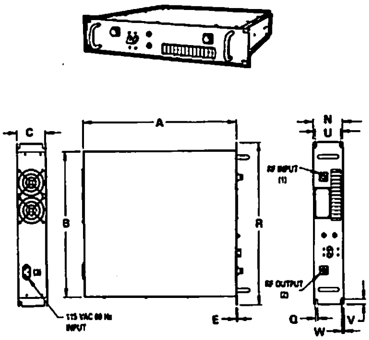
CASE 389D-01



STYLE 1:
PIN 1. RF IN
2. VDC
3. GROUND
4. RF OUT
5. VDC
6. GROUND

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	216.92	217.42	8.540	8.560
B	121.67	122.17	4.790	4.810
C	36.58	37.08	1.440	1.460
E	6.10	6.60	0.240	0.260
N	106.43	106.93	4.190	4.210
R	6.74	7.23	0.265	0.285
U	114.05	114.55	4.490	4.510
V	40.39	40.89	1.590	1.610

CASE 389E-01



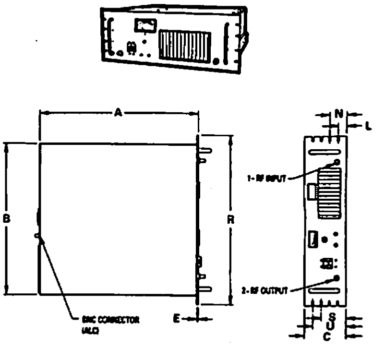
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	461.40	462.15	18.165	18.195
B	431.42	432.18	16.985	17.015
C	86.75	87.50	3.415	3.445
E	2.67	3.42	0.105	0.135
N	87.76	88.51	3.455	3.485
Q	6.23	6.98	0.245	0.275
R	482.22	482.98	18.985	19.015
U	75.82	76.58	2.985	3.015
V	14.86	15.62	0.585	0.615
W	5.47	6.22	0.215	0.245

STYLE 1:
PIN 1. RF INPUT
2. RF OUTPUT
3. AC INPUT

CASE 389F-01

8

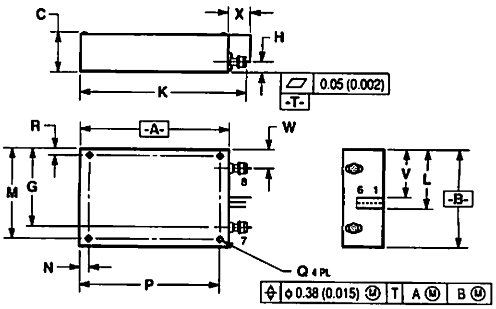
CASE DIMENSIONS (continued)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	521.72	524.76	20.54	20.66
B	549.91	552.45	21.65	21.75
C	220.22	221.49	8.67	8.77
E	2.80	5.33	0.11	0.21
L	36.33	38.86	1.43	1.53
N	80.78	83.31	3.18	3.28
R	608.33	610.87	23.95	24.05
S	137.93	140.46	5.43	5.53
U	182.33	184.91	7.18	7.28

STYLE 1:
PIN 1. RF INPUT
2. RF OUTPUT

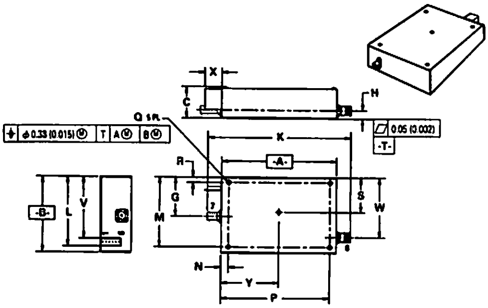
CASE 389G-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	133.7	134.2	5.26	5.28
B	—	86.0	—	3.39
C	—	36.2	—	1.42
G	67.9	68.2	2.67	2.68
H	9.1	9.7	0.36	0.38
K	—	146.5	—	5.77
L	53.5	54.3	2.11	2.14
M	79.6 BSC		3.13 BSC	
N	8.5 BSC		0.33 BSC	
P	125.5 BSC		4.94 BSC	
Q	4.4	4.6	0.17	0.18
R	6.2 BSC		0.24 BSC	
V	42.7	43.1	1.68	1.70
W	17.5	17.9	0.69	0.70
X	—	13.5	—	0.53

STYLE 1:
PIN 1. +V SUPPLY 25 V
2. FREE
3. GROUND
4. GROUND
5. GROUND
6. GROUND
7. RF INPUT
8. RF OUTPUT

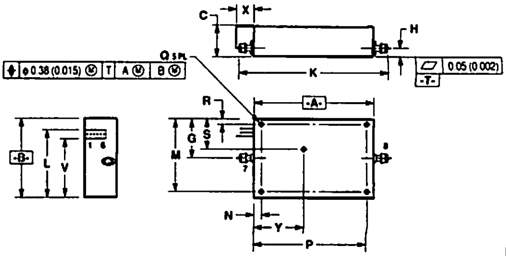
CASE 389J-02
(ACR)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	133.7	134.2	5.26	5.28
B	—	86.0	—	3.39
C	—	36.2	—	1.42
G	39.4	40.0	1.55	1.57
H	10.7	11.3	0.42	0.44
K	—	176.0	—	6.93
L	79.0	80.0	3.11	3.15
M	79.5 BSC		3.13 BSC	
N	8.5 BSC		0.33 BSC	
P	125.5 BSC		4.94 BSC	
Q	4.4	4.6	0.17	0.18
R	6.0 BSC		0.24 BSC	
S	35.0 BSC		1.38 BSC	
V	68.1	69.1	2.68	2.72
W				
X	—	13.5	—	0.53
Y	67.0 BSC		2.64 BSC	

STYLE 1:
PIN 1. + V SUPPLY
2. + V SUPPLY
3. TEST POINT Ic
4. DO NOT USE
5. GROUND
6. GROUND
7. RF INPUT
8. RF OUTPUT

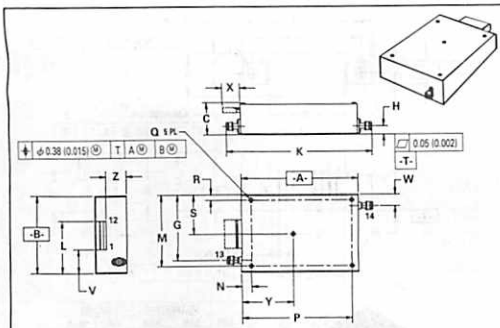
CASE 389K-01
(AMR)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	133.7	134.2	5.26	5.28
B	—	86.0	—	3.39
C	—	36.2	—	1.42
G	42.3	43.1	1.66	1.70
H	9.1	9.7	0.36	0.38
K	—	155.0	—	6.10
L	76.9	77.9	3.03	3.07
M	79.5 BSC		3.13 BSC	
N	8.5 BSC		0.33 BSC	
P	125.5 BSC		4.94 BSC	
Q	4.4	4.6	0.17	0.18
R	6.0 BSC		0.24 BSC	
S	37.9 BSC		1.49 BSC	
V	66.0	67.0	2.60	2.64
X	—	13.5	—	0.53
Y	54.6 BSC		2.15 BSC	

STYLE 1:
PIN 1. +V SUPPLY
2. +V SUPPLY
3. TEST POINT IC
4. DO NOT USE
5. GROUND
6. GROUND
7. RF INPUT
8. RF OUTPUT

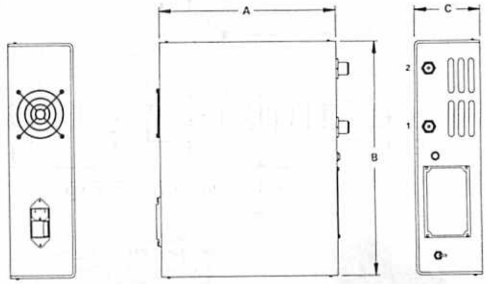
CASE 389L-02
(AMR)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	133.7	134.2	5.26	5.28
B	—	86.0	—	3.38
C	—	36.2	—	1.42
G	73.0	73.5	2.87	2.89
H	9.1	9.7	0.36	0.38
K	—	155.0	—	6.10
L	58.6	59.0	2.30	2.32
M	79.6 BSC		3.13 BSC	
N	20.5 BSC		0.81 BSC	
P	125.5 BSC		4.94 BSC	
Q	4.4	4.6	0.17	0.18
R	6.2 BSC		0.24 BSC	
S	42.9 BSC		1.69 BSC	
V	27.0	27.6	1.06	1.09
W	12.1	12.5	0.48	0.49
X	—	11.0	—	0.43
Y	62.0 BSC		2.44 BSC	
Z	25.8	26.6	1.02	1.05

STYLE:
PIN 1. $+V_{CC}$ 2
2. $+V_{CC}$ 2
3. $+V_{CC}$ 2
4. GROUND
5. GROUND
6. DETECTION −
7. DETECTION +
8. GROUND
9. GROUND
10. $+V_{CC}$ 1
11. $+V_{CC}$ 1
12. $+V_{CC}$ 1
13. RF INPUT
14. RF OUTPUT

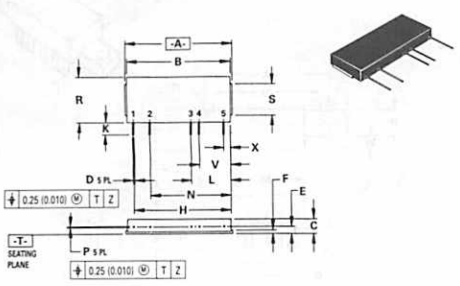
CASE 389N-01



STYLE 1:
PIN 1. RF INPUT
2. RF OUTPUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	228.6	231.1	9.00	9.10
B	298.4	301.0	11.75	11.85
C	85.1	87.6	3.35	3.45

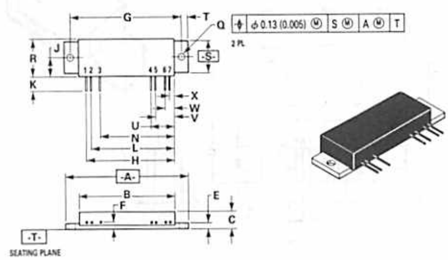
CASE 389R-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	32.77	33.14	1.290	1.305
B	32.01	32.38	1.260	1.275
C	4.45	4.57	0.175	0.180
D	0.46	0.55	0.018	0.022
E	1.02	1.14	0.040	0.045
F	1.96	2.41	0.077	0.095
H	30.61 BSC		1.205 BSC	
K	2.54	—	0.100	—
L	12.83 BSC		0.505 BSC	
N	25.53 BSC		1.005 BSC	
P	0.21	0.30	0.008	0.012
R	13.85	14.22	0.545	0.560
S	9.53	9.90	0.375	0.390
V	10.29 BSC		0.405 BSC	
X	2.67 BSC		0.105 BSC	

STYLE 1:
PIN 1. RF INPUT/V CONT
2. VS1
3. VS2
4. VS3
5. RF OUTPUT
CASE: GROUND

CASE 413-01



STYLE 1:
PIN 1. RF OUTPUT
2. GROUND
3. D.C. TERMINAL
4. GROUND
5. D.C. GAIN
6. GROUND
7. RF INPUT

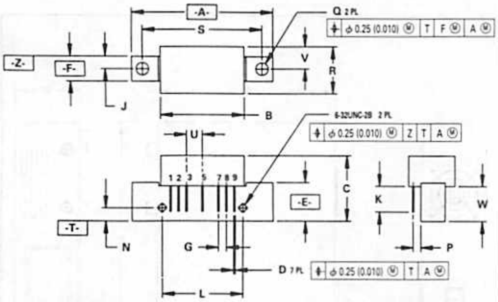
STYLE 2:
PIN 1. RF OUTPUT
2. GROUND
3. Vs 2
4. GROUND
5. Vs 1
6. GROUND
7. RF INPUT

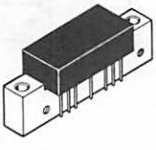
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	67.06	67.56	2.640	2.660
B	51.82	52.95	2.040	2.085
C	8.51	9.14	0.335	0.360
E	2.54	2.92	0.100	0.115
F	2.16	2.62	0.085	0.115
G	61.09 BSC		2.405 BSC	
H	47.88	48.64	1.885	1.915
J	10.16	11.18	0.400	0.440
K	5.85	7.62	0.230	0.300
L	45.34	46.10	1.785	1.815
N	40.26	41.02	1.585	1.615
Q	3.46	3.70	0.136	0.146
R	20.32	20.82	0.800	0.820
S	17.02	17.52	0.670	0.690
U	12.32	13.08	0.485	0.515
V	9.78	10.54	0.385	0.415
W	4.70	5.46	0.185	0.215
X	2.16	2.92	0.085	0.115

CASE 700-04

8

CASE DIMENSIONS (continued)

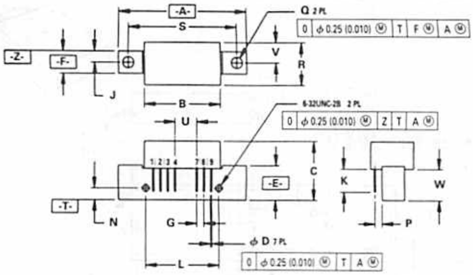


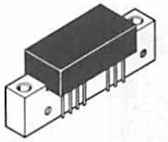


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.00 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	5.08 BSC		0.200 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. DELETED
5. VDC
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

CASE 714-04

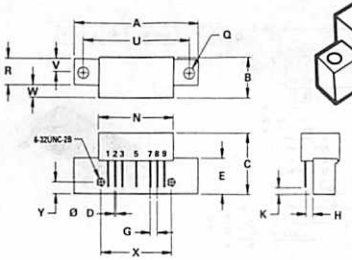


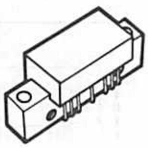


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	45.08	—	1.775
B	26.42	26.92	1.040	1.060
C	20.57	21.34	0.810	0.840
D	0.46	0.56	0.018	0.022
E	11.81	12.95	0.465	0.510
F	7.62	8.25	0.300	0.325
G	2.54 BSC		0.100 BSC	
J	3.96 BSC		0.156 BSC	
K	8.00	8.50	0.315	0.355
L	25.40 BSC		1.000 BSC	
N	4.19 BSC		0.165 BSC	
P	2.54 BSC		0.100 BSC	
Q	3.76	4.27	0.148	0.168
R	—	15.11	—	0.595
S	38.10 BSC		1.500 BSC	
U	7.62 BSC		0.300 BSC	
V	7.11 BSC		0.280 BSC	
W	11.05	11.43	0.435	0.450

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. VDC
5. DELETED
6. DELETED
7. GROUND
8. GROUND
9. RF OUTPUT

CASE 714C-04

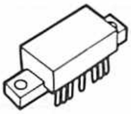


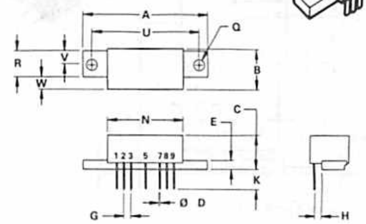


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	44.33	44.57	1.745	1.755
B	—	14.85	—	0.585
C	—	22.09	—	0.870
D	0.49	0.55	0.019	0.022
E	12.45	12.95	0.490	0.510
G	2.42	2.66	0.095	0.105
H	2.42	2.66	0.095	0.105
K	1.78	2.79	0.070	0.110
N	26.80	27.55	1.055	1.085
Q	3.76	5.33	0.148	0.210
R	7.75	8.25	0.305	0.325
U	37.85	38.35	1.490	1.510
V	3.87	4.14	0.152	0.163
W	4.20	4.44	0.165	0.175
X	25.15	25.65	0.990	1.010
y	4.07	4.31	0.160	0.170

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
5. $+V_{CC}$
7. GROUND
8. GROUND
9. RF OUTPUT

CASE 714F-01
(CA, POS. SUPPLY)

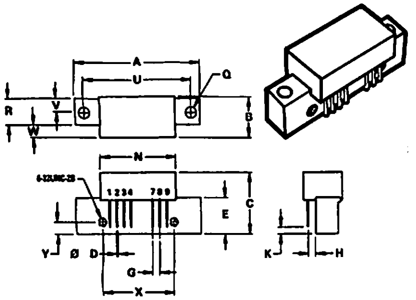




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	44.33	44.57	1.745	1.755
B	13.97	14.27	0.550	0.570
C	10.93	11.93	0.430	0.470
D	0.44	0.50	0.017	0.020
E	3.05	3.30	0.205	0.130
G	2.42	2.66	0.095	0.105
H	2.42	2.66	0.095	0.105
K	6.48	7.74	0.255	0.305
N	26.67	27.17	1.050	1.060
Q	3.81	4.06	0.150	0.160
R	7.88	8.12	0.310	0.320
U	37.85	38.35	1.490	1.510
V	3.94	4.06	0.155	0.160
W	4.07	4.57	0.160	0.180

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
5. $+V_{CC}$
7. GROUND
8. GROUND
9. RF OUTPUT

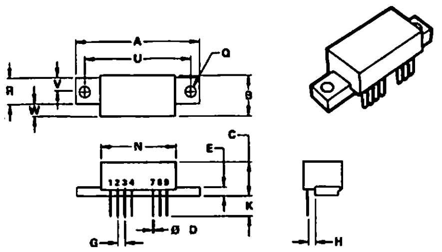
CASE 714G-01
(CA LP, POS. SUPPLY)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	44.33	44.57	1.745	1.755
B	—	14.85	—	0.585
C	—	22.09	—	0.870
D	0.49	0.55	0.019	0.022
E	12.45	12.95	0.490	0.510
G	2.42	2.66	0.095	0.105
H	2.42	2.66	0.095	0.105
K	1.78	2.79	0.070	0.110
N	26.80	27.55	1.055	1.085
Q	3.76	5.33	0.148	0.210
R	7.75	8.25	0.305	0.325
U	37.85	38.35	1.490	1.510
V	3.87	4.14	0.152	0.163
W	4.20	4.44	0.165	0.175
X	25.15	25.65	0.990	1.010
Y	4.07	4.31	0.160	0.170

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. $-V_{CC}$
7. GROUND
8. GROUND
9. RF OUTPUT

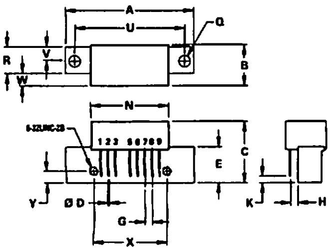
CASE 714H-01
(CA, NEG. SUPPLY)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	44.33	44.57	1.745	1.755
B	13.97	14.47	0.550	0.570
C	10.93	11.93	0.430	0.470
D	0.44	0.50	0.017	0.020
E	3.05	3.30	0.205	0.130
G	2.42	2.66	0.095	0.105
H	2.42	2.66	0.095	0.105
K	6.48	7.74	0.255	0.305
N	26.67	27.17	1.050	1.090
Q	3.81	4.06	0.150	0.160
R	7.88	8.12	0.310	0.320
U	37.85	38.35	1.490	1.510
V	3.94	4.06	0.155	0.160
W	4.07	4.57	0.160	0.180

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. $-V_{CC}$
7. GROUND
8. GROUND
9. RF OUTPUT

CASE 714L-01
(CA LP, NEG. SUPPLY)

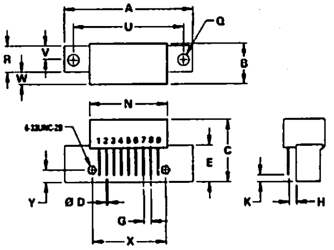


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	44.33	44.57	1.745	1.755
B	—	14.85	—	0.585
C	—	22.09	—	0.870
D	0.49	0.56	0.019	0.022
E	12.45	12.95	0.430	0.510
G	2.42	2.66	0.095	0.105
H	2.42	2.66	0.095	0.105
K	1.78	2.79	0.070	0.110
N	26.80	27.55	1.055	1.085
Q	3.76	5.33	0.148	0.210
R	7.75	8.25	0.305	0.325
U	37.85	38.35	1.490	1.510
V	3.87	4.14	0.152	0.163
W	4.20	4.44	0.165	0.175
X	25.15	25.65	0.990	1.010
Y	4.07	4.31	0.160	0.170

STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
5. V_{CC} 1
6. V_{CC} 2
7. GROUND
8. GROUND
9. RF OUTPUT

STYLE 2:
PIN 1. RF INPUT
2. GROUND
3. GROUND
5. V_{CC} 1
6. V_{CC} 2
7. GROUND
8. GROUND
9. RF OUTPUT, V_{CC} 3

CASE 714M-01



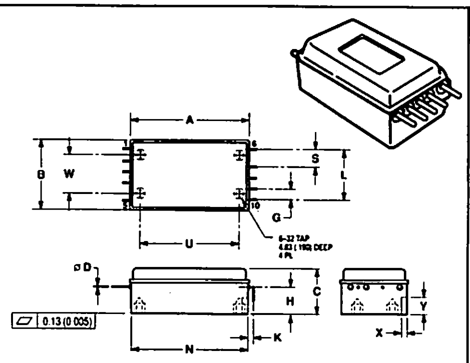
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	44.33	44.57	1.745	1.755
B	—	14.85	—	0.585
C	—	22.09	—	0.870
D	0.49	0.55	0.019	0.022
E	12.45	12.95	0.490	0.510
G	2.42	2.66	0.095	0.105
H	2.42	2.66	0.095	0.105
K	1.78	2.79	0.070	0.110
N	26.80	27.55	1.055	1.085
Q	3.76	5.33	0.148	0.210
R	7.75	8.25	0.305	0.325
U	37.85	38.35	1.490	1.510
V	3.87	4.14	0.152	0.163
W	4.20	4.44	0.165	0.175
X	25.15	25.65	0.990	1.010
Y	4.07	4.31	0.160	0.170

STYLE 2:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. RESISTOR-GROUND
5. GROUND
6. GROUND
7. GROUND
8. V_{CC} 1
9. RF OUTPUT

STYLE 3:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. V_{CC} 1
5. GROUND
6. GROUND
7. GROUND
8. V_{CC} 2
9. RF OUTPUT

CASE 714P-01

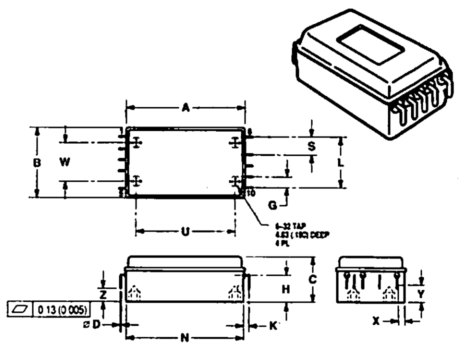
8



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	53.52	54.61	2.107	2.150
B	31.12	31.75	1.225	1.250
C	20.45	21.46	0.805	0.845
D	0.46	0.56	0.018	0.022
G	4.83	5.33	0.190	0.210
H	12.45	12.95	0.490	0.510
K	8.13	8.51	0.320	0.335
L	23.12	23.62	0.910	0.930
N	52.15	52.90	2.053	2.083
S	7.87	8.38	0.310	0.330
U	45.34	46.10	1.785	1.815
W	17.53	18.03	0.690	0.710
X	2.29	2.79	0.090	0.110
Y	7.37	7.87	0.290	0.310

STYLE 1
PIN 1 24 V
2 GROUND
3 INPUT
4 GROUND
5 TEST
6 TEST
7 GROUND
8 OUTPUT
9 GROUND
10 24 V

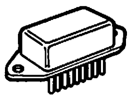
CASE 825-03
(FF)

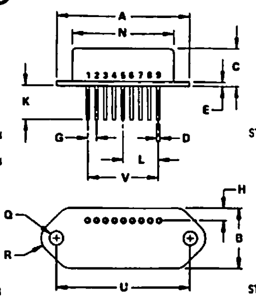


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	53.52	54.61	2.107	2.150
B	31.12	31.75	1.225	1.250
C	20.45	21.46	0.805	0.845
D	0.46	0.56	0.018	0.022
G	4.83	5.33	0.190	0.210
H	12.45	12.95	0.490	0.510
K	2.54	3.05	0.100	0.120
L	23.12	23.62	0.910	0.930
N	52.15	52.90	2.053	2.083
S	7.87	8.38	0.310	0.330
U	45.34	46.10	1.785	1.815
W	17.53	18.03	0.690	0.710
X	2.29	2.79	0.090	0.110
Y	7.37	7.87	0.290	0.310
Z	5.84	6.86	0.230	0.270

STYLE 1:
PIN 1 24 V
2 GROUND
3 INPUT
4 GROUND
5 TEST
6 TEST
7 GROUND
8 OUTPUT
9 GROUND
10 24 V

CASE 825A-02
(FF)





STYLE 1:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. NO CONNECTION
5. $+V_{CC}$
6. NO CONNECTION
7. GROUND
8. GROUND
9. RF OUTPUT

STYLE 2:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. $-V_{CC}$
5. NO CONNECTION
6. NO CONNECTION
7. GROUND
8. GROUND
9. RF OUTPUT

STYLE 3:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. NO CONNECTION
5. V_{CC} 1
6. V_{CC} 2
7. GROUND
8. GROUND
9. RF OUTPUT

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	46.39	47.39	1.826	1.866
B	17.02	17.52	0.670	0.690
C	9.91	11.04	0.390	0.435
D	0.44	0.48	0.017	0.019
E	1.02	1.27	0.040	0.050
G	2.42	2.66	0.095	0.105
H	3.31	3.81	0.130	0.150
K	9.28	9.77	0.365	0.385
L	9.91	10.41	0.390	0.410
N	26.95	27.45	1.061	1.081
Q	3.84	4.09	0.151	0.161
R	4.15	4.64	0.163	0.183
U	37.72	38.48	1.485	1.515
V	20.07	20.57	0.790	0.810

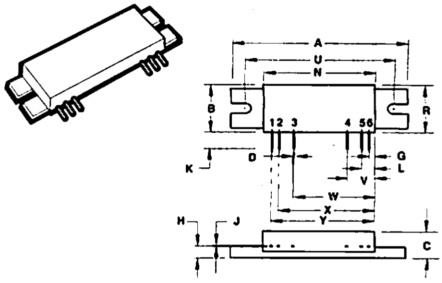
CASE 826-01
(SIP)

STYLE 4:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. NO CONNECTION
5. V_{CC} 1
6. V_{CC} 2
7. GROUND
8. GROUND
9. RF OUTPUT, V_{CC} 3

STYLE 5:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. V_{CC} 1
5. V_{CC} 2
6. V_{CC} 3
7. GROUND
8. GROUND
9. RF OUTPUT, V_{CC} 4

STYLE 6:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. RESISTOR-GROUND
5. GROUND
6. GROUND
7. GROUND
8. V_{CC} 1
9. RF OUTPUT

STYLE 7:
PIN 1. RF INPUT
2. GROUND
3. GROUND
4. V_{CC} 1
5. GROUND
6. GROUND
7. GROUND
8. V_{CC} 2
9. RF OUTPUT



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	66.91	67.10	2.634	2.642
B	19.99	20.19	0.787	0.795
C	8.89	9.09	0.350	0.358
D	0.56	0.76	0.022	0.030
G	2.44	2.64	0.096	0.104
H	4.17	4.36	0.164	0.172
J	0.23	0.27	0.009	0.011
K	6.41	6.60	0.252	0.260
L	4.98	5.18	0.196	0.204
N	52.41	52.60	2.063	2.071
Q	3.41	3.60	0.134	0.142
R	16.90	17.09	0.665	0.673
U	58.40	58.59	2.299	2.307
V	10.06	10.26	0.396	0.404
W	40.54	40.74	1.596	1.604
X	45.62	45.82	1.796	1.804
Y	48.16	48.36	1.896	1.904

STYLE 2
PIN 1. RF OUTPUT
2. GROUND
3. V_{CC} 2
4. V_{CC} 1
5. GROUND
6. RF INPUT

CASE 830-01
(MX)

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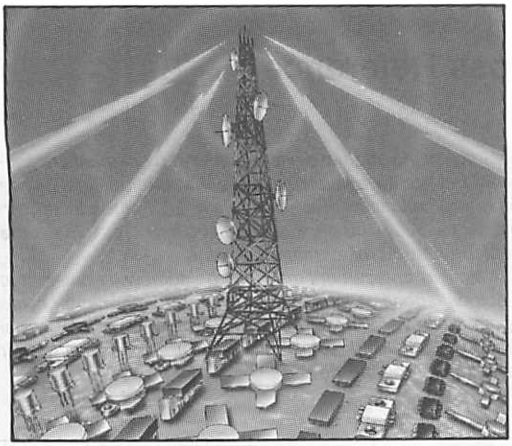

Volume II

Cross Reference and Sales Offices

9

Alphanumeric Cross Reference

Considerable judgment is necessary in creating a cross-reference for RF devices. The only real proof of a replacement is through direct substitution in a particular circuit or system. Guidelines used to compare low power parts were dc voltage ratings, cutoff frequency, current rating, junction capacitance and noise figure. For high power parts the parameters used were dc voltage ratings, output power, gain, frequency of operation and output capacitance.

A direct replacement will always be in a package that is the same as or for all practical purposes equivalent to the package of the original device. Similar replacement are generally but not always in packages that are identical or can be readily substituted; for example a .280" stud package in place of a .380" stud package or a 100 mil ceramic package in place of a 80 mil ceramic package.

A similar replacement may also be somewhat different in electrical specifications such as lower gain or higher noise figure. However, it is Motorola's closest device to the original and is considered sufficiently similar to warrant further investigation by the device user.

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page No.
4006		MRF464	2-654
40080		MRF476	2-666
40081		MRF476	2-666
40082		MRF475	2-662
40240	MRF501		2-690
40279		2N5641	2-64
40280	2N4427		2-23
40281		MRF485	2-678
40282		2N6081	2-100
40290	2N3553		2-8
40291		PT9734	2-1123
40292		PT9734	2-1123
40340		MRF342	2-581
40341		MRF497	2-687
40446		MRF475	2-662
40578	2N3866		2-10
40581		MRF475	2-662
40582		MRF475	2-662
40608	2N5943		2-83
40665		2N5641	2-64
40666		PT9734	2-1123
40893	2N5946		2-90
40894		2N5179	2-54
40895		2N5179	2-54
40896		2N5179	2-54
40897		2N5179	2-54
40915	2N5031		2-36
40934	TP2502		2-1162
40936		MRF401	2-601
40940	MRF5175		2-1028
40941		MRF313	2-531
40953	MRF207		1-7
40954	MRF212		1-6
40955	MRF1946A		2-1000
40964	MRF515		2-697
40965	MRF515		2-697
40967	2N5944		2-90
40968	2N5946		2-90
40970	MRF644		2-798
40971	MRF646		2-802

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page No.
40972	MRF607		2-784
40973	2N6081		2-100
40974	2N6082		2-103
40975	2N6083		2-106
40976	2N3553		2-8
40977	2N5642		2-67
41009	TP2502		2-1162
41010	2N5946		2-90
41024	2N5108		2-40
41025	MRF321		2-549
41026	MRF323		2-553
41027	MRF321		2-549
41028	MRF323		2-553
41038	MRF905		2-917
80091	MRF511		2-692
80099	MRF525		2-712
80167	MRF511		2-692
80231	MRF511		2-692
2C2857	2C2857		4-21
2C3866	2C3866		4-21
2C4957	2C4957		4-21
2C5108	2C5108		4-21
2C5160	2C5160		4-21
2C5883	2C5883		4-21
2C5943	2C5943		4-21
2N1491		MRF586	2-772
2N2631		2N3553	2-8
2N2857	2N2857		2-2
2N2876		2N5641	2-64
2N2947		MRF485	2-678
2N3118		MRF544	2-722
2N3119		MRF544	2-722
2N3296		2N5641	2-64
2N3309A		2N3553	2-8
2N3375		2N5641	2-64
2N3478		2N5179	2-54
2N3553	2N3553		2-8
2N3600	2N5179		2-54
2N3632		PT9734	2-1123
2N3733		PT9734	2-1123

ALPHANUMERIC CROSS REFERENCE (continued)

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page No.
2N3818		PT9734	2-1123
2N3866	2N3866		2-10
2N3866A	2N3866A		2-10
2N3880		2N5032	2-36
2N3924	2N3924		2-14
2N3925		2N5589	—
2N3926		MRF485	2-678
2N3927		2N6081	2-100
2N3948	2N3948		2-17
2N3950		MRF497	2-687
2N3959	2N3959		2-19
2N3960	2N3960		2-19
2N3961		2N5641	2-64
2N4012		2N5641	2-64
2N4040		MRF321	2-549
2N4041		MRF5174	2-1025
2N4072		MRF515	2-697
2N4073	2N4073		—
2N4127		2N5642	2-67
2N4128		2N5642	2-67
2N4130		MRF464	2-654
2N4416	2N4416		—
2N4427	2N4427		2-23
2N4428	2N4428		2-25
2N4440		MRF5175	2-1028
2N4932		2N6081	2-100
2N4933		MRF342	2-581
2N4957	2N4957		2-27
2N4958	2N4958		2-27
2N4959	2N4959		2-27
2N5016		MRF323	2-553
2N5031	2N5031		2-36
2N5032	2N5032		2-36
2N5053	2N6305		2-116
2N5054	2N6304		2-116
2N5070		MRF401	2-601
2N5071		MRF342	2-581
2N5090		MRF5174	2-1025
2N5102		MRF342	2-581
2N5108	2N5108		2-40
2N5109	2N5109		2-44
2N5160	2N5160		2-50
2N5161		2N6096	—
2N5162		2N6096	—
2N5179	2N5179		2-54
2N5180	2N5179		2-54
2N5262	MRF544		2-722
2N5421	2N4427		2-23
2N5422	MRF607		2-784
2N5423		MRF261	2-519
2N5424		2N6081	2-100
2N5583	2N5583		2-60
2N5589	2N5589		—
2N5590	2N5590		—
2N5591	2N5591		—
2N5635		MRF5174	2-1025
2N5636		MRF321	2-549
2N5637		MRF323	2-553
2N5641	2N5641		2-64
2N5642	2N5642		2-67

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page No.
2N5643	2N5643		2-70
2N5644		2N5944	2-90
2N5645		MRF652	2-816
2N5646		MRF653	2-820
2N5687	MRF607		2-784
2N5688		2N6081	2-100
2N5689		2N6081	2-100
2N5690		MRF234	2-502
2N5691		MRF450A	2-79
2N5697	MRF515		2-697
2N5698		2N5944	2-90
2N5699		2N5945	2-90
2N5710	2N4073		—
2N5711		2N5641	2-64
2N5712		2N5642	2-67
2N5713		2N5643	2-70
2N5773		MRF5174	2-1025
2N5774		MRF321	2-549
2N5775		MRF325	2-557
2N5829		2N4957	2-27
2N5834	2N3553		2-8
2N5835	2N5835		2-73
2N5836	2N5836		2-73
2N5837	2N5837		2-73
2N5841		MRF914	2-922
2N5842		MRF914	2-922
2N5846		MRF433	2-640
2N5847		MRF232	2-674
2N5848	MRF234		2-502
2N5849	2N5849		2-79
2N5862	2N5862		—
2N5913	MRF607		2-784
2N5914		2N5944	2-90
2N5915		2N5946	2-90
2N5916		MRF5174	2-1025
2N5917		MRF5174	2-1025
2N5918		MRF321	2-549
2N5919A		MRF323	2-553
2N5941	MRF466		2-658
2N5942		MRF464	2-654
2N5943	2N5943		2-83
2N5944	2N5944		2-90
2N5945	2N5945		2-90
2N5946	2N5946		2-90
2N5947	MRF511		2-692
2N5992		MRF232	2-494
2N5993		MRF234	2-502
2N5994		MRF315	2-537
2N5995		MRF212	1-6
2N5996		2N5591	—
2N6080	2N6080		2-97
2N6081	2N6081		2-100
2N6082	2N6082		2-103
2N6083	2N6083		2-106
2N6084	2N6084		2-109
2N6093		MRF464	2-654
2N6094	2N6094		—
2N6095	2N6095		—
2N6096	2N6096		—
2N6097	2N6097		—

ALPHANUMERIC CROSS REFERENCE (continued)

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page No.
2N6104		MRF325	2-557
2N6105		MRF325	2-557
2N6136		MRF644	2-798
2N6166	2N6166		2-112
2N6197	2N5641		2-64
2N6198	2N5642		2-67
2N6199	2N5643		2-70
2N6200		2N5643	2-70
2N6201		2N6166	2-112
2N6202		MRF5174	2-1025
2N6203		MRF321	2-549
2N6204		MRF323	2-553
2N6205		MRF325	2-557
2N6206		MRF891	2-891
2N6207		MRF892	2-895
2N6255		MRF237	2-506
2N6256		MRF559	2-747
2N6304	2N6304		2-116
2N6305	2N6305		2-116
2N6366		2N6080	2-97
2N6367		MRF433	2-640
2N6368		MRF455	2-652
2N6370	MRF410		2-608
2N6439	2N6439		2-121
2N6455	2N6082		2-103
2N6456	MRF450A		2-648
2N6457		MRF492	2-684
2N6458	MRF406		2-604
2N6459	MRF450		2-648
2N6460	MRF492		6-684
2N6603	2N6603		2-125
2N6604	2N6604		2-129
2N6618	2N6618		2-133
2N6679	2N6679		2-135
2N6985	2N6985		2-137
2N6986	2N6986		2-141
2SA1161		MM4049	2-216
2SA1223		MRF536	2-216
2SA1228	MM4049		2-216
2SA1230		MRF536	2-216
2SA1245	MMBR4957L		2-231
2SA711	2N3959		2-19
2SA800	MM4049		2-216
2SC1043	MRF587		2-772
2SC1044	2N6304		2-116
2SC1081		MRF654	2-824
2SC1090-1		2N6604	2-129
2SC1119		MRF901	2-907
2SC1239		MRF475	2-662
2SC1251		MRF587	2-772
2SC1252		MRF586	2-772
2SC1253		MRF586	2-772
2SC1254	2N6304		2-116
2SC1256		MRF237	2-506
2SC1257		2N6081	2-100
2SC1258	2N6081		2-100
2SC1259		2N6083	2-106
2SC1260	2N2857		2-2
2SC1268		MRF572	2-754
2SC1275	2N2857		2-2
2SC1297		2N5643	2-70
2SC1298		MRF315A	2-537
2SC1306		MRF485	2-678
2SC1307	MRF485		2-678
2SC1329	2N5849		2-79
2SC1336		MRF572	2-754
2SC1365	MRF586		2-772
2SC1366	MRF586		2-772
2SC1424	MRF914		2-922
2SC1426		MRF965	2-153
2SC1560		MRF572	2-754
2SC1589		MRF260	2-515
2SC1590		MRF262	2-523
2SC1591		MRF262	2-523
2SC1592		MRF587	2-772
2SC1593		MRF587	2-772
2SC1594		MRF587	2-772
2SC1600		MRF586	2-772
2SC1603		MRF752	2-836
2SC1604		MRF750	2-832
2SC1605A		MRF2628	2-1009
2SC1606		2N6080	2-97
2SC1678	MRF476		2-666
2SC1689		MRF315A	2-537
2SC1729		MRF2628	2-1009
2SC1763		MRF464	2-654
2SC1764	MRF464		2-654
2SC1804		MRF321	2-549
2SC1805		MRF323	2-553
2SC1807		BFY90	2-166
2SC1808		MRF652	2-816
2SC1945	MRF479		2-674
2SC1946		MRF1946	2-1000
2SC1946A		MRF1946A	2-1000
2SC1947	MRF237		2-506
2SC1949		MRF962	2-153
2SC1955	MRF237		2-506
2SC1966		2N5945	2-90
2SC1967		2N5946	2-90
2SC1968A		MRF641	2-794
2SC1969	MRF475		2-662
2SC1970		MRF553	2-733
2SC1971	MRF260		2-515
2SC1972	MRF262		2-523
2SC1988	MRF914		2-922
2SC2025		MRF965	2-153
2SC2026	MPS911		2-251
2SC2040	MRF587		2-772
2SC2065		MRF587	2-772
2SC2075	MRF476		2-666
2SC2081	2N5944		2-90
2SC2082		2N5946	2-90
2SC2083		MRF654	2-824
2SC2098	MRF475		2-662
2SC2099	MRF406		2-604
2SC2100	MRF492		6-684
2SC2101		2N6081	2-100
2SC2102	MRF2628		2-1009
2SC2103A	MRF1946A		2-1000
2SC2104		MRF652	2-816

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page No.
2SC2105		MRF653	2-820
2SC2106		MRF654	2-824
2SC2131	MRF629		1-9
2SC2132		MRF646	2-802
2SC2148		2N6604	2-129
2SC2149		MRF572	2-754
2SC2174	MRF572		2-754
2SC2178		MRF221	2-100
2SC2181	MRF224		2-109
2SC2207	MRF475		2-662
2SC2217		MRF572	2-754
2SC2218		MRF572	2-754
2SC2222		2N5946	2-90
2SC2280		2N5944	2-90
2SC2281		2N5946	2-90
2SC2282	MRF2628		2-1009
2SC2290	MRF454		2-650
2SC2329		MRF607	2-784
2SC2350	MRF911		2-919
2SC2351	MMBR571L		2-241
2SC2367		MRF572	2-754
2SC2369	MRF2369		2-1004
2SC2395	MRF433		2-640
2SC2420	MRF1946		2-1000
2SC2494K		MRF750	2-832
2SC2494M		MRF750	2-832
2SC2495K		MRF752	2-836
2SC2495M		MRF752	2-836
2SC2496A		MRF646	2-802
2SC2498	MPS911		2-251
2SC2499	MPS901		2-247
2SC2508	MRF1946		2-1000
2SC2509	MRF479		2-674
2SC2510	MRF422		2-616
2SC2570	MPS571		2-241
2SC2586	MRF629		1-9
2SC2627		2N6080	2-97
2SC2628		MRF2628	2-1009
2SC2629		MRF1946A	2-1000
2SC2630		MRF247	2-512
2SC2642		MRF641	2-794
2SC2643		MRF644	2-798
2SC2652		MRF448	2-642
2SC2694	MRF247		2-512
2SC2753	MPS571		2-241
2SC2759	MMBR911L		2-251
2SC2782	MRF247		2-512
2SC2783	MRF646		2-802
2SC2876		MRF571	2-754
2SC2879	MRF421		2-612
2SC2886		MRF321	2-549
2SC2887		MRF321	2-549
2SC2888		MRF314A	2-533
2SC2889		MRF315A	2-537
2SC2890		MRF316	2-541
2SC2891	MRF317		2-545
2SC2892	MRF5174		2-1025
2SC2893	MRF321		2-549
2SC2894		MRF323	2-553
2SC2895	MRF325		2-557
2SC2896	2N6439		2-121
2SC2897	MRF327		2-565
2SC2905		MRF646	2-802
2SC2906AK		MRF754	2-840
2SC2906AM		MRF754	2-840
2SC2915	MRF648		2-806
2SC2917	MRF247		2-512
2SC2931		MRF557	2-742
2SC2932		MRF840	2-859
2SC2933		MRF842	2-869
2SC2946A		MRF646	2-802
2SC2952		MRF586	2-772
2SC2953		MRF587	2-772
2SC2954		MRFQ19	2-1065
2SC3011		MMBR901L	2-225
2SC3019	MRF559		2-747
2SC3020		MRF652	2-816
2SC3021		MRF653	2-820
2SC3022		MRF644	2-798
2SC3099	MMBR901L		2-225
2SC3101	MRF630		2-790
2SC3102		MRF648	2-806
2SC3103		MRF752	2-836
2SC3104		MRF754	2-840
2SC3105		MRF844	2-873
2SC3120		MMBR911L	2-251
2SC3133	MRF479		2-674
2SC3139		MRF890	2-887
2SC3147		MRF247	2-512
2SC319	2N4427		2-23
2SC320	MRF607		2-784
2SC3268		MRF5711L	2-1033
2SC3282	MRF842		2-869
2SC3283	MRF844		2-873
2SC3301		MRF5711L	2-1033
2SC3302	MRF571		2-754
2SC3355		MPS571	2-241
2SC3356		MMBR571L	2-241
2SC3358		MRF572	2-754
2SC3429	MMBR571L		2-241
2SC3445		MMBR571L	2-241
2SC3484		MRF571	2-754
2SC3582		MPS571	2-241
2SC3583		MMBR571L	2-241
2SC3604		MRF572	2-754
2SC3660A		TPV8200B	2-1339
2SC567	MRF502		2-690
2SC568	MRF501		2-690
2SC571	2N3924		2-14
2SC572		MRF485	2-678
2SC573		2N6081	2-100
2SC585		PT9734	2-1123
2SC597	2N3553		2-8
2SC598		MRF5175	2-1028
2SC600		PT9734	2-1123
2SC628	MRF607		2-784
2SC635		2N5641	2-64
2SC636		PT9734	2-1123
2SC637		MRF485	2-678
2SC638		2N6081	2-100

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page No.
2SC651	2N4428		2-25
2SC652		2N4428	2-25
2SC730	2N4427		2-23
2SC821		2N4427	2-23
2SC822	2N4427		2-23
2SC823		2N5109	2-44
2SC824		2N5943	2-83
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MRF525	MRF525		2-712
MRF526		MRF586	2-772
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MRF543	MRF543		2-720
MRF544	MRF544		2-722
MRF545	MRF545		2-725
MRF546	MRF546		2-729
MRF547	MRF547		2-731
MRF548	MRF548		2-718
MRF549	MRF549		2-720
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MRF555	MRF555		2-738
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MRF873	MRF873		2-883
MRF890	MRF890		2-887
MRF891	MRF891		2-891
MRF892	MRF892		2-895
MRF894	MRF894		2-899
MRF898	MRF898		2-903
MRF901	MRF901		2-907
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MRF9011L	MRF9011L		2-1047
MRF902	2N6603		2-125
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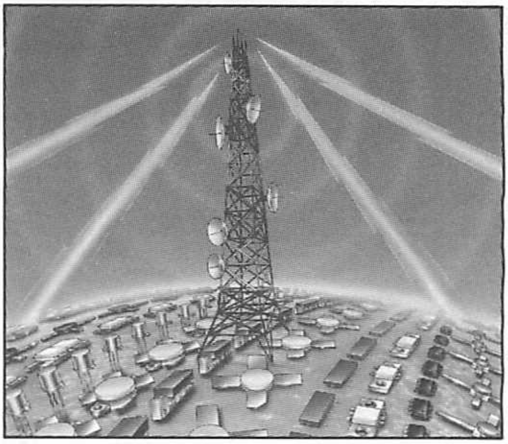

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