SECTION 2.
SYSTEM THEORY OF OPERATION

2.1 GENERAL

The Communications System Analyzer can perform nine basic functions: it can act as a generator, a wattmeter, a monitor, a duplex generator, a code synthesizer, a frequency counter, a digital voltmeter (DVM), an oscilloscope, and a distortion/SINAD meter. General operation of the unit will simultaneously incorporate all these functions.

The following discussion will cover the block diagrams for each of the basic functions plus a discussion on the processor control of the system. A functional block diagram of the total system is shown at the end of the section in Figure 2-1. To clarify the total system configuration, only the major signal paths between each of the modules are shown.

2.2 SYSTEM CONTROL

2.2.1 PROCESSOR

System control is the primary responsibility of the internal microprocessor. To control the operating mode, the processor manipulates inputs from front-panel controls and system-status inputs. From the front panel, the processor monitors the keyboards, the function-select switch, the modulation-control switch, the RF-scan switch, the image switch, the bandwidth switch, the horizontal and vertical range switches, and the step-attenuator switch. This information, plus internal status information, causes the processor to display the appropriate information on the CRT, to program the center frequency, to set up the generate or monitor mode, and to make the internal switching arrangements for the selected operating state.

2.2.2 PROCESSOR BUS

The interface to and from the microprocessor is via the processor bus. This bus consists of a 16-bit address bus, an 8-bit data bus, and a 7-bit control bus. The bus interfaces the processor to its program memory (ROM), scratch pad memory (RAM), IEEE interface option, cellular mobile telephone option, and the peripheral-interface adapters (PIA). The PIA is the mechanism by which the processor interfaces with the system. A PIA consists of a dual 8-bit latch which may be programmed as either an input or an output for the microprocessor. System input and control information passes to and from the microprocessor via three system control busses attached to a PIA, which is located on the Processor Interface board (A11).

2.2.3 CONTROL BUSSES

The three control busses within the System Analyzer are called the RF control bus and AF control busses 1 and 2. The AF control busses consist of a 4-bit address bus, a 4-bit data bus, and two enable lines. The four address bits determine which of 16 possible latches the four bits of data are to be sent to or received from. The enable lines trigger the actual transfer of data. The RF control bus is a clocked serial bus which consists of five data lines, a clock line, and a latch line. The serial data stream is 24 bits long. Tables 2-1 through 2-6 show the busses and the function of each bit. Figure 2-2 at the end of the section shows the overall bus structure of the System Analyzer.

Table 2-1. AF BUS Control

DATA ADRS	AF BUS #1 D3	AF BUS #1 D2	AF BUS #1 D1	AF BUS #1 D0	AF BUS #2 D3	AF BUS #2 D2	AF BUS #2 D1	AF BUS #2 D0
0	AUDIO SYNTH BITS 0-3				Display LEDs			
1	AUDIO SYNTH BITS 7-4				Function LEDs			
2	AUDIO SYNTH BITS 11-8				Mode LEDs			
3	AUDIO SYNTH BITS 15-12				INPUT SCOPE ATTENUATION			
					0.001	0.01	0.1	1.0
4	PL SELECT	DPL CLOCK ENABLE	DPL SELECT	AUDIO SYNTH BIT 16	(MON +DSB) /GEN SELECT	$\overline{\text{OFFSET}}$ $\overline{\text{ATTEN}}$ ENABLE	ATTEN INT/EXT SELECT	EXT IN AC/DC SELECT
5	MOD TO SPEAKER ENABLE	AUDIO ATTEN 30 dB	AUDIO SYNTH BIT 17	AUDIO ATTEN 10 dB	RF ATTENUATOR POSITION			
6	DPLX MOD ENABLE	DSBSC MOD ENABLE	FM MOD ENABLE	AM MOD ENABLE	RF OVER TEMP	$\overline{\text{WB SIG}}$ $\overline{\text{PRESENT}}$	ANT SELECT	SPARE INPUT
7	BINARY MOD ENABLE				$\overline{\text{IF}}$ $\overline{\text{OVERLOAD}}$	SIGNAL PRESENT	OFFSET ON/OFF	WB/NB
8	DVM MODE SELECT				$\overline{\text{CSSG}}$ $\overline{\text{CONT}}$ $\overline{\text{EN}}$	$\overline{\text{CSSG}}$ $\overline{\text{BURST}}$ $\overline{\text{EN}}$	IMAGE HI/LO	MON/GEN
	SIGNAL STRENGTH	DV2	DV1	DV0				
9	SCOPE TRIGGER ENABLE	PK DET FM MOD ENABLE	PK DET AM MOD ENABLE	PK DET DEMOD ENABLE	SCOPE VERTICAL SWITCH POSITION			
					$\overline{\text{10V/DIV}}$	$\overline{\text{1V or 25 kHz/ DIV}}$	$\overline{\text{0.1V or 2.5 kHz/ DIV}}$	$\overline{\text{0.01V or 0.25 kHz/DIV}}$
A	DIST NOTCH FILTER X1/×10	INT DVM ×0.1 ENABLE	WB/NB SELECT	ALARM ENABLE	SPARE INPUT	SCOPE HORIZONTAL SWITCH POSITION		
B	HORIZ SCOPE MODE SELECT		VERT SCOPE MODE SELECT					
C	ANTENNA ENABLE	MOD TO SCOPE DISABLE	EXT/ DISTORTION SELECT	0.01-1/ 1-10 SWEEP SELECT				
D		SCOPE TIME BASE CONTROL			PERIOD/ FREQ SELECT	COUNTER/ DVM SELECT	SPARE OUTPUT	SPARE OUTPUT
		C2	C1	C0				
E					DVM RMS/DIR SELECT	COUNTER RANGE		
F						COUNTER INPUT SELECT		
						IF/BFO		EXTERNAL

Table 2-2. RF BUS Control

BIT	CONWD1	CONWD2	CONWD3	CONWD4*	CONWD5
0				0.5-1 GHz EN	
1				GHz LOOP SENSE	
2				VCO SELECT	
3				300-350 CLAMP	
4				350-500 MHz EN	
5	MOD CONT A	MOD ×2/×1	MOD SENSE	0.01-250 MHz EN	SW1
6	MOD CONT B	BW CONT	MOD CONT C	250-350 MHz EN	SW2
7	÷N MSB	÷N MSB	÷N MSB	WB AMP HI/LO	÷N MSB
8	↑	↑	↑	R0 $\overline{\text{AM/FM/CW CRT EN}}$	↑
9				R1 $\overline{\text{WB DET EN}}$	
10	24 MHz	60 MHz	310-440 MHz	R2 $\overline{\text{NBFM GAIN ×10}}$	DUPLEX
11	LOOP	LOOP	LOOP	R3 SPARE	GENERATOR
12	CONTROL	CONTROL	CONTROL	R4 $\overline{\text{SPARE}}$	CONTROL
13				R5 $\overline{\text{SPKR EN}}$	
14				R6 $\overline{\text{BIT 12}}$	
15	↓	↓	↓	R7 DEMOD INV	↓
16	÷N LSB	÷N LSB	÷N LSB	R8 $\overline{\text{WB/NB}}$	÷N LSB
17	÷A MSB	÷A MSB	÷A MSB	R9 $\overline{\text{LPFL 300}}$	÷A MSB
18	↑	↑	↑	R10 $\overline{\text{LPFL 3K}}$	↑
19				R11 $\overline{\text{HPFL 3K}}$	
20				R12 $\overline{\text{HPFL 300}}$	
21				R13 $\overline{\text{AM EN}}$	
22				R14 $\overline{\text{FM EN}}$	
23	÷A LSB	÷A LSB	÷A LSB	R15 $\overline{\text{SSB EN}}$	÷A LSB

*Note: Functions with bar over top are active low.
Bits 0-7 of CONWD4 are RF Synthesizer control bits.
Bits 8-23 of CONWD4 are Receiver control bits.

Table 2-3. MOD Control

A	B	C	BW CONT	Function
0	0	0	0	SWEEP
0	1	1	0	NARROW MOD
1	0	1	0	WIDE MOD
1	1	1	1	MOD INHIBIT

Table 2-4. Receiver Control

R0	R1	R2	R8	R13	R14	R15	Function
0	1	1	1	0	1	1	AM WB
0	1	1	0	0	1	1	AM NB
0	1	1	1	1	1	0	CW/SSB WB
0	1	1	0	1	1	0	CW/SSB NB
0	1	1	1	1	0	1	FM WB
0	1	0	0	1	0	1	FM NB
0	0	X	X	1	1	1	WB DET

Table 2-5. Duplex Control

SW1	SW2	Function
0	0	0-10 MHz
1	0	45 MHz
1	1	OFF

Table 2-6. Receiver Filters

Low-Pass			High-Pass			
R9	R10	FREQ	R6	R11	R12	FREQ
0	1	300 Hz	0	1	1	5 Hz
1	0	3 kHz	1	1	0	300 Hz
1	1	20 kHz	1	0	0	3 kHz

2.2.4 IEEE BUS

Systems with the IEEE remote-control option interface the IEEE bus through a general purpose interface bus (GPIB) adapter on the IEEE Interface board (A13). When enabled, all control inputs to the system pass through the IEEE bus, and the front panel's controls are ignored.

2.3 GENERATE MODE

2.3.1 GENERAL

The generate mode provides a variable-level RF output that is phase-locked to the internal 10-MHz standard. AM, FM, and sideband modulation is possible on the output signal.

A block diagram of the generate mode is shown at the end of the section in Figure 2-3.

2.3.2 FREQUENCY STANDARD

To provide a 10-MHz signal to the EXTERNAL 10 MHz OUTPUT and to the RF Synthesizer module (A9), the Frequency-Standard Interface board (A16) contains a 10-MHz crystal oscillator with buffering and switching. An external 10-MHz standard signal can be used by switching the IN/OUT switch on the bottom panel to IN. The signal applied to the 10-MHz STD input/output port on the back is then routed through the A16 board to the A9 module.

2.3.3 RF SYNTHESIZER

The RF Synthesizer uses the 10-MHz standard signal for its phase-locked-loop reference frequencies and also converts the 10-MHz standard signal to a TTL level for system use. The RF Synthesizer consists of a fixed 640-MHz loop and a programmable GHz loop. The programming of the GHz loop is provided by the RF CONTROL BUS from the processor. The Synthesizer Output board chooses one of three possible outputs for the SYNTH RF output signal. The first is directly from the GHz loop. The second is the output of the divide-by-two on the GHz loop, which provides frequencies from 250 to 500 MHz. For outputs below 250 MHz, the output of the GHz loop is mixed with the fixed 640-MHz signal, and the difference signal is used for the output. To obtain outputs from 10 kHz to 250 MHz, the processor programs the GHz loop for frequencies between 640.01 and 890 MHz, respectively.

FM and sweep modulation is also implemented in the GHz loop by modulating its 60.5 MHz reference. The Audio Synthesizer board (A10) supplies the FM modulation signal, which provides modulation frequencies from 5 Hz to 20 kHz. FM capability is 100 kHz peak deviation. The Scope/DVM Control board (A7) supplies the sweep-modulation signal. The sweep capability, 10 MHz, is used for both the sweep-generator and the spectrum-analyzer functions.

2.3.4 WIDEBAND AMPLIFIER

The SYNTH RF signal is amplified and leveled in the RF Input module (A17) by the Wideband Amplifier (A17A2). The signal level at the output of the Wideband Amplifier is detected and compared to the AM MOD + DC REF signal from the front panel's level control. If there is a difference between the two signal levels, the ALC amplifier provides an error voltage. This error voltage controls the attenuation of the voltage-controlled attenuator (VCA) in the direction that will make the detected RF output equal to the AM MOD + DC REF signal. There are two possible VCAs for the output leveling. The VCA on the Wideband Amplifier board is used for frequencies from 1 to 1000 MHz. For frequencies below 1 MHz, the VCA on the Processor Interface board (A11) is set to minimum attenuation, and the VCA on the RF Synthesizer module (A9) does the leveling. Amplitude modulation is incorporated by summing the modulation signal with the dc reference signal, thus forcing the leveling loop to vary the output level in proportion to the modulating signal. The signal from the RF-level detector (CARRIER + MOD LVL) is used by the processor to determine the RF output level and the percent AM. The leveled output range of the Wideband Amplifier is from −3 dBm to +13 dBm (0.16 to 1.0 Vrms).

The leveled output from the Wideband Amplifier is applied to the Generate/Monitor switch. For generating AM, FM, and CW signals, the switch connects the Amplifier output to the step attenuator. For double sideband-suppressed carrier (DSBSC) generation, the Wideband Amplifier output is connected to the local-oscillator (L.O.) port on the receive mixer, and the attenuator is connected to the RF port. The DSBSC modulation signal then drives the IF port of the mixer, giving a DSBSC signal at the RF port and thus at the step attenuator. For monitor mode, the Wideband Amplifier output is connected to the L.O. port on the receive mixer, and the attenuator is connected to the RF port. The difference-frequency output of the receive mixer is sent to the Receiver board through the 10.7 MHz IF output.

2.3.5 STEP ATTENUATOR

Level control in 10-dB increments is provided by the step attenuator. The total range of the attenuator is from 0 to 130 dB. For the basic System Analyzer, the step attenuator is controlled directly by a knob on the front panel. With the IEEE control option (A13), the step attenuator is electrically programmable and controlled by the processor. In this case, the knob on the front panel is connected only to a rotary switch which directs the processor in setting the attenuation level. Under IEEE control. commands coming via the IEEE bus determine the attenuator setting.

2.3.6 INPUT/OUTPUT

The step attenuator is connected to the output port relay, which chooses between the Antenna or RF In/Out port. There is a 30-dB difference between these two ports. The Antenna port is for receiving low-level signals (less than 100 mW) and for generating high-level signals (+13 dBm). The RF In/Out port is for receiving high-level signals, with a maximum of 125W.

2.4 WATTMETER

Input power measurements from 1 to 125W are made only through the RF In/Out port. (To measure the power of signals under 1W, see paragraph 2.5, MONITOR MODE.)

A block diagram of the wattmeter is shown at the end of the section in Figure 2-4.

The RF input signal is first attenuated by a 14-dB attenuator and then is loaded with a 50-ohm, 16-dB attenuator. A sample of the input RF voltage between the two attenuators is detected by the power detector, to give a dc output proportional to the peak RF voltage. The amplifier following the detector buffers and amplifies the detected voltage to provide the RF INPUT POWER signal to the processor. The processor then determines and displays the RF input power.

A temperature sensor located near the flange of the RF load alerts the processor when the load temperature exceeds 80°C. The processor responds to the OVER TEMPERATURE signal by displaying a warning message on the CRT and by sounding the audible alarm.

2.5 MONITOR MODE

2.5.1 GENERAL

In monitor mode, RF signals from an antenna or from a transmitter can be checked directly for frequency error, signal strength, modulation level, and spectral content. Also provided is off-the-air decoding of two-tone or 5/6-tone paging, private line (PL), digital private line (DPL) or mobile telephone signaling. Another feature is Scan Lock, which allows the System Analyzer to acquire a received signal of greater than −30 dBm.

A block diagram of the monitor mode is shown at the end of the section in Figure 2-5.

2.5.2 RF INPUT

For signals less than 100 mW, the RF signal to be monitored is applied to the Antenna port; for signals greater than 100 mW, to the RF In/Out port. The port-select switch routes one of these signals to the step attenuator.

In the monitor mode, the RF input from the step attenuator is connected to the RF port on the receive mixer. The output from the Wideband Amplifier is switched to the L.O. port on the receive mixer. The processor programs the RF Synthesizer for an output frequency that is offset 10.7 MHz from the frequency to be monitored. The offset may be above or below the center frequency, as selected by the front panel's Image switch. The 10.7-MHz difference signal at the IF port of the receive mixer is filtered by a 20-MHz low-pass filter. The filter output provides the 10.7-MHz IF signal to the Receiver board (A8). The overall gain of the RF Input module (A17) is −8 dB ±2 dB.

2.5.3 RECEIVER

The 10.7-MHz IF signal is first filtered and amplified on the Receiver board, providing a bandwidth of 280 kHz. This signal is split between the linear IF and the logarithmic IF by an active power splitter. The linear IF provides for demodulation of AM, FM, and SSB signals. The logarithmic IF provides two functions: spectrum analyzer and signal-strength indicator.

2.5.3.1 Linear IF

The linear IF bandwidth is determined by a wide/narrowband filter which follows the power splitter. The modulation-acceptance bandwidths are ±6 kHz for narrowband and ±100 kHz for wideband. Next, the IF signal is down-converted to 700 kHz by an active AGC'd mixer. Immediately following the second mixer is the 700-kHz second IF amplifier. The output level of the amplifier is rectified to detect amplitude modulation and to provide AGC control on the second IF amplifier, the second mixer, and the delayed-AGC amplifier. The second IF signal is applied to the FM demodulator and to the BFO mixer for SSB demodulation. The L.O. signal for the BFO mixer comes from a 700-kHz (±3 kHz) oscillator on this board. This oscillator is controlled from the front panel.

Demodulated audio from the AM, FM, or SSB demodulator is routed to the audio filters by the audio-select switch, which is under processor control. The audio filters consist of a selectable-bandwidth low-pass filter (300 Hz, 3 kHz, or 20 kHz), and a selectable-bandwidth high-pass filter (300 Hz or 3 kHz). The selected demodulator output is used to provide three receiver outputs: 1) The VOL CONTROL AUDIO signal is the unfiltered version of the selected demodulator output. It goes to the Volume control on the front panel, to an amplifier on the Scope/DVM Control board (A7) and finally to the speaker; 2) The DEMOD CAL AUDIO output is the filtered version of the demodulator output and provides calibrated audio levels for determining modulation level; 3) The DEMOD OUT signal is also a filtered version of the demodulator output and drives the front panel's DEMOD OUT port.

2.5.3.2 Logarithmic IF

The 10.7-MHz IF input signal is down-converted to 460 kHz by mixing the input signal with the 10.24-MHz signal from a second local oscillator. The second local oscillator is provided by a crystal oscillator on the Receiver board. Two outputs are provided by the logarithmic amplifier and detector. These outputs provide a dc voltage that is proportional to the logarithm of the 10.7-MHz IF input level. One output, SPECTRUM ANALYZER VOLT, is the vertical input to the scope for the spectrum-analyzer display. The other output, SIG STRENGTH VOLTAGE, is measured by the digital voltmeter (DVM) on the Processor Interface board (A11) to provide the signal strength (in dBm) of the 10.7-MHz IF input signal. The logarithmic amplifier has a dynamic range of approximately 80 dB, covering input levels from −110 to −30 dBm.

2.5.3.3 Signal-Present Detector

During Scan Lock operation, a wideband-signal detector indicates the presence of a signal within 20 MHz of the L.O. frequency. The 10.7 MHz IF input is amplified and applied to a diode detector. When the signal level is above about −30 dBm and within 20 MHz of the L.O. frequency, the WB SIG PRES output goes low, indicating signal presence.

2.5.3.4 Frequency-Error Indicator

One of three signals internal to the Receiver may be switched to the IF/BFO output for use in frequency-error indication. During AM and FM monitor operation, the limited, linear IF output is selected and routed to the frequency counter on the Processor Interface board (A11). The difference between this frequency and 700 kHz is computed by the processor and displayed as frequency error. During SSB monitor operation, the BFO output is switched to the IF/BFO output. The difference between this frequency and 700 kHz is computed and displayed as BFO error. During Scan Lock operation, the wideband-signal detector's output is switched to the IF/BFO output. The frequency of this signal is equal to the difference between the RF input frequency and the L.O. frequency.

2.6 DUPLEX GENERATOR

Simultaneous generate and monitor functions are available with the Duplex Generator. The frequency spread between generate and monitor frequencies is limited to a range of 0 to 10 MHz and a fixed frequency of 45 MHz.

A block diagram of the Duplex Generator function is shown at the end of the section in Figure 2-6.

The Duplex Generator signal is generated by mixing the L.O. signal for the first receive mixer with a signal from the offset phase-locked-loop (PLL). The frequency of the offset PLL equals the desired spread between generate and monitor frequencies, minus the 10.7-MHz IF offset. The monitor function is unaffected by the Duplex mode and operates as described in paragraph 2.5.

Frequency modulation of the Duplex output is obtained by modulating the offset PLL via the OFFSET MOD signal line. The OFFSET MOD signal is generated on the Audio Synthesizer board (A10). The offset PLL is controlled via the RF CONTROL BUS.

2.7 CODE SYNTHESIZER

Three simultaneous modulation sources are possible with the internal code synthesizer. The levels of a private line (PL) or digital private line (DPL) source, a fixed 1-kHz source, and external modulation sources can be individually controlled and summed together to give the composite modulation signal. The code synthesizer provides the modulation source for the system in the generate mode and can be used as an audio-frequency source. For the IEEE option, modulation levels can be controlled by the processor.

A block diagram of the code synthesizer is shown at the end of the section in Figure 2-7.

The PL signaling-sequence is generated by an audio synthesizer with an output frequency range from 5 Hz to 20 kHz in 0.1-Hz steps. The frequency is programmed by the processor in response to the operator's request from the keyboard through the CRT display. The programmable attenuator following the audio synthesizer provides attenuation levels of 10 dB and 30 dB for the Tone-Remote-Access Sequence.

DPL code words are generated by the processor in response to the code entered by the operator. The 23-bit DPL word is stored in the DPL generator and continuously output when selected. Either PL or DPL signals are switched to the code synthesizer level control (Code Synth Lvl) on the front panel.

A 1-kHz reference signal from the RF Synthesizer is bandpass-filtered to provide a low distortion, 1-kHz sinewave to the front panel's 1 KHz Level control.

Two sources of external modulation are possible through two ports on the front panel: a standard Motorola microphone-interface port and a BNC port. The microphone input (Mic) is connected to an instantaneous deviation-control (IDC) circuit for peak-limiting. The composite of the two external modulation sources is the signal which goes to the Ext Level control on the front panel.

On systems without the IEEE option, the wipers of the level-control potentiometers will be jumpered from their respective inputs to the summation amplifier on the Audio Synthesizer board (A10). On those systems with the IEEE option, select switches on the IEEE Interface board send either the tops of the level controls (Code Synth, 1 KHz, or Ext) or their respective wipers to the programmable attenuators. For remote control, they select the tops; for local control, the wipers. During the IEEE control mode, the processor-controlled programmable attenuator on the IEEE board controls the modulation level. For the local mode, the attenuators are programmed for zero attenuation so that the wipers of the level control set the modulation levels directly.

The three modulation sources are summed together on the Audio Synthesizer board according to what is set on the level controls. This composite modulation signal is applied to 1) the appropriate modulator, 2) the modulation-measuring circuitry (MOD CAL AUDIO), 3) the audio amplifier (SPKR AUDIO) and 4) the front panel's modulation output port (Mod Out). To provide a low-impedance output, the signal to the front panel's port is driven by a buffer amplifier.

For AM, the composite modulation is summed with +5 Vdc. This signal (5V + AM MOD) is applied to the top of the front panel's RF Level control. The wiper

of the RF Level control is then applied to the AM MOD + DC REF input of the Wideband Amplifier board (A17A2). The dc component on this input controls the average power output, and the ac component provides AM. On systems under IEEE option control, the wiper of the RF Level control is connected to a programmable attenuator on the IEEE Interface board (A13) and then to the AM MOD + DC REF input of the Wideband Amplifier. This allows remote control of the RF output power.

2.8 FREQUENCY COUNTER

Three possible signal sources can be connected to the frequency counter. Two of the signals are internal to the system: one is used to determine the error frequency of the monitored carrier (IF/BFO), and the other is used to decode the off-the-air signal sequences. The third input is from the external input port (Counter In) on the front panel.

A block diagram of the frequency counter is shown at the end of the section in Figure 2-8.

The Receiver's (A8) DEMOD CAL AUDIO output, which is used for signal-sequence decoding, is routed through a gain-selectable amplifier and the Scope/DVM Control board (A7) and to the Front-Panel Interface board (A15). A switch on the Front-Panel Interface board routes this signal or the signal from the front panel's external input port to the range attenuator. The range attenuator provides stepped sensitivity settings according to the setting on the front panel's vertical range switch. An amplifier following the range attenuator amplifies and limits the signal amplitude for the frequency-counter input.

A select switch on the Processor Interface board (A11) routes either the frequency-counter output from the Front-Panel Interface board or the IF/BFO output from the Receiver to the frequency-counter circuitry. The signal selected is determined by the system's operating mode and controlled by the processor.

The frequency counter uses two different measuring techniques: the direct count and the reciprocal count. A 16-bit gated accumulator is used in the direct-count method to determine the input frequency. Gate times from 1 msec to 10 sec are user-selectable or automatically selected by the processor to give the maximum possible resolution. The gate times are derived from the SYNTH 1 KHz signal coming from the Audio Synthesizer board (A10).

The same 16-bit accumulator is used in the reciprocal-count method. The accumulator counts the number of clock cycles coming from a clock generator during one period of the unknown signal. Clock rates from 10 MHz to 100 kHz are user-selectable or automatically selected by the processor to give the maximum possible resolution. The clock rates are derived from the SYNTH 10 MHz signal coming from the RF Synthesizer module (A9).

The 16-bit frequency-counter output is transferred directly to the processor bus through a peripheral-interface adapter (PIA). The processor, in turn, adjusts the data for the gate time used and then processes the information to obtain the required frequency display.

2.9 DIGITAL VOLTMETER (DVM)

The DVM circuitry allows the processor to access many voltages throughout the system. From this information, the processor is able to determine and display parameters such as output power level, modulation level, input power level, etc. In addition, an external voltage applied to the DVM input port on the front panel can be measured and displayed.

A block diagram of the DVM function is shown at the end of the section in figure 2-9.

Internal voltage measurements are selected and ranged over two decades by the internal DVM-select switch and the X1.0/X0.1 attenuator, respectively, on the Scope/DVM Control board (A7). The resulting 0 to 1-Vdc signal is routed to the internal/external DVM-select switch on the Processor Interface board (A11) which applies the voltage to the A/D converter. The A/D converter converts the input voltage into a 10-bit digital number which is input to the processor. One of eight internal voltages may be selected for measurement as required by the processor to determine display data. Inputs to the A/D must be less than 1 Vdc; therefore, with the decade-ranging attenuator (X1.0/X0.1), the maximum input voltage to the internal DVM is 10 Vdc. The X1.0 position gives improved resolution for reading voltages less than 1 Vdc. To keep CRT information current, each of the required measurements is made in sequence, at an approximate rate of thirty per second.

The following signals can be connected to the DVM input:

- Two modulation signals (MOD CAL AUDIO and CARRIER + MOD LVL) and a demodulated signal (DEMOD CAL AUDIO) are made available to the peak detectors. Measuring the positive and negative peaks of the selected signal enables the processor to determine the level of modulation.
- A low-pass filter (LPFL) removes the ac component from the CARRIER + MOD LVL signal so that the output level of the generated RF can be determined. (See paragraph 2.3.4.)
- The SIG STRENGTH VOLTAGE line from the logarithmic amplifier on the Receiver board (A8) provides a dc level proportional to the strength in dBm of the on-channel received signal.
- The RF INPUT POWER signal line from the RF Input module provides the processor input for the internal wattmeter (paragraph 2.4). Inputs for the external wattmeter element (EXT FWD PWR and EXT RFL PWR) from the front panel's port provide the information for the external-wattmeter display.

- A signal line (DC IN) from the rear panel's dc-input port (DC POWER) is brought to the processor to determine battery voltage. The voltage is attenuated by a factor of 10 to stay with the 10V maximum input to the select switch. The processor uses the battery-voltage measurement to warn the operator when the battery is near its discharged state.
- A rectified and filtered version of the input to the 1-kHz notch filter is the last internal measurement point. This measurement is used in calculating the distortion/SINAD reading. (For further information on the distortion/SINAD meter, see paragraph 2.10.)
- In the external DVM mode, voltages applied to the external DVM input port on the front panel are ranged by processor-control over four decades on the Front-Panel Interface board (A15). The result is a 0 to 1-Vrms signal at the output of the attenuator for inputs of 0 to 300 Vrms. The signal is routed directly through the A7 board by the rms/distortion-select switch to the rms-to-dc converter on the A11 board. It is then routed through the internal/external DVM-select switch, to the A/D converter, and finally to the processor's data bus.

For external dc measurements, the ac/dc-select switch chooses the dc-coupled path from the DVM input port. A low-pass filter on the A15 board removes ac components. The rejection of the low-pass filter at 50 Hz is at least 20 dB. The rms-to-dc converter reads the absolute value of the dc input, and the sign detector provides polarity information.

For ac voltage measurements, the low-pass filter is reprogrammed for less than 1% attenuation out to 20 kHz. The ac/dc-select switch chooses the ac-coupled path, and the rms-to-dc converter converts the ac input into a dc voltage equal to the rms voltage of the input.

2.10 DISTORTION/SINAD METER

The System Analyzer can measure the distortion of a signal with a fundamental frequency of 1 kHz. As the block diagram (Figure 2-9) shows at the end of the section, the 1-kHz input enters the DVM input port through the ac-coupled path and is ranged to between 0 and 1 Vrms by the ranging attenuator. The signal is then routed through the notch filter where the fundamental frequency is removed. The rms/distortion-select switch chooses output of the notch filter and sends it to the rms-to-dc converter's input. Here, the rms-to-dc converter measures the rms voltage (to 10 kHz) of the distortion components. The input of the notch is rectified, filtered, and multiplied by 1.11 (the rms-to-average ratio for a sinusoid). The resulting dc voltage is measured by the internal DVM as described in paragraph 2.9. The processor divides the rms output voltage of the notch filter by the rms input voltage to the notch filter to obtain a distortion ratio, and then converts the distortion ratio to dB for the SINAD display. The display for percent distortion is obtained by multiplying the distortion ratio by 100.

2.11 OSCILLOSCOPE

Three basic functions are provided by the system oscilloscope: 1) alphanumeric, 2) modulation, and 3) external-oscilloscope display.

A block diagram of the oscilloscope is shown at the end of the section in Figure 2-10.

Drive signals for the CRT are provided by circuits on the Scope Amplifier board (A2). Horizontal and vertical signals are amplified by their respective amplifiers from input levels of 0.5 V/Div to the levels required on the deflection plates. A Z-Axis modulator circuit controls the cathode-to-grid bias voltage on the CRT to give intensity control.

2.11.1 HORIZONTAL INPUT

External or internal signals can be selected for the horizontal-amplifier input. External signals come from the front panel's Ext Horiz input port. Internal signals come from the A7 Scope/DVM Control board (INT SCOPE HORIZ) or from the horizontal timebase generator on the Scope Amplifier board (A2). When either the external input or the timebase generator is selected, it is summed with a dc signal (HORIZ POSITION) which comes from the front panel's Horiz position control. The dc signal controls the horizontal position of the scope display.

The front panel's Ext Horiz input is applied to the top of the horizontal vernier-gain potentiometer. The wiper of the gain potentiometer provides the HORIZ INPUT signal to the pre-amplifier on the Front-Panel Interface board (A15). The pre-amplifier provides the required horizontal-input sensitivity and buffers the signal from the select switch on the Scope Amplifier board.

The horizontal timebase generator provides a six-decade sweep range from 1 μsec to 100 msec per division. Control of the timebase generator comes from the front panel's horizontal switch through the processor.

The INT SCOPE HORIZ signal is a sawtooth waveform which is provided by the output of either the horizontal character-sweep generator or the synthesizer-sweep generator. A switch on the Scope/DVM Control board controls which output is selected. During character display, it selects the character sweep, which provides the horizontal sweep for the raster-scan character display. During spectrum-analyzer and RF generator sweep operation, control of the INT SCOPE HORIZ signal alternates between character sweep and synthesizer sweep. This allows the oscilloscope and character information to be simultaneously displayed on the CRT. This also allows the scope sweep to be synchronized with the RF Synthesizer sweep.

2.11.2 VERTICAL INPUT

One of four possible signals can be switched to the vertical amplifier's input by a select switch on the Scope/DVM Control board. The 700-kHz IF and SPEC ANA VERT signals from the Receiver board provide the displays for IF envelope and spectrum analyzer, respectively. The vertical character-sweep generator provides the vertical sweep for the raster-scan character display. The remaining input (VERT FROM RNG SW) is connected either to the front panel's external vertical input or to the modulation-scope input (INT SCOPE TO RNG SW).

A vertical pre-amplifier on the Front-Panel Interface board gives a vertical sensitivity of 10 mV/Div and provides positioning and vernier-gain capability for its input. This amplifier provides the VERT FROM RNG SEL output to the A7 board. It is preceded by a four-decade range attenuator which is controlled from the front panel's vertical switch through the processor. The attenuator provides external vertical-input sensitivities from 0.01 to 1.0 V/Div and modulation-scope sensitivities from 0.25 to 25 kHz/Div.

A select switch ahead of the attenuator chooses between the external vertical input or the modulation-scope inputs. Further switching selects ac or dc coupling for the external input. The modulation-scope signal path is switched to one of three possible sources on the Scope/DVM Control board. Demodulation signals from the Receiver are selected via the DEMOD CAL AUDIO path. FM signals are selected via the MOD CAL AUDIO signal path; AM signals are selected via the CARRIER + MOD LVL signal paths. The Audio Synthesizer board provides the MOD CAL AUDIO signal, while the RF Input module provides the CARRIER + MOD LVL signal.

A Z-Axis select circuit on the Scope/DVM Control board gates either the CHARACTER GEN signal for character displays or the retrace blanking signal from the timebase generator for scope displays to the Z-Axis modulator on the Scope Amplifier board.

Figure 2-1. Block Diagram

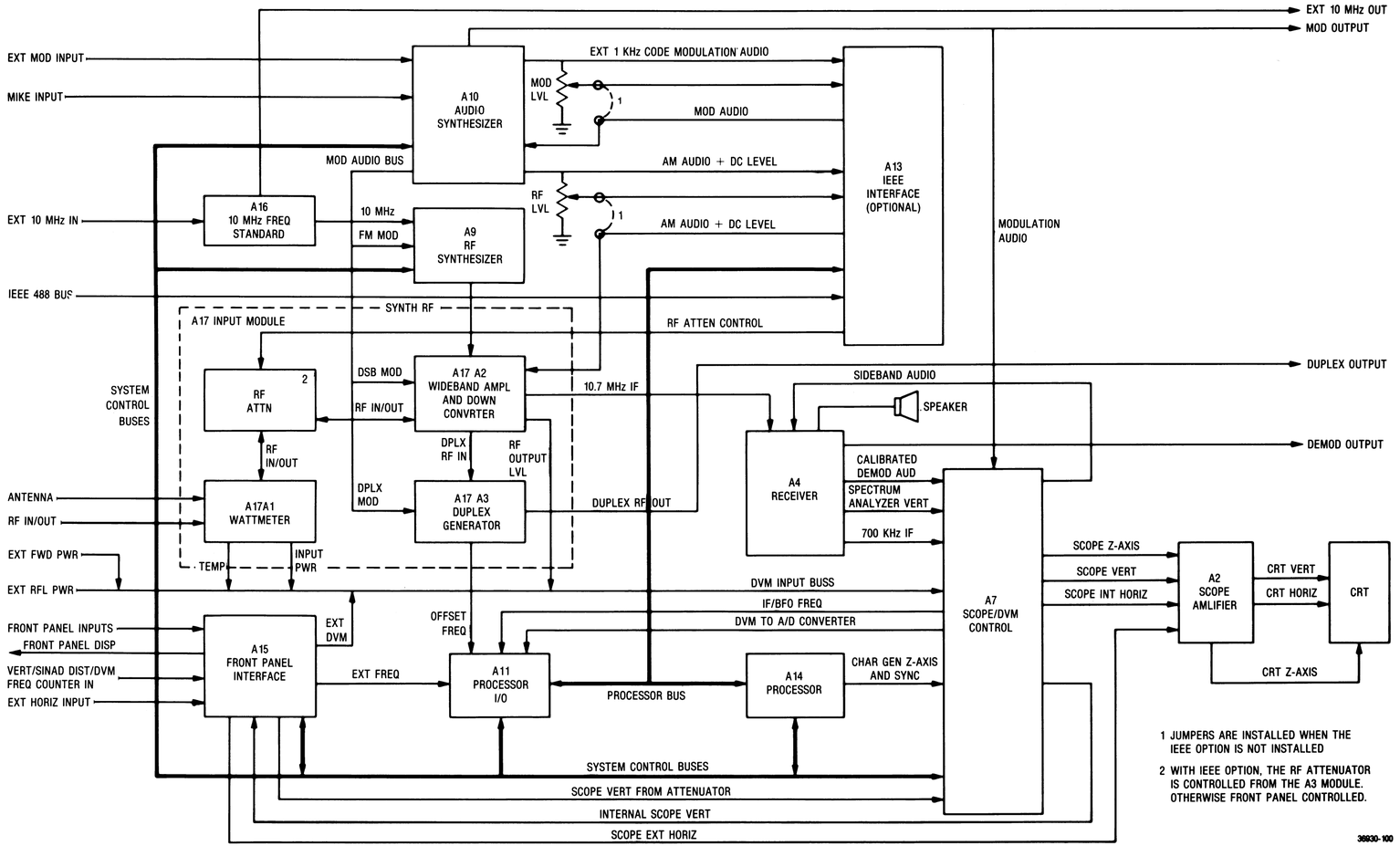


Figure 2-2. Bus Structure

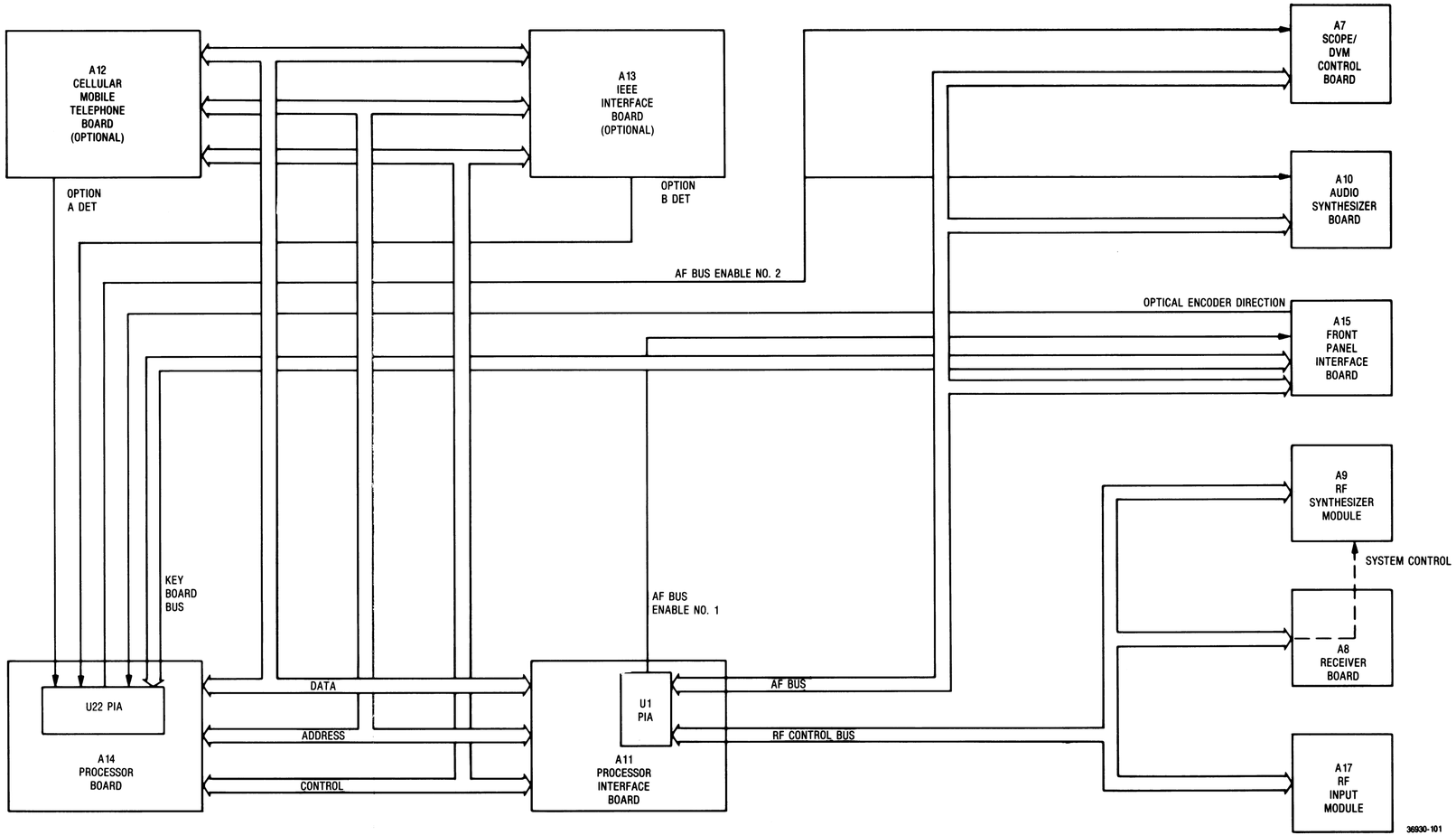
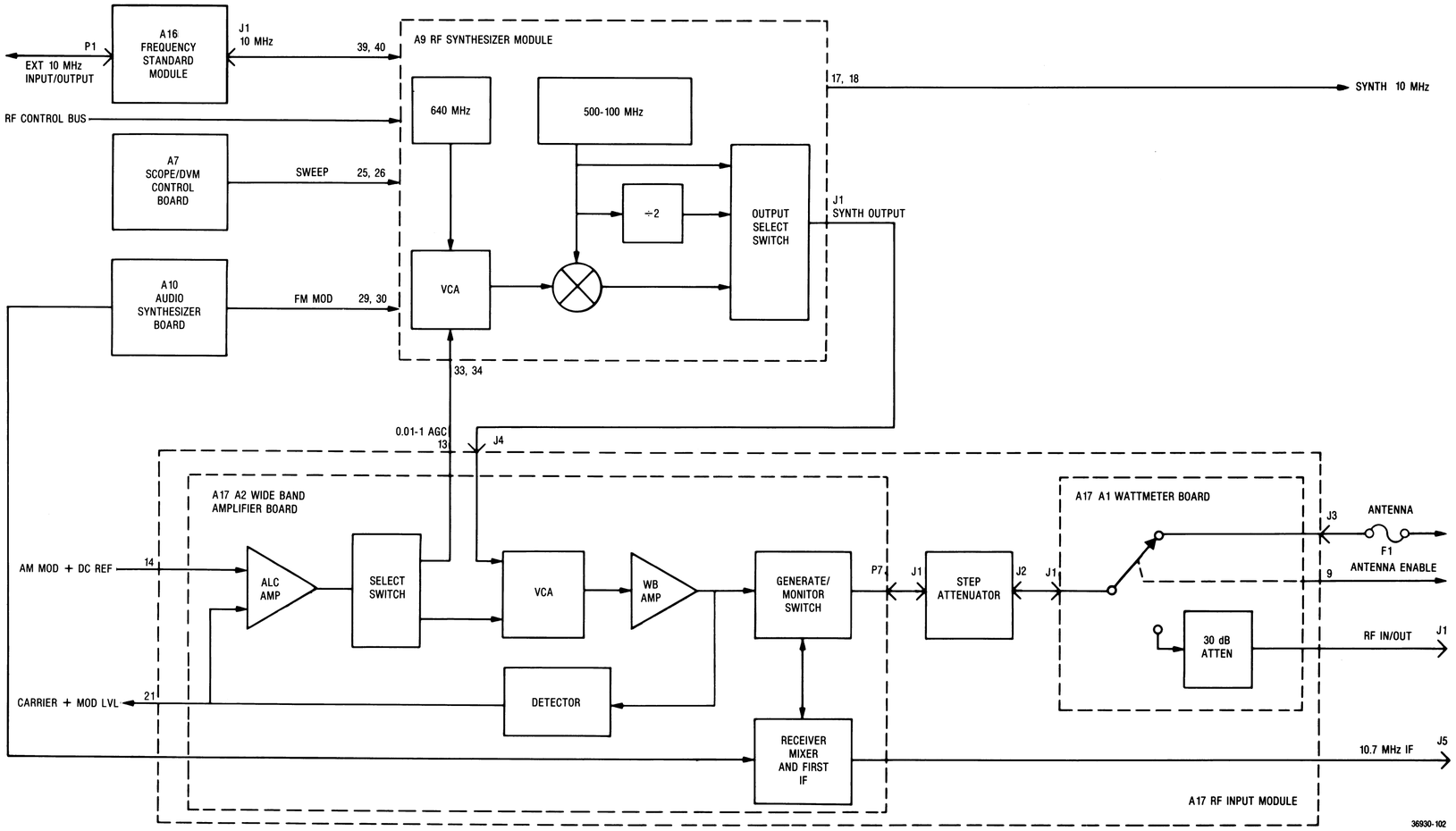


Figure 2-3. Block Diagram



WATTMETER

Figure 2-4. Block Diagram

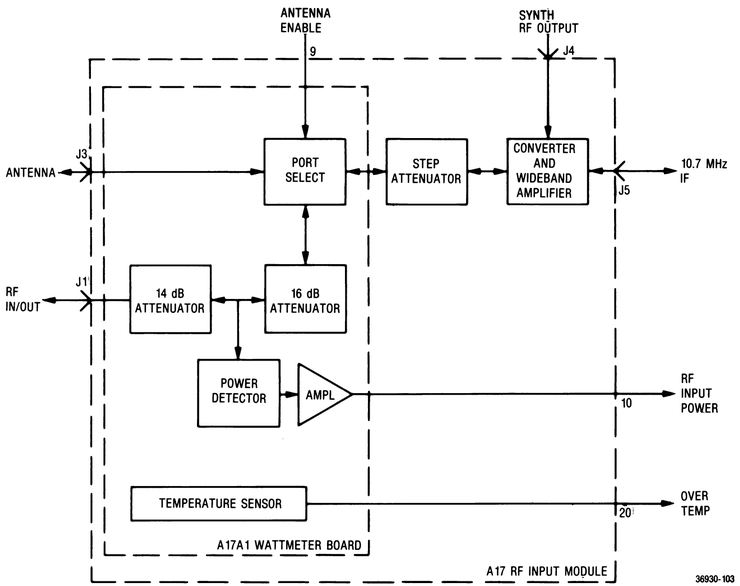
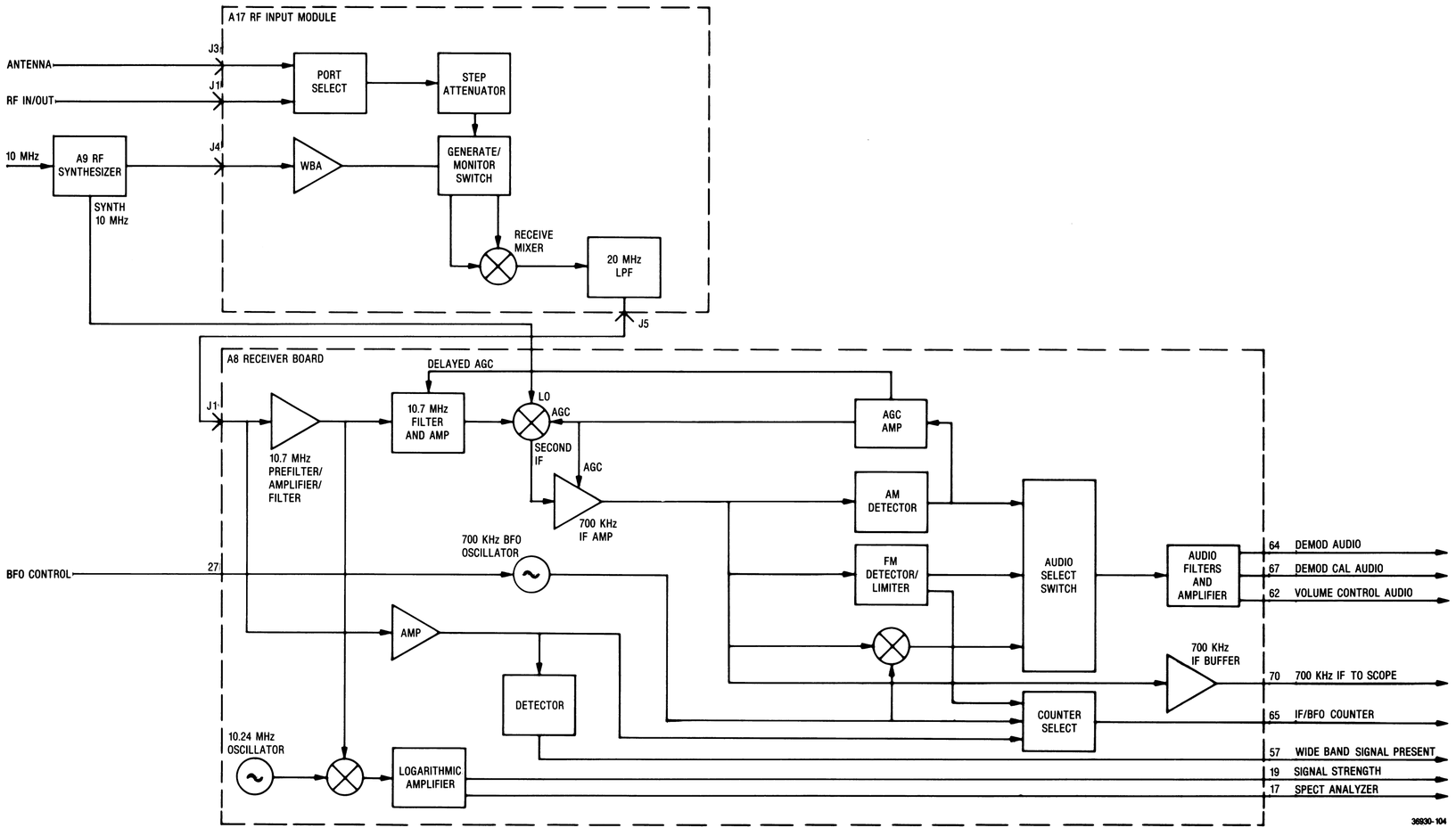


Figure 2-5. Block Diagram



DUPLEX GENERATOR

Figure 2-6. Block Diagram

CODE SYNTHESIZER

Figure 2-7. Block Diagram

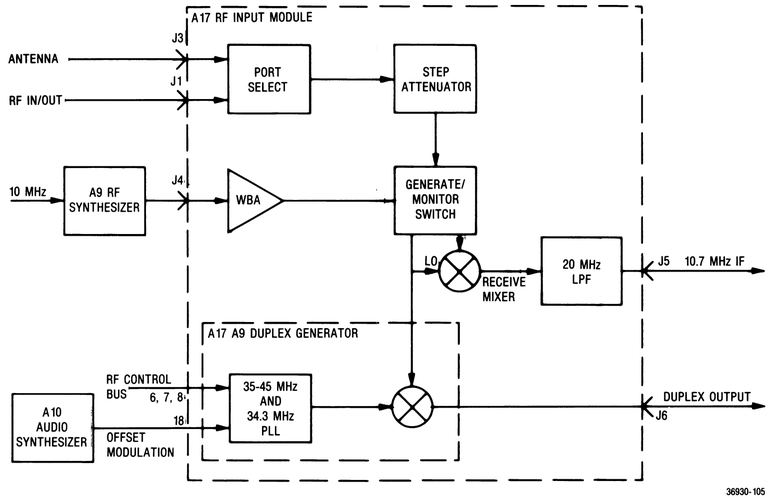


Figure 2-6. Duplex Generator - Block Diagram

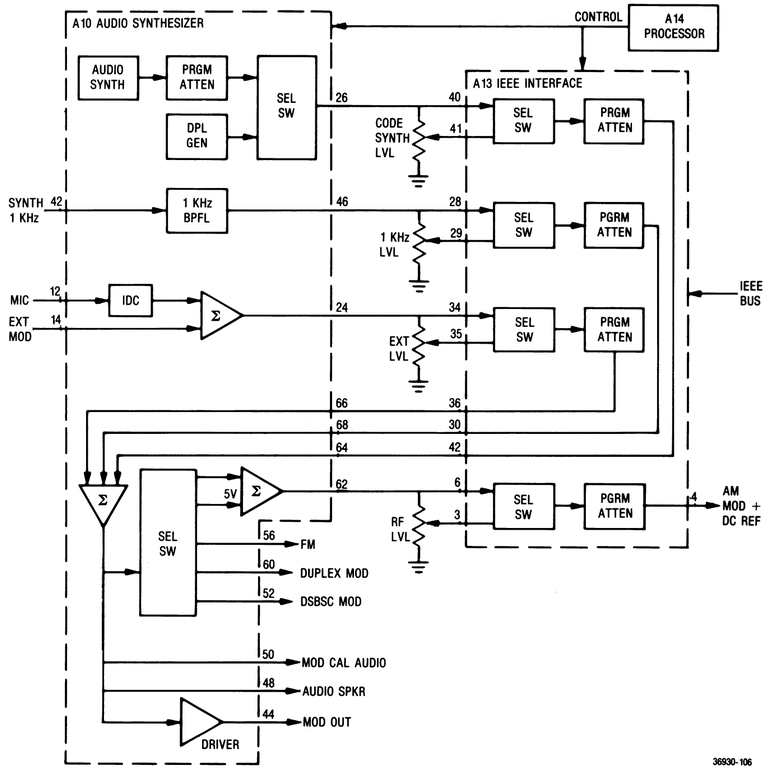
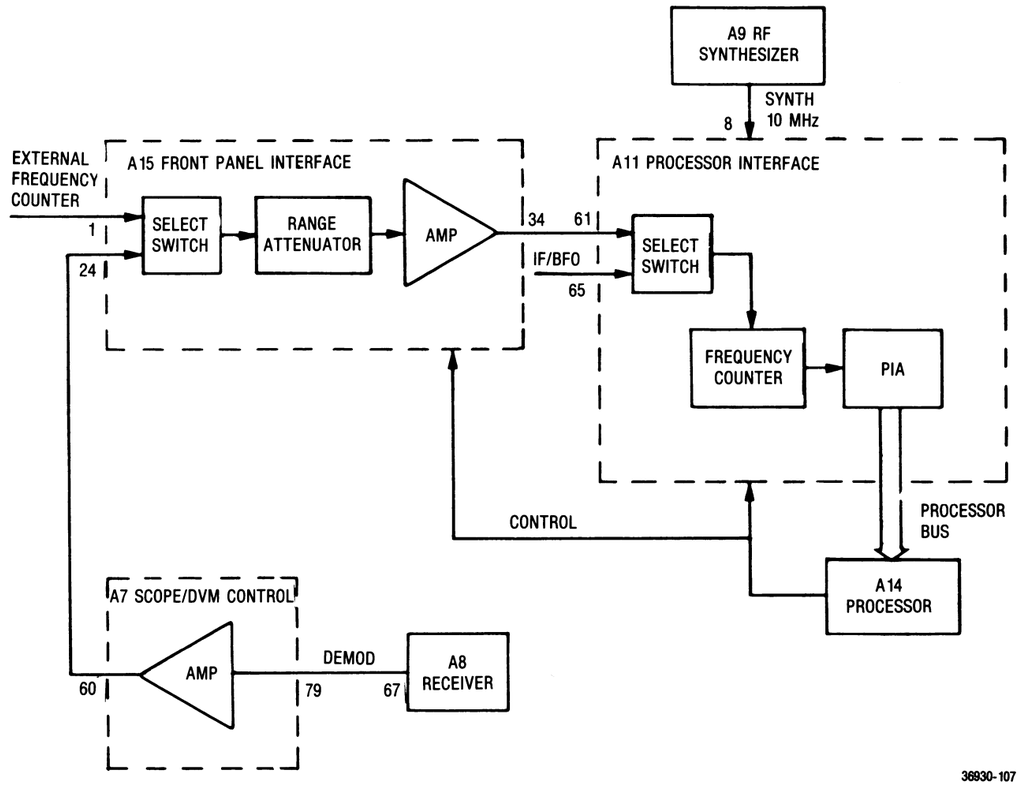


Figure 2-7. Code Synthesizer - Block Diagram

FREQUENCY COUNTER

Figure 2-8. Block Diagram



DVM/DISTORTION ANALYZER

Figure 2-9. Block Diagram

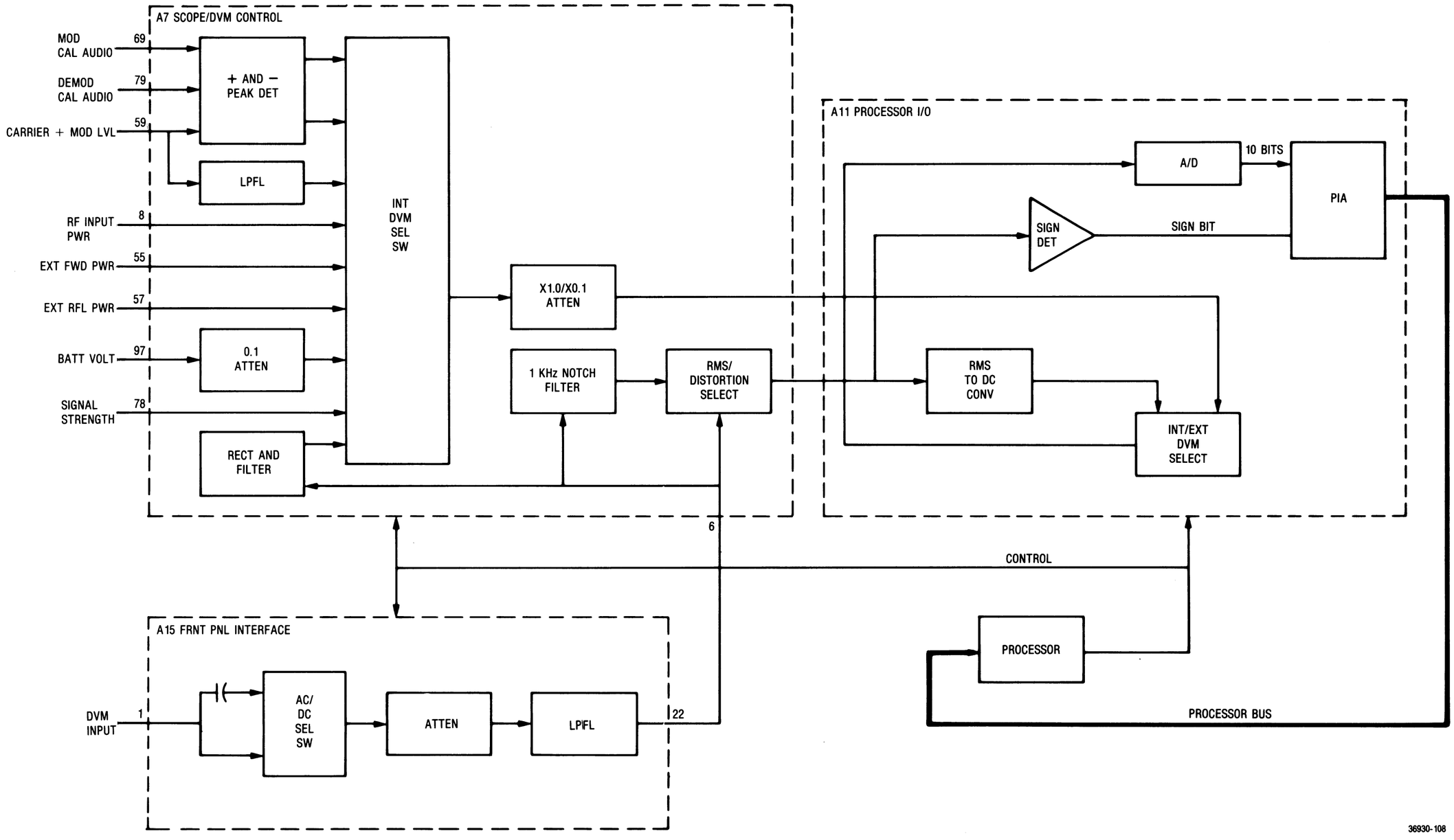


Figure 2-10. Block Diagram