## SECTION 14. PROCESSOR BOARD (A14)

### 14.1 DESCRIPTION

The Processor board provides primary control and data manipulations for the System Analyzer. This board contains the microprocessor, program read-only memory (ROM), nonvolatile memory (NVM), ran-dom-access memory (RAM), peripheral-interface adapter (PIA), timing generator, and character generator. Input and output information is transferred through the PIA and the address, data, and control busses. The board uses a Motorola M6800-series microprocessor, $2 \mathrm{~K} \times 8$ of RAM, $1 \mathrm{~K} \times 8$ of NVM, and $24 \mathrm{~K} \times 8$ of paged ROM.

A block diagram of the Processor board is shown at the end of this section in Figure 14-2, a schematic in Figure 14-3, and the printed wiring board assembly and parts list in Figure 14-4.

### 14.2 THEORY OF OPERATION

### 14.2.1 MICROPROCESSOR

An M6809 microprocessor controls the System Analyzer's operating modes. The device has an 8 -bit data bus, a 16 -bit address bus, and a control bus which synchronizes data transfer and specialized processor functions. The microprocessor uses the $4-\mathrm{MHz}$ crystal (Y1) to provide an operating frequency of 1 MHz on the $E$ and $Q$ lines.

### 14.2.2 MEMORY

### 14.2.2.1 Memory Access

To allow the microprocessor's 16 -bit address to access more than 64 K of memory, the memory is structured in pages, as shown in Figure 14-1. The pages are broken down into chip-select blocks. To select a page of memory, the processor uses two outputs (PB1 and PB2) from PIA U22. (See the A11 section, paragraph 13.2.1.1 for a description of the PIA.) These two signals work in conjunction with the address decoders (U23, U50, and U51) to select the proper memory device.

### 14.2.2.2 Program Read-Only Memory (ROM)

The program memory for the main System Analyzer is located on page 2 of the memory map. The ROM consists of three $8192 \times 8$-bit and two $16,384 \times$ 8 -bit read-only memory devices. The program memory for the IEEE option (Option B) and the cellular mobile telephone option (Option A) is contained on pages 1 and 3 . Option B uses a single $8192 \times 8$-bit ROM device, while Option A uses two $16,384 \times 8$-bit ROM devices.


Figure 14-1. Memory Map

### 14.2.2.3 Random-Access Memory (RAM)

The random-access memory provides temporary data storage for the processor and for the CRT alphanumeric display. The RAM for the main program and all options is located on page 2 of memory. The main program's RAM can store 1024 eight-bit words, of which 512 are used for the CRT display data. Option A has provisions for a $1024 \times 8$-bit RAM device.

### 14.2.2.4 Nonvolatile Memory (NVM)

The nonvolatile memory provides storage for 1024 8 -bit words. Data that is to be held during power-off is held in the NVM, which consists of a battery-backed RAM. When the power is turned on, the microprocessor reads the NVM contents to obtain its start-up mode, the RF and tone-memory presets, and the remainder of the preset data. If the operator changes a preset, the microprocessor changes the data in the NVM to remember the new preset.

### 14.2.3 INPUT/OUTPUT

Peripheral-interface adapters provide input and output latches for external data to and from the processor. The PIA on this board (U22) provides for nine inputs from the keyboard, four column inputs (COL 03 ), and five row inputs (ROW $0-4$ ). When the two inputs OPT A DET and OPT B DET are pulled low, they signal the processor that the Option A or Option B boards are installed. Another input (OPTO DIR) provides the processor with the optical encoder's direction of rotation. Two outputs, PB0 and PB1, select the memory page.

### 14.2.4 CHARACTER DISPLAY

### 14.2.4.1 General

Characters are displayed on the CRT as 8-by-8 dot matrices. Thirty-two dot matrices, of which the last two are always blank, make one character line. Sixteen character lines, of which the last one is always blank, make a display frame. Thus, the total number of matrices available for character display is $30 \times 15$ or 450 . The two blank matrices and the blank line are used for horizontal and vertical retrace blanking, respectively. The display is generated by dot rows. As the CRT sweeps the first dot row of a character line, the character generator outputs a serial-bit pattern of 1's and 0 's that turns the CRT intensity on and off. The result is a row of dots that, when combined with the next seven rows, forms a character.
The frame display is stored at U27 in $32 \times 16$ bytes of RAM; this RAM is shared by the character generator and the processor. The two are synchronized to
access the RAM during alternate half cycles of the master E clock. The RAM multiplexer (U24-U26) allows both the processor and the character generator to have non-interference access to the RAM every other 0.5 microsecond. In RAM, the processor stores an 8 -bit word representing the character to be displayed.

### 14.2.4.2 Timing Generator

The timing generator provides timing signals for the character generator. All the timing signals are synchronized to the $1-\mathrm{MHz} \mathrm{E}$ clock from the microprocessor. The E and Q clocks are exclusive-OR'd to provide a $2-\mathrm{MHz}$ signal which is used to clock the 8 bit shift register (U13). This clock signal provides the dot rate. The $1-\mathrm{MHz}$ E clock is divided-by-four by U19, and the resulting signal is used to latch one dot-matrix row into U11. This provides a dot-matrix rate of 250 kHz . The divided-by-four signal is further divided by . a 12 -bit binary counter (U10 and U15), to provide a row rate of 7812.5 Hz , a character line rate of 976.5 Hz , and a frame rate of 61.04 Hz .

### 14.2.4.3 Character Generator

The character generator simultaneously scans the RAM in sequence with the CRT display scan. The signals for the CRT display scan come from the horizontal and vertical character-sweep generators on the Scope Amplifier board (A7). The 12 -bit binary counter provides the 9 bits of information stored in RAM. As each location in RAM is addressed, the 8 -bit word stored at that location is latched into the 8 -bit latch (U11) at the dot-matrix rate of 250 kHz . Seven of the bits are held in the latch and are applied to the character ROM (U12); the remaining bit is not used. An additional 3 bits from the 12 -bit binary counter tell which row of dots is being scanned. Thus, the 10 bits being applied to the character ROM define a particular dot row of a particular character. The 8 -bit pattern that defines this dot row is then available at the output of the character ROM. This output is parallelloaded into the 8 -bit shift register, U13. The 8 bits are serially shifted out on the CHAR GEN Z-AXIS line at a dot rate of 2 MHz . The 12 -bit binary counter also provides synchronizing signals for the character-sweep generators on the A 7 board. The horizontal and vertical character-sweep generators are reset and started by one-shots U34A and U34B, respectively. The horizontal one-shot enable is located at the end of a dot row. The vertical one-shot enable has two sources: the CHAR GEN RESET line for dual-display mode, and the 12 -bit binary counter end-of-frame for character display. Also provided is a signal LINE 1 which signals the dual-display control on the Scope/DVM Control board that the first character line has been traced.





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PROCESSOR BOARD (A14) (Cont)

| $\begin{gathered} \text { Find } \\ \text { No. } \end{gathered}$ | $\begin{aligned} & \text { dy. } \\ & \text { req. } \end{aligned}$ | Parno. | Nomenclature | Part value |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  <br> CMOS RAM <br> CMOS RAM CMOS RAM <br> cmos ram <br> EPROM |

