### 15.1 DESCRIPTION

The Front-Panel Interface board provides two system functions. The first of these is to interface the system's Processor board (A14) with other system modules: primarily the Receiver board (A8), the FrontPanel Interface board itself, the RF Input module (A17), and the Front Panel (A18). The second function is to provide an analog interface between 1) external signals or internal-modulation/demodulation signals and 2) the basic measurement functions in the System Analyzer, the DVM, the scope, and the frequency counter.
A block diagram of the Front-Panel Interface board is shown at the end of this section in Figure 15-1, a schematic in Figure 15-2, and the printed wiring board assembly and parts list in Figure 15-3.

### 15.1.1 PROCESSOR-CONTROL INTERFACE

Control information for the front panel is carried by the AF DATA BUS in 4-bit groups. Information that the microprocessor reads from the Front-Panel Interface includes encoded data from the RF ATTN 0-130 and horizontal SWP SEL inputs, data from the vertical RNG SEL INPUTS, and data from other miscellaneous inputs. Information that the microprocessor sends to the Front-Panel Interface includes data that controls the input switches (Q2, Q3, Q6), the range attenuator (Q4, Q5, Q7, Q8), and the LEDs on the front panel.

Data is transferred to the AF DATA BUS by 3 -state input buffers U13, U17, U19, and U20, and it is transferred from the AF DATA BUS by latches U8 and U9. The microprocessor sequentially addresses each buffer and latch through the AF ADD BUS and address decoder U21. Data is transferred to/from the selected latch/buffer while the AF BUS EN 2 signal is low.

### 15.1.2 ANALOG INTERFACE

The analog outputs of the Front-Panel Interface are driven by four amplifiers: the scope-vertical preamplifier (U3, Q9, Q13, Q14), the DVM buffer amplifier (U5, U6, U4B), the frequency-counter pre-amplifier (Q12, U7) and the scope-horizontal pre-amplifier (U4A). Circuits for input selection (K2-K4, Q2, Q3, Q6), the range attenuator (K5-K8, Q4, Q5, Q7, Q8), and
the unity-gain buffer amplifier (Q1) drive the inputs of the first three amplifiers. The input to the scopehorizontal pre-amplifier comes directly from the edgecard connector.

### 15.2 THEORY OF OPERATION

### 15.2.1 PROCESSOR-CONTROL INTERFACE

### 15.2.1.1 AF Bus

Information is carried between the microprocessor and the Front-Panel Interface by the AF Bus. It consists of a 4 -bit, tri-state data bus (AF DATA BUS 0-3) and a 4 -bit address bus (AF ADD BUS 0-3). When AF BUS EN 2 is asserted low, the input/output (I/O) function of the AF DATA BUS lines is determined by the address on the AF ADD BUS lines. Depending on that address, address decoder U21 can select the following I/O devices: 1) data buffers U13, U17, U19, and U20; 2) data latches U8 and U9; and data latches A18U6, A18U7, and A18U8.

A summary of the functions of the AF DATA BUS lines for each state of the AF ADD BUS is given in Table 15-1.

### 15.2.1.2 LED Control

The AF BUS ADDRESSES 0,1 , and 2 control the output to the display, function, and modulation LEDs on the Front-Panel Display board (A18A1). Latchselects LS0, LS1, and LS2 are asserted low to latch the data that is present on the AF ADD BUS. These latchselects and the AF DATA BUS are connected to the Display board (A18A1) via J1 and a ribbon cable assembly.

Table 15-2 shows which LED is selected when the state of the AF DATA BUS is as shown and the appropriate latch-select (LS0, LS1, or LS2) is strobed low.

### 15.2.1.3 Range-Attenuator Control (ATTN X1, X0.1, X0.01, X0.001)

Location 3 of the AF BUS accesses outputs which control the range attenuator. Table $15-3$ shows the allowable states of these four control bits, and the function of those states.

Table 15-1. AF ADD and DATA BUS

| $\frac{\overline{\text { AFBUS }}}{\text { EN } 2}$ | AF ADD BUS <br> Lines |  |  |  | INPUT/ OUTPUT | $\overline{\mathrm{LSX}}$ <br> ASSERTED | AF DATA BUS 3 | AF DATA BUS 2 | AF DATA BUS 1 | AF DATA BUS 0 | NOTE |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 3 | 2 | 1 | 0 |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 0 | 0 | I | 0 | DISPLAY 3 | DISPLAY 2 | DISPLAY 1 | DISPLAY 0 | * |
| 0 | 0 | 0 | 0 | 1 | I | 1 | FUNCTION 3 | FUNCTION 2 | FUNCTION 1 | FUNCTION 0 | * |
| 0 | 0 | 0 | 1 | 0 | I | 2 | MODE 3 | MODE 2 | MODE 1 | MODE 0 | * |
| 0 | 0 | 0 | 1 | 1 | I | 3 | ATTEN X 0.001 | ATTEN X 0.01 | ATTEN X 0.1 | ATTEN X 1 |  |
| 0 | 0 | 1 | 0 | 0 | I | 4 | Not Used | Not Used | EXT INPUT SELECT | DC SELECT |  |
| 0 | 0 | 1 | 0 | 1 | 0 | 5 | RF ATTEN 3 | RF ATTEN 2 | RF ATTEN 1 | RF ATTEN 0 |  |
| 0 | 0 | 1 | 1 | 0 | 0 | 6 | RF OVER TEMP | $\overline{\text { WB SIG PRES }}$ | ANT SEL | SPARE |  |
| 0 | 0 | 1 | 1 | 1 | 0 | 7 | $\overline{\text { IF OVERLOAD }}$ | $\overline{\text { SIG PRES }}$ | $\begin{aligned} & \text { OFFSET ON/ } \\ & \text { OFF } \end{aligned}$ | WB/NB |  |
| 0 | 1 | 0 | 0 | 0 | 0 | 8 | $\overline{\text { CSSG CONT EN }}$ | $\overline{\overline{\text { ENS }}}$ | IMAGE HI/LO | MON/GEN |  |
| 0 | 1 | 0 | 0 | 1 | 0 | 9 | 10V/DIV RNG SEL | $\begin{aligned} & \text { 1V/DIV RNG } \\ & \text { SEL } \end{aligned}$ | $\begin{aligned} & \text { 0.1V/DIV RNG } \\ & \text { SEL } \end{aligned}$ | 0.01V/DIV RNG SEL |  |
| 0 | 1 | 0 | 1 | 0 | 0 | 10 | SPARE BIT | SWP SEL 2 | SWP SEL 1 | SWP SEL 0 |  |
| 0 | 1 | 0 | 1 | 1 | X | N | X | X | X | X |  |
| 0 | 1 | 1 | X | X | X | N | X | X | X | X |  |
| 1 | X | X | X | X | X | N | X | X | X | X |  |

Table 15-2. Decoding for Display, Function, and Modulation LEDs

| AF DATA BUS Lines |  |  |  | Display LED Selected ( $\overline{\mathrm{LS} 0}$ Strobed Low) | Function LED Selected (LS1 Strobed Low) | Modulation LED Selected ( $\overline{\mathrm{LS} 2}$ Strobed Low) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 1 | 2 | 3 |  |  |  |
| 0 | 0 | 0 | 0 | Gen/Mon Mtr | FM | PL/DPL |
| 0 | 0 | 0 | 1 | Modulation | CW | PL/DPL INV |
| 0 | 0 | 1 | 0 | Spect Analyzer | AM | Tone A |
| 0 | 0 | 1 | 1 | Duplex Gen | SSB/DSBSC | Tone B |
| 0 | 1 | 0 | 0 | RF Memory | SWP 1-10 MHz | Tone Seq |
| 0 | 1 | 0 | 1 | Signaling Seq | SWP $0.01-1 \mathrm{MHz}$ | Tone Remote |
| 0 | 1 | 1 | 0 | Freq Counter | Not Allowed | Not Allowed |
| 0 | 1 | 1 | 1 | DVM/DIST | Not Allowed | Not Allowed |
| 1 | 0 | 0 | 0 | Ext Wattmeter | Not Allowed | Not Allowed |
| 1 | 0 | 0 | 1 | IF | Not Allowed | Not Allowed |
| 1 | 0 | 1 | 0 | Scope AC | Not Allowed | Not Allowed |
| 1 | 0 | 1 | 1 | Scope DC | Not Allowed | Not Allowed |
| 1 | 1 | 0 | 0 | Not Allowed | Not Allowed | Not Allowed |
| 1 | 1 | 0 | 1 | Not Allowed | Not Allowed | Not Allowed |
| 1 | 1 | 1 | 0 | Not Allowed | Not Allowed | Not Allowed |
| 1 | 1 | 1 | 1 | Not Allowed | Not Allowed | Not Allowed |

Table 15-3. Range-Attenuator Switching

| Attenuation | ATTEN Lines |  |  |  | Gain from Selected Input to DVM FROM RNG SW Output | Gain from Selected Input to VERT FROM RNG SW Output (VERNIER CAL POS) | Sensitivity of EXT FREQ. CNTR and EXT FREQ. CNTR Outputs to Selected Input |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | X0.001 | X0.01 | X0.1 | X1 |  |  |  |
| X1 | 0 | 0 | 0 | 1 | 1 | 50 | 30 MV |
| X0.1 | 0 | 0 | 1 | 0 | 0.1 | 5 | 300 MV |
| X0.01 | 0 | 1 | 0 | 0 | 0.01 | 0.5 | 3 V |
| X0.001 | 1 | 0 | 0 | 0 | 0.001 | 0.05 | 30 V |

### 15.2.1.4 Input-Switching Control

Location 4 of the AF BUS accesses outputs which control selection of the external (P1-1) or internal (P124 ) inputs and ac or dc coupling of the external input. This control is achieved with data-bus bits 0 and 1 as shown in Table 15-4.

Table 15-4. Input Switching

| EXT INPUT <br> SEILECT | DC <br> SELECT | Input Source | Coupling |
| :---: | :---: | :--- | :---: |
| 1 | 1 | EXT INPUT | dc |
| 1 | 0 | EXT INPUT | ac |
| 0 | X | INT SCOPE TO RNG SW | dc |

### 15.2.1.5 RF-Attenuator Encoding

The RF ATTEN 0-130 dB inputs indicate the setting of the RF step attenuator in the RF Input module (A17). When one of these inputs is driven high, the corresponding attenuation has been selected. These fourteen inputs are converted to a 4 -bit code ( RF ATTEN 0-3) by priority encoders U10 and U12 and OR gates U12. Location 5 of the AF BUS accesses these outputs. Table 15-5 shows the encoding of the RF ATTEN 0-130 dB inputs into the RF ATTEN 0-3 output.

Table 15-5. RF-Attenuator Encoding

| RF ATTEN Lines |  |  |  |  |  |  |  |  |  |  |  |  |  | RF ATTEN Bits |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 130 dB | 120 dB | 110 dB | 100 dB | 90 dB | 80 dB | 70 dB | 60 dB | 50 dB | 40 dB | 30 dB | 20 dB | 10 dB | 0 dB | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |  | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |

### 15.2.1.6 Miscellaneous Inputs

Locations 6-8 of the AF BUS access miscellaneous
data inputs. Table 15-1 gives the specific location of each input on the bus. Table 15-6 gives a brief description of each input.

Table 15-6. Functions of Miscellaneous Inputs

| Input | Function |
| :---: | :---: |
| RF OVER TEMP | When high, indicates the Wattmeter (A17A1) is overheated. |
| $\overline{\text { WBSIG PRES }}$ | Comes from the Receiver (A8) - during the system's scan-acquisition, indicates the presence of a signal at the monitor input. |
| ANT SEL | Comes from the Front Panel (A18) - selects the system's I/O port. When the variable RF Level control is pulled out, this signal goes high, selecting the Antenna port. When the control is pushed in, this signal goes low, selecting the RF In/Out port. |
| $\overline{\text { IF OVERLOAD }}$ | Comes from the Receiver - indicates the monitor is being over-driven. |
| $\overline{\text { SIG PRES }}$ | Comes from the Receiver - indicates the presence of a signal on the monitor input which is sufficiently high to open the Receiver squelch. |
| OFFSET ON/OFF | Indicates the position of the Duplex Gen switch on the RF Input module (A17). |
| WB/NB | Indicates the position of the bandwidth (BW) switch on the front panel. |
| CSSG CONT EN and CSSG BURST EN | Indicate whether the front panel's Modulation switch is set to Cont or Burst, respectively. |
| IMAGE HI/LO | Indicates the position of the Image/Duplex switch on the front panel. |
| MON/GEN | Indicates the position of the Function switch on the front panel. |

### 15.2.1.7 Range-Select Inputs

The 0.01 to $10 \mathrm{~V} /$ Div RNG SEL inputs indicate which scope vertical-input sensitivity has been selected. When one of these inputs is low, the corresponding sensitivity has been selected. The microprocessor programs the appropriate attenuation in the range attenuator via the ATTN X 0.001 to 1 signals. Location 9 on the AF BUS accesses the 0.01 to 10V/ Div RNG SEL inputs.

### 15.2.1.8 Sweep-Select Encoding

The $1 \mu$ s to $100 \mathrm{~ms} /$ DIV SWP SEL and EXT HORIZ SEL inputs indicate the position of the Oscilloscope Horiz switch on the front panel. When one of these inputs is high, the corresponding switch position has been selected. These inputs are converted to a 3 -bit code, SWP SEL $0-2$, by priority encoder U18, according to the algorithm in Table 15-7. Location 10 on the AF BUS accesses the SWP SEL 0-2 outputs.

Table 15-7. Sweep-Select Encoding

| SWP SEL Lines |  |  |  |  |  |  | SWP SEL Bits |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| EXT HORIZ SEL | $100 \mathrm{~ms} / \mathrm{DIV}$ | $10 \mathrm{~ms} / \mathrm{DIV}$ | $1 \mathrm{~ms} / \mathrm{DIV}$ | $100 \mu \mathrm{~s} / \mathrm{DIV}$ | $10 \mu \mathrm{~s} / \mathrm{DIV}$ | $1 \mu \mathrm{~s} / \mathrm{DIV}$ | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

### 15.2.1.9 RF-Scan Encoding

The OPTICAL ENC A and B inputs carry information from the RF Scan optical encoder on the front panel. This encoder is interfaced to the system microprocessor by U22, U23, and Q16 on the Front-Panel Interface. As the RF Scan control is rotated, each
change in the OPTICAL ENC A input causes the FIRQ output, which goes to the microprocessor, to pull low for approximately $10 \mu \mathrm{~s}$. The OPTO CCW output, which goes to a PIA on the Processor board (A14), indicates the direction of the scanning. This output is generated by latching the OPTICAL ENC B input and exclusively ORing it with the OPTICAL ENC A input.

### 15.2.1.10 Input/Output Characteristics

All digital inputs and outputs are interfaced to ' B ' series CMOS logic, which operates from $0 \mathrm{~V} / 5 \mathrm{~V}$ supplies. To facilitate interface with a mechanical switch, some inputs have pull-up or pull-down resistors.

### 15.2.1.11 Miscellaneous Front-Panel Interconnections

The Front-Panel Interface provides miscellaneous interconnections between the front panel and the rest of the system. These connections come from the front panel through two ribbon cables and connectors, J1 and J2. They are then routed through edge connector P1.

### 15.2.2 ANALOG INTERFACE

### 15.2.2.1 Input Switching (K2-K4, Q2, Q3, Q6)

The input to the range attenuator can be selected from either the EXT INPUT or the INT SCOPE TO RNG SW inputs. Ac or dc coupling may be selected for the external input. Input switching is controlled by the DC SELECT and EXT INPUT SELECT signals, as shown in Table 15-4. The generation of these signals is discussed in paragraph 15.2.1.4.

### 15.2.2.2 Range Attenuator (K5-K8, Q4, Q5, Q7, Q8)

The range attenuator provides four selectable values of attenuation: $\mathrm{X} 1, \mathrm{X} 0.1, \mathrm{X} 0.01$, and X 0.001 . Attenuation is controlled by the ATTEN X 0.001 to 1 signals, as shown in Table 15-3. Compensation capacitor C11 is adjusted for maximum bandwidth. To adjust C11, see Section 3 on alignment.

### 15.2.2.3 Unity-Gain Buffer Amplifier

Unity-gain buffer amplifier Q11 buffers the signals under test from the frequency-counter pre-amplifier, the DVM buffer amplifier, and the scope's vertical preamplifier inputs. R54 (coarse) and R55 (fine) are adjusted so that there is a voltage gain of one from the EXT INPUT to TP1. To align R54 and R55, see Section 3 on alignment.

### 15.2.2.4 Scope Vertical Pre-Amplifier (U3, Q9, Q13, Q14)

The scope's vertical pre-amplifier has a nominal gain of 50 when the front panel's vertical-gain potentiom-
eter (which is connected between VERT GAIN and VERT GAIN RETURN) is set to 0 ohms. When the gain potentiometer is set at 5 K ohms, the gain of the amplifier is less than or equal to 5 . The front panel's 5 K ohm vertical-position potentiometer (which is connected between VERT POSITION and ground) varies the dc offset of the amplifier. This amplifier drives the VERT FROM RNG SW output. R19 and R25 adjust the gain and balance, respectively, of the vertical pre-amplifier. To align R19 and R25, see Section 3 on alignment.

Table 15-3 shows, as a function of the range-attenuator setting, the vertical pre-amplifier's gain from the selected input to the VERT FROM RNG SW output.

### 15.2.2.5 DVM Buffer Amplifier

The DVM buffer amplifier provides switched-bandwidth buffering between the unity-gain amplifier (Q11) and the DVM circuitry on the Scope/DVM Control board(A7). In ac mode, operational amplifier U7 operates as a unity-gain amplifier with a gain flatness of $\pm 2$ percent out to 20 kHz . In dc mode, analog switches U6A and U6C switch C26 and C22, respectively, into the amplifier circuit. In this configuration, the amplifier has a dc gain of 1 and a minimum attenuation of 30 dB at 50 Hz . The amplifier bandwidth is controlled by a signal from latch U9, which has the opposite sense of the DC SELECT signal. U4B inverts the sense of this signal and then translates it from a logic level of 0 to +5 V to a logic level of -8 to +8 V . The signal is now compatible with the control inputs of U6A and U6C. R41 is adjusted for a gain of one from TP1 to the DVM FROM RNG SW output. To adjust R41, see Section 3 on alignment.

Table $15-3$ shows the gain from the selected input to the DVM FROM RNG SW output as a function of the range-attenuator setting.

### 15.2.2.6 Frequency-Counter Pre-Amplifier

The frequency-counter pre-amplifier (Q12 and U7) converts the output of unity-gain buffer Q11 to ECL levels. The output is differentially connected through the EXT FREQ CNTR and EXT FREQ CNTR outputs to the Processor Interface board (A11). Table $15-3$ shows the sensitivity of this amplifier as a function of the range attenuator.

### 15.2.2.7 Scope Horizontal Pre-Amplifier

The scope's horizontal pre-amplifier provides a nominal voltage gain of 5 between the HORIZ INPUT and the HORIZ TO SCOPE AMP output.


FRONT-PANEL INTERFACE BOARD (A15)
(RTC-1011A)
Figure 15-1. Block Diagram



WARNING:
WARNNG:
STATIC-SENSITIVE PARTS


## font-panel interface board (A15) (Cont

| $\begin{aligned} & \text { Find } \\ & \text { No. } \end{aligned}$ | $\begin{aligned} & \text { ary. } \\ & \text { Req. } \end{aligned}$ | Par No. | Nomenclature | Part value |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |


| Fond | ¢ | Parno. | Nomenocature | Part value |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Mcceme simut |

