G E N E R A L D Y N A M I C S

VOL. I

Communications System Analyzer R2600D/ R2625B R2660D/R2670B

Maintenance Manual **RLN5237A**

68-P57058J Rev. A

G E N E R A L D Y N A M I C S

COMMUNICATIONS SYSTEM ANALYZER

Printed in USA

Maintenance Manual RLN5237A

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VOLUME II

1. SCOPE OF MANUAL

This manual contains information for the maintenance of General Dynamics R2600 series Communications System Analyzer, and is intended for use by technicians previously trained in servicing this product. Contact your local General Dynamics Sales representative for training availability and scheduling.

2. PURPOSE AND USE

This maintenance manual is designed specifically as an aid to troubleshooting and repairing the System Analyzer.

Chapters on modules/subassemblies have all been standardized to follow the same format. If you know how any one of them is organized you will automatically know the organization of all of them. A model of typical module/subassembly chapters appears on page vi.

2.1 Manual Organization

The chapters in this manual that cover a specific module or subassembly follow the same format. The subsections appear in figure A on page vi. The content of each subsection is described in detail here where "X" represents any section from 4 to 20, and option modules in appendices.

X.1 General Description
General information about the module appears here.

X.2 Signals Summary
X.2A Signal Descriptions
Each of the modules connectors are summarized. The signals used at each connector appear in alphabetical order with a brief description. Signal source and destinations (relative to this module) are included in the signal description where applicable.

X.2B Connector Descriptions
Each connector is summarized by pin numbers and signal names. Signals that appear at a connector but are not used in the module in any way are marked by the bullet symbol (•).

X.3 Block Diagram Description
General statements about major signal flow appear here. This text can be used with the module block diagram.

X.4 Detailed Description
Theory of operation to the component level (where applicable) is included here and can be used with the module schematic.

X.5 Block Diagram

Component Location Diagram
This drawing indicates the physical location of components mounted on the circuit board.

Schematic
Throughout this manual the asterisk symbol (*) is used only with signal names to indicate the signal is active when in a logic low (0) state. Footnotes within the text are indicated by use of the bullet symbol (•).

3. WARNINGS AND CAUTIONS

You should observe several precautions when handling this equipment.

WARNING

This unit is designed to be operated with a ground connection to the chassis via a three-wire Power connection. If the unit is not properly grounded while operating from an AC power source, the voltage potential between it and ground may cause an electrical shock.

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All sections for individual modules/subassemblies follow this convention (sections 4 to 17)

FIGURE A. Organization of manual (X = any section from 4 to 17)

CAUTION

This equipment contains parts that are subject to damage by static electricity. Take proper precautions when handling them. Refer to page xi in this section for more information.

4. SERVICE

The Motorola Test-Equipment Service Centers service all R2600 Series Communications System Analyzers. The Centers maintain a stock of original equipment replacement parts and a complete library of service information.

5. ADDRESSES

5.1 SERVICE LOCATIONS

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SAFE HANDLING OF CMOS INTEGRATED CIRCUIT DEVICES

Many of the integrated circuits are of the CMOS (Complementary Metal Oxide Semiconductor) type. Because of their high open circuit impedance, CMOS ICs are vulnerable to damage from static charges. Care must be taken in handling, shipping and servicing them and the assemblies in which they are used.

Even though protection devices are provided in CMOS IC inputs, the protection is effective only against overvoltage in the hundreds of volts range such as are encountered in an operating system. In a system, circuit elements distribute static charges and load the CMOS circuits, decreasing the chance of damage. *However, CMOS circuits can be damaged by improper handling of the modules even in a system.*

To avoid damage to circuits, observe the following handling, shipping, and servicing precautions:

1. Prior to and while servicing a circuit module, particularly after moving within the service area, momentarily touch *both* hands to a bare metal earth grounded surface This will discharge any static charge which may have accumulated on the person doing the servicing.

NOTE

Wearing Conductive Wrist Strap will minimize static buildup during servicing.

WARNING

When wearing a Conductive Wrist Strap be careful near sources of high voltage. The good ground provided by the wrist strap will also increase the danger of lethal shock from accidentally touching high voltage sources.

2. Whenever possible, avoid touching any electrically conductive parts of the circuit module with your hands.

3. When servicing a circuit module, avoid carpeted areas, dry environments, and certain types of clothing (silk, nylon, etc.) because they contribute to static buildup.

4. All electrically powered test equipment should be grounded. Apply *the ground lead* from the test equipment to the circuit module *before connecting the test probe.* Similarly, *disconnect the test probe before removing the ground lead.*

5. If a circuit module is removed from the system, it is desirable to lay it on a conductive surface (such as the pad in the Electrostatic Protection Kit) which is connected to ground through 100kΩ of resistance.

WARNING

If the conductive surface is connected directly to ground, be cautious of possible electrical shook from contacting the pad at the same time as other electrical circuits.

6. When soldering, be sure the soldering iron is grounded.

7. Prior to connecting jumpers, replacing circuit components, or touching CMOS pins (if this becomes necessary in the replacement of an integrated circuit device), be sure to discharge any static buildup as described in procedure 1. Since voltage differences can exist across the human body, it is recommended that only one hand be used if it is necessary to touch pins on the CMOS device and associated board wiring.

8. When replacing a CMOS integrated circuit device, leave the device in its metal rail container or conductive foam until it is to be inserted into the printed circuit module.

9. All low impedance test equipment (such as pulse generators, etc.) should be connected to CMOS device inputs after power is applied to the CMOS circuitry. Similarly, such low impedance equipment should be disconnected before power is turned off.

10. Replacement modules shipped separately from the factory will be packaged in a conductive material. Any modules being transported from one area to another should be wrapped in a similar material. NEVER USE NON-CONDUCTIVE MATERIAL for packaging these modules.

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Section 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

The R2600 Communication System Analyzers offer a variety of features and capabilities integrated within one piece of equipment. The R2600 series can perform tests normally associated with the following discrete test instruments:

- RF Signal Generator
- Sensitive Measurement Receiver
- Spectrum Analyzer
- Duplex Offset Generator
- Frequency Counter
- AC/DC Voltmeter
- 50 kHz Oscilloscope
- RF Wattmeter
- Signal Strength Meter
- Frequency Error Meter
- SINAD Meter
- Distortion Meter
- Sweep Generator
- Audio Generator
- Modulation Analyzer
- Signaling Simulator (DTMF, PL, DPL, 5/6 Tone, Select V, Single and Multi-tone sequences)
- RF Scan/Counter

Options within the R2600 series expand the test capabilities to include the following:

- Cable Fault Locator
- Tracking Generator
- Programmable Test Set-Ups
- High Performance Spectrum Analyzer with Markers
- Two-way radio protocols such as:
  Motorola Analog Trunking
  PROJECT 25 (APCO Project 25 Standard) Conventional and Encrypted
  ASTRO Conventional and Encrypted
  Motorola ASTRO Trunking
  SECURENET Secure Voice
  PROJECT 25 Trunking
  iDEN (Integrated Dispatch Enhanced Network)

The R2600D model offers increased capability over the C models. Functional improvements include:

- High Brightness color TFT Liquid Crystal Display (LCD)
- Flash Memory for external updates of operational software
- Higher speed serial port (115.2 kbps)
- VGA compatible output port for external monitor
- Significantly improved response and screen update time

Physical differences include:

- CRT assembly replaced by a thin LCD module with the same viewing area
- A Display Processor Module in the location previously occupied by the CRT control board
- Lower overall weight

1.2 POWER SOURCE

The Analyzer's primary power source is selectable between 110 or 220 volts AC rms over the frequency range of 50-440 Hz. The Analyzer can also be operated from a +11 to +18 VDC power source.

1.3 OPERATOR INTERFACE

All controls and input/output ports have been functionally grouped and human engineered for location. A Liquid Crystal Display (LCD), numeric keypad, screen defined softkeys, cursor movement keys, and optical tuning knob form the primary operator to system interface. A speaker within the Analyzer monitors audio information.

Displays provide a maximum amount of information using clear and concise notation. The system is easy to use. Standardized format for LCD input/output with appropriate error and warning messages enhances operation of the analyzer.

The LCD is divided into three independent sections, known as cursor zones. Access to each is achieved through the cursor control keys. The three zones are referred to as the RF Control, Audio Control, and Display zones. A message line and a softkey label area are also included.

Operator-entered information contained within CRT displays is stored in non-volatile memory. Storage is automatic; when information is changed on the CRT by the operator, the corresponding information in nonvolatile memory is also changed.

The ability to select one of 30 stored preset selections is also provided. Each has 7 parameters associated with it:

1) Monitor frequency
2) Generate frequency
3) Duplex offset
4) Modulation type (AM or FM)
5) Bandwidth (wide or narrow)
6) Audio synthesizer format (PL, DPL, Tone A, Tone B, 5/6 Tone, Tone Remote, Select V, A/B Sequence Select, General Sequence, and audio synthesizer code associated with one of these formats)
7) DTMF code (up to 16 digits)

1.4 GENERATOR/RF OUTPUT

The modulation generator provides the modulating signal source for the RF generator. The source is internally connected to either the frequency modulator or amplitude modulator as required by the operation mode. The signal source is the summation of a fixed 1 KHz sine wave, an independent external input, an internal code *synthesizer, a* DTMF Generator, and the microphone. (NOTE: when using the external input, a fixed reference input level must be maintained at the external input for accurate modulation display) Each source has a separate level adjustment (including an off position) via the front panel display.

The Generator Module output is a 310.7 ±55MHz signal that is sent to the RF Output module. The RF Output module converts the signal to the proper output frequency, It is then available at either the RF Gen Out port or the RF I/O port at the front panel via the Wattmeter Module. Output port selection is determined by the operator.

1.5 MONITOR/RF INPUT

The Analyzer can monitor RF input energy either directly from a transmitter or from an antenna, to accurately determine frequency, power level, and modulation level. The RF wattmeter is located at the RF I/C port and operates simultaneously with the Analyzer monitor function. Input port selection (front panel Antenna or RF I/O port) is determined by the operator.

WARNING

Although the RF Wattmeter is capable of accepting input levels up to 125 watts, do not use it ***for continuous*** *RF power measurements over 25 watts. Refer to System Specifications (Section 2) for RF Wattmeter duty cycle limits. An over-temperature condition will appear to the user in the form of an audible signal and onscreen warning when equipment damage is imminent.*

WARNING

DO NOT apply RF power directly to the Antenna, a port, The Antenna port is intended to be used as an antenna connection only. Equipment damage may occur if RF power is applied directly to this port This type of damage is not covered under warranty

The Analyzer decodes tone sequences, private line signals, digital private line signals, and DTMF signals to determine; the generating code (if applicable), individual tone frequencies, and tone durations. The decoder accepts signal inputs from either the internal demodulator or from the multipurpose front panel BNC input port. Selection between the signal sources is made on the front panel display.

RF input signal flow starts at either the antenna port or RF I/O port at the front panel (to the RF Wattmeter Module). The signal is then sent to the RF Input Module. From the RF Input Module the signal is sent to the Receiver and Spectrum Analyzer modules.

1.6 SPECTRUM ANALYZER

The spectrum analyzer displays the frequency spectrum from either the antenna or the RF I/O port on the LCD. The Spectrum Analyzer demodulates the signal at the center of the display and is operational up to a full scale frequency dispersion of 10MHz.

1.7 OSCILLOSCOPE

The general purpose scope is activated via the front panel display and has calibrated vertical input sensitivities and horizontal sweep rates. Automatic, normal, and single sweep trigger modes synchronize the horizontal time base to the vertical input signal.

1.8 DIGITAL VOLTMETER

The DVM is a general purpose AC and DC digital voltmeter. A three digit readout and bar graph depicting the measured voltage are displayed simultaneously. The DVM has manual or automatic ranging between three input voltage ranges (1, 10, or 70Vrms full scale) and an AC frequency range from 50Hz to 20KHz.

1.9 SINAD/DISTORTION METER

The fixed frequency automatic EIA SINAD/Distortion meter operates simultaneously with the basic generate and monitor modes.

1.10 FREQUENCY/PERIOD COUNTER

The frequency/period counter can be used over the input level range of 100mV rms to 70V rms. Sensitivity is controlled by the min/max operator selection.

NOTE A single BNC input port (Metering In) is used at the front panel for external inputs to the Oscilloscope, Digital Voltmeter, SINAD/Distortion Meter, and the Frequency/ Period Counter.

1.11 MODULE/ SUBASSEMBLY DESIGNATIONS

Al	Front Panel
AlAl	EMI Filter
A2	RF Wattmeter
A3	RF Motherboard
A4	Processor Module
A5	* Generator Module
A6	*RF Output Module
A7	* High Synthesizer Module
A8	* RF Input Module
A9	* Low Synthesizer Module
A10	* Receiver Module
All	* Spectrum Analyzer Module
A12	Interface Module
A12A2	Interface Filter Phase Demod Module
A13	Frequency Standard Module
A14	Rear Panel
A14Al	Power Supply
A15	Display Processor Module

* Indicates modules installed inside the RF Cardcage

Section 2A
SYSTEM THEORY OF OPERATION

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2.1 POWER SUPPLY

Produces the following DC voltages for other modules/subassemblies:

+5V -5V +12V -12V +40V

2.2 FREQUENCY STANDARD MODULE

When the power supply is operating properly, the Frequency Standard module can begin operating. This module converts a 10MHz reference input signal into two 10MHz output signals for the system's use.

Switch S1 (at bottom panel) allows the operator to select the source of the Frequency Standard's 10MHz input. internal or external. When S1 is switched to the Internal position, this module will provide a 10MHz output signal for the Rear Panel 10MHz IN/OUT connector.

2.2.1 Frequency Standard 10MHz Source

NOTE: The 10MHz input Signal (internal or external) must be traceable to N.I.S.T. standards.

S1 switched to Internal
The Frequency Standard gets its 10MHz input from an oscillator mounted on the Frequency Standard Module. The oscillator is an OCXO (oven compensated crystal oscillator) that is accurate to within 0.1ppm (1Hz). The RF frequency accuracy for the entire Analyzer is based upon the accuracy of the Frequency Standard's 10MHz input signal.

S1 switched to External
The Frequency Standard gets its 10MHz input from the Rear Panel 10MHz IN/OUT connector,

2.2.2 Frequency Standard Outputs

Whenever a 10MHz input signal is available, this module will produce the following output signals:

SYNTH 10MHz REF for analog/RF circuitry (such as the system's PLL loops, for example)

SYSCLK for digital timing (including the microprocessor clock)

2.3 PROCESSOR MODULE

When SYSCLK is available from the Frequency Standard Module, the Processor Module will begin executing the program stored in its ROM memory. A small battery located on this board powers RAM when power is off to allow recovery of previously stored information.

The Processor Module's primary functions are:

l) Accept operator commands entered at the keypad, and send the appropriate control signals to execute those commands.
2) Monitor the state of the Analyzer to produce information for the Liquid Crystal Display (LCD) and/or to control the Analyzer.

2.3.1 Display Processor Module (Refer to figure 2.4)

The Display Processor Module accepts operator specific information from the main Processor Module and presents it via the LCD. An LCD controller generates required control and timing signals to operate the display. A separate on board processor performs the manipulation necessary for a graphical representation of control settings, results data, waveforms, etc.

2.4 PLL LOOP PROGRAMMING(Refer to figure 2.4)

Whenever the carrier frequency is changed by the operator, the Processor Module programs all the PLL loops simultaneously in the following manner.

1) The processor's address bus is decoded as chip selects for the output latches located on the Interface Module. The data bus from the processor is buffered and sent to the Interface Module.
2) At the Interface Module, the output latches are each controlled via the data bus and the individual chip selects for the output latches. Via the output latches, the PLL data lines are controlled high or low for each PLL This is the first bit of the serial data words to each PLL
3) SYNTH CLOCK is asserted which causes all the PLLs to shift in their first data bit.
4) Each PLL data line is controlled high or low for the next serial data bit and SYNTH CLOCK is asserted again. This is repeated until the last data bit of the PLLs serial data words have been sent.
5) SYNTH LATCH is asserted to latch the serial data into all PLLs at the same time.
6) All PLLs are now programmed according to the operator-selected mode and carrier frequency.

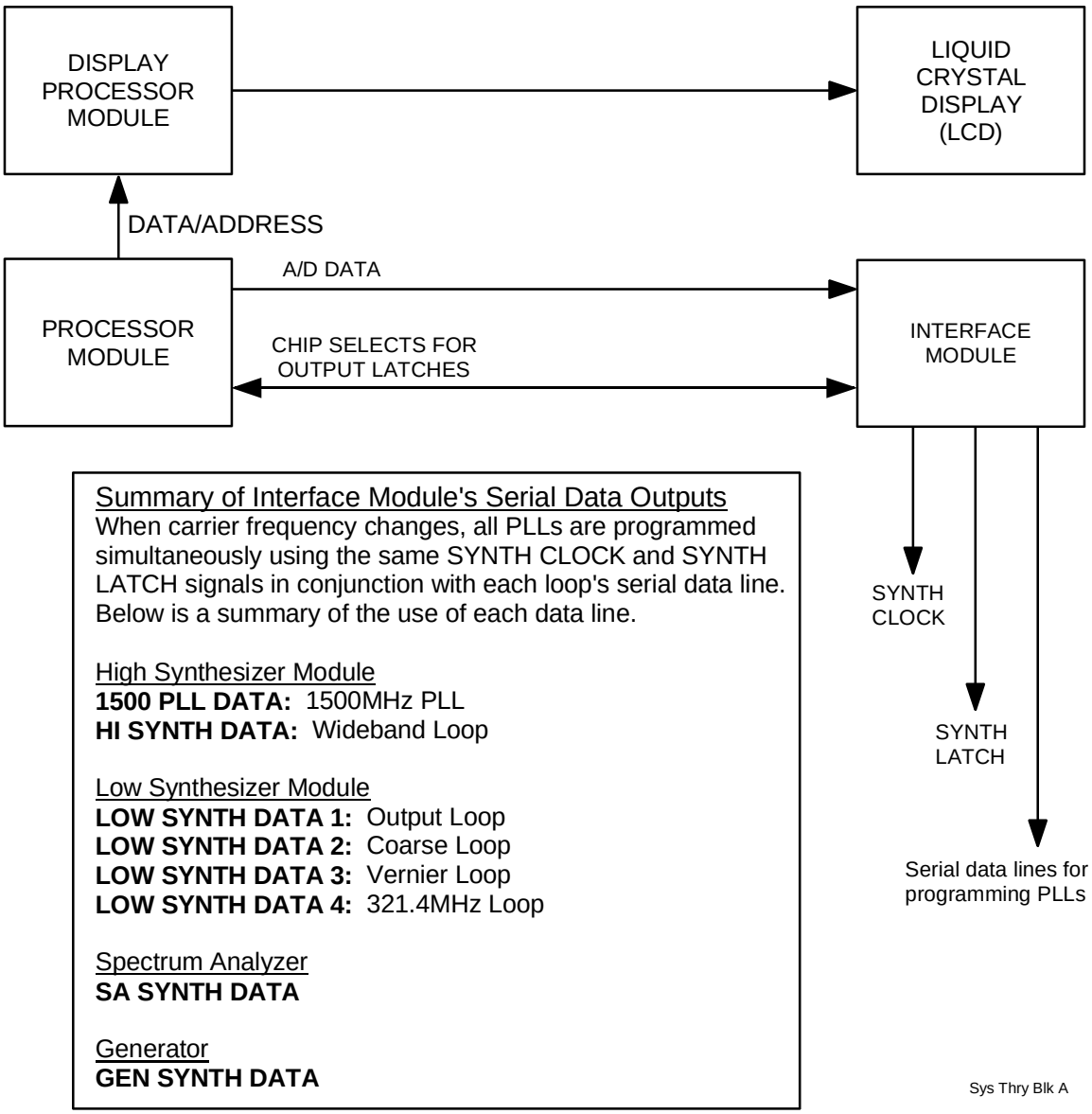

Fig. 2.4 Digital Programming of PLL Loops

2.5 LOW SYNTHESIZER MODULE

The Low Synthesizer Module utilizes 4 PLL loops to produce two output signals.

Three PLL loops (coarse, vernier, output) are used together to create the "LOW SYNTH RF' output signal. This signal used by the High Synthesizer Module. The frequency range is 100 to 119.9999MHz in 100Hz steps. The 100Hz step size for carrier frequencies is due to the Vernier loop on this module.

The fourth loop creates the "321.4 MHz RCV LO" signal. It is fixed at 321.4MHz and is sent to the Receiver Module where it is used as a local oscillator for monitor functions.

2.6 HIGH SYNTHESIZER MODULE

This module uses two PLL loops to produce 4 output signals.

The 1500MHz PLL is mixed with LOW SYNTH RF from the Low Synthesizer Module to create two output signals: 1400MHz RCV LO and 1400MHz GEN LO. The frequency range of these signals is 1390.0001 to 1400MHZ in 100Hz steps.

The Wideband PLL uses a 1500MHz signal from the other PLL loop to produce two output signals: 1st RCV LO and 1st GEN LO. The frequency range of these signals is 1710 to 2710MHz.

2.7 310.7MHz IF SIGNALS

2.7.1 Generate Mode

The Generator Module output is the modulated 310.7MHz GEN IF signal that is routed to the RF Output Module. In AM mode, it is fixed at 310.7MHz. In normal FM mode, it is 310.7MHz. In FM Duplex or Sweep Generate modes it is 310.7MHz ±55MHz in 5KHz steps.

2.7.2 Monitor Mode

The RF Input Module outputs two 310.7MHz signals. 310.7MHz RCV IF is sent to the Receiver Module for demodulation and signal measurements. The other signal is called 310.7MHz SA IF and is sent to the Spectrum Analyzer Module.

2.8 RF FREQUENCY CONVERSION

2.8.1 Monitor Mode

1. Processor programs PLL loops at the High and Low Synthesizers according to carrier frequency entered at front panel.

2. Signal from either the Antenna port or the RF I/O port is input to the RF Input module. (When the RF I/O port is selected, the RF Wattmeter sends the input signal to the RF Input Module via the CAL RF signal.) The RF Input module mixes this input signal with 1st RCV LO (1710 to 2710MHz from High Synth) to produce an on-board IF signal.

3. The on-board IF signal (1700.7001 to 1710.7MHz) is mixed with 1400MHz RCV LO (1390.0001 to 1400MHz from High Synth) to produce two 310.7MHz IF signals. One is routed to the Receiver Module (310.7MHz RCV IF) and the other is routed to the Spectrum Analyzer Module (310.7MHz SA IF).

4A. The 310.7MHz SA IF is routed to the Spectrum Analyzer Module where it eventually becomes the SIG STRENGTH signal. SIG STRENGTH is sent to the Interface Module for signal strength measurements and for processor control of the Spectrum Analyzer display functions.

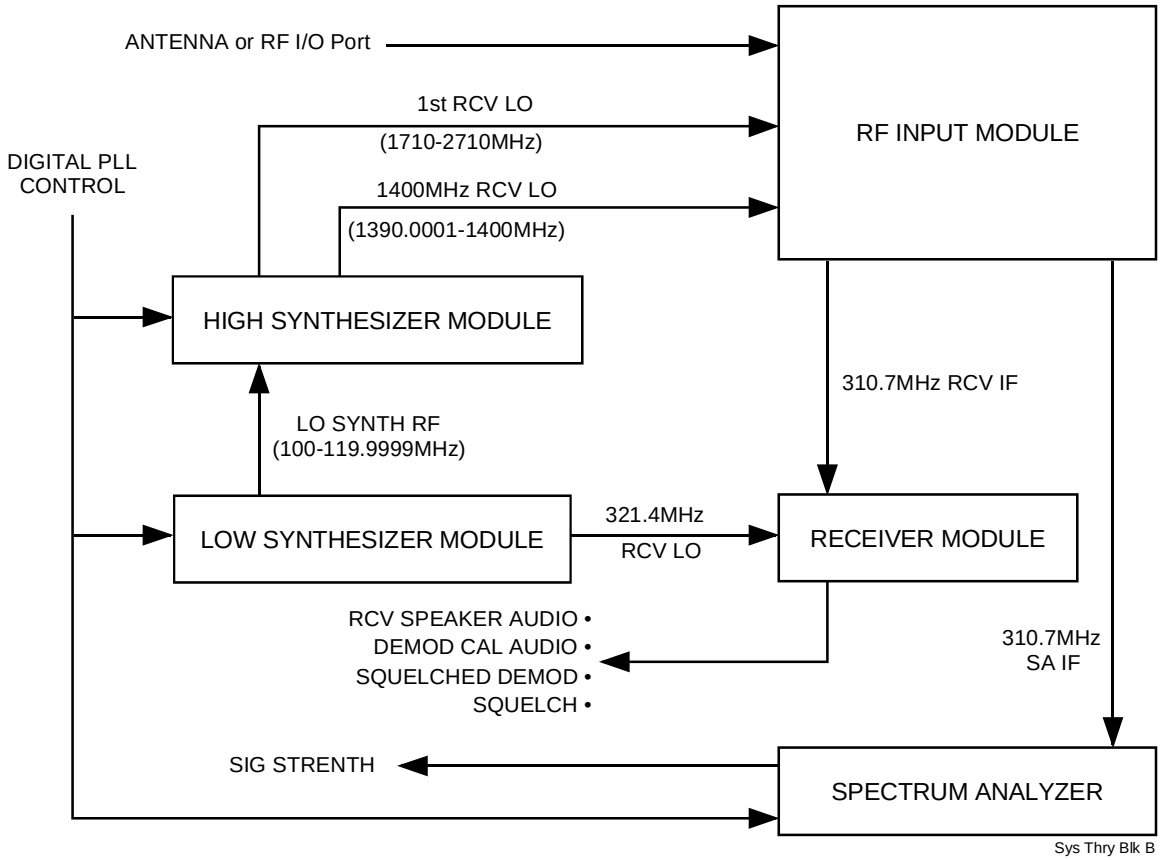

Fig. 2.8.1 Monitor Mode Frequency Conversion Major Signal Flow

4B. The 310.7MHz RCV IF routed to the Receiver Module is mixed with 321.4MHz RCV LO (from Low Synth) to create a 10.7MHz signal (NOTE: the wideband/ narrowband filters are in the 10.7MHz path).

5. The system's 10MHz reference is mixed with the10.7MHz signal at the Receiver Module to produce a 700KHz IF signal. A voltage limited version of the 700KHz IF signal is sent to the Interface Module for frequency error measurement .

6. An AM/FM receiver chip on the Receiver Module demodulates the 700KHz IF to produce a demodulated audio signal. The demodulated audio is high and low pass filtered before becoming DEMOD CAL AUDIO to the Interface Module.

7. The Processor and Interface modules then use the demodulated audio signal for the scope, tone decoding, etc. according to the current mode of operation.

2.8.2 Generate Mode

1. Processor Module provides the digital GEN AUDIO signal to the Interface Module according to the audio configuration determined by the operator. The Interface Module provides AC coupling to GEN AUDIO to create MOD CAL AUDIO, which is routed to the Generator Module.

   The Processor also programs the High and Low Synthesizer loops according to the carrier frequency entered at the front panel.

2. The Generator Module creates a modulated 310.7MHz IF signal for the RF Output Module. The Generator Module operation is determined by the modulation type (AM or FM).

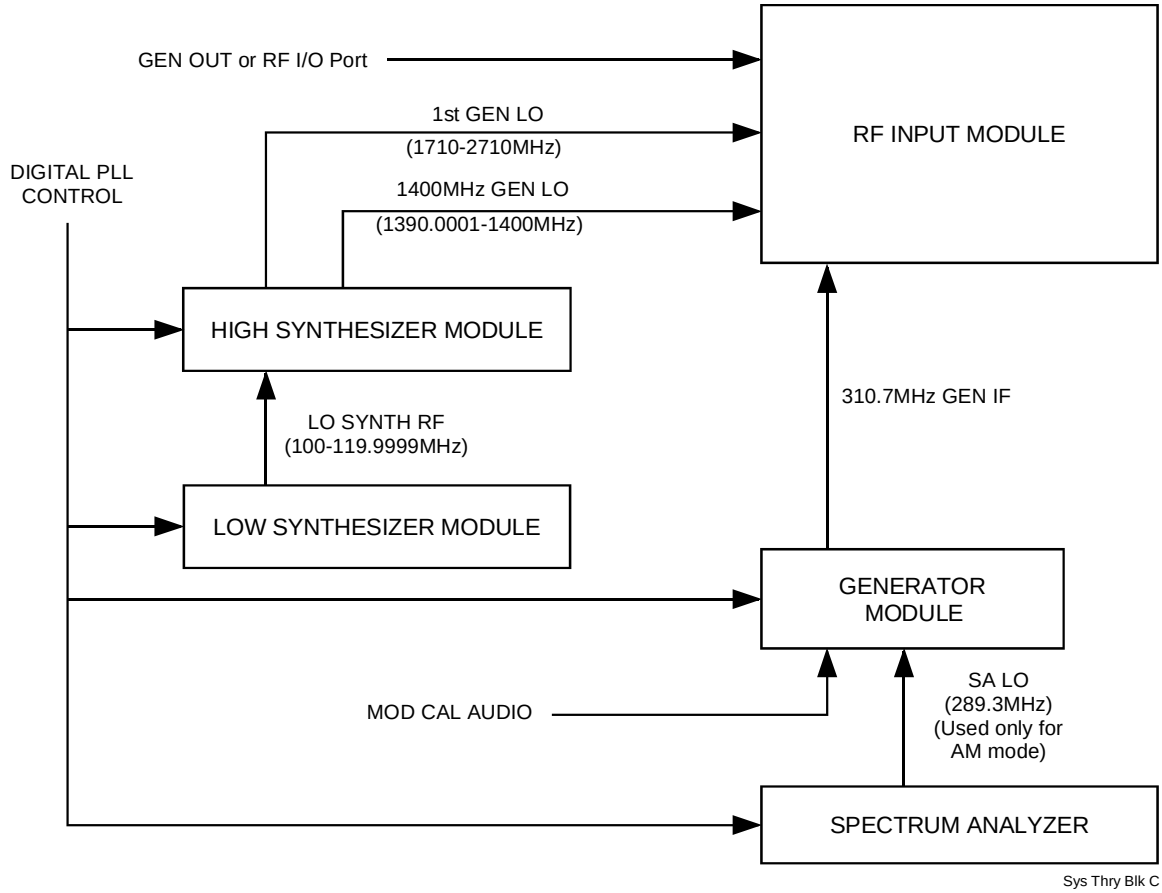

Fig. 2.8.2 Generate Mode Frequency Conversion Major Signal Flow

- FM MODE
  - The Generator conditions MOD CAL AUDIO for wideband/ narrowband, and uses it as input to a 215MHz VCO (resulting in an FM modulated 215MHz signal).
  - The PLL is Programmed to 525.7MHz (using VCO1).
  - The 215MHz and 525.7MHz signals are mixed to create the FM modulated 310.7MHz GEN IF.

- AM MODE
  - The PLL is programmed for 557.4MHz (using VCO2).
  - The 557.4MHz signal is mixed with the output of the 215MHz VCO (which is now fixed at 215MHz since FM mode is turned off). The result is an unmodulated 342.4MHz signal.
  - A divide-by-16 conversion translates the 342.4MHz signal to 21.4 MHz.
  - The 21.4MHz signal and MOD CAL AUDIO are both input to a balanced AM modulator, resulting in a 21.4MHz AM modulated signal.
  - Since the Spectrum Analyzer is not enabled during generate mode, its PLL is set to 289.3MHz and the signal is input to the Generator Module as SA LO.
  - SA LO (289.3MHz) and the 21.4MHz AM modulated signal are mixed to produce the 310.7MHz GEN IF.

3. The RF Output mixes the 310.7MHz GEN IF from the Generator Module with the 1400MHz GEN LO signal (1390.0001 to 1400MHz from High Synth) to produce a 1700.7001 to 1710.7MHz IF signal.
4. The 1700.7001 to 1710.7MHz IF signal is then mixed with 1st GEN LO (1710 to 2710MHz from High Synthesizer) to produce the desired carrier frequency.
5. The output of the RF Output Module is called GEN OUT and is routed to the RF Wattmeter.
6. The RF Wattmeter then performs the switching (under processor control) to select either the GEN OUT port or the RF I/O port.

- PM MODE

Operation is the same as in FM mode except that the audio signal is pre-emphasized on the Processor model.

2.9 MODULATION

Synthesized audio sources are created at the Processor Module. External audio input at the Front Panel is routed through the Interface Module and sent to the Processor Module where all audio is summed together

The summed audio signal is called GEN AUDIO and is sent from the Processor Module to the Interface Module. The Interface Module performs capacitive coupling to eliminate any DC offset and the signal is renamed MOD CAL AUDIO.

MOD CAL AUDIO is sent to the Generator Module where it is AM or FM modulated onto the 310.7MHz GEN IF signal.

2.9.1 FM Mode

In FM mode, the Generator's PLL loop is activated. Two VCOs are contained in the Generator's PLL. In FM Duplex and Sweep Generate modes, the 310.7MHz GEN IF signal can range from 255.7 to 365.7MHz. VCO1 is used for IF frequencies from 255.7 to 310.7MHz and VCO2 is used for IF frequencies from 310.7050MHz to 365.7MHz.

2.9.2 AM MODE

In AM mode the Generator's PLL is set to 342.4MHz. This signal is divided by 16 to create a 21.4MHz signal. The 21.4MHz signal is then AM modulated.

The Spectrum Analyzer's PLL loop is available since it is not used for display functions during generate mode. In AM generate mode, the Spectrum Analyzers PLL is set to 289.3MHz and the output signal is sent to the Generator Module as "SA LO".

SA LO (289.3MHz) from the Spectrum Analyzer and the modulated 21.4MHz signal are mixed to produce the AM modulated 310.7MHz GEN IF output signal.

2.10 DEMODULATION

(refer to the Receiver Module block diagram)

- The RF Input Module sends 310.7MHz RCV IF to the Receiver Module.
- The Low Synthesizer provides the 321.4MHz RCV LO signal that is mixed with 310.7MHz RCV IF. The result is a 10.7MHz on-board IF signal.
- Wide or narrow band filtering is then applied.
- The filtered 10.7MHz IF signal is mixed with SYNTH 10MHz REF from the Frequency Standard Module which results in a 700MHz IF signal.
- An output signal called LIM 700KHz is sent to the Interface Module at this point for frequency error measurements.
- MOD SEL 2 from the Interface Module selects AM or FM demodulation.
- The demodulated audio goes through a 5Hz high pass filter and is then split into two paths. The first path is RCV SPEAKER AUDIO for the speaker.

The. second path is sent through high and or low pass filters selected by the operator, except for a 1Hz high pass filter that remains in place at all times. The output of the second path is DEMOD CAL AUDIO and is sent to the Interface Module. The RCV SPEAKER AUDIO and SQUELCHED DEMOD, signals are the DEMOD CAL AUDIO signal that is switched in and out by SQUELCH.

2.11 SQUELCH CONTROL

A potentiometer at the Front Panel allows the operator to adjust the SQUELCH LEVEL signal between 0 and +12VDC. SQUELCH LEVEL is sent to the Processor Module where it is passed on to the Interface Module without any modification. The Interface Module then sends it directly to the Receiver Module.

The Receiver Module compares the SQUELCH LEVEL signal to the AGC voltage to determine what input signal level will break squelch. The result is the signal named SQUELCH.

The SQUELCH signal controls switches on the Receiver Module to enable or disable the RCV SPEAKER AUDIO and SQUELCHED DEMOD audio signals. SQUELCH is also sent to the Interface Module.

2.12 AUDIO GENERATION

(refer to page 4 of the Processor Module block diagram).
The Processor Module with it's ASIC performs all synthesized audio generation including setting the levels for each synthesized source. The Processor Module also sums these synthesized audio sources together to create the INT MOD signal.

The Interface Module takes the signals from the Front Panel's EXT MOD IN and MIC in connectors and sums them together to create the EXT MOD + MIC IN signal. This signal is sent to the Processor Module.

The Processor Module sums INT MOD with EXT MOD + MIC IN and audio from any hardware options (as applicable). The result is GEN AUDIO.

GEN AUDIO is sent to the Interface Module where capacitive coupling eliminates any DC offset. The signal is then renamed MOD CAL AUDIO.

MOD CAL AUDIO is sent to the Generator Module for the purpose of modulating the 310.7MHz GEN IF signal. MOD CAL AUDIO is also conditioned for WB/NB and sent to the Front Panels MOD OUT connector.

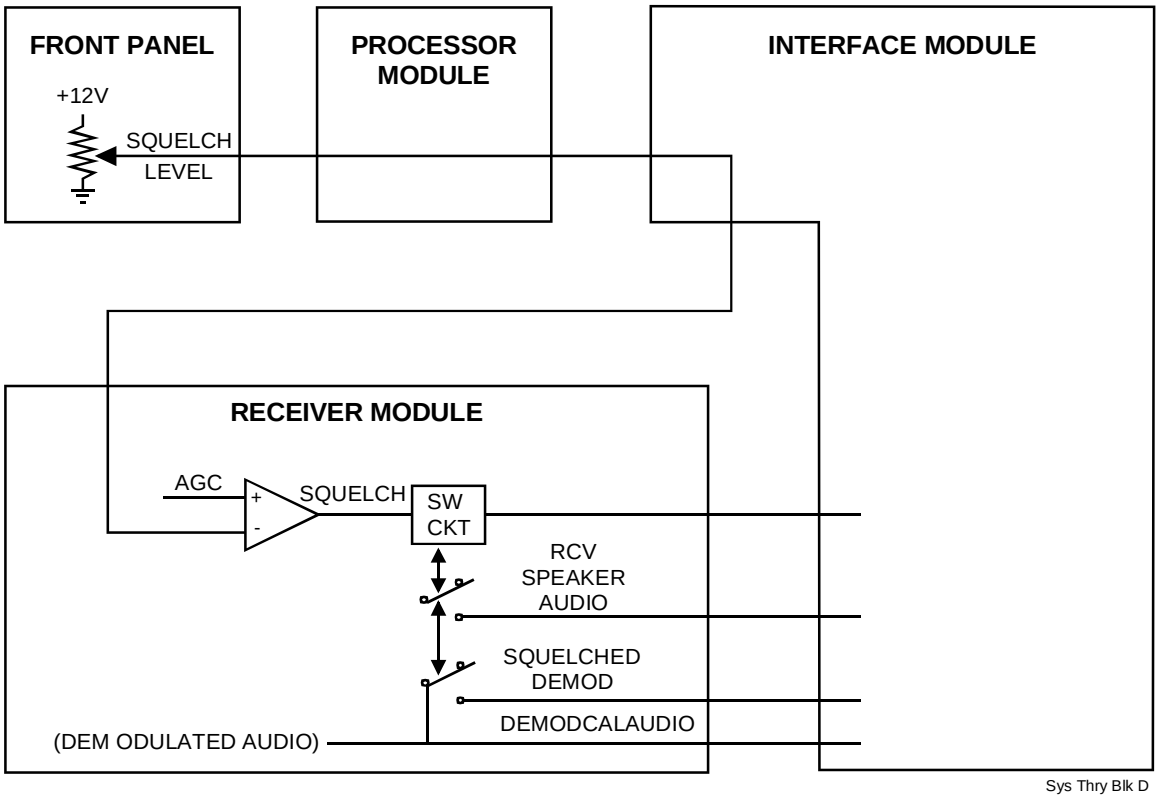

Fig. 2.11 Squelch Control

2.13 AUDIO MONITORING & METERING FUNCTIONS

(refer to page 2 of the Interface Module block diagram).

2.13.1 Pos/Neg Peak Detection Circuitry

The Interface Module receives SQUELCHED DEMOD (demodulated squelched audio) from the Receiver Module. The processor controls a MUX at the Interface Module to select either SQUELCHED DEMOD (demodulated audio) or MOD CAL AUDIO (modulation audio) for pos/neg peak detection circuitry.

2.13.2 Intemal/External Decoding

When the operator selects INTERNAL or EXTERNAL (off-the-air) decoding at the special function screen, the Interface Module selects one of two signals:

- SQUELCHED DEMOD (demodulated audio) from the Receiver Module (internal).
- The Front Panel METER IN signal (external).

The selected signal goes through DVM ranging circuitry and becomes DVM FROM RANGE. (DVM ranging selections are made under processor control according to operator selections).

2.13.3 DVM FROM RANGE Signal

The DVM FROM RANGE signal is routed to several places, including:

- A 1KHz notch filter and a rectifier/x1.1 circuit for SINAD/Distortion functions
- To a MUX where it may be selected from among other signals to become the COUNTER signal to the Processor Module. The processor (and ASIC) use the COUNTER signal to perform audio decoding for PL, DPL, Select V, 5/6 Tone, Tone A/B, General Sequence, and the frequency/period counters.
- It is sent directly to the Processor Module's DTMF decoder.

2.13.4 12-bit A/D Conversion (for Metering)

The 12-Bit A/D converter at the Interface Module is used for a variety of metering functions. At the Interface Module one of the following signals is selected (under processor control) for 12-bit A/D conversion:

- Positive peak signal from peak detector circuitry.
- Negative peak signal from peak detector circuitry.
- DC INPUT + (for monitoring battery voltage)
- The output of an RMS to DC converter. The input to this converter is either DVM FROM RANGE or the output of the 1KHz notch filter.
- The output of a Rectifier/x1.1 circuit. The input to this circuit is DVM FROM RANGE. The processor calculates % distortion of a 1KHz input signal by dividing the RMS output voltage of the notch filter by the output of the rectifier/x1.1 circuit.
- An RF DVM input signal. This may be any one of the following signals:
  - INPUT PWR DET is a voltage level that is proportional to the RF Wattmeter power level input.
  - OUTPUT PWR DET is a voltage level that is proportional to the RF Wattmeter's power level output.
  - INPUT TEMP SENSE voltage level proportional to the temperature of RF Wattmeter's input power detector.
  - OUTPUT TEMP SENSE voltage level proportional to the temperature of RF Wattmeter's output power detector.
  - SA/DVM SPARE is not used in the current version of the Analyzer.
  - SIG STRENGTH voltage level proportional to the level of the Spectrum Analyzer's 310.7MHz SA IF input.
  - SA TEMP SENSE voltage level proportional to the Spectrum Analyzers log amp.

When the 12-bit A/D converter has sampled its input and has valid data ready for the data bus on BD0-11, it generates a BUSY signal to the Interface Decode Module.

The interface Decode Module then generates a DTACK* to the Processor Module. This tells the Processor Module that valid data is available for reading at the 12-bit A/D converter.

2.13.5 8-bit A/D Conversion (for Scope functions)

At the interface Module one of the following signals is selected (under processor control):

- A ÷12 version of the METER IN input signal from the Front Panel.
- MOD CAL AUDIO (modulation audio)
- DEMOD CAL AUDIO (demodulated audio)

The selected signal is sent to scope ranging circuitry for amplification or attenuation.

Next, the signal is sent through Aliasing Filter and x4.0 Scale Factor circuitry. The output is sent to trigger control circuitry. It is also summed with an offset adjustment voltage and the output of the vertical position D/A converter.

8-bit A/D conversion is then performed on the summed signal. The outputs of the 8-bit A/D converter are A/D DATA 0-7 to the Processor Module.

2.14 REMOTE CONTROL INTERFACE

The major items of interest for operating under remote control mode are as follows:

- The Analyzer will automatically go into remote control mode whenever a valid remote control message is received at the RS-232 port (printer port).

- The RS-232 port may not be used for a printer output during the time that the Analyzer is in remote control mode because the two modes would conflict with each other. If printer output is desired, the computer which is controlling the Analyzer must ask for measuring information from the Analyzer, then use this information to produce its own printout.

- During remote control mode, a softkey at the Analyzer display allows a manual switch back to local control mode. This ability to manually switch back to local mode can be enabled/disabled via the "GM" (local lockout) remote control command.

- Once the Analyzer is operating in remote control mode, there are three ways it may be switched back to local mode:
  1) The “GL” remote control command (overrides a GM command).
  2) Power off/on of the Analyzer.
  3) Front panel softkey selection if the remote control device has not previously issued a "GM" (local lockout) disable command.

- The remote control may perform any function that can be done manually except:
  1) Memory presets (setting and using)
  2) Activating the Analyzer's print function.

- The remote control may interrogate any numeric measurement field available at the LCD.

- The command "FS" specifies protocol parameters for the RS-232 port. The controller should wait minimum of 1 second after reconfiguring the port before sending any new commands.

Section 3
SYSTEM TEST AND CALIBRATION / ALIGNMENT

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Section 3
SYSTEM TEST AND CALIBRATION / ALIGNMENT

3.1 GENERAL DESCRIPTION

The alignment procedures appearing here are presented in two parts. The first part is a system test. The second part contains alignment procedures for each of the individual modules/subassemblies. Whenever a module or subassembly has been repaired or replaced, perform the System Test Calibration/Alignment is not necessary unless the unit fails the system checkout.

NOTE

All tests and calibrations specified in this section are performed under normal ambient room temperature. The RF Attenuator should remain in the 0dB position (no attenuation) unless otherwise noted. All inputs and outputs must be loaded with the proper termination.

3.1.1 Recommended Test Equipment

The equipment listed here is recommended, but may be substituted with equipment of equal or greater accuracy. The procedures appearing in this section of the manual are based upon the use of the equipment listed below. Test equipment used must be traceable to N.I.S.T. standards.

3.2 SYSTEM TEST

The System Test must be performed whenever the Analyzer has been repaired or when any modules/subassemblies have been recalibrated. System Test may also be conducted periodically to check the validity of values appearing in the display screen.

If you are using test equipment other than the equipment specified in paragraph 3.1-1 then the substitute equipment must be at least 4 to 10 times more accurate than the specification being tested. For example, to check an output level of 0dBm ±4dB, your test equipment should be accurate to within at least 1dB and preferably to within 0.4dB. This applies only to the degree that current technology can comply with the 4-10 times accuracy rule.

Technicians familiar with the complete system test may wish to use the abbreviated quick check list (Figure 3.2) found at the end of Section 3.2.

In all of the following tests, "Unit Under Test" is abbreviated to “UUT”.

Signal Generator
- Fluke 6060B

Digital Voltmeter
- Hewlett Packard 3478A

Oscilloscope
- Tektronix 2465B

Spectrum Analyzer
- Tektronix 497P
- with tracking generator option
- OR
- Hewlett Packard 8560A
- With backing generator option

Measuring Receiver
- Hewlett Packard 8902A

RF power source at a known RF level

Power Supplies
- DC 0 to 24VDC
- AC 0 to 65VAC rms

Encode /Decode Equipment
for Code Synthesis (PL, DPL, DTMF, etc.)
- R2001D System Analyzer
- OR
- R2600A System Analyzer

NOTE

Before starting any system tests, terminate GEN OUT port into 50Ω and remove any cables at the front panel RF I/O and ANT ports, then calibrate the UUT via the front panel "CAL" button.

3.2.1 GEN OUT Port Tests

3.2.1.1 Un-modulated Output Level

1. Program UUT for generate mode, 3MHz carrier frequency, 0dBm output level, GEN OUT port, narrowband FM, modulation off (CW signal).

2. Use external measuring equipment to verify that the signal at the GEN OUT port of the UUT meets the A, B, C, and D specifications given for this test at carrier frequencies of 3,155,457,806,856, and 999.99 MHz.

3. Program UUT for -25dBm output level, AM mode, 0% modulation.

4. Use external measuring equipment to verify that the signal at the GEN OUT port of the UUT meets the B and E specifications given for this test at carrier frequencies of 3,128,398, and 999.99MHz.

5. Change output level to -80dBm. Check B and F at carrier frequencies of 3, 128,398, and 999.99MHz.

A. Output level 0dBm ±4dB

B. Carrier frequency at GEN OUT port within 10MHz frequency accuracy of UUT (±1ppm TCXO, ±0.1ppm OCXO).

C. AVG incidental AM <=1%

D. RMS residual FM <=20Hz (300Hz to 3KHz BW)
NOTE: Record value for later use.

E. Output level -25dBm ±4dB

F. Output level -80dBm ±4dB

3.2.1.2 Spurs

1. Program UUT for generate mode, carrier frequency of 3MHz, 0dBm output level, GEN OUT port, FM modulation off (CW signal).

2. Use external measuring equipment to verify that the signal at the GEN OUT port of the UUT meets the following specifications at 3, 128, 398, and 999-99MHz.
   Harmonics: <= -20dBC
   Frequency spur: <= -30dBC

3.2.1.3 AM Internal Tone Modulation

1. Program UUT for GEN OUT port, internal 1MHz tone modulation source, -6dBm output level, 5%AM.

2. Use external measuring equipment to verify that the signal at the GEN OUT port of the UUT meets the B specification given below at carrier frequencies of 3, 128, 398, and 999.99MHz.

3. Change AM modulation to 30% and check the A and C specifications given below at carrier frequencies of 3, 128, 398, and 999.99MHz.

4. Change AM modulation to 80% and check the A and D specifications given below at carrier frequencies of 3, 128, 398, and 999.99MHz.

A. Peak incidental FM <=1 KHz
Total harmonic distortion <=5%

B. Modulation index between 0 and 10%

C. Modulation index between 25 and 35%

D. Modulation index between 75 and 85%

3.2.1.4 AM External Modulation

1. Apply a 0.707±0.02Vrms 1KHz tone at the EXT MOD IN port of the UUT.

   Program UUT for GEN OUT port, EXT MOD IN modulation source, 50% EXT AM modulation, -6dBm output level, at a carrier frequency of 3MHz.

2. Use external measuring equipment to verify that the signal at the GEN OUT port of the UUT meets the following specifications:

A. Modulation index: 45 to 55%
B. Peak incidental FM: <=1KHz
C. Total harmonic distortion: <= 5%

3. Change the frequency of the externally applied 1KHz tone to 5MHz and repeat step 2, checking only the A and B specifications.

4. Change the frequency of the externally applied 5KHz tone to 10KHz and repeat step 2, checking only the A and B specifications.

3.2.1.5 FM Internal Tone Modulation

1. Program UUT for GEN OUT port, internal 1KHz tone modulation source, 0dBm output level, narrowband FM at 50Hz deviation, at a carrier frequency of 3MHz.

2. Use external measuring equipment to verify that the signal at the GEN OUT port of the UUT meets the B specification given below at carrier frequencies of 3, 155, 457, 806, 856, and 999.99MHz.

3. Change FM deviation at UUT to 3KHz. Check A, B, and C at carrier frequencies of 3, 155, 457, 806, 856, and 999.99MHz.

4. Change FM deviation at UUT to 9.95KHz. Check A, B, and C at carrier frequencies of 3, 155, 457, 806, 856, and 999.99MHz.

5. Change UUT to wideband FM at 15.5KHz deviation. Check B and D at carrier frequencies of 155, 457, 806, 856, and 999.99MHz.

6. Change FM deviation at UUT to 50KHz. Check A, B, and D at carrier frequencies of 155, 457, 806, 856, and 999.99MHz.

7. Change FM deviation at UUT to 99.5MHz. Check A, B, and D at carrier frequencies of 155, 457, 806, 856, and 999.99MHz.

A. Total harmonic distortion: <=3%
(within 300Hz to 3KHz bandwidth)

B. Peak incidental AM <= 1%
(within 300Hz to 3KHz bandwidth)

C. FM Deviation within ±5%
±25Hz, ±pk residual FM noise (narrowband)

D. FM Deviation within ±5%
±250Hz, ±pk residual FM noise (wideband)

3.2.1.6 FM External Modulation

1. Apply a 0.707 ±0.02 Vrms 1KHz tone at the EXT MOD IN port of the UUT.

2. Program UUT for GEN OUT port, EXT MOD IN modulation source, -10dBm output level, narrowband FM at 50Hz deviation.

3. Use external measuring equipment to verify that the signal at the GEN OUT port meets the B specification given below at carrier frequencies of 3, 155, 457, 806, 856, and 999.99 MHz.

4. Change FM deviation at UUT to 3KHz. Check A and B at carrier frequencies of 3, 155, 457, 806, 856, and 999-99MHz.

5. Change FM deviation at UUT to 9.95KHz. Check A and B at carrier frequencies of 3, 155, 457, 806, 856, and 999.99MHz.

6. Change UUT to wideband FM at 15.5KHz deviation.

7. Check C at carrier frequencies of 3, 155, 457, 806, 856, and 999.99MHz.

8. Repeat step 7 with FM deviation at UUT set for 50KHz and 99.5KHz, checking A and C.

A. Total harmonic distortion: <=3%
Peak incidental AM: <=1 %

B. FM Deviation within ±5%,
±25Hz, ±pk residual FM noise (narrowband)

C. FM Deviation within ±5%,
±250Hz, ±pk residual FM noise (wideband)

3.2.1.7 MIC IN/DEMOD OUT

1. Program UUT Generate mode parameters for GEN OUT port, 0dBm, 50% External AM.

   Put UUT in Monitor mode, Antenna port, AM, carrier frequency of 999MHz.

   Use the “SPF” key (special functions menu) to enable the generate mode speaker.

2. Key the microphone and speak into it. Ensure that the Analyzer automatically switches to generate mode. Voice communications should be audible at the speaker and audio should be present on the modulation scope of the UUT.

3.2.2 Antenna and DEMOD OUT Port Tests

3.2.2.1 Input Level

1. Program UUT for monitor mode, Antenna port, 3MHz carrier frequency.

   Apply a -55dBm CW signal to the Antenna port at 3MHz.

2. Top of UUT display area should read input power at -55dBm ±4dB, and carrier frequency within accuracy of UUT 10MHz frequency standard (±1 ppm TCXO, ±0.1ppm OCXO).

3. Repeat step 2 at 455MHz and 999.99MHz.

4. Increase the input level of the signal at the Antenna port to -45dBm. Change input attenuator of UUT to 20dB. UUT display should read signal power at -45dBm ±4dB.

5. Change input attenuator of UUT to 40dB. UUT display should read signal power at -45dBm ±4dB.

3.2.2.2 DEMOD OUT FM, Baseband, Audio Filters

1. Program UUT for monitor mode, narrowband FM monitor frequency of 3MHz. On R2600 only, enable the 300Hz highpass and 3KHz lowpass filters.

   Apply a -55dBm FM signal, 1KHz modulation tone, 0.4KHz deviation, at 3MHz to the Antenna port. This test will refer to the 1KHz modulation tone as "tone X'.

2. Check A, B, C, E, and G at 3, 398, and 999MHz.

3. Change deviation of input signal at Antenna port to 5KHz. Check D, E, and H at 3, 398 and 999MHz.

4. Program UUT for wideband FM and change deviation of input signal at Antenna port to 30KHz. Check D, F, and I at 3, 398, and 999MHz.

5. Change deviation of input signal at Antenna port to 75KHz. Check D, F, and J at 3, 398, and 999MHz.

NOTE

Perform steps 6-9 only for the R2600 analyzer.

6. Gradually decrease the frequency of tone X while measuring the output level of the DEMOD OUT port. When the output level of the DEMOD OUT port has decreased to 70% of the value recorded in step 5J, tone X should be between 250 and 350Hz (lower 3dB cutoff frequency).

7. At the UUT, disable the 300Hz highpass filter and enable the 5Hz highpass filter. The output level of the DEMOD OUT signal should return to the value recorded in step 5J (±5%).

8. Gradually increase the frequency of tone X while measuring the output level of the DEMOD OUT port. When the output level of the DEMOD OUT port has decreased to 70% of the value recorded in step 5J, tone X should be between 3 and 4KHz (upper 3dB cutoff frequency).

9. At the UUT, disable the 3KHz highpass filter and enable the 20KHz highpass filter. The output level of the DEMOD OUT signal should return to the value recorded in step 5J (±5%).

A. Measured input level at UUT is -55dBm: ±4dB.

B. Measured carrier frequency at UUT is within 10MHz accuracy of UUT (±1 ppm TCXO, ±0. 1 ppm OCXO)

C. Audio frequency at DEMOD OUT port = 1 KHz ±2Hz

D. Harmonic distortion at DEMOD OUT port <=6%.

E. Measured deviation at UUT is within ±5%, ±25Hz (narrowband).

F. Measured deviation at UUT is within ±5%, ±250Hz (wideband).

G. DEMOD OUT Port, output level 0.226 ±0.03Vrms.

H. DEMOD OUT Port output level 2.83 ±0.19Vrms.

I. DEMOD OUT Port, output level 1.7 ±0.lVrms.

J. DEMOD OUT Port, output level 4.24 ±0.226Vrms.
(NOTE: record the actual measured value for later use)

3.2.2.3 DEMOD OUT, FM Sensitivity

1. Program UUT for monitor mode, narrowband, monitor frequency of 3MHz, Antenna port, FM. If Analyzer is an R2600 model, enable the 300Hz highpass and 3KHz lowpass filters.

   Apply a -101dBm FM signal (2uV), 1KHz modulation tone, 3KHz deviation, at 3MHz to the Antenna port.

3. Measure the demodulated audio signal at the DEMOD OUT port. The SINAD level of this audio signal should be >= 10dB when carrier frequency is 3, 398, and 999MHz.

3. Program UUT for wideband FM, monitor frequency of 3MHz, with 300Hz highpass and 3KHz lowpass filters enabled.

   Apply a -87dBm FM signal (10uV), 1KHz modulation tone, 50KHz deviation, at 3MHz to the Antenna port.

4. Measure the demodulated audio signal at the DEMOD OUT port. The SINAD level of this audio signal should be >= 10dB when carrier frequency is 3, 398, and 999MHz.

3.2.2.4 DEMOD OUT, AM

1. Program UUT for monitor mode, monitor frequency of 3MHz, AM. If Analyzer is an R2600 model, enable the 300Hz highpass and 3KHz lowpass filters.

   Apply a -50dBm AM signal, 1KHz modulation tone, 10% modulation, at 3MHz to the Antenna port.

2. Check specifications A, B, C, and E at 3, 398, and 999MHz.

3. Change input signal at the Antenna port to 30% modulation. Check B, D, and F at 3, 398, and 999MHz.

4. Change input signal at the Antenna port to 70% modulation. Check B, D, and G at 3, 398, and 999MHz.

A. Measured carrier frequency at UUT within 10MHz frequency accuracy of UUT (±1ppm TCXO, ±0.1ppm OCXO).

B. Measured AM modulation within 5% above/below actual % modulation

C. DEMOD OUT audio frequency at UUT 1KHz ±0.1Hz

D. Harmonic distortion at DEMOD OUT <= 6%

E. DEMOD OUT output level 0.57 ±0.28Vrms

F. DEMOD OUT output level 1.7 ±0.28Vrms

G. DEMOD OUT output level 3.96 ±0-28Vrms

3.2.2.5 Spectrum Analyzer

1. Program UUT for monitor, carrier frequency of 3MHz, Spectrum Analyzer mode (20KHz/div).

   Apply a -50dBm CW signal at 3MHz to the Antenna port.

2. Check A and B at 3, 398, and 999MHz.

3. Change the Spectrum Analyzer setup of the UUT to 100KHz/division. Repeat step 2.

4. Change the Spectrum Analyzer setup of the UUT to 1MHz/division. Repeat step 2.

5. Change applied carrier frequency to 4MHz above, then below 398MHz. Ensure that signal at UUT Spectrum Analyzer display moves above and below center frequency by 4MHz ±1 minor horizontal division.

6. Modulate the input signal with a 1KHz modulation tone, 10KHz deviation. Change display mode to modulation scope. The 1KHz demodulated audio tone should be displayed on the LCD and heard on speaker.

A. Measured signal level at UUT is -50dBm (Spectrum Analyzer display ±4dB , Antenna ±4dB) Frequency spur <=40dBC

B. Verify that the fundamental signal is at the center of the LCD±1 minor division.

3.2.3 RF I/O Port Tests

3.2.3.1 Input, Low Power

1. Program UUT for monitor, carrier frequency of 3MHz, monitor RF I/O port.

   Apply a -45dBm CW signal at 3MHz to the RF I/O port.

2. Check A at 3, 398, and 999MHz.

3. Change input level of signal at RF I/O port to 0dBm. Check A at 3, 398, and 999MHz.

4. Change the input signal at the RF I/O port to +10dBm, 41MHz carrier, wideband FM, 1KHz modulation tone, 30KHz modulation. Program UUT to monitor this signal. Check B and C at carrier frequencies of 41, 111, and 797MHz.

A. Measured signal level at UUT is within ±4dB

B. Measured carrier frequency at UUT within 10MHz frequency accuracy of UUT (±lppm TCXO, ±0.1pprn OCXO)

   Measured frequency deviation at UUT within 5%, ±250Hz, ± peak residual FM noise.

C. DEMOD OUT total harmonic distortion <= 3%

3.2.3.2 Output

1. Program UUT for generate mode, carrier frequency of 3MHz, RF I/O port, -50dBm CW signal.

2. Measure the RF signal level at the RF I/O port with external measuring equipment. Signal level at RF I/O port should be –50dBm ±2dB. Check signal level again at carrier frequencies of 398 and 999MHz.

3.2.3.3 Wattmeter

1. Apply a CW (unmodulated) RF signal at a known RF level up to 125 watts (+5ldBm) to the RF I/O port with UUT configured to monitor this signal. It may be necessary to enable UUT attenuation.

WARNING

*The maximum allowable input power is 125 Watts, but this is at **no more than a 20% duty cycle** (max 1 minute out of five minutes). Do not use the RF Wattmeter for continuous input over 25 Watts to avoid circuit damage.*

2. Input power reading at UUT should be within ±0.4dBm of the actual input level at the RF I/O port.

3.2.4 Duplex Tests

3.2.4.1 GEN OUT / Antenna

1. Program UUT as follows:
   RF Control: DUPLEX
   Preset: -- -- B/W:WB
   Mon Freq: 398.0000 MHz
   Offset: +00.010 MHz
   Mon: 0dB ANT
   Gen: -006.5dBm GEN

   Mod Sum: 75.0 KHz
   Fixed 1 KHz: 75.0 KHz

   Apply -70dBm, 398MHz carrier, FM, 1KHz modulation tone, at 3KHz deviation, to the Antenna port.

2. Check A, B and C at the GEN OUT port Check D at the DEMOD OUT port.

3. Repeat step 2 with UUT offset of +1.1MHz, and again at +55MHz offset.

4. Change the FM deviation of the input signal at the Antenna port to 15.5KHz and repeat steps 2 and 3.

5. Change the FM deviation of the input signal at the Antenna port to 99KHz and repeat steps 2 and 3.

A. AVG signal level at GEN OUT port is -6.5dBm ±4dB

B. Deviation frequency ±5%, ±250Hz, ± peak residual FM noise

C. Peak incidental AM is <= 1 %

D. Total harmonic distortion <=3%

3.2.4.2 GEN OUT/ RF I/O

1. Program UUT as follows:
   RF Control: DUPLEX
   Preset: -- -- B/W: WB
   Mon Freq: 398.0000 MHz
   Offset:+00.010 MHz
   Mon: 0dB RF I/O
   Gen: -011.0dBm GEN
   Mod Sum: 75.0 KHz
   Fixed 1 KHz: 75.0 KHz

Apply -45dBm, 398MHz carrier, FM, 1KHz modulation tone, at 3KHz deviation, to the RF I/O port.

2. Check A, B and C at the GEN OUT port. Check D at the DEMOD OUT port.

3. Repeat step 2 with UUT offset of +1.lMHz, and again at +55MHz offset.

4. Change the FM deviation of the input signal at the RF I/O port to 15.5KHz and repeat steps 2 and 3.

5. Change the FM deviation of the input signal at the RF I/O port to 99KHz and repeat steps 2 and 3.

A. AVG signal level at GEN OUT port is -11dBm ±4dB

B. Deviation frequency ±5%, ±250Hz, ± peak residual FM noise

C. Peak incidental AM is <=1 %

D. Total harmonic distortion <= 3%

3.2.5 Frequency Standard Test

1. Measure the output level of the 10MHz IN/OUT port at the rear panel. It should be >0dBm into 50Ω.

2. Set the UUT 10MHz IN/OUT switch to input mode and apply a precision 10MHz, ±lppm, -10dBm signal to the 10MHz IN/OUT connector at the rear panel of the UUT.

3. Program UUT for generate mode, GEN OUT port, 100MHz, CW 0dBm. Measure the frequency error at the GEN OUT port. It should be within ±1ppm.

4. Remove the 10MHz input signal from the 10MHz IN/OUT port at the rear panel. Return the selection switch to output mode.

3.2.6 METER IN Port Tests

NOTE

Ensure that the proper selection has been made at the special functions screen for internal/external metering during these tests. Set for external metering.

3.2.6.1 DVM, DC Measurements

1. Program UUT for DVM mode, DC, 1V full scale. Apply a +0.9VDC signal to the Metering Input port of the UUT. Check A. Repeat this step with -0.9VDC.

2. Change UUT to 10V fall scale, and apply a +9.0VDC signal. Check A.

3. Change UUT to 100V full scale, and apply a +24VDC signal. Check A.

4. R2600 models only: repeat steps 1, 2, and 3 with UUT in auto scale.

A. Reading at UUT±1%, ±1 least significant digit

3.2.6.2 DVM, AC Measurements

1. Program UUT for DVM mode, AC, 1V full scale. Apply a 0.5Vrms signal at 100Hz to the Metering Input port of the UUT. Check A.

2. Change UUT to 10Vrms full scale, and apply a 4.0Vrms 1KHz signal. Check B.

3. Change UUT to 70Vrms full scale, and apply a 65Vrms 60Hz signal. Check C.

4. R-2600 models only: repeat steps 1, 2, and 3 with UUT in auto scale.

A. Reading at UUT is 0.5Vrms ±0.025Vrms

B. Reading at UUT is 4.0 ±0.2Vrms

C. Reading at UUT is 65 ±3.25Vrms

3.2.6.3 SINAD/Distortion Meter

1. Setup UUT for generate mode, narrowband FM, internal 1KHz modulation tone set for 7.5KHz deviation and enable the display for SINAD meter.

   Setup UUT Tone A frequency to 2KHz and 1.88KHz deviation. Leave Tone A function off at this time.

2. Connect the MOD OUT port to the Meter In port at the front panel. SINAD reading should be between -45dB and -25dB. Switch UUT to Distortion Meter. Reading should be <1%.

3. Without disturbing the internal 1KHz settings, put Tone A into continuous mode. Distortion reading should be 25% ±2%. SINAD reading should he -12dB ±ldB.

3.2.6.4 Frequency Counter (R2600 Models Qnly)

1. Program UUT for frequency counter mode, maximum vertical sensitivity 0.1Hz resolution. Apply a Sine wave 2Vrms, at 10Hz to the Meter In port of the UUT. Check A.

2 Check A again with input signal frequencies of 1KHz and 20KHz.

3. Change UUT to 1Hz resolution. Perform check B at input signal frequencies of 10Hz, 5KHz, 100KHz, and 500KHz.

4. Change UUT resolution to auto scale. Check C at input signal frequencies of 10Hz, 1KHz, 5KHz, 20KHz, 100KHz, and 500KHz.

A. Frequency reading at UUT within ±0.1 Hz

B. Frequency reading at UUT within ±1 Hz

C. Frequency reading at UUT within ±10 Hz

3.2.6.5 PL, DTMF, DPL Decode

1. Program UUT for PL decode. Apply the following PL tones to the Meter In port and verify that the UUT decodes the correct PL codes:

67.0Hz (XZ), 103.5Hz (1A), 141.3Hz (4A), 250.3Hz(M7)

2. Program UUT for DTMF decode. Apply the following DTMF tone sequence (with 0.4 sec duration for each tone) to the Meter In port and verify that the correct DTMF codes are decoded at the UUT.

"#0123456789*ABCD"

3. Program UUT for DPL decode. Apply the following DPL codes to the Meter In port and verify that the UUT correctly decodes the DPL codes:

032, 114, 245, 431, 664

3.2.6.6 Oscilloscope

1. Program UUT for external scope mode, 200mV/div vertical, 20usec/div horizontal, automatic trigger. Center the middle vertical position. Apply a 0.8Vpp, 25KHz sine wave to the Meter In Port.

2. Verify that the signal is centered on the UUT LCD, continuously triggered, with pk amplitude at ±2 divisions vertical (±1 minor division), and signal period of 2 divisions horizontal (±1 minor division).

3. Change input signal to 1.0V pk, 1KHz sine wave. Change UUT to 500mV/div vertical, 500usec/div horizontal. Repeat step 2.

4. Add a +0.5VDC offset to the input signal and verify that trace remains the same as before, except +1 major vertical division.

3.2.7 MOD OUT Port Tests

3.2.7.1 Tone A& B

1. Program UUT for generate mode, GEN OUT port, -8.5dBm, 799MHz, wideband FM, 49KHz deviation, with Tone A frequency of 169.8Hz.

2. Check A and B at Tone A frequencies of 169.8Hz, 5.4012KHz, and 19.9995KHz.

3. Repeat step 2 with Tone B mode.

A. Frequency at MOD OUT within ±0.01 %

B. Output level at MOD OUT 2.77 ±0.35Vrms

3.2.7.2 DTMF, DPL Encode

1. Program UUT for generate mode, narrowband FM, GEN OUT port, -5.5dBm, 799MHz, 9KHz deviation, DTMF output. Program DTMF for "*0123456789ABCD" with 0.1 sec durations, 0.05 seconds delay for each sequence.

2. Use external decoding equipment at the MOD OUT port to verify that UUT sends the correct DTMF tones.

3 Program UUT for DPL output. Use external decoding equipment at the MOD OUT port to verify that the UUT sends the following DPL codes correctly.

023, 134, 306, 631, 734

3.2.8 VGA Port

Program UUT for monitor mode, any function. Connect the VGA monitor to the UUT. Verify that the VGA monitor displays the same data as on the LCD of the UUT.

R2600 System Test Quick Checklist

GEN OUT Port Tests

- ❑ 1. Un-modulated output level, frequency, incidental AM, residual FM
  (Record residual FM rms value _____)
- ❑ 2. Un-modulated harmonics, spurs
- ❑ 3. AM and FM modulation, internal and external
- ❑ 4. MIC IN / DEMOD OUT

ANTENNA Port Tests

- ❑ 5. Un-modulated input level, frequency accuracy, attenuators
- ❑ 6. FM, DEMOD OUT, Audio Filters
  (Record 3.2.2.2, step 5J value _____)
- ❑ 7. DEMOD OUT FM Sensitivity, DEMOD OUT AM
- ❑ 8. Spectrum Analyzer signal level, frequency accuracy.

RF I/O Port Tests

- ❑ 9. Low Power Input
- ❑ 10. Output
- ❑ 11. High Power Input (RF Wattmeter)

DUPLEX Tests

- ❑ 12. GEN OUT, Antenna
- ❑ 13. GEN OUT, RF I/O

❑ **FREQUENCY STANDARD Tests**

METER IN Port Tests

- ❑ 14. AC and DC DVM Measurements
- ❑ 15. SINAD, Distortion Meter
- ❑ 16. Frequency Counter
- ❑ 17. PL, DTMF, DPL Decode
- ❑ 18. Oscilloscope

❑ **MOD OUT Port Tests**

- ❑ 19. TONE A, TONE B
- 20. DTMF, DPL Encode

❑ **VGA Port**

Fig 3.2 System Test Quick Checklist

3.3 MODULE/SUBASSEMBLY ADJUSTMENTS

The procedures appearing here are for a complete, extended alignment. Most Analyzers never require such an extensive effort to calibrate them. Generally, adjustments should not be made unless out of tolerance.

In most cases, only the basic alignment procedure is required to calibrate the unit.

Before attempting any adjustments to individual module/subassemblies, allow sufficient warm-up time for the 10MHz frequency standard to stabilize. Also, perform all adjustments at normal room temperature.

Recommended measurement equipment appears on page 3-3. If substitute equipment is used, it must be capable of equal or greater accuracy than the equipment on page 3-3. As a general rule, measurement equipment should be at least 4 to 10 times more accurate than the tolerance of the specification being tested. For example, if a signal resolution is ±10%, the measurement equipment must be accurate to at least ±4% and preferably to within 1%. This rule applies only to the accuracy permitted by the current level of technology.

Figure 3.3 at the end of this section illustrates the general locations of adjustments for each adjustable module.

BASIC ALIGNMENT PROCEDURE

Perform the following checks/adjustments (adjust only if necessary) for a basic alignment The bullet symbol (•) has been added where these steps appear in the extended alignment procedure text as a convenience to the reader.

3.3.1	Power Supply
3.3.2	Frequency Standard
3.3.4.3	Reference spurs
3.3.6.1	Steps 5 and 6 only
3.3.6.2	AGC Adjustment
3.3.6.3	AM/FM Demod Level Adjustment
3.3.6.4	Squelched Demod Offset Adjustment
3.3.8.5	Loop Operation
3.3.8.6	FM Deviation Level
3.3.8.8	AM Modulation Sensitivity Adjust
3.3.10.2	DTMF Encode Level
3.3.10.3	Internal 1KHz Level

EXTENDED ALIGNMENT PROCEDURE

Performing an extended alignment procedure entails following all the procedures appearing in this section of the manual. The extended alignment procedure is rarely needed and possibly may never be required for a particular Analyzer. The adjustment procedures that appear here should be performed in the order given, since many adjustments rely on previously adjusted signals. The order of extended system calibration is:

Power Supply
10MHz standard
Low Synthesizer
High Synthesizer
RF Input and Receiver
Spectrum Analyzer
Generator and RF Output
Processor Module
Interface Module
Perform System Checkout Procedure

• 3.3.1 Power Supply

Adjust R40 for +12VDC ±300mV at J2 pin 10. (NOTE: access to the +12VDC measurement is easier at the Processor Module J7 pin 2)

• 3.3.2 Frequency Standard

1. Remove bottom cover of Analyzer to gain access to the Frequency Standard Module.

2. Ensure that switch S1 (10MHz IN/OUT) is in the internal position.

3. Check the SYSCLK voltage at J1-9. It should be 2.5Vpp ±0.5V.

4. Check the high and low swing voltages for SYNTH 10MHz REF at J2. Low <=0.5VDC, High >=4.0VDC.

5. Remove the slotted scew cap from the OCXO housing. Monitor the frequency at the 10MHz IN/OUT rear panel connector. Ensure that the frequency can be adjusted 350Hz above and below 10MHz with the oscillator adjustment.

6. Ensure the the frequency standard has been operating for at least 25 minutes. Adjust oscillator for 10MHz ±10Hz at the 10MHz IN/0UT rear panel connector. Replace the slotted scew cap.

7. Check the rear panel 10MHz IN/OUT port for: Level>=250mVrms (1dBm) into 50Ω, and harmonics are <=-26dBc.

8. Put switch S1 (10MHz IN/OUT) to the external position and apply a 10MHz ±100Hz signal at 70mVrms (-10dBm) ±10mV to the rear panel 10MHz IN/OUT port.

9. Check the SYSCLK signal at JI-9 for the following: Frequency = 10MHz ±100Hz, Amplitude >=2Vpp.

10. Return switch S1 to the internal position and reinstall the Analyzer bottom cover.

3.3.3 Low Synthesizer

NOTE

This module does not contain any field adjustable components, but output signals must be checked prior to adjusting other modules.

NOTE

The following checks for frequency, output level, and residual FM are all made with measuring equipment in a 300Hz to 3KHz bandwidth using "average" mode.

1. Test the 321.4MHz RCV LO signal at J2 for the following (into 50Ω nominal impedance):
   Frequency: 321.4MHz ±4KHz
   Output Level: -2dBm ±2dB
   Residual FM: 20.0Hz max

2. Setup UUT for monitor mode, 459.3MHz carrier. Check the LOW SYNTH RF signal at J1 (into 50Ω impedance) for the following:
   Output Level: -2dBm ±2dB
   Residual FM: 10.0Hz max

UUT Carrier Freq	J1 Frequency (±2KHz)
459.3MHz	100.0MHz
464.3MHz	105.0MHz
469.2999MHz	109.9999MHz

3. Repeat step 2 with UUT in generate mode.

3.3.4 High Synthesizer

NOTE

This module does not contain any field adjustable components, but output signals must be checked prior to adjusting other modules.

Install the High Synthesizer Module on an extender card. Use ribbon cable extenders and RF cable extenders as necessary to reconnect module to the Analyzer. Power on UUT. Allow enough time for the 10MHz standard to stabilize before starting adjustments.

3.3.4.1 1400MHz VCO Checkout

1. For each of the following carrier frequencies, check J4 and J5 for an output level of +2.0dBm ±2.5dB and frequencies indicated:

UUT Carrier Freq	J4 and J5 Freq (±20KHz)
9.3MHz	1400MHz;
14.3MHz	1395MHz
19.2999MHz	1390.0001MHz

3.3.4.2 Loop Operation

Program UUT for monitor mode and carrier frequencies indicated below. For each carrier frequency, check the following:

J1 frequency within ±10KHz

J1 output level of -3dBm to +4dBm

Carrier	J1 (1st RCV LO) Freq
9.3MHz	1720MHz
19.29999MHz	1720MHz
89.3MHz	1800MHz
219.3MHz	1930MHz
349.3MHz	2060MHz
489.3MHz	2200MHz
649.3MHz	2360MHz
839.3MHz	2550MHz

• 3.3.4.3 Reference Spurs

1. Setup UUT for monitor mode and check spurs at J3 and J4 when UUT is programmed for carrier frequencies of 9.3MHz, 479.3MHz, 489.3MHz, and 999.3MHz.

   Spur frequencies at 200KHz, 1.25MHz, 2.5MHz, 5MHz and 10MHz should all be <=60dBc at J3 and J4.

2. Power off UUT. Return High Synthesizer Module to its normal installation.

3.3.5 RF Input

Power off UUT and install the RF Input Module on an extender card. Use ribbon cable extenders and RF cable extenders as necessary to reconnect module to the Analyzer. Power on UUT.

3.3.5.1 310.7MHz Bandpass Filter Alignment

1. Set up UUT for monitor mode, Antenna port, 310.7MHz, 40dB attenuation.

2. Apply a 260 to 360MHz swept signal at -40dBm, to the Antenna Port.

3. Monitor J5 (310.7MHz RCV IF) and adjust C59, C65, C72, and C88 for the response shown in figure 3.3.5.1.

NOTE

Swept signal applied at Antenna port should be in sync with measurement device monitoring J5.

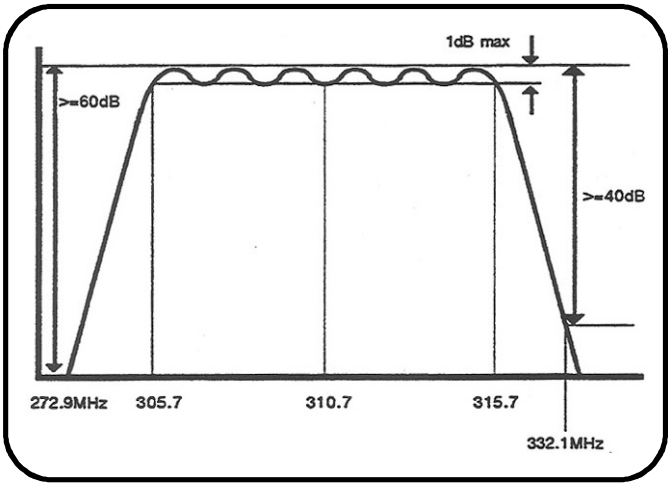


Fig 3.3.5.1 310.7MHz RCV IF BPF Response

3.3.5.2 Attenuator Accuracy

1. Setup UUT for monitor mode, 100MHz, no attenuation (0 dB). Apply a 100MHz CW signal at -40dBm to the Antenna port.

2. Record the output level of J5 at 310.7MHz.

3. Setup UUT for 20dB attenuation. Output level at J5 should drop 20dB ±l.3dB from the value recorded in step 2.

4. Setup UUT for 40dB attenuation. Output level at J5 should drop 20dB ±l.3dB from the value recorded in step 3.

5. Repeat steps 1 through 4, except with carrier frequencies of 500Mhz and 900MHz.

3.3.5.3 1dB Compression Point

1. Set up UUT for monitor mode, 990MHz, no attenuation (0dB). Apply a 990MHz -45dBm signal to the Antenna port while monitoring the output level at J5.
2. Increase the RF level into the Antenna port in 1dB steps until the gain measured at J5 has decreased 1dB from its linear response (ie, 1dB compression point). The RF input level at the Antenna port should be greater than -35dBm at the 1dB compression point.

3.3.5.4 Spurious and Rejection

1. Set up UUT for monitor mode, 10MHz, no attenuation (0dB), front panel Antenna port terminated into 50Ω.

2. The 320.7MHz spur at J5 should be less than -8dBm.

3. Change UUT monitor frequency to 50MHz. The 320.7MH.z spur at J5 should be less than -8dBm.

3.3.5.5 310.7MHz SA IF Output level

1. Set up UUT for monitor mode, 500MHz, no attenuation (0dB).

2. Apply a 500MHz, -40dBm signal to the Antenna port and record the 310.7MHz output level at J5.

3. Move the input signal at the Antenna port to J2 (CAL RF) and terminate the Antenna port into 50Ω.

4. The Output level at J6 (at 310.7MHz) should be equal to the level recorded in step 2 ±2dB).

   Power off UUT and return RF Input Module to its normal installation.

3.3.6 Receiver

Power off UUT and install the Receiver Module on an extender card. Use ribbon cable extenders and RF cable extenders as necessary to reconnect module to the Analyzer. Disconnect J1, J2 and terminate each input with 50Ω. Power on UUT.

• 3.3.6.1 10.7MHz Filter Check and Alignment

1. Set up UUT for monitor mode, Antenna port, 500MHz, wideband FM, 5Hz highpass and 20KHz lowpass audio filtering.

2. Defeat the AGC by connecting TP146 to a 1KΩ resistor to ground. Apply a 10.7MHz signal swept ±400KHz at -80dBm into TP182.

3. Monitor TP63 for the response shown in figure 3.3.6.1A. This is a check only, no adjustment is available. in wideband mode (NOTE: swept signal at TP182 should be in sync with measurement device monitoring TP63).

4. Change UUT to narrowband. Adjust C15, C16, C17, and C19 for a filter response at TP63 that has a flat middle with maximum signal level.

5. Remove the 10.7MHz swept signal from TP182 and remove the resistor from TP146. Apply a 310.7MHz signal at -50dBm, modulated by a 1KHz tone, 3KHz deviation to J1 (310.7 RCV IF). Reconnect J2 (321.4MHz RCV LO). Enable the 300Hz highpass and 3KHz lowpass audio filters at UUT.

6. Turn R89 fully CW (do not let the potentiometer armature go into its "dead zone"). Fine tune C15, C16, C17, and C19 for maximum SINAD at the front panel DEMOD OUT port.

7. Remove connections to J1 and J2 (terminate into 50Ω). Set up UUT for 5Hz highpass and 20KHz lowpass audio filtering. Defeat the AGC by connecting TP146 to a 1KΩ resistor to ground. Apply a 10.7MHz signal swept ±400KHz at a level of -80Bm into TP182 again.

8. Response at TP63 should now meet parameters shown in figure 3.3.6.1B (NOTE: If responses do not have shoulders as in diagrams below, take readings relative to the maximum amplitude).

9. Reconnect J1 and J2.

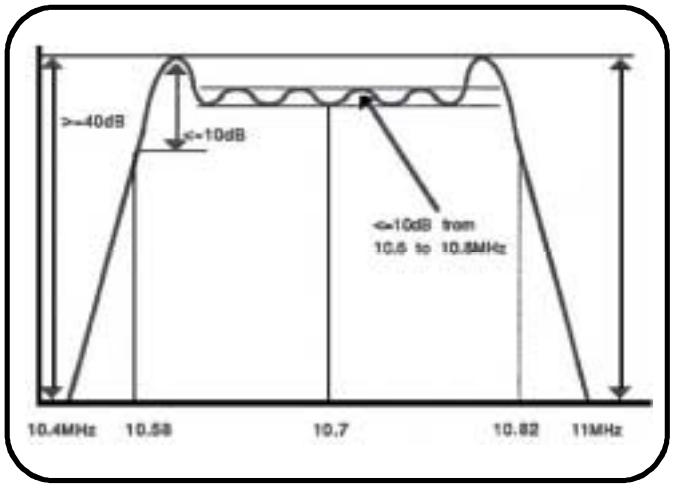


Fig 3.3.6.1A 10.7Mhz Wideband Filter Response

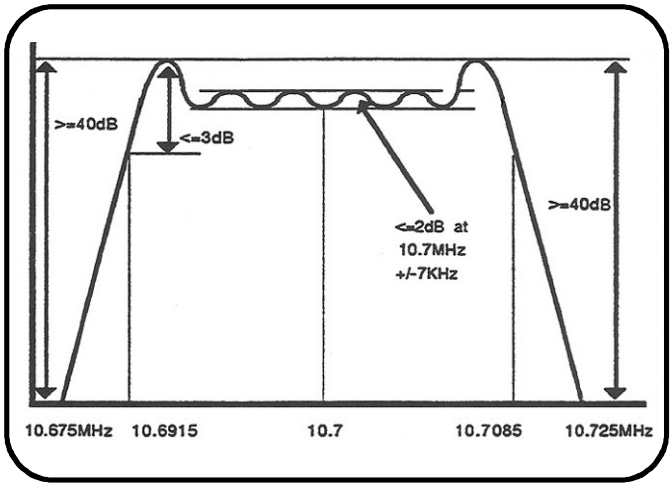


Fig 3.3.6.1B 10.7Mhz Narrowband Filter Response

• 3.3.6.2 AGC Adjustment

1. Setup UUT for monitor mode, AM, 5Hz highpass and 20KHz lowpass audio filters. Apply a 310.7MHz, -60dBm signal, 1KHz modulation tone, 30%AM modulation to J1 (310.7MHz IF).

2. Set J1 input level to -60dBm. Record the output level of the front panel DEMOD OUT port for later reference.

3. Change J1 input level to -30dBm. Increase J1 input level in 1dB steps until the output level of Squelched Demod at P1-87 drops 0.5dB from the level recorded in step 2. J1 input level should now be -19dBm ±1dB. If necessary, adjust R89 and repeat steps 2 and 3.

• 3.3.6.3 AM/FM Demod Level Adjustment

1. Setup UUT for monitor mode, narrowband FM, 3KHz lowpass and 300Hz highpass filters enabled.

   Apply a 310.7MHz signal, 1KHz modulation tone, 5KHz deviation, at -60dBm to J1.

2. Adjust R153 for 2.83Vrms ±0.01V at P1-87 (Squelched Demod).

3. Change UUT to wideband, 20KHz lowpass; and 5Hz highpass filters enabled. Change input signal at J1 to 50KHz deviation.

4. Adjust R145 for 2.83Vrms ±0.01V at P1-87 (Squelched Demod).

5. Change UUT to AM, 3KHz lowpass and 300Hz highpass filters enabled. Change input signal at J1 to 50% AM modulation.

6. Adjust R119 for 2.83Vrms ±0.01V at P1-87 (Squelched Demod).

• 3.3.6.4 Squelched Demod Offset Adiustment

1. Setup UUT for monitor mode, narrowband FM, 20KHz lowpass; and 5Hz highpass filters enabled.

   Apply a 310.7MHz CW signal at -60dBm to J1.

2. Adjust the Front Panel Squelch knob for 12VDC ±0.5V at Pl-84. Squelch LED should now be on.

3. Adjust R92 for 0.0mVDC ±1mV at P1-87.

   Power off UUT and return the Spectrum Analyzer Module to its normal installation.

3.3.7 Spectrum Analyzer

Power off UUT and install the Spectrum Analyzer Module on an extender card. Use ribbon cable extenders and RF cable extenders as necessary to reconnect module to the Analyzer.

3.3.7.1 VCO Tuning Voltage Adjustment

Setup UUT for generate mode, AM. Adjust C101 for 8.0VDC ±200mV at U15 pin 6.

3.3.7.2 Dispersion

1. Setup UUT for Monitor mode, 500MHz carrier, Spectrum Analyzer display, 1MHz per division. Apply a 500MHz CW signal at -50dBm to the Antenna port. Ensure that input signal appears in center of Spectrum Analyzer display ±1 minor division.

2. Without changing UUT setup, change input signal frequency to 496MHz. Signal at center of UUT display should be 4 major divisions to the left of center ±1 minor division. Repeat this step with input signal at 504MHz and check for 4 major divisions to the right of center.

3. If necessary, adjust R125 so the 496MHz and 504MHz signals appear in the correct locations ±1 minor division.

4. If UUT cannot be adjusted properly then C101 is not adjusted for the linear portion of the VCO. If necessary, repeat adjustments 3.3.7.1 and 3.3.7.2.

3.3.7.3 21.4MHz Filter Alignment:

1. Setup UUT for generate mode, AM, 500MHz carrier. Apply a swept 310.7MHz ±100KHz signal at -50dBm to J1 (310.7 SA IF).
2. Monitor the signal at P1-85 with an oscilloscope (trigger at P1-82). Adjust C5 and C9 for a flat middle, maximum amplitude, and minimum ripple at P1-85.

3.3.7.4 455KHz Wideband Amplitude

1. Setup UUT for monitor mode, 500MHz, Spectrum Analyzer display, at 20KHz per division. Apply a 500MHz CW signal at -50dBm to the Antenna port.

2. Signal amplitude at center of Spectrum Analyzer display should indicate -50dBm ±1minor division. Note actual value for later use.

3. Change UUT display to 1MHz per division. Adjust R51 so that the signal amplitude at center of display is equal, to the amplitude noted in step 3.
   Power off UUT and return the Spectrum Analyzer Module to its normal installation.

3.3.8 Generator

Power off UUT and install the Generator Module on an extender card. Use ribbon cable extenders and RF cable extenders as necessary to reconnect module to the Analyzer.

3.3.8.1 255-365MHz Bandpass Filter Alignment

1. Remove the solder connection between E1/E2 and E4/E5. Solder an RF connection for signal injection at E5 (signal) and E6 (ground). Disconnect J2 (SA LO) and terminate J2 with 50Ω impedance.

2. Power on UUT after reinstalling module into extender card. Set up UUT for generate mode, narrowband FM without modulation (CW), Antenna port, at any carrier frequency.

3. Apply a 215 to 470MHz swept signal at -18dBm to the cable soldered to E5/E6.

4. Monitor J1 (310.7MHz GEN IF) and adjust C88, C91, C95, C99, CI00, C105, and C114 for the response shown in figure 3.3.8.1. Swept signal applied at E5 should be in sync with measurement device at J1.

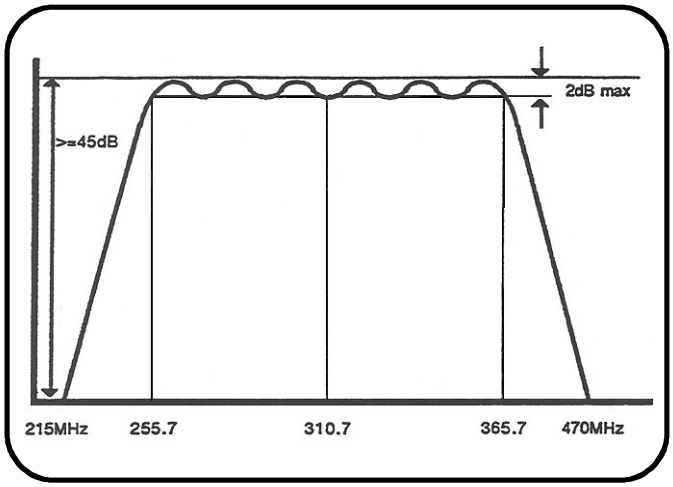


Fig 3.3.8.1 255-365MHz Bandpass Filter Response

3.3.8.2 215MHz VCO Adjust

1. Power off UUT and solder an RF connection for frequency measurement at TP211A1 (signal) and TP211B1 (ground).

2. Power on UUT and set up for generate mode, narrowband FM without modulation (CW), Antenna port, at any carrier frequency.

3. Adjust C62 for a VCO frequency of 215 ±1MHz at TP211A.

4. Power off UUT and remove RF cable at TP211A1/Bl. Remove the RF cable at E5/E6 and solder cable to El (signal) and E3 (ground). Do not resolder the E1/E2 and E4/E5 connections at this time. Power on UUT.

3.3.8.3 3l0.7MHz Bandpass Filter Alignment

1. Apply a 310.7 ±25MHz at 10dBm swept signal (285.7 to 335.7MHz) at E1.

2. Monitor J1 and adjust C19, C20, C21, and C22 for the response shown in figure 3.3.8.3 (NOTE: swept signal applied at Antenna port should be in sync with measurement device at J1.

3. Power off UUT and remove RF cable at E1/E3. Resolder the E1/E2 and E4/E5 connections. Power on UUT.

4. Put Analyzer in generate AM mode with no modulation. Monitor 310.7MHz output of Generator Module at Jl. Adjust R9 for an amplitude of -17.5dBm.

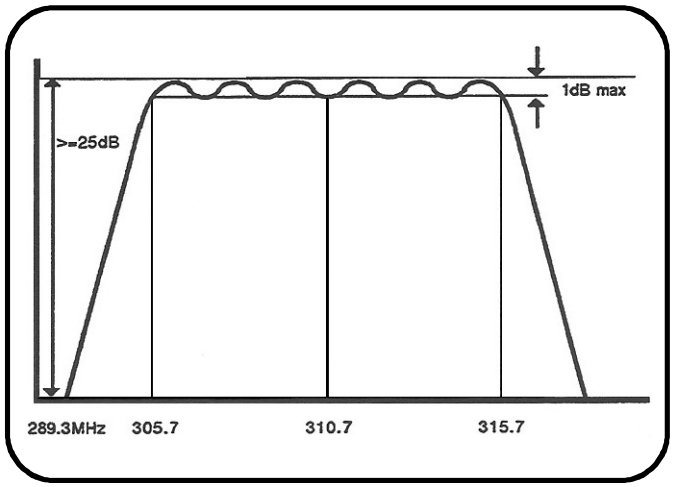


Fig 3.3.8.3 310.7MHz Bandpass Filter Response

3.3.8.4 Dual Band VCO Alignment

1. Set up UUT for generate mode, 500MHz, narrowband FM, CW, at any carrier frequency and disconnect J2.

2. Short TP221 to ground (shorts across C106) to clamp the loop filter at its highest frequency. Apply +5VDC to the junction of R135, R156, and C93. Adjust C168 for a frequency of 330MHz ±1MHz at J1.

3. Change UUT from FM to AM. Adjust C169 for a frequency of 380 ±1MHz at J1.

4. Remove the ground jumper and +5VDC that were connected in step 2. Reconnect J2.

• 3.3.8.5 Loop Operation

1. Setup UUT for Duplex mode, 500MHz, narrowband FM, with an offset of -55MHz.

2. Monitor the output level at J1 (310.7MHz GEN). It should be -15.5 to -18.ldBm for the following conditions.

Duplex offset	J1 Frequency
-55MHz	365.7
0MHz	310.7
+0.1MHz	310.6
+55MHz	255.7

3. If the output level is incorrect at any of the step 2 conditions, adjust R32 and repeat step 2.

• 3.3.8.6 FM Deviation Level

1. Set up UUT for generate mode, 500MHz, narrowband FM, 5KHz deviation. Modulate the carrier with an external 1KHz tone.

2. Adjust the level of the external 1KHz modulation tone until MOD CAL AUDIO at P1-38 of the Generator Module is 4.0 ±0.01Vrms.

3. Adjust R90 for 5KHz ±_0.5KHz (rms) deviation at J1 (310.7MHz GEN).

4. Change the UUT to wideband and repeat step 2.

5. Adjust R89 for 50KHz ±0.5KHz (rms) deviation at J1.

3.3.8.7 Loop Gain and FM Mod Frequency Response

1. Set up UUT for generate mode, 500MHz, narrowband FM. Modulate the carrier with an external 1KHz tone. This procedure will refer to the external 1KHz modulation tone as “tone X”.

2. Adjust the level of tone X until MOD CAL AUDIO at P1-38 of the Generator Module is 4.0 ±0.01Vms.

3. Connect a modulation analyzer to J1 (310.7MHz GEN). Measure the output level at the demodulated audio output of the mod analyzer and record the value for later reference. This procedure will refer to the demodulated audio at the modulation analyzer as “tone A”.

4. Change tone X to 5.0Hz ±02Hz. Adjust R143 so that tone A is -0.2 ±0.2dB from the value recorded in step 3. NOTE: an oscilloscope may be required for this if the DVM being used cannot measure signals at 5Hz.

5. Change UUT to wideband. Change tone X to 1KHz. Measure tone A and record the value for later reference.

6. Change tone X to 5.0Hz ±0.2Hz. Measure Tone A again. Tone A should be -0.2dB ±0.3 from the reference value recorded in step 5.

7. Change tone X to 20KHz ±500Hz. Tone A should now be within ±0.7dB from the reference value recorded in step 5.

• 3.3.8.8 AM Modulation Sensitivity Adjustment

1. Set up UUT for generate mode, 500MHz, AM. Modulate the carrier with an external 1KHz tone.

2. Adjust the level of the external 1KHz modulation tone until MOD CAL AUDIO at P1-38 of the Generator Module is 4.0 ±0.01Vrms.

3. Adjust R68 for 50% ±0.5% (rms) AM modulation at J1 (310.7MHz GEN) (mod analyzer should be set up for average mode, 300Hz to 3KHz bandwidth).

3.3.9 RF Output

This module is calibrated automatically by the Analyzer during the system calibration triggered via the front panel CAL button. There are no manual adjustments on this module

3.3.10 Processor Module

Power off UUT. Remove Processor Module from it's mounting hardware and relocate it across the top of the UUT to gain access to adjustments. It is mandatory to place a non-conductive surface between the Processor Module and the UUT hardware to prevent shorting the Processor circuitry. Reconnect cables with the Processor module relocated across the top of the UUT. Allow sufficient warm-up time for the 10MHz standard to stabilize after powering the unit back on.

3.3.10.1 +8V Regulator

Adjust R229 for +8VDC ±50mV at U29 (U89) pin 3.

• 3.3.10.2 DTMF Encode Level

1. Setup UUT for generate mode, Gen Out port, wideband FM, DTMF modulation, all digits DTMF code 1, 50KHz modulation.

2. Monitor the Gen Out port with an RF modulation analyzer. Adjust R164 to achieve 50KHz ±5% modulation at the Gen Out port.

• 3.3.10.3 Intemal 1KHz Level

1. Setup UUT for generate mode, Gen Out port, wideband FM, internal 1KHz modulation, 50KHz modulation.

2. Monitor the Gen Out port with an RF modulation analyzer. Adjust R159 for maximum modulation at the Gen Out port.

3. Adjust R155 to achieve 50KHz ±5% modulation at the Gen Out port

   Power off UUT and. return Processor Module to its normal installation.

3.3.11 Interface Module

Power off UUT and install the Interface Module on an extender card. Use ribbon cable extenders and RF cable extenders as necessary to reconnect module to the Analyzer. Allow sufficient warm-up time for the 10MHz standard to stabilize after powering the unit back on.

3.3.11.1 +8 and -2VDC Regulator Adjustments

1. Adjust R236 for +8VDC ±1mV at U68, pn 3

2. Adjust R56 for -2VDC ±2mV at U31, pin 26.

3.3.11.2 Meter In Port Offset Adjustment

1. Setup UUT for external DVM with no input at the front panel Meter In port.

2. Adjust R72 for 0.0 ±100µVDC at U16 pin 6.

3.3.11.3 DVM Offset Adjustment

1. Setup UUT for DC voltmeter display, 1V scale, with no input at the front panel Meter In port.

2. Adjust R153 for 0.0 ±500µVDC at U42 pin 6.

3. Change UUT to AC voltmeter. U42 pin 6 should change less than 1mVDC between AC and DC modes. If necessary, adjust R72 to achieve this and repeat steps 1, 2 and 3.

3.3.11.4 Scope Offset Adjustment #1

1. Setup UUT for external oscilloscope, AC coupled, 10mV/div with no input at the Meter In front panel port.

2. Adjust R105 for 0.0 ±500µVDC at U34 pin 6.

3. Change UUT to DC coupling. Less than 50uVDC of change should occur at U34 pin 6 while switching UUT between AC and DC coupling. If necessary, adjust R72 to achieve this and redo DVM Offset adjustment (3.3.11.3) and Scope Offset Adjustment #1 (this adjustment).

NOTE

It may be necessary to perform the DVM Offset Adjustment (3.3.11.3) and Scope Offset Adjustment #1 (3.3.11.4) several times to achieve the following (with no signal at the front panel Meter In port):

DVM Mode U42-6 = 0.0 ±500µVDC (in DC mode) and less than 1mVDC change between AC/DC modes (adjusted with R72 and R153).

Scope Mode U34-6 = 0.0 ±500µVDC (in AC mode) and less than 500µVDC change between AC/DC modes (adjusted with R72 and R105).

3.3.11.5 Scope Offset Adjustment #2

1. Setup UUT for external scope, DC coupling, 20mV/div. Adjust R145 for 0.0 ±500µVDC at U46 pin 6.

2. Change UUT to 10mV/div. Adjust R167 for 0.0 ±500µVDC at U43 pin 6.

3.3.11.6 Scope Vertical Positioning

Setup UUT for external scope, DC coupled, 20mV/div. Using front panel controls, ensure that trace can be moved to upper and lower limits of the graticle. If trace cannot be moved to either upper or lower edge of graticle, adjust R57 and try again.

3.3.11.7 Scope Linearity

1. Setup UUT for external oscilloscope. Apply a 4Vpp sine wave signal to the Meter In port. Adjust input signal frequency and UUT front panel controls so that 1 or 2 full cycles appear within the scope screen.

2. Adjust R120 for a symmetrical sine wave trace on the scope display of the UUT.

3.3.11.8 Generate Audio Offset

1. Setup UUT for generate mode, FM, no modulation (CW), general sequence audio mode.

2. Adjust R181 for 0.0 ±100µVDC at U49 pin 6.

3.3.11.9 Metering Input Compensation (Coarse)

1. Setup UUT for external scope, AC coupled, 2V/div, 200µsec/div. Apply an 8Vpp 1KHz square wave signal to the UUT front panel metering in port.

2. View the UUT scope display and adjust C23 so the peak on the rising edge of the square wave just disappears.

3.3.11.10 DVD Offset

1. Setup UUT for AC Voltmeter, 1V scale.

2. Adjust R189 for 0.0 ±200µVDC at U60 pin 6

3. Adjust R196 for 0.0 ±500µVDC at U61 pin 12.

4. Verify that U70 pin 3 is 250µV or less.

5. Monitor U72 pin 6 with an oscilloscope. The signal will be changing high and low due to the processor's sampling of the A/D converter. For the following adjustment it will be necessary to stop the processor. With no signal connected to the Rear Panel 10MHz IN/OUT port, switch S1 to the EXTERNAL position so U72 pin 6 stays low. Several attempts may be required.

6. Adjust R188 for 0.0 ±100µVDC at U72 pin 6 (use an external DVM. Verify that U61 pin 8 is 0.0 ±500µVDC.

7. Retum switch S1 to the INTERNAL position. Power UUT off, then on to reset the processor.

3.3.11.11 Sign-POS/NEG

1. Setup UUT for DC Voltmeter, 1V scale.

2 With no signal applied to the Meter In port, observe the UUT display screen and adjust R239 so that the sign field alternates between plus (+) and minus (-).

3.3.11.12 RMS to DC Gain

1. Setup UUT for AC Voltmeter, auto ranging. Apply a 1KHz sine wave at approx 1.8Vpp to the Meter In port.

2. Adjust 1KHz input signal level to produce 3.0Vrms ±2mVrms at U70 pin 3.

3. Adjust R214 for 3.0VDC ±1mVDC at U61 pin 12.

2. Adjust R259 for a 0.9VAC ±1mV reading on the UUT display screen.

3.3.11.13 DVM Gain

1. Setup UUT for AC Voltmeter, 1V scale. Apply a 1KHz sine wave at 0.9Vrms at Meter In port.

3.3.11.14 Metering Input Compensation (Fine)

1. Setup UUT for AC Voltmeter, 1V scale. Apply a 1KHz triangle wave signal at 230mVrms to the Meter In port. UUT display should read 230 ±1mV

2 Change input signal frequency to 20KHz. Verify that signal level is still 230mVrms with external DVM and reconnect input signal to UUT Meter In port.

3. UUT display should read 230 ±1mV. If necessary, adjust C23 and repeat steps 1, 2 and 3.

3.3.11.15 Notch Filters

1. Setup UUT for SINAD meter. Apply a 998Hz sine wave at approx 200mVrms to the UUT Meter In port. Adjust input signal level so that U83 pin 1 is lVrms ±50mV.

2. Alternately adjust R269 and R291 for minimum AC rms voltage at U85 pin 1 (typically less than 75mVrms).

3. Change input signal frequency to 1002Hz. Adjust input signal level so that U83 pin 1 is 1Vrms ±50mV.

2. Alternately adjust R286 and R285 for minimum AC rms voltage at U81 pin 15 (typically less than 75mVrms).

R2600 Basic Alignment Quick Checklist

- ❑ 1. Power Supply
- ❑ 2. Frequency Standard

High Synthesizer

- ❑ 3. WB Loop Setup and VCO Operating Range

Receiver

- ❑ 4. 10.7MHz Filter Check and Alignment
- ❑ 5. AGC Adjustment
- ❑ 6. AWFM Demod Level Adjustment
- ❑ 7. Squelched Dernod Offset Adjustment

Generator

- ❑ 8. Loop Operation
- ❑ 9. FIVI Deviation Adjustment
- ❑ 10. AM Modulation Sensitivity Adjust

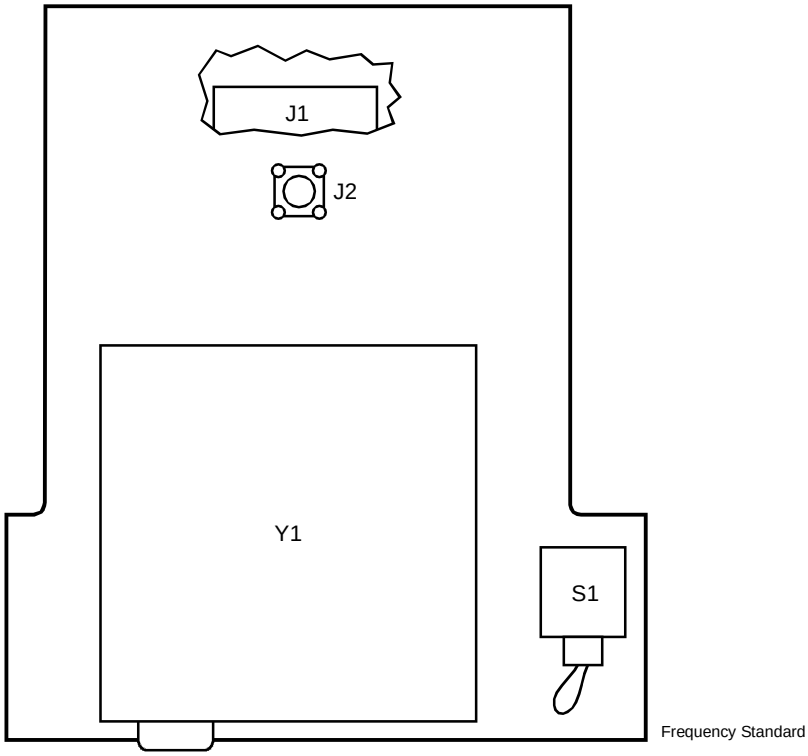
Processor Module

- ❑ 11. DTMF Encode Level
- ❑ 12. Internal I KHz Level

Recheck Frequency Standard

Perform System Test After Alignment

Fig. 3.3A Basic Alignment Quick Checklist



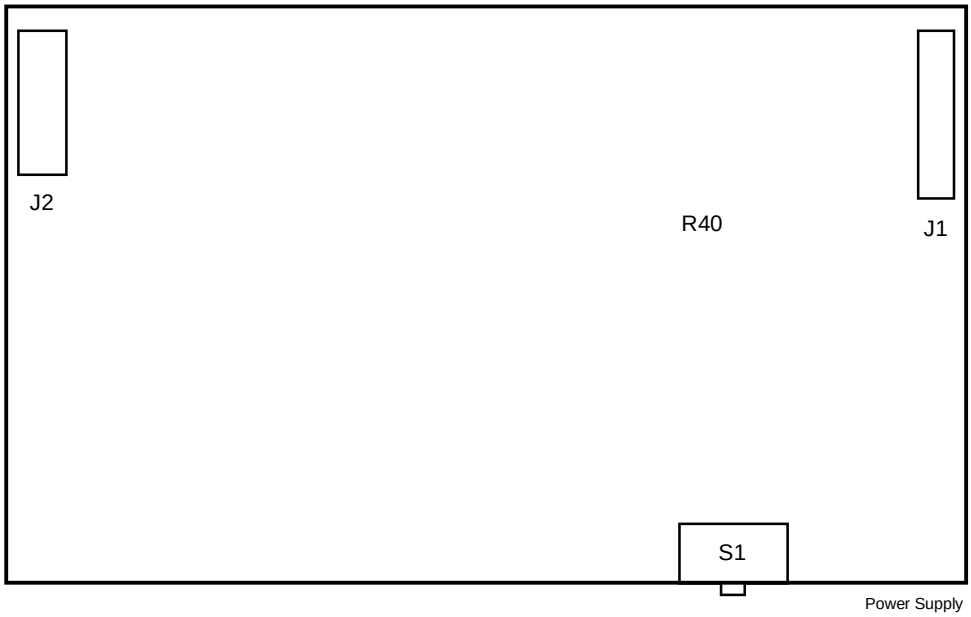
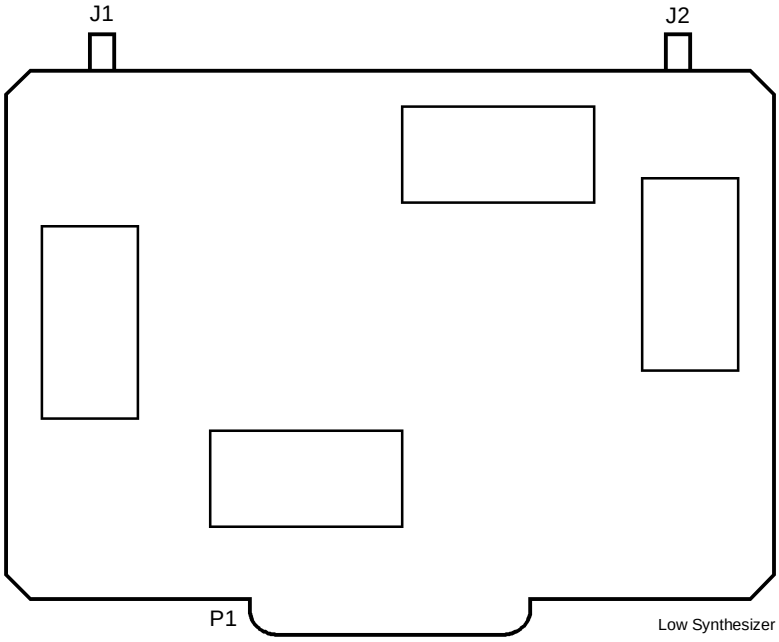


Fig 3.3B Adjustment Locations (1 of 5)



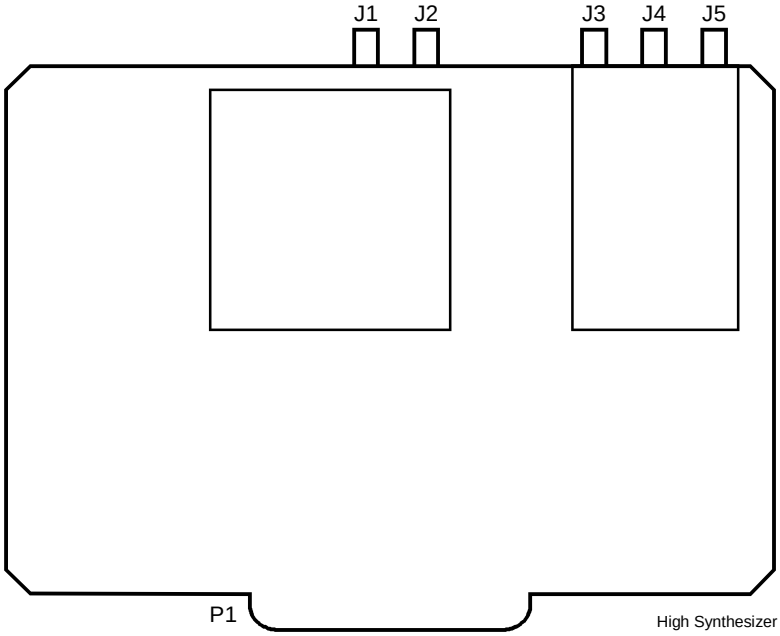
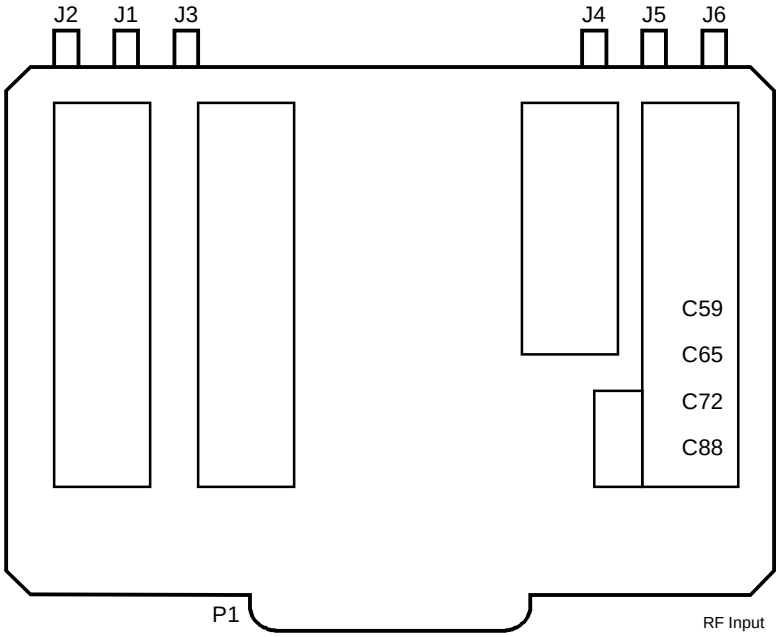


Fig 3.3B Adjustment Locations (2 of 5)



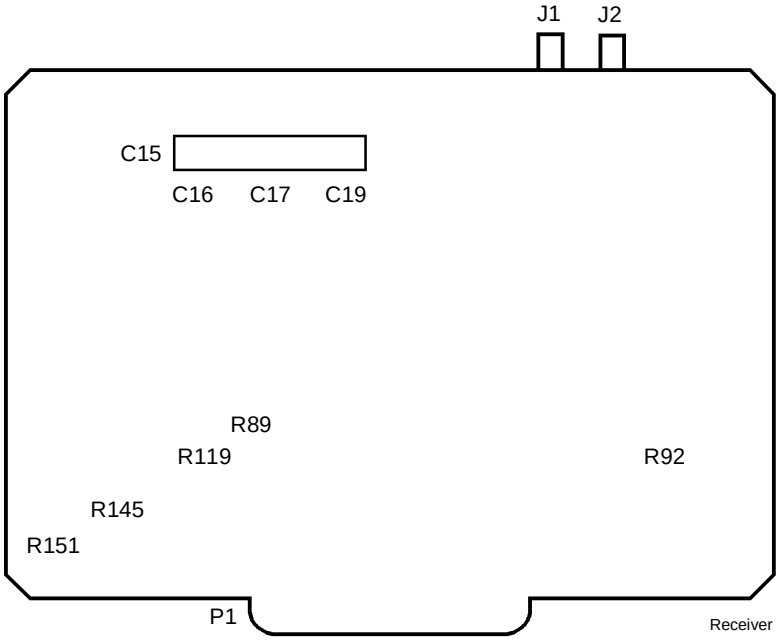
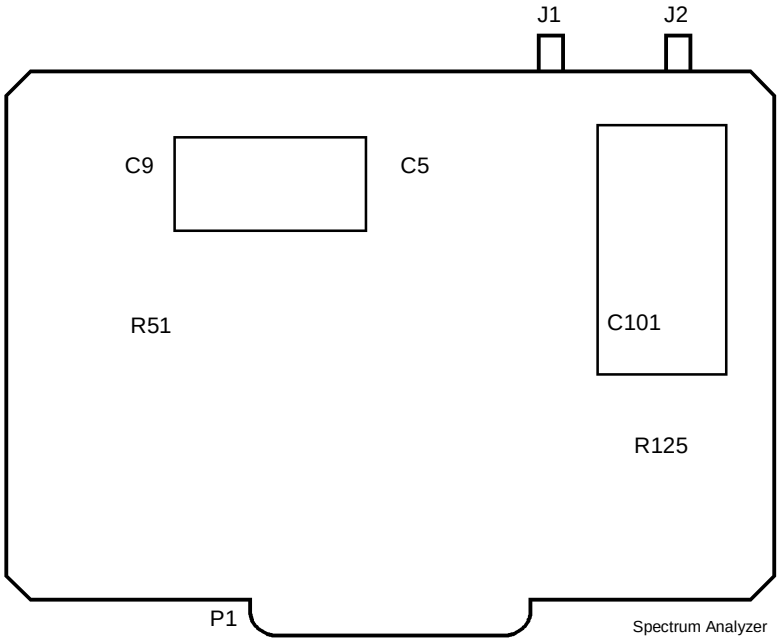


Fig 3.3B Adjustment Locations (3 of 5)



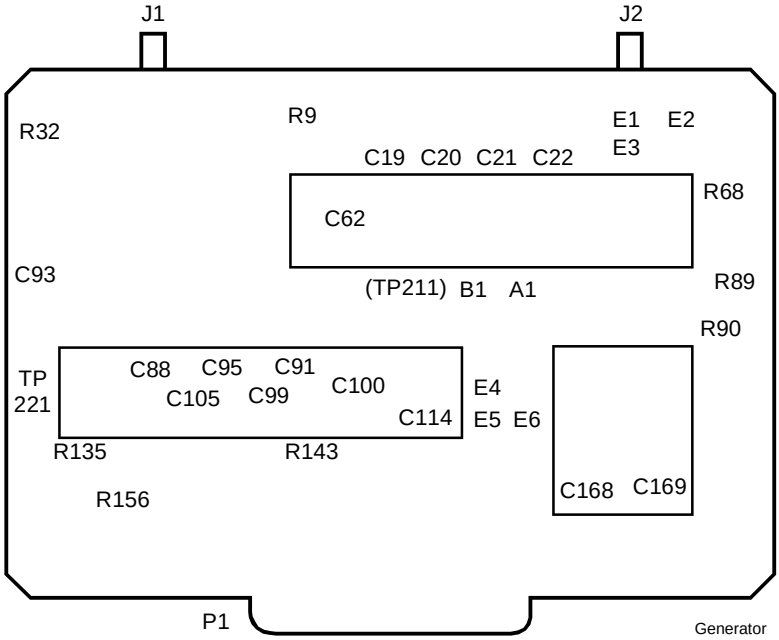
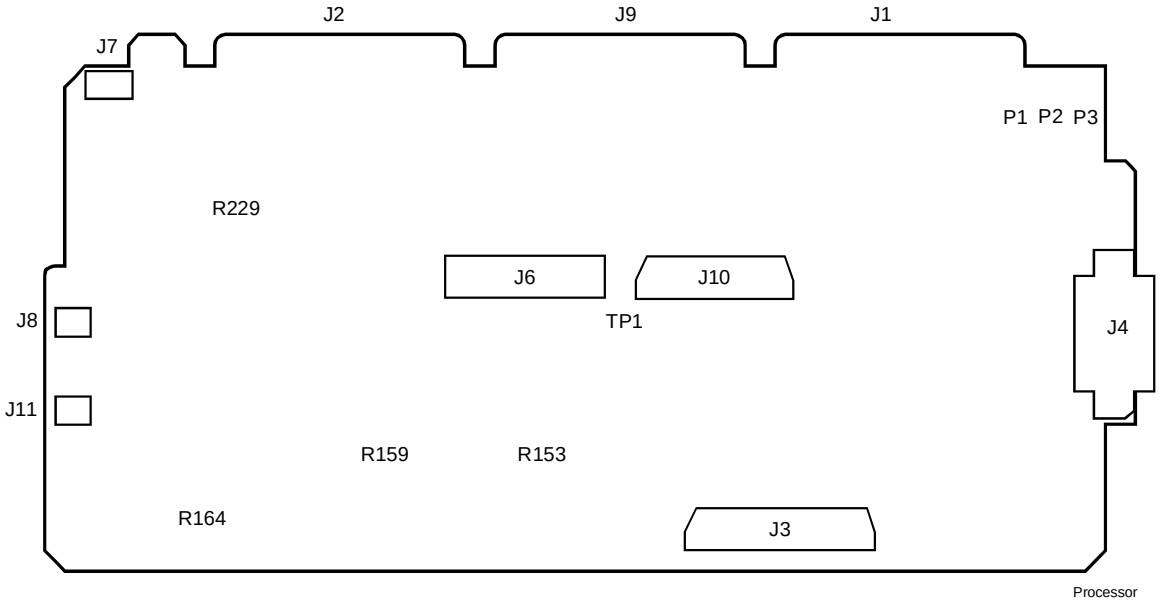


Fig 3.3B Adjustment Locations (4 of 5)



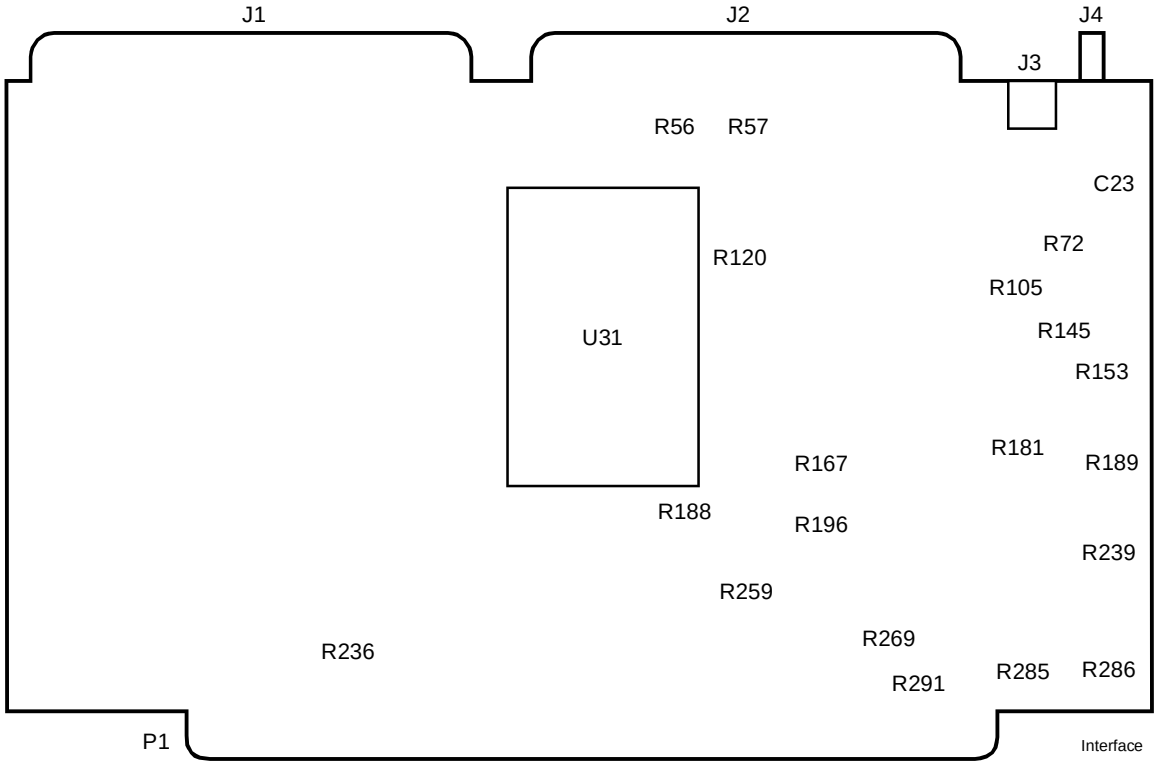


Fig 3.3B Adjustment Locations (5 of 5)

Section 4
HIGH TIER FREQUENCY STANDARD

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Section 4
HIGH TIER FREQUENCY STANDARD

4.1 GENERAL DESCRIPTION

The High Tier Frequency Standard Module (A13) is installed at the bottom of the Analyzer towards the rear panel. The module provides 10 MHz reference signals for the system's use.

This module uses an Oven Compensated Crystal Oscillator (OCXO). The OCXO, provides stability of ±0.1ppm (±1Hz) over temperature variation.

Switch S1 (10 MHz IN/OUT SELECT) is accessible from the Analyzers bottom cover. Remove bottom cover for access to the module.

Adjustment of the 10MHz standard is mandatory after replacement or repair of this module. Refer to the alignment procedure in section 3 of this manual.

4.2 SIGNALS SUMMARY

4.2A Signal Descriptions

SYNTH 10 MHz Ref (Synthesized 10 MHz Reference) is the 10 MHz reference output signal used for RF module timing.

SYSCLK is a 10 MHz output signal to connector J1. It is routed to the RF Motherboard for the Analyzers digital timing.

10 MHz IN/OUT is an input or output depending upon the position of mechanical switch S1 (accessible from the bottom of the Analyzer).

+12 Vdc and -12Vdc supply power to this module.

4.2B Connector Descriptions

J1 (Ribbon Cable to Processor Module)

pin	
1,2	+12V
3,4	not used
5,6	-12V
7,8	not used
9	SYSCLK
10	GND

J2 SYNTH 10 MHz REF

(SMB connector to RF Motherboard)
V_{out} (high) = 4.0 to 5.0V
V_{out} (low) = 0.0 to 0.5V
Output duty cycle = 40 to 60%
R_{out} = 350Ω max
C_{load} = 50pf max

SMB Connector to Rear Panel 10 MHz IN/OUT
As an output: 250mVrms min into 50Ω, capacitively, coupled
As an input: Minimum range of 70-1000mVrms into 50Ω at 10MHz, 20-80% duty cycle.

4.3 BLOCK DIAGRAM DESCRIPTION

4.3.1 Power Supply Conditioning

Power to the module is supplied by +12Vdc and -12Vdc at connector J1. Filtering/regulation circuitry produces the +5V and -5V voltages required by this module. The OCXO uses +12V instead of the regulated +5V.

4.3.2 Internal/External Oscillator Selection

Switch S1 (accessible from the bottom of the Analyzer) selects 10 MHz IN/OUT as an input or output.

INTERNAL: S1 connects the supply voltage to the internal oscillator and 10MHz IN/OUT is selected as a buffered output.

EXTERNAL: S1 disconnects the supply voltage to the internal oscillator to eliminate beat note interference with the external source. The external 10 MHz input signal (connected at rear panel) is buffered and substituted for the internal oscillator.

4.4 DETAILED DESCRIPTION

4.4.1 Power Supply Conditioning

Voltage regulators U2 and U4 are configured in series to add filtering for power supply noise rejection and to reduce the power dissipated in each to proper levels. U2 outputs the +5V regulated signal which is the supply voltage for comparator U1, Solid state analog switch U5, CMOS quad AND U3, and output amplifier Q4 for SYSCLK.

Voltage regulator VR5 provides a -5V output with a high degree of filtering. The -5V Filt line is used for the comparator Ul and analog switch U5.

4.4.2 Internal/External Oscillator Selection

When S1 is switched to internal, U5A detects the oscillator supply voltage (+5V Reg) and develops the control signal INTH (internal, active low). VR3 and D3 clamp EXTH (External, active low) to a safe level for U5.

4.4.3 SYSCLK Output

High speed comparator Ul provides a square wave representation of the 10MHz reference signal. The square wave is converted to an HCMOS logic level using

R49, C30, R13, and Q4. HCMOS gates U3A and U3B are used to buffer the 10MHz reference signal to drive a filter and the SYSCLK load. The filter is designed to output a sine wave with less than 10% total harmonic distortion with a digital input of 20% to 80% duty cycle. This allows the processor module to develop a 50% duty cycle wave form for the microprocessor.

4.4.4 SYNTH 10MHz Ref Output

U3D is used to drive the synthesizer reference signal. Fast rise and fall times reduce phase jitter.

4.4.5 10MHz IN/OUT

When 10MHz IN/OUT is selected by S1 as an output, Ul is used to drive bandpass filter circuit C15, C16, L3, and L4. The filter is designed to output a sine wave with less than 10% total harmonic distortion, at a minimum level of 250 mVrms output into 50 ohms.

When 10MHz IN/OUT is selected by S1 as an input, Ul is used to convert the input sine wave into a square wave. Hysteresis (R-27, R-28) set at approximately 1/2 the minimum input level of 70mVrms prevents Ul from triggering on noise.

4.5 BLOCK DIAGRAM

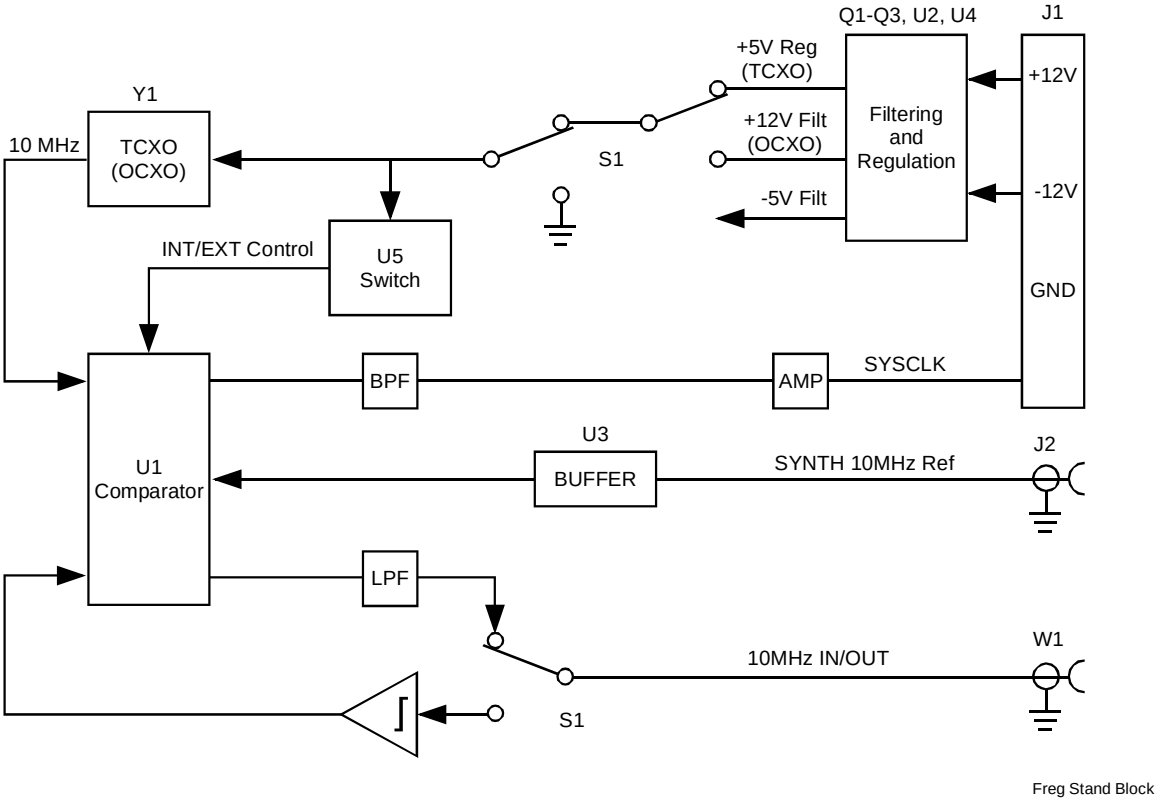
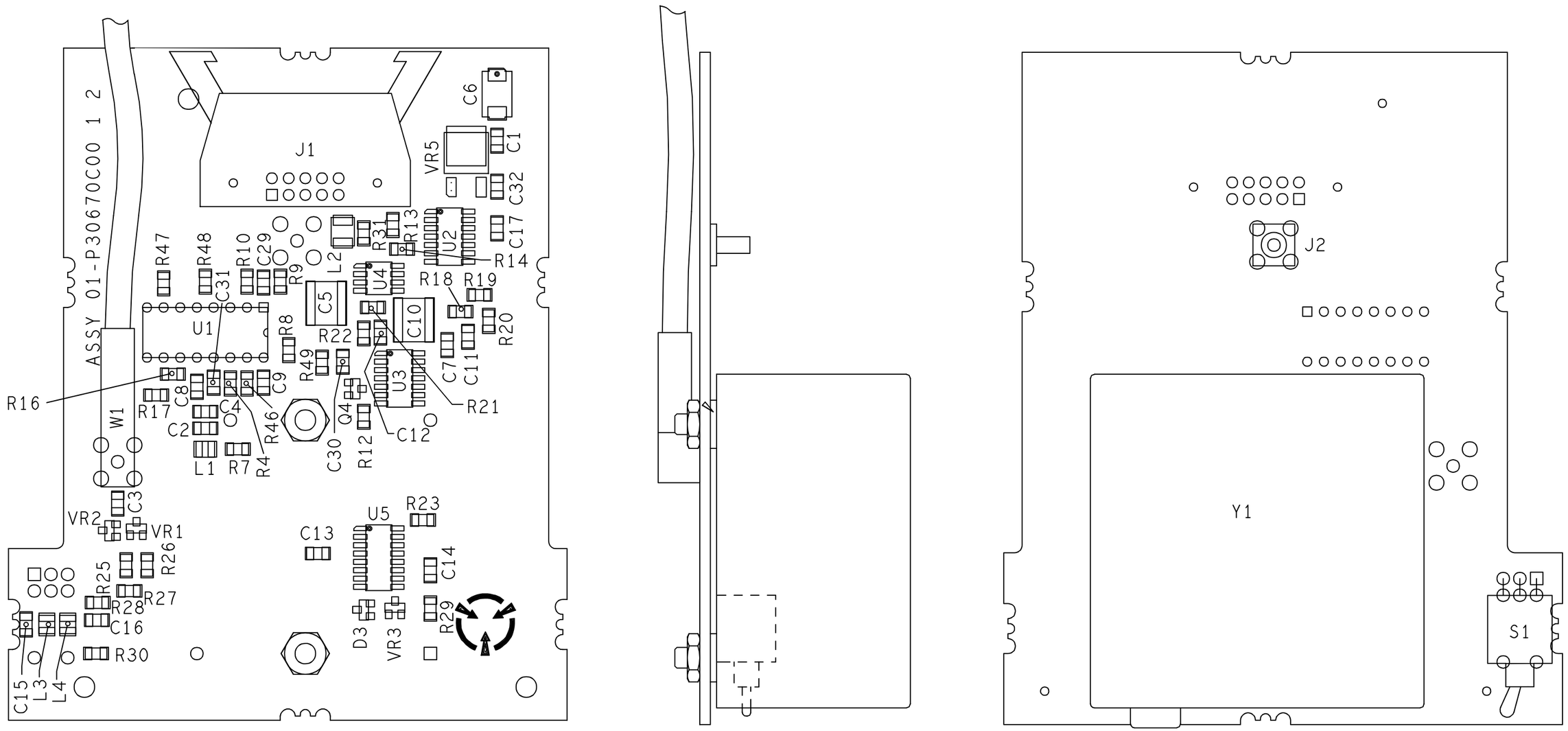


Figure 4.5 High Tier Frequency Standard Block Diagram



CIRCUIT CARD ASSEMPLY
HIGH TIED FREQUENCY STANDARD

01-P30670C REV. C

SHEET 1 OF 1

DWG NO.	SH
63-P30672C	1

REVISIONS

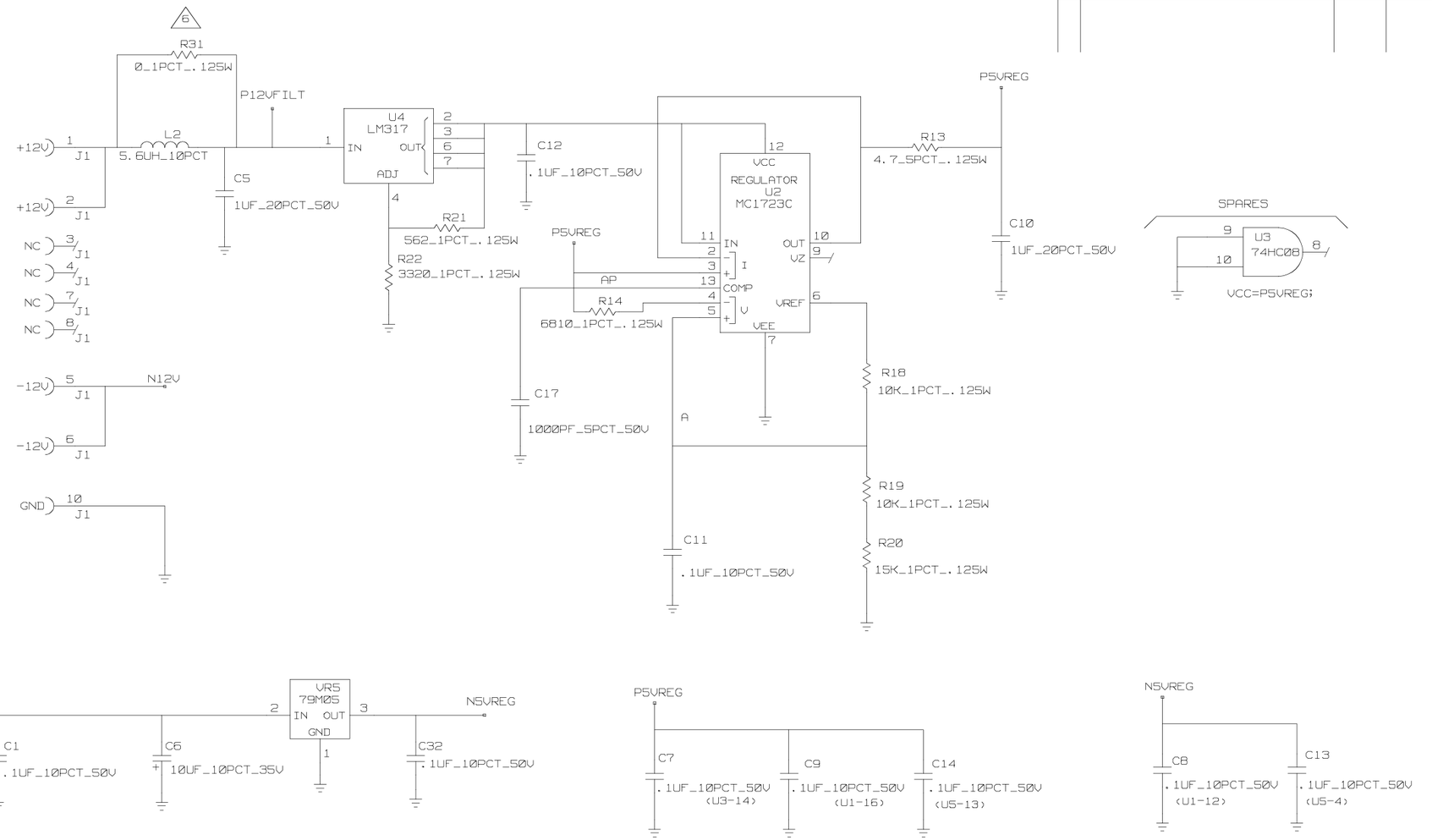
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	INITIAL RELEASE		

NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A13.
2. FOR REFERENCE DRAWINGS REFER TO:
   01-P30670C ASSEMBLY
   12-P30673C TEST PROCEDURE
3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 1PCT, 1/8 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL INDUCTORS ARE IN UH.
   ALL VOLTAGES ARE IN DC.
4. TERMINATIONS CODED WITH THE SAME LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
5. DEVICE TYPE NUMBERS ARE LISTED IN TABLE 1.

6. ASSEMBLY 01-P30670C002 ONLY. HIGH STABILITY

8. ASSEMBLY 01-P30670C001 ONLY. STANDARD



REFERENCE DESIGNATIONS	
HIGHEST USED ON	NOT USED
C31	C18-C28
D3	D1, D2
J2	
L4	
Q4	Q1,Q2,Q3
R49	R1-R3,R5,R6,R11, R15,R24,R37-R45,
S1	
U5	
VR5	VR4
W1	
Y1	

* TABLE 1

REF DES	DEVICE TYPE	VCC CONNECTION PIN	VCC CONNECTION VOLTS	GND CONN	NO CONN
U1	MC3430	16	+5VREG	8	
		12	-5VREG		
U2	MC1723C				1,8,14
U3	74HC08SC	14	+5VREG	7	
U4	LM317L				5,8
U5	DG211	12,13	+5VREG		
		4	-5VREG	5	

* TABLE 1 IS FOR REFERENCE ONLY.

REV																	
SHEET																	
REV STATUS REV						A	A										
OF SHEETS SHEET						1	2										

PROJ NO. 10744	
NEXT ASSY	USED ON
APPLICATION	

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS LISTED IN DOD-STD-100

DWN BY V.HARWOOD 94-01-28

DOC CHK BY

DSGN CHK BY M.ONEY 94-01-31

CONTR NO.

ISSUED B35550-233(A)94-12-7

QA APVD K.NELSON 94-01-31

MATL APVD W.MCDONALD 94-01-31

MFG APVD K.CHANEY_94-01-31

ENGRG APVD M.ONEY 94-01-31

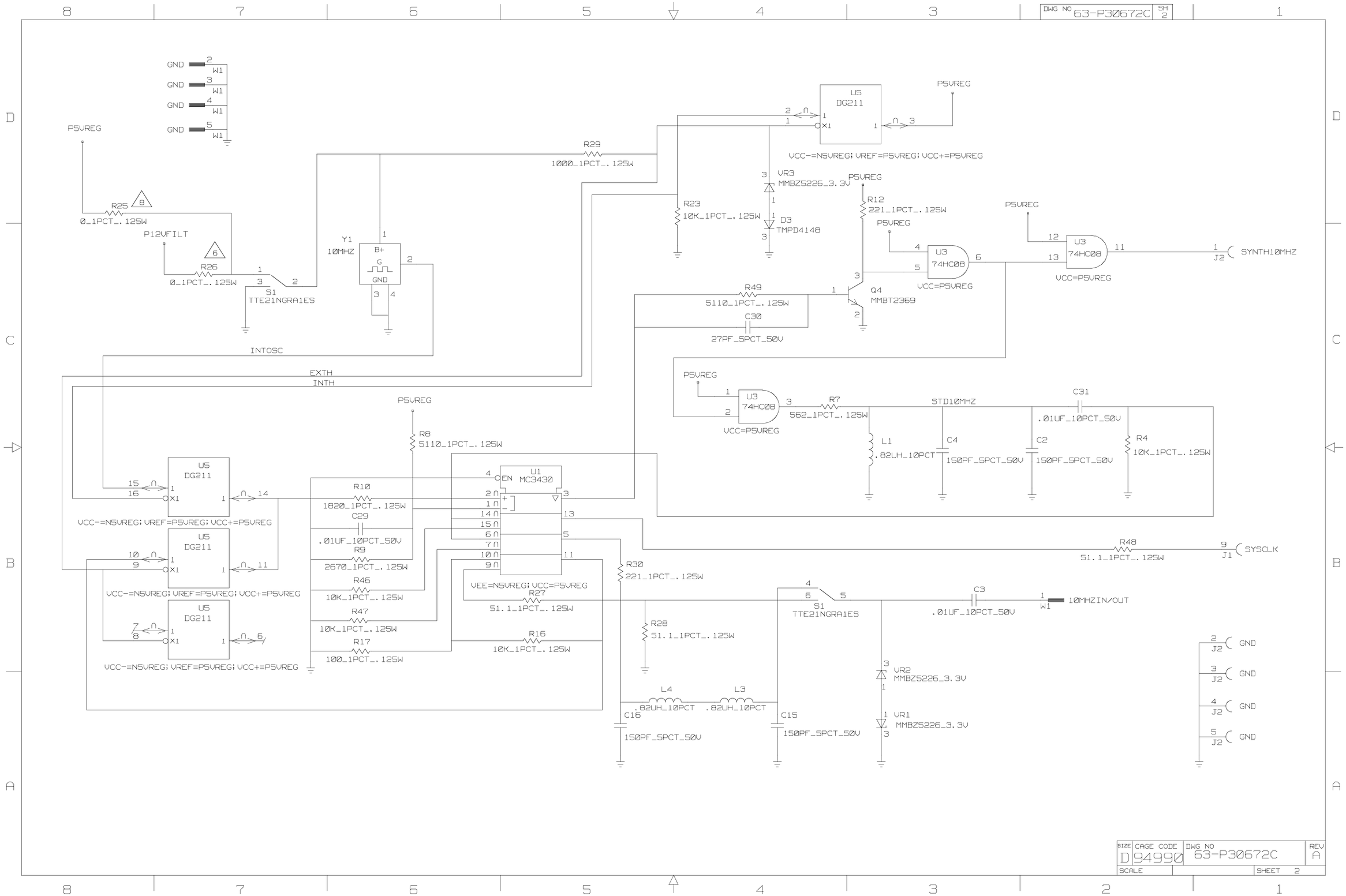
CUST APVD

MOTOROLA INC. G.E.G.
COMMUNICATIONS DIVISION
8201 E.MC DOWELL RD.,P.O.BOX 1417
SCOTTSDALE, ARIZONA 85252-1417

SCHEMATIC DIAGRAM HIGH TIER FREQUENCY STANDARD

SIZE	CAGE CODE	DWG NO.
D	94990	63-P30672C

SCALE NONE SHEET 1 OF 2



SIZE	CAGE CODE	DWG NO	REV
D	94990	63-P30672C	A
SCALE		SHEET 2	

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5.1 GENERAL DESCRIPTION

The High Synthesizer Module (A7) is installed in the RF cardcage, in the third slot from the center of the Analyzer.

This module outputs two local oscillator signals (coarse and fine) for both Generate and Monitor functions. One ranges from 1710 to 2710MHz (1st LO) in 10MHz steps for coarse frequency control. The other ranges from 1380.0001 to 1400MHz in 100Hz steps for fine frequency control (1400MHz LO).

The fine frequency control is synthesized using the LO SYNTH RF signal from the Low Synthesizer Module. The actual 1400MHz LO frequency is equal to 1500MHz minus the LO SYNTH RF frequency.

5.2 SIGNALS SUMMARY

5.2A Signal Descriptions

HI SYNTH DATA input from the Interface Module is the serial data used to program the 1st GEN and Receiver LOs in conjunction with the SYNTH CLOCK and SYNTH LATCH lines.

LOW SYNTH RF input from the Low Synthesizer Module provides the vernier frequency steps for both the generate and monitor functions.

SYNTH CLOCK input is used to clock data into the synthesizer loops.

SYNTH LATCH input is used to latch the serially clocked data.

SYNTH 10MHz Reference input from frequency Standard Module provides a reference to synthesizer loops.

1st GEN LO and *1st RCV LO* outputs from the wideband PLL are used as a variable LO when the system is in the generate and monitor functions of the Analyzer (1710 to 2710MHz in 10MHz steps).

1400MHz GEN LO and *1400MHz RCV LO* are outputs of the 1500 MHz PLL used for fine frequency control of the generate and monitor functions of the Analyzer (1380.0001 to 1400MHz in 100Hz steps).

1500 PLL DATA is the serial data line for programming the PLL that controls the 1500MHz LO.

+5V, -5V, +12V, -12V, and +40V supply power to the High Synthesizer module.

5.2B Connector Descriptions

P1 50 (Pin Edge Connector to RF Motherboard)

pin	
1, 2	GND
3, 4	+5V
5, 6	-5V ECL
7, 8	+40V
9-11	not used
12	SYNTH CLOCK
13	SYNTH LATCH
14-18	not used
19	1500 PLL DATA
20-31	not used
32	HIGH SYNTH DATA
33-38	not used
39, 40	GND
41, 42	SYNTH 10MHz REF
43, 44	GND
45, 46	-12V
47, 48	+12V
49, 50	GND

SMB CONNECTORS

J1 1st GEN LO
Output freq: 1710 to 2710MHz in 10MHz steps
Output power: -4.0dBm to +3.0dBm
Impedance: 50Ω nominal
VSWR: 2:1 maximum.

J2 1st RCV LO
Output freq: 1710 to 2710MHz in 10MHz steps
Output power: -4.0dBm to +3.0dBm
Impedance: 50Ω nominal
VSWR: 2.1 maximum

J3 LOW SYNTH RF
Freq: 100 to 119.9999MHz in 100Hz steps
Input level: -2dBm ±2dB
Output impedance: 50Ω nominal
VSWR: 2:1 maximum

J4 1400 MHz RCV LO
Freq: 1390.0001 to 1400MHz in 100Hz steps
Output level: +2.0 ±2.5dBm
Output impedance: 50Ω nominal
VSWR: 2:1 maximum

J5 1400 MHz GEN LO
Freq: 1390.0001 to 1400MHz in 100Hz steps
Output level: +2.0 ± 2.5dBm
Output impedance: 50Ω nominal
VSWR: 2.1 maximum

5.3 BLOCK DIAGRAM DESCRIPTION

This module contains two phase lock loops. The frequencies of both PLLs are controlled by the system processor via serial lines. The first PLL is the 1500MHz loop, which produces the 1400MHz LO signal for the system. The second PLL is the Wideband loop, which produces the 1st LO output signals that cover the 1710-2710MHz range.

Note that the Low Synthesizer provides a RF input to this module.

5.3.1 1500MHz PLL

The 1400MHz RCV LO signal, produced by the loop's VCO, is mixed up with the LOW SYNTH RF input signal (from the Low Synthesizer Module) which has a range of 100 to 119.9999MHz in 100Hz steps. The resulting 1500MHz signal is input into the prescaler input of the Phase Lock Loop (PLL) IC.

In the PLL IC, the signal is divided by a fixed ratio of 450 down to equal the reference frequency of 3.3333MHz, which was created by dividing the 10MHz reference by 3. Because the PLL divide ratios never change, the 1500MHz IF is always exactly 1500MHz. Therefore, the actual frequency of the 1400MHz LO is 1500MHz minus the frequency of LOW SYNTH RF.

5.3.2 Wideband PLL

The Wideband PLL creates the 1st RCV LO and 1st GEN LO output signals (1710-2710MHz) by programming the PLL IC with control words that sets the loop output frequency. The output frequency is selected in 10MHz steps.

5.4 DETAILED DESCRIPTION

The High Synthesizer module can be divided into three sections, The 1500MHz RF PLL, the Wideband RF PLL, and the control or digital section.

5.4.1 1500MHz RF PLL

The 1400MHz LO is created by a microwave VCO that utilizes an external buffer amplifier. The amplifier's output is split using a three-way resistive power divider.

Two of the signals become the modules LO outputs. The third signal is amplified and then drives the RF port of mixer U404 where it is mixed with the LOW SYNTH RF input signal from the Low Synthesizer Module (100-119.9999MHz). The mixing creates the 1500MHz IF, which is always maintained at exactly 1500MHz by the PLL. This signal is amplified before going to the bandpass filter that rejects the unwanted mixer products.

The bandpass filter output is connected into the U401 prescaler input at Fin. Internal to the PLL, the 1500MHz input is divided by 450, which is derived by prescaler divider and the N counter inputs. This 3.3333MHz result is one of the two inputs into the internal phase detector. The second input to the internal phase detector is created by dividing the 10MHz reference signal by 3. This signal was input at the OSCIN pin and is divided by the R counter. The output of the phase detector is connected to the loop filter and controls the VCO.

5.4.2 Wideband RF PLL

The 1710-2710MHz LO is created by a pair of separate VCOs, each covering half of the band. The VCOs RF output is amplified by a monolythic buffer amplifier and then goes to a three-way power divider. Two of the signals become the module's 1st LO outputs, while the third signal is amplified to become the feedback input signal for the U301 PLL IC. This input will be internally divided by the prescaler and the N counter as determined by software inputs to become one of three phase detector input frequencies. The other phase detector input is formed by dividing the 10MHz reference in the R counter by 4, 5, or 6. The phase detector output is passed through the loop filter and controls the VCOs.

Selection of the VCOs is accomplished by using a feature of the PLL IC. The FLO output of the PLL is controlled by software to switch the power applied to the VCOs. A low output selects the low frequency VCO. The FLO output also drives a diode switch which selects which VCO is connected to the output amplifier.

5.4.3 Digital Control

The digital sections of both the 1500MHz and Wideband PLL circuits is the programming of the R and N counters and the Function Latches of their PLL IC's

The Wideband PLL is programmed by writing the appropriate instructions into the PLL IC. The 1500MHz PLL loop is fixed programmed but must continue to receive the fixed programming instructions every time the Cochise PLLs are being programmed. Figure 5.4.1 contains the required register loading to program this PLL.

The programming procedure for the Phase Lock Loop (PLL) ICs is described in the PLL IC data sheet, National part # LMX2306/LMX2316/LMX2326. Three registers must be programmed within the IC in order to achieve proper operation of the Loop. Programming is achieved via a serial data stream supplied by 1500 PLL DATA or HISYNTH DATA, through the DATA pin of the IC. Registers are programmed sequentially so a programming sequence consists of three program instructions. Each instruction is clocked serially into a 21-BIT DATA REGISTER with data bits MSB (Most Significant Bit) first. The DATA REGISTER acts as a buffer register that receives the serial data and, based on the 2-bit control instruction, loads the appropriate internal register. The last two bits of the 21-bit data stream provide the control instruction that selects which of the three internal registers receives that data stream.

5.4.3.1 Word Format

Following is a description of how the three registers are utilized to program the Phase Lock Loop circuits for the desired frequency and operational modes.

5.4.3.1.1 R COUNTER Word Format

The R-COUNTER register is programmed for the scaling factor to establish the phase comparison reference frequency for the PLL phase/frequency comparator. The R-COUNTER depiction in Figure 5.4.1 is the serial data stream that must be clocked in to the 21-BIT DATA REGISTER. When the control bits are (0,0) in LSB's 1 and 2, then the 19 remaining bits get loaded into the R COUNTER register. The data transfer is done internally when the Synth Latch line transitions from low to high. As shown, the value programmed into the lower 14 bits of the R-COUNTER determines the divide ratio for the input 10MHz Reference signal. The range of values for the R COUNTER is 3 to 16,383 and the maximum reference frequency specified for the LMX23X6 chip is 40 MHz. The LD Precision (LD Precision controls the digital Lock Detect sensitivity) bit is set to 1.

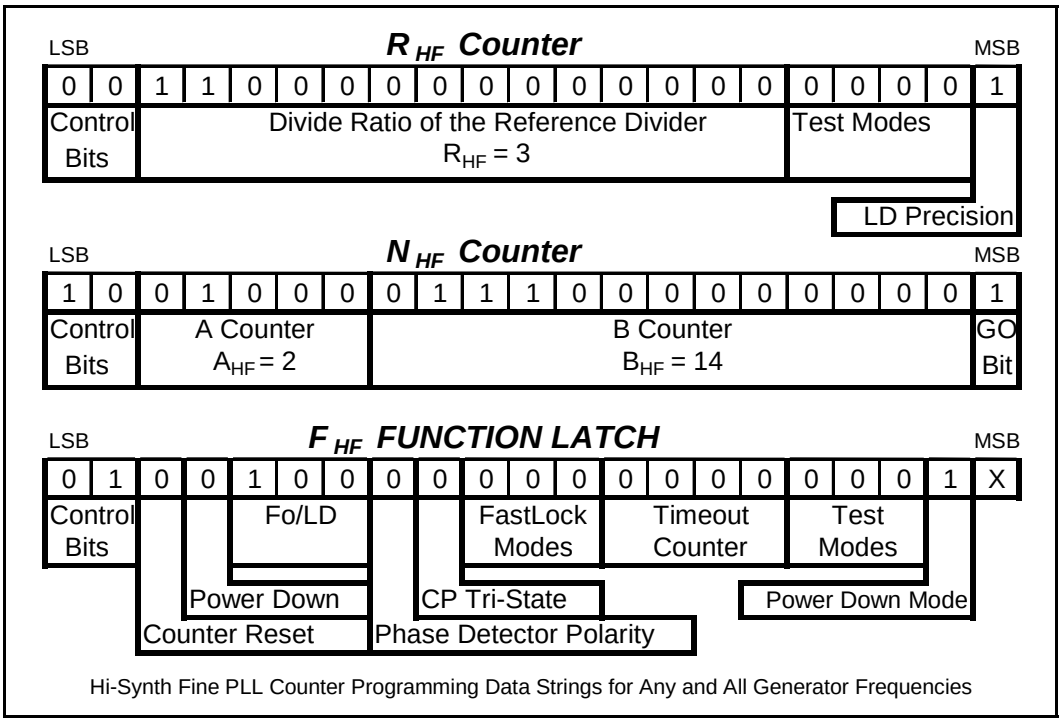


Figure 5.4.1. These Data Strings Provide the Required Register Loading to Program the 1500 PLL Loop

5.4.3.1.2 N Counter Word Format

The VCO output frequency is scaled from the reference frequency by the values programmed into the N COUNTER. A sample of the VCO signal is fed back to the f_{in} pin of the PLL IC and divided down by the N COUNTER to the same frequency as the reference frequency determined by the R COUNTER. This, in affect, multiplies the phase detector reference frequency by the N COUNTER setting to determine the VCO output frequency. The N-COUNTER data structure shown in Figure 5.4.1 portrays the bit stream clocked into the DATA REGISTER for programming the N COUNTER value. The control bits (1,0) determine that the preceding 19 bits will be loaded into the internal N-COUNTER register when the Synth Latch line is asserted. The VCO frequency, f_{vco}, is determined by the A Counter (A) and B Counter (B) values by the following expression;

$f_{vco} = N \times f_{osc}/R = [(P \times B) + A] \times f_{osc}/R$
where;

f_{vco}: Output frequency of external voltage controlled oscillator (VCO).

f_{osc}: Output frequency of the stable reference frequency oscillator (e.g. 10.000000 MHz).

P: Preset modulas of the prescaler (P=32 for the LMX2316/26)

R: Programmed divide ratio of the R COUNTER.

B: Programmed divide value of binary (modulo P) 13-bit programmable counter (3 to 8191).

A: Programmed divide value of the 5-bit swallow counter
($0 \leq A \leq 31$, $A \leq B$ for LMX 2316/26)

Note

The N divide ratio is; N = P x B + A. Therefore the minimum N divide value is 96 (32 x 3) for LMX 2316/26. The maximum is 262,143 ([32 x 8191] + 31) for LMX 2316/26.

The GO Bit (N19) is set to "1" for high gain (1.0 ma) operation of the charge pump or set to "0" for normal charge pump gain (0.25 ma). The Hi-Synth PLLs are set to high gain (logic "1").

5.4.3.1.3 FUNCTION LATCH Word Format

The Function Latch programs additional functionality into the PLLs. The FUNCTION LATCH register is organized as shown in Figure 5.4.1. For the Cochise, we are utilizing only 4 features controlled by the function latch. They are:

FoLD: To use the Digital Lock Detect of the PLL IC, F3 is set to "1" while F4 and F5 are set to "0". This will enable the FoLD pin of the IC to give a logic "1" when the PLL IC achieves lock.

Phase Detector Polarity: F6 is set to correspond to the VCO control characteristics. For negative voltage vs. VCO frequency, F6 is set at a logic "0". If the VCO control slope were positive, the bit would be set at a logic "1". In the High Synthesizer, the VCO control voltage slopes are positive. But, the loop filters each contain an inverting amplifier thereby changing the apparent control slope at the PLL output to negative. The proper bit for F6 is a logic "0" for both PLLs.

FL_0: The IC's FL_0 pin (logic output) is controlled by F9. FL_0 is high when F9 = 1 and low otherwise. This function is used in the Hi-Synthesizer high frequency PLL to select one of two VCOs. Two VCOs are needed to cover the entire 1.7 to 2.7 Gigahertz frequency range. The FL_0 is zero for VCO frequencies 2240 or less. Above this frequency, F9 is programmed to "1" so that FL_0 is high and selects the high frequency VCO.

Power Down Mode: This bit is set to 1 so that synchronous power down could be implemented.

All other Function Latch bits are set to "0" for normal operation in the Cochise Test Set. The Control Bits for normal programming of the Function Latch should be (0, 1).

5.4.3.2 Timing

Data is be supplied to each PLL in a serial format through a Data Input pin on the IC. The serial data must be clocked in one bit at a time and then transferred internally within the IC into one of three registers when the Latch Enable line is activated.

Setup Times (t_{su})	
Synth data to Synth Clock:	20ns. Min.
Synth clock to Synth latch:	32ns. Min.
Hold Time (t_h); Synth clock to Synth Data:	12ns. Min.
Recovery Time (t_r); Synth Latch to Synth Clock:	10ns. Min.
Rise Time and Fall Times (t_r, t_f)	
Synth Latch, Synth Clock, Low Synth Data 1-4	2us. Max.
Pulse width (t_w)	
Synth Latch, Synth Clock, Low Synth Data 1-4	35ns. Min.

Figure 5.4.2 is a timing diagram for the High Synth Data and 1500 PLL Data, Synth Clock, and Synth Latch (Enable).

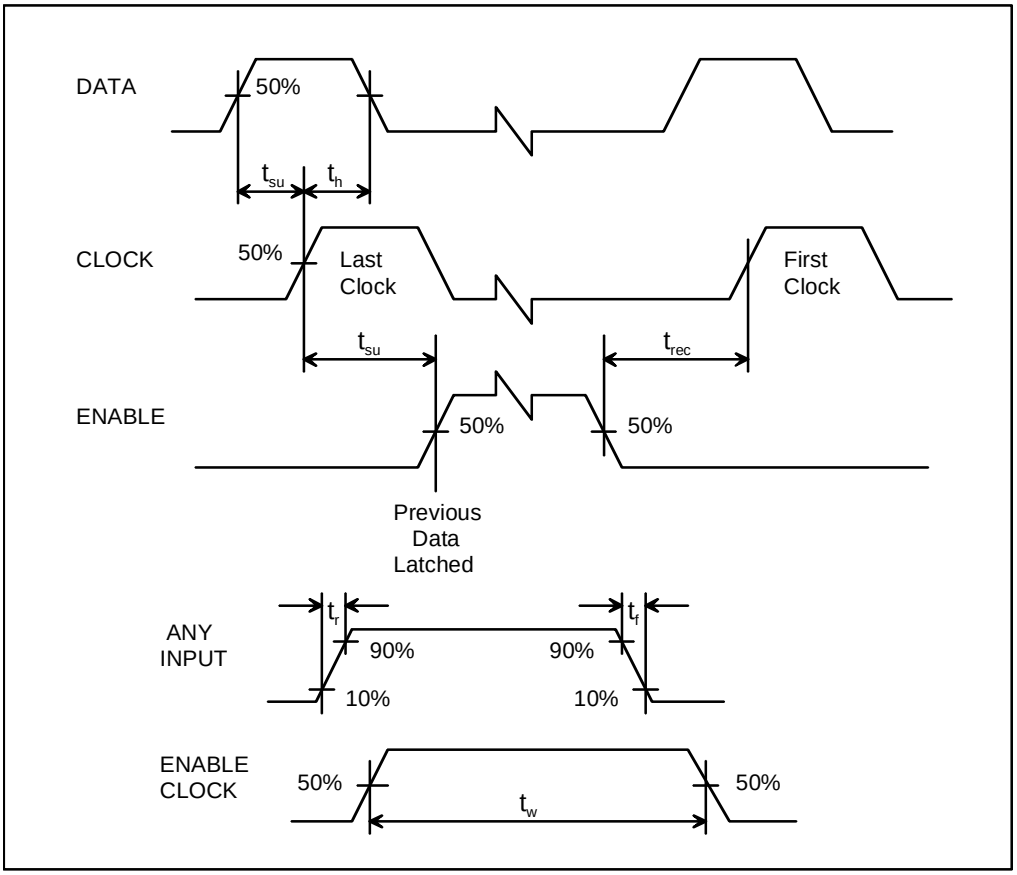


Figure 5.4.2. High Synthesizer Timing

5.4.3.3 Pertinent Equations

For a given Cochise Test Set generator output frequency, the PLLs must be programmed so that the combined result of all the outputs produces the desired result.

In the Cochise, software interprets the user's intention, software displays the user's selection on the screen (test set display), and software generates the instructions that program the appropriate PLLs that synthesize the selected frequency to be provided by the Generator. Figure 5.4.3 shows the composite block diagram of the Low-Synth, the Hi-Synth and the RF Output assemblies that produces the frequency selection for the Cochise Generator.

The expression from Figure 5.4.3 for the generator output frequency, FOUT is:

$F_{OUT} = F_{HC} - 1{,}810.7\text{MHz} + F_C - F_F/160$ (all frequencies in MHz)

Where:

F_{OUT} is the Generator output frequency specified to be 400KHz to 999.9MHz in 100Hz increments.

F_{HC} is the Hi-Synthesizer coarse frequency PLL VCO output (1,710 to 2,710MHz in 10MHz increments)

F_C is the Low-Synthesizer coarse frequency PLL VCO output (102.4 to 122.0MHz in 400KHz increments)

F_F is the Low-Synthesizer fine frequency PLL VCO output (384 to 320.016MHz in 16KHz increments; F_F /160 provides 100Hz increments).

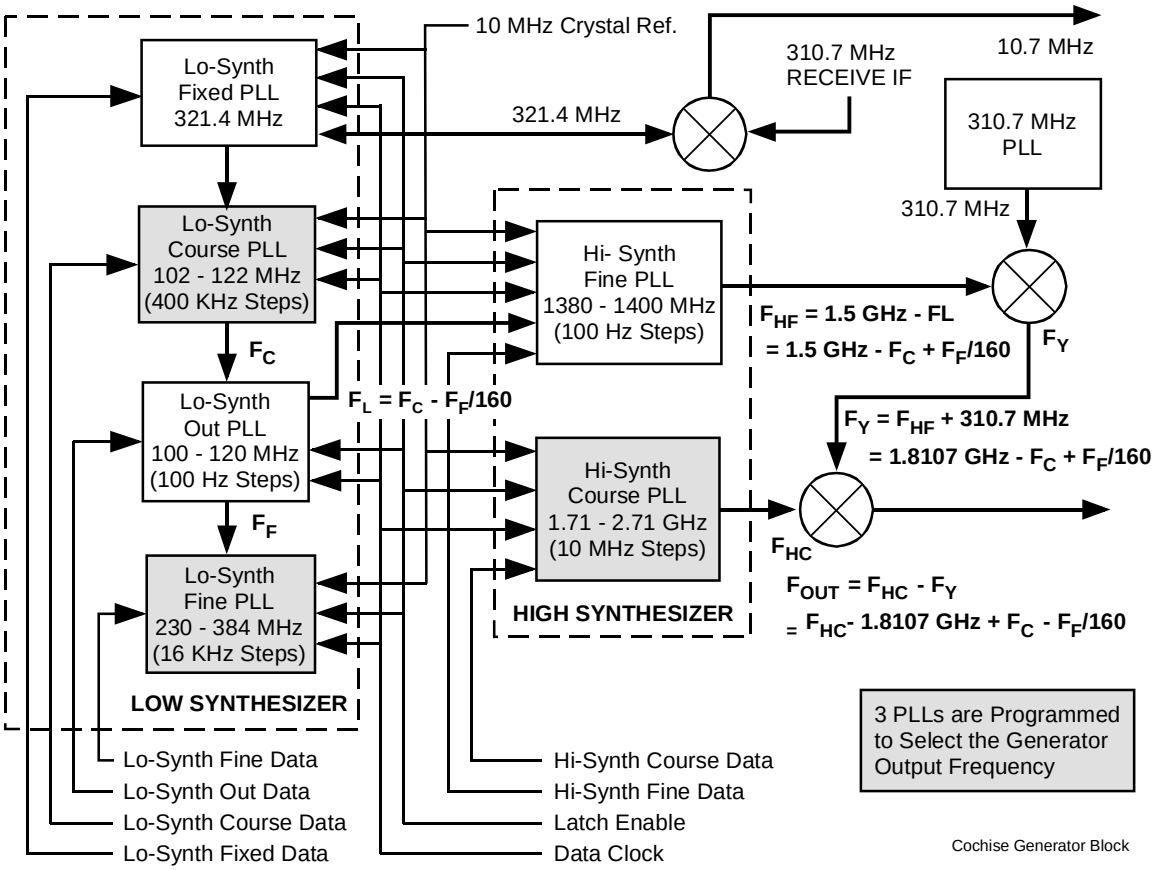


Figure 5.4.3 The Cochise generator frequency is selected by 3 programmable Phase Locked Loops. The generator output frequency is selected by programming the coarse loop (FHF) of the High Synthesizer Assembly and the coarse (FC) and fine (FF) loops of the Low Synthesizer Assembly

5.4.3.4 Calculation of R, N, A, and B Values

For the High Synthesizer Coarse Frequency or Wideband Loop, we can generate the expressions for programming the R-Counter and the N-Counter (B and A values). The R-Counter value is not constant in this loop as in most loops. Additionally we use a feature of the Function Latch to select which of two VCOs is powered to generate the output frequency. The High Synthesizer Coarse Loop PLL frequency expression is:

$$\mathbf{F_{HC} = 1{,}710{,}000{,}000 + 10{,}000{,}000 \times INTEGER\ [(F_G+700{,}000)/10{,}000{,}000)]}$$

Here, the phase/frequency detector reference is variable; and the R counter value is 6, 5, or 4 providing reference frequencies from the 10MHz reference of 1.6666, 2.0 or 2.5MHz respectively. This is varied to maintain a more constant loop gain (less variable loop filter) for this synthesizer.

The N counter value is $N_{HC} = F_{HC} / F_{HCref} = F_{HC} / (10MHz / R_{HC})$. Recalling that N = PxB + A, we can express B_{HC} and A_{HC}, where the counter modulus for this PLL chip is 32, as follows:

$$B_{HC} = INTEGER((F_{HC}/(10{,}000{,}000/R_{HC}))/32)$$
$$A_{HC} = F_{HC}/(10{,}000{,}000/R_{HC}) - 32 \times B_{HC}$$

The programming for the Function Latch needs to call out positive VCO frequency sensitivity, high gain mode for the charge pump, and Flo high or low to select the proper VCO. The following table provides a summary of the programming requirements for the two High Synthesizer PLLs.

Hi-Synthesizer PLLs		
1500 PLL	**Hi-Synth**	F_G<280x10^6,R_{HC}=6 (F_{HC}; 1710-1960)
F_{HF}	F_{HC}	F_G<770x10^6,R_{HC}=5 (F_{HC}; 1970-2460)
R_{HF}=3	R_{HC}=6,5 or 4	$F_G \geq$ 770x10^6,R_{HC}=4 (F_{HC}; 2470-2710)
N=32B+A	N=32B+A	F=(10^7/R)x(32B+A)
N_{HF}=450	N_{HC}=Variable	**Select VCO with Flo Function**
B_{HF}=14	B_{HC}=Var.	**F_G<550x10^6, Flo = 0 ($F_{HC} \leq$ 2240)**
A_{HF}=2	A_{HC}=Var.	**$F_G \geq$ 550x10^6, Flo = 1 ($F_{HC} \geq$ 2250)**

5.4.3.5 Calculation of Loop Filter Bandwidth Stabilization

Loop filter bandwidth relates directly to the N counter value (inverse square root). For a fixed R-Counter value in the Hi Synth Coarse loop, the loop filter bandwidth is changed by 26% as the N-Counter varies the VCO output from 1710 to 2710MHz. One method to diminish the range of values for the N Counter is to decrease the R Counter value in the Hi Synth Coarse loop as the VCO frequency is increased. Decreasing the R Counter increases the reference frequency at the phase detector. As the reference frequency in increased, lower multiples (provided by the N Counter) are required to achieve a given VCO output frequency. The table shows how reprogramming the R Counter value reduces the 26% loop filtering variability to 12%.

Frequency Range (VCO)	***R-Counter Value***	***Reference Frequency***	***N-Counter Value Range***	***Min/Max Filter Bandwidth Ratio***	***Comments***
1710-2710	5	2.00000	855-1355	1.26:1	26 % Change in Filter
1710-1969	6	1.66667	1026-1180	1.1:1.02	10 % Change in Filter
1970-2459	5	2.00000	985-1230	1.12:1	12% Change in Filter
2460-2710	4	2.50000	984-1084	1.05:1	5% Change in Filter

5.4.3.6 Programming Example

To demonstrate the application of the functions to calculate the programming values, this section provides an example where the selected Cochise Generator output frequency is 900MHz. The applicable equations for the three variable PLLs are:

F_{HC} = 1,710,000,000 + 10,000,000 x INTEGER[(F_G+700,000)/10,000,000)]

F_C = 102,400,000 + 400,0000 x INTEGER[(F_G+700,000)/400,000)] - 10,000,000 x INTEGER[(F_G+700,000)/10,000,000)]

F_F = 384,000,000 - 160 x (F_G + 700,000) + 160 x 400,000 x INTEGER[(F_G+700,000)/400,000)].

Substituting F_G = 900MHz for the F_{HC} equation we get the following:

F_{HC} = 1,710,000,000 + 10,000,000 x INTEGER[(F_G+700,000)/10,000,000)]
= 1,710,000,000 + 10,000,000 x INTEGER[(900,000,000+700,000)/10,000,000)]
= 1,710,000,000 + 10,000,000 x INTEGER[(900,700,000)/10,000,000)]
= 1,710,000,000+10,000,000 x INTEGER(90.07)=1,710,000,000+10,000,000x90
= 1,710,000,000 + 900,000,000
= 2,610,000,000 = 2.61GHz

Substituting F_G = 900MHz for the F_C equation we get the following:

F_C = 102,400,000 + 400,0000 x INTEGER[(F_G+700,000)/400,000)] – 10,000,000 x INTEGER[(F_G+700,000)/10,000,000)]
= 102,400,000 + 400,0000 x INTEGER[(900,000,000+700,000)/400,000)] – 10,000,000 x INTEGER[(900,000,000+700,000)/10,000,000)]
= 102,400,000 + 400,0000 x INTEGER[(900,700,000)/400,000)] – 900,000,000
= 102,400,000 + 400,0000 x INTEGER(2,251.75) – 900,000,000
= 102,400,000 + 400,0000 x 2,251 – 900,000,000
= 102,400,000 + 900,400,000 – 900,000,000
= 102,400,000 + 400,0000
= 102,800,000 = 102.8MHz

Substituting F_G = 900MHz for the F_F equation we get the following:

F_F = 384,000,000 - 160 x (F_G + 700,000) + 160 x 400,000 x INTEGER[(F_G+700,000)/400,000)].
= 384,000,000 - 160 x (900,000,000 + 700,000) + 160 x 400,000 x INTEGER[(900,000,000+700,000)/400,000)].
= 384,000,000 - 160 x 900,700,000 + 160 x 400,000 x INTEGER[(900,700,000)/400,000)].
= 384,000,000 – 160 x 900,700,000 + 160 x 900,400,000
= 384,000,000 – 160 x (900,700,000 - 900,400,000)
= 384,000,000 – 160 x 300,000 = 384,000,000 – 48,000,000
= 336,000,000 = 336MHz

To check our results, we use the equation for $F_G = f(F_{HC}, F_C, F_F)$ where we substitute the calculated values and we should get F_G = 900MHz

F_G = F_{HC} + F_C - F_F/160 - 1810.7MHz
= 2,610MHz + 102.8MHz – 336MHz/160 – 1810.7MHz
= (2,610 + 102.8 – 2.1 – 1810.7) MHz
= 900MHz

The frequencies we calculate, as in the previous example, are used to calculate the data strings that must be loaded into the PLL registers of the frequency synthesizers. This then results in the VCO frequencies that produce the generator output. The methodology to generate the data strings is demonstrated next.

From the discussion in Section 5.4.3.4, the register values can be calculated from the desired frequencies needed from the PLLs.

High Synthesizer COARSE LOOP (Hi-Synth Data) R-Register value:
This is given as a variable as shown in the table in section 5.4.3.4. For 900MHz generator output, the table states that R = 4 providing a reference frequency of 2.5MHz (10 MHz/ 4 = 2.5 MHz).

Low Synthesizer COARSE LOOP (Hi-Synth Data) N-Register values:

For **F_{HC} = 2.61GHz**, N = 2,610 MHz/2.5MHz = 1044

B_{HC} = INTEGER(N/P) = INTEGER(N/32) = INTEGER(1044/32) = INTEGER(32.625) = **32**
A_{HC} = N – PxB = N – 32 x B = 1044 – 32 x 32 = 1044 – 1024 = **20**

High Synthesizer COARSE LOOP (Hi-Synth Data) register data strings are shown in Figure 5.4.4 which contains all 3 register programming strings for each PLL of the Hi-Synth Data and 1500 PLL Data on the High Synthesizer Assembly.

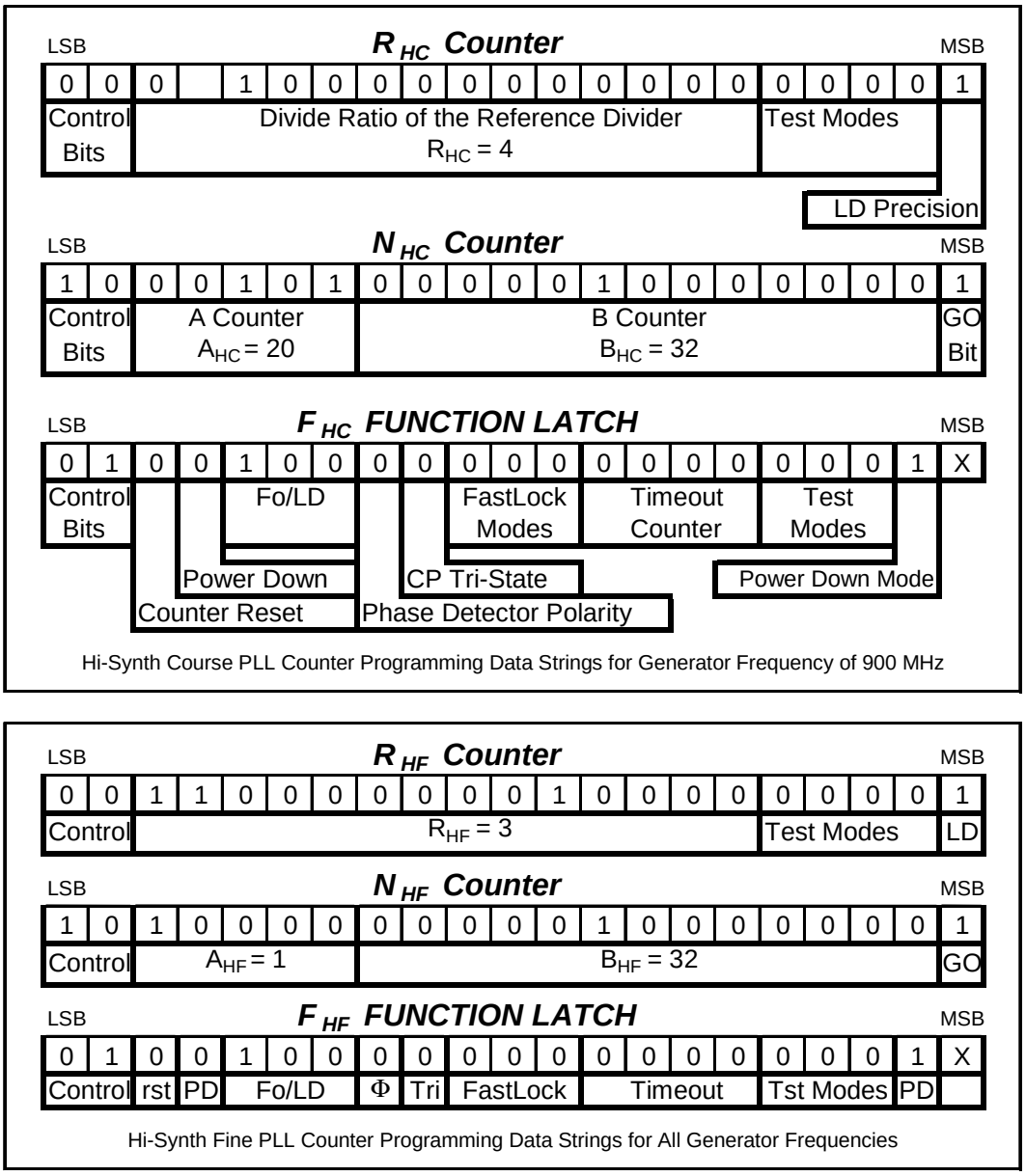


Figure 5.4.4. High Synthesizer Programming Strings for 900.0000MHz Generator Output

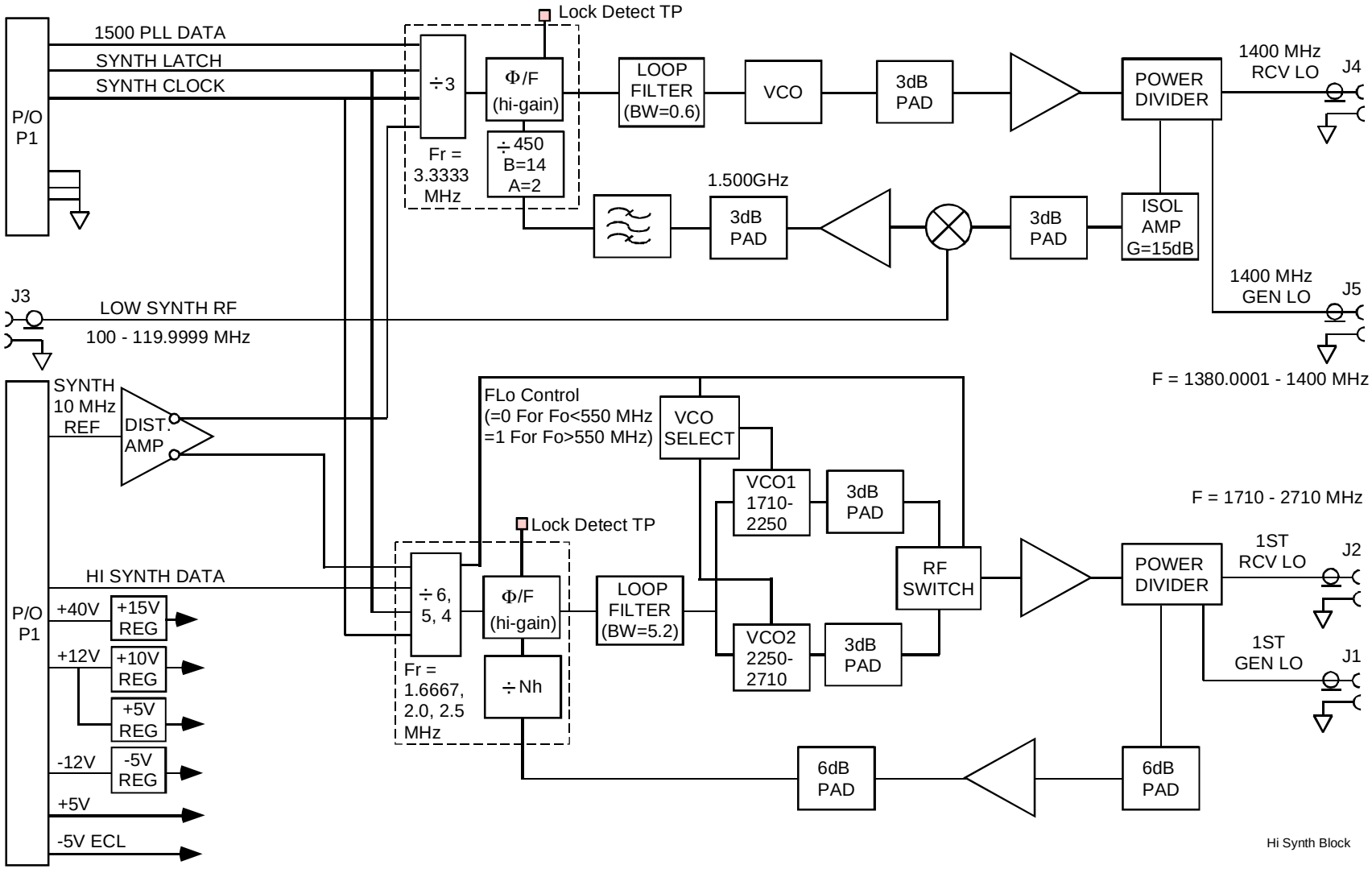
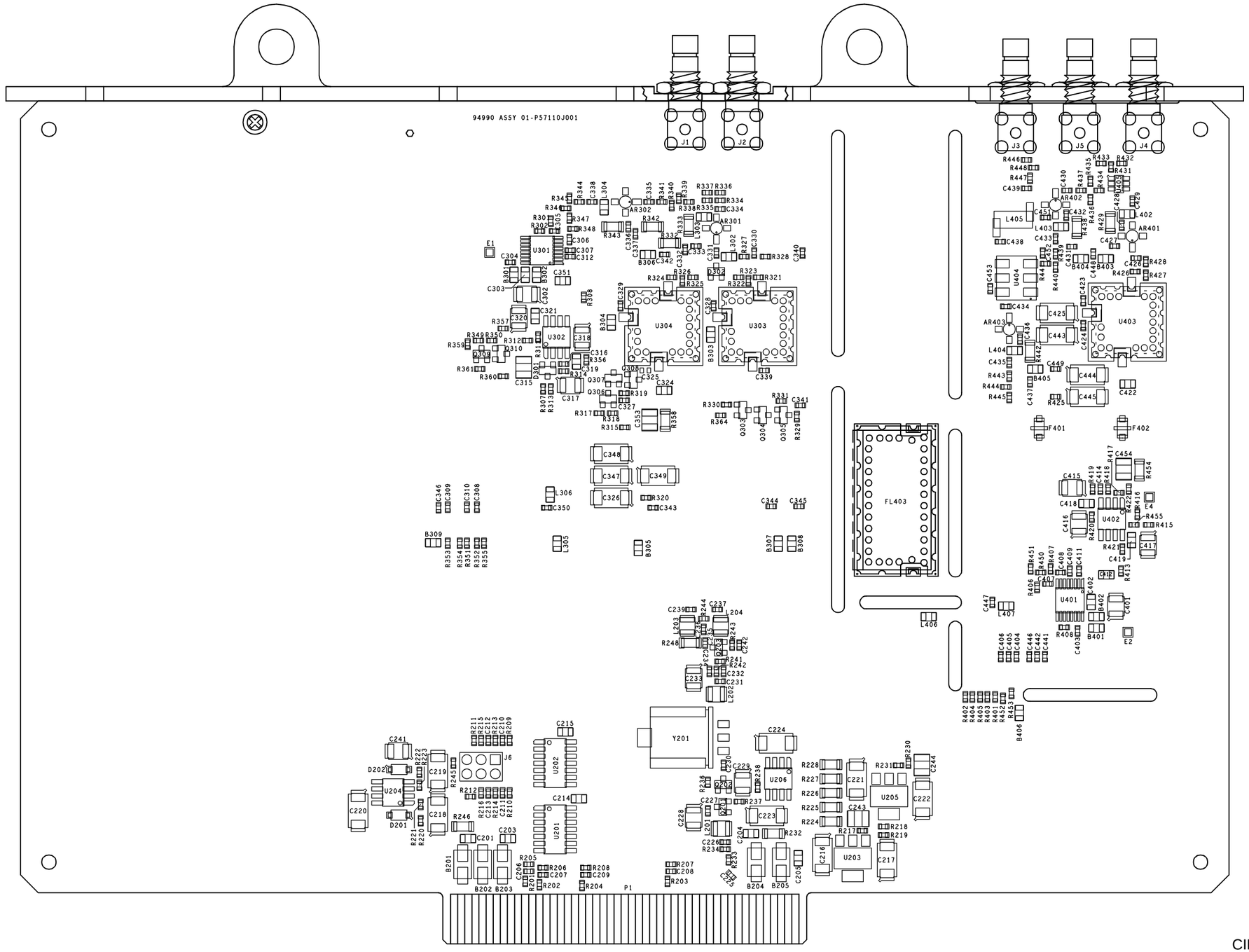


Figure 5.5 High Synthesizer Block Diagram



CIRCUIT CARD ASSEMBLY
HIGH SYNTHESIZER

01-P57110J REV. A

SHEET 1 OF 1

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
-	INITIAL RELEASE	00-08-03	A. GATTO

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A7

2. FOR REFERENCE DRAWINGS REFER TO:
   01-P57110J ASSEMBLY
   12-P57113J TEST PROCEDURE

3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL INDUCTANCE VALUES ARE IN NH.
   ALL CAPACITOR VALUES ARE IN PF.
   ALL VOLTAGES ARE IN DC.

4. TERMINATIONS CODED WITH THE SAME LETTERS OR NUMBERS ARE ELECTRICALLY CONNECTED.

5 DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH MANUFACTURER. ENGINEERING APPROVED EQUIVALENT DEVICE MAY BE USED.

6 TO ALLOW EACH PLL TO BE PROGRAMMED INDIVIDUALLY (I.E. FOR EXTERNAL PROGRAMMING) THE FOLLOWING RESISTOR PLACEMENT IS REQUIRED:

R352	REPLACED BY	R351
R354	REPLACED BY	R355
R403	REPLACED BY	R402
R404	REPLACED BY	R405

NOTE:
AFTER RESISTOR SUBSTITUTION, THE FUNCTIONALITY OF THE DATA AND LATCH ARE INTERCHANGED.

ALL SHEETS ARE THE SAME REVISION STATUS

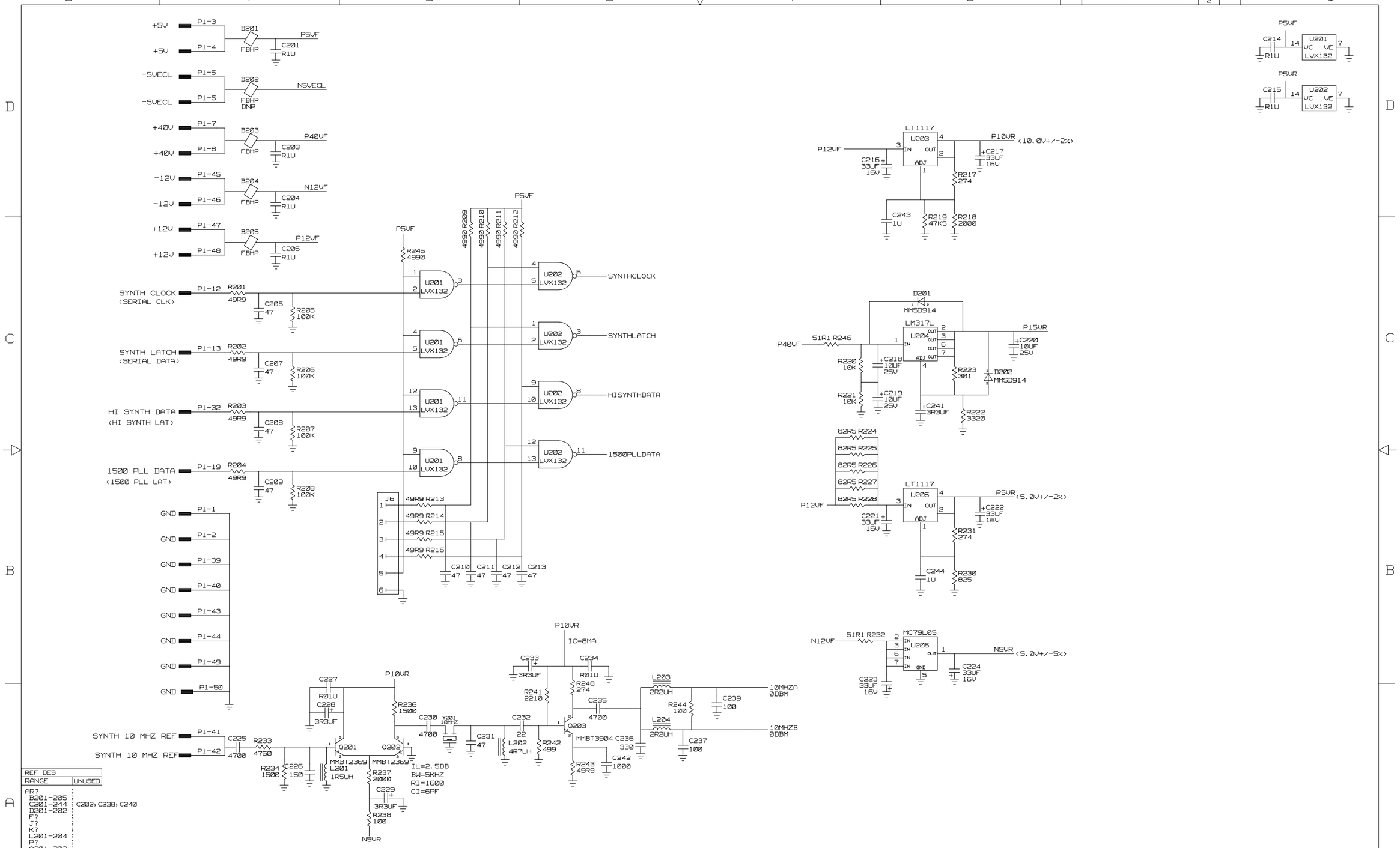
		CONTR	
		ISSRNB35550-476(-)00/08/07	
		APPROVALS	
		DWN P. SCOTT	24-04-00
		CHKR	
		QA T. DAVINO	00-08-07
		MATL J. HARNISH	00-08-03
01-P57110J	COCHISE	MFG W. MACDONALD	00-08-03
NEXT ASSY	USED ON	ENG A. GATTO	00-08-03
APPLICATION		CUST	

MOTOROLA INC.
GOVERNMENT AND SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

TITLE
SCHEMATIC DIAGRAM
HIGH SYNTHESIZER

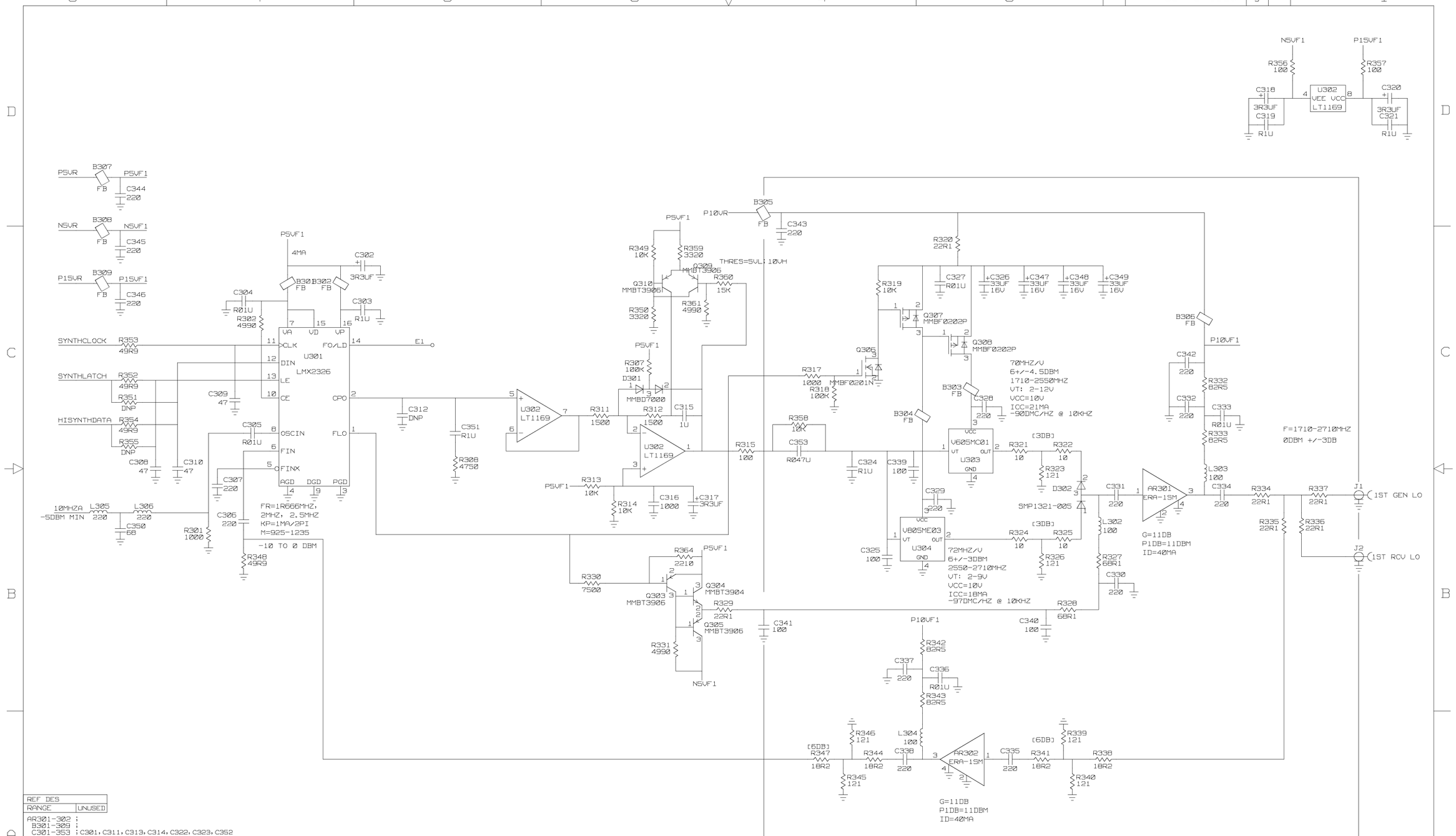
SIZE	CAGE CODE	DWG NO
D	94990	63-P57112J

SCALE NONE SHEET 1 OF 4



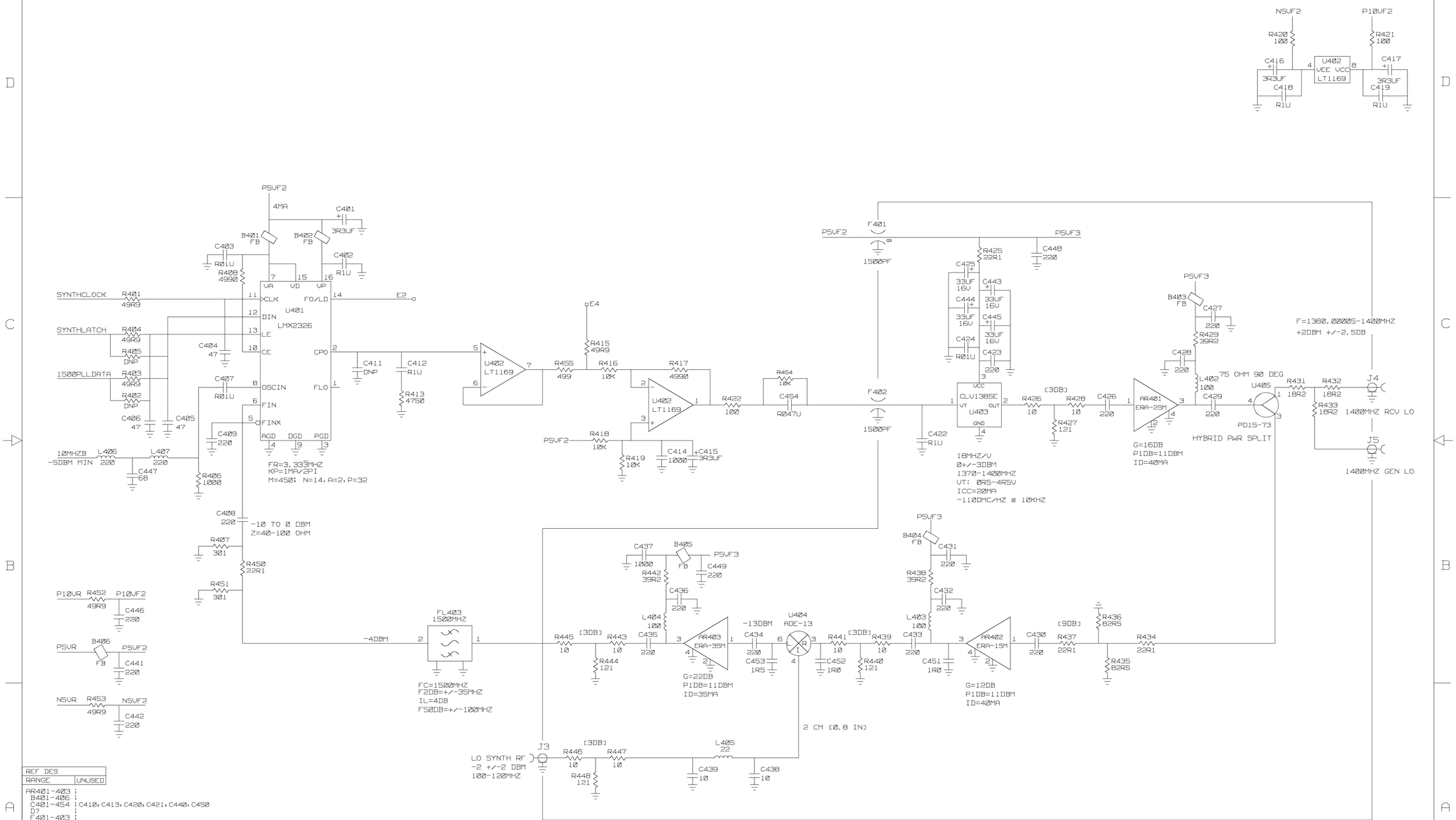
REF DES	
RANGE	UNUSED
AR?	
B201-205	
C201-244	C202, C238, C240
D201-202	
F?	
J?	
K?	
L201-204	
P?	
Q201-203	
R201-248	R229, R239, R240, R247
SW?	
T?	
U201-206	
W?	
Y201	

SIZE	CAGE CODE	DWG NO	REV
D	94990	63-P57112J	-
SCALE NONE		SHEET 2	



REF DES RANGE	UNUSED
AR301-302	
B301-309	
C301-353	C301, C311, C313, C314, C322, C323, C352
D301-302	
F?	
J001-002	
K?	
L302-306	
P?	
Q301-310	Q301, Q302
R301-364	R303-R306, R309, R310, R316, R363
SW?	
T?	
U301-304	
W?	
Y?	

SIZE	CAGE CODE	DWG NO	REV
D	94990	63-P57112J	-
SCALE NONE		SHEET 3	



REF DES RANGE	UNUSED
AR401-403	
B401-406	
C401-454	C410, C413, C420, C421, C440, C450
D?	
F401-403	
J3-5	
K?	
L402-407	
P?	
Q?	
R401-455	R409-R412, R414, R423, R424, R430, R449
SW?	
T?	
U401-405	
W?	
Y?	

SIZE	CAGE CODE	DWG NO	REV
D	94990	63-P57112J	-
SCALE NONE		SHEET 4	

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6.1 GENERAL DESCRIPTION

The Low Synthesizer Module (A9) is installed in the RF cardcage in the fifth slot from the center of the Analyzer.

The Low Synthesizer Module generates two signals. The first is the LOW SYNTH RF signal (100MHz to 119.9999MHz in 100Hz steps) used by the High Synthesizer Module to provide vernier control of both the monitor and generator frequencies. The other signal is the fixed frequency 321.4MHz RCV LO used by the Receiver Module as a local oscillator for monitor functions.

6.2 SIGNALS SUMMARY

6.2A Signal Descriptions

LO SYNTH DATA 1-4. These four inputs are used as serial data lines for programming synthesizer loops 1-4.

LOW SYNTH RF output is sent to the High Synthesizer Module for vernier control of monitor and generate frequencies.

SYNTH CLOCK input is used to, clock data into the four synthesizer loops.

SYNTH LATCH input is used to latch the data serially clocked in.

10 MHz REF input from Frequency Standard Module provides a reference frequency to the synthesizer loops.

321.4 MHz RCV LO output is sent to the Receiver Module where it is used as a local oscillator for monitor functions.

+12V, -12V, and +40V supply power to this module.

6.2B Connector Descriptions

P1 50 (Pin Edge-Connector to RF Motherboard)

pin	
1, 2	GND
3, 6	not used
7, 8	+40V
9-11	not used
12	SYNTH CLOCK
13	SYNTH LATCH
14-25	not used
26	LO SYNTH DATA 1
27	not used
28	LO SYNTH DATA 2
29	not used
30	LO SYNTH DATA 3
31	not used
32	LO SYNTH DATA 4
33, 38	not used
39, 40	GND
41, 42	SYNTH 10MHz REF
43, 44	not used
45, 46	-12V
47, 48	+12V
49, 50	GND

SMB Connectors

J1 LOW SYNTH RF
Frequency: 100 to 119.9999MHz in 100Hz steps
Output level: -2dBm ±2dB
Output impedance: 50Ω nominal
VSWR: 2:1 maximum

J2 321.4MHz RCV LO
Frequency: 321.4MHz
Output level: -2dBm ±2dB
Output impedance: 50Ω nominal
VSWR: 2.1 maximum

6.3 BLOCK DIAGRAM DESCRIPTION

The Low Synthesizer module consists of four phase-locked loops. A combination of three of the loops provides the LOW SYNTH RF signal. The fourth loop generates the 321.4MHz RCV LO signal for the Receiver Module. Each of these loops utilizes a monolithic, integrated frequency synthesizer with a prescaler input. These synthesizers have programmable reference and feedback dividers which require clock, data, and enable lines. Each synthesizer shares clock and enable lines (SYNTH CLK and SYNTH LATCH) but have individual serial data lines (LO SYNTH DATA 1-4).

6.4 DETAILED DESCRIPTION

The VCOs are Hartley configurations. All operate from nominal +10Vdc supplies. Each oscillator uses a tapped microstrip inductor as the tank inductance.

6.4.1 PLL Programming

Data is be supplied to each PLL in a serial format through a Data Input pin on the IC. The serial data must be clocked in one bit at a time and then transferred internally within the IC into one of three registers when the Latch Enable line is activated. All four PLLs must be programmed simultaneously since they use common clock and enable lines.

6.4.1.1 Low Synth PLL Control Word Format

The programming procedure for the Phase Lock Loop (PLL) ICs is described in the PLL IC data sheet, National part # LMX2306/LMX2316/LMX2326. Three registers must be programmed within the IC in order to achieve proper operation. Programming is achieved via a serial data stream supplied through the DATA pin of the IC. Registers are programmed sequentially so a programming sequence consists of three program instructions. Each instruction is clocked serially into a 21-BIT DATA REGISTER with data bits MSB (Most Significant Bit) first. The DATA REGISTER acts as a buffer register that receives the serial data and, based on the 2-bit control instruction, loads the appropriate internal register. The last two bits of the 21-bit data stream provide the control instruction that selects which of the three internal registers receives that data stream.

Following is a description of how the three registers are utilized to program the Phase Lock Loop circuits for the desired frequency and operational modes.

6.4.1.1.1 R COUNTER Word Format

For 3 of the 4 loops, the input 10MHz signal is divided to an appropriate reference. The Low Synthesizer Output loop (LO SYNTH RF in Figure 6.5) has a fixed divide by 8 value for the R-Counter. This ratio works on a difference frequency generated by mixing the OUTPUT LOOP frequency with the Low Synthesizer COARSE LOOP frequency.

The R-COUNTER register is programmed for the scaling factor to establish the phase comparison reference frequency for the PLL phase/frequency comparator. The R-COUNTER depiction in Figure 6.4.1 is the serial data stream that must be clocked in to the 21-BIT DATA REGISTER. When the control bits are (0,0) in C1 and C2, then the 19 remaining bits get loaded into the R COUNTER register. The data transfer is done internally when the Synth Latch line transitions from low to high. As shown, the value programmed into the lower 14 bits of the R-COUNTER determines the divide ratio for the input reference signal. The range of values for the R COUNTER is 3 to 16,383 and the maximum reference frequency specified for the LMX23X6 chip is 40MHz. The LD Precision (LD Precision controls the digital Lock Detect sensitivity) bit is set to 1.

6.4.1.1.2 N COUNTER Word Format

The VCO output frequency is scaled from the reference frequency by the values programmed into the N COUNTER. A sample of the VCO signal is fed back to the f_{in} pin of the PLL IC and divided down by the N COUNTER to the same frequency as the reference frequency determined by the R COUNTER. This, in affect, multiplies the phase detector reference frequency by the N COUNTER setting to determine the VCO output frequency.

The N-COUNTER data structure shown in Figure 6.4.2 portrays the bit stream clocked into the DATA REGISTER for programming the N COUNTER value. The control bits (1,0) determine that the preceding 19 bits will be loaded into the internal N-COUNTER register when the Synth Latch line is asserted. The VCO frequency, f_{vco}, is determined by the A Counter (A) and B Counter (B) values by the following expression;

$$f_{vco} = N \times f_{osc}/R = [(P \times B) + A] \times f_{osc}/R$$

where;

f_{vco}: Output frequency of external voltage controlled oscillator (VCO).

f_{osc}: Output frequency of the stable reference frequency oscillator (e.g. 10.000000MHz).

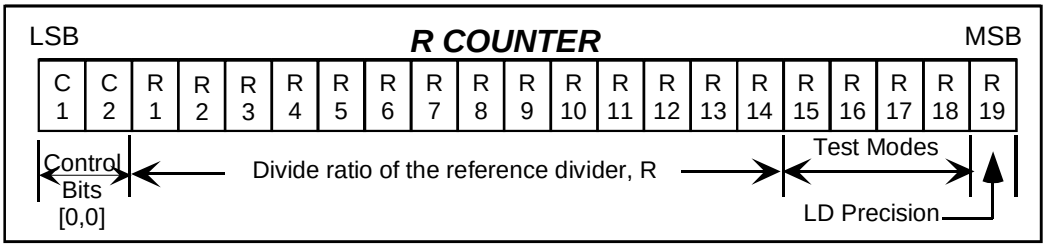


Figure 6.4.1.1 The R COUNTER sets the divide ratio to divide the 10MHz Ref oscillator (or other reference) to the reference frequency at the PLL phase/frequency detector

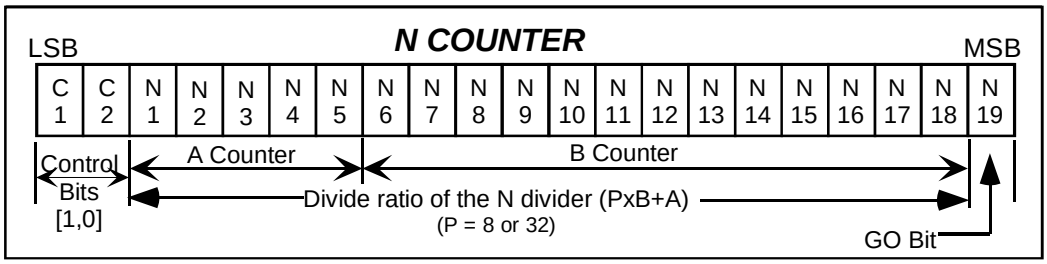


Figure 6.4.2. The N COUNTER determines the VCO frequency by setting a multiplication value in the N COUNTER that translates the phase comparator reference frequency to the VCO frequency

P: Preset modulus of the prescaler (P=8 for the LMX2306)
R: Programmed divide ratio of the R COUNTER.
B: Programmed divide value of binary (modulo P) 13-bit programmable counter (3 to 8191).
A: Programmed divide value of the 5-bit swallow counter (0≤A≤7, A≤B for LMX 2306)

Note

The N divide ratio is; N = P x B + A. Therefore the minimum N divide value is 24 (8 x 3) for LMX 2306. The maximum is 65,535 ([8 x 8191] + 7) for LMX 2306.

The GO Bit is set to "1" for high gain (1.0mA) operation of the charge pump or set to "0" for normal charge pump gain (0.25mA). Only the 321.4MHz Loop is set to high gain in the Low Synthesizer.

6.4.1.1.3 FUNCTION LATCH Word Format

The Function Latch programs additional functionality into the PLLs. The FUNCTION LATCH register is organized as shown in Figure 6.4.3. For the Low Synthesizer, we are utilizing only 3 features controlled by the function latch.

The 3 controls that are used in the function latch for the Low Synthesizer are the following:

FoLD: To use the Digital Lock Detect of the PLL IC, F3 is set to "1" while F4 and F5 are set to "0". This will enable the FoLD pin of the IC to give a logic "1" when the PLL IC achieves lock.

Phase Detector Polarity: F6 is set to correspond to the VCO control characteristics. For negative voltage vs. VCO frequency, F6 is set at a logic "0". If the VCO control slope were positive, the bit would be set at a logic "1". In the Low Synthesizer, the VCO control voltage slopes are positive. But, the loop filters each contain an inverting amplifier thereby changing the apparent control slope at the PLL output to negative. The proper bit for F6 is a logic "0" for all four PLLs.

Power Down Mode: This bit is set to 1 so that synchronous power down could be implemented.

All other Function Latch bits are set to "0" for normal operation in the Cochise Test Set. The Control Bits for normal programming of the function latch should be (0, 1).

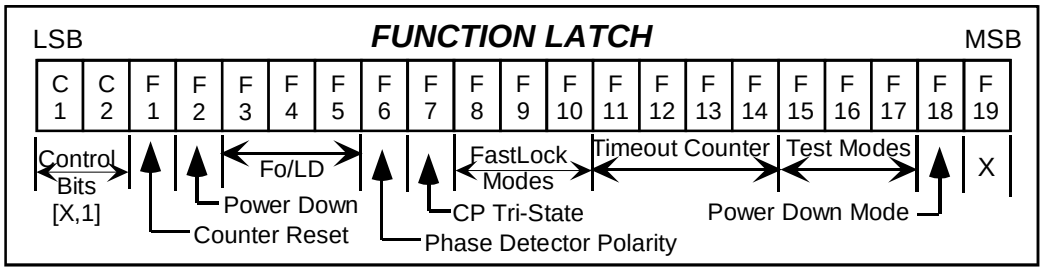


Figure 6.4.3. The FUNCTION LATCH controls several important characteristics of the PLL IC such as VCO polarity, Digital Lock Detect and other features for PLL operational enhancements

6.4.1.2 Switching Characteristics

Data shall be clocked in on a low-to-high transition of the Synth Clock line and shall be latched on a low-to-high transition of the Synth Latch line.

Setup Times (t_{su})	
Synth data to Synth Clock:	20ns. min.
Synth clock to Synth latch:	32ns. min.
Hold Time (t_h)	
Synth clock to Synth Data:	12ns. min.
Recovery Time (t_r)	
Synth Latch to Synth Clock:	10ns. min.
Rise Time and Fall Times (t_r, t_f)	
Synth Latch, Synth Clock, Low Synth Data 1-4	2us. max.
Pulse width (t_w)	
Synth Latch, Synth Clock, Low Synth Data 1-4	35ns. min.

Figure 6.4.4 is a timing diagram for the Low Synth Data 1-4, Synth Clock, and Synth Latch (Enable).

6.4.1.3 Pertinent Equations

For a given Cochise Test Set generator output frequency, the PLLs must be programmed so that the combined result of all the outputs produces the desired result.

In the Cochise, software interprets the user's intention, software displays the user's selection on the screen (test set display), and software generates the instructions that program the appropriate PLLs that synthesize the selected frequency to be provided by the Generator. Figure 6.4.5 shows the composite block diagram of the Low-Synth, the Hi-Synth and the RF Output assemblies that produces the frequency selection for the Cochise Generator.

The expression from Figure 6.4.5 for the generator output frequency, F_{OUT} is:

$F_{OUT} = F_{HC} - 1{,}810.7\text{MHz} + F_C - F_F/160$
(all frequencies in MHz)

Where:

F_{OUT} is the Generator output frequency specified to be 400KHz to 999.9Hz in 100Hz increments.

F_{HC} is the Hi-Synthesizer coarse frequency PLL VCO output (1,710 to 2,710MHz in 10MHz increments)

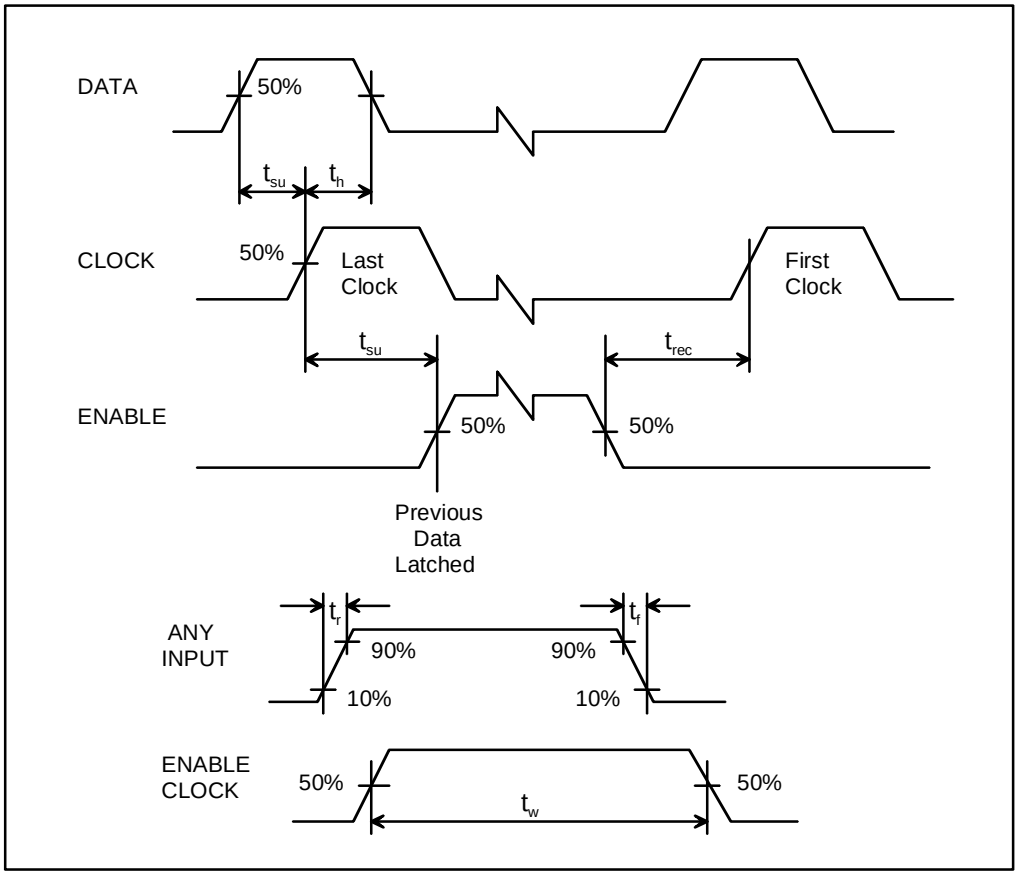


Figure 6.4.4. Timing Diagram Showing the Relationship of PLL Programming Waveforms

F_C is the Low-Synthesizer coarse frequency PLL VCO output (102.4 to 122.0MHz in 400KHz increments)
F_F is the Low-Synthesizer fine frequency PLL VCO output (384 to 320.016MHz in 16KHz increments).

6.4.1.3.1 Calculation of R, N, A, and B Values

For the Low Synthesizer Coarse and Vernier Frequency Loops, we can generate the expressions for programming the R-Counter and the N-Counter (B and A values).

$$\mathbf{F_C = 102{,}400{,}000 + 400{,}0000 \times INTEGER[(F_G+700{,}000)/400{,}000)] - 10{,}000{,}000 \times INTEGER[(F_G+700{,}000)/10{,}000{,}000)]}$$

$$\mathbf{F_F = 384{,}000{,}000 - 160 \times (F_G + 700{,}000) + 160 \times 400{,}000 \times INTEGER[(F_G+700{,}000)/400{,}000)].}$$

The N counter value is $N = F / F_{ref} = F / (10MHz / R)$. Recalling that $N = PB + A$, we can express B and A, where the counter modulus for these PLL chips is 8, as follows:

$$B = INTEGER(N/P) = INTEGER(N/8) = ((F/(10{,}000{,}000/R))/8)$$
$$A = N – PxB = N – 8 \times B = F/(10{,}000{,}000/R) – 8 \times B$$

The programming for the PLLs needs to call out positive VCO frequency sensitivity and low gain mode for the charge pumps (except high for the fixed loop).

The table following summarizes the programming values for the PLL counters.

Data 1 (Output)	Data 2 (Course)	Data 3 (Fine.Vernier)	Data 4 (Fixed)
F_L	$\mathbf{F_C}$	$\mathbf{F_F}$	321.4 MHs
R_L=8	R_C=25	R_F=625	R_X=50
N=8B+A	N=8B+A	N=8B+A	N=8B+A
N_L=1280	N_C=Variable	N_F=Variable	N_X=1607
B_L=160	B_C=Var.	B_F=Var.	B_X=200
A_L=0	A_C=Var.	A_F=Var.	A_X=7
Charge Pump=Low	Charge Pump=Low	Charge Pump=Low	Charge Pump=High

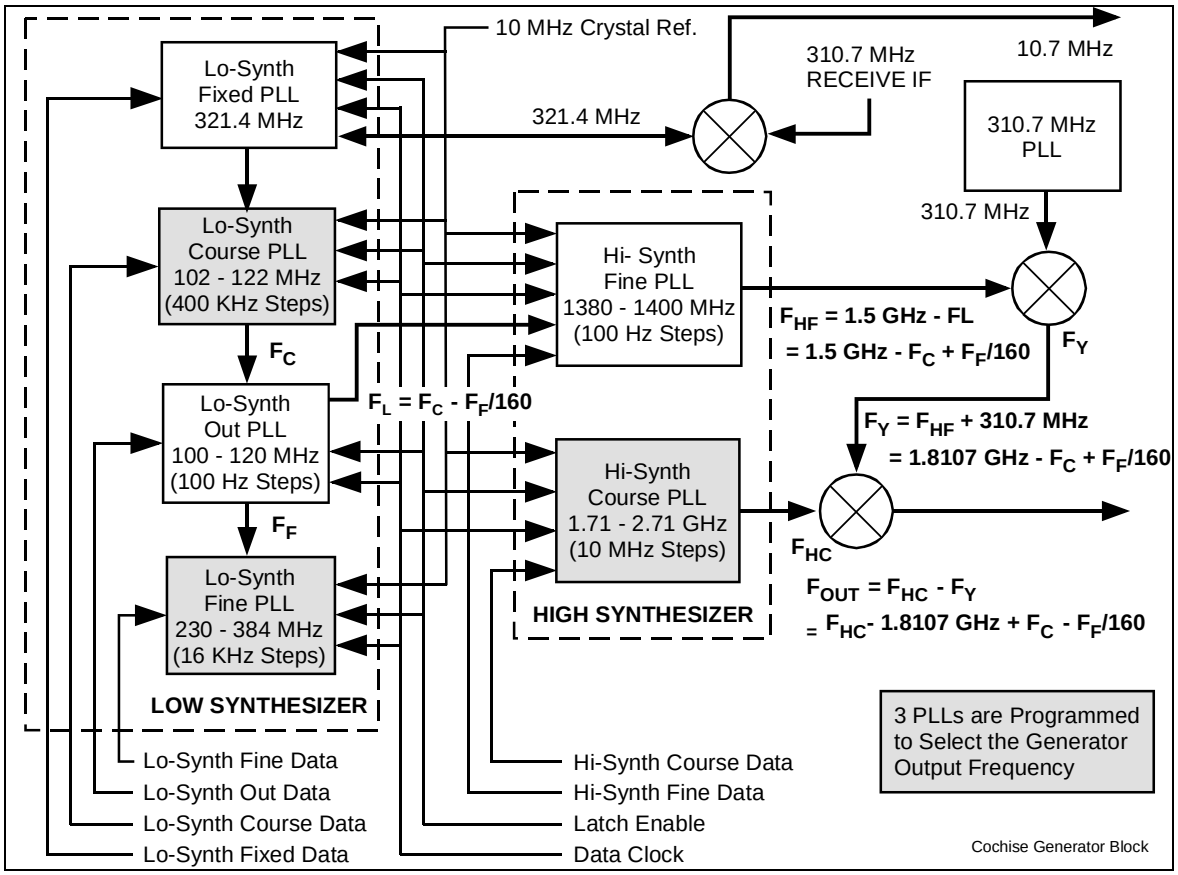


Figure 6.4.5. The Cochise generator frequency is selected by 3 programmable Phase Locked Loops. The generator output frequency is selected by programming the coarse loop (FHF) of the High Synthesizer Assembly and the coarse (FC) and fine (FF) loops of the Low Synthesizer Assembly

6.4.1.3.2 Programming Example

To demonstrate the application of the functions to calculate the programming values, this section provides an example where the selected Cochise Generator output frequency is 900MHz.

The applicable equations for the three variable PLLs are;

F_{HC} = 1,710,000,000 + 10,000,000 x INTEGER[(F_G+700,000)/10,000,000)]
F_C = 102,400,000 + 400,0000 x INTEGER[(F_G+700,000)/400,000)] - 10,000,000 x INTEGER[(F_G+700,000)/10,000,000)]
F_F = 384,000,000 - 160 x (F_G + 700,000) + 160 x 400,000 x INTEGER[(F_G+700,000)/400,000)].

Substituting F_G = 900MHz for the F_{HC} equation we get the following:

F_{HC} = 1,710,000,000 + 10,000,000 x INTEGER[(F_G+700,000)/10,000,000)]
= 1,710,000,000 + 10,000,000 x INTEGER[(900,000,000+700,000)/10,000,000)]
= 1,710,000,000 + 10,000,000 x INTEGER[(900,700,000)/10,000,000)]
= 1,710,000,000+10,000,000 x INTEGER(90.07)=1,710,000,000+10,000,000x90
= 1,710,000,000 + 900,000,000
= 2,610,000,000 = 2.61GHz

Substituting F_G = 900MHz for the F_C equation we get the following:

F_C = 102,400,000 + 400,0000 x INTEGER[(F_G+700,000)/400,000)] – 10,000,000 x INTEGER[(F_G+700,000)/10,000,000)]
= 102,400,000 + 400,0000 x INTEGER[(900,000,000+700,000)/400,000)] – 10,000,000 x INTEGER[(900,000,000+700,000)/10,000,000)]
= 102,400,000 + 400,0000 x INTEGER[(900,700,000)/400,000)] – 900,000,000
= 102,400,000 + 400,0000 x INTEGER(2,251.75) – 900,000,000
= 102,400,000 + 400,0000 x 2,251 – 900,000,000
= 102,400,000 + 900,400,000 – 900,000,000
= 102,400,000 + 400,0000
= 102,800,000 = 102.8MHz

Substituting F_G = 900MHz for the F_F equation we get the following:

F_F = 384,000,000 - 160 x (F_G + 700,000) + 160 x 400,000 x INTEGER[(F_G+700,000)/400,000)].
= 384,000,000 - 160 x (900,000,000 + 700,000) + 160 x 400,000 x INTEGER[(900,000,000+700,000)/400,000)].
= 384,000,000 - 160 x 900,700,000 + 160 x 400,000 x INTEGER[(900,700,000)/400,000)].
= 384,000,000 – 160 x 900,700,000 + 160 x 900,400,000
= 384,000,000 – 160 x (900,700,000 - 900,400,000)
= 384,000,000 – 160 x 300,000 = 384,000,000 – 48,000,000
= 336,000,000 = 336MHz

To check our results, we use the equation for F_G = f(F_{HC}, F_C, F_F) where we substitute the calculated values and we should get F_G = 900MHz
F_G = F_{HC} + F_C - F_F/160 - 1810.7MHz
= 2,610MHz + 102.8MHz – 336MHz/160 – 1810.MHz
= (2,610 + 102.8 – 2.1 – 1810.7)MHz
= 900MHz

The frequencies we calculate, as in the previous example, are used to calculate the data strings that must be loaded into the PLL registers of the frequency synthesizers. This then results in the VCO frequencies that produce the generator output. The methodology to generate the data strings is demonstrated next.

From the discussion in Section 6.4.1.3.1, the register values can be calculated from the desired frequencies needed from the PLLs.

Low Synthesizer COARSE LOOP (Data 2) R-Register value:

To generate a reference frequency of 400KHz, R = 10MHz/400KHz = 25.

Low Synthesizer COARSE LOOP (Data 2) N-Register values:
For **F_C = 102.8MHz**, N = 102.8MHz/400KHz = 257

B_C = INTEGER(N/P) = INTEGER(N/8) = INTEGER(257/8) = INTEGER(32.125) = **32**
A_C = N – PxB = N – 8 x B = 257 – 8 x 32 = 257 – 256 = **1**

Low Synthesizer VERNIER LOOP (Data 3) R-Register value:

To create a reference frequency of 16KHz, R = 10MHz/16KHz = 625.

Low Synthesizer VERNIER LOOP (Data 3) N-Register values:
For **F_F = 336,000,000 = 336MHz**, N = 336MHz/16KHz = 21,000

B_F = INTEGER(N/P) = INTEGER(N/8) = INTEGER(21,000/8) = INTEGER(2,625) = **2,625**

A_F = N – PxB = N – 8 x B = 21,000 – 8 x 2,625 = 21,000 – 21,000 = **0**

Figure 6.4.6 shows not only the variable data strings for a 900.0000MHz generator frequency, but also displays the data strings for the two fixed program PLLs.

LSB — ***R_C Counter*** — MSB

0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Control		R_C = 25														Test Modes				LD

LSB — ***N_C Counter*** — MSB

1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Control		A_C = 1					B_C = 32													GO

LSB — ***F_C FUNCTION LATCH*** — MSB

0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X
Control		rst	PD	Fo/LD			Φ	Tri	FastLock			Timeout				Tst Modes			PD	

Low-Synth Course (Data 2) PLL Counter Programming Data Strings for Generator Freq. of 900.0000 MHz

LSB — ***R_F Counter*** — MSB

0	0	1	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	1
Control		R_F = 625														Test Modes				LD

LSB — ***N_F Counter*** — MSB

1	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	1	0	0
Control		A_F = 0					B_F = 2,625													GO

LSB — ***F_F FUNCTION LATCH*** — MSB

0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X
Control		rst	PD	Fo/LD			Φ	Tri	FastLock			Timeout				Tst Modes			PD	

Low-Synth Fine (Data 3) PLL Counter Programming Data Strings for Generator Frequency of 900.0000 MHz

LSB — ***R_L Counter*** — MSB

0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Control		R_L = 8														Test Modes				LD

LSB — ***N_L Counter*** — MSB

1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
Control		A_L = 1					B_L = 32													GO

LSB — ***F_L FUNCTION LATCH*** — MSB

0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X
Control		rst	PD	Fo/LD			Φ	Tri	FastLock			Timeout				Tst Modes			PD	

Low-Synth RF (Data 1) PLL Counter Programming Data Strings for Any and All Generator Frequencies

LSB — ***R_X Counter*** — MSB

0	0	0	1	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	1
Control		R_F = 50														Test Modes				LD

LSB — ***N_X Counter*** — MSB

1	0	1	1	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1
Control		A_X = 7					B_X = 200													GO

LSB — ***F_X FUNCTION LATCH*** — MSB

0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	X
Control		rst	PD	Fo/LD			Φ	Tri	FastLock			Timeout				Tst Modes			PD	

Low-Synth Fixed (Data 4) PLL Counter Programming Data Strings for Any and All Generator Frequencies

Figure 6.4.6. Programming strings for Low Synth variable and fixed PLLs for a generator frequency of 900.0000MHz

6.4.2 LOW SYNTH RF

The LOW SYNTH RF signal is generated by the interaction of three phase-locked loops. This signal can range from 100MHz to 119.9999MHz in I00Hz steps. The three loop arrangement provides low noise and a small step size without a “close-in” reference spur. The output signal is used by the High Synthesizer module and is at a nominal level of -2 dBm into 50 ohms. Each loop is described in the following paragraphs.

6.4.2.1 Vernier Loop

This loop uses the system 10MHz clock as a reference input and generates 320.016MHz to 384.0MHz in steps of 16KHz. The Vernier PLL loop internal reference frequency is 16KHz.

6.4.2.2 Coarse Loop

This loop uses the system 10MHz clock as a reference input. The loop generates 102.4MHz to 122MHz in steps of 400KHz. The Coarse PLL loop reference frequency is 400KHz.

6.4.2.3 Output Loop

The Output Loop generates a 100.0MHz to 119.9999MHz output frequency in steps of 100Hz. This loop uses the output of the Vernier Loop as a reference input. This reference input is divided by 1280 to provide an internal reference frequency of 250.0125 to 300.0KHz in 12.5Hz steps.

The feed back signal present in the Output Loop is derived from the difference between the output frequency and the Coarse Loop frequency. This difference frequency is obtained at the IF Mixer port and maintained between 2.0001MHz and 2.4MHz by the acquisition circuitry.

6.4.2.4 Low Synth Output PLL Capture Circuit

The Low Synthesizer Output Loop VCO implementation operates to hold the difference frequency between it and the Coarse Loop to 2.25 ± 0.25MHz (the exact lock frequency being determined by the Fine Loop frequency). This difference can be achieved with the Output VCO either above or below the Coarse Loop by the desired amount. Proper operation of the Low-Synth Assembly demands that the Output VCO be below the Coarse Loop VCO. To insure that the two VCOs align in the proper relationship (Output VCO frequency below the Coarse VCO frequency), a special auto-alignment circuit has been implemented. This circuit operates on the charge pump terminal of the Output PLL IC to insure that the desired relative frequencies, i.e. Output VCO frequency below the Coarse VCO frequency, are always maintained. In fact, if the Output Loop is not locked, the circuitry “ping-pongs” the Output VCO frequency between limits that keep it in close proximity (± 4MHz) to the desired difference frequency compared to the Coarse VCO.

Figure 6.4.7 is a schematic of the “Ping-Pong” circuit that performs the auto-alignment function to keep the proper frequency relationship between the Coarse VCO and the Output VCO.

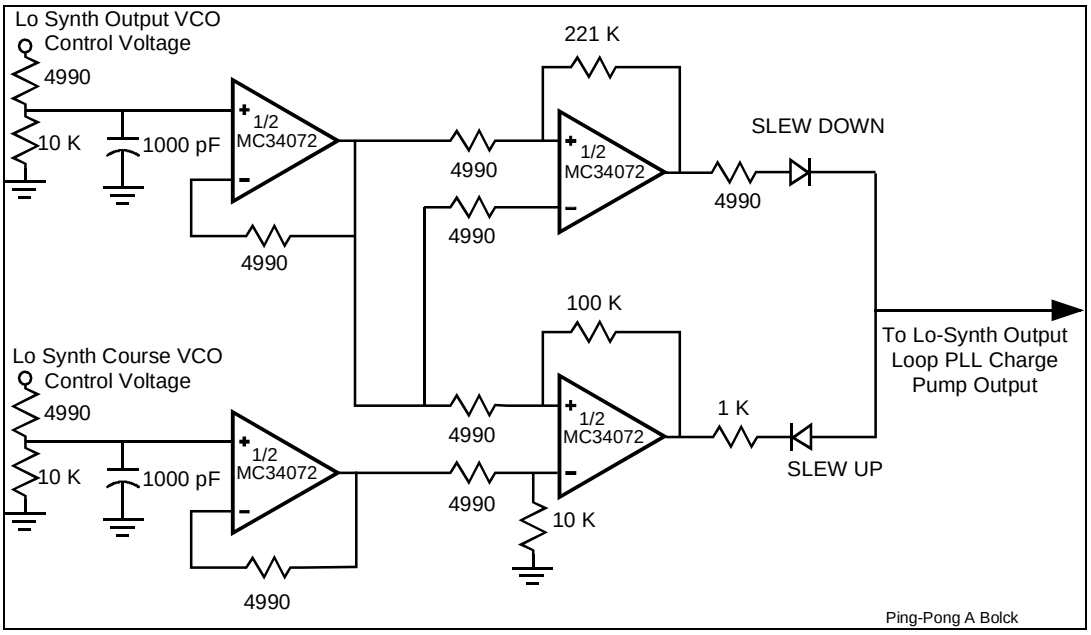


Figure 6.4.7. The Auto-Alignment Circuit is implemented with two integrated circuits that monitor the two VCO voltages and couple to the Output PLL IC Charge Pump Terminal via two diodes in order to over-ride the PLL Operation if required

The Auto-Alignment Circuit has three states. The dominant state is the Normal State when the Loops are properly aligned and locked. Another important state is the Slew Down State which prevents the Output Loop from attempting to phase lock when it satisfies the desired difference frequency but it is above rather than below the Coarse frequency. A third state is the Slew Up state which hastens the capture and lock time for the Output Loop when it is found more than 6MHz below the Coarse Loop. The three states are described in more detail as follows:

Normal State: When both loops are locked in the appropriate relative alignment (Output VCO frequency 2.25 ± 0.25MHz below the Coarse VCO frequency), the two diodes connecting to the Output Loop PLL charge pump are both reverse biased and the "Ping-Pong" circuit is disconnected from the loop. This normal condition is illustrated in Figure 6.4.8 where the "Ping-Pong" circuit schematic has been annotated with node voltages that are representative of nominal operation.

Slew Down State: If the Output Loop is attempting to control its VCO frequency above the Coarse Loop VCO frequency, the "Ping-Pong" circuit will forward bias the SLEW DOWN diode and drive the Output Loop VCO so that the PLL will capture and lock to the correct operating point. This SLEW DOWN operation is illustrated in Figure 6.4.9 where the schematic has been annotated with node voltages that represent the desired SLEW DOWN condition.

Slew Up State: If the Output Loop VCO frequency is excessively (more than 6 MHz) below the Coarse Loop VCO frequency, the SLEW UP diode will be forward biased. This will drive the Output Loop charge pump voltage to increase the VCO control voltage thereby increasing the Output Loop frequency. This enhances the capture capability of the output loop. This SLEW UP operation is illustrated in Figure 6.4.10 where the schematic has been annotated with node voltages that represent the SLEW UP condition.

There are some assumptions that have to hold for the Auto-Alignment circuit to function properly. The most important is that the VCO voltage characteristics (control voltage vs. VCO output frequency) for the Output Loop VCO and the Coarse Loop VCO are very similar. Also the frequency vs. voltage slope is approximately 3.3MHz/Volt. These assumptions are expected to hold as the circuit topologies for the two VCOs are identical. And generally it is also expected that the components being installed onto a printed wiring assembly will come from the same manufacturing lot.

6.4.3 321.4MHz RCV LO

This signal is derived from a single phase-locked loop. This loop uses the system 10MHz as a reference. The reference is divided by 50 thus providing a 200KHz loop reference frequency. The loop output is a fixed frequency 321.4MHz signal. This signal is used by the Receiver module and is output at a nominal level of –2dBm into 50 ohms.

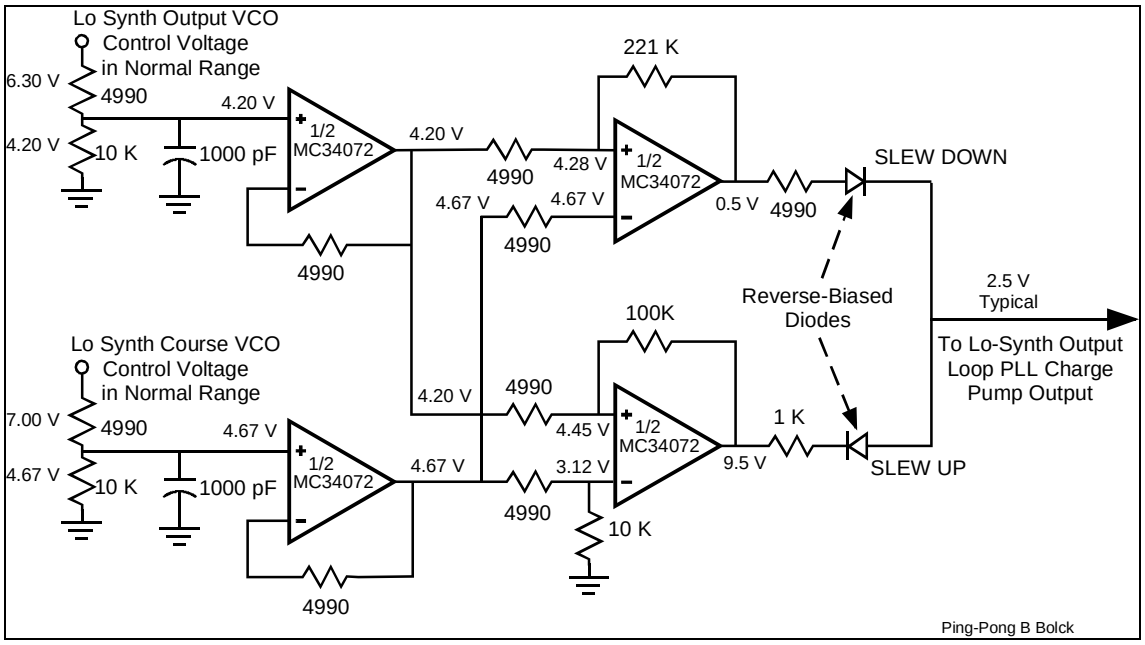


Figure 6.4.8. When Low-Synth loops are locked in normal operation, the Auto-Alignment Circuit output is disconnected from the Output PLL IC

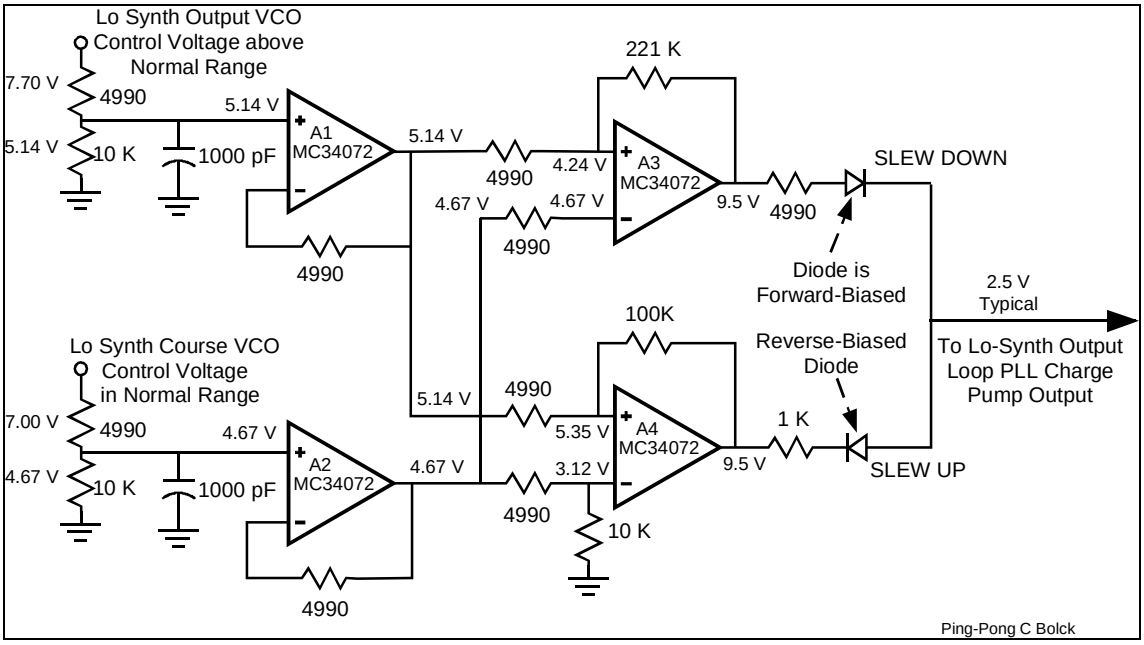


Figure 6.4.9. SLEW DOWN operation is enabled whenever the Output VCO control voltage ranges above the Coarse VCO control voltage

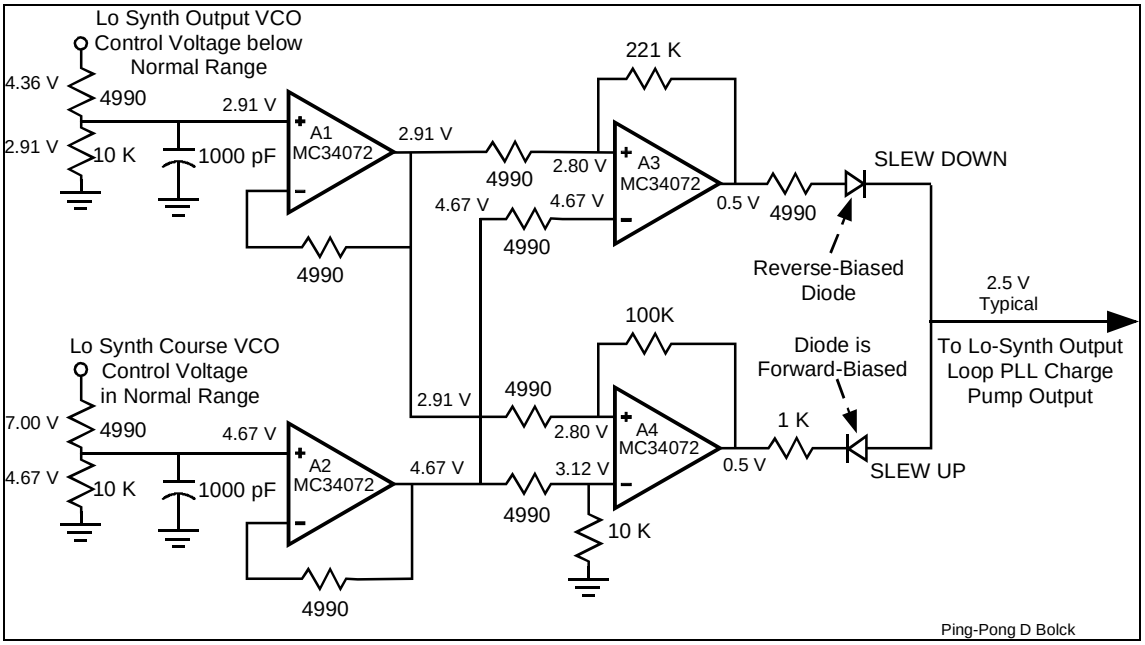


Figure 6.4.10. SLEW UP is enabled to decrease the time interval required to phase lock the Output VCO when it ranges considerably below the desired operating point

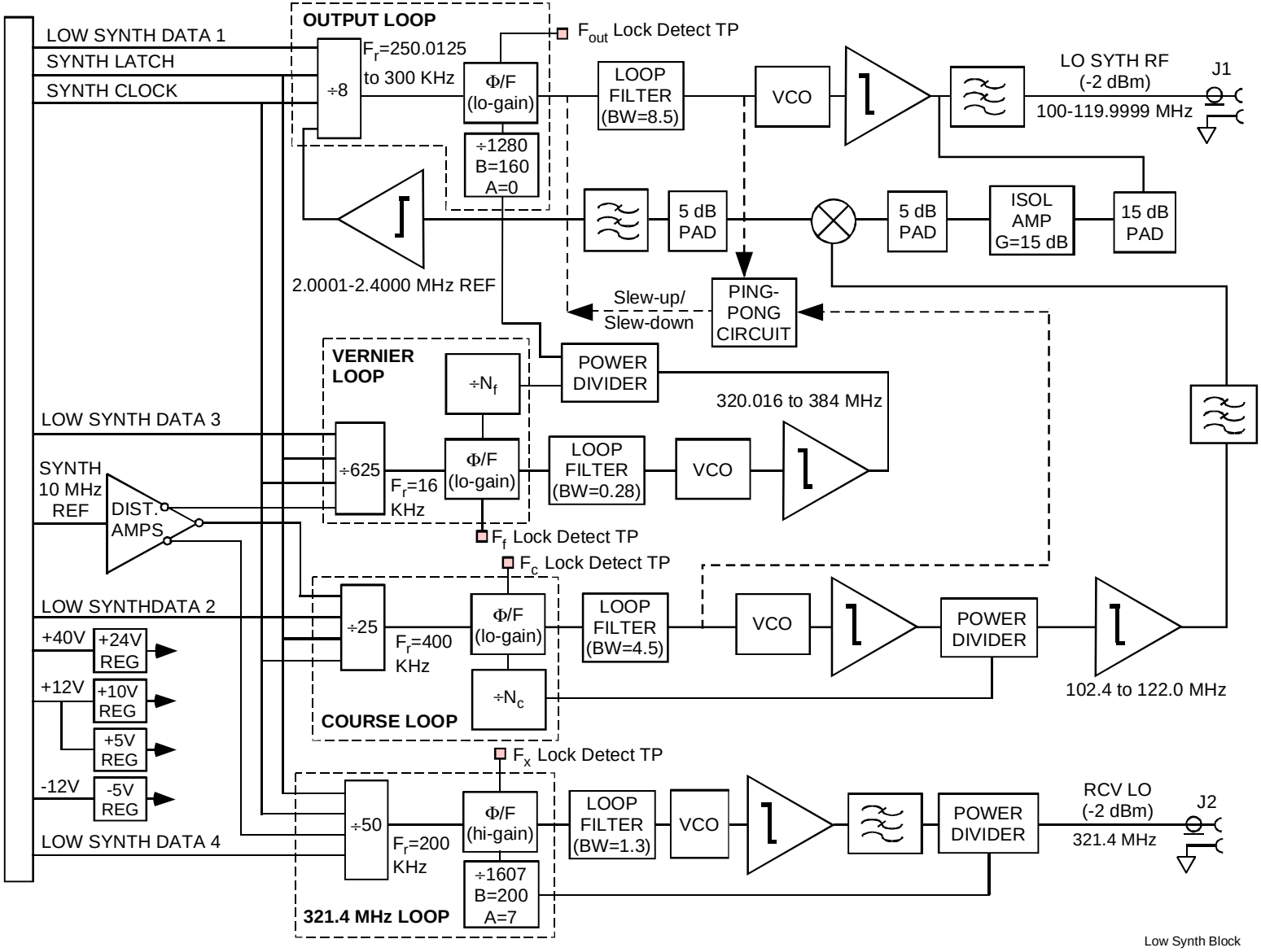
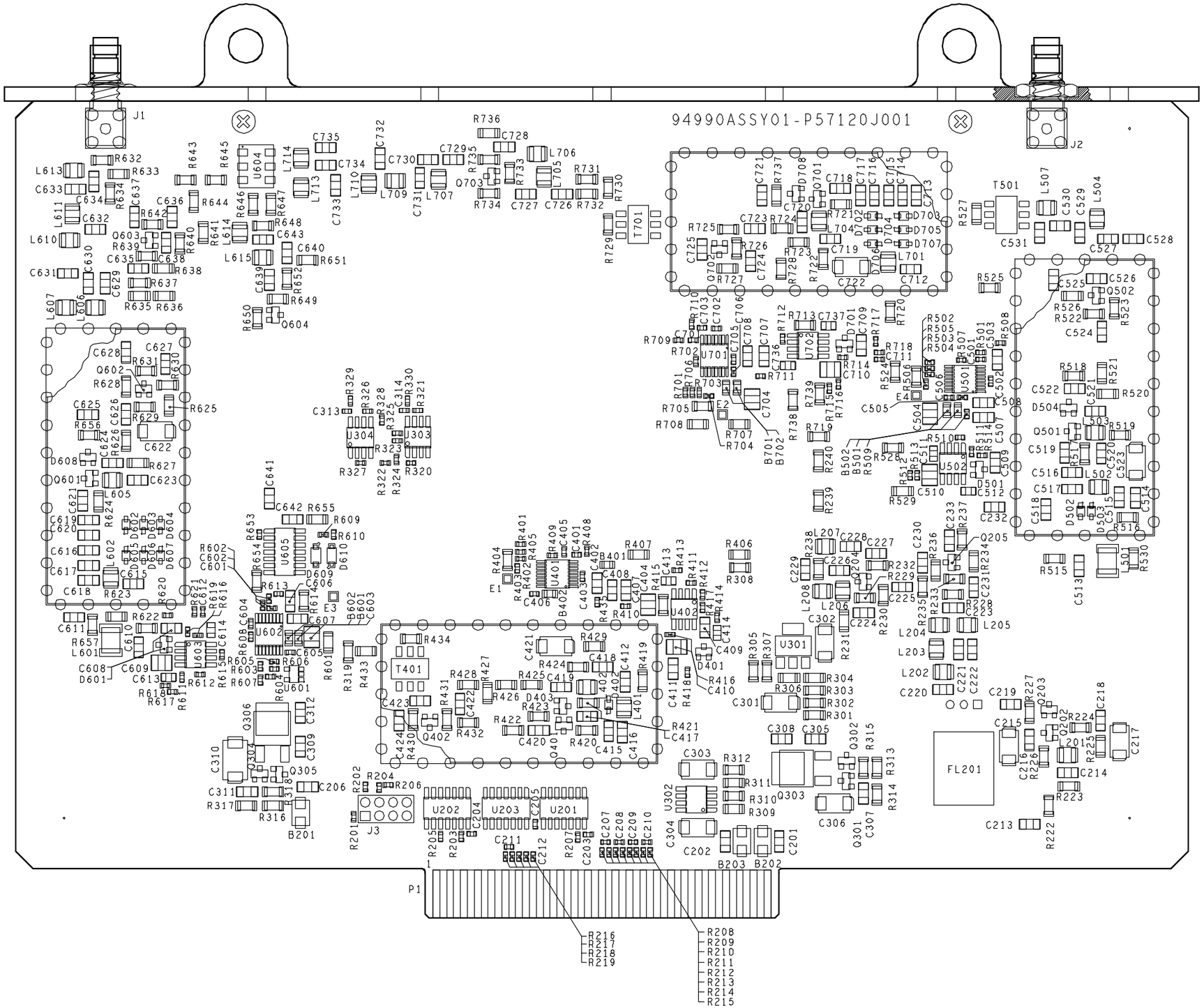


Figure 6.5 Block Diagram



CIRCUIT CARD ASSEMBLY
LOW SYNTHESIZER

01-P57120J REV. -

SHEET 1 OF 1

DWG NO 63-P57122J SH 1

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
-	INITIAL RELEASE	00-08-28	A. GATTO

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A9.

2. FOR REFERENCE DRAWINGS REFER TO:
   01-P57120J ASSEMBLY
   12-P57123J TEST PROCEDURE

3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL INDUCTANCE VALUES ARE IN NH.
   ALL CAPACITANCE VALUES ARE IN PF.

4. TERMINATIONS CODED WITH THE SAME LETTERS OR NUMBERS ARE ELECTRICALLY CONNECTED.

5. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH MANUFACTURER. ENGINEERING APPROVED EQUIVALENT DEVICE MAY BE USED.

6. TO ALLOW EACH PLL TO BE PROGRAMMED INDIVIDUALLY (I.E. FOR EXTERNAL PROGRAMMING) THE FOLLOWING RESISTOR PLACEMENT IS REQUIRED:

R402	REPLACED BY	R403
R404	REPLACED BY	R405
R503	REPLACED BY	R504
R506	REPLACED BY	R505
R604	REPLACED BY	R605
R606	REPLACED BY	R607
R703	REPLACED BY	R704
R705	REPLACED BY	R706

   NOTE: AFTER RESISTOR SUBSTITUTION, THE FUNCTIONALITY OF THE DATA AND LATCH ARE INTERCHANGED.

ALL SHEETS ARE THE SAME REVISION STATUS

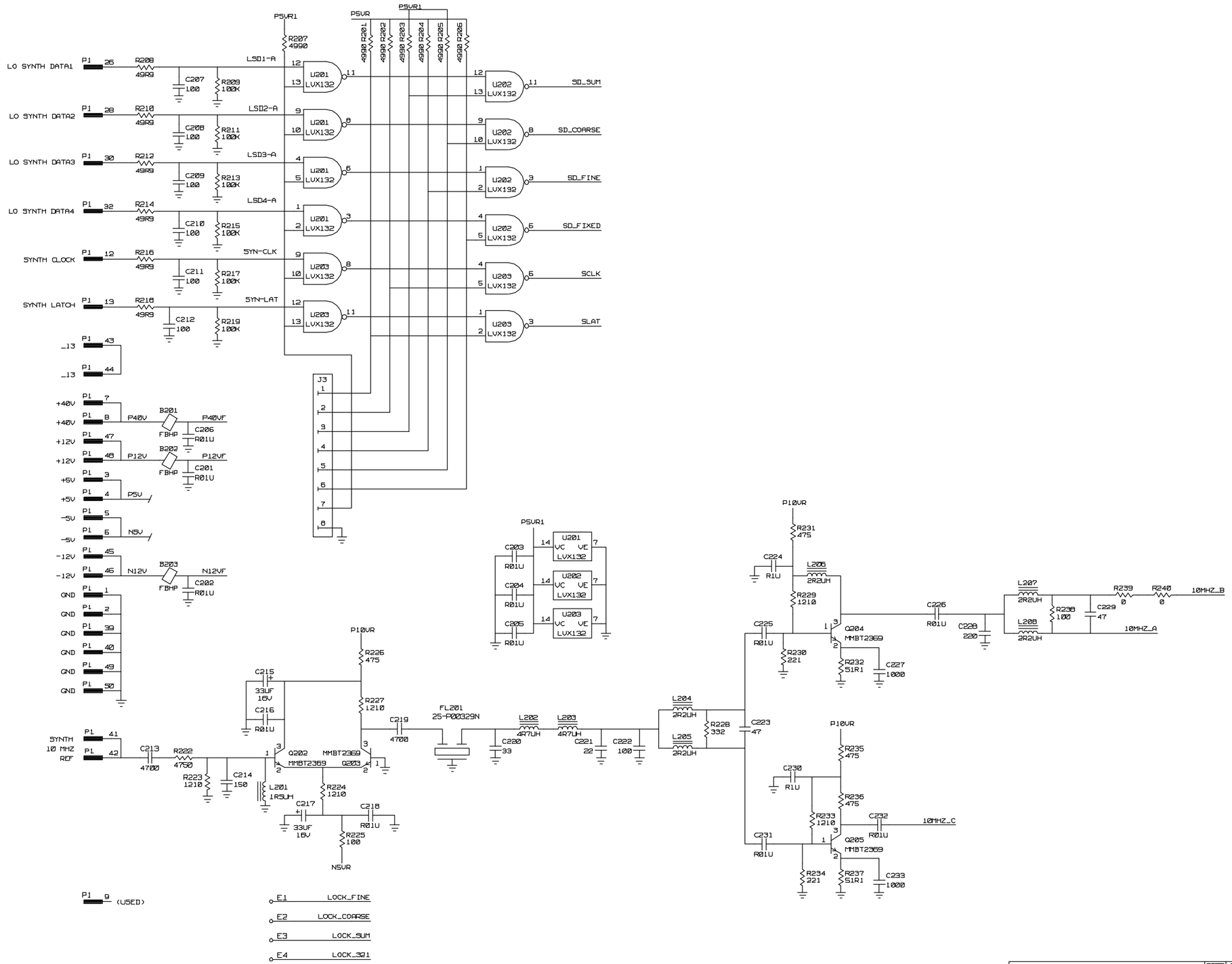
		CONTR	
		ISS	B35550-488(-)00-08-28
		APPROVALS	
		DWN	L. BARROW 00-06-22
		CHKR	
		QA	T. DAVINO 00-08-28
		MATL	J. HARNISH 00-08-25
01-P57120J	COCHISE	MFG	W. MACDONALD 00-08-26
NEXT ASSY	USED ON	ENG	A. GATTO 00-08-24
APPLICATION		CUST	

MOTOROLA INC.
GOVERNMENT AND SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

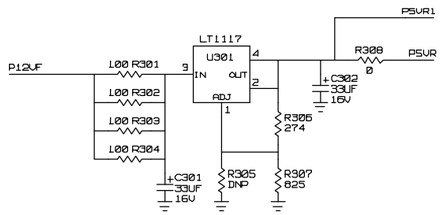
TITLE
SCHEMATIC DIAGRAM
LOW SYNTHESIZER

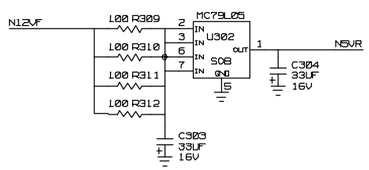
SIZE	CAGE CODE	DWG NO
D	94990	63-P57122J

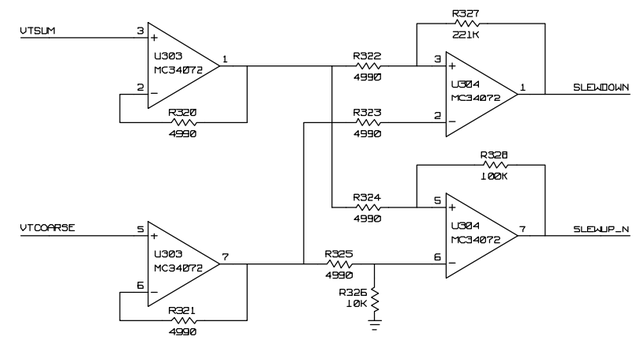
SCALE NONE SHEET 1 OF 7

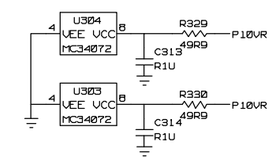


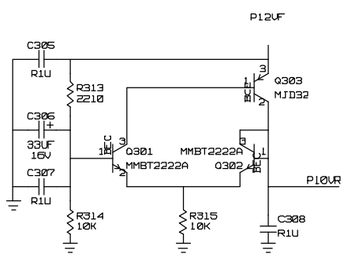
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57122J	REV -
	SCALE NONE		SHEET 2	

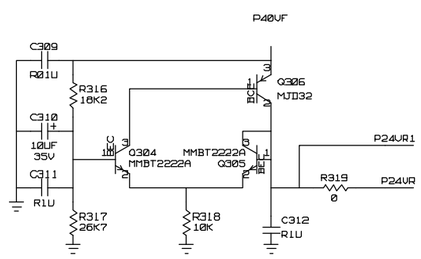






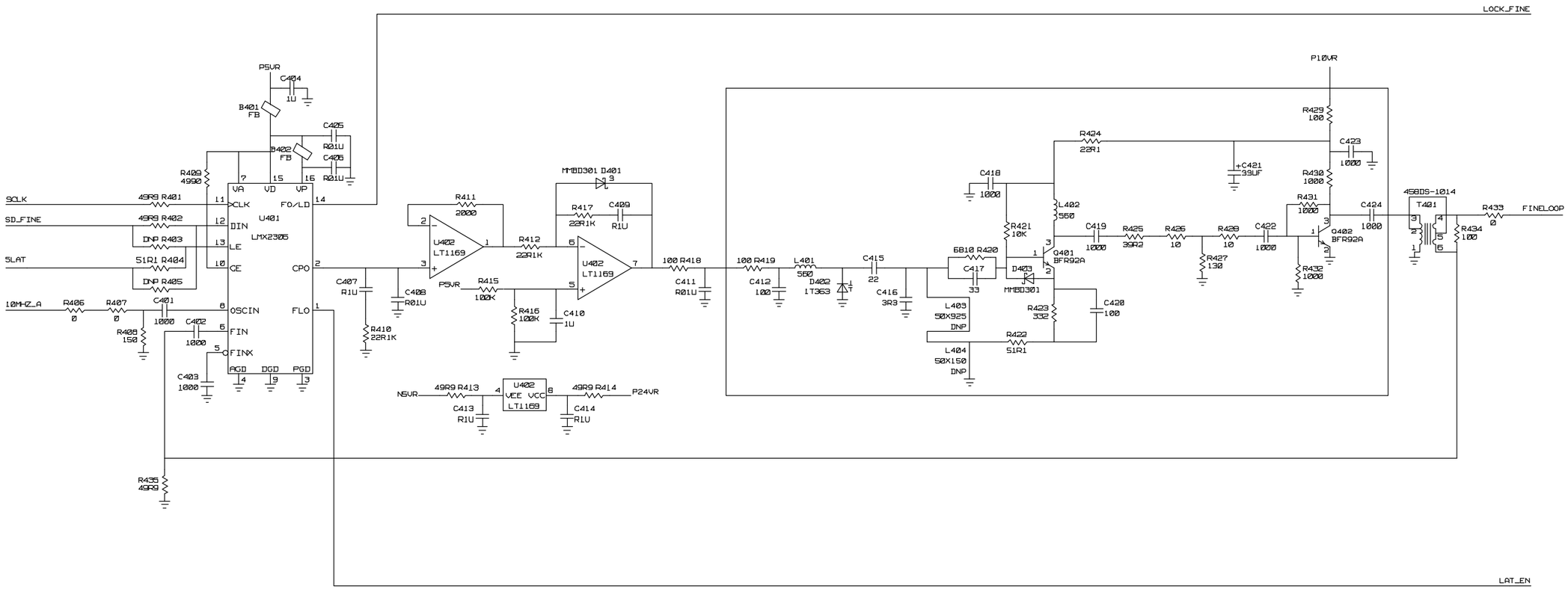






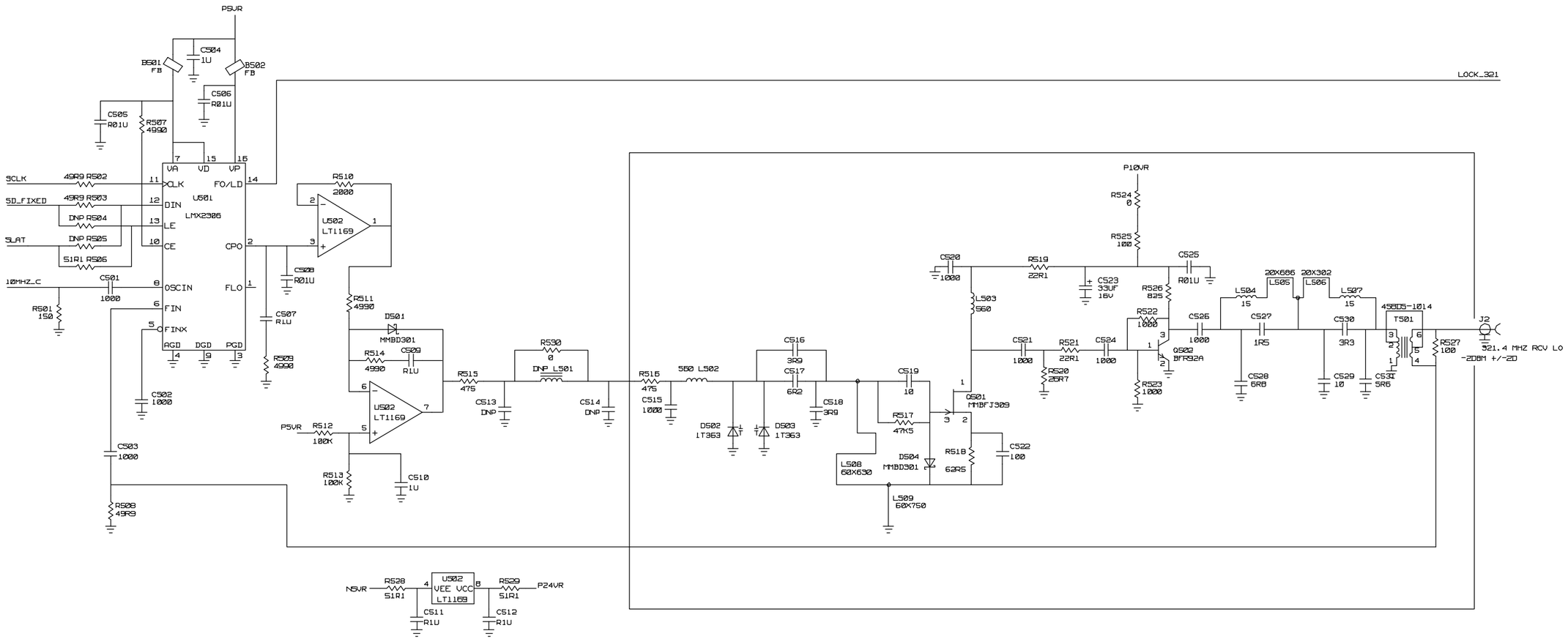
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57122J	REV –
	SCALE NONE		SHEET 3	

FINE LOOP



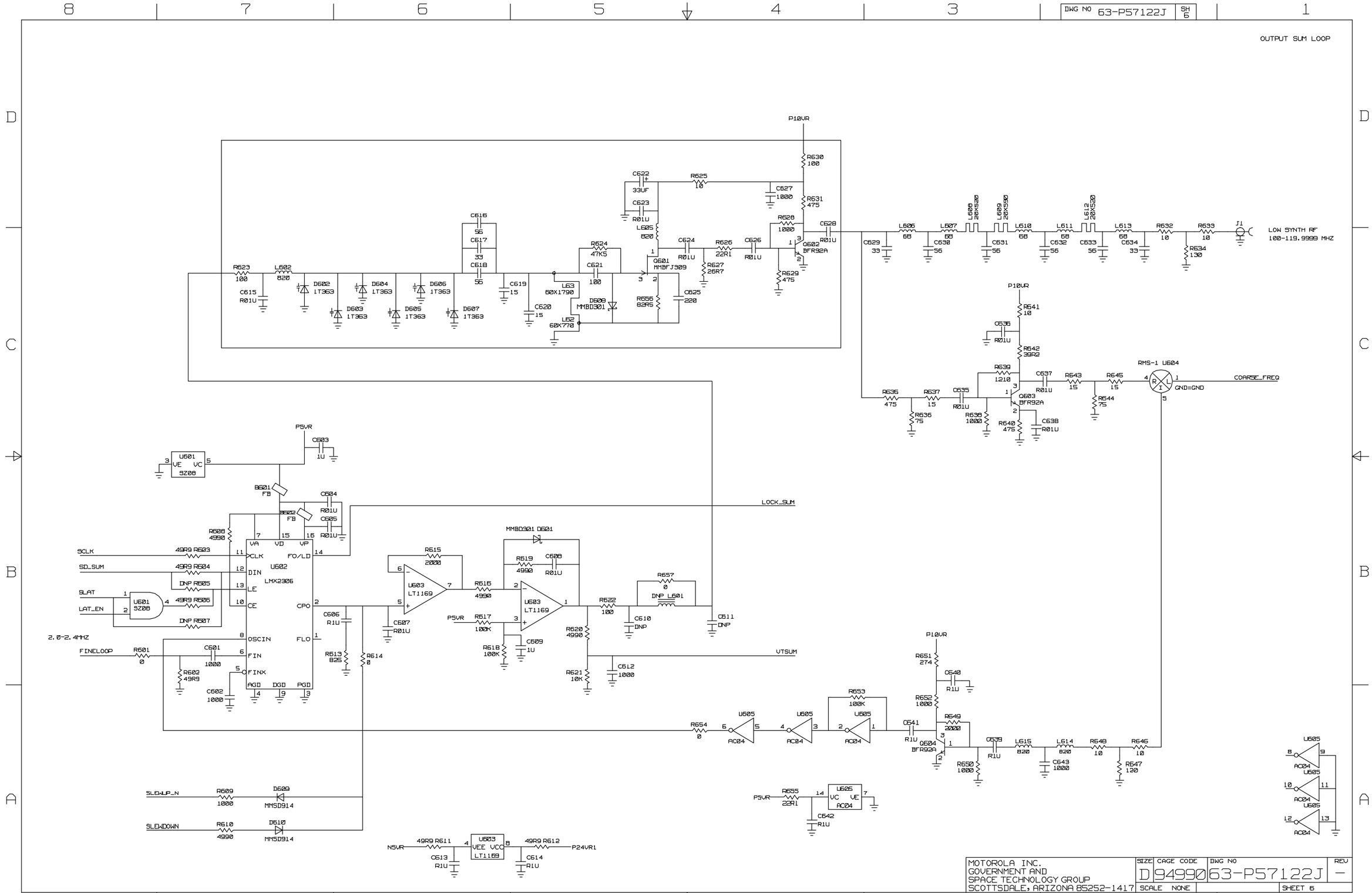
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57122J	REV –
	SCALE NONE		SHEET 4	

321.4MHZ FIXED LOOP



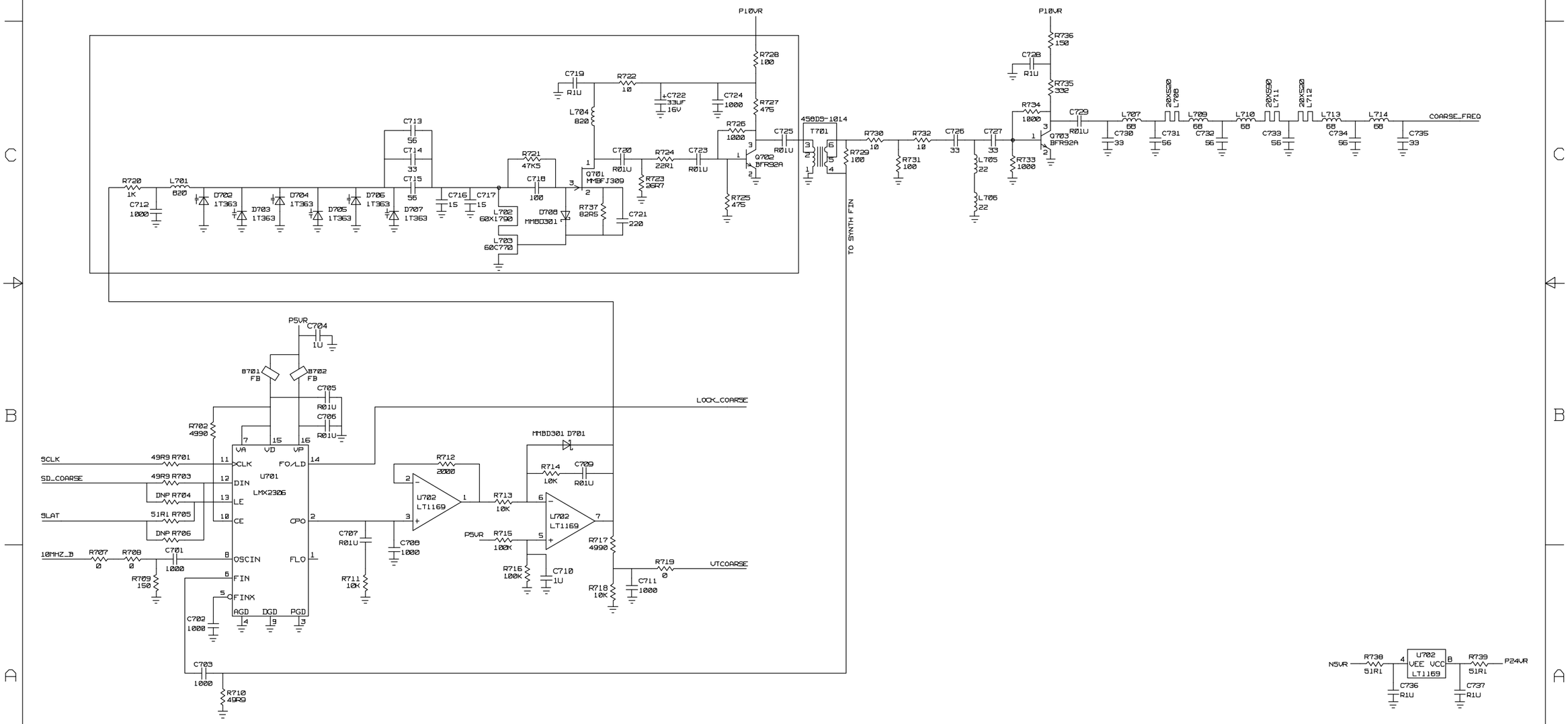
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57122J	REV -
	SCALE NONE		SHEET 5	

OUTPUT SUM LOOP



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57122J	REV -
	SCALE NONE		SHEET 6	

COARSE LOOP



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57122J	REV -
	SCALE NONE			SHEET 7

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Return to main TABLE OF CONTENTS

Return to Section 6

Go to Section 8

7.1 GENERAL DESCRIPTION

The Spectrum Analyzer Module (All) is installed in the RF cardcage in the seventh slot from the center of the Analyzer.

This module performs three major functions. The first of these is a log amp function for use in the system's spectrum analyzer mode and for signal strength readings. The second function is to provide a local oscillator for the Generator Module. Finally, the Spectrum Analyzer Module provides a digital scan lock signal used by the system processor to lock onto input signals during scan mode.

Throughout this maintenance manual the abbreviation "SA" represents the words "Spectrum Analyzer".

7.2 SIGNALS SUMMARY

7.2A Signal Descriptions

Signals appearing here are in alphabetical order and interface to/from the Interface Module unless otherwise specified.

LATCHED WRITE 0-7 These 8 inputs are used as static data lines for programming the SA CAL DAC (Spectrum Analyzer CALibration level Digital-to-Analog Converter).

SA BW1 & 2 (Spectrum Analyzer Bandwidth 1 and 2) These inputs are used to select one of two SA bandwidths: 6KHz or 30KHz.

*SA CAL LATCH** input is used to latch data into the SA Calibration Level DAC and Latch.

SA LO output to the Generator Module is used as a local oscillator in that module. In AM Generate mode the SA LO is locked to 289.3MHz. In the spectrum analyzer display mode, SA LO is swept around a center frequency of 289.3MHz.

SA *SWEEP WIDTH 1-4* inputs select the sweep width in Spectrum Analyzer and Sweep Generator modes.

SA SYNTH DATA input is used as the data line for the SA's synthesizer. It is used in conjunction with SYNTH CLOCK and SYNTH LATCH.

SA TEMP SENSE output is a 0 to +5VDC level that is proportional to the temperature of the log amp.

SCAN LOCK FREQ is the limited output of the 21.4MHz signal divided down. This signal is used for the scan lock function.

SIG STRENGTH output is a 0 to +5VDC voltage that is proportional to the strength of the signal present at the 310.7MHz SA IF input line from the RF Input Module.

SWEEP input sweeps the SA VCO during Spectrum Analyzer and Sweep Generate functions. It is a digitally stepped sawtooth waveform.

SWEEP EN (Sweep Enable) input enables/disables the sweep of Spectrum Analyzer or Sweep Generator modes.

SYNTH CLOCK input clocks SA SYNTH DATA into the synthesizer loop.

SYNTH LATCH input latches the SA SYNTH DATA previously clocked into the synthesizer loop.

SYNTH 10MHz Ref input signal from the Frequency Standard Module provides the 10MHz reference signal used by the SA LO PLL.

310.7MHz SA IF input from the RF Input Module is down-converted to create the 21.4MHz signal for this module.

+12V, -12V, +5v, and +40V from P1 supply power to this module.

7.2B Connector Descriptions

P1 (100 Pin Edge Connector to RF Motherboard)

pin	
1,2	GND
3-4	+5V
5-6	not used by this module
7,8	+40V
9	SA BW 1
10-12	not used by this module
13	SA SWEEP WIDTH 1
14	not used by this module
15	SA SWEEP WIDTH 2
16	not used by this module
17	SA SWEEP WIDTH 3
18	not used by this module
19	SA SWEEP WIDTH 4

20-22	not used by this module
23	SA CAL LATCH*
24-37	not used by this module
38	SYNTH CLOCK
39	SWEEP EN
40	SYNTH LATCH
41-48	not used by this module
49	LATCHED WRITE 0
50	not used by this module
51	LATCHED WRITE 1
52	not used by this module
53	LATCHED WRITE 2
54	not used by this module
55	LATCHED WRITE 3
56	not used by this module
57	LATCHED WRITE 4
58	not used by this module
59	LATCHED WRITE 5
60	not used by this module
61	LATCHED WRITE 6
62	not used by this module
63	LATCHED WRITE 7
64-66	not used by this module
67	SA SYNTH DATA
68-73	not used by this module
74	SCAN LOCK FREQ
75-78	not used by this module
79	SA TEMP SENSE
80,81	not used by this module
82	SWEEP
83,84	not used by this module
85	SIG STRENGTH
86-88	not used by this module
89,90	GND
91,92	SYNTH 10 MHz REF
93,94	not used by this module
95,96	-12V
97,98	+12V
99, 100	GND

SMB Connectors

J1	310.7 MHz SA IF from RF Input Module Center freq: 310.7MHz Output impedance: 50Ω nominal VSWR: 2:1 maximum
J2	SA LO to Generator Module Output freq 289.3MHz fixed (AM generate) Output freq sweep, 284.3 to 294.3MHz (spectrum analyzer display mode) Output impedance: 50Ω nominal VSWR: 2:1 maximum

7.3 BLOCK DIAGRAM DESCRIPTION

The 310.7MHz SA IF signal from the RF Input Module is mixed with a 284.3 to 294.3MHz signal from an on-board VCO for downconversion to 21.4MHz. The 21.4MHz signal is used to create the SCAN LOCK FREQ and SIG STRENGTH signals.

The output of the VCO in the PLL is used to create the SA LO signal to the generator module.

Spectrum Analyzer sweep widths are selected in a 1, 2, 5 sequence from 20KHz to 10MHz. This is accomplished by processor control of the VCO control voltage.

7.4 DETAILED DESCRIPTION

7.4.1 310.7 MHz to 21.4MHz Downconversion

A signal at the 310.7MHz input is first attenuated by a 3dB pad consisting of R1, R2, and R9. The 310.7MHz signal is down-converted at mixer U1 to 21.4MHz by a 289.3MHz VCO. The signal is then split into two paths, the Scan Lock path and the Signal Strength path.

7.4.1.1 Scan Lock Path

The Scan Lock signal is amplified by U4 and Q5 and limited by Q6. If the signal is strong enough to cause full limiting, a CMOS level capable of toggling flip-flops U19 and U25 is produced. The flip-flops divide the signal by 16. The Scan Lock signal is sent to the Interface Module and measured to determine the center frequency of the input signal.

7.4.1.2 Signal Strength Path

BANDPASS FILTER

The main signal is first amplified by Q1 and then filtered by crystal filter FL1 (center freq. of 21.4MHz with a 30KHz bandwidth). This filter strips off unwanted spurious mixer products and provides very good skirt selectivity. The output of the filter is matched to a 3dB pi attenuator consisting of R11, R21, and R27. This attenuator provides a well defined load to the filter.

455 KHz DOWN CONVERSION

The 21.4MHz filter is down-converted to 455KHz by active mixer U2. The LO for this mix is provided by a crystal oscillator internal to U2. An external 20.945MHz crystal controls the frequency of this oscillator.

SELECTABLE IF BANDWIDTHS

The output of the mixer is amplified by approximately 20dB by Q3. A bank of 2 user selectable 455KHz ceramic filters allows the user to choose either a 30KHz or 6KHz IF bandwidth.

The 30KHz path consists of a single filter while the 6KHz path consists of 2 filters. The desired filter is selected by turning on a series diode at the input (D3 or D8) and output (D1 or D7) filter path. Series diodes in the undesired filter are reverse biased. U13 performs this diode switching according to the state of the SA BW1 signal.

A variable attenuator in the 30KHz filter path is used to equalize the attenuation between the 30KHz and 6KHz filter paths. From the filter the 455KHz signal is routed to a 3dB pi attenuator consisting of R61, R65, and R38.

GAIN CONTROLLER AMP
The signal is then amplified by a gain controlled amp. The gain of this amplifier is controlled by a voltage that is programmed by D-A converter U20. The gain of this amplifier is set by the processor to calibrate the top line adjustment of the SA display.

LOG AMP
The 455KHz signal is then input to log amp U9. The log amp produces a voltage, which is proportional to the log of the input signal power. The Signal Strength voltage is filtered by an active filter built around U16. This voltage is sent to the Interface Module and displayed on the Spectrum Analyzer display screen, and is used for signal strength readings.

7.4.2 VCO Control

Resident to the Spectrum Analyzer Module is a VCO with two outputs. One is used in the 310.7MHz to 21.4MHz downconversion and the other (SA LO) is a local oscillator used by the Generator Module. Built around the VCO is a PLL. The input voltage to the VCO is a summer with 2 inputs. The first input is a sweep voltage used to linearly sweep the VCO around 289.3MHz. The second input is a sample and hold circuit that stores the voltage from the PLL loop filter. The loop filter outputs the voltage necessary to hold the VCO at 289.3MHz or swept when used in spectrum analyzer modes.

7.4.2.1 Sweep

The sweep voltage is a -8 V to +8 V ramp voltage consisting of a 256 bit staircase produced by a D-A converter on the Interface Module. This voltage is first filtered by an active 1.6KHz lowpass filter at U17. This voltage is then scaled to a programmable attenuator under processor control via the SA Sweep Width 1-4 signals.

The attenuator provides sweep widths in a 1, 2, 5 sequence. Dispersions ranging from 20KHz to 10MHz are available. The attenuator consists of a series of precision voltage dividers. The desired divider ratio is selected by turning on the appropriate line on U22, a 1 to 8 line demultiplexer. If a full sweep is selected, the voltage dividers are bypassed by analog switch U18, allowing the sweep voltage to go unattenuated. The sweep voltage is then buffered by a noninverting unity gain amplifier, U15.

Before each sweep of the VCO, the sweep input is set to zero, and the PLL is locked to 289.3MHz. The exact tuning voltage is then sampled and held. This ensures that the center frequency of the sweep is exact. The loop is then unlocked and the VCO is swept around 289.3MHz. The loop is then locked, and the process is repeated.

7.4.2.2 PLL

The PLL consists of a phase/frequency detector, U5, and an active loop filter using U10. The VCO includes JFET Q17 for the oscillator and Q8 for the buffer amp. Varactor D10 controls the oscillator frequency.

7.4.2.3 Sample and Hold

The sample and hold circuit consists of the holding cap C109, and analog switch U18, and op-amp U14. In the sample mode (when the PLL is locked), the analog switch U18 is closed and C109 is charged by the loop filter to the voltage required to maintain lock. In hold mode, when the loop is being swept, U18 is opened, but C109 holds the center frequency voltage. This voltage is summed with the sweep voltage at U15. A current source using Q9 and R103 acts to add +8V to offset the summer. This results in a nominal tuning voltage of +8V when locked. This offset also causes the nominal voltage on the sample and hold capacitor to be near 0 volts, improving its hold time.

7.5 BLOCK DIAGRAM

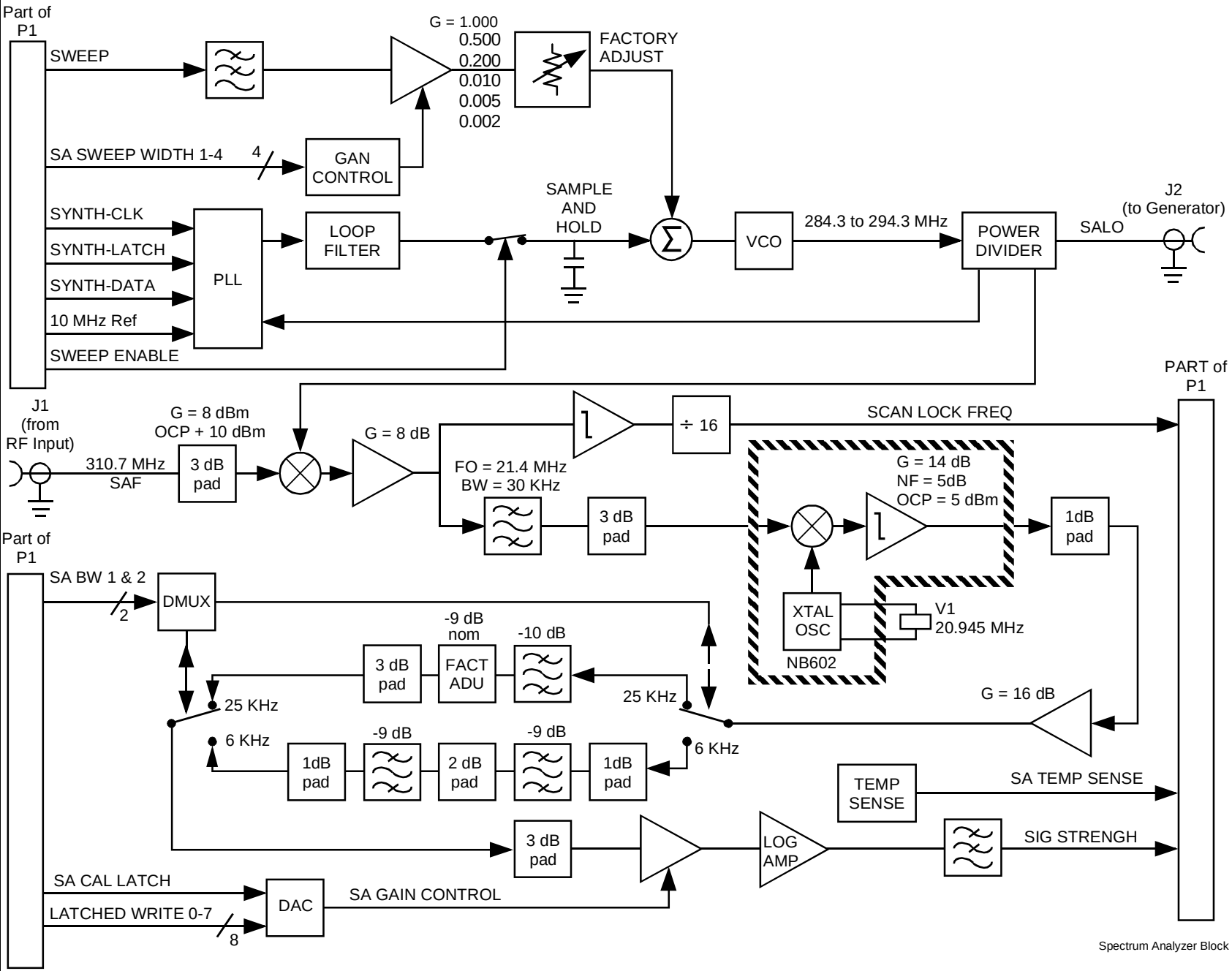
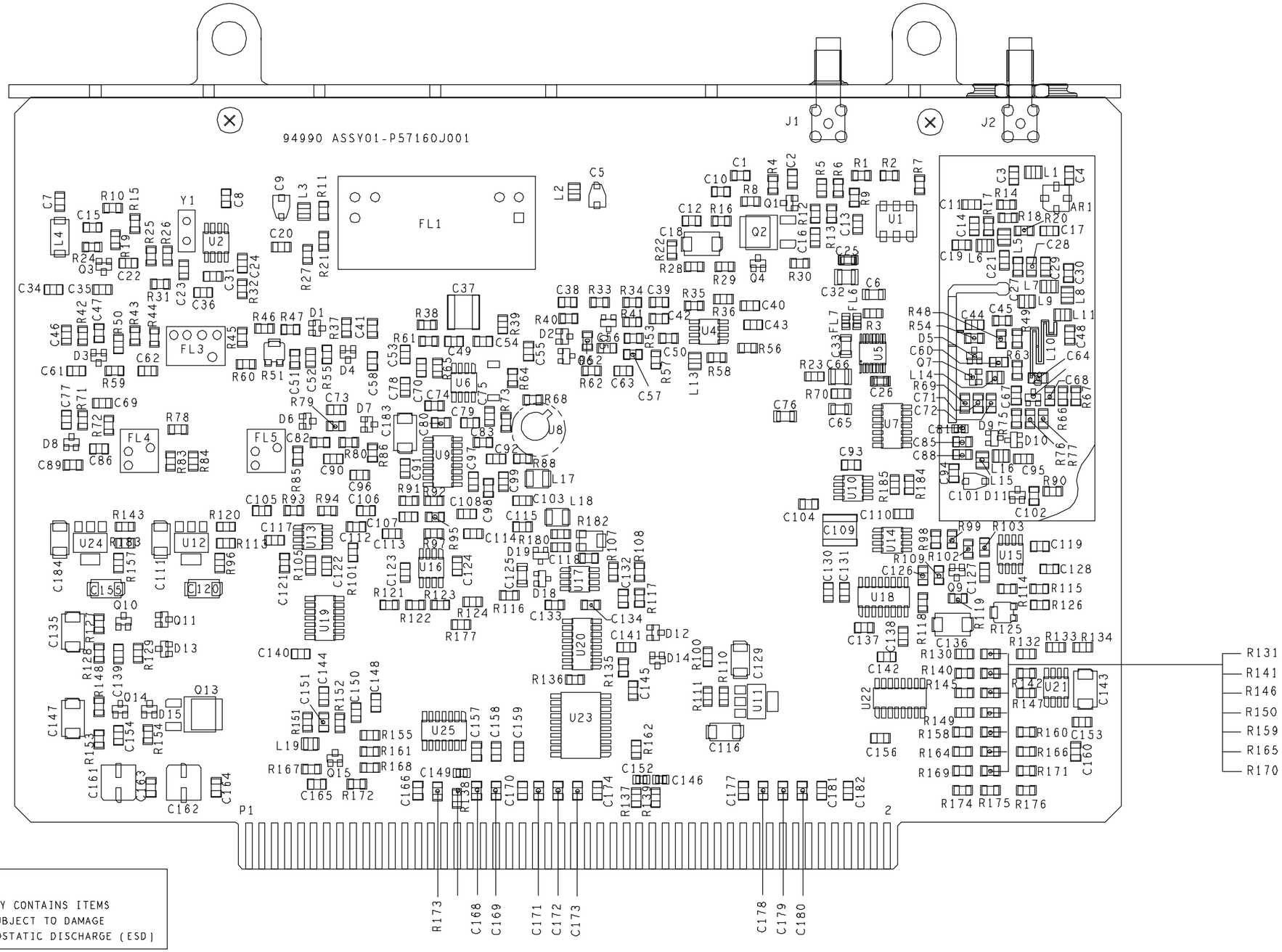


Fig. 7.5 Spectrum Analyzer Block Diagram



CAUTION
THIS ASSEMBLY CONTAINS ITEMS
WHICH ARE SUBJECT TO DAMAGE
FROM ELECTROSTATIC DISCHARGE (ESD)

CIRCUIT CARD ASSEMBLY
SPECTRUM ANALYZER

01-P57160J REV. XA

SHEET 1 OF 1

DWG NO 63-P57162J SH 1

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
XA	ENGINEERING CONTROL	4-28-00	N BROWN

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A11.

2. FOR REFERENCE DRAWINGS REFER TO:
   01-P51760J ASSEMBLY
   12-P57163J TEST PROCEDURE

3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS.
   ALL VOLTAGES ARE IN DC.

4. TERMINATIONS CODED WITH THE SAME LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.

5. CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE 1.

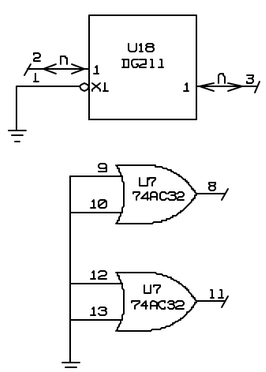
6. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH MANUFACTURER. SEE ASSEMBLY PARTS LIST FOR PROPER PART NUMBER.

REFERENCE DESIGNATIONS	
HIGHEST NUMBER USED	NOT USED
AR1	
C183	C59
D17	
FL7	
J2	
L19	L12
P1	
Q15	
R185	
U25	
Y1	

TABLE 1 (5)

REF DES	DEVICE TYPE (6)	CONN	VOLTS	GND CONNECTIONS	PAGE FOUND ON
U1	RM5-1			2,3,6	4
U2	NE602			3	5
U3	504PF	2	+5VREG	5	8
U4	MC1350			3,7	4
U5	LMX2306	5	+5VREG	8	8
U6	MC1350			3,7	6
U7	74AC32	14	+5VREG	7	1,8
U8	LM335				3
U9	NE6040	4	+6V	2,13	6
U10	MC34072	8	+10VREG		7,8
		4	-10V		
U11	LT1117				3
U12	LT1117				3
U13	MC34072	8	+10VREG		5
		4	-10V		
U14	TL072		+10VREG		8
			-10V		
U15	MC34081	7	+15V		8
		4	-10V		
U16	MC34072	8	+10VREG		6
		4	-10V		
U17	MC34072	8	+10VREG		6,7
		4	-10V		
U18	DG211	13	+10VREG		1,7,8
		12	+5VREG		
		4	-10V	5	
U19	74AC74	14	+5VREG	7	4
U20	DAC-08	1	+10VREG		6
		7	-10V		
U21	LM317				3
U22	DG508	13	+10VREG		7
		3	-10V	14	
U23	74ACT374	20	+5VREG	10	6
U24	LT1117				3
U25	74AC74	14	+5VREG		4

SPARES



ALL SHEETS ARE THE SAME REVISION STATUS

		CONTR
		ISS
		APPROVALS
		DWN P. MURPHY 00-04-06
		CHKR
		QA
		MATL
01-P57160J	COCHISE	MFG
NEXT ASSY	USED ON	ENG
APPLICATION		CUST

MOTOROLA INC.
GOVERNMENT AND SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

TITLE
SPECTRUM ANALYZER
SCHEMATIC DIAGRAM

SIZE	CAGE CODE	DWG NO
D	94990	63-P57162J
SCALE NONE		SHEET 1 OF 9

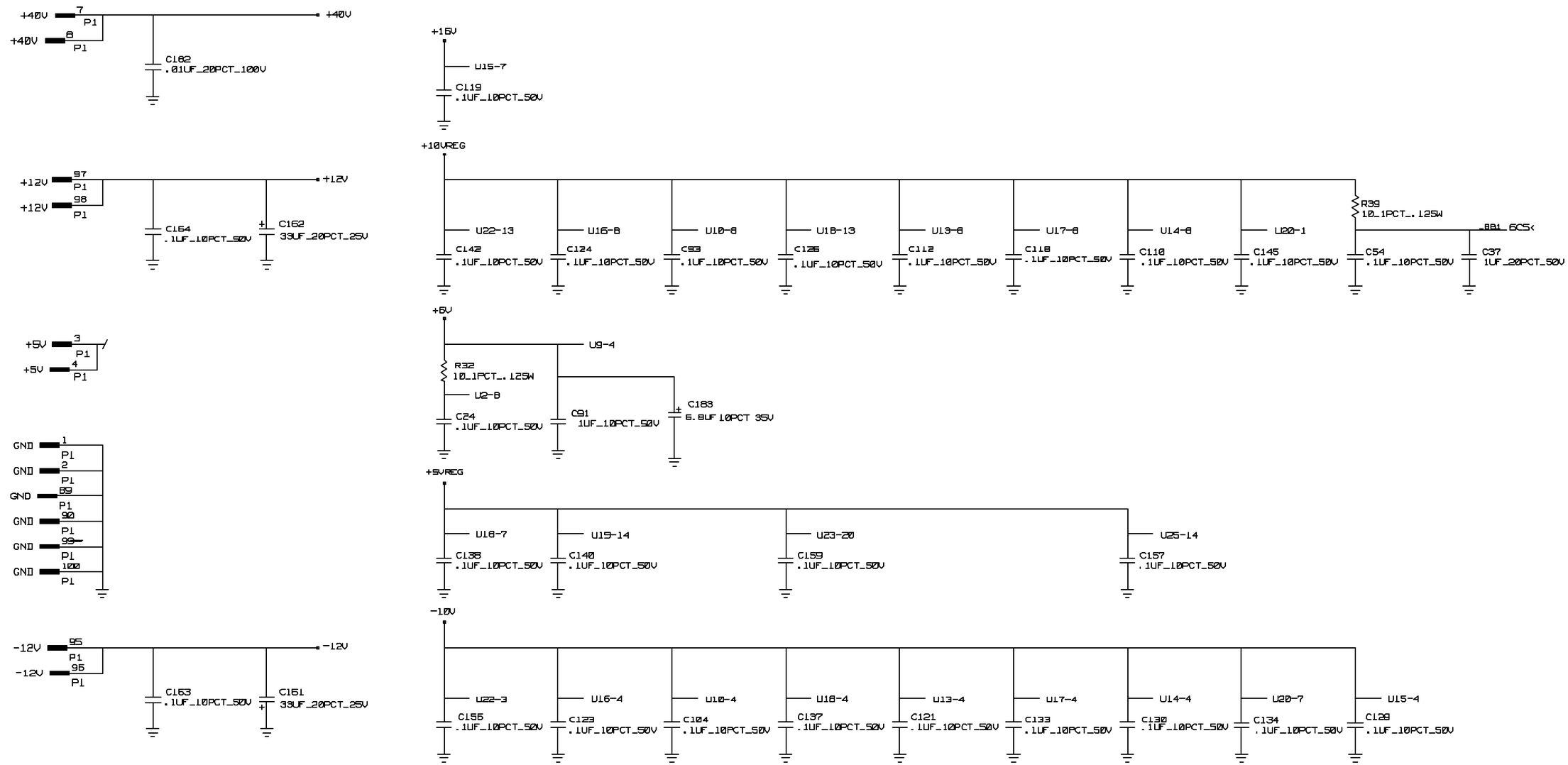
ASME Y14.1-1993 DRAWING FORMAT - 3/08

DRAWING
63P57162J_XA
63P57162J
LAST MODIFIED WEDNESDAY

CONCEPT

DATCOPACK1-HDCD

*11103-22-1 C



MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

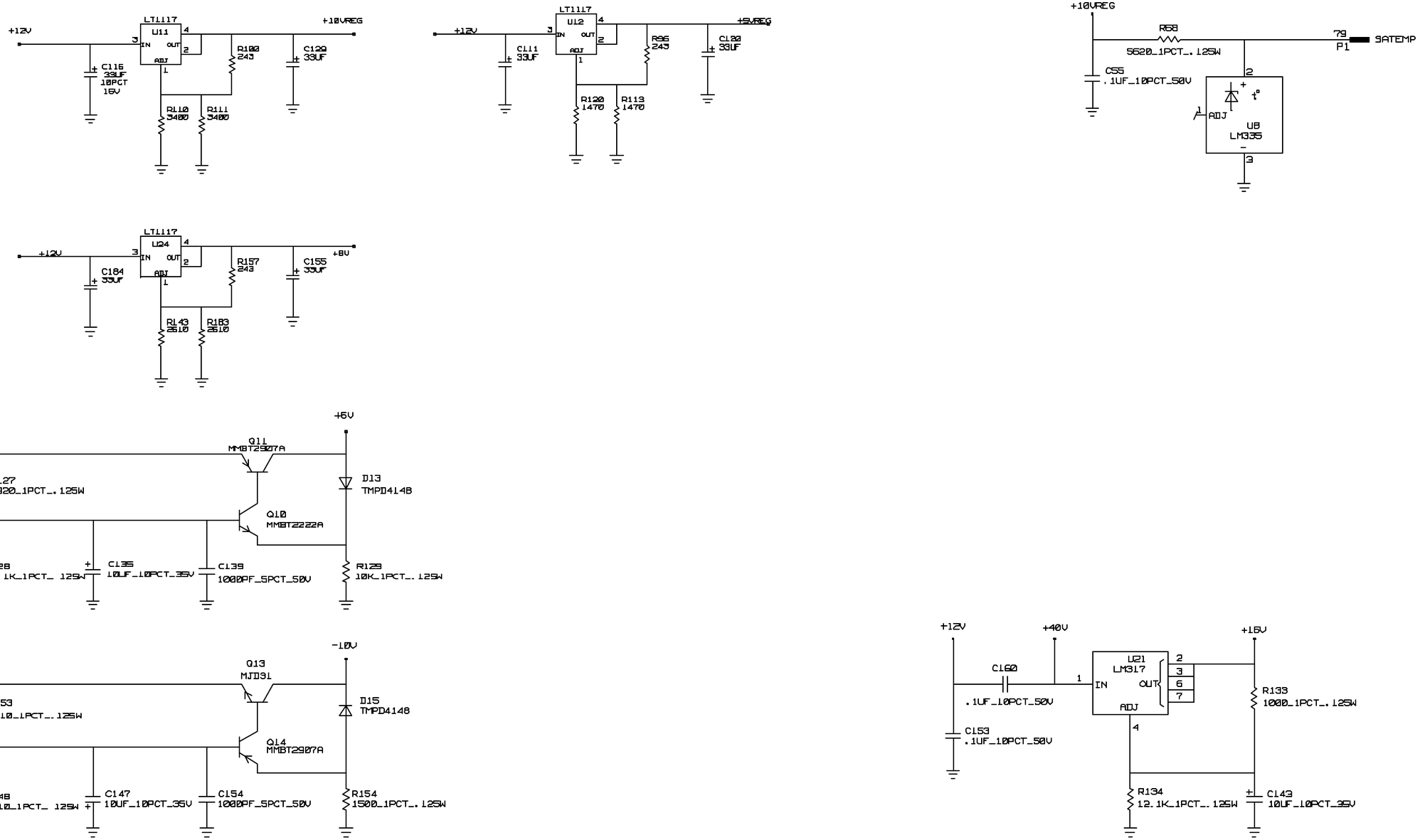
SIZE	CAGE CODE	DWG NO	REV
D	94990	63-P57162J	XA
SCALE NONE		SHEET 2	

DRAWING
63P57162J_XA
63P57162J
LAST MODIFIED: Fri Apr 28 12:13:08 2000

CONCEPT

ASME Y14.1-1995 DRAWING FORMAT - 2/95

*1102-22-1 C



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE	CAGE CODE	DWG NO	REV
	D	94990	63-P57162J	XA
	SCALE NONE		SHEET 3	

ASME Y14.1-1995 DRAWING FORMAT - 3/05

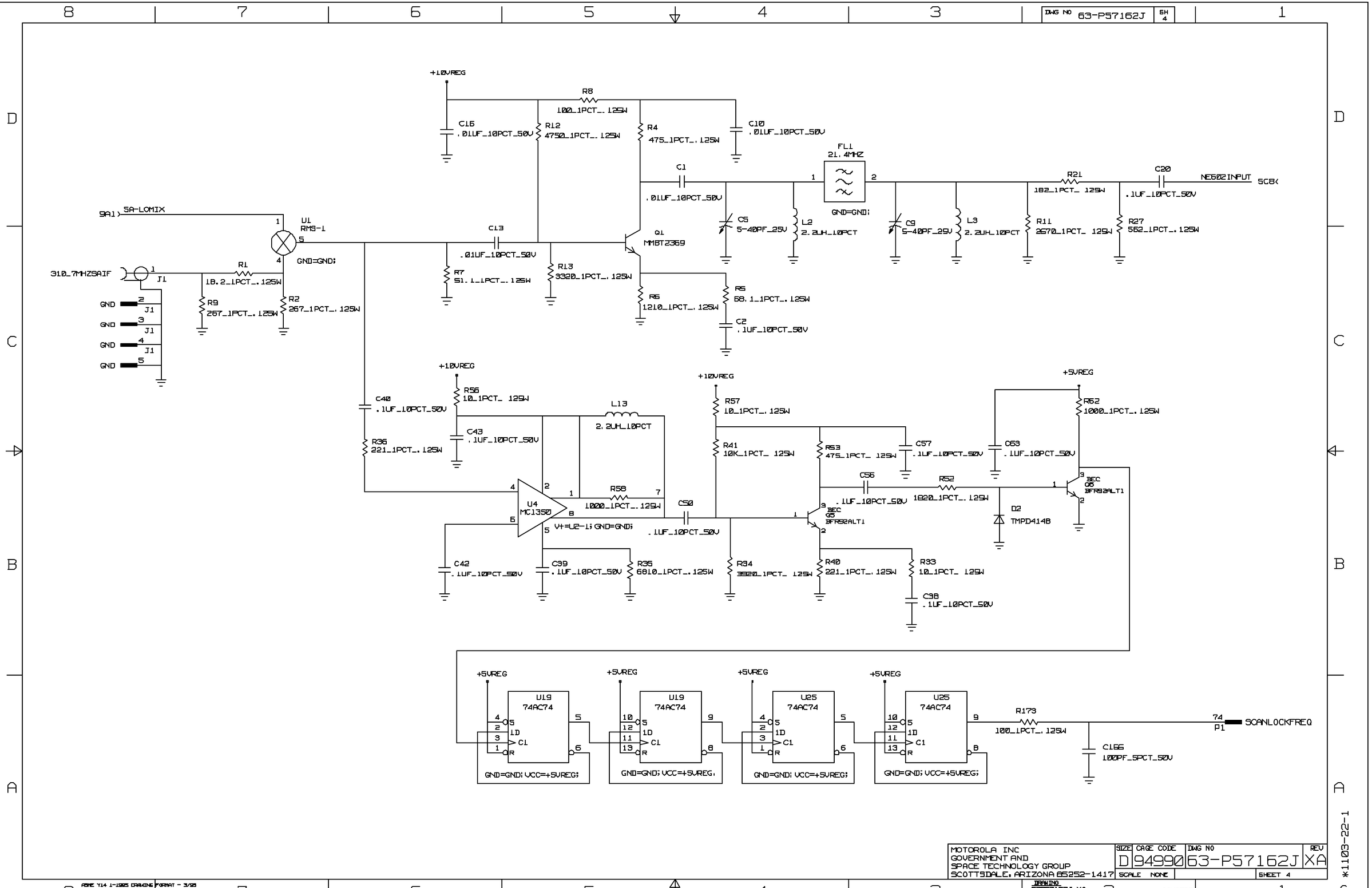
DRAWING 63P57162J_XA 63P57162J

LAST MODIFICATION: Apr 28 12:13:28 2000

CONCEPT

DATZGRAPHIC

*1103-22-1



MOTOROLA INC GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE	CAGE CODE	DWG NO	REV
	D	94990	63-P57162J	XA
	SCALE NONE			SHEET 4

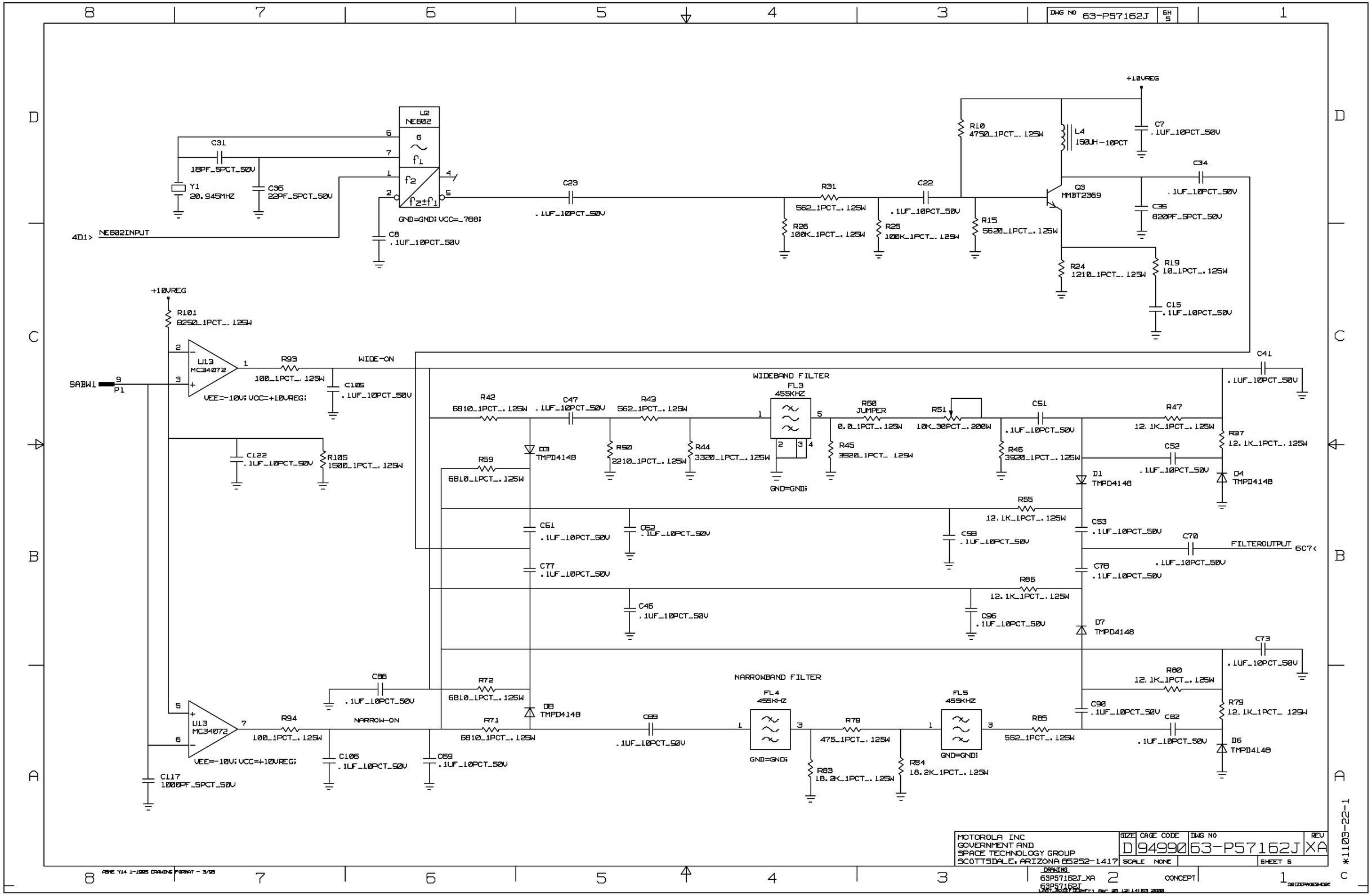
DRAWING 63P57162J_XA 63P57162J

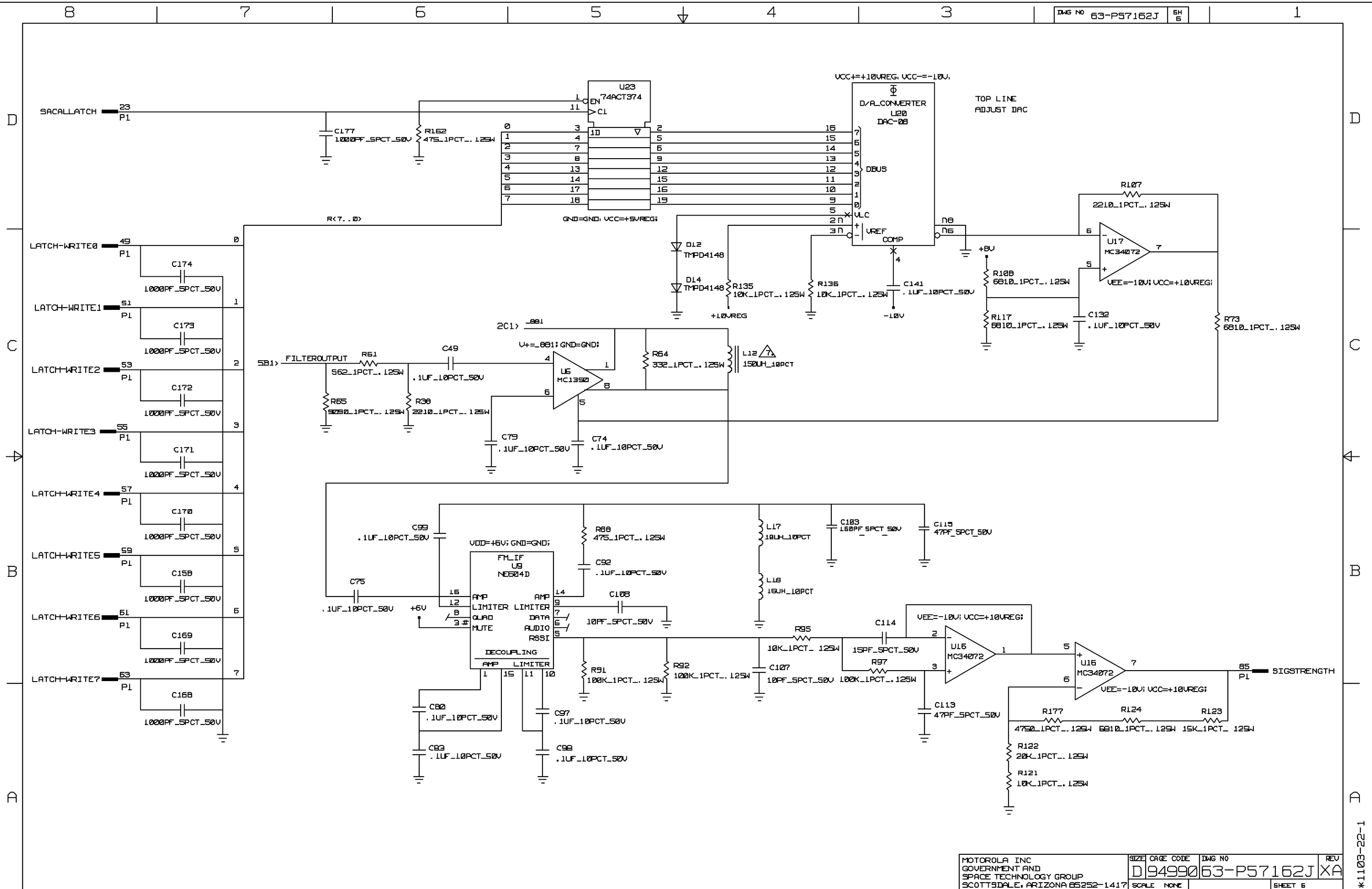
LAST MODIFIED: Fri Apr 20 12:13:45 2001

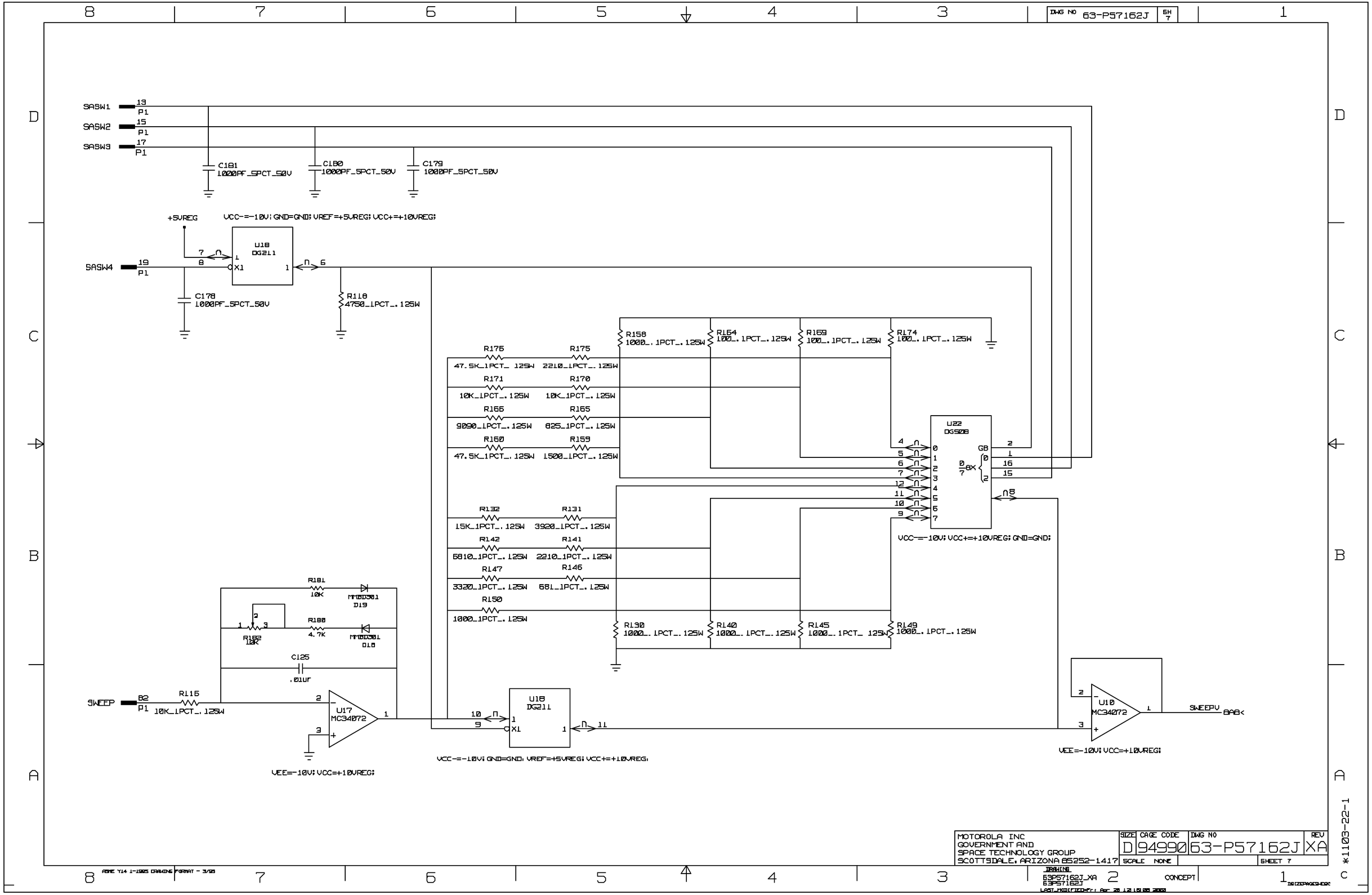
CONCEPT

ASME Y14.1-1995 DRAWING FORMAT - 3/95

*1103-22-1


DWG NO 63-P57162J SH 5
U2 NE602
C31 18PF_5PCT_50V
Y1 20.945MHZ
C36 22PF_5PCT_50V
C8 .1UF_10PCT_50V
GND=GND; VCC=_788;
4D1> NE602INPUT
C29 .1UF_10PCT_50V
R31 562_1PCT_.125W
R26 100K_1PCT_.125W
C22 .1UF_10PCT_50V
R25 100K_1PCT_.125W
R10 4750_1PCT_.125W
R15 5620_1PCT_.125W
L4 150UH-10PCT
C7 .1UF_10PCT_50V
Q3 MMBT2369
C34 .1UF_10PCT_50V
C35 820PF_5PCT_50V
R24 1210_1PCT_.125W
R19 10_1PCT_.125W
C15 .1UF_10PCT_50V
+10VREG
R101 8250_1PCT_.125W
U13 MC34072
VEE=-10V; VCC=+10VREG;
SABW1 P1
R93 100_1PCT_.125W
WIDE-ON
C105 .1UF_10PCT_50V
C122 .1UF_10PCT_50V
R105 1500_1PCT_.125W
WIDEBAND FILTER
FL3 455KHZ
R42 5810_1PCT_.125W
C47 .1UF_10PCT_50V
R43 562_1PCT_.125W
D3 TMPD4148
R50 2210_1PCT_.125W
R44 3320_1PCT_.125W
R60 JUMPER 0.0_1PCT_.125W
R51 10K_30PCT_.200W
R45 3320_1PCT_.125W
C51 .1UF_10PCT_50V
R46 3920_1PCT_.125W
R47 12.1K_1PCT_.125W
R37 12.1K_1PCT_.125W
C52 .1UF_10PCT_50V
D1 TMPD4148
D4 TMPD4148
C41 .1UF_10PCT_50V
R59 6810_1PCT_.125W
R55 12.1K_1PCT_.125W
C61 .1UF_10PCT_50V
C62 .1UF_10PCT_50V
C58 .1UF_10PCT_50V
C53 .1UF_10PCT_50V
C70 .1UF_10PCT_50V
FILTEROUTPUT 6C7<
C77 .1UF_10PCT_50V
C78 .1UF_10PCT_50V
R85 12.1K_1PCT_.125W
C45 .1UF_10PCT_50V
C96 .1UF_10PCT_50V
D7 TMPD4148
C73 .1UF_10PCT_50V
R80 12.1K_1PCT_.125W
C86 .1UF_10PCT_50V
R72 6810_1PCT_.125W
NARROWBAND FILTER
FL4 455KHZ
FL5 455KHZ
D8 TMPD4148
C90 .1UF_10PCT_50V
R79 12.1K_1PCT_.125W
R94 100_1PCT_.125W
NARROW-ON
R71 6810_1PCT_.125W
C99 .1UF_10PCT_50V
R78 475_1PCT_.125W
R65 562_1PCT_.125W
C82 .1UF_10PCT_50V
D6 TMPD4148
C106 .1UF_10PCT_50V
C69 .1UF_10PCT_50V
R83 18.2K_1PCT_.125W
R84 18.2K_1PCT_.125W
C117 1000PF_5PCT_50V
GND=GND;
MOTOROLA INC
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D CAGE CODE 94990 DWG NO 63-P57162J REV XA
SCALE NONE SHEET 5
DRAWING 63P57162J_XA 63P57162T
CONCEPT
ASME Y14.1-1995 DRAWING FORMAT - 3/95


DWG NO 63-P57162J SH 6
SACALLATCH
U23 74ACT374
C177 1000PF_5PCT_50V
R162 475_1PCT_.125W
R<7..0>
GND=GND; VCC=+5VREG;
VCC+=+10VREG; VCC-=-10V;
D/A_CONVERTER U20 DAC-08
DBUS
VLC
VREF
COMP
TOP LINE ADJUST DAC
D12 TMPD4148
D14 TMPD4148
R135 10K_1PCT_.125W
R136 10K_1PCT_.125W
C141 .1UF_10PCT_50V
+10VREG
-10V
R107 2210_1PCT_.125W
U17 MC34072
VEE=-10V; VCC=+10VREG;
R108 6810_1PCT_.125W
R117 6810_1PCT_.125W
C132 .1UF_10PCT_50V
R73 6810_1PCT_.125W
LATCH-WRITE0
LATCH-WRITE1
LATCH-WRITE2
LATCH-WRITE3
LATCH-WRITE4
LATCH-WRITE5
LATCH-WRITE6
LATCH-WRITE7
C174 1000PF_5PCT_50V
C173 1000PF_5PCT_50V
C172 1000PF_5PCT_50V
C171 1000PF_5PCT_50V
C170 1000PF_5PCT_50V
C158 1000PF_5PCT_50V
C169 1000PF_5PCT_50V
C168 1000PF_5PCT_50V
FILTEROUTPUT
R61 562_1PCT_.125W
C49 .1UF_10PCT_50V
R65 9090_1PCT_.125W
R38 2210_1PCT_.125W
V+=_881; GND=GND;
U6 MC1350
R64 332_1PCT_.125W
L12 150UH_10PCT
C79 .1UF_10PCT_50V
C74 .1UF_10PCT_50V
C99 .1UF_10PCT_50V
VDD=+5V; GND=GND;
FM_IF U9 NE604D
AMP LIMITER QUAD MUTE
AMP LIMITER DATA AUDIO RSSI
DECOUPLING
AMP LIMITER
C75 .1UF_10PCT_50V
+5V
R88 475_1PCT_.125W
C92 .1UF_10PCT_50V
C108 10PF_5PCT_50V
L17 10UH_10PCT
L18 15UH_10PCT
C103 150PF_5PCT_50V
C115 47PF_5PCT_50V
R91 100K_1PCT_.125W
R92 100K_1PCT_.125W
C107 10PF_5PCT_50V
R95 10K_1PCT_.125W
C114 15PF_5PCT_50V
R97 100K_1PCT_.125W
C113 47PF_5PCT_50V
U16 MC34072
VEE=-10V; VCC=+10VREG;
R177 4750_1PCT_.125W
R124 6810_1PCT_.125W
R123 15K_1PCT_.125W
R122 20K_1PCT_.125W
R121 10K_1PCT_.125W
SIGSTRENGTH
C80 .1UF_10PCT_50V
C83 .1UF_10PCT_50V
C97 .1UF_10PCT_50V
C98 .1UF_10PCT_50V
MOTOROLA INC
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D CAGE CODE 94990 DWG NO 63-P57162J REV XA
SCALE NONE SHEET 6
DRAWING 63P57162J_XA 63P57162J
CONCEPT
ASME Y14 1-1985 DRAWING FORMAT - 3/35
*1103-22-1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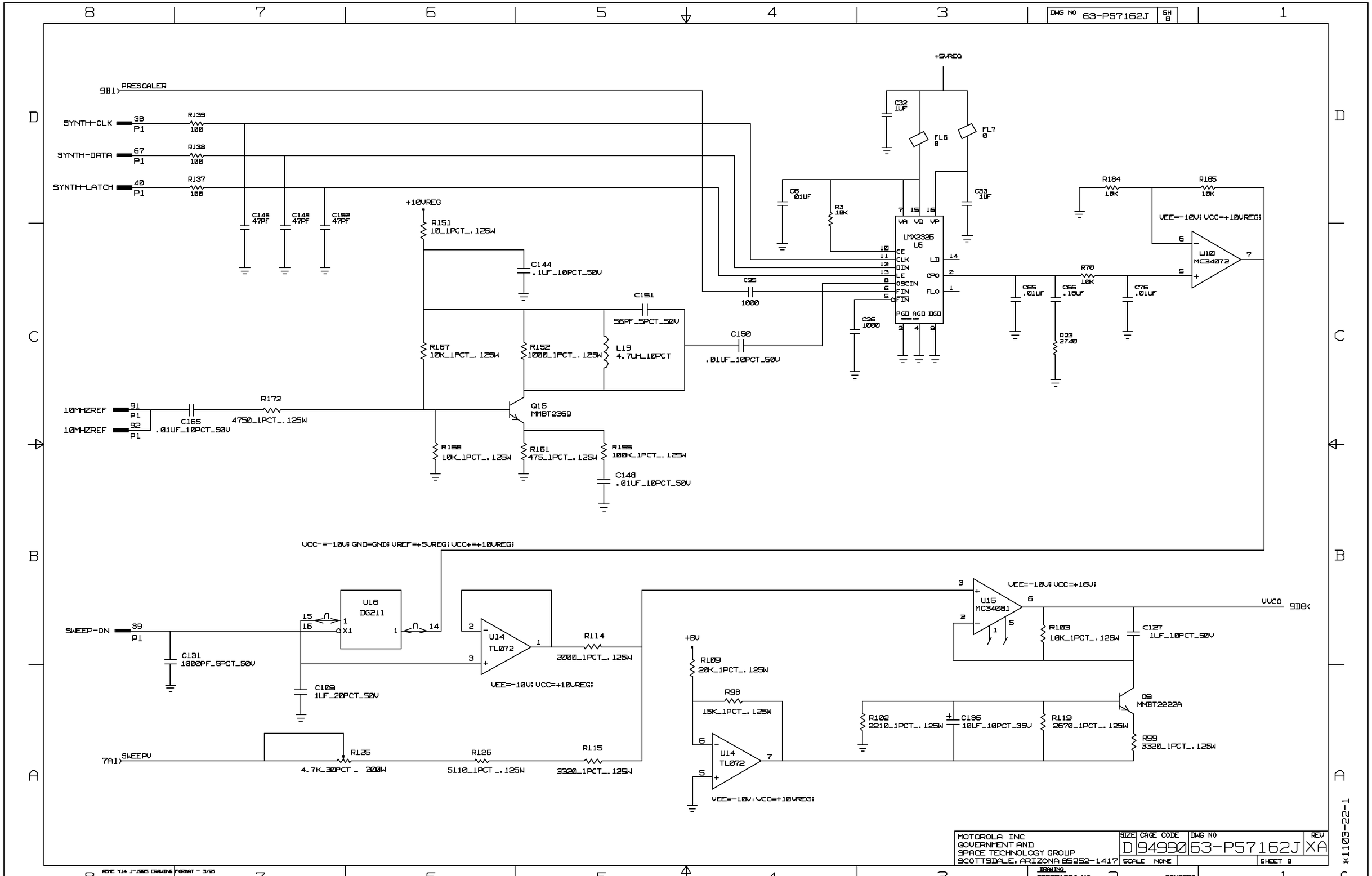
SH 7
SASW1
SASW2
SASW3
SASW4
SWEEP
SWEEPV
C181 1000PF_5PCT_50V
C180 1000PF_5PCT_50V
C179 1000PF_5PCT_50V
C178 1000PF_5PCT_50V
+5VREG
VCC-=-10V; GND=GND; VREF=+5VREG; VCC+=+10VREG;
U18 DG211
R118 4750_1PCT_.125W
R115 10K_1PCT_.125W
U17 MC34072
VEE=-10V; VCC=+10VREG;
R181 10K
R182 10K
R180 4.7K
MMBD301 D19
MMBD301 D18
C125 .01UF
R158 1000_.1PCT_.125W
R154 100_.1PCT_.125W
R169 100_.1PCT_.125W
R174 100_.1PCT_.125W
R176 47.5K_1PCT_.125W
R175 2210_1PCT_.125W
R171 10K_1PCT_.125W
R170 10K_1PCT_.125W
R166 9090_1PCT_.125W
R165 825_1PCT_.125W
R160 47.5K_1PCT_.125W
R159 1500_1PCT_.125W
R132 15K_1PCT_.125W
R131 3920_1PCT_.125W
R142 6810_1PCT_.125W
R141 2210_1PCT_.125W
R147 3320_1PCT_.125W
R146 681_1PCT_.125W
R150 1000_1PCT_.125W
R130 1000_.1PCT_.125W
R140 1000_.1PCT_.125W
R145 1000_.1PCT_.125W
R149 1000_.1PCT_.125W
U22 DG508
VCC-=-10V; VCC+=+10VREG; GND=GND;
U10 MC34072
VEE=-10V; VCC=+10VREG;
MOTOROLA INC
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D
CAGE CODE 94990
DWG NO 63-P57162J
REV XA
SCALE NONE
SHEET 7
CONCEPT
ASME Y14.1-1985 DRAWING FORMAT - 3/95
*1103-22-1


DWG NO 63-P57162J SH 8
PRESCALER
SYNTH-CLK 38 P1 R139 100
SYNTH-DATA 67 P1 R138 100
SYNTH-LATCH 40 P1 R137 100
C146 47PF
C149 47PF
C152 47PF
+10VREG
R151 10_1PCT_.125W
C144 .1UF_10PCT_50V
C151 56PF_5PCT_50V
R167 10K_1PCT_.125W
R152 1000_1PCT_.125W
L19 4.7UH_10PCT
C150 .01UF_10PCT_50V
10MHZREF 91 P1
10MHZREF 92 P1
C165 .01UF_10PCT_50V
R172 4750_1PCT_.125W
Q15 MMBT2369
R158 10K_1PCT_.125W
R161 475_1PCT_.125W
R155 100K_1PCT_.125W
C148 .01UF_10PCT_50V
+5VREG
C32 1UF
FL6 0
FL7 0
C6 .01UF
R3 10K
C33 1UF
C25 1000
C26 1000
LMX2325 U5
VA VD VP
CE CLK DIN LE OSCIN FIN RFIN
LD GPO FLO
PGD AGD DGD
R184 10K
R185 10K
VEE=-10V;VCC=+10VREG;
U10 MC34072
R70 10K
C65 .01UF
C66 .10UF
C76 .01UF
R23 2740
VCC-=-10V;GND=GND;VREF=+5VREG;VCC+=+10VREG;
SWEEP-ON 39 P1
U18 DG211
C131 1000PF_5PCT_50V
C109 1UF_20PCT_50V
U14 TL072
R114 2000_1PCT_.125W
VEE=-10V;VCC=+10VREG;
+8V
R109 20K_1PCT_.125W
R98 15K_1PCT_.125W
U14 TL072
VEE=-10V;VCC=+10VREG;
SWEEPV
R125 4.7K_30PCT_.200W
R126 5110_1PCT_.125W
R115 3320_1PCT_.125W
U15 MC34081
VEE=-10V;VCC=+16V;
VVCO
R103 10K_1PCT_.125W
C127 1UF_10PCT_50V
Q9 MMBT2222A
R102 2210_1PCT_.125W
C136 10UF_10PCT_35V
R119 2670_1PCT_.125W
R99 3320_1PCT_.125W
MOTOROLA INC
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D CAGE CODE 94990 DWG NO 63-P57162J REV XA
SCALE NONE SHEET 8
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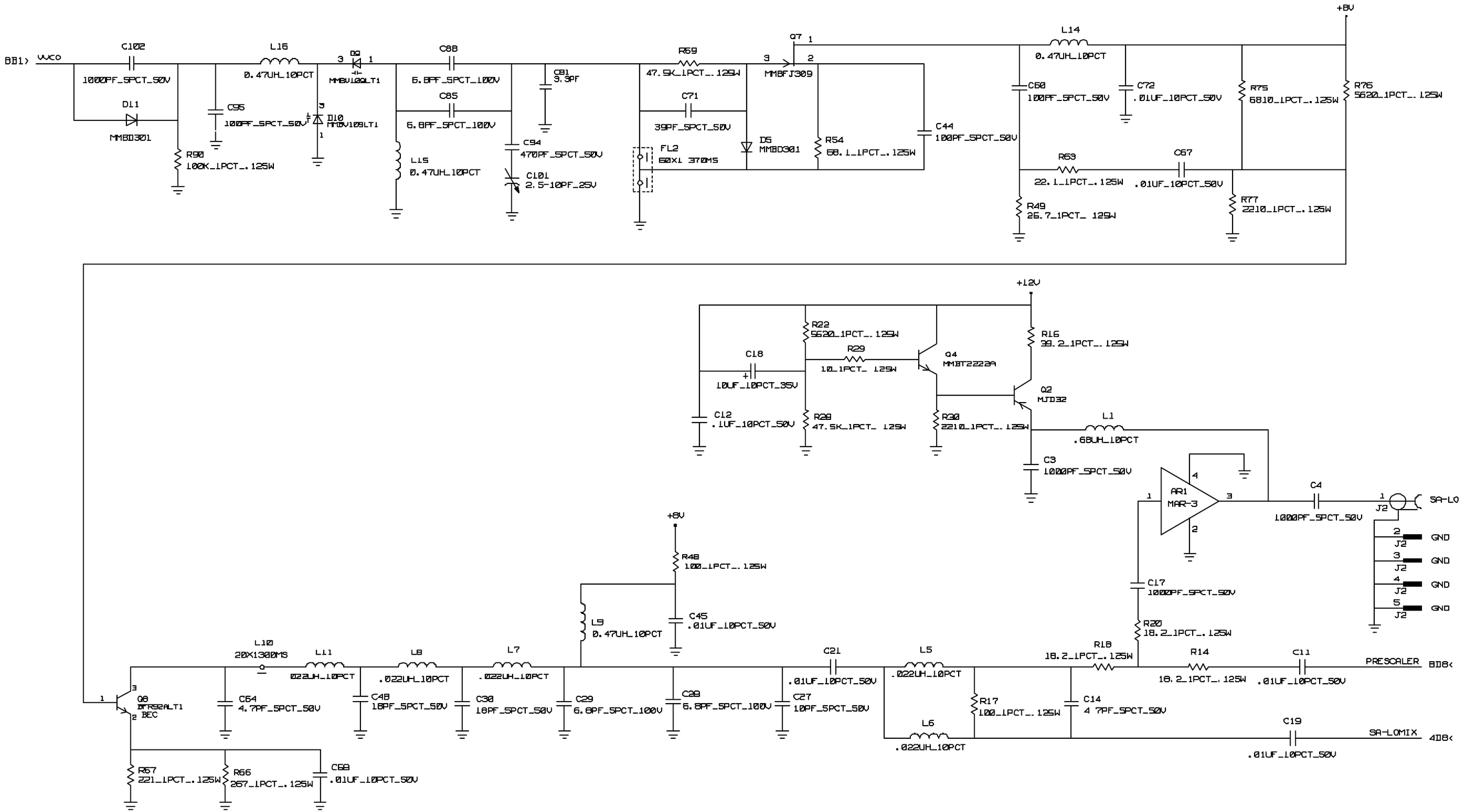
CONCEPT
ASME Y14.1-1995 DRAWING FORMAT - 3/95
*1103-22-1



MOTOROLA INC GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57162J	REV XA
	SCALE NONE			SHEET 9

DRAWING 63P57162J_XA 63P57162J 2 CONCEPT

LAST MODIFIED: Fri Apr 28 12:10:43 2000

ASME Y14 1-1985 DRAWING FORMAT - 3/95

*1103-22-1 C

MOTOR
SPACE AND SYSTEMS
TECHNOLOGY GROUP

10-20-00

SIZE SHEETS

ASSOC LIST:
DOC:

	RESP. ENGINEER
SIGNATURES	
DATE	
PHONE/AREA	

FILE
MFG. ENG.
MATL.
QA
TEST

FG. X5
TEGRA
S/M
S/C
MFG. PLNR.
FROM REPRO :
PDO DIST :
PRINTS DIST :

PRODUCT DEFINITION ORDER

CONTRACT NO.

REFER TO SPP-17 SERIES FOR FORM INSTRUCTIONS

EQUIPMENT P.I.A. NO.(S)	P.I.A.PROGRAM TITLE
10744	COCHISE

DOCUMENTATION CHARGE NO. 10744-1100

	A	DISTRIBUTE PRINT WITH RN
	B	INCORP IMMED AFTER MCO DIST
	C	DIST CHANGED PRINT WITH MCO
	D	ACCUMULATE CHANGE-DISTR MCO
X	E	DISTRIBUTE VA

RETURN DOC ORIG TO DC
RETURN PDO ORIG TO DC

DISTRIBUTION CODE	REPRODUCTION QTY C	P	A	D	F
1103-04	15				

CHANGE CLASSIFICATION

	NOT APPLICABLE
	CLASS I
X	CLASS II

GOVT APPVL OF CLASS N/A DATE

CUST APPROVAL OF CLASS N/A DATE

INTERCHANGEABILITY STATUS

	NOT APPLICABLE
X	TWO-WAY
	NON

APPROVAL REQUIRED

CUST		YES	X	NO
GOVT		YES	X	NO
PRG MGR		YES	X	NO
PRG MGR		YES	X	NO

PROJECT INCORP CHECK REQUIRED BY TONY GATTO EXT 1-6924

REMARKS:

Carolyn Galligan 441-1824

DOCUMENT OR PART NO. 01-P57160J001 CLASSIFIED DOC

PRESENT REVISION	NEW REVISION
XA	~

ASSOCIATED LIST PL WL

TITLE CIRCUIT CARD ASSEMBLY SPECTRUM ANALYZER

NEXT HIGHER ASSY PART NO(S) 01-P30203C001, 01-P57060J001

APPVL	ORIGINAL	REVISION R1	REVISION R2
ORIG	A. GATTO		
DATE	10/13/00		
EXT NO	1-6924		
R&D	A. Gatto		
DATE	10/13/2000		
MFG	J. Hamel		
DATE	10-13-2000		
MATL	W. McDonald		
DATE	10-13-00		
QA	T. Davis		
DATE	10/17/00		
TEST	B. Watts		
DATE	10-16-00		
CDM	C. Bailey		
DATE	10-17-00		

MASTER CHANGE ORDER	MCO		DASH
CHANGE ORDER	CO		-
RELEASE NOTICE	RN		-
VARIATION AUTHORITY	VA	X	B35551 -198
STOP ORDER	SO		-
INFORMATION MEMO	IM		-

BASIC NO. REV

THERE ARE ✓ RELATED DASH NUMBERS TO BASIC NO
THIS CHANGE CANCELS VA ' OR SO NO.

SOFTWARE IMPACTS

OPERATIONAL SOFTWARE	YES		NO	X
TEST SOFTWARE	YES		NO	X

HARDWARE EFFECTIVITY

TYPE	FIRM		PLANNED	X	RECORD
LEVEL	END ITEM		SUB-ASSY	X	PART
CONT NO	01-P57160J001				
C.I. NO.					
S/N					
LOT					
DATE					
REWORK	NO	X	YES		SEE BELOW X
RETROFIT					

MAT'L DISPOSITION/MFG. EFFECTS

NONE

EFFECTIVE IMMEDIATELY ON REV -XA
PRINTED WIRING BOARDS

REASON FOR ORDER:

COMPLETES THE DESIGN MODIFICATIONS REQUIRED FOR PROPER PERFORMANCE OF NEW S/A ASSEMBLY. THE SUM OF COMPONENT VALUE CHANGES IN MCO L48748 AND MODIFICATIONS IN THIS VA HAVE THE FOLLOWING EFFECTS:

1. STABILIZE THE LOOP FILTER FOR NEW SYNTHESIZER IC.
2. COMPENSATION OF THE VARACTOR TUNED 289.3 MHZ VCO CIRCUIT BECAUSE OF PWB LAYOUT CHANGES.

SERVICE CENTER DISTRIBUTION YES X NO

FORMAT USED:
CADAM CATIA ALLEGRO PRO-E META
WP5 W5.1 WORD DESIGNER

NO. B35551-198

PAGE 1 OF 2

*COMPUTER GENERATED EXCEL 4.0

10-20-00 10-12-00

B35551-198-01

SPACE SYSTEMS TECHNOLOGY GROUP

PRODUCT DEFINITION ORDER

CONTINUATION SHEET

ITEM	DOCUMENT NO.	REV	OWC	DESCRIPTION	DOC SIZE	NEXT HIGHER ASSY.

BASIC NO.					REV
MASTER CHANGE ORDER	MCO			DASH	
CHANGE ORDER	CO		-		
RELEASE NOTICE	RN		-		
VARIATION AUTHORITY	VA	X	B35551 - 198		
STOP ORDER	SO		-		
INFORMATION MEMO	IM		-		
DOCUMENT/PART REF NO			01-P571160J001		
MAT'L DISPOSITION /MFG. EFFECTS CONT.					

Add the following parts:

1. Solder a 0.0 Ohm jumper (P/N 06S11077A01) across D19 pads as shown in Fig. 1.

Note: D18, D19, R180, and R182 should be initially unpopulated per MCO L48748.

2. Solder a 0.0 Ohm jumper (P/N 06S11077A01) across D9 pads as shown in Fig. 2.

Note: D9, D10, and L15 should be initially unpopulated per MCO L48748.

3. Install P/N MMBV109LT1 screened at R26XX project level in location D10 as shown in Fig. 2.

FIG. 1

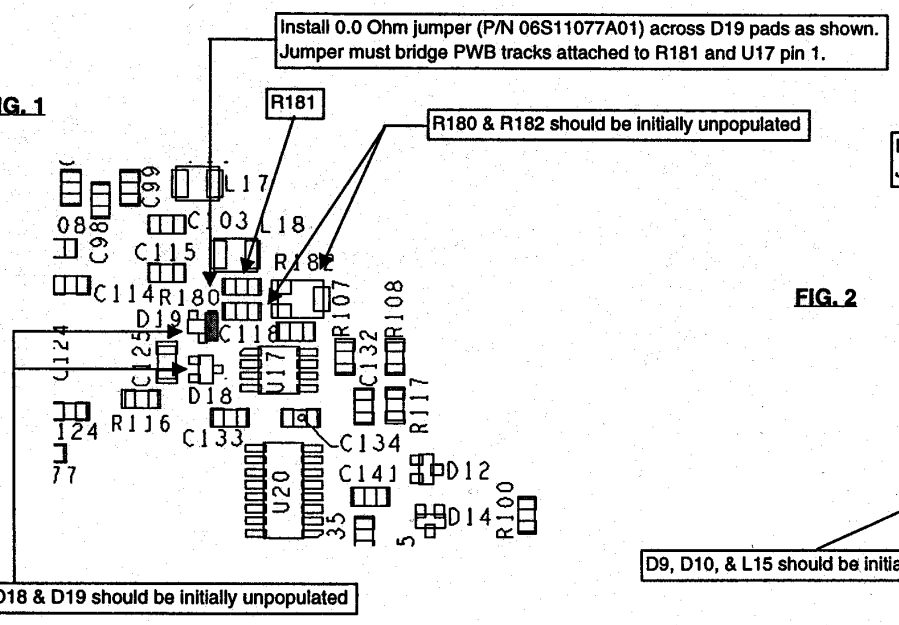
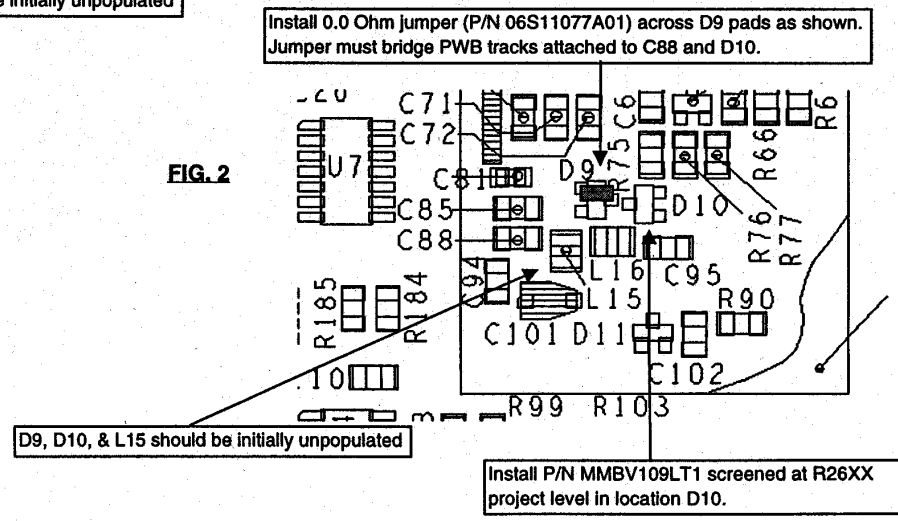


FIG. 2



QTY PER	VENDOR NAME	FIND NO.	QTY REQ	CODE IDENT NO	DRAWING OR DOCUMENT NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	SUPPLEMENTARY PART OR IDENTIFYING NO	NOTES

*COMPUTER GENERATED EXCEL 4.0

NO. B35551-198

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Go to Section 9

8.1 GENERAL DESCRIPTION

The High Tier receiver Module (A10) is installed in the RF cardcage in the sixth slot from the center of the Analyzer.

The High Tier Receiver Module recovers modulation signals from the 310.7MHz IF input signal (from RF Input Module). The input signal can be amplitude or frequency modulated with baseband information.

Separate detectors are provided for AM and FM. The demodulated outputs are routed to a set of audio filters.

Selectable high-pass and low-pass filters then further process the recovered modulation signal before it leaves the High Tier Receiver Module. Separate board outputs provide audio signals to the Interface Module for determining modulation level, the input frequency error, and for the speaker amplifier. Squelch circuitry allows muting of audio signals when there is no input signal present

This upgraded version of the Receiver Module is provided with the R2660 and R2670 models and is back-compatible with the R2600 model. It has additional features to support options. Two additional 10.7MHz outputs are added, one without AGC. The AGC can be disabled with the use of an additional control line.

The system processor provides primary control of the High Tier Receiver Module's functions via a set of latched parallel data lines.

8.2 SIGNALS SUMMARY

8.2A Signal Descriptions

AUDIO HPF 1-2 inputs from *the* Interface Module select the desired audio highpass filter (5Hz, 300Hz, 3KHz). See figure 8.4.2.2.

AUDIO LPF 1-2 inputs from the Interface Module select the desired audio lowpass filter (20KHz, 3KHz 300Hz). See figure 8.4.2.2.

DEMOD CAL AUDIO output is the unsquelched output of the demodulated receive signal.

IF OVERLOAD output to Interface Module is not used in the current Analyzer version.

LIM 700KHz output to the Interface Module is the limited output of the 700KHz IF and is used for frequency error measurements.

MOD SEL 2 selects AM or FM mode (0=AM, 1=FM).

RCV SPEAKER AUDIO output is the squelched version of the demodulated signal that is filtered only by a 5Hz highpass filter.

SPLITBAND input is reserved for possible use in future product development. It is not used in the current Analyzer version.

SQUELCH output indicates when the 310.7MHz RCV IF signal level is above a threshold set by the SQUELCH LEVEL input signal.

SQUELCH LEVEL input from Front Panel squelch adjustment sets the 310.7MHz RCV IF signal level required to break squelch.

SQUELCHED DEMOD output is a squelched version of the demodulated receive signal. (DEMOD CAL AUDIO).

SYNTH 10MHz REF input from Frequency Standard Module provides the reference signal for a 10MHz local oscillator.

WB/(NB)* selects wideband or narrowband mode.

DAGC EN* is an active low control signal that enables the Delayed AGC function in the 10.7MHz signal path.

310.7 MHz RCV IF input is the modulated IF signal from the RF Input Module.

321.4 MHz RCV LO from the Low Synthesizer Module is used to convert the 310.7MHz IF to a 10.7MHz IF.

OPTION 10.7MHz output is provided for use by options. This signal is not altered by the Delayed AGC (DAGC) circuit.

OPTION 10.7MHz-2 output is provided for by use by options. This signal is processed by the Delayed AGC (DAGC) circuit.

+12V and -12V at P1 supply power to the module.

8.2B Connector Descriptions

P1 (100 Pin Edge Connector to RF Motherboard)

pin	
1,2	GND
3-22	not used by this module
23	SQUELCH
24-40	not used by this module
41	DAGCEN*
42-67	not used by this module
68	WB/(NB)*
69	SPLITBAND, (not used at this time)
70-72	not used by this module
73	LIM 700 KHz
74-76	not used by this module
77	MOD SEL 2
78,79	not used by this module
80	AUDIO HPF 1
81	AUDIO HPF 2
82	AUDIO LPF 1
83	AUDIO LPF 2
84	SQUELCH LEVEL
85	not used by this module
86	RCV SPEAKER AUDIO
87	SQUELCHED DEMOD
88	DEMOD CAL AUDIO
89,90	GND
91,92	SYNTH 10 MHz REF
93-96	not used by this module
97,98	+12V
99,100	GND

SMB Connectors

J1 310.7 MHz RCV IF
Center Freq: 310.7MHz
1dB bandwidth. 10MHz minimum
60dB bandwidth: 42.8MHz maximum
Input level: -15dBm maximum
Input impedance: 50Ω nominal
VSWR: 2:1 maximum

J2 321.4 MHz RCV LO
Input freq. 321.4MHz
Input level: -2dBm, ±2dB
Input impedance: 50Ω nominal
VSWR: 2:1 maximum

J3 OPTION 10.7 MHz
Center Frequency: 10.7 MHz
Output Level: 0±3.5dB relative to 310.7 MHz RCV IF input level

J4 OPTION 10.7 MHz -2
Center Frequency: 10.7 MHz
Output Level -55dBm ±3dB during closed loop delayed AGC operation

8.3 BLOCK DIAGRAM DESCRIPTION

The linear IF section consists of:

1) Mixer that down-converts 310.7MHz IF to 10.7 MHz
2) Linear gain-controlled 10.7MHz amplifier chain and switchable IF bandwidths
3) Mixer that down-converts the 10.7 MHz IF to 700KHz
4) AGC amp
5) AM detector
6) FM detector

The major parts of the audio processing section are:

1) The speaker buffer amplifier
2) A 4 pole, selectable bandwidth highpass filter
3) A 4 pole, selectable bandwidth lowpass filter

8.4 DETAILED DESCRIPTION

8.4.1 Linear IF Section

8.4.1.1 310.7 MHz to 10.7 MHz Downconversion

The 310.7MHz RCV IF signal from the RF Input Module is input at J1. A resistive attenuator on this line (R4, R5, R13) provides a good load to the RF port of mixer U3. The local oscillator for this mix is the 321.4MHz RCV LO signal at J2 created by the Low Synthesizer Module. The 321.4MHz RCV LO, signal is amplified up to +7dBm by amplifier AR1. At U3, the 310.7MHz signal is down-converted to 10.7MHz.

8.4.1.2 10.7 MHz Amplifier Chain

The sum and difference of the RF and the LO frequencies are output at the IF port of U3 to an amplifier built around Q1. The IF port is presented a 50 ohm termination by R20. The output of this amp drives FL2. The output impedance of the transistor amp is approximately 330 ohms and represents the proper drive impedance for FL2.

FL2 has a bandwidth of approximately 280KHz. This filter rejects the unwanted mixer products while passing the desired 10.7 MHz product. Resistors R19 and R30 provide the proper terminating impedance to FL2. The output of FL2 drives gain controlled amplifier U2. The gain of this amplifier is controlled by the voltage driving pin 5.

SWITCHABLE IF BANDWIDTHS

The output of U2 drives selectable IF filters. Filter bandwidths of 280KHz and 17KHz can be selected (wideband/narrowband respectively: splitband is not utilized in the current Analyzer version). The desired filter is selected by turning on series diodes to the desired filter. Shunt diodes short the undesired filters to AC ground to eliminate leakage paths around the selected filter.

The output of the filter bank is input to a gain controlled amplifier, U4. The gain of this amplifier is controlled in the same manner as amplifier U2.

8.4.1.3 10.7 MHz IF to 700KHz IF Downconversion

The amplifier U4 drives an AM High Tier Receiver IC, U1. This IC contains gain controlled amplifiers, an active mixer, an AM detector, an audio preamplifier, and AGC circuitry.

In U1, the input signal is amplified by a gain controlled amplifier and then goes to an active mixer that down-converts the 10.7MHz IF to 700KHz. This down conversion permits the distribution of the IF gain between two, different frequency, amplifier strips to ease isolation and shielding requirements. A 10MHz LO for this mix is derived from the master 10MHz reference. This signal is converted from a CMOS logic signal to a sine wave by an amplifier built around Q12. The output of this amplifier is filtered by a tank circuit consisting of L18 and C170 resulting in a 10MHz sine wave.

The output of the mixer (at U1-1) is filtered by an external 3 pole lowpass filter to reject all unwanted mixer products. The output of this filter feeds two paths, one is the AM path, the other is the FM, path.

8.4.1.4 AM Path

The AM path feeds a transistor amplifier built around Q4. The output of this amplifier is further filtered by a tank circuit consisting of L12 and C45. The output of the amplifier drives a gain controlled amplifier contained in Ul (at U1-3). This amplifier feeds an AM detector, which demodulates the signal. The resultant demodulated signal is input to an audio preamplifier (in U1) and to AGC circuitry.

8.4.1.5 AGC Amplifier

The AGC loop provides the level of accuracy necessary for the AM modulation measurements. The AGC circuitry controls the gain of IF amps internal to U1 as well as amplifiers U2 and U4. AGC to U2 and U4 is delayed to prevent deterioration of the High Tier receiver's noise figure under initial gain-reduction.

There are two loop filters for the AGC loop. The first loop filter consists of C34, C41, C52, C53, and internal 7000 ohm resistors between U1 pin 7 and ground and between U1 pin 7 and pin 8. This filter is second order and has a bandwidth of 30Hz. The second loop filter consists of R80 and C112. This loop filter controls the delayed AGC and has a bandwidth of a few Hertz.

From the audio preamplifier the demodulated audio is input to a 10KHz lowpass filter internal to U1. To widen the audio bandwidth of the AM audio, the audio is input to a frequency compensation network consisting of C155, C162, and R128. U27 and U22 provide additional gain and AM-gain calibration. The demodulation gain is adjusted by R119. Thermistor RT1 compensates for the slight thermal drift in the demodulation gain in U1.

The delayed AGC control uses amplifiers U11A and U11B to control U2 and U4 amplifier gains. A delayed AGC enable (DAGC EN*) switch is comprised of Q16 and Q17. A logic high DAGC EN* input forces the U11B output to a maximum value which forces the AGC gain to minimum value. This disables the AGC and is used when the option output OPTION 10.7 MHz is utilized.

8.4.1.6 FM Path

The FM path is through amplifier U9. An LC tank circuit on the output of U9 (L17, C87) filters the signal further. The output of U9 feeds a limiter made up of Q6 and Q8. Diode D10 acts as a clamp to eliminate the possibility of large signals overloading the limiter. The output of the limiter is a 0-5V logic level that drives U18. U18 acts as a buffer and is used to drive the 700KHz output and the pulse counting discriminator.

The 700KHz output is a limited version of the 700KHz FM signal. It is output to the interface board where it is counted. The frequency of this signal is used to calculate the instantaneous frequency error of the High Tier receiver input signal.

A pulse counting (averaging) technique is used for FM demodulation. That is, a constant width and amplitude pulse is generated for each zero-crossing of the IF signal. The pulses are then averaged in an RC lowpass filter to generate a voltage proportional to the input frequency. The output is then a DC voltage proportional to the average frequency, with the FM demodulated signal riding on top.

The High Tier receiver uses a dual edge triggered monostable timer to provide a pulse with each zero-crossing, thereby doubling the carrier frequency and easing the filtering requirements. Differential amplification by U23 removes the DC offset and increases detection gain by 6dB. The pulse width is set for a 50 percent duty cycle at 700KHz, the nominal IF center frequency. The amplifier formed by half of U23 and U33 provide additional filtering and FM gain calibration at R153.

8.4.2 Audio Processing Circuits

Under processor control, the audio processing circuits provide filtering, gain scaling, squelch, and detector selection. A processor controlled demultiplexer selects either AM or FM audio. The audio at this point is filtered by a 5Hz highpass filter and split into two paths.

8.4.2.1 Speaker Audio

The first path goes to the speaker buffer amplifier. The speaker buffer is gated off and on by the squelch control. The speaker audio bypasses the low and highpass filters, and is filtered only by a 5Hz highpass filter. Speaker audio is then routed to the interface board where it is amplified to drive the speaker.

8.4.2.2 Other Audio (R-2600 series only)

FILTERING

The second audio path is through one of three 4 pole, selectable bandwidth highpass filters. These filters provide 5Hz, 300Hz, and 3KHz highpass filtering. The 300Hz and 3KHz filters can be bypassed for low frequency signals. From the highpass filter, the audio is routed to one of three 4 pole, selectable bandwidth lowpass filters. The filters provide lowpass filtering at either 300Hz, 3KHz or 20 KHz.

OUTPUTS

From the lowpass filter, the audio is split into 2 paths.

The first path goes to a buffer amp that drives the DEMOD CAL AUDIO line. This line is used primarily by Analyzer options.

The second output is the SQUELCHED DEMOD AUDIO line that drives the metering circuitry in the Interface module. A large blocking cap (C114) together with an offset adjustment (R92) on the last op-amp stage of this output provide the very low DC offset needed for accurate measurements. This output is gated off and on by the squelch control.

HPF 1	HPF 2	AudioHighpass Filter
0	0	5 Hz
1	0	300 Hz
0	1	3 KHz
1	1	undefined

LPF 1	LPF 2	Audio Lowpass Filter
0	0	20 KHz
1	0	3 KHz
0	1	300 Hz
1	1	undefined

Fig. 8.4.2.2 Audio Filter Selections (R2600 series only)

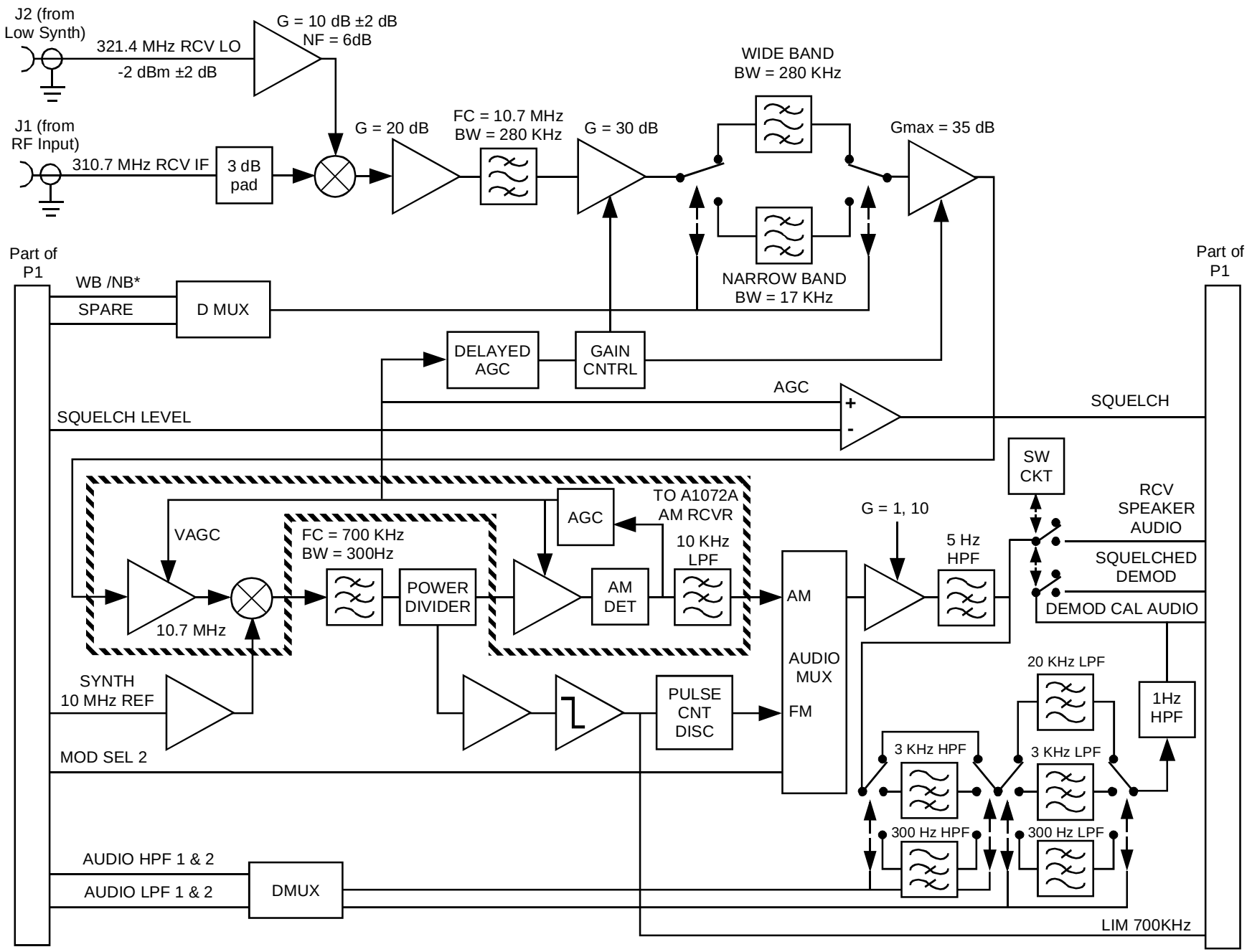
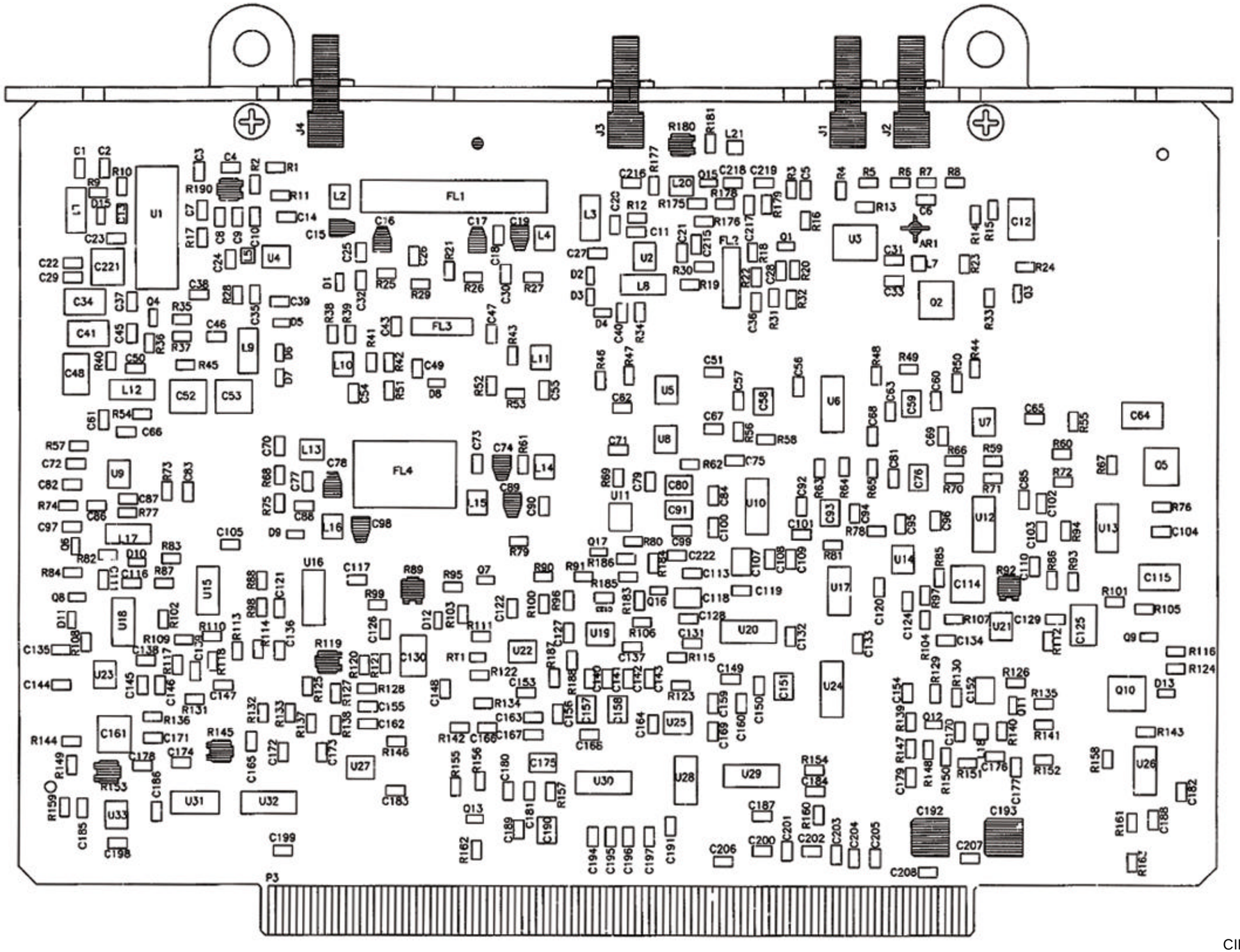


Fig. 8.5 High Tier Receiver Module Block Diagram



CIRCUIT CARD ASSEMBLY
HIGH TIER RECEIVER

01-P30680C REV. A

SHEET 1 OF 1

DWG NO 63-P30682C SH 1

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
	CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY		
	INITIAL RELEASE		
A	ECO E5A143 CARD TO CONCEPT JFP	95-04-06	95-04-05 D.ANAYA

NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A10.

2. FOR REFERENCE DRAWINGS REFER TO:
   01-P30680C ASSEMBLY
   12-P30683C TEST PROCEDURE

3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS.
   ALL CAPACITORS ARE IN UF.
   ALL INDUCTORS ARE IN UH.
   ALL VOLTAGES ARE IN DC.

4. TERMINATIONS CODED WITH THE SAME LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.

5. DEVICE TYPE NUMBERS AND CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE 1.

TABLE 1 * *

REF DES	DEVICE TYPE	VCC CONNECTION +5VREG	+10VREG	-10VFIL	+12V	GND CONN	NO CONNECTION
AR1	MAR-3					2,4	
U1	TDA1072A		13*			16	
U2	MC1350		1,2 *			3,7	
U3	RMS-1					2,3,6	
U4	MC1350		1,2 *			3,7	
U5	MC34072		8	4			
U6	DG211	12	13	4			
U7	MC34081		7	4			
U8	MC34072		8	4			
U9	MC1350		1,2 *			3,7	
U10	DG211	12	13	4			
U11	MC34072		8	4			
U12	DG211	12	13	4			
U13	MC1723C				12	7	
U14	MC34072			4			
U15	74AC025C	14				7	
U16	74LS221	16				8	
U17	74AC025C	14				7	
U18	74AC025C	14				7	
U19	MC34072		8	4			
U20	DG211	12	13	4			
U21	MC34081		7	4			
U22	MC34072		8	4			
U23	MC34072		8	4			
U24	74AC139	16				8	
U25	MC34072		8	4			
U26	MC1723C				12	7	
U27	MC34072		8	4			
U28	74AC00	14				7	
U29	74AC139	16				8	
U30	DG211	12	13	4			
U31	74AC00	14				7	
U32	DG211	12	13	4			
U33	MC34072		8	4			

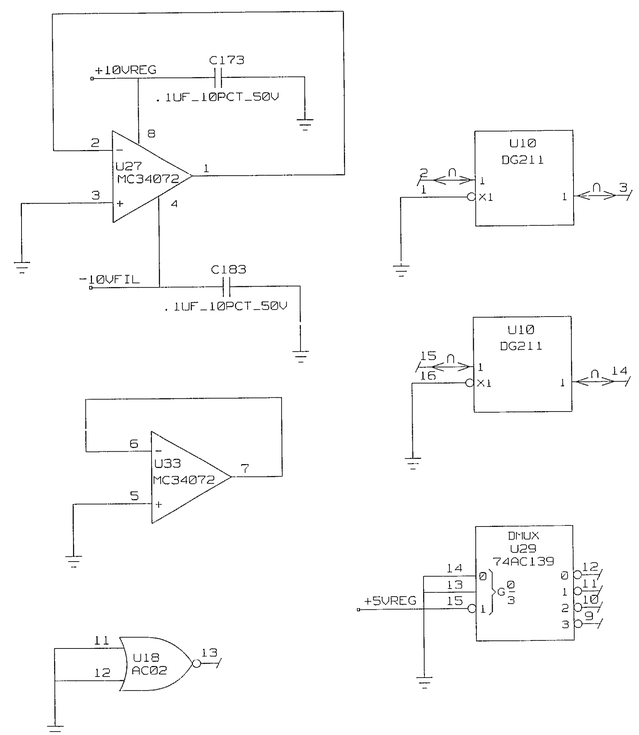
* CONNECTED TO VCC THRU 10 OHM RESISTOR

* * TABLE 1 IS FOR REFERENCE ONLY.
ALL CONNECTIONS ARE SHOWN ON SCHEMATIC.

TABLE 2

REFERENCE DESIGNATIONS	
HIGHEST NUMBER USED	NOT USED
AR1	
C222	C42,44,106, 112,209-214, 220
D15	D14
FL4	
J4	
L21	L6,19
P3	P1,2
Q17	Q14
R190	R164-174, 182,189
RT1	
U33	

SPARES:



ALL SHEETS CARRY THE SAME REVISION LETTER

ALL SHEETS ARE THE SAME REVISION STATUS

		CONTR	
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		APPROVALS	
		DWN	V.HARWOOD 94-01-28
		CHKR	A.HELWIG 94-01-31
		QA	K.NELSON 94-01-31
		MATL	K.CHANEY 94-01-31
01-P30680C	COCHISE	MFG	K.CHANEY_94-01-31
NEXT ASSY	USED ON	ENG	A.HELWIG 94-01-31
APPLICATION		CUST	

MOTOROLA INC.
GOVERNMENT AND SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

TITLE
HIGH TIER RECEIVER
SCHEMATIC DIAGRAM

SIZE D | CAGE CODE 94990 | DWG NO 63-P30682C

SCALE NONE | SHEET 1 OF 11

1103-22-1

ASME Y14.1-1995 DRAWING FORMAT - 3/95

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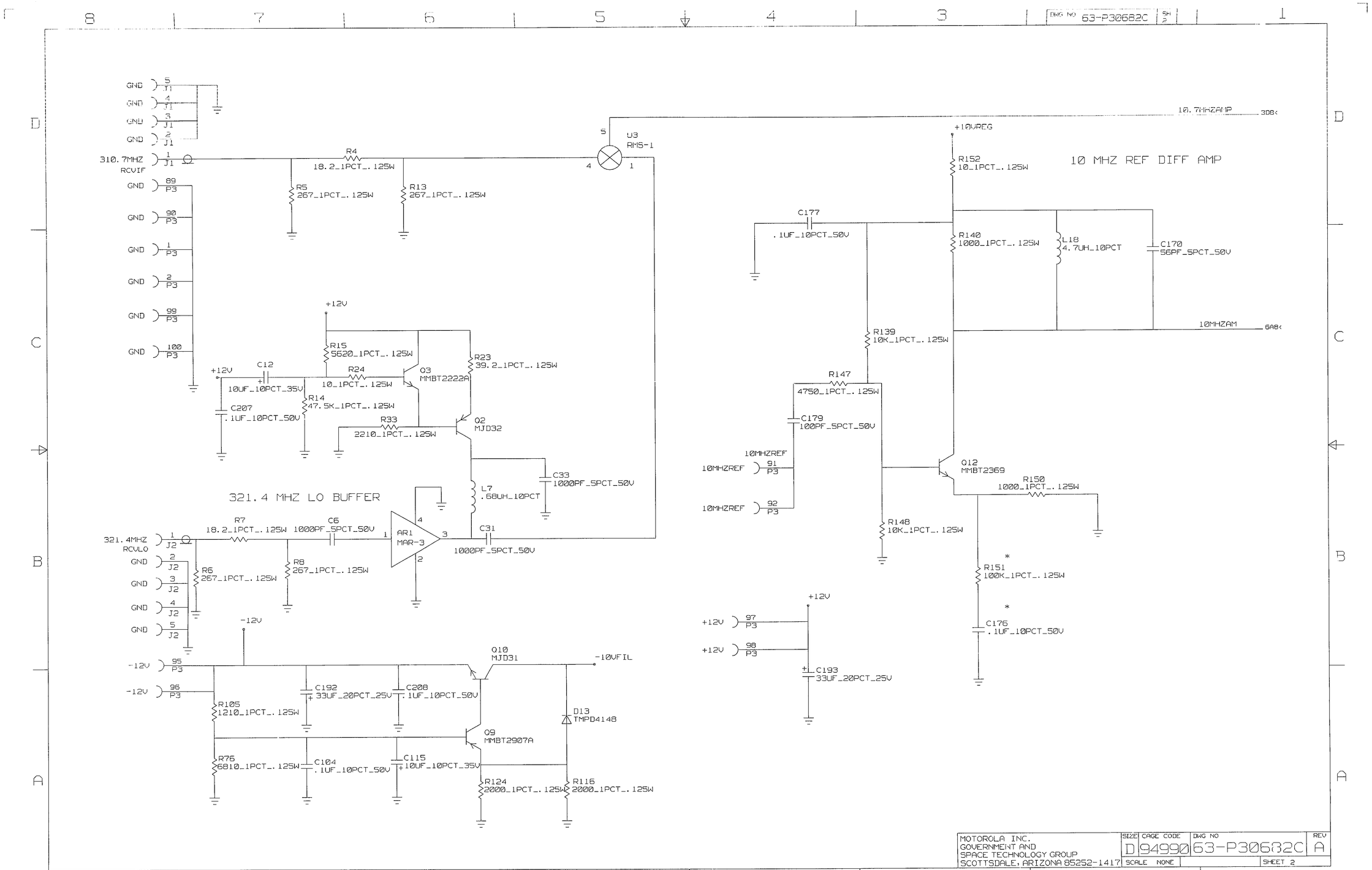
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10 MHZ REF DIFF AMP
321.4 MHZ LO BUFFER
310.7MHZ RCVIF
321.4MHZ RCVLO
10.7MHZAMP
10MHZAM
10MHZREF
+10VREG
-10VFIL
U3 RMS-1
AR1 MAR-3
Q2 MJD32
Q3 MMBT2222A
Q9 MMBT2907A
Q10 MJD31
Q12 MMBT2369
D13 TMPD4148
R4 18.2_1PCT_.125W
R5 267_1PCT_.125W
R13 267_1PCT_.125W
R15 5620_1PCT_.125W
R23 39.2_1PCT_.125W
R24 10_1PCT_.125W
R14 47.5K_1PCT_.125W
R33 2210_1PCT_.125W
C12 10UF_10PCT_35V
C207 .1UF_10PCT_50V
C33 1000PF_5PCT_50V
L7 .68UH_10PCT
R7 18.2_1PCT_.125W
C6 1000PF_5PCT_50V
C31 1000PF_5PCT_50V
R6 267_1PCT_.125W
R8 267_1PCT_.125W
R105 1210_1PCT_.125W
C192 33UF_20PCT_25V
C208 .1UF_10PCT_50V
R76 6810_1PCT_.125W
C104 .1UF_10PCT_50V
C115 10UF_10PCT_35V
R124 2000_1PCT_.125W
R116 2000_1PCT_.125W
R152 10_1PCT_.125W
C177 .1UF_10PCT_50V
R140 1000_1PCT_.125W
L18 4.7UH_10PCT
C170 56PF_5PCT_50V
R139 10K_1PCT_.125W
R147 4750_1PCT_.125W
C179 100PF_5PCT_50V
R148 10K_1PCT_.125W
R150 1000_1PCT_.125W
R151 100K_1PCT_.125W
C176 .1UF_10PCT_50V
C193 33UF_20PCT_25V
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D
CAGE CODE 94990
DWG NO 63-P30682C
REV A
SCALE NONE
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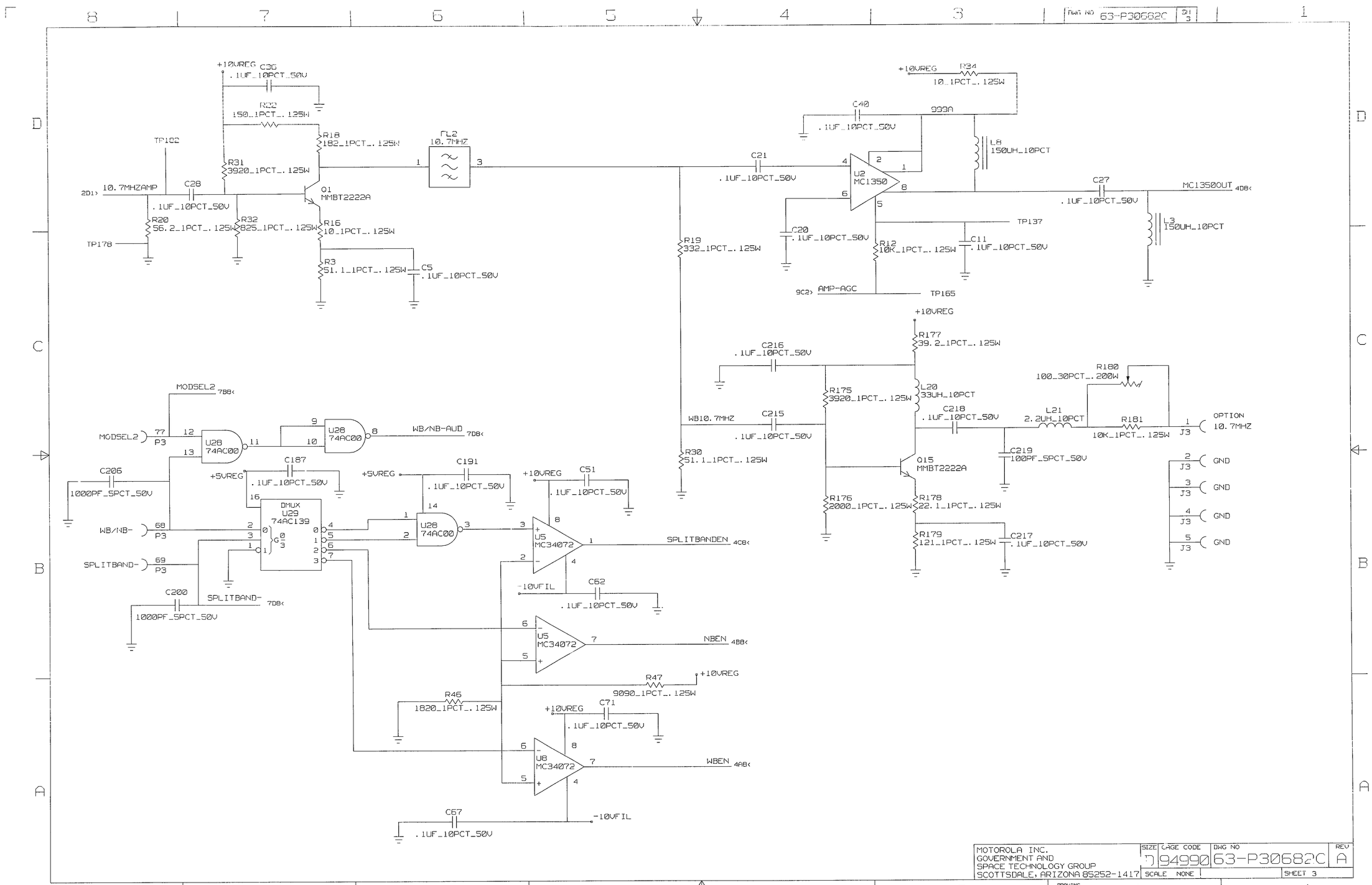

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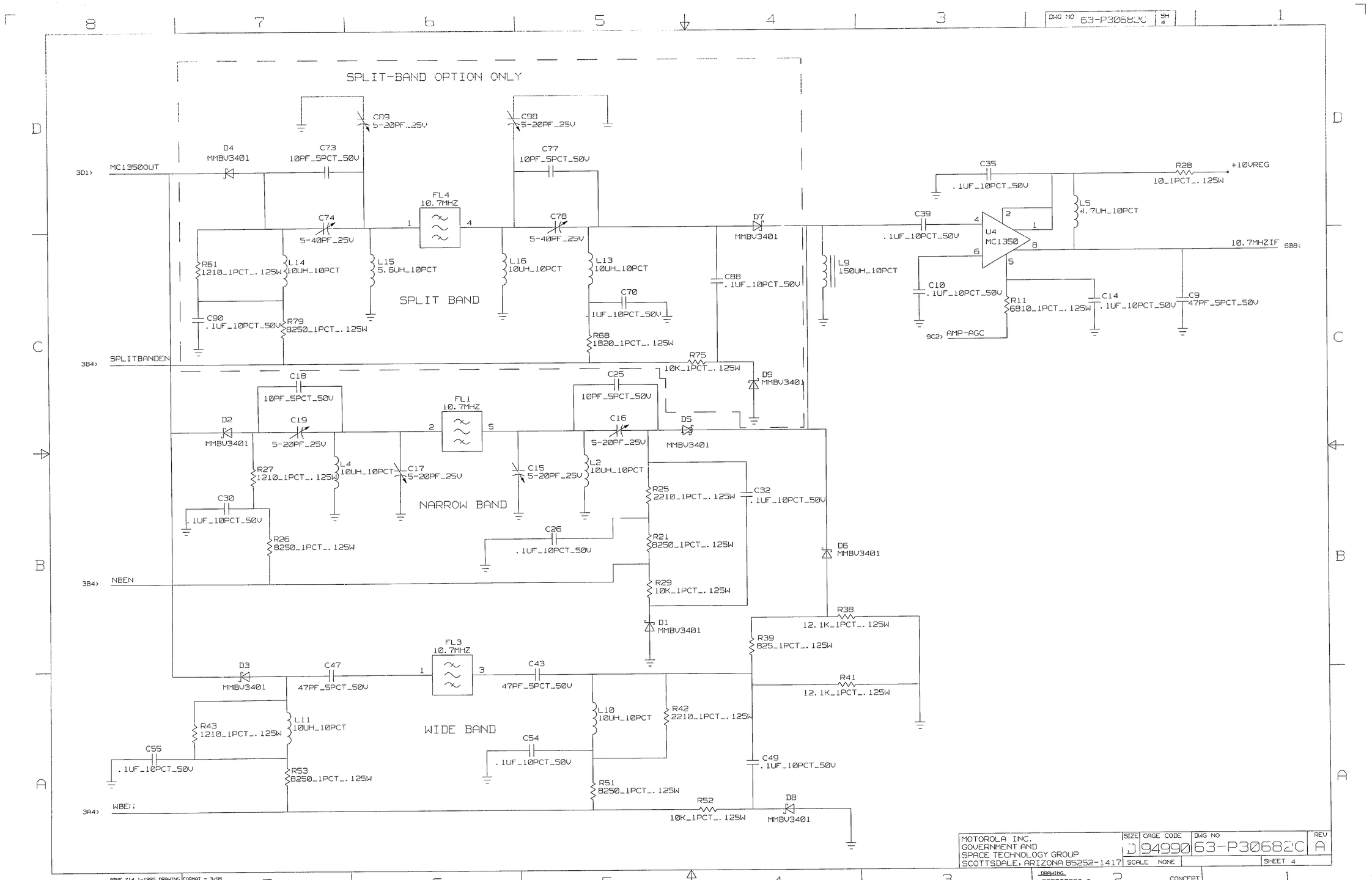
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SPLIT-BAND OPTION ONLY
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C98 5-20PF_25V
D4 MMBV3401
C73 10PF_5PCT_50V
C77 10PF_5PCT_50V
3D1> MC13500UT
FL4 10.7MHZ
C74 5-40PF_25V
C78 5-40PF_25V
D7 MMBV3401
R61 1210_1PCT_.125W
L14 10UH_10PCT
L15 5.6UH_10PCT
L16 10UH_10PCT
L13 10UH_10PCT
SPLIT BAND
C90 .1UF_10PCT_50V
R79 8250_1PCT_.125W
C70 .1UF_10PCT_50V
R68 1820_1PCT_.125W
C88 .1UF_10PCT_50V
3B4> SPLITBANDEN
R75 10K_1PCT_.125W
D9 MMBV3401
C35 .1UF_10PCT_50V
R28 10_1PCT_.125W
+10VREG
L5 4.7UH_10PCT
C39 .1UF_10PCT_50V
U4 MC1350
10.7MHZIF 6B8<
L9 150UH_10PCT
C10 .1UF_10PCT_50V
R11 6810_1PCT_.125W
C14 .1UF_10PCT_50V
C9 47PF_5PCT_50V
9C2> AMP-AGC
C18 10PF_5PCT_50V
FL1 10.7MHZ
C25 10PF_5PCT_50V
D2 MMBV3401
C19 5-20PF_25V
C16 5-20PF_25V
D5 MMBV3401
R27 1210_1PCT_.125W
L4 10UH_10PCT
C17 5-20PF_25V
C15 5-20PF_25V
L2 10UH_10PCT
NARROW BAND
C30 .1UF_10PCT_50V
R26 8250_1PCT_.125W
R25 2210_1PCT_.125W
C32 .1UF_10PCT_50V
C26 .1UF_10PCT_50V
R21 8250_1PCT_.125W
D6 MMBV3401
3B4> NBEN
R29 10K_1PCT_.125W
D1 MMBV3401
R38 12.1K_1PCT_.125W
R39 825_1PCT_.125W
FL3 10.7MHZ
D3 MMBV3401
C47 47PF_5PCT_50V
C43 47PF_5PCT_50V
R41 12.1K_1PCT_.125W
R43 1210_1PCT_.125W
L11 10UH_10PCT
WIDE BAND
L10 10UH_10PCT
R42 2210_1PCT_.125W
C55 .1UF_10PCT_50V
C54 .1UF_10PCT_50V
C49 .1UF_10PCT_50V
R53 8250_1PCT_.125W
R51 8250_1PCT_.125W
3A4> WBEN
R52 10K_1PCT_.125W
D8 MMBV3401
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE J CAGE CODE 94990 DWG NO 63-P30682C REV A
SCALE NONE
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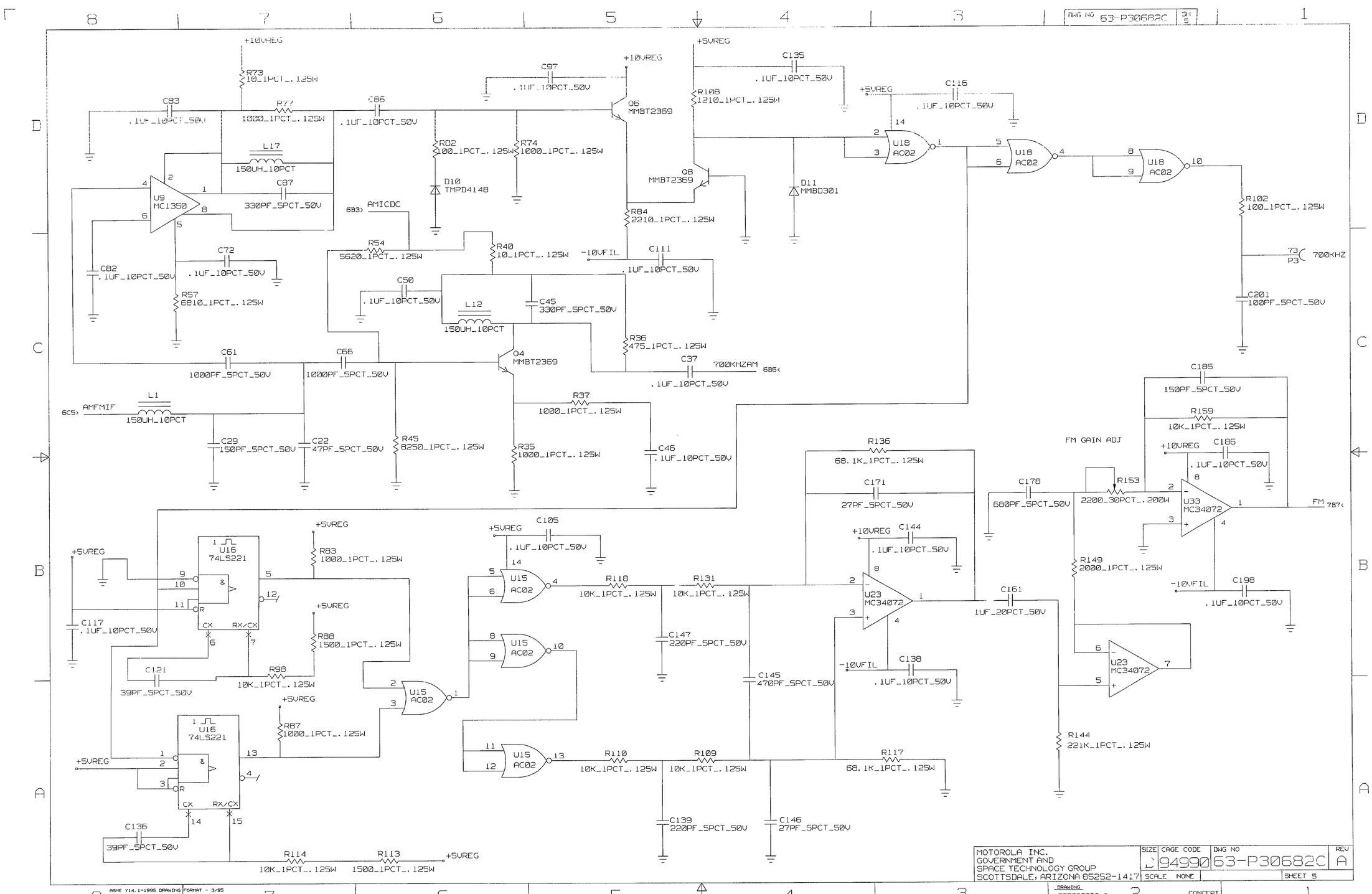
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R77 1000_1PCT_.125W
C86 .1UF_10PCT_50V
C97 .1UF_10PCT_50V
Q6 MMBT2369
+5VREG
C135 .1UF_10PCT_50V
R108 1210_1PCT_.125W
C115 .1UF_10PCT_50V
U18 AC02
L17 150UH_10PCT
C87 330PF_5PCT_50V
U9 MC1350
R02 100_1PCT_.125W
R74 1000_1PCT_.125W
D10 TMPD4148
Q8 MMBT2369
D11 MMBD301
R84 2210_1PCT_.125W
AMICDC
R102 100_1PCT_.125W
73 P3 700KHZ
C201 100PF_5PCT_50V
C82 .1UF_10PCT_50V
C72 .1UF_10PCT_50V
R57 6810_1PCT_.125W
R54 5620_1PCT_.125W
R40 10_1PCT_.125W
-10VFIL
C111 .1UF_10PCT_50V
C50 .1UF_10PCT_50V
L12 150UH_10PCT
C45 330PF_5PCT_50V
R36 475_1PCT_.125W
C37 .1UF_10PCT_50V
700KHZAM
Q4 MMBT2369
C61 1000PF_5PCT_50V
C66 1000PF_5PCT_50V
L1 150UH_10PCT
AMFMIF
C29 150PF_5PCT_50V
C22 47PF_5PCT_50V
R45 8250_1PCT_.125W
R37 1000_1PCT_.125W
R35 1000_1PCT_.125W
C46 .1UF_10PCT_50V
C185 150PF_5PCT_50V
R159 10K_1PCT_.125W
FM GAIN ADJ
C186 .1UF_10PCT_50V
R136 68.1K_1PCT_.125W
C171 27PF_5PCT_50V
C178 680PF_5PCT_50V
R153 2200_30PCT_.200W
U33 MC34072
FM
U16 74LS221
R83 1000_1PCT_.125W
C105 .1UF_10PCT_50V
C144 .1UF_10PCT_50V
U15 AC02
R118 10K_1PCT_.125W
R131 10K_1PCT_.125W
U23 MC34072
C161 1UF_20PCT_50V
R149 2000_1PCT_.125W
C198 .1UF_10PCT_50V
C117 .1UF_10PCT_50V
R88 1500_1PCT_.125W
C147 220PF_5PCT_50V
C145 470PF_5PCT_50V
C138 .1UF_10PCT_50V
C121 39PF_5PCT_50V
R98 10K_1PCT_.125W
R87 1000_1PCT_.125W
R144 221K_1PCT_.125W
R110 10K_1PCT_.125W
R109 10K_1PCT_.125W
R117 68.1K_1PCT_.125W
C139 220PF_5PCT_50V
C146 27PF_5PCT_50V
C136 39PF_5PCT_50V
R114 10K_1PCT_.125W
R113 1500_1PCT_.125W
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE J CAGE CODE 94990 DWG NO 63-P30682C REV A
SCALE NONE SHEET 5
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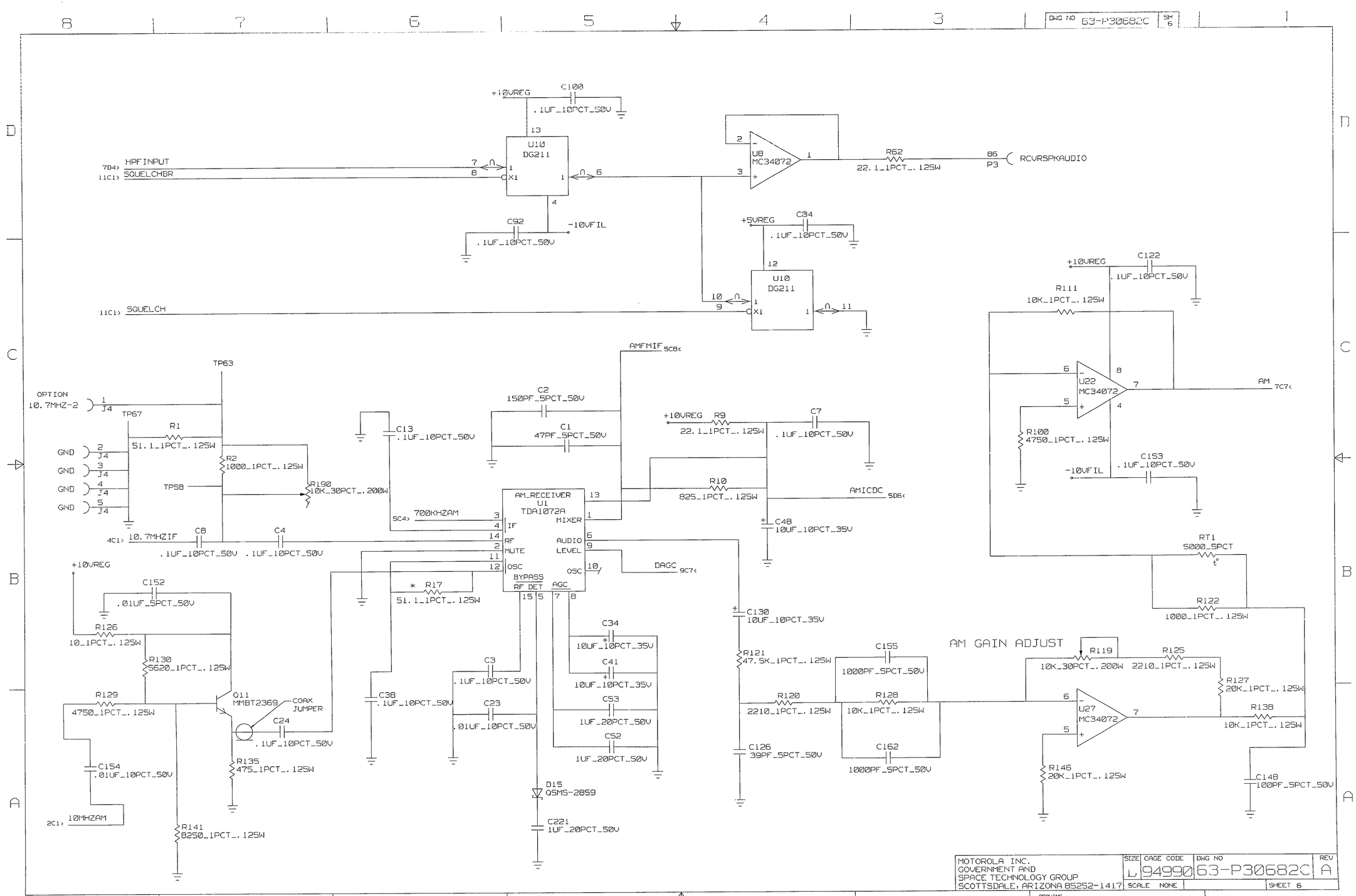
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U10
DG211
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-10VFIL
C92
.1UF_10PCT_50V
U8
MC34072
R62
22.1_1PCT_.125W
RCVRSPKAUDIO
+5VREG
C34
.1UF_10PCT_50V
11C1> SQUELCH
C122
R111
10K_1PCT_.125W
U22
MC34072
AM 7C7<
R100
4750_1PCT_.125W
C153
.1UF_10PCT_50V
AMFMIF 5C8<
TP63
OPTION
10.7MHZ-2
J4
TP67
R1
51.1_1PCT_.125W
GND
R2
1000_1PCT_.125W
TP58
R190
10K_30PCT_.200W
C2
150PF_5PCT_50V
C1
47PF_5PCT_50V
C13
.1UF_10PCT_50V
R9
22.1_1PCT_.125W
C7
.1UF_10PCT_50V
R10
825_1PCT_.125W
AMICDC 5D6<
C48
10UF_10PCT_35V
AM_RECEIVER
U1
TDA1072A
MIXER
IF
RF
MUTE
OSC
BYPASS
RF DET
AUDIO
LEVEL
AGC
5C4> 700KHZAM
4C1> 10.7MHZIF
C8
.1UF_10PCT_50V
C4
.1UF_10PCT_50V
DAGC 9C7<
R17
51.1_1PCT_.125W
RT1
5000_5PCT
R122
1000_1PCT_.125W
C152
.01UF_5PCT_50V
R126
10_1PCT_.125W
R130
5620_1PCT_.125W
Q11
MMBT2369
COAX JUMPER
C24
.1UF_10PCT_50V
R129
4750_1PCT_.125W
C154
.01UF_10PCT_50V
R135
475_1PCT_.125W
2C1> 10MHZAM
R141
8250_1PCT_.125W
C38
.1UF_10PCT_50V
C3
.1UF_10PCT_50V
C23
.01UF_10PCT_50V
C34
10UF_10PCT_35V
C41
10UF_10PCT_35V
C53
1UF_20PCT_50V
C52
1UF_20PCT_50V
D15
QSMS-2859
C221
1UF_20PCT_50V
C130
10UF_10PCT_35V
R121
47.5K_1PCT_.125W
R120
2210_1PCT_.125W
C126
39PF_5PCT_50V
C155
1000PF_5PCT_50V
R128
10K_1PCT_.125W
C162
1000PF_5PCT_50V
AM GAIN ADJUST
R119
10K_30PCT_.200W
R125
2210_1PCT_.125W
U27
MC34072
R127
20K_1PCT_.125W
R138
10K_1PCT_.125W
R146
20K_1PCT_.125W
C148
100PF_5PCT_50V
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE L
CAGE CODE 94990
DWG NO 63-P30682C
REV A
SCALE NONE
SHEET 6
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DRAWING 63P30682C_A P30682C
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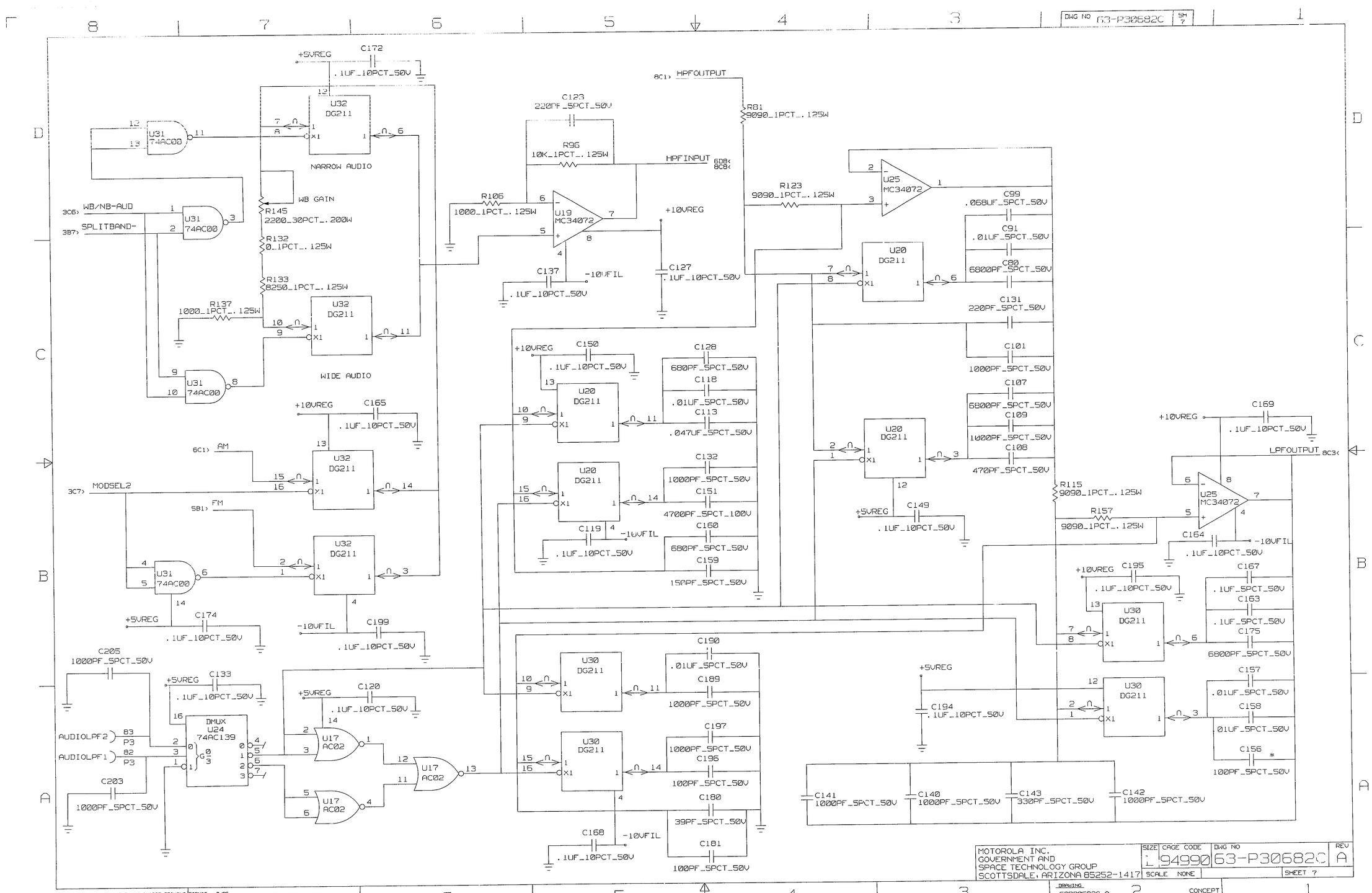
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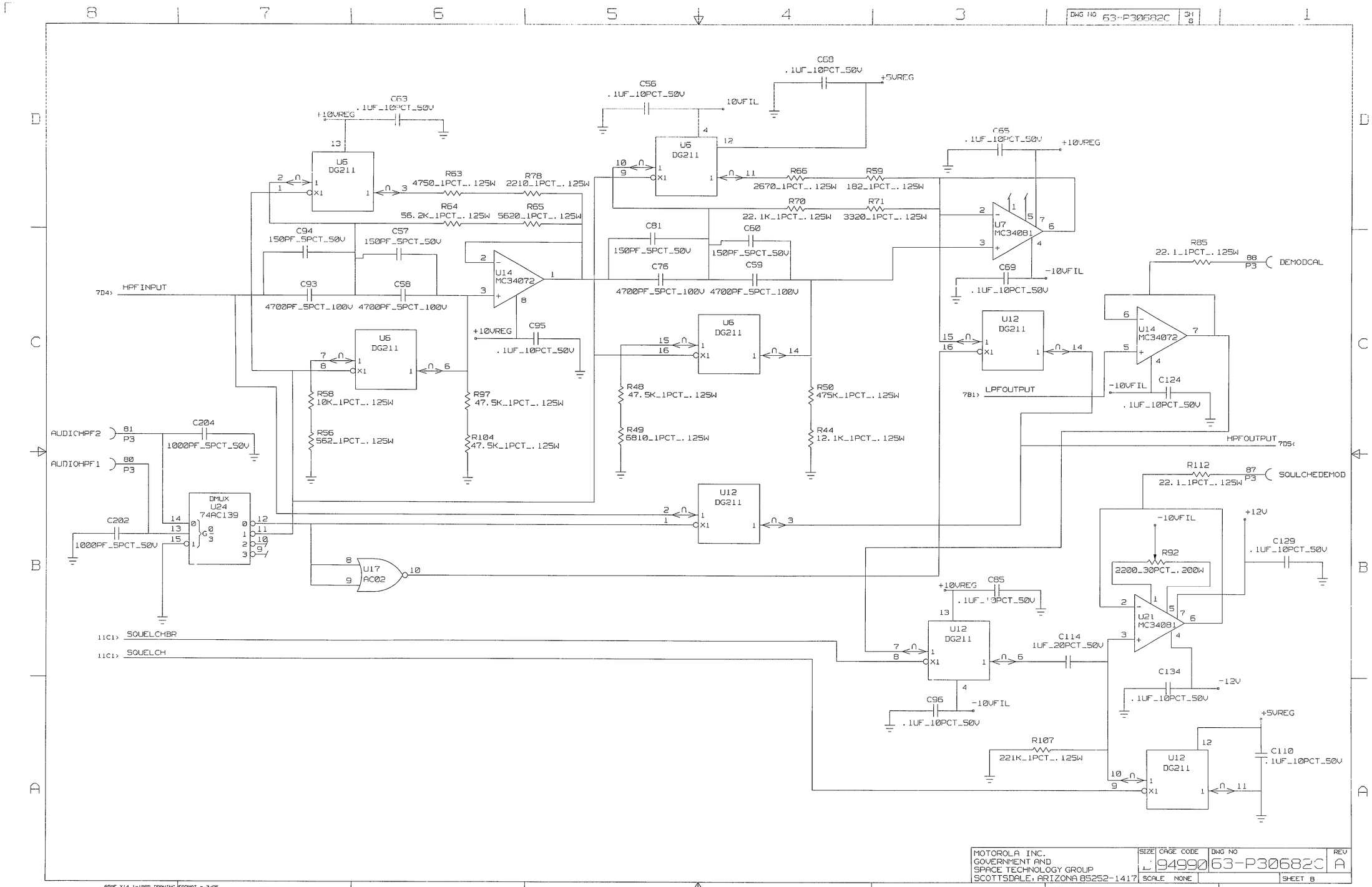
U32
DG211
U31
74AC00
NARROW AUDIO
WB GAIN
R145
2200_30PCT_.200W
R132
0_1PCT_.125W
R133
8250_1PCT_.125W
R137
1000_1PCT_.125W
WIDE AUDIO
3C6> WB/NB-AUD
3B7> SPLITBAND-
+10VREG
C165
6C1> AM
3C7> MODSEL2
5B1> FM
C174
-10VFIL
C199
C205
1000PF_5PCT_50V
C133
C120
DMUX
U24
74AC139
AUDIOLPF2
AUDIOLPF1
C203
U17
AC02
C123
220PF_5PCT_50V
R96
10K_1PCT_.125W
R106
1000_1PCT_.125W
U19
MC34072
C137
C127
8C1> HPFOUTPUT
R81
9090_1PCT_.125W
HPFINPUT
R123
9090_1PCT_.125W
U25
MC34072
C99
.068UF_5PCT_50V
C91
.01UF_5PCT_50V
C80
6800PF_5PCT_50V
C131
220PF_5PCT_50V
C101
1000PF_5PCT_50V
C107
6800PF_5PCT_50V
C109
1000PF_5PCT_50V
C108
470PF_5PCT_50V
C150
C128
680PF_5PCT_50V
C118
.01UF_5PCT_50V
C113
.047UF_5PCT_50V
C132
1000PF_5PCT_50V
C151
4700PF_5PCT_100V
C160
680PF_5PCT_50V
C159
150PF_5PCT_50V
C149
R115
9090_1PCT_.125W
R157
9090_1PCT_.125W
C169
LPFOUTPUT 8C3<
C164
C195
C167
C163
C175
6800PF_5PCT_50V
C157
C158
C156
100PF_5PCT_50V
C194
C190
C189
1000PF_5PCT_50V
C197
C196
100PF_5PCT_50V
C180
39PF_5PCT_50V
C181
100PF_5PCT_50V
C168
C141
1000PF_5PCT_50V
C140
1000PF_5PCT_50V
C143
330PF_5PCT_50V
C142
1000PF_5PCT_50V
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE L
CAGE CODE 94990
DWG NO 63-P30682C
REV A
SCALE NONE
SHEET 7
DRAWING 63P30682C_A P30682C
CONCEPT
TICKD
DSIZEPAGE2MD2C
ASME Y14.1-1995 DRAWING FORMAT - 3/95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C56 .1UF_10PCT_50V
10VFIL
C63 .1UF_10PCT_50V
+10VREG
U6 DG211
U5 DG211
C65 .1UF_10PCT_50V
+10VREG
R63 4750_1PCT_.125W
R78 2210_1PCT_.125W
R66 2670_1PCT_.125W
R59 182_1PCT_.125W
R64 56.2K_1PCT_.125W
R65 5620_1PCT_.125W
R70 22.1K_1PCT_.125W
R71 3320_1PCT_.125W
U7 MC34081
C94 150PF_5PCT_50V
C57 150PF_5PCT_50V
C81 150PF_5PCT_50V
C60 150PF_5PCT_50V
U14 MC34072
C76 4700PF_5PCT_100V
C59 4700PF_5PCT_100V
C69 .1UF_10PCT_50V
-10VFIL
R85 22.1_1PCT_.125W
88 P3
DEMODCAL
7D4> HPFINPUT
C93 4700PF_5PCT_100V
C58 4700PF_5PCT_100V
+10VREG
C95 .1UF_10PCT_50V
U12 DG211
R58 10K_1PCT_.125W
R97 47.5K_1PCT_.125W
R48 47.5K_1PCT_.125W
R50 475K_1PCT_.125W
7B1> LPFOUTPUT
C124 .1UF_10PCT_50V
R56 562_1PCT_.125W
R104 47.5K_1PCT_.125W
R49 6810_1PCT_.125W
R44 12.1K_1PCT_.125W
AUDIOHPF2 81 P3
C204 1000PF_5PCT_50V
HPFOUTPUT 7D5<
AUDIOHPF1 80 P3
R112 22.1_1PCT_.125W
87 P3
SQUELCHEDEMOD
DMUX U24 74AC139
C202 1000PF_5PCT_50V
-10VFIL
+12V
R92 2200_30PCT_.200W
C129 .1UF_10PCT_50V
U17 AC02
+10VREG
C85 .1UF_10PCT_50V
U21 MC34081
11C1> SQUELCHBR
11C1> SQUELCH
C114 1UF_20PCT_50V
C134 .1UF_10PCT_50V
-12V
C96 .1UF_10PCT_50V
-10VFIL
+5VREG
R107 221K_1PCT_.125W
C110 .1UF_10PCT_50V
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE C
CAGE CODE 94990
DWG NO 63-P30682C
REV A
SCALE NONE
SHEET 8
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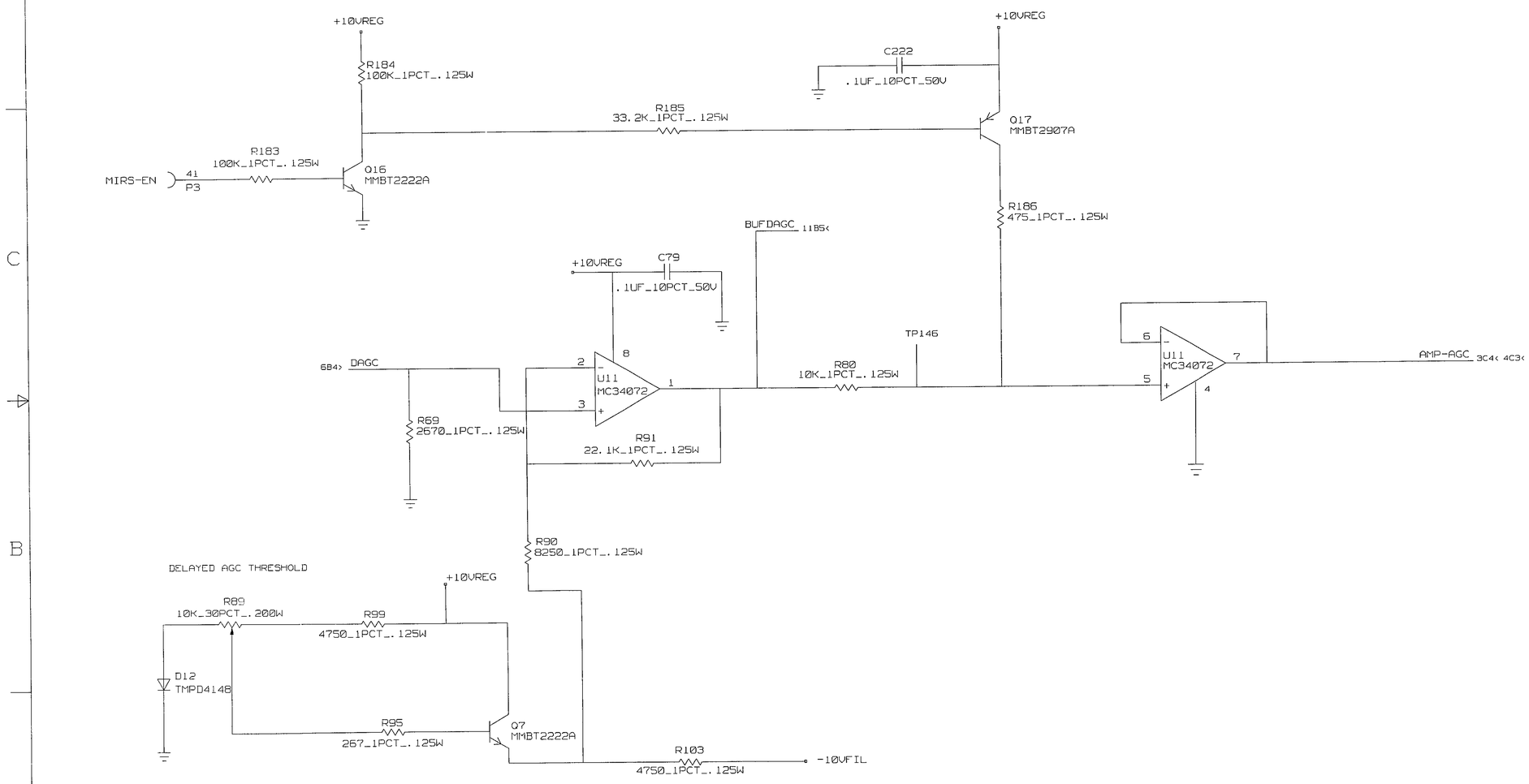

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ASME Y14.1-1995 DRAWING FORMAT - 3/95

DRAWING 63P30682C_A P30682C

CONCEPT TICKD

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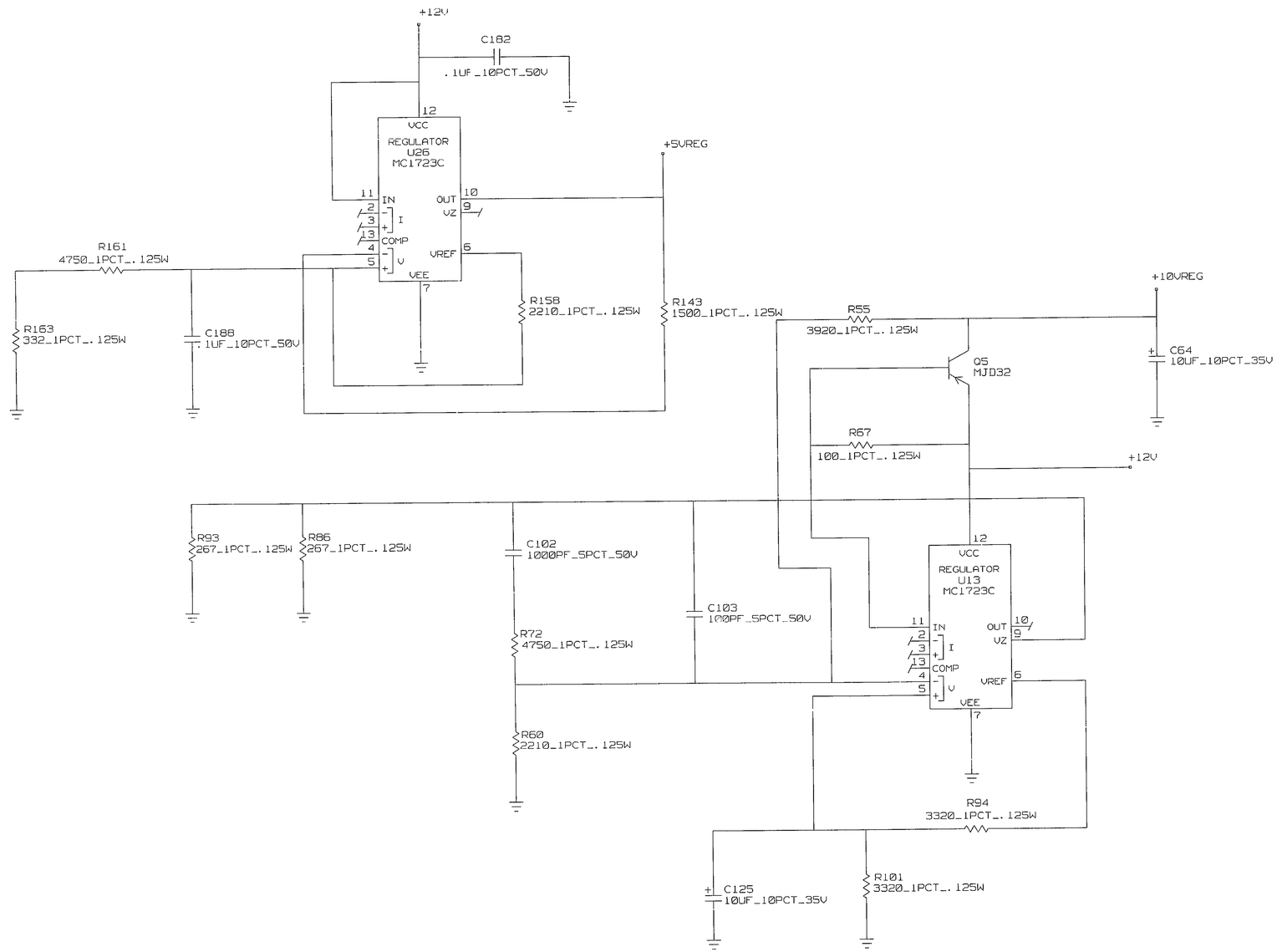

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	SCALE NONE		SHEET 10	

ASME Y14.1-1995 DRAWING FORMAT - 3/95

DRAWING 63P30682C_A P30682C

CONCEPT

TICKD

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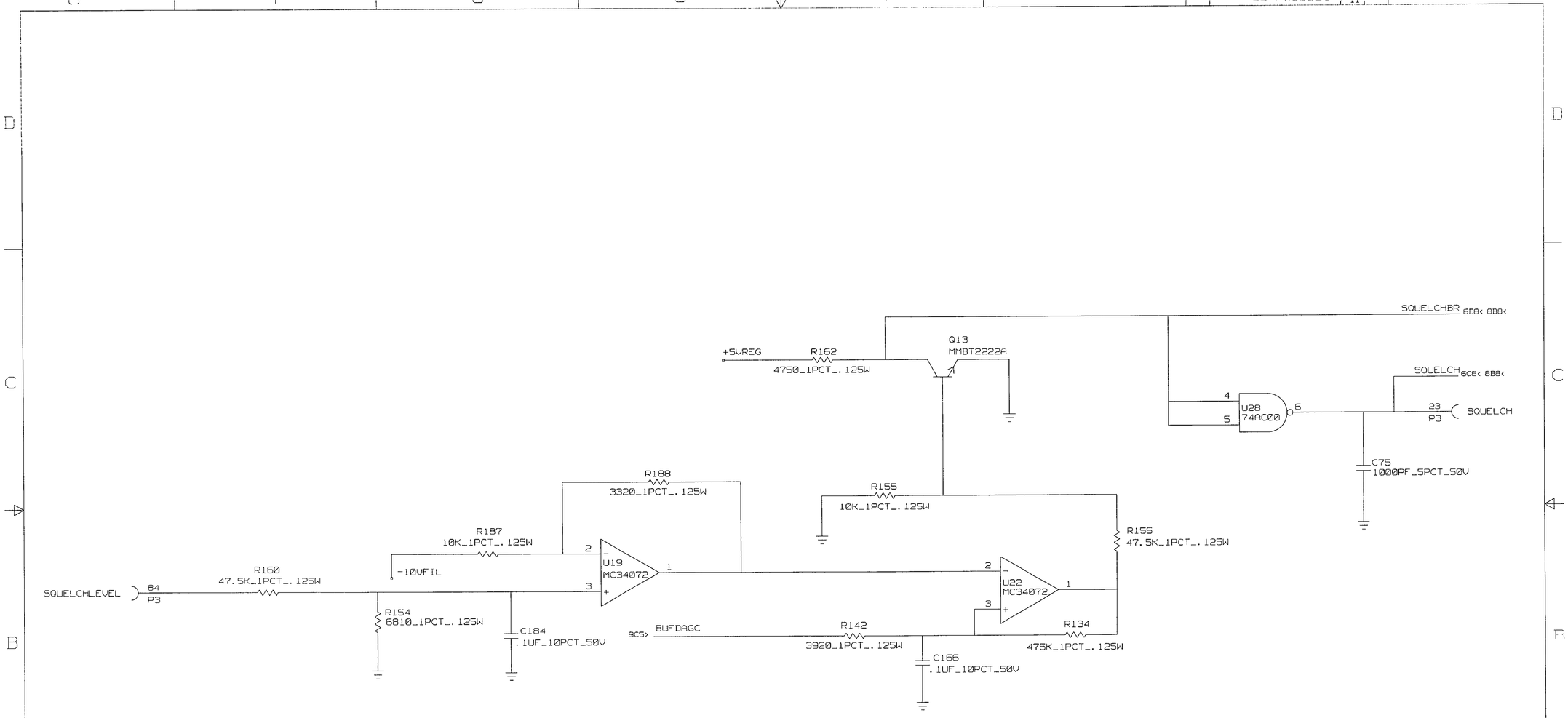

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	SCALE NONE		SHEET 11	

ASME Y14.1-1995 DRAWING FORMAT - 3/95

DRAWING 63P30682C_A P30682C

CONCEPT

TICKD

DSIZEPAGE2HD2C

Section 9
HIGH TIER GENERATOR MODULE

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9.1 GENERAL DESCRIPTION

The High Tier Generator Module (A5) is installed in the RF cardcage in the slot closest to the center of the Analyzer.

This module produces the 310.7 MHz LO signal that feeds the RF Output module. The modulation audio signal comes from the Interface Module to the High Tier Generator module's MOD CAL AUDIO input.

9.2 SIGNALS SUMMARY

9.2A Signal Descriptions

*GEN HI/(LO)** input enables switching between two VCO bands (for <=310.7 MHz or >310.7MHz frequency J1).

GEN SYNTH DATA input is the data line for programming the frequency synthesizer.

MOD CAL AUDIO input modulates the IF output signal (310.7MHz GEN).

MOD SEL 1, 2 & 3 input lines select the High Tier Generator's mode of operation and modulation type.

SA LO input from the Spectrum Analyzer Module at 289.3 MHz mixes with the High Tier Generator's 21.4MHz signal to produce the 310.7MHz GEN during AM mode.

SYNTH CLOCK input clocks data into the frequency synthesizer

SYNTH LATCH input latches the data serially clocked in by SYNTH CLOCK.

SYNTH 10 MHz Ref from the Frequency Standard Module is a single-ended input that drives a limiting amplifier.

*WB/(NB)** (wideband/narrowband) input changes the gain of the modulation.

310.7MHz GEN output is a 310.7MHz signal that can be unmodulated, or AM, FM or PM modulated. This signal also has the capability of being swept around a center frequency of 310.7MHz or can be offset from the 310.7MHz by any frequency within 310.7MHz ±55MHz in 5KHz steps. In addition, a low phase noise duplex signal capability is provided to support an Integrated Radio System (iDEN) Test option.

-5V, +12V, -12V, and +40V supply power to the module.

9.2B Connector Descriptions

P1 (50 Pin Edge Connector to RF Motherboard)

pin	
1,2	GND
3,4	not used by this module
5,6	-5V
7,8	+40V
9-11	not used by this module
12	SYNTH CLOCK
13	SYNTH LATCH
14	GEN SYNTH DATA
15,16	not used by this module
17	MOD SEL 3
18-21	not used by this module
22	WB/(NB)*
23	not used by this module
24	MOD SEL 1
25	not used by this module
26	MOD SEL 2
27	not used by this module
28	GEN HI/(LO)*
29-37	not used by this module
38	MOD CAL AUDIO
39,40	GND
41,42	SYNTH 10MHz REF
43,44	not used by this module
45,46	-12V
47,48	+12V
49,50	GND

SMB Connectors

J1 310.7MHz GEN
Center freq: 310.7 MHz
Freq sweep range: 310.7 MHz ± 5 MHz approx
Duplex offset freq: 255.7-365.7 MHz, 5 KHz steps
Output Impedance: 50Ω nominal
VSWR: 2:1 maximum
Output level: -17.5 ± 2.5dB
(FM or AM mode, 0% modulation)

J2 SA LO
Input freq 289.3 MHz in AM mode
Input freq sweep: 289.3 ±5 MHz
(FM or CW modes)
Input impedance: 50 Ω nominal
VSWR: 2.1 maximum

9.3 BLOCK DIAGRAM DESCRIPTION

In AM mode the High Tier Generator's output frequency is fixed at 310.7MHz and the modulation is applied.

In the FM/Duplex mode, the generator frequency is 310.7 ± 55 MHz in 5 KHz Steps and the signal can be FM modulated up to 99.5 KHz deviation. When the module's output frequency is at 310.7 MHz the system's transmit frequency is the same as its received frequency. When the High Tier Generator's frequency is offset by a certain amount, the system's transmit frequency is then offset by a like amount. The FM modulation capabilities are unaffected by the offset.

9.4 DETAILED DESCRIPTION

The three main sections are the modulation, synthesizer and AM sections.

9.4.1 Modulation Section

The modulation section consists of the module's mode-control circuitry, the 215MHz VCO FM modulator, and the AM double-balanced modulator.

9.4.1.1 Mode Control Circuitry

The MOD SEL 1, 2 & 3 Signals determine which mode is selected via Q12, U8, and U5. This circuit controls the RF switches and the modulation analog switch (part of U5), which routes the audio signal as needed.

9.4.1.2 Audio Processing

The modulation audio Signal comes from the Interface Module and is called MOD CAL AUDIO. This is lowpass filtered (at U3) using an active opamp filter with a 20KHz cutoff frequency. The audio signal then goes through AM/FM select analog switches and then to resistive attenuators, which are adjusted at manufacturing to set the FM and AM sensitivities. The WB/NB* signal selects the sensitivity of the FM modulator (12.5 or 1.25 KHz/volt) by choosing the proper audio attenuator at the input to the 215MHz VCO. The FM attenuators are temperature compensated to counteract variations in the 215MHz modulator's sensitivity.

9.4.1.3 215MHz VCO FM Modulator

The 215MHz VCO uses a stripline resonator with a varactor that is very lightly coupled to achieve the very small modulation sensitivity The 215MHz signal then is mixed with the 470-580MHz LO that is created in the synthesizer section.

9.4.1.4 AM Modulator

The AM double-balanced modulator is realized using an analog multiplier IC (U2). The 21.4MHz carrier is the result of setting the synthesizer (U11) frequency to 342.4MHz and sending it to the ECL divide-by-16 circuitry (U6, U4). In AM mode, the analog multiplier (U2) has as its input the audio modulation that has had a bias voltage added to it.

9.4.2 Synthesizer Section

The synthesizer section produces the 310.7 ±55MHz output signal in the FM/Duplex and CW modes and a 342.4MHz LO for use inside the module when in AM mode. A Low Phase Noise CW mode is provided for use by the iDEN option. This signal is 310.7MHz with duplex off-sets of ±39MHz and ±45 MHz.

The 310.7 ±55MHz signal is created by mixing the 215MHz LO with the 470.7-580.7MHz LO from VC01 or VC02 (selected via GEN HI/LO*). These two oscillators each cover half the band.

VCO1 is selected for synthesizer frequencies of 470.7 to 525.7 MHz (resulting in 255.7 to 310.7MHz at J1). VC02 is selected for frequencies >525.7MHz up to 580.7MHz (for frequencies >310.7 up to 365.7 MHz at J1). The resulting 310.7 ±55MHz frequency is amplified, bandpass filtered, and split into two paths.

One path goes through a buffer amp (AR3), then a limiting amp (Q10) to the PLL's UHF prescaler. The other path goes through a high power amplifier (AR1) and then through the RF switches to either the module output or to the divide-by 16 circuitry. The high power amplifier is needed to reduce the level of the higher harmonics, which can not be filtered out.

In the standard mode, the bandwidth of the PLL is about 1Hz so that the loop does not track out the modulation on the 215MHz signal for frequencies above 5Hz. Because the loop bandwidth is narrow, acquisition speed up circuitry is needed to keep the acquisition time as fast as possible.

In the low phase noise mode, the PLL bandwidth is modified to about 1KHz. This provides improved noise performance of the PLL for the iDEN option operation. The signal is not modulated in this mode.

The phase/frequency detector, N-A dividers and reference frequency dividers are all contained in a single PLL chip (U11) in conjunction with a 128/129 or 64/65 dual modulus prescaler (U9). The 128/129 configuration is selected for standard PLL mode. The 64/65 configuration is selected for the low phase noise PLL mode. The synthesizer is controlled serially from the interface module via the Gen Synth Data, Clock and Latch lines (see figures 9.4.2 A and B).

9.4.3 AM Section

The AM section contains the RF switches and the circuitry needed to produce and mix the 21.4MHz signal with the 289.3MHz SA LO.

In the AM mode the RF switches divert the LO into the divide-by-16 circuit and connect the modules output to the 10 MHz wide bandpass filter. When in these modes, the synthesizer is set to a frequency of 342.4MHz, and then divided by 16 to create the 21.4MHz signal. This 21.4MHz signal is the carrier that goes to the double-balanced modulator U2, where it is AM modulated. The modulated 21.4MHz carrier is then mixed with the 289.3 MHz SA LO to create the 310.7 MHz GEN output signal.

While in the FM/Duplex mode the RF switches are set so that the 310.7 MHz LO is fed directly to the output, as shown in the block diagram.

For PM operation, the AM signal path is used and the FM is enabled. The differentiation of the audio signal is performed before it is input to the MOD CAL AUDIO port of the module. The FM modulator provides the angle modulation necessary for PM.

15-bit Divide-by-R Data Word

control lsb msb(1st bit into shift reg)

1 0 0 0 0 1 0 1 1 1 1 1 0 0 0

In the High Tier Generator Module the R divider is set to 2000.

18-bit Divide-by-N, A Data Word

control	lsb msb	lsb msb
0	<— 7 bits —>	<— 10 bits —>
	A	N

Data is clocked in on the rising edge of SYNTH CLOCK When all 15 (or 18) bits have been entered, the rising edge of SYNTH LATCH latches the data as a parallel word and the frequency then switches.

Fig 9.4.2A PLL Data Word Format

$N_{tot}=F_o/F_{ref}$

$N=INT(N_{tot}/P)$

$A=N_{tot} - (N*P)$

F_o =operating frequency in 5KHz steps

F_{ref} =reference frequency = 5KHz (or 100KHz in low phase noise mode)

P=prescaler divide ratio=128 (or 64 in low phase noise mode)

N = "N" counter value

A = "A" counter value

Fig 9.4.2B PILL N and A Values

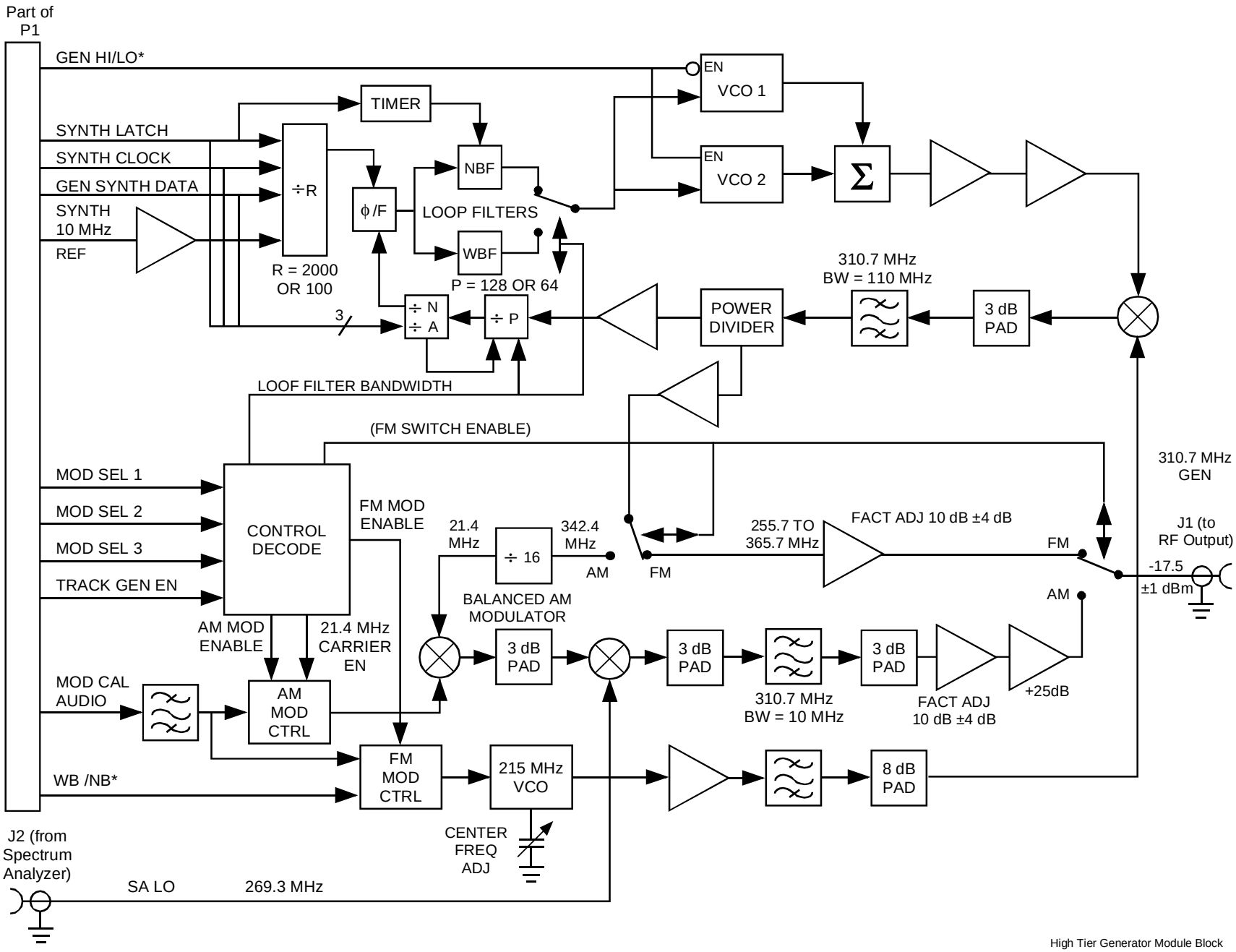
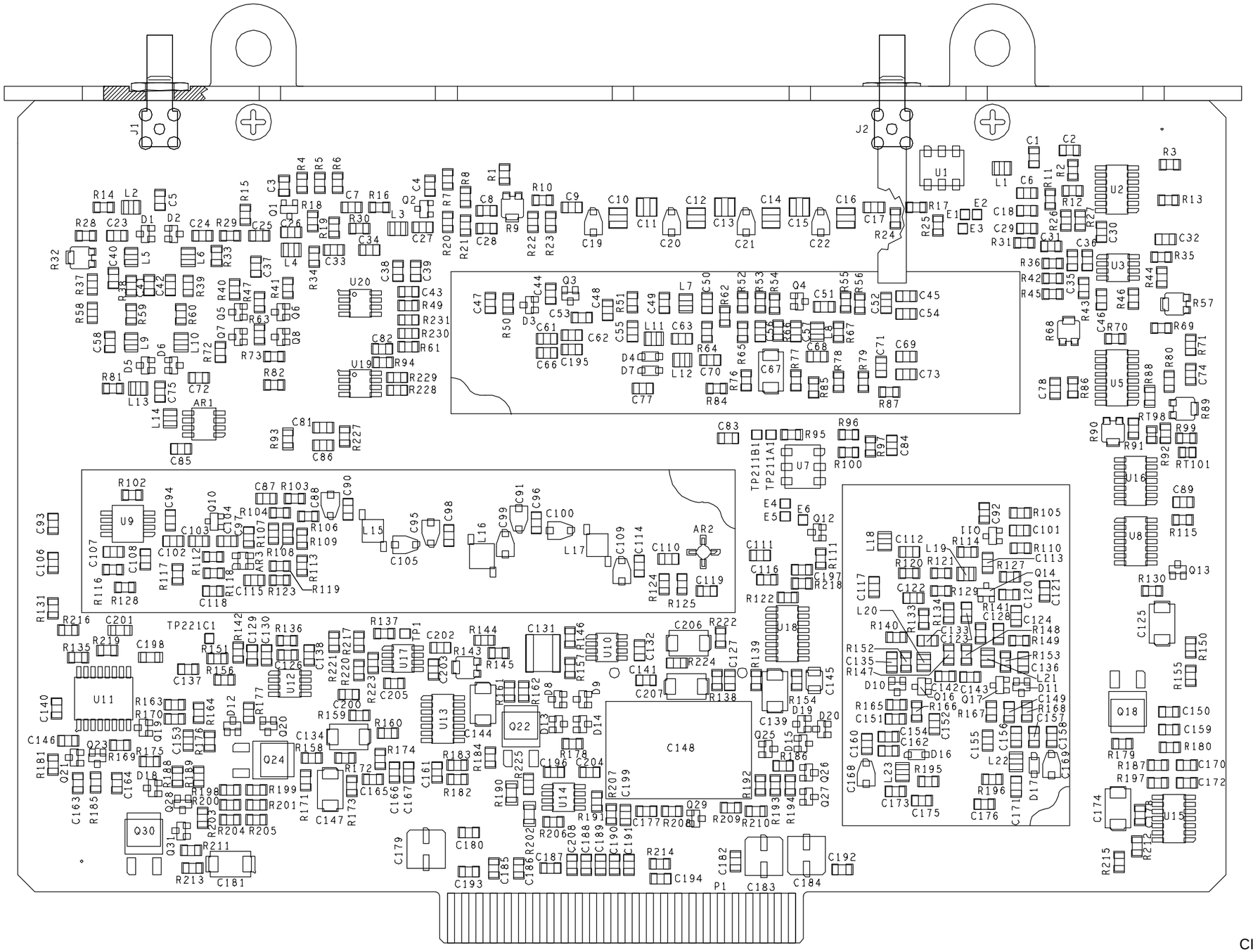


Fig. 9.5 High Tier Generator Module Block Diagram



CIRCUIT CARD ASSEMBLY
HIGH TIER GENERATOR

1-P30690C REV. B

SHEET 1 OF 1

DWG NO 63-P30692C SH 1

REVISION HISTORY				
REV	DESCRIPTION		DATE	APPROVED
-	INITIAL RELEASE			
A	SEE MCO C35978	VAH 94-07-20		A. KOESTNER
B	SEE CO E36125	FAD 95-02-21	95-04-10	A. KOESTNER
C	SEE CO L48777-3	LLB 01-01-08	01-02-01	A. GATTO
D	SEE CO L48824-1 R1	JFP 01-05-15	01-05-15	A. GATTO

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A5.
2. FOR REFERENCE DRAWINGS REFER TO:
   01-P30690C ASSEMBLY
   12-P30693C TEST PROCEDURE
3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL INDUCTANCE VALUES ARE IN *H.
   ALL VOLTAGES ARE IN DC.
4. TERMINATIONS CODED WITH THE SAME LETTERS OR NUMBERS ARE ELECTRICALLY CONNECTED.

5. DEVICE TYPE NUMBERS AND CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE 1. PORTIONS OF THE TYPE NUMBER MAY BE UNDERLINED AND USED AS A CODE TO IDENTIFY DEVICES ON DIAGRAM.

6. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH MANUFACTURER. ENGINEERING APPROVED EQUIVALENT DEVICE MAY BE USED.

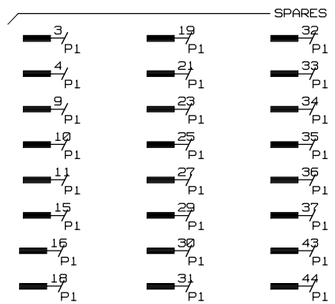
7. SELECT-IN-TEST COMPONENT.

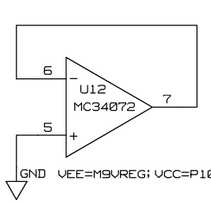
TABLE 1 (5)

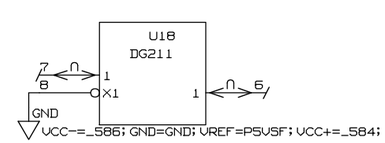
REF DES	DEVICE TYPE (6)	+5VSF	GND	+10VREG	-9VREG	+20VSF	FOUND ON SHEET	
U1	RMS-2						8	
U2	MC1496D				14		7	
U3	MC34072D			8	4		7	
U5	DG211CSE	12	5	13	4		7	
U7	RMS-2						6	
U8	74AC32	14	7				7	
U9	MB501LPF	2	5				3	
U10	OP-27GS				4	7	3	
U11	MC14158FN1	4	6				3	
U12	MC34072D			8	4		1,3	
U13	MC1723CD						2	
U14	LM317						2	
U15	MC1723CD						2	
U16	74AC86	14	7				1,7	
U17	OP-27GS				4	7	3	
U18	DG211CSE	12	5		4		1,3	
U19	10EL33						7	
U20	10EL33						7	
AR1	UPC1678G	8	2,3,6,7				4	
AR2	MAR-3		2,4				4	
AR3	UPC1675G	3	1				4	

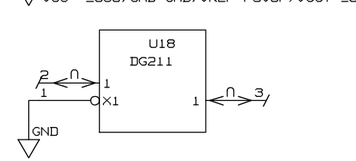
REFERENCE DESIGNATIONS	
HIGHEST NUMBER USED	NOT USED
AR3	
C208	C59, C60, C64, C65, C76, C79, C80, C208
D20	
E6	
J2	
L23	
P1	
Q31	Q9, Q15
R225	R48, R74, R75, R83, R98 R101, R126, R132, R226
RT101	RT1-RT97, RT99, RT100
U20	U4, U6

SPARES









ALL SHEETS ARE THE SAME REVISION STATUS

		CONTR
		ISS B35550-235-94-01-31
		APPROVALS
		DWN V. HARWOOD 94-01-28
		CHKR M. ONEY 94-01-31
		QA K. NELSON 94-01-31
		MATL W. MCDONALD 94-01-31
		MFG K. CHANEY 94-01-31
NEXT ASSY	USED ON	ENG M. ONEY 94-01-31
APPLICATION		CUST

MOTOROLA INC.
GOVERNMENT AND SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

TITLE
SCHEMATIC DIAGRAM
HIGH TIER GENERATOR

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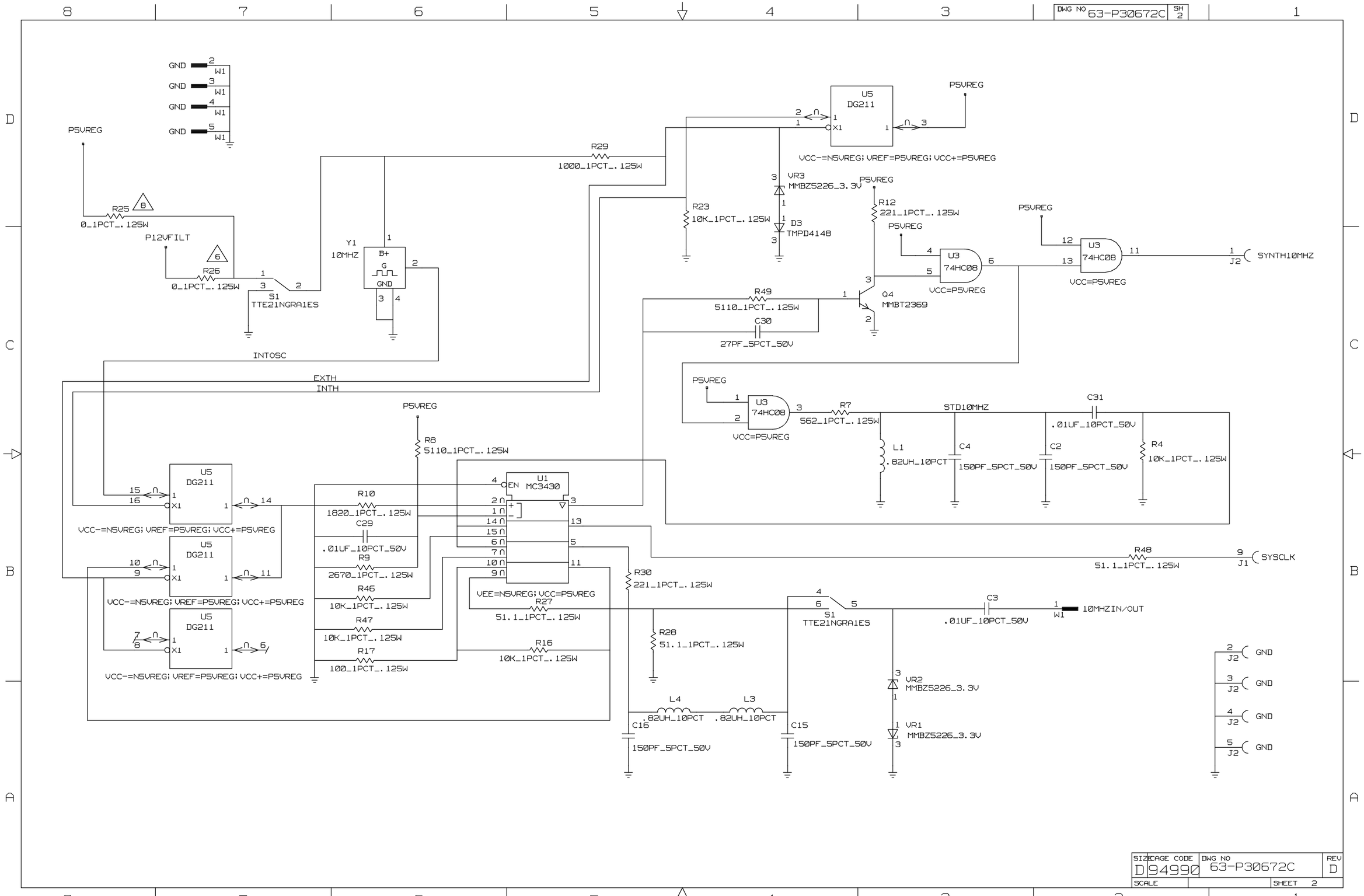
SCALE NONE		SHEET 1 OF 9



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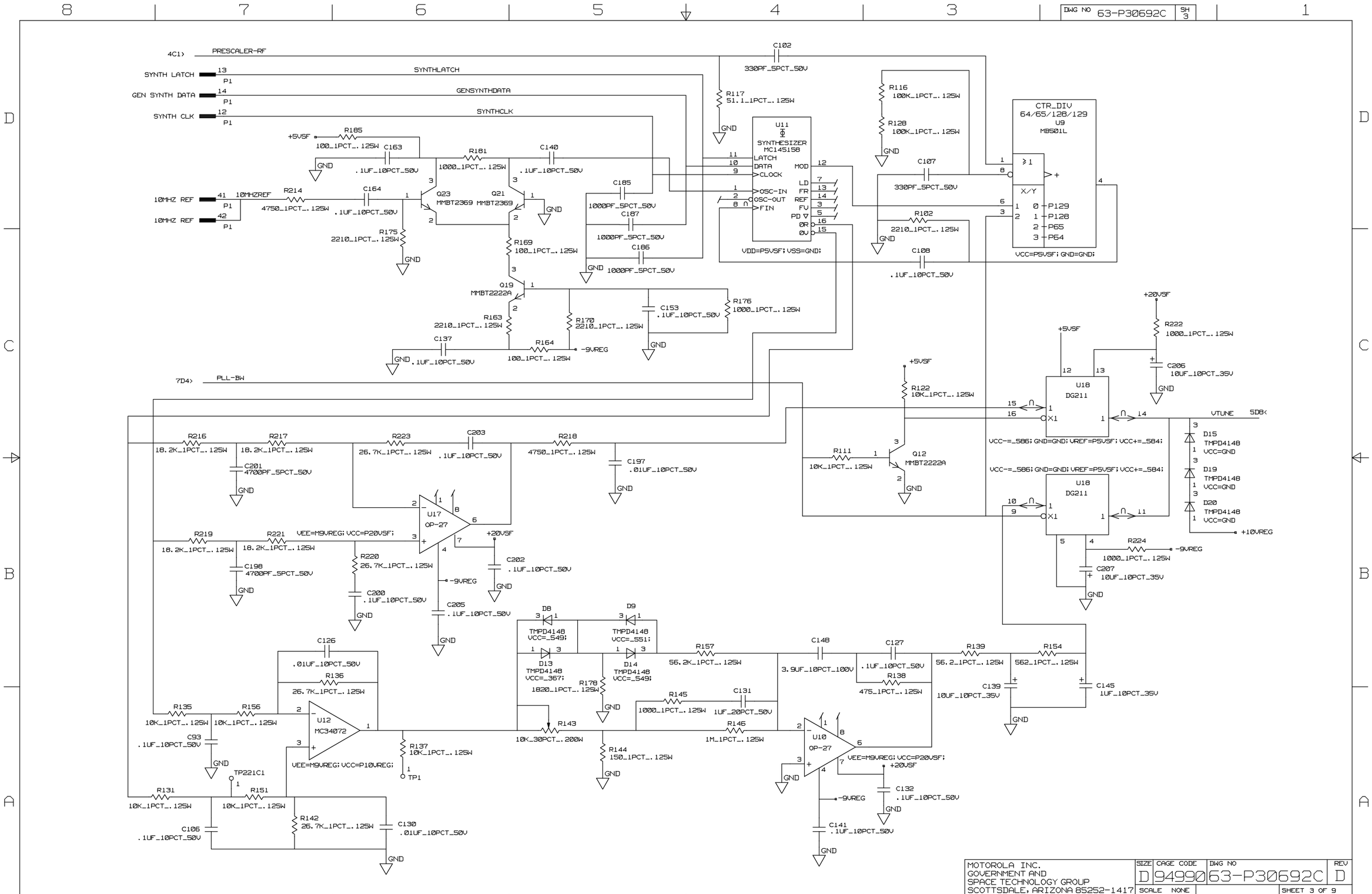
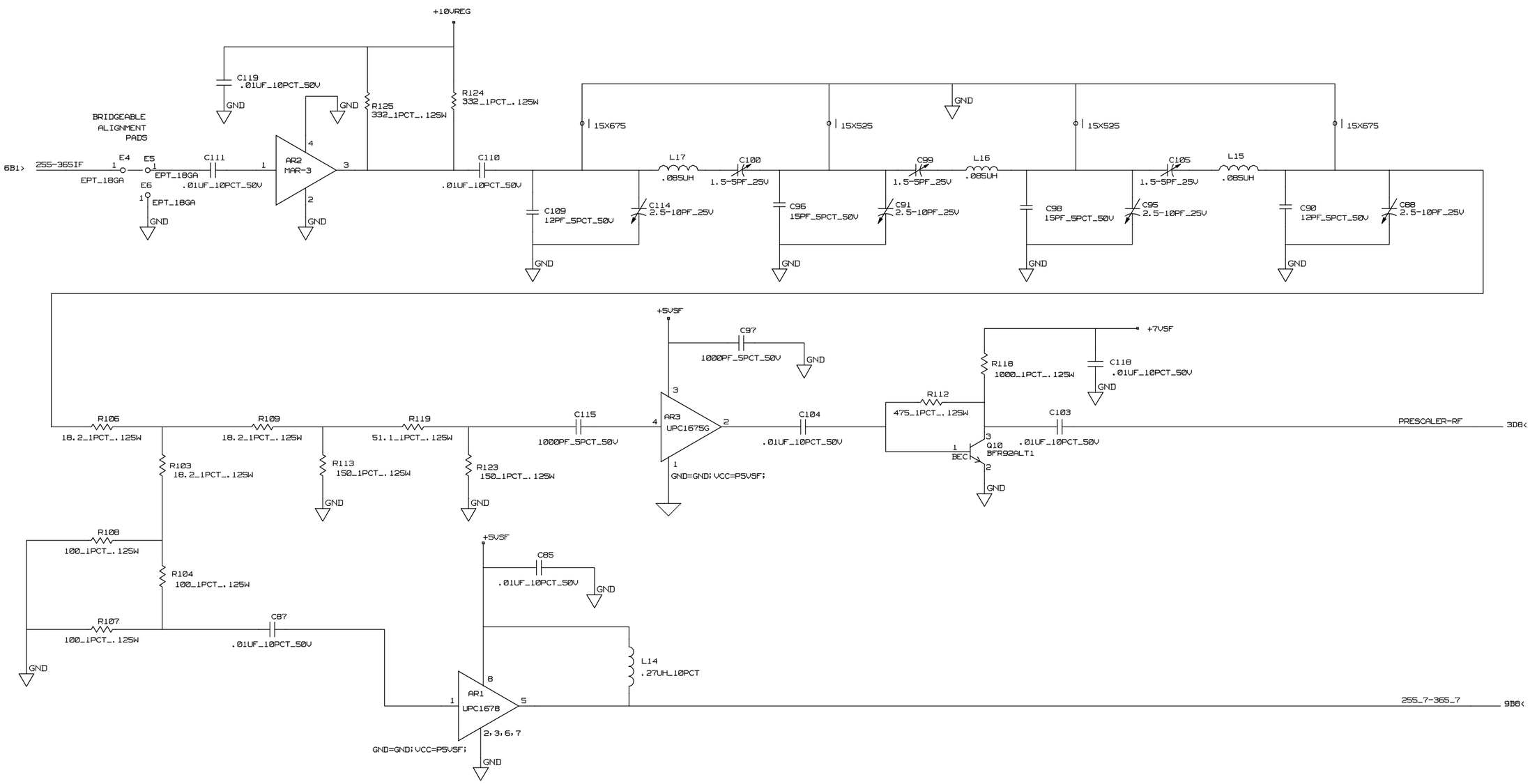
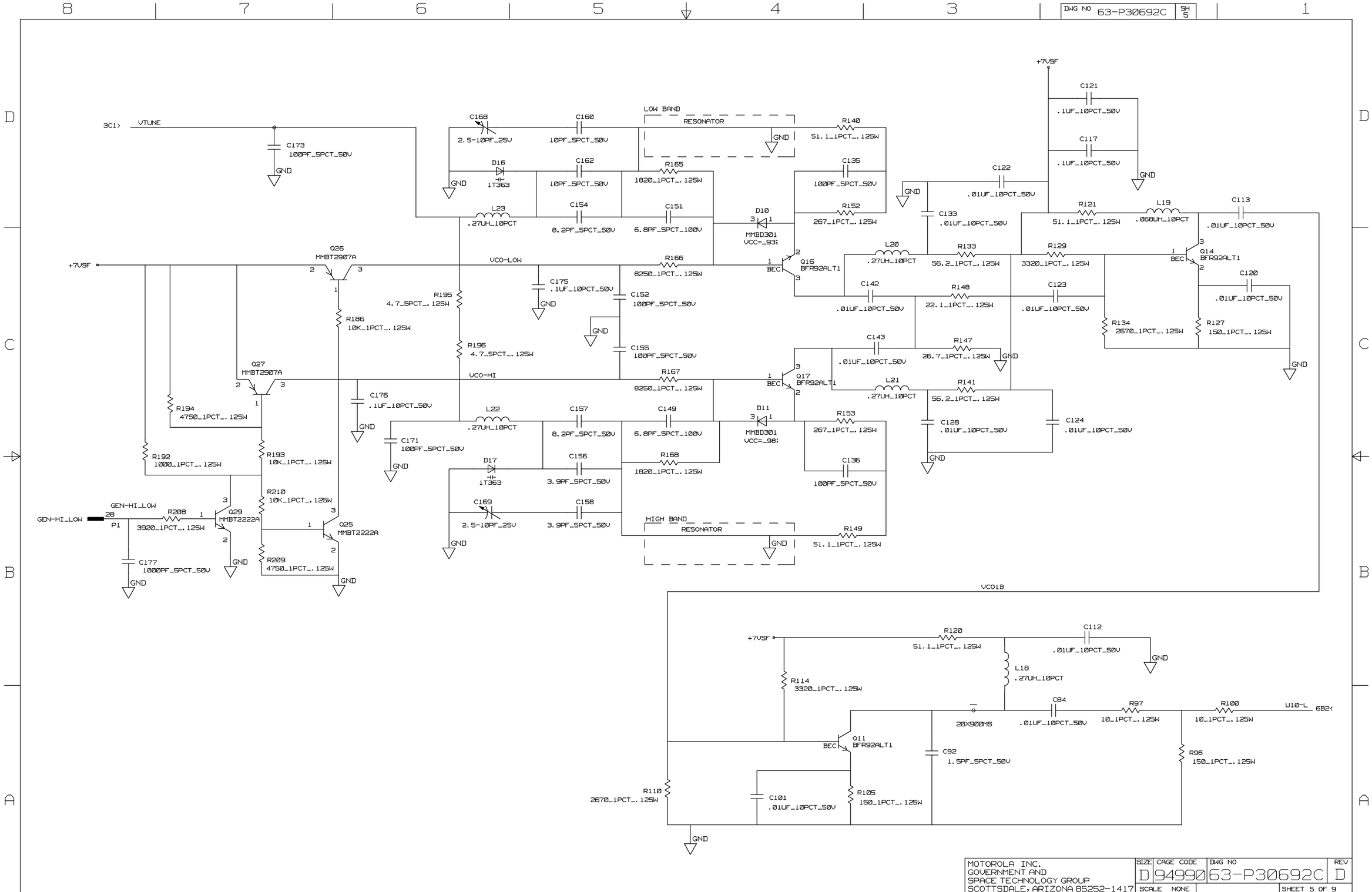

DWG NO 63-P30692C SH 3
4C1> PRESCALER-RF
SYNTH LATCH 13 P1 SYNTHLATCH
GEN SYNTH DATA 14 P1 GENSYNTHDATA
SYNTH CLK 12 P1 SYNTHCLK
10MHZ REF 41 P1 10MHZREF
10MHZ REF 42 P1
7D4> PLL-BW
C102 330PF_5PCT_50V
R117 51.1_1PCT_.125W
U11 SYNTHESIZER MC145158
LATCH DATA CLOCK OSC-IN OSC-OUT FIN MOD LD FR REF FV PD 0R 0V
VDD=P5VSF; VSS=GND;
R116 100K_1PCT_.125W
R128 100K_1PCT_.125W
C107 330PF_5PCT_50V
R102 2210_1PCT_.125W
C108 .1UF_10PCT_50V
CTR_DIV 64/65/128/129 U9 MB501L
X/Y P129 P128 P65 P64
VCC=P5VSF; GND=GND;
R185 100_1PCT_.125W
C163 .1UF_10PCT_50V
R181 1000_1PCT_.125W
C140 .1UF_10PCT_50V
C164 .1UF_10PCT_50V
R214 4750_1PCT_.125W
Q23 MMBT2369
Q21 MMBT2369
C185 1000PF_5PCT_50V
C187 1000PF_5PCT_50V
C186 1000PF_5PCT_50V
R175 2210_1PCT_.125W
R169 100_1PCT_.125W
Q19 MMBT2222A
R163 2210_1PCT_.125W
R170 2210_1PCT_.125W
C153 .1UF_10PCT_50V
R176 1000_1PCT_.125W
C137 .1UF_10PCT_50V
R164 100_1PCT_.125W
-9VREG
R122 10K_1PCT_.125W
Q12 MMBT2222A
R111 10K_1PCT_.125W
U18 DG211
VCC-=_586; GND=GND; VREF=P5VSF; VCC+=_584;
VTUNE 5D8<
R222 1000_1PCT_.125W
C206 10UF_10PCT_35V
D15 TMPD4148 VCC=GND
D19 TMPD4148 VCC=GND
D20 TMPD4148 VCC=GND
+10VREG
R224 1000_1PCT_.125W
C207 10UF_10PCT_35V
R216 18.2K_1PCT_.125W
R217 18.2K_1PCT_.125W
C201 4700PF_5PCT_50V
R223 26.7K_1PCT_.125W
C203 .1UF_10PCT_50V
R218 4750_1PCT_.125W
C197 .01UF_10PCT_50V
U17 OP-27
R219 18.2K_1PCT_.125W
R221 18.2K_1PCT_.125W
VEE=M9VREG; VCC=P20VSF;
C198 4700PF_5PCT_50V
R220 26.7K_1PCT_.125W
C200 .1UF_10PCT_50V
C205 .1UF_10PCT_50V
C202 .1UF_10PCT_50V
D8 TMPD4148 VCC=_549;
D9 TMPD4148 VCC=_551;
D13 TMPD4148 VCC=_367;
D14 TMPD4148 VCC=_549;
R178 1820_1PCT_.125W
R157 56.2K_1PCT_.125W
C148 3.9UF_10PCT_100V
C127 .1UF_10PCT_50V
R138 475_1PCT_.125W
R139 56.2_1PCT_.125W
R154 562_1PCT_.125W
C139 10UF_10PCT_35V
C145 1UF_10PCT_35V
C126 .01UF_10PCT_50V
R136 26.7K_1PCT_.125W
R135 10K_1PCT_.125W
R156 10K_1PCT_.125W
U12 MC34072
VEE=M9VREG; VCC=P10VREG;
C93 .1UF_10PCT_50V
R137 10K_1PCT_.125W
TP1
TP221C1
R143 10K_30PCT_.200W
R145 1000_1PCT_.125W
C131 1UF_20PCT_50V
R146 1M_1PCT_.125W
R144 150_1PCT_.125W
U10 OP-27
VEE=M9VREG; VCC=P20VSF;
C132 .1UF_10PCT_50V
C141 .1UF_10PCT_50V
R131 10K_1PCT_.125W
R151 10K_1PCT_.125W
C106 .1UF_10PCT_50V
R142 26.7K_1PCT_.125W
C130 .01UF_10PCT_50V
GND
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D CAGE CODE 94990 DWG NO 63-P30692C REV D
SCALE NONE
SHEET 3 OF 9



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30692C	REV D
	SCALE NONE			SHEET 4 OF 9



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE	CAGE CODE	DWG NO	REV
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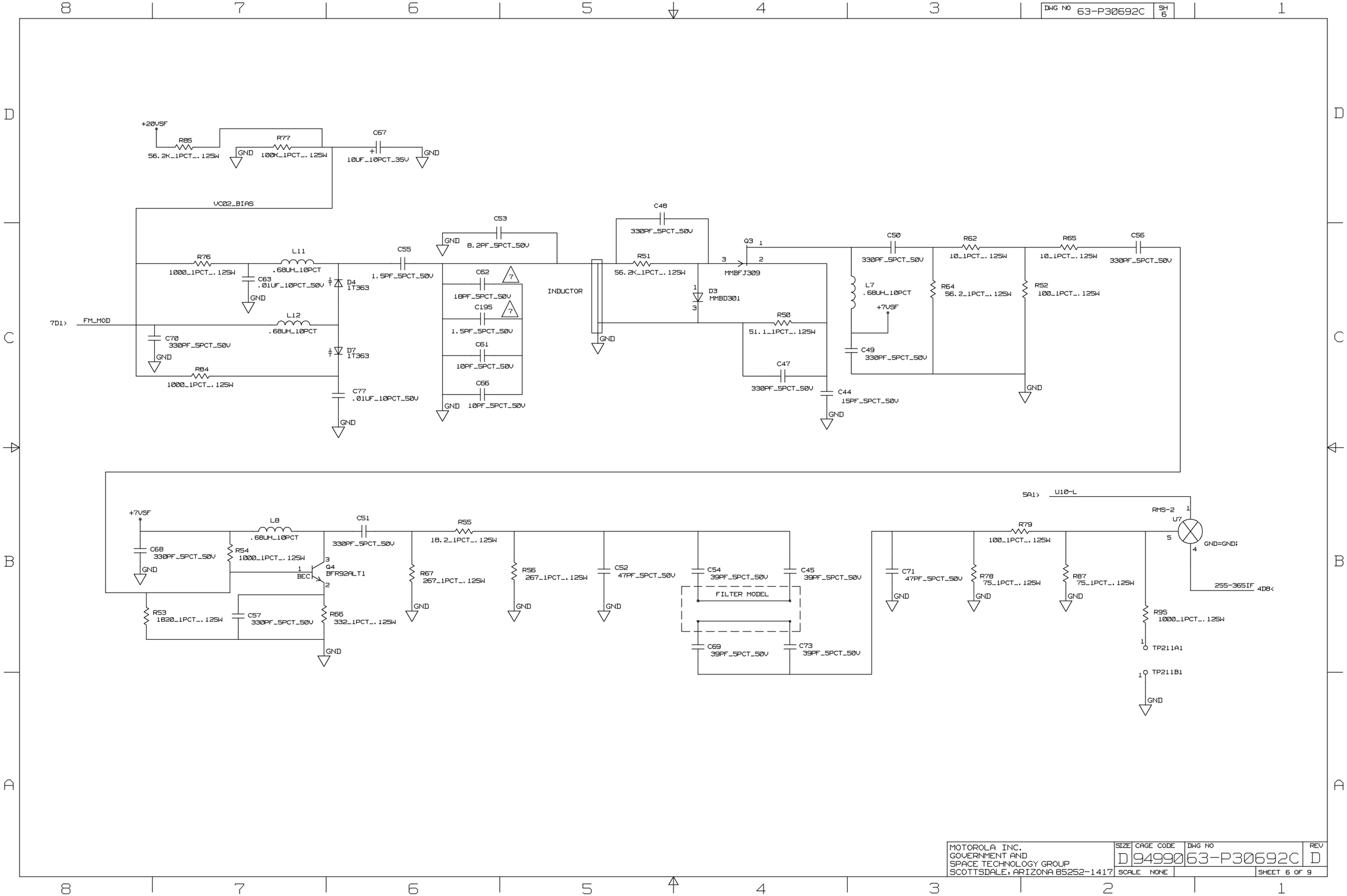
	SCALE NONE		SHEET 5 OF 9	



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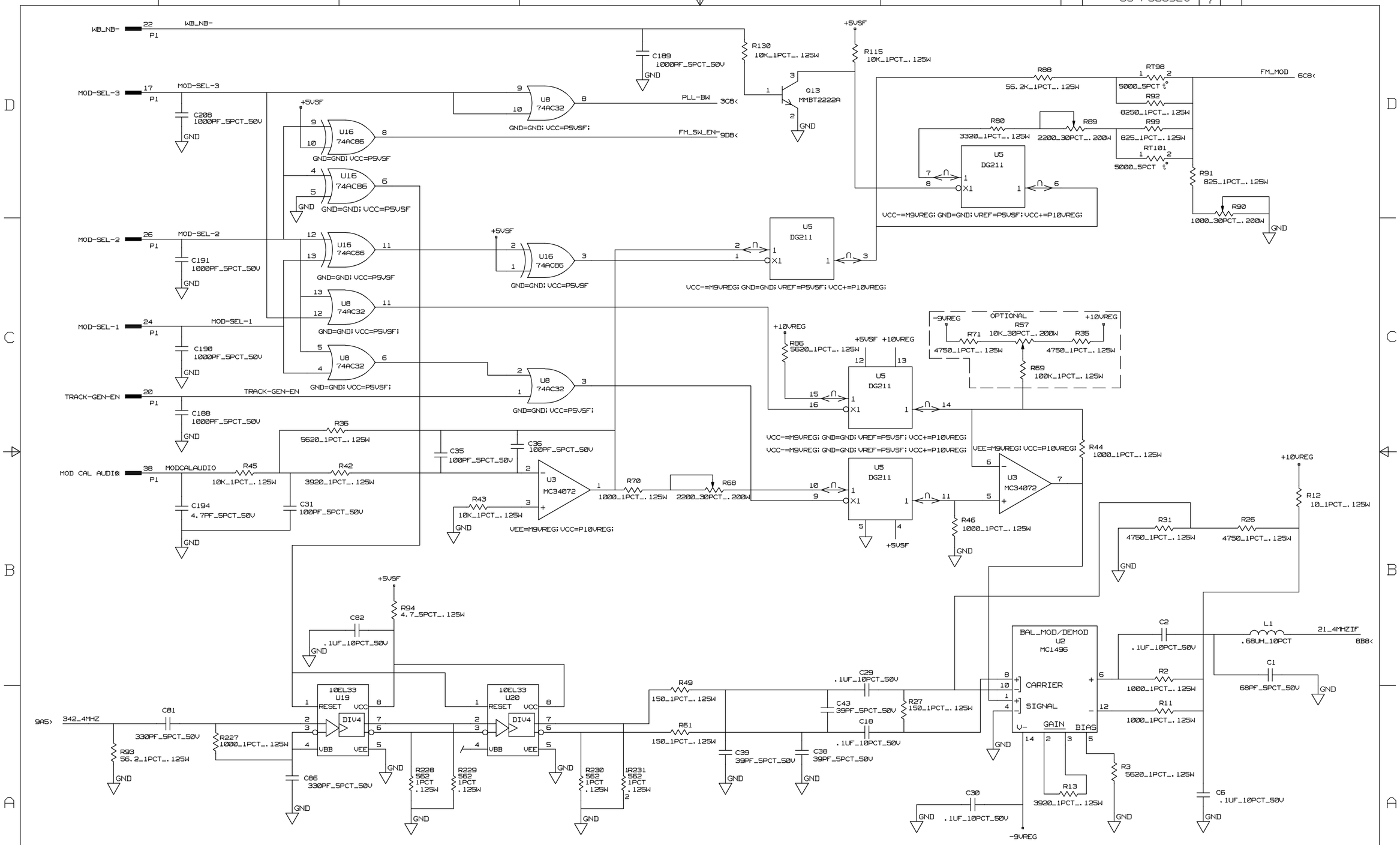
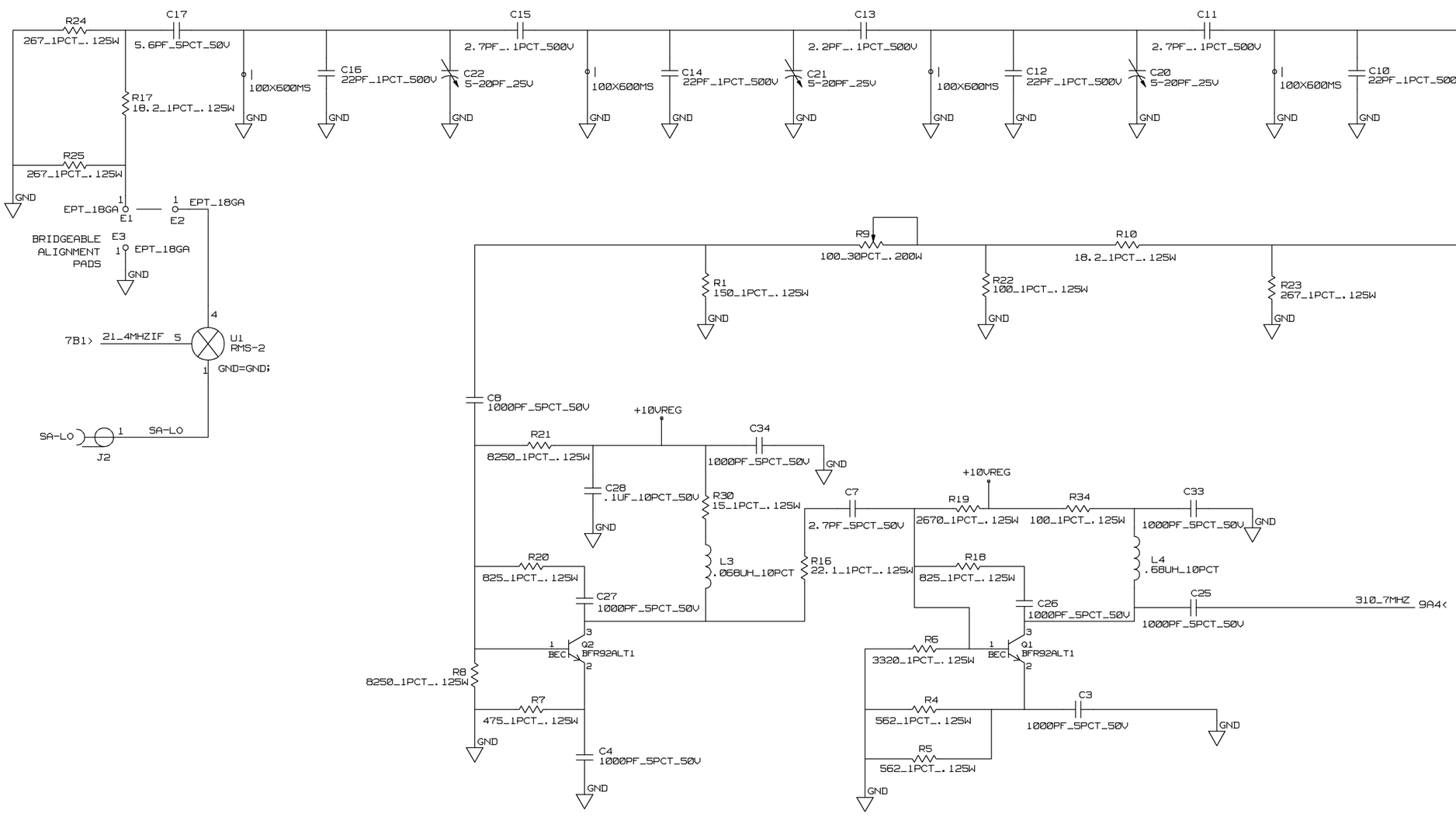
	SCALE NONE			SHEET 6 OF 9


DWG NO 63-P30692C SH 7
WB_NB-
MOD-SEL-3
MOD-SEL-2
MOD-SEL-1
TRACK-GEN-EN
MOD CAL AUDIO
PLL-BW
FM_SW_EN-
FM_MOD
21_4MHZIF
342_4MHZ
U8 74AC32
U16 74AC86
U5 DG211
U3 MC34072
Q13 MMBT2222A
U19 10EL33
U20 10EL33
BAL_MOD/DEMOD U2 MC1496
CARRIER
SIGNAL
GAIN
BIAS
OPTIONAL
GND=GND; VCC=P5VSF;
VCC-=M9VREG; GND=GND; VREF=P5VSF; VCC+=P10VREG;
VEE=M9VREG; VCC=P10VREG;
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D CAGE CODE 94990 DWG NO 63-P30692C REV D
SCALE NONE
SHEET 7 OF 9



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE	CAGE CODE	DWG NO	REV
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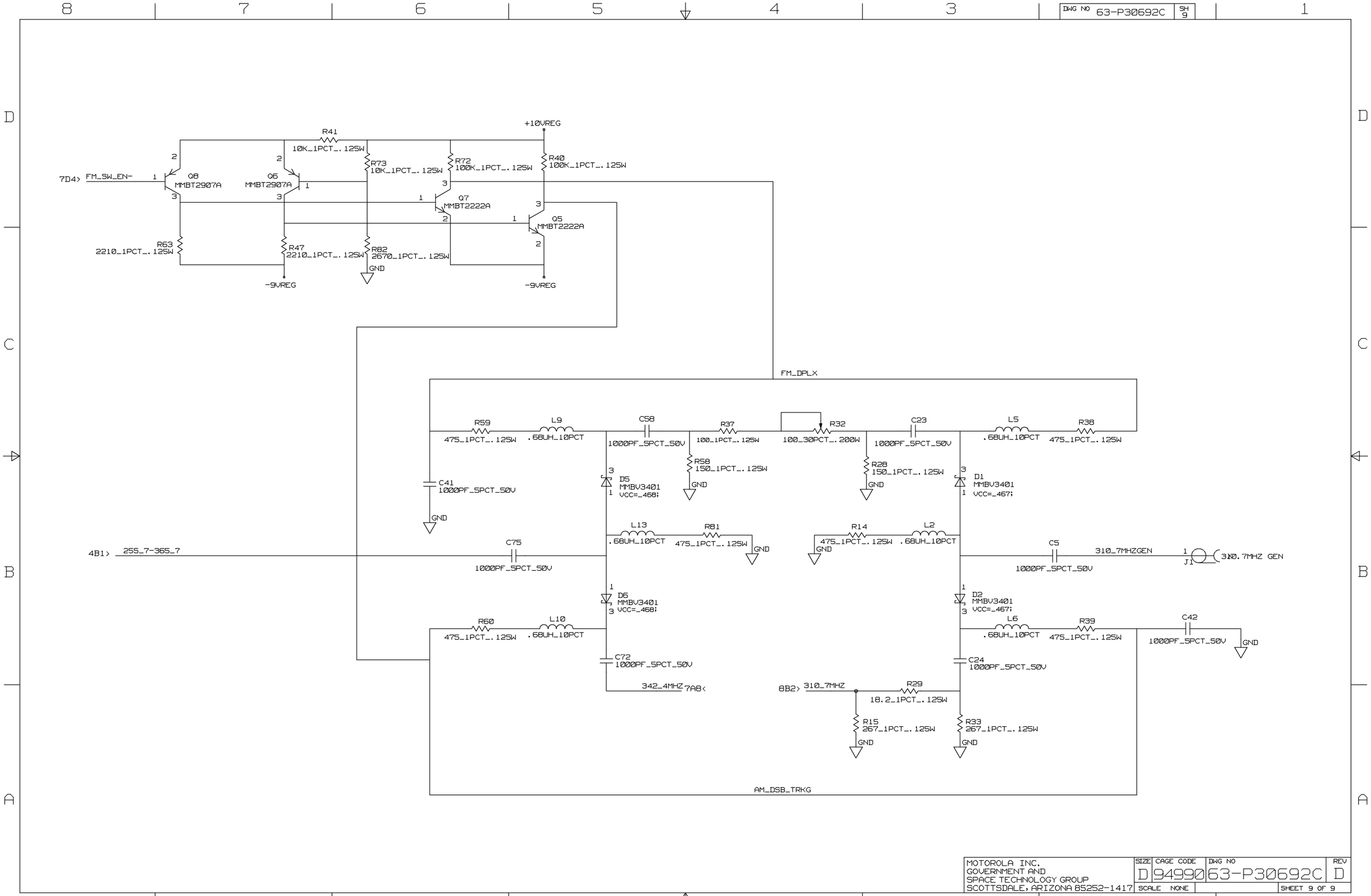
	SCALE NONE		SHEET 8 OF 9	



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30692C	REV D
	SCALE NONE		SHEET 9 OF 9	

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Go to Section 11

10.1 GENERAL DESCRIPTION

The RF Input Module (A8) is installed in the RF cardcage in the fourth slot from the center of the Analyzer.

The primary function of the RF Input module is to perform a dual frequency translation on the front panel antenna input. The first Conversion translates the 0.4 to 999.9999MHz input Signal to 1700.7001-1710.7MHz. The second conversion translates this signal to 310.7MHz. There are two outputs at 310.7MHz, one for the receiver and one for the spectrum analyzer.

WARNING

The Antenna Port is intended for monitoring low level RF signals ***up to 0 dBm ONLY****. DO NOT use the Antenna Port to measure signals. Instead, switch to the RF I/O Port. Refer to Section 12 of this manual (RF Wattmeter) for input level limits at the RF I/O Port.*

10.2 SIGNALS SUMMARY

10.2A Signal Descriptions

*CAL RF ENABLE** input data line enables either the *CAL RF* path or the ANT path.

CAL RF input is for either receiving RF externally from the RF I/O Port or internally while calibrating the Generator Output.

FP ANTENNA is the input from the front panel Antenna Port.

INPUT ATTEN 1 INPUT ATTEN 2** inputs enable the 20 dB attenuators 1 & 2 on this module.

SYNTH 10 MHz Ref input signal from the Frequency Standard Module provides a 10MHz reference.

1st RCV LO input from the High Synthesizer Module is used to up-convert the received signal from the front panel to the 1700.7001-1710.7MHz 1st IF.

310.7MHz IF output is the product of the received signal being up-converted to 1700.7001-1710.7MHz and then down-converted to 310.7MHz.

1400 MHz RCV LO input from the High Synthesizer Module is a local oscillator used to down-convert the 1700.7001-1710.7MHz IF to a 310.7MHz IF.

+5V, -5V, +12V and *-12V* supply power to the module.

10.2B Connector Descriptions

P1 (50 Pin Edge Connector to RF Motherboard)

pin	
1,2	GND
3,4	+5V
5,6	-5V
7,8	not used by this module
9	READ SPARE 1 ●
10	RF ATTEN SPARE 1 ●
11	READ SPARE 2 ●
12	INPUT ATTEN 2*
13	INPUT ATTEN 1 ●
14	RF ATTEN SPARE 2●
15	not used by this module
16	CAL RF ENABLE*
17-38	not used by this module
39,40	GND
41-44	not used by this module
45,46	-12V
47,48	+12V
49,50	GND

- Signal is a spare in the basic Analyzer, but may be utilized in conjunction with future product development.

SMB Connectors

J1 FRONT PANEL ANTENNA
Input freq: 400KHz to 999.9999MHz
Input level: -101dBm to 0dBm
Input impedance: 50Ω nominal
VSWR: 2:1 maximum

J2 CAL RF
Input freq: 400KHz to 999.9999MHz
Input level: -76dBm to 0dBm
Input impedance: 50Ω nominal
VSWR: 2:1

J3 1st RCV LO
Input freq: 1710MHz to 2710MHz
Input resolution: 10MHz

Input level: 0dBm ±3dB
Input impedance: 50Ω nominal
VSWR: 2:1 maximum
Incidental AM: <3.0% (300Hz to 3KHz BW)
Spurious suppression: >40dBc
Ref spurious suppression: >60dBc

J4 1400MHz RCV LO
Input freq: 1390.0001-1400MHz in 100Hz steps
Input level: +2dBm ±2.5dB
Input impedance: 50Ω nominal
VSWR: 2:1 maximum
Incidental AM: <3.0% (300Hz to 3KHz BW)
Spurious suppression: >40dBc
Ref spurious suppression: >60dBc

J5 310.7MHz RCV IF
Center freq: 310.7MHz
Output impedance: 50Ω nominal
VSWR: 2:1

J6 310.7MHz SA IF
Center freq: 310.7MHz
Output impedance: 50Ω nominal
VSWR: 2:1

10.3 BLOCK DIAGRAM DESCRIPTION

This module amplifies and filters signals present at the Antenna port then up-converts this signal to a 1700.7001-1710.7MHz IF. The IF is then down converted to a 310.7MHz IF for the Spectrum Analyzer and monitor functions. The level of the 310.7MHz IF is controlled by switching fixed attenuators as required.

The module provides coarse attenuation in 20dB steps to the input signal for a maximum value of 40dB. The module has a CAL RF input, which is used to calibrate the response of the RF input path over the range of input frequencies and temperature. The CAL RF path is also used to feed the RF I/O input to the Spectrum Analyzer and Receiver.

10.4 DETAILED DESCRIPTION

10.4.1 Frequency Conversion

Refer to figure 10.4.1 for the following description.

The first frequency mix in this module takes the wide band input from the front panel antenna port (400KHz to 999.9999MHz) and converts it to 1700.7001-1710.7MHz (via mixer U10). The conversion is accomplished using the 1st RCV LO signal (1710MHz to 2710MHz in 10MHz steps) provided by the High Synthesizer Module. The result of this mix is an IF in the range of 1700.7001 to 1710.7MHz.

The second mixer (U7) translates the 1700.7001-1710.7MHz signal to 310.7 MHz using the 1400 MHz RCV LO signal (1390.0001-1400MHz) which also originates from the High Synthesizer Module This is the final conversion and the 310.7MHz signal is then output to the Receiver and Spectrum Analyzer modules.

10.4.2 RF Attenuation

Two switchable 20dB attenuators are used in this module to extend the range of the receiver. The attenuators are located in the wideband input of the module They are switched in using RF switches which are controlled by the digital input lines INPUT ATTEN1 and INPUT ATTEN2.

INPUT ATTEN1 controls K2 and K3 to direct the input signal to a 20dB pad consisting of R30, R33, and R44. INPUT ATTEN2 controls K4 and K5 to switch in 20dB attenuation from R70, R73, and R80.

The final attenuator in the module is factory adjusted (via selection of resistor values) with a range of -2dB to -25dB and is located in the 310.7MHz RF path of the module. Its purpose is to compensate for variances in all components in the RF path of the module and set the conversion gain to a specific value.

10.4.3 Gain Stages

10.4.3.1 RF Path

Eight separate amplifiers are employed in the RF path.

The first two amplifiers are in the wide band RF input of the module (AR4, AR6). Each amplifier produces a nominal +11dB gain.

The next two amplifiers (AR1, AR5) are used at 1710.7MHz and provide +9dB gain each.

The final four amplifiers are located in the 310.7MHz portion of the RF path (Q15, Q12, Q6, Q7). These amplifiers are identical and each has +12dB gain.

10.4.3.2 Other Paths

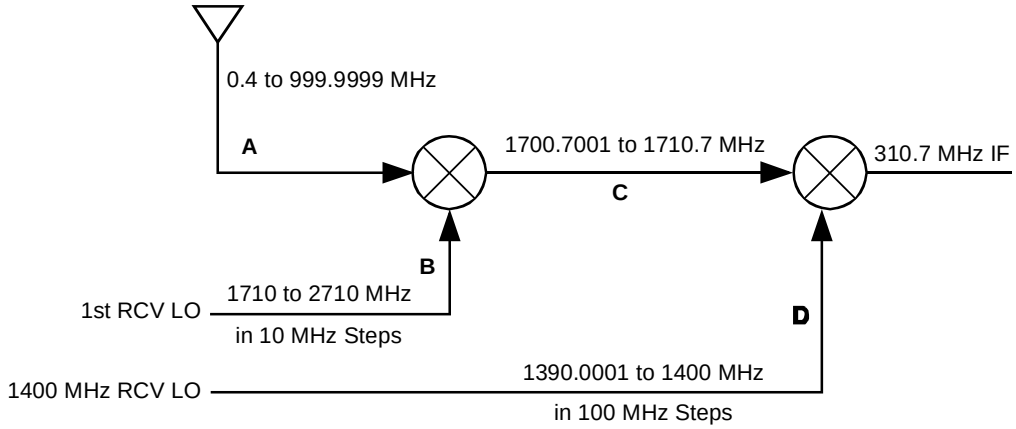
The 1st RCV LO signal (1710-2710MHz) is amplified to +7dBm by AR1 and AR5. The 1400MHz RCV LO signal (1390.0001 to 1400MHz) is amplified to +7dBm by AR2.

10.4.4 Filtering

The first filter in the module (W2-W6, C61, C69, C81) is the 1300MHz lowpass which acts like a preselector by only allowing signals in the range of 400KHz to 1000MHz to pass unattenuated.

The second filter FL1 is placed in the 1700.7001-1710.7MHz IF path. This is a bandpass filter with a center frequency of 1710.7MHz and a 3dB bandwidth of 50MHz. Its primary purpose is to reject the unwanted image frequency resulting from the first mix.

The final filter is placed after the 1710.7MHz conversion. This is a 310.7MHz bandpass filter with a 3dB bandwidth of 15MHz. It rejects the unwanted image resulting from the 310.7MHz frequency conversion. It also sets the initial bandwidth of the receiver IF to 15MHz. The filter response is adjustable with trimcaps C88, C72, C65, and C59.



1st RCV LO and 1400 MHz LO from the High Synthesizer Module's PLL loops are programmed by the system Processor so the final mix at the RF Input Module always results in a 310.7 MHz IF.

A = Carrier Frequency B = Wideband PLL (from HI SYNTH) C = B - A

<u>To calculate B and D for any carrier frequency:</u>
1. Carrier Freq + 0.7 = XXY.YYYY
2. B = XX0.0 + 1710
3. D = 1400 -Y.YYYY

EXAMPLES (referenced to A, B, C, and D, on diagram above) (all values are in MHz):

Carrier (A)	B	C (B - A)	D (C - 310.7)	310.7 MHz (C - D)
459.2999	2160	1700.7001	1390.0001	1700.7001 - 1390.0001
459.3	2170	1710.7	1400	1710.7 - 1400
890.1234	2600	1709.8766	1399.1766	1709.8766 - 1399.1766
123.65	1830	1706.35	1395.65	1706.35 - 1395.65
0.4	1710	1709.6	1398.9	1709.6 - 1398.9
457.325	2160	1702.675	1391.975	1702.675 - 1391.975

RF Input Req Block

Fig. 10.4.1 RF Input Frequency Conversion

10.4.5 Calibration

A CAL RF input is provided which is selectable using the digital control line CAL RF EN (NOTE. CAL RF EN is documented as CAL RF/(ANT)* at the Interface Module).

The CAL RF input port is switched during the Analyzer's system CAL function to allow an input signal to be injected internally from the RF Wattmeter Module. This input level is reduced in precise steps so the log amplifier in the Receiver Module can be accurately calibrated over its entire range.

10.5 BLOCK DIAGRAM

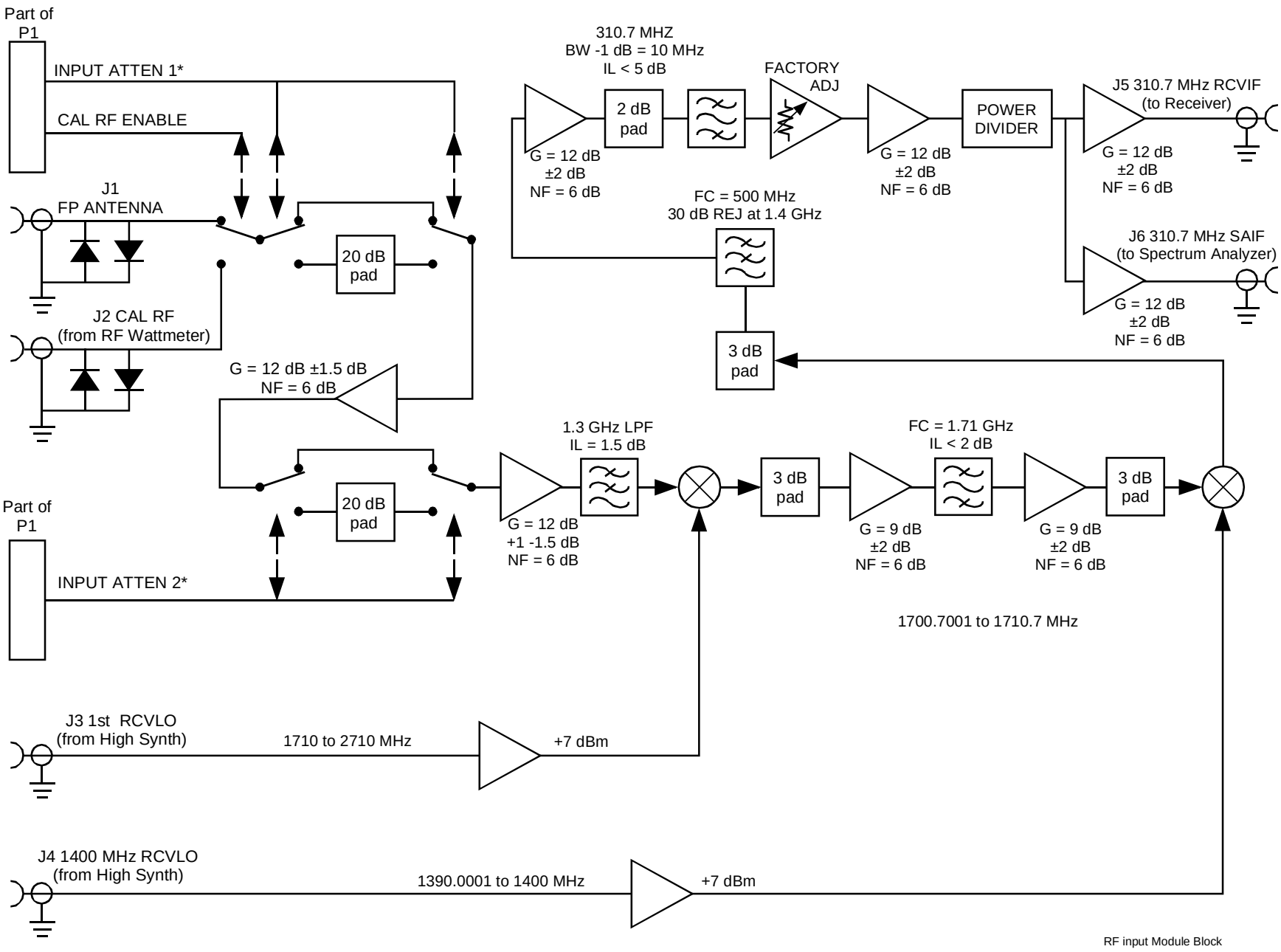
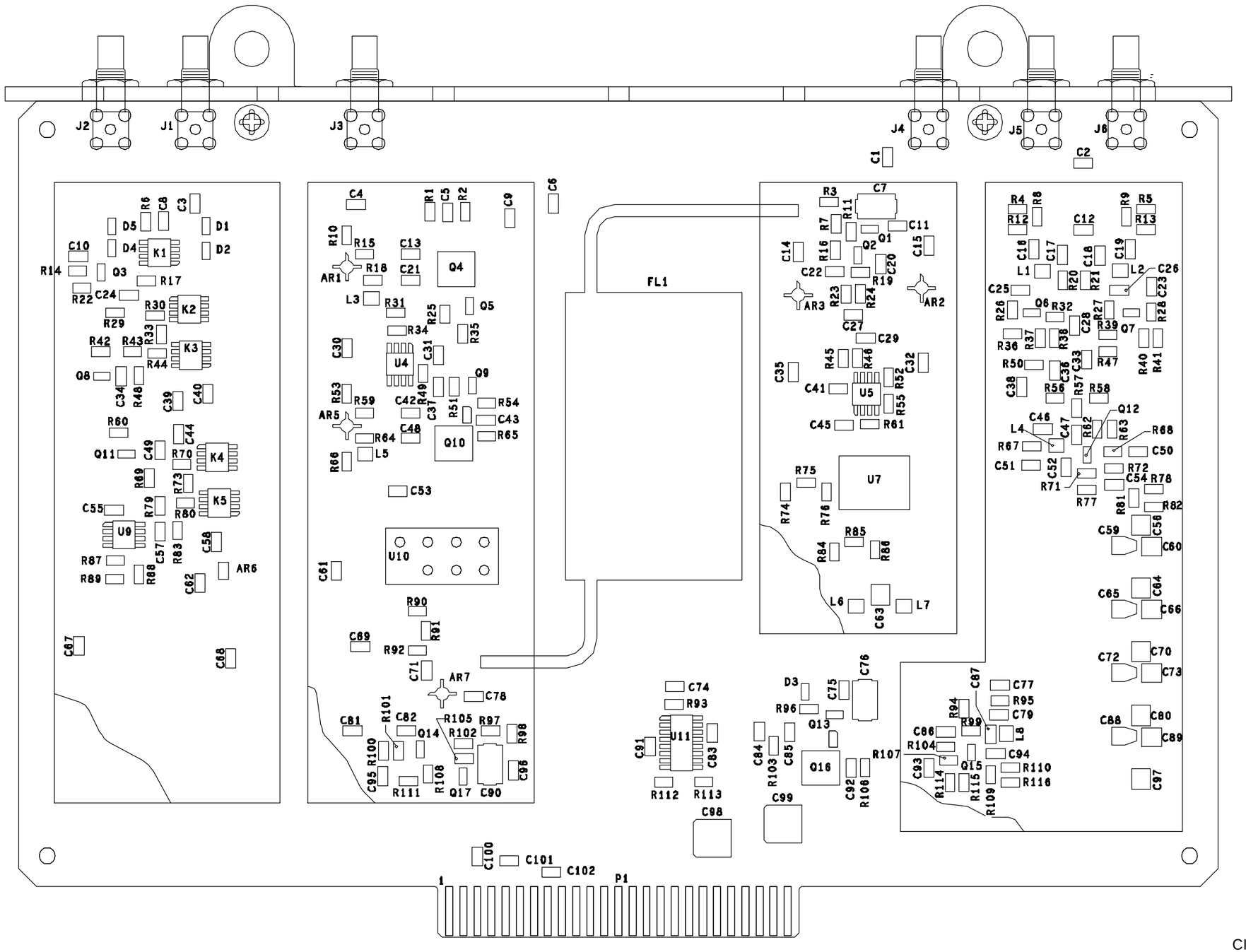


Fig. 10.5 RF Input Module Block Diagram



CIRCUIT CARD ASSEMBLY
RF INPUT

01-P30320C REV. D

SHEET 1 OF 1

DWG NO 63-P30322C SH 1

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1AB.
2. FOR REFERENCE DRAWINGS REFER TO:
   01-P30320C ASSEMBLY
   12-P30323C TEST PROCEDURE
3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL VOLTAGES ARE IN DC.
4. TERMINATIONS CODED WITH THE SAME LETTERS OR NUMBERS ARE ELECTRICALLY CONNECTED.

5 DEVICE TYPE NUMBERS AND CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE 1. PORTIONS OF THE TYPE NUMBER MAY BE UNDERLINED AND USED AS A CODE TO IDENTIFY DEVICES ON DIAGRAM.

6 DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH MANUFACTURER. ENGINEERING APPROVED EQUIVALENT DEVICE MAY BE USED.

7 SELECT IN TEST VALUE. SEE TABLE 2 ON SHEET 4.

TABLE 1 (5)

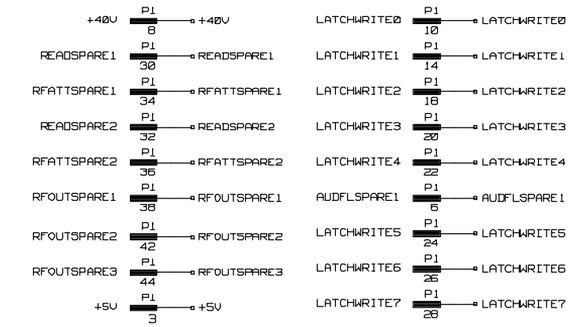
REF DES	DEVICE TYPE (6)	+5	GND	+12V	-12V
U1				1	
U2					
U3					
U4	LM317				
U5	LM317				
U6					
U7	SMDC3		4,5		
U8					
U9	LM317				
U10	MLP-B77S		2,5,6,7		
U11	DG211	12		13	4

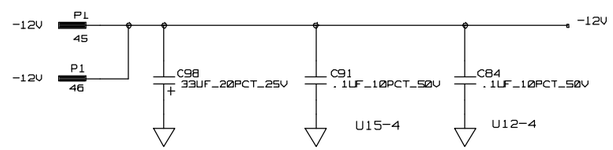
REFERENCE DESIGNATIONS

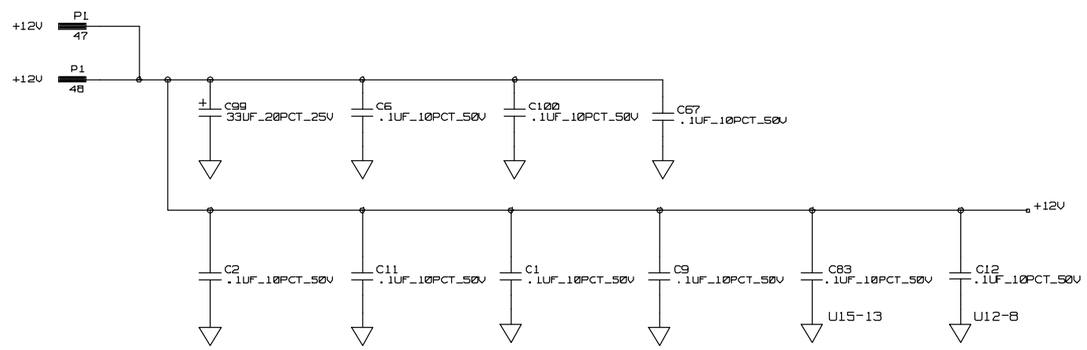
HIGHEST NUMBER USED	NOT USED
AR7	AR4
C102	
D5	
FL1	
J6	
K5	
L8	
P1	
Q17	
R116	
U11	U1,U2,U3,U6,U8

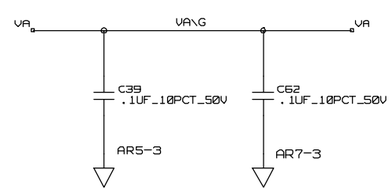
STRIPLINES

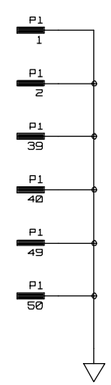
LENGTH	WIDTH	REFERENCE DESIGNATIONS
.600	.015	W1,W3,W7
.490	.015	W2
.385	.015	W4
.120	.015	W5
.050	.015	W6
.750	.015	W8











REVISION HISTORY

REV	DESCRIPTION	DATE	APPROVED
	CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY		
B	INITIAL RELEASE & RENUMBER B.B.	90-2-15	
C	SEE MCO B35653 90-07-31 R.D.S.	90-8-9	D.DUNCAN
D	SEE CO C35809-1 92-05-29 ORF	92-5-29	P.AMMON
E	CBDS CONVERSION CO E36163-3 JFP 95-08-07	95-08-07	KOESTNER

ALL SHEETS ARE THE SAME REVISION STATUS

		CONTR
		ISS B35550-53B_90/04/17
		APPROVALS
		DWN S.MEELHUYSEN 89-03-27
		CHKR
		QA K.NELSON_90/04/17
		MATL
01-P30320C	COCHISE	MFG JOHN DECAMP_90/04/12
NEXT ASSY	USED ON	ENG D.ZELINKA_90/04/11
APPLICATION		CUST

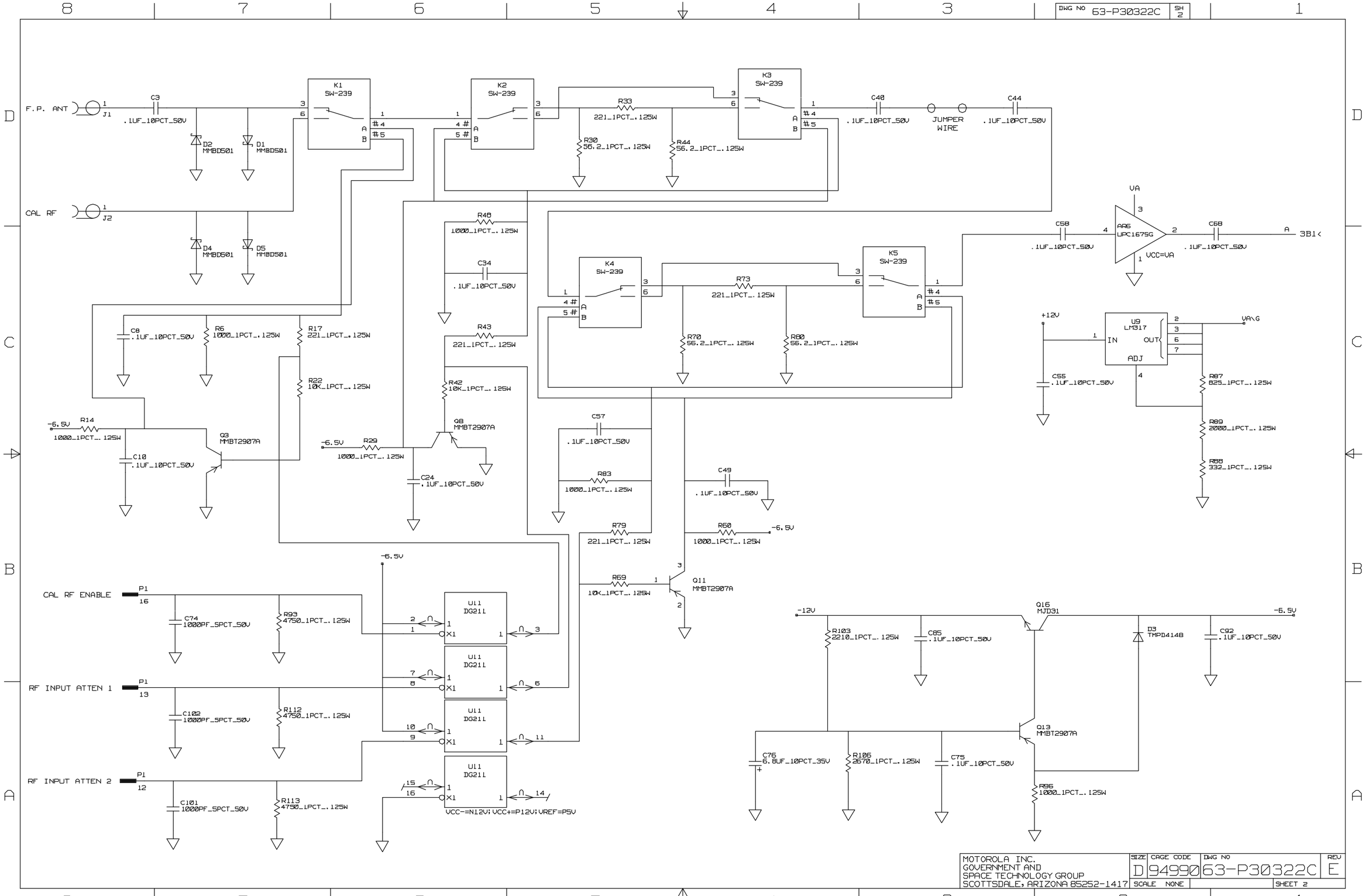
MOTOROLA INC.
GOVERNMENT AND SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

TITLE

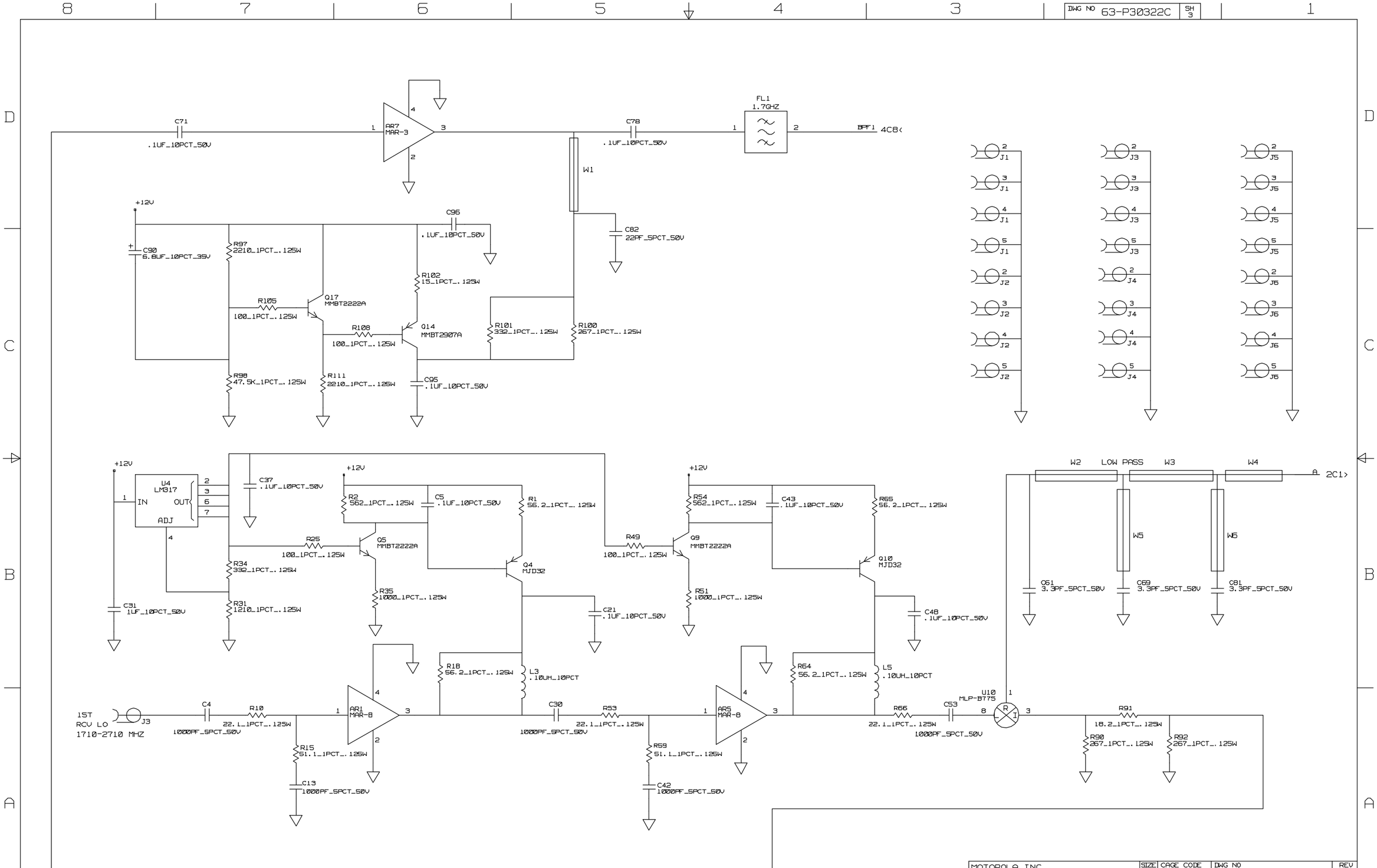
RF INPUT SCHEMATIC DIAGRAM

SIZE	CAGE CODE	DWG NO
D	94990	63-P30322C

SCALE NONE SHEET 1 OF 5



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D / CAGE CODE 94990	DWG NO 63-P30322C	REV E
	SCALE NONE		SHEET 2



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	SCALE NONE		SHEET 3	

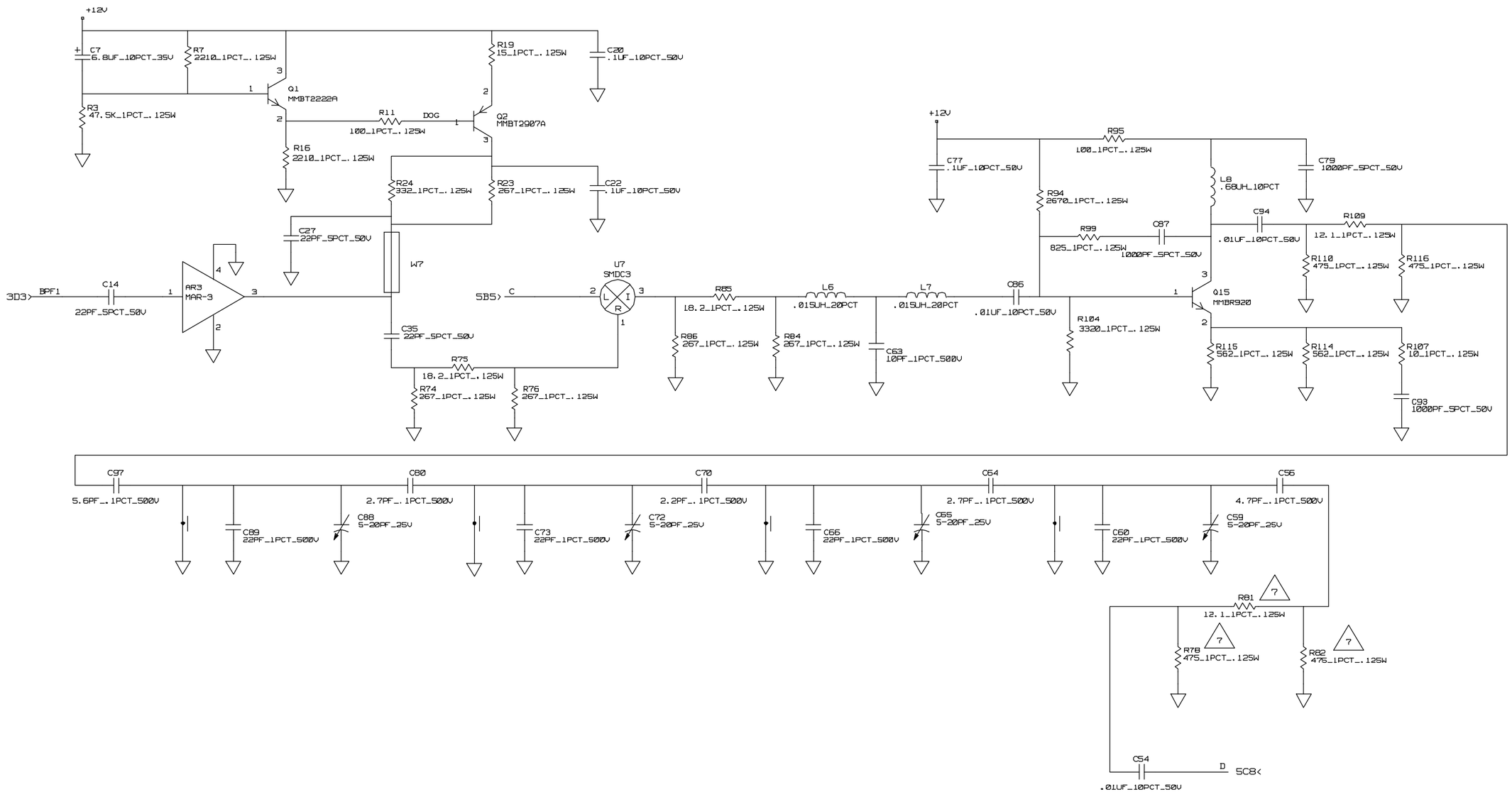
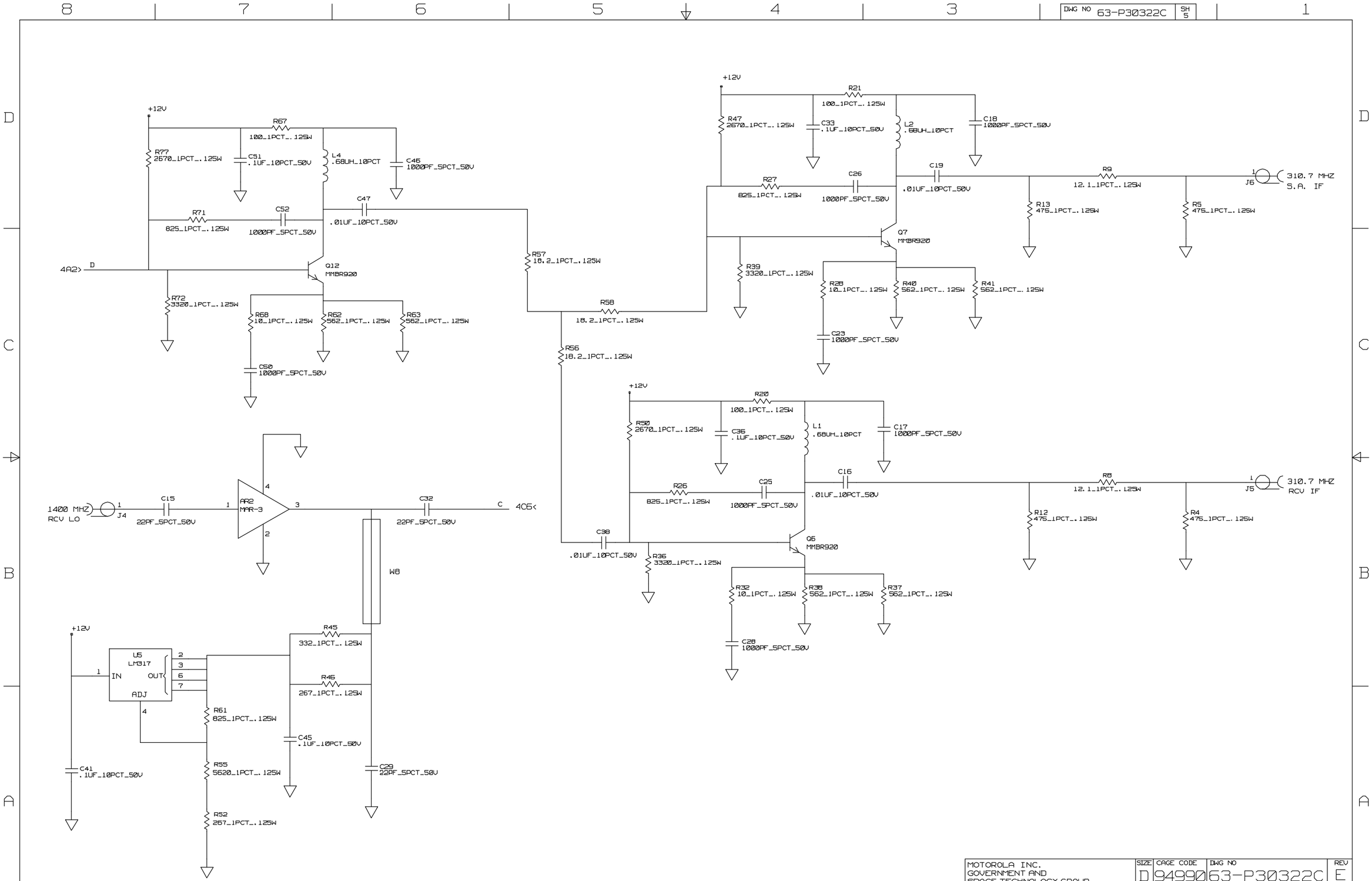


TABLE 2

ATTEN. (DB)	3	4	5	6
RB1	18.2	26.7	33.2	39.2
R78, R82	267	221	182	150



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30322C	REV E
	SCALE NONE		SHEET 5	

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11.1 GENERAL DESCRIPTION

The RF Output Module (A6) is installed in the RF cardcage in the second slot from the center of the Analyzer.

The primary function of the RF Output Module is to provide two frequency translations to the 310.7MHz GEN IF input signal. The module also provides image filtering, spurious signal suppression, switchable 20dB attenuators, and continuously adjustable RF attenuation. The RF output from the module is in the range of 400KHz to 999.9999MHz and is routed to the RF Wattmeter Module.

11.2 SIGNALS SUMMARY

11.2A Signal Descriptions

*CAL LATCH 1-2** inputs calibrate the output level in the generate path. Each input clocks the data from LATCHED WRITE 0-7 into a latch and 8-bit DAC.

GEN OUT output is the generated signal to the Wattmeter Module.

LATCHED WRITE 0-7 input lines are used as a static data bus. All eight lines are used with VERNIER LATCH 1* & 2* and CAL LATCH 1* & 2*.

*OUTPUT ATTEN 1** input enables or disables a 20dB attenuator in the 310.7MHz path.

RF OPTION input is reserved for future options to input a RF signal into the generate path.

*VERNIER LATCH 1-2** inputs fine tune the output level to finer steps. Each input clocks the data from LATCHED WRITE 0-7 into a latch and 8-bit DAC.

1st GEN LO input from the High Synthesizer Module is used to downconvert the 1710.7MHz Generate IF to the desired output frequency.

310.7 MHz GEN IF input from the Generator Module can be modulated or unmodulated.

1400 MHz LO input from the High Synthesizer Module is a fixed local oscillator used to up-convert the 310.7MHz Gen to 1710.7 MHz 2nd IF.

+5V, +12V and *-12V* supply power to the module.

11.2B Connector Descriptions

P1 (50 Pin Edge Connector to RF Motherboard)

pin	
1,2	GND
3,4	+5V
5-8	not used by this module
9	READ SPARE 1 ●
10	RF ATTEN SPARE 1 ●
11	READ SPARE 2 ●
12	not used by this module
13	OUTPUT ATTEN 1*
14-16	not used by this module
17	RF OUTPUT SFARE1 ●
18	VERNIER LATCH 1*
19	RF OUTPUT SPARE 2 ●
20	VERNIER LATCH2*
21	not used by this module
22	CAL LATCH 1*
23	LATCHED WRITE 0
24	CAL LATCH 2*
25	LATCHED WRITE 1
26	not used by this module
27	LATCHEDWRITE2
28	not used by this module
29	LATCHEDWRITE3
30	not used by this module
31	LATCHED WRITE 4
32	not used by this module
33	LATCHEDWRrIE5
34	not used by this module
35	LATCHED WRITE 6
36	not used by this module
37	LATCHED WRITE 7
38	not used by this module
39,40	GND
41-44	not used by this module
45,46	-12V
47,48	+12V
49,50	GND

- Signal is a spare in the basic Analyzer, but may be utilized in future product development.

SMB Connectors

J1 310.7MHz GEN
Input freq: 255.7 to 365.7MHz
Input level: -17.5dBm ±2.5dB
Input impedance: 50Ω nominal
VSWR: 2:1 maximum

J2 RF OPTION
Input freq: 310.7MHz
Input coupling: -20dB ±1dB

J3 1400MHz GEN LO
Input freq: 1390.0001-1400MHz in 100Hz steps
Input level: +2dB ±2.5dB
Input impedance: 50Ω nominal
VSWR: 2:1

J4 1st GEN LO
Input freq: 1710-2710MHz in 10MHz steps
Input level: -4dBm to +3dBm
Input impedance: 50Ω nominal
VSWR: 2:1

J5 GEN OUT
Output freq: 400KHz to 999.9999MHZ
Input impedance: 50Ω nominal
VSWR: 2:1

11.3 BLOCK DIAGRAM DESCRIPTION

The RF Output module amplifies or attenuates, and then translates a signal input at the 310.7MHz Gen port to 400KHz - 999.9999MHz.

The first conversion is from the 310.7 ±55MHz to 1710.7 ±55MHz. The 1710.7MHz signal is then downconverted to the desired output frequency in the 400KHz to 999.9999MHz range.

The gain of the module is variable through electronically controlled attenuators. The output of this module is through the Gen Out Port.

11.4 DETAILED DESCRIPTION

11.4.1 Frequency Conversion

The first mix in this module (at U3) takes the 310.7MHz GEN input signal and translates this to 1700.7001-1710.7MHz using the 1400MHz GEN LO input signal (1390.0001-1400MHz).

This LO signal (from the High Synthesizer Module) is amplified by the 1400MHz LO buffer amplifier (AR1) before it is fed into the mixer.

The second mix of the module (at U9) takes the resultant 1700.7001-1710.7MHz and translates this to the desired output frequency in the range of 400KHz to 999.9999MHz using the 1st GEN LO signal, which is in the range of 1710MHz to 2710MHz. The 1st GEN LO signal comes from the High Synthesizer module and is amplified by AR3 and AR6 before it is fed into the mixer.

11.4.2 Step Attenuator

This module contains one 20 dB attenuator pad that can be switched in electronically to provide coarse attenuation adjustment to the RF path.

The attenuator is located in the 310.7MHz path (R56, R59, R66) and is switched in and out using PIN diode switches controlled with the OUTPUT ATTEN1* signal.

11.4.3 Variable Attenuation

There are three variable attenuator sections; CAL LEVEL1, CAL LEVEL2, and VERNIER LEVEL.

The LATCHED WRITE 0-7 signals are a binary representation of the desired attenuation level. All attenuators are controlled by 8-bit D/A converters. The DACs are programmed with the LATCHED WRITE 0-7 data via latches, which are set by the VERNIER LATCH1*, VERNIER LATCH2*, CAL LATCH 1*, and CAL LATCH 2* control lines.

11.4.3.1 Cal Level 1

The CAL LEVEL1 attenuator is located in the 1700-1710MHz IF path and is programmable in no greater than 1dB steps. It has a range of 24dB and is used to offset gain variations of the module due to frequency and temperature.

The CAL LATCH 1* signal is used to latch the LATCHED WRITE 0-7 data into U22. The U22 outputs are then available at D/A converter U14. The CAL VCA1 signal sets the amount of attenuation achieved with Q3 and Q4.

11.4.3.2 Cal Level 2

The CAL LEVEL 2 attenuator has a range of 25dB and is located in the 400KHz to 1000MHz path. Its operation is similar to the CAL LEVEL1 attenuator.

The CAL LATCH 2* signal is used to latch the LATCHED WRITE 0-7 data into U23. The U23 outputs are then available at D/A converter U15. The CAL VCA2 signal sets the amount of attenuation achieved with U25 and U26.

11.4.3.3 Vernier Level

The vernier level attenuator is located in the 310.7MHz GEN path. It is programmable in no greater than 0.1dB steps and has a range of 24dB total This is used as a fine level set for the output signal.

Two latches and two 8-bit A/D converters are used to set the vernier level attenuator VERNIER LATCH1* causes U20 to latch the data at LATCHED WRITE 0-7. The digital information is then available to D/A converter U12. VERNIER LATCH2* causes U21 to latch data for D/A converter U13.

Two op-amps contained in U17 use different values for feedback resistors R117 and R118. This configures the circuit so that D/A converter U12 is used for coarse adjustment and U13 is used for fine adjustment.

The U17 output voltages are combined at U18 to create the OUTLVL signal. OUTLVL is then input to the vernier level attenuator U11.

11.4.3.4 Factory Set Attenuator

A factory set attenuator (R74, R68, R65) is also included in the module. The attenuator has 18dB of attenuation range and is used to compensate for the part to part variations of all components in the RF path of the module.

11.4.4 Gain Stages

The RF Output Module contains four gain stages throughout the RF path.

1. At 310.7MHz one amplifier (AR9) provides a nominal gain of +11dB.

2. At 1710.7MHz there are two identical amplifiers (AR2, AR7) on either side of CAL VCA1, each having +9dB gain.

3. At 400KHz to 999.9999MHz there are two identical amplifiers (AR10, AR8) on either side of CAL VCA2, each having a nominal gain of +11dB.

4. There are also two more +11dB gain amplifiers (AR5, AR4) just before the J5 GEN OUT port.

11.4.5 Filters

The 1710.7MHz bandpass filter (FLI) is placed immediately following the first mix and has a bandwidth of 150MHz. This filter is for image rejection as well as suppression of the LO leakage through the mixer.

One 1400MHz notch filter is also present in the 1710.7MHz section to provide an additional 20dB of attenuation to the undesired 1400MHz LO signal.

The final filter in the module is the 1200MHz lowpass, which is placed after the final mix. This filter provides attenuation to all signals above the desired output frequency range-

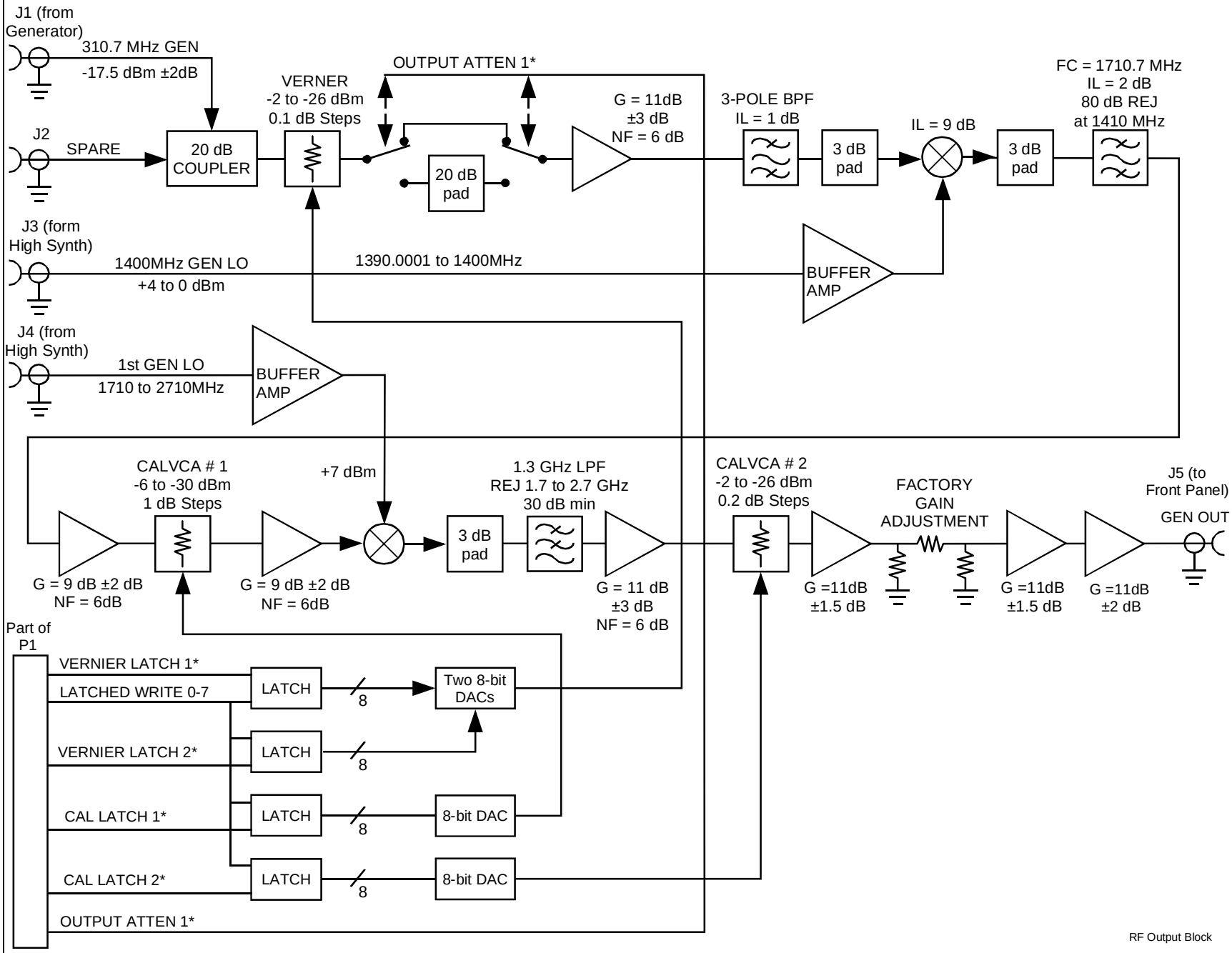
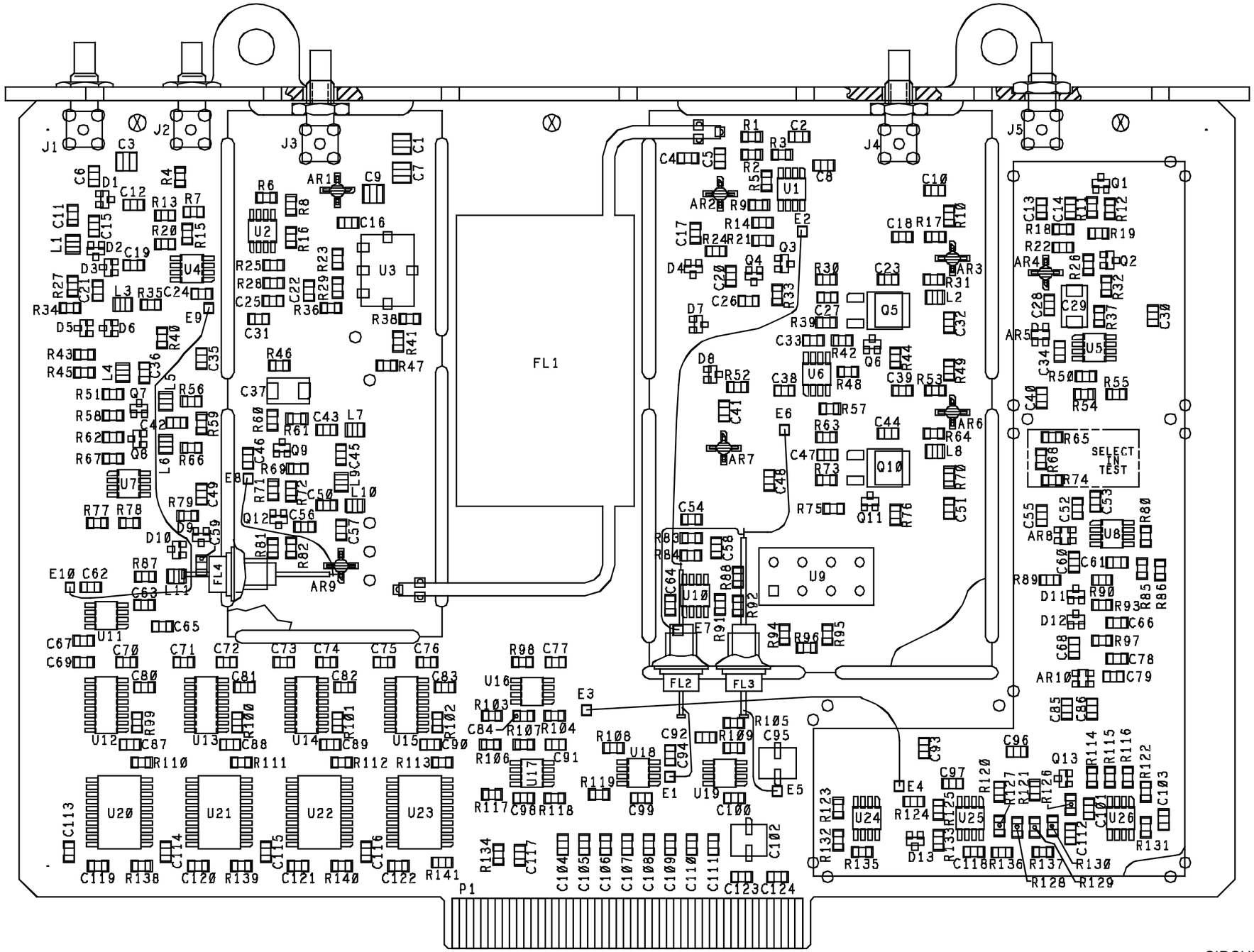


Fig. 11.5 RF Output Block Diagram

WIRE LIST

FROM	TO
FL2-1	E1
FL2-2	E2
FL3-1	E5
FL3-2	E6
FL3-2	E7
E3	E4
FL4-1	E9
FL4-1	E10
FL4-2	E8



CIRCUIT CARD ASSEMBLY
RF OUTPUT

01-P30400C REV. F

SHEET 1 OF 1

DWG NO 63-P30402C SH 1

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
C	INITIAL RELEASE AND RENUMBER. D.S.S.	02/26/90	
D	REVISED PER MCO B35613 JSB 06/26/90		
E	REVISED PER CO C35804-1 PVA 92-05-01	92-05-01	P.WEITZEL
F	REVISED PER MCO C35818 SLG 92-07-07	92-07-07	P.AMMON
G	REVISED PER CO E36146-2 DEB 95-08-07	95-08-07	KOESTNER
H	REVISED PER CO E36540-1 CJN 00-02-03	00-02-03	A.GATTO

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1A6.
2. FOR REFERENCE DRAWINGS REFER TO:
   01-P30400C ASSEMBLY
   12-P30403C TEST PROCEDURE
3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL INDUCTANCE VALUES ARE IN µH.
   ALL VOLTAGES ARE IN DC.
4. TERMINATIONS CODED WITH THE SAME LETTERS OR NUMBERS ARE ELECTRICALLY CONNECTED.

5. DEVICE TYPE NUMBERS AND CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE 1. PORTIONS OF THE TYPE NUMBER MAY BE UNDERLINED AND USED AS A CODE TO IDENTIFY DEVICES ON DIAGRAM.

6. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH MANUFACTURER. ENGINEERING APPROVED EQUIVALENT DEVICE MAY BE USED.

7. ON SHEET 9, R104 VALUE IS CHANGED FOR -002 ASSEMBLY.

8. SELECT AT TEST.

TABLE 1 (5)

REF DES	DEVICE TYPE (6)	+5	GND	+12V	-12V	LOCATION
U1	LM317LD			1		7
U2	LM317LD			1		5
U3	SMDC3		4,5			4
U4	LM317LD			1		3
U5	LM317LD			1		5
U6	LM317LD			1		7
U7	MC34072			8	4	4
U8	LM317LD			1		5
U9	MLP-B77S		2,5,6,7			6
U10	LM317LD			1		7
U11	MC34072			8	4	3
U12	DAC-08			1	7	8
U13	DAC-08			1	7	8
U14	DAC-08			1	7	9
U15	DAC-08			1	7	9
U16	MC34072			8	4	9
U17	MC34072			8	4	8
U18	MC34072			8	4	8,9
U19	LM317LD			1		9
U20	74ACT374	20	10			8
U21	74ACT374	20	10			8
U22	74ACT374	20	10			9
U23	74ACT374	20	10			9
U24	LM317LD			1		5
U25	MC34072			8	4	6
U26	MC34072			8	4	6

REFERENCE DESIGNATIONS	
HIGHEST NUMBER USED	NOT USED
AR10	
C124	
D13	
E10	
FL4	
J5	
L11	
P1	
Q13	
R141	
U26	

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

ALL SHEETS ARE THE SAME REVISION STATUS

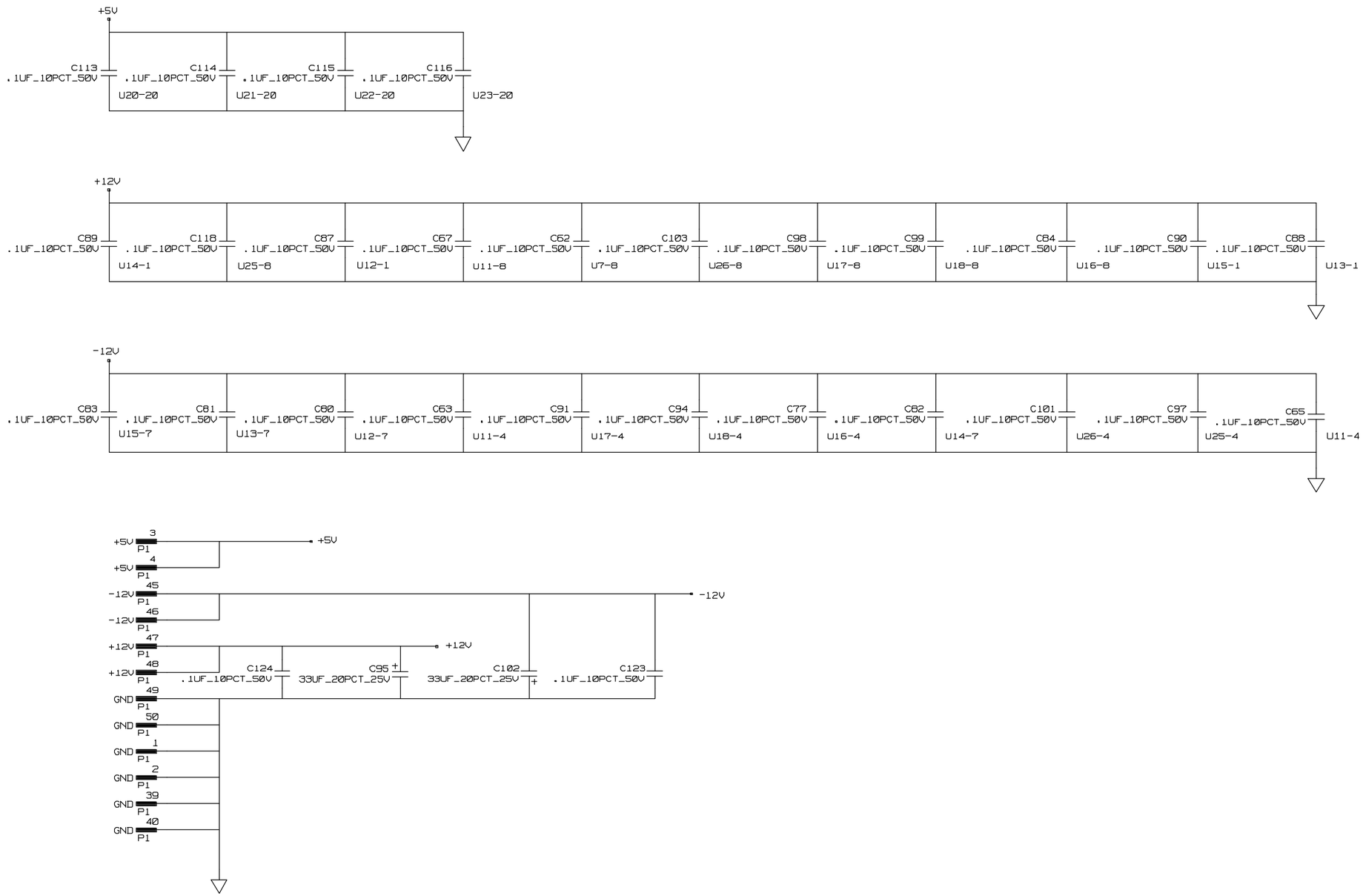
		CONTR	3980
		ISS	35550-53(C)90/4/17
		APPROVALS	
		DWN	K.HAGEDON
		CHKR	
		QA	K.NELSON 90/4/12
		MATL	
01-P30400C	COCHISE	MFG	J.DECAMP 90/4/12
NEXT ASSY	USED ON	ENG	D.ZELINKA 90/4/12
APPLICATION		CUST	

MOTOROLA INC.
GOVERNMENT AND SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

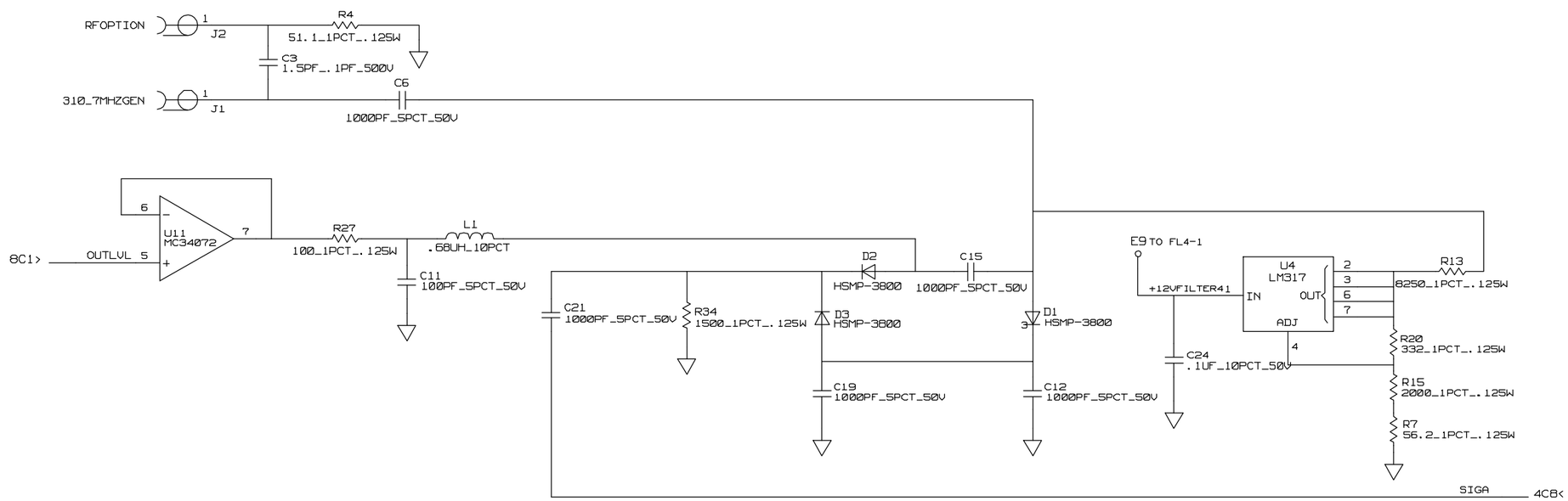
TITLE
R.F. OUTPUT
SCHEMATIC DIAGRAM

SIZE D CAGE CODE 94990 DWG NO 63-P30402C

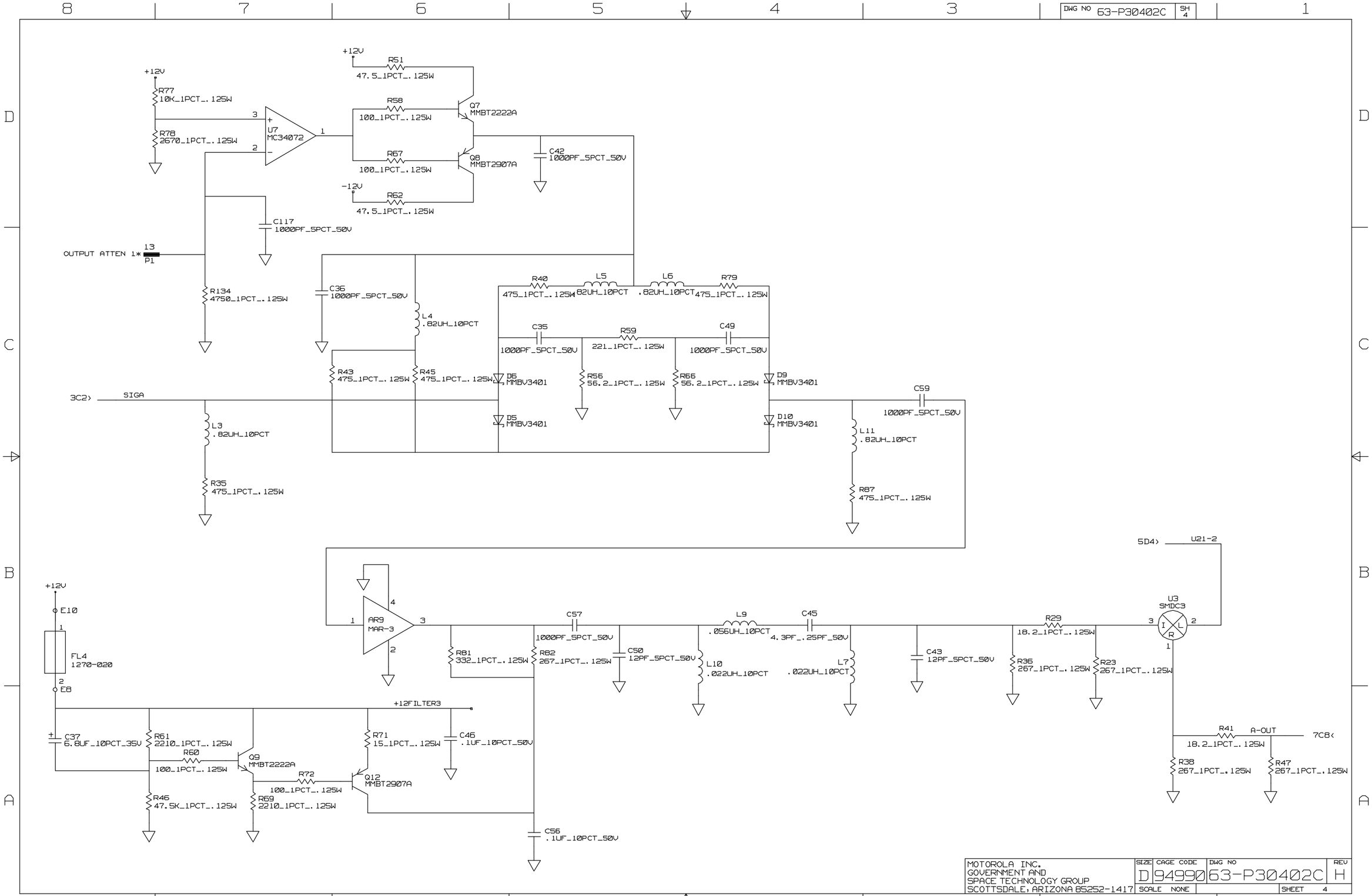
SCALE NONE SHEET 1 OF 9



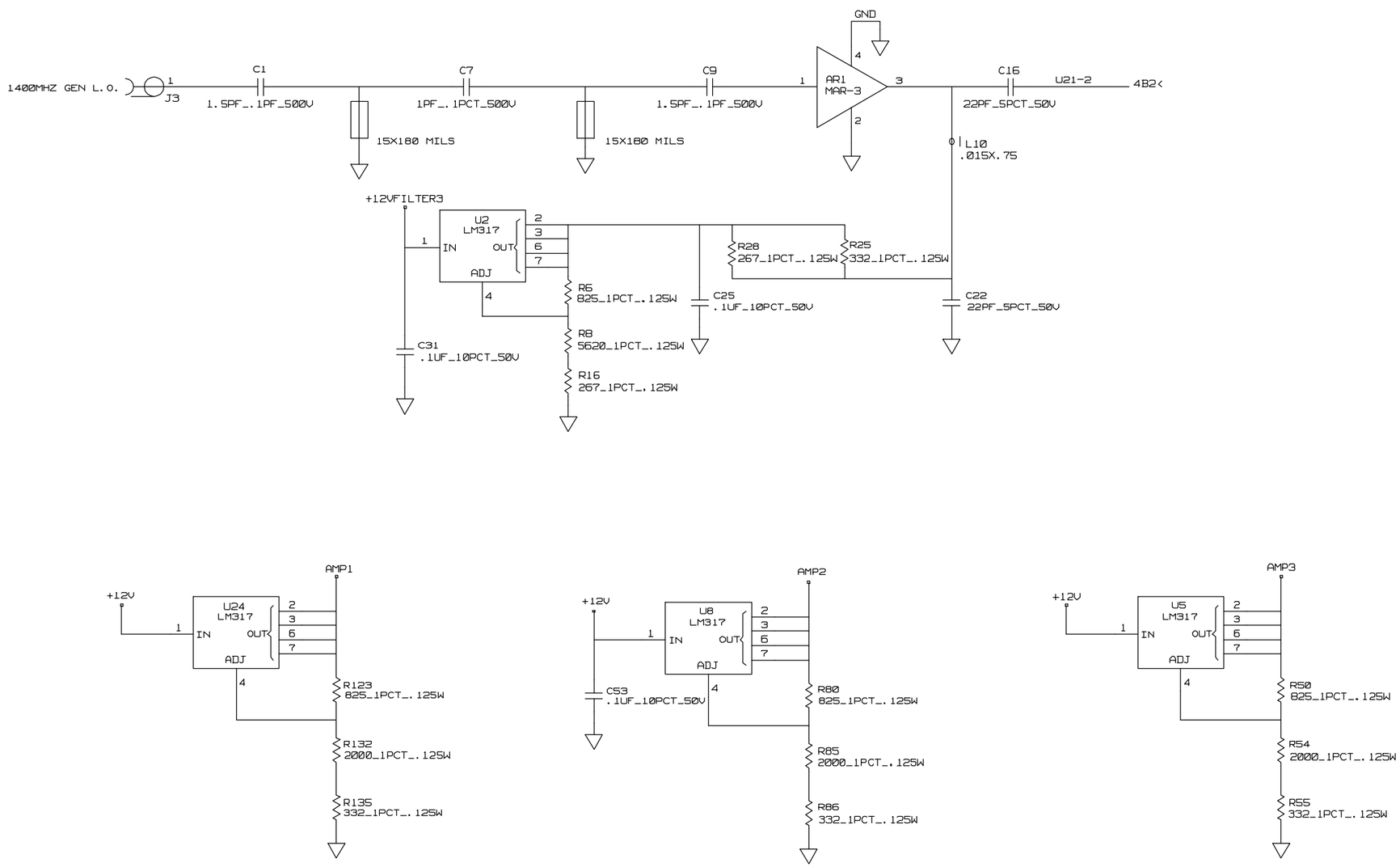
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30402C	REV H
	SCALE NONE		SHEET 2	



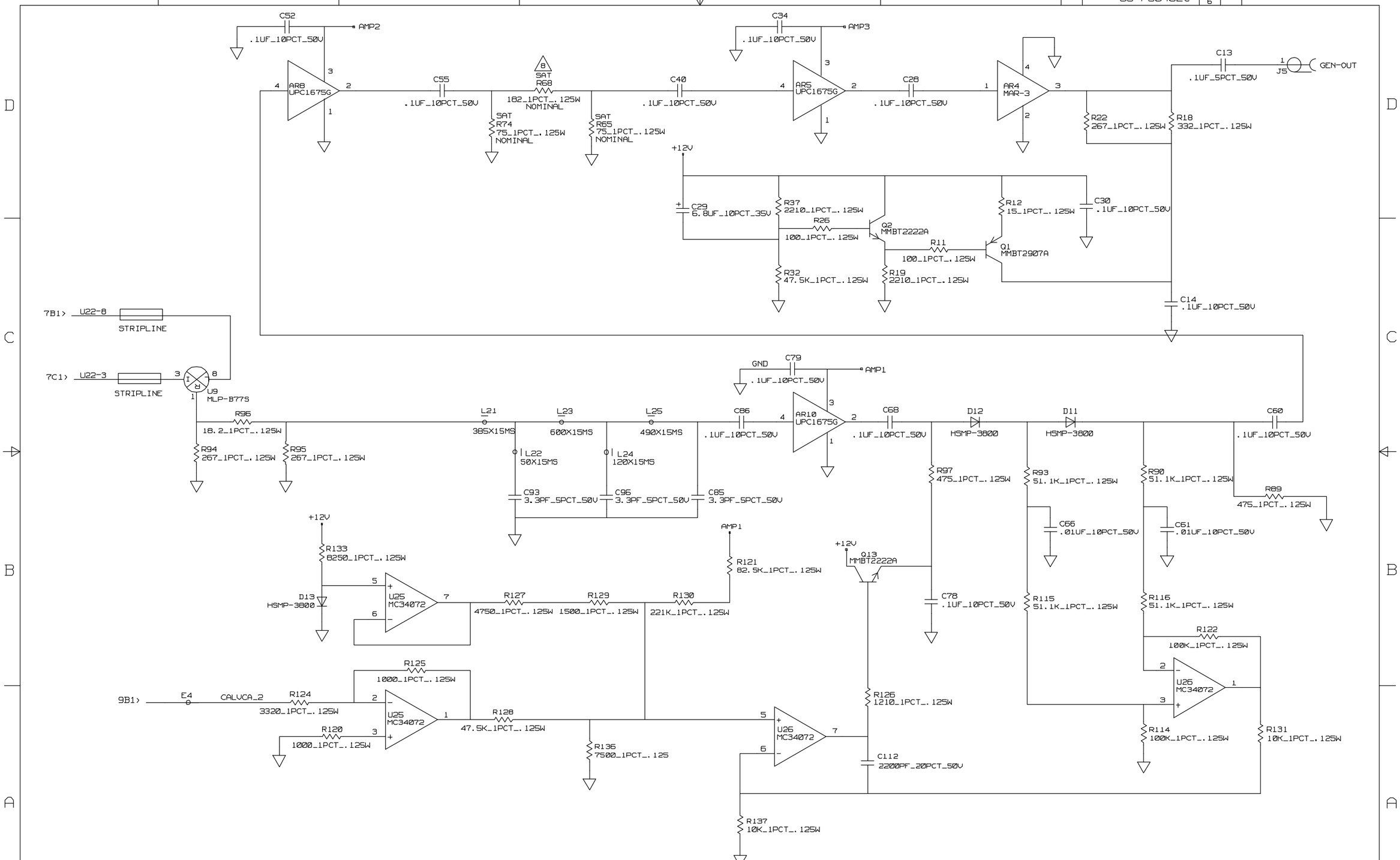
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30402C	REV H
	SCALE NONE			SHEET 3



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30402C	REV H
	SCALE NONE			SHEET 4



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30402C	REV H
	SCALE NONE		SHEET 5	



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30402C	REV H
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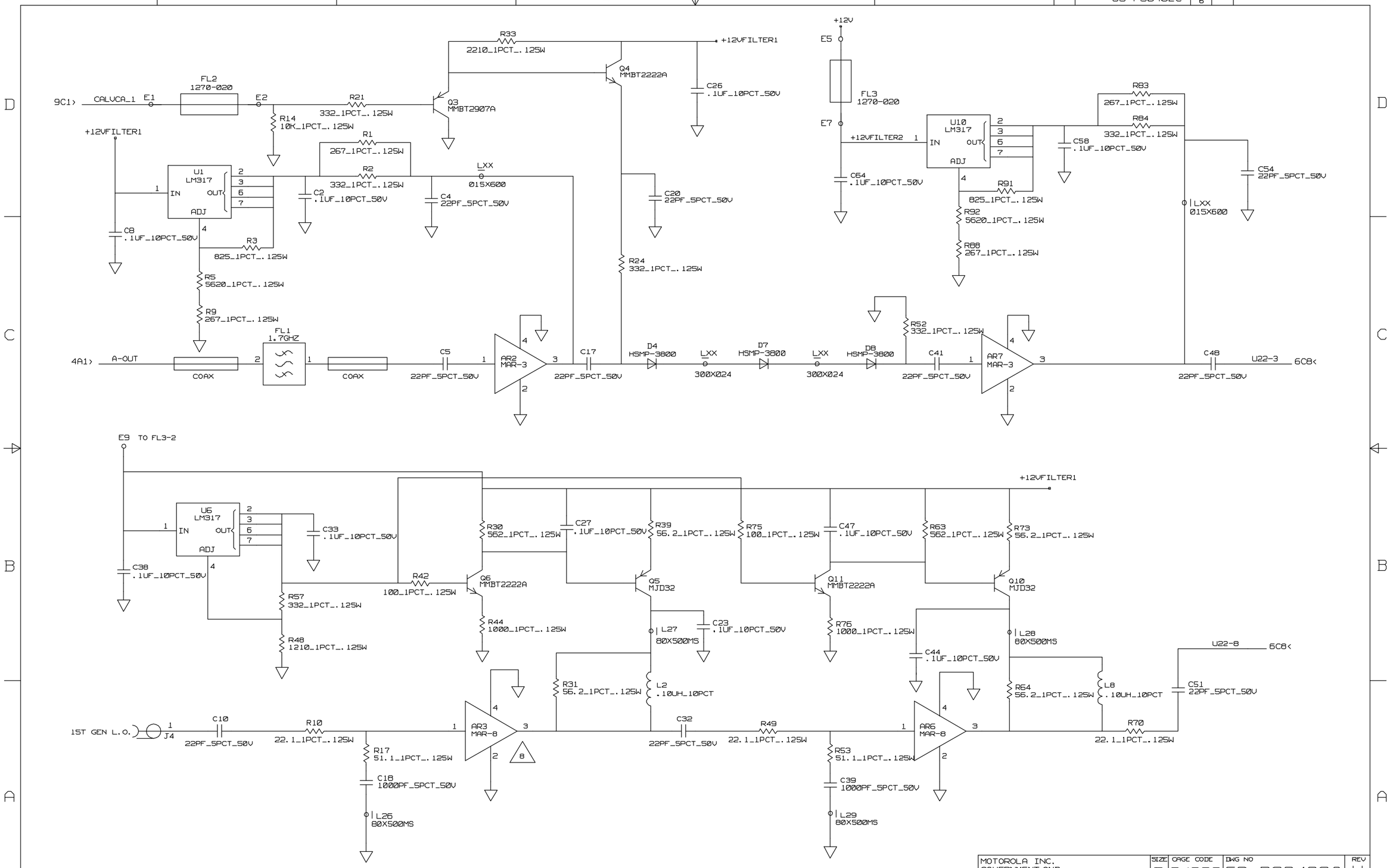

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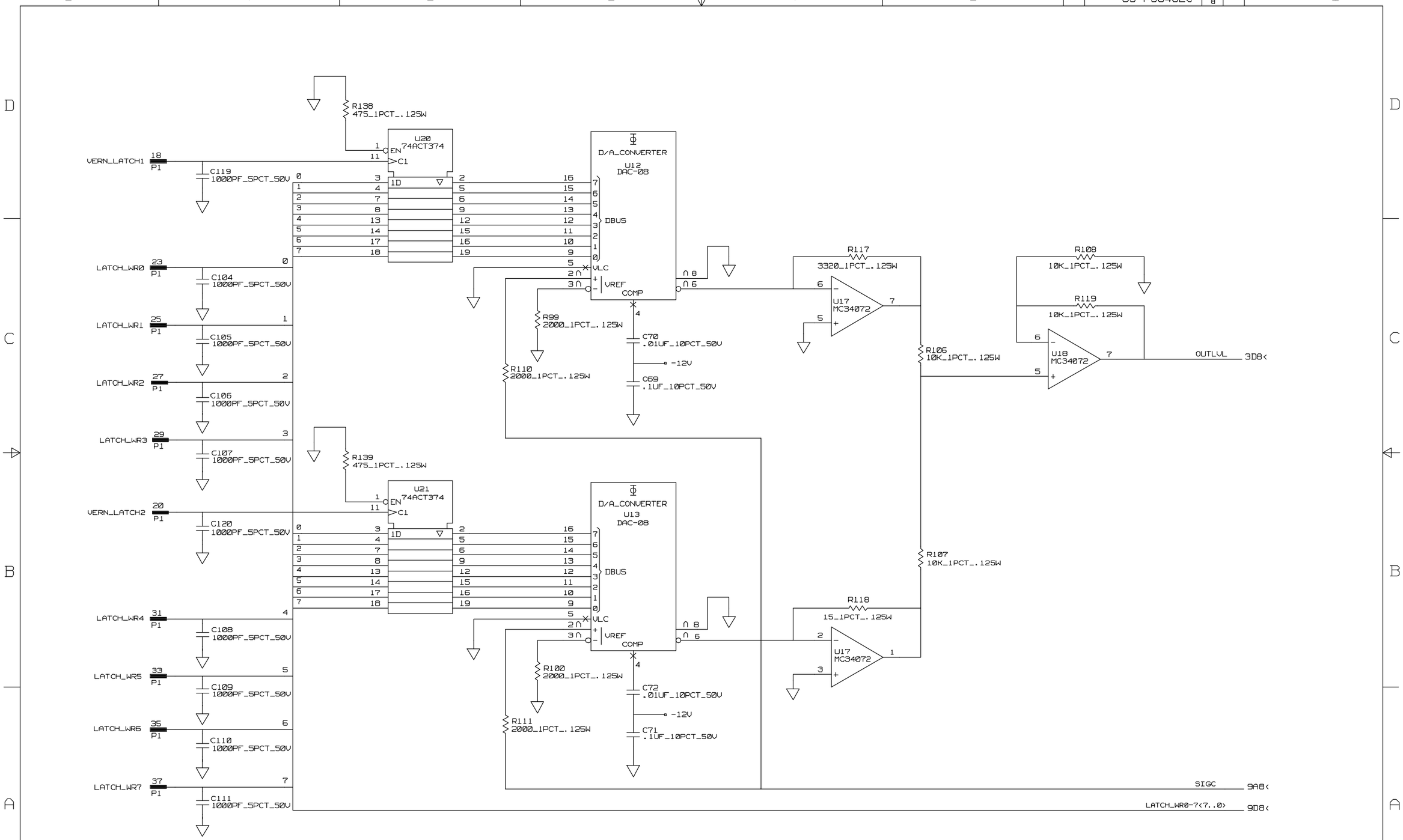
	SCALE NONE		SHEET 7	



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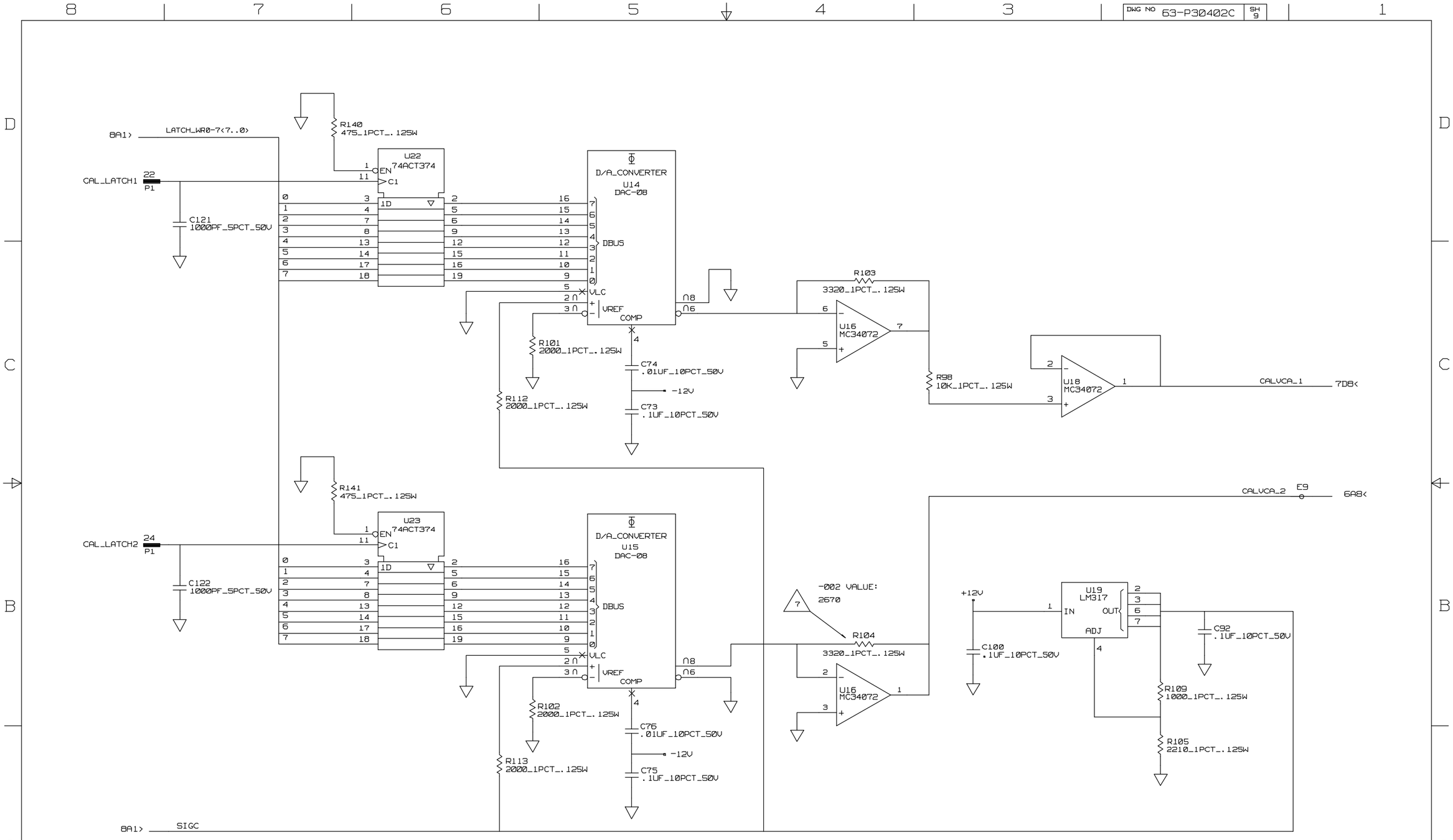

MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30402C	REV H
	SCALE NONE		SHEET 9	

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12.1 GENERAL DESCRIPTION

The RF Wattmeter is designated as module A2 and is located underneath the LCD Display.

The RF Wattmeter Module performs several functions. First, it performs all high level RF power measurements for the Analyzer. Second, it provides a path to the receiver for signal strength measurements and self-calibration for the generate mode. Third, it performs the switching functions necessary to generate signals to either of two front panel ports

The Analyzer provides an over-temperature warning to the user in the form of an audible signal and an on-screen warning.

NOTE

There is no guarantee of accuracy of the input power reading when in AM mode with modulation.

WARNING

The maximum allowable input power is 125Watts, but this is at no more than a 20% duty cycle (max 1 minute out of five minutes) Do not use the RF Wattmeter for continuous input over 25 Watts to avoid circuit damage.

NOTE

The RF Wattmeter is not a field repairable item since recalibration is mandatory after repair of the module. Recalibration requires highly specialized factory equipment, which considers the characteristics of a specific module during prom programming. Contact one of the Motorola Service Centers listed in the foreword of this manual for information on calibration, repair, and/or replacement of the RF Wattmeter module.

12.2 SIGNALS SUMMARY

12.2A Signal Descriptions

CAL RF output is either the Gen Out input signal or the RF I/O input signal depending on the state of the GEN OUT/(RF I/O)* control signal.

FP GEN OUT is the output signal for the Front Panel Gen Out port on the front panel.

*G** is an input used in the factory to program the EPROM while the EPROM is on the module. A logic 0 indicates Read or Standby mode while a logic 1 indicates Program mode. When in the system, this line is not connected to any other modules.

GEN OUT input is the signal to be output to the RF I/O or FP Gen Out ports.

*GEN OUT/(RF I/O)** input is used as a control line to select the output port to be either the RF I/O port (logic 0) or the FP GEN OUT port (logic 1). This signal is also used at other modules in the system.

*INPUT DET GAIN** input from the Interface Module is used to switch in additional amplification at low input power levels.

INPUT POWER DET is a 0 to +5VDC output that is proportional to the RF Power Level Input.

INPUT TEMP SENSE is a 0 to +5VDC output that is proportional to the temperature of the Input Power Detector.

LATCHED WRITE 0-7 inputs address the correct location in the EPROM.

*OUTPUT AMP I** input is used to enable an 18.5dB amplifier stage in the generate path.

*OUTPUT ATTEN 2** input is used to insert a 22.5dB attenuator into the generate path.

OUTPUT POWER DET is a 0 to +5VDC output that is proportional to the RF Power Level Output.

OUTPUT TEMP SENSE is a 0 to +5VDC output that is proportional to the temperature of the Output Power Detector.

OVERTEMP output indicates when the temperature of the receive input power detector is over a specified level. A logic 1 indicates an over temperature condition.

READ BUS 0-7 These lines are used by the system processor to read the contents of the EPROM.

VPP line is an input that is used to program the EPROM while the EPROM is in the module during factory calibration. When in the system, this line is not connected to any other modules.

RF I/O line is a bi-directional signal, which is used as a high level input/low level output port to the front panel.

*WATT ADD LATCH 1-2** inputs are used to enable the latches that address the EPROM. WATT ADD LATCH 1* addresses the eight least significant bits and WATT ADD LATCH 2* addresses the seven most significant bits.

WATT DATA EN* input latches data from the EPROM into READ BUS 0-7.

+5V, +12V, and -12V supply power to the module.

12.2B Connector Descriptions

P1 (50 Pin Edge Connector (RF Motherboard interface)

pin	
1,2	GND
3,4	+5V
5,6	not used at this module
7	INPUT PWR DET (receive power detect)
8	OUTPUT PWR DET (generate power detect)
9	INPUT TEMP SENSE (temperature sensor of monitor power detect)
10	OUTPUT TEMP SENSE (temperature sensor of generate power detect)
11	OUTPUT AMP 1* (reduces gain by 20dB)
12	OUTPUT ATTEN 2* (enables a 20dB pad)
13	G* (factory use only)
14	READ BUS 0
15	VPP (factory use Only)
16	READ BUS 1
17	READ SPARE1 ●
18	READ BUS 2
19	READ SPARE 2 ●
20	READ BUS 3
21	GEN OUT/(RFI/O)*
22	READ BUS 4
23	RF OUTPUT SPARE 1 ●
24	READ BUS 5
25	RF OUTPUT SPARE 2 ●
26	READ BUS 6
27	INPUT DET GAIN* (input pwr det voltage gain)
28	READBUS7
29	LATCHED WRITE 0
30	OVERTEMP (receive overtemp)
31	LATCHED WRITE 1
32	WATT ADD LATCH1* (address latch)
33	LATCHED WRITE 2
34	WATT ADD LATCH2*(address latch)
35	LATCHED WRITE 3
36	WATT DATA EN* (data enable)
37	LATCHED WRITE 4
38	SPARE BUS ●
39	LATCHED WRITE 5
40	not used by this module
41	LATCHED WRITE 6
42	not used by this module
43	LATCHED WRITE 7
44	not used by this module
45,46	-12V
47,48	+12V
49,50	G1ND

• Signal is a spare in the basic Analyzer, but may be utilized in future product development

J1 RF I/O (Type N Connector)

RF I/O
I/O Freq: 400KHz to 999.9999MHz
I/O impedance: 50Ω nominal
VSWR: 1.5:1
Input Level: -50 to +20dBm (+20 to +51 for frequencies above 1MHz)

SMB Connectors

J2 GEN OUT (from Generator Module)
Input freq: 400KHz to 999.9999MHz
Max input level: -4.7dBm min
Input impedance: 50 Ω nominal
VSWR: 2:1 maximum

J3 CAL RF
Output freq: 400KHz to 999.9999MHz
Output impedance: 50Ω nominal
VSWR: 2:1 maximum

J4 FP GEN OUT (to Front Panel)
Output freq: 400KHz to 999.9999MHz
Output impedance: 50Ω nominal
VSWR: 2:1 maximum

12.3 BLOCK DIAGRAM DESCRIPTION

The RF Wattmeter uses two power detectors, an input detector to measure the power input to the RF I/O port, and an output detector to measure power output at the FP Gen Out port. The working range of the input at the detector is from -10dBm to +21dBm. The output detector operates over the range of -15dBm to +10dBm. Temperature sensors are mounted isothermally to each power detector to allow the system microprocessor to monitor the power detector's temperature.

Each of the two power detectors outputs a voltage that increases with an increase of input power. This voltage is applied to an analog to digital converter (resident on the Interface Module). The processor then looks up calibration factors based on the power detector voltage, frequency, and temperature in the calibration EPROM resident on the RF Wattmeter Module. This EPROM is factory calibrated with the RF Wattmeter over power levels, temperature and frequency. The calibration data is valid only for the wattmeter for which it is calibrated. The processor utilizes these calibration factors to calculate the power level.

The RF Wattmeter has two RF inputs; the RF I/O port (Front Panel) and the J2 Gen Out signal (from the RF Output Module). The RF I/O port is a high level port designed for inputs up to 125 watts (max 1 minute continuous, 4 minutes off). Gen Out is the output of the RF Output Module.

Signals input to the RF I/O port are attenuated by 36dB and are output at the J3 CAL RF port. Signals input at the J2 Gen Out port are switched either to the J4 FP GEN OUT port or to both the J1 RF I/O and J3 CAL RF ports.

12.4 DETAILED DESCRIPTION

The RF Wattmeter module performs all high level RF power measurement in the Analyzer's RF system. Power measurements are made at the RF I/O Port. The RF Wattmeter is factory calibrated and is the basis for the power measurement accuracy of the system. When the Front Panel CAL function is activated the system calibrates both the receive and generate paths using the RF Wattmeter.

This module has one bi-directional port, the RF I/O port (J1). There is also one input port, the GEN OUT port (J2). There are seven output pins;

1. INPUT POWER DET (P1-7)
2. OUTPUT POWER DET (Pl-8)
3. INPUT TEMP SENSE (Pl-9)
4. OUTPUT TEMP SENSE (Pl-10)
5. CAL RF (J3)
6. FP GEN OUT (J4)
7. OVERTEMP (P1-30)

Only +12Vdc, -12Vdc, and +5V supplies are used. The -12Vdc supply is filtered to -6.5Vdc.

12.4.1 Monitor Mode

12.4.1.1 RF I/O Port

The RF I/O port accepts inputs over the frequency range of 400KHz to 999.9999MHz at power levels of -50dBm to +51dBm. The maximum VSWR at this port is 1.5:1.

Signals applied at this port are attenuated by a 24dB power attenuator, U12. This attenuator, when mounted in the unit, is capable of withstanding 125W for 1 minute continuous with a minimum of 4 minutes off

12.4.1.2 CAL RF Port

This output is used by the RF Input Module. The signal is eventually passed on to the Receiver and Spectrum Analyzer Modules for measuring signal strength. It has a maximum, VSWR of 2:1.

Signal strengths of low power level signals are measured by the Spectrum Analyzer Module, which receives the CAL RF signal through the RF Input Module. CAL RF is obtained from the output of a 13dB attenuator (R118, R114, R107). The attenuator input is obtained from a 6dB splitter R109, R113, R104) which is attached to another 6dB splitter at U12. CAL RF is also used during system calibration.

12.4.1.3 Input Power DET

This dc output (P1-7) operates only over the input frequency range of 1MHz to 999.9999 MHz. It is used to measure power levels of +20dBm to +51dBm.

The signal is applied to the detector at the output of a 6dB splitter formed by resistors R108, R111, and R112. The detector is a peak detector with diode D8 rectifying the input signal. Diode D7 is used to provide temperature compensation. Both diodes are biased at 20 microamperes. The diodes' forward voltage is matched to within 15mV at 200 microamperes to allow a larger op-amp gain to be used. U11 is the amp used for this detector. At low power levels additional amplification is provided by U31. This amp is switched in by INPUT DET GAIN*.

12.4.1.4 Input Temp Sense

This dc output (Pl-9) is used to measure the temperature of the input power detector for the purpose of automatic temperature compensation. The circuit consists of a sensor temperature sensor, U10 and bias circuitry.

12 4.1.5 Overtemp

This dc output (P1-30) is used to indicate if too much power is being input to the RF I/O port by measuring the temperature near the power attenuator

The circuit uses the same sensor temperature sensor as INPUT TEMP SENSE. Op-amp U9 is used as a comparator.

12.4.2 Generate Mode

The J2 GEN OUT port accepts inputs from the RF Output Module over the frequency range of 400KHz to 999.9999MHz and at power levels of up to -4.7dBm. The maximum VSWR at this port is 2:1.

The port has a 1.3GHz lowpass filter (microstrip inductors L1-L5 and capacitors C13 and C20) followed by a switchable 22.5dB attenuator (R30, R33, R40). The RF switches are K1 and K2.

This attenuator is followed by a switchable 18.5dB amplifier, AR1 The RF switches here are K3 and K4. The amplifier receives dc bias from the regulator U5. The output is biased from the current source consisting of Q3-Q9, U1, and associated resistors and capacitors. Potentiometer R25 adjusts the reference current in the current source to set the amplifier output voltage, AR1 pin 5, to 5.0Vdc.

Signals can be output to either the FP GEN OUT port or the RF I/O port These paths are selected by RF switches K5 and K6.

12.4.2.1 J4 FP GEN OUT Port

This output is used to generate signals at power levels of 0dBm to -80dBm. It has a maximum VSWR of 2:1. The output is protected from applied power by diodes D4, D5, D9, and D10.

12.4.2.2 J1 RF I/O Port (as an output)

When the proper switch selections are made, this port is used to output signals at levels of -130 to -50dBm.

12.4.2.3 Output Power DET

This dc output (Pl-8) is used to measure output power levels of -25 to 0dBm (at FP GEN OUT) during system calibration.

The signal is applied to the detector at the output of K4. The detector is a peak detector with diode D3 rectifying the input signal. Diode D6 is used to provide temperature compensation. Both diodes are biased at 20 microamperes. The diodes' forward voltage is matched to within 15mv at 200 microamperes to allow a larger op-amp gain to be used. U7 is the amp used for this detector.

12.4.2.4 OUTPUT TEMP SENSE

This dc output (Pl-10) is used to measure the temperature of the output power detector for the purpose of automatic temperature compensation. The circuit consists of a zener temperature sensor, U8 and bias circuitry.

12.4.3 Calibration Date Storage

Calibration data obtained during factory calibration is stored in a UV-EPROM U4 Two 8-bit latches, U2 and U3, are used to latch 15 address lines to the EPROM.

12.5 BLOCK DIAGRAM

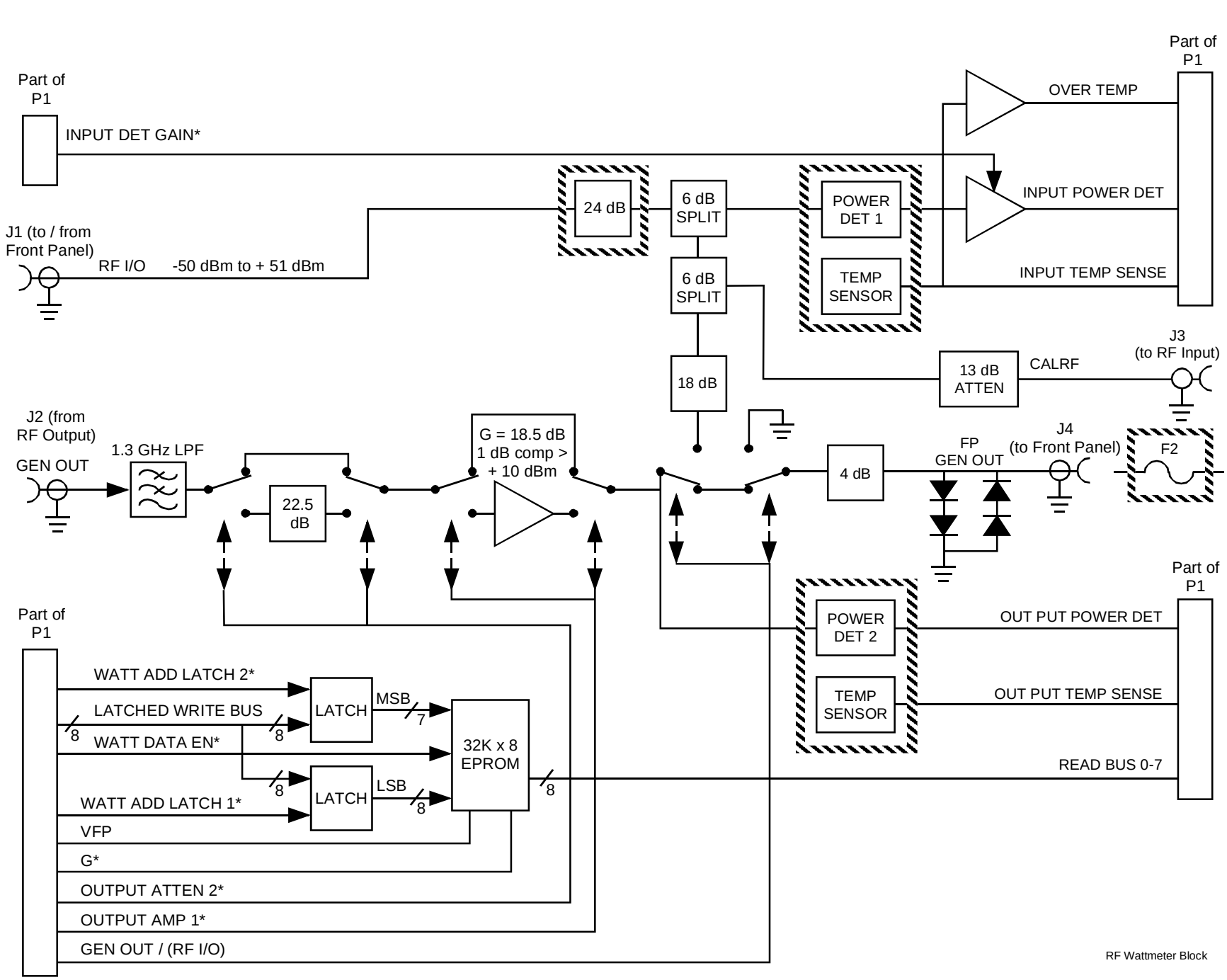
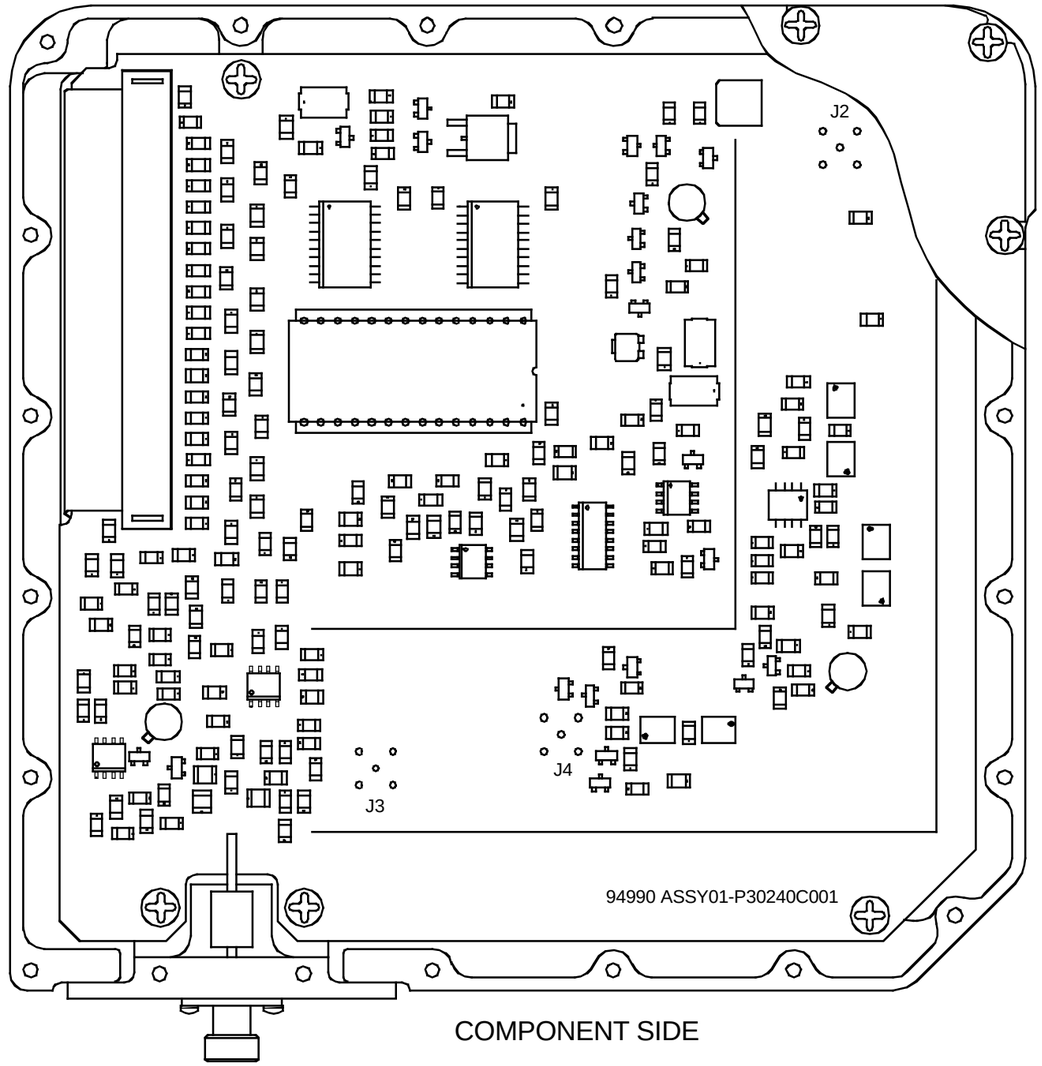
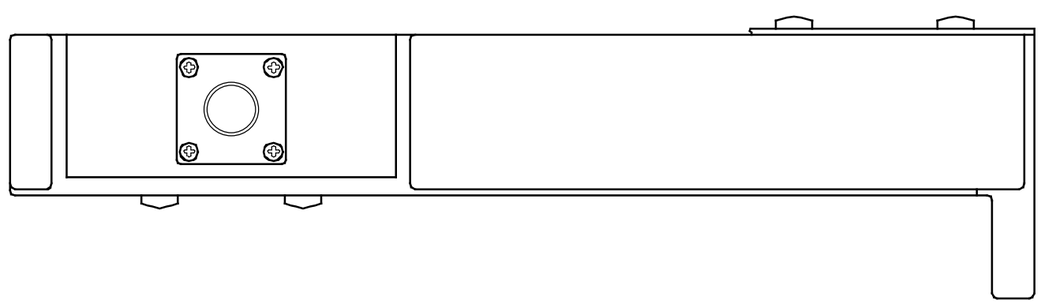


Fig. 12.5 RF Wattmeter Block Diagram



COMPONENT SIDE



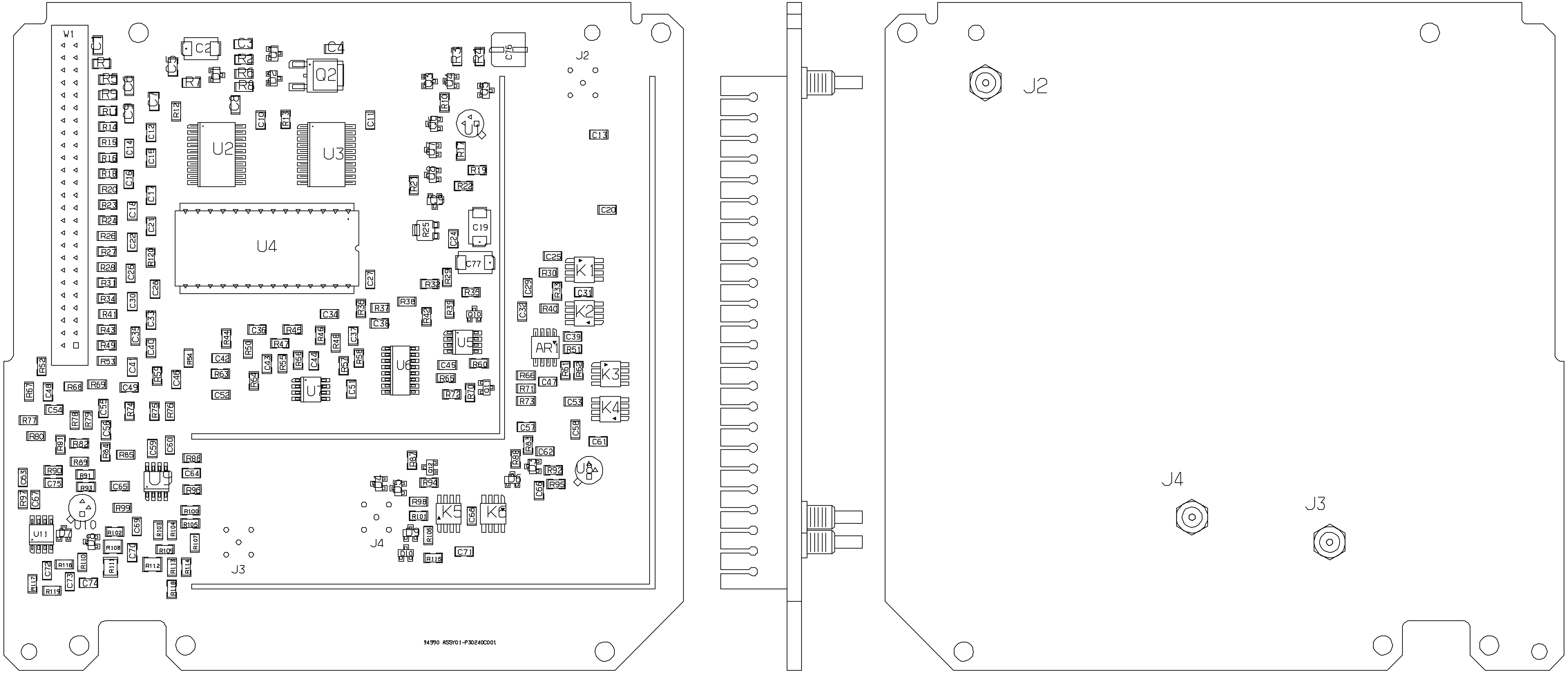
CAUTION

THIS ITEM IS SENSITIVE TO ELECTROSTATIC DISCHARGE (ESD).

CIRCUIT CARD ASSEMBLY
RF WATTMETER

01-P30240C REV. D

SHEET 1 OF 2



COMPONENT SIDE

BACK SIDE

CIRCUIT CARD ASSEMBLY
RF WATTMETER

01-P30240C REV. D

SHEET 2 OF 2

DWG NO 63-P30242C SH 1

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
B	INITIAL RELEASE AND RENUMBER D.S.S.	02/26/90	
C	REVISED PER MCO B35582 5-16-90 LRS	90/05/18	D.DUNCAN
D	REVISED PER MCO E36156-1 FAD 95-07-10	95-07-13	A.KOESTNER

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1A2.

2. FOR REFERENCE DRAWINGS REFER TO:
   01-P30240C ASSEMBLY
   12-P30243C TEST PROCEDURE

3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL VOLTAGES ARE IN DC.

4. TERMINATIONS CODED WITH THE SAME LETTERS OR NUMBERS ARE ELECTRICALLY CONNECTED.

5. DEVICE TYPE NUMBERS AND CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE 1. PORTIONS OF THE TYPE NUMBER MAY BE UNDERLINED AND USED AS A CODE TO IDENTIFY DEVICES ON DIAGRAM.

6. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH MANUFACTURER. ENGINEERING APPROVED EQUIVALENT DEVICE MAY BE USED.

7. SELECT AT TEST.

TABLE 1 (5)

REF DES	DEVICE TYPE (6)	GND	+5	NO CONN.
U1	LM335AH			
U2	74ACT374SC	10	20	19
U3	74ACT374SC	10	20	
U4	TMS27C256-17J	14	28	
U5	LM317D			
U6	DG211CSE			
U7	MC34072D			
U8	LM335AH			1
U9	MC34072D			
U10	LM335AH			1
U11	MC34072D			
U12	58-P30247C001			
AR1	UPC167B			

REFERENCE DESIGNATIONS	
HIGHEST NUMBER USED	NOT USED
AR1	
C77	C23, C50
D10	
J4	
K6	
P1	
Q12	
R120	
U11	
AT1	

ALL SHEETS ARE THE SAME REVISION STATUS

		CONTR X
		ISS B35550-53B_90-4-17
		APPROVALS
		DWN F.DEPIERRO 95-03-31
		CHKR
		QA
		MATL
		MFG
NEXT ASSY	USED ON	ENG
APPLICATION		CUST

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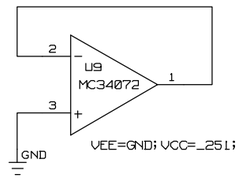
SCOTTSDALE, ARIZONA 85252-1417

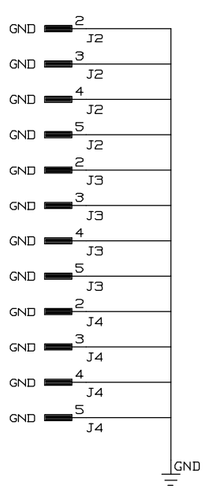
TITLE
WATTMETER
SCHEMATIC DIAGRAM

SIZE	CAGE CODE	DWG NO
D	94990	63-P30242C

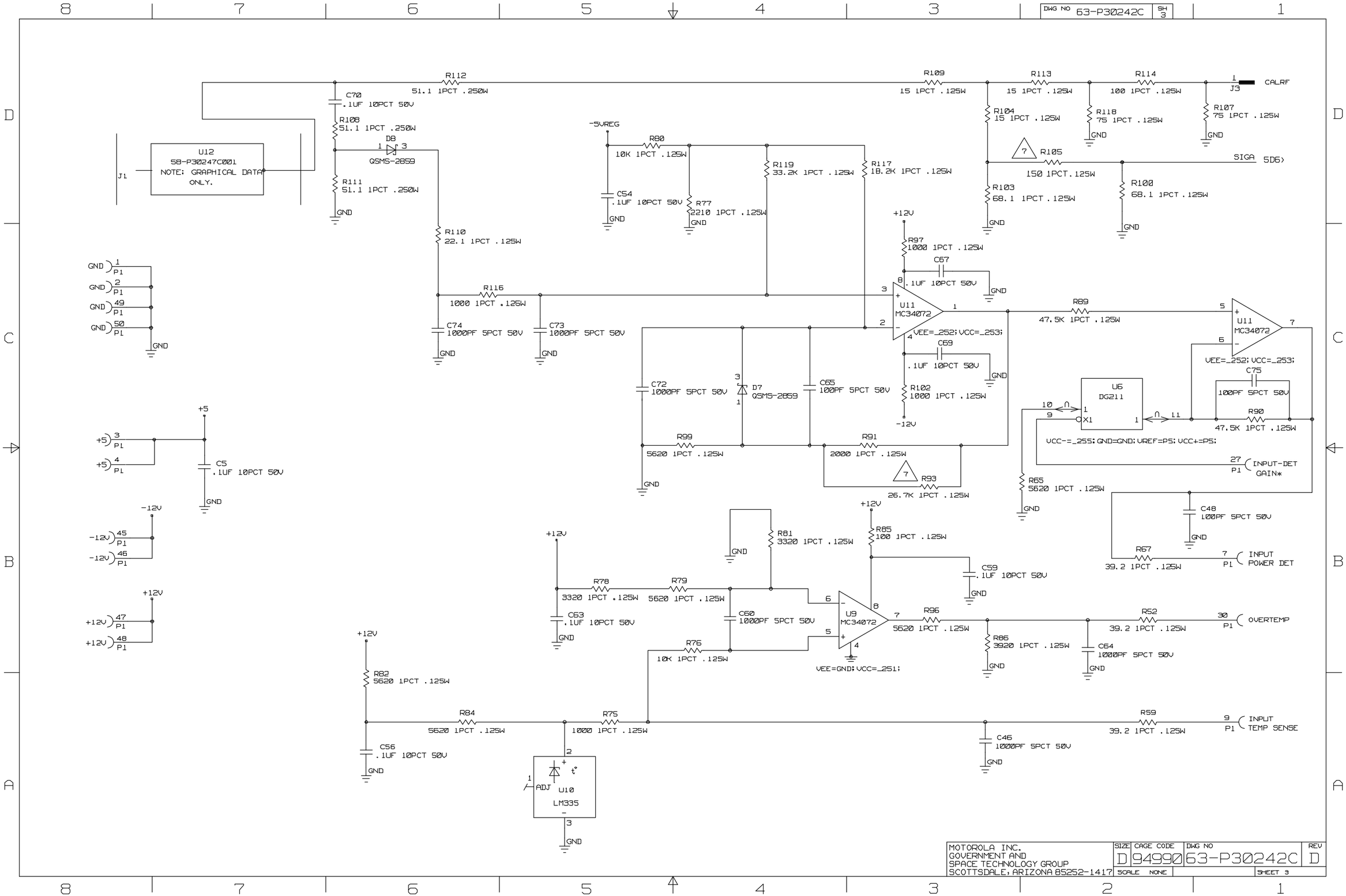
SCALE NONE SHEET 1 OF 6

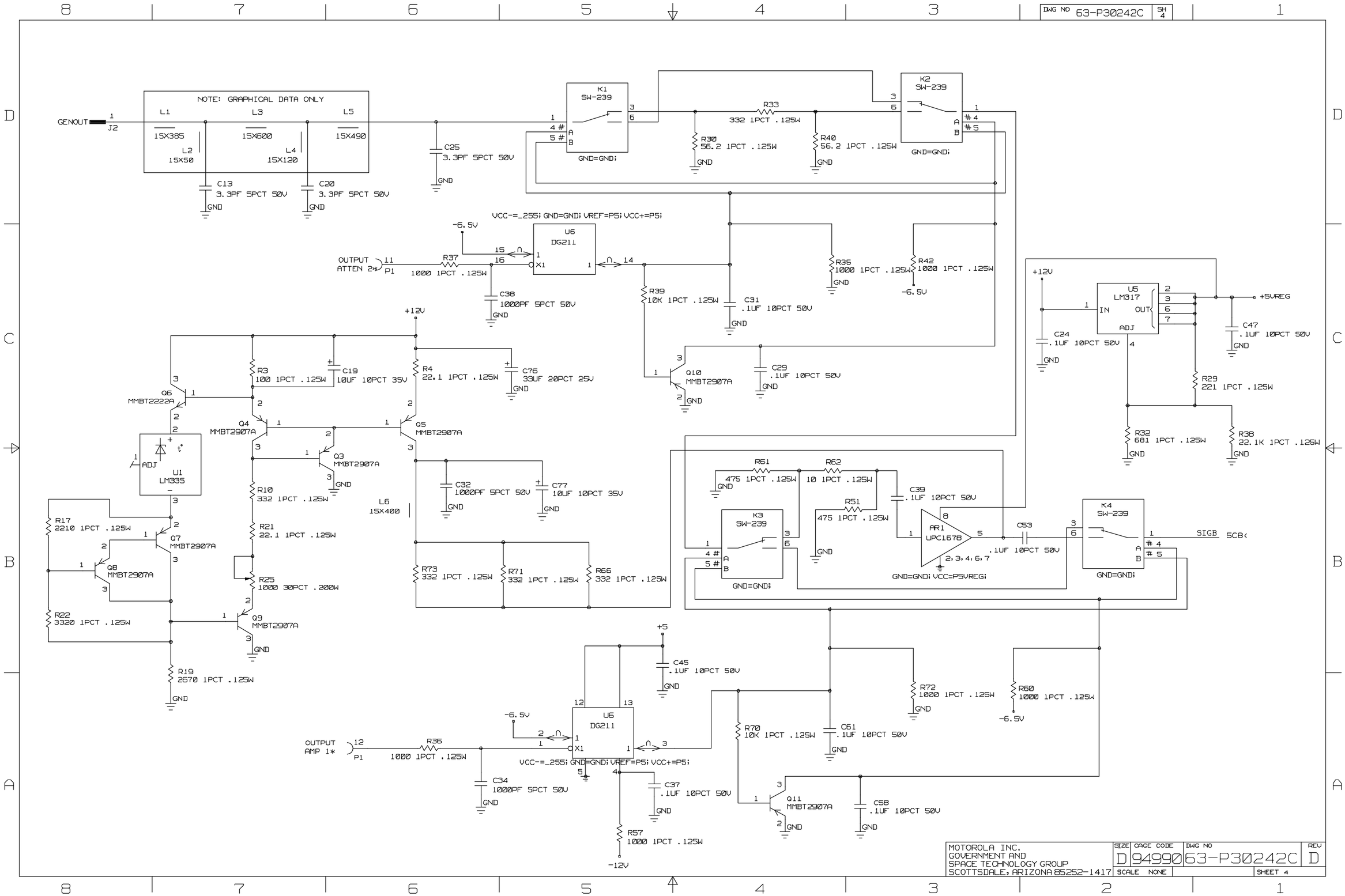
SPARES

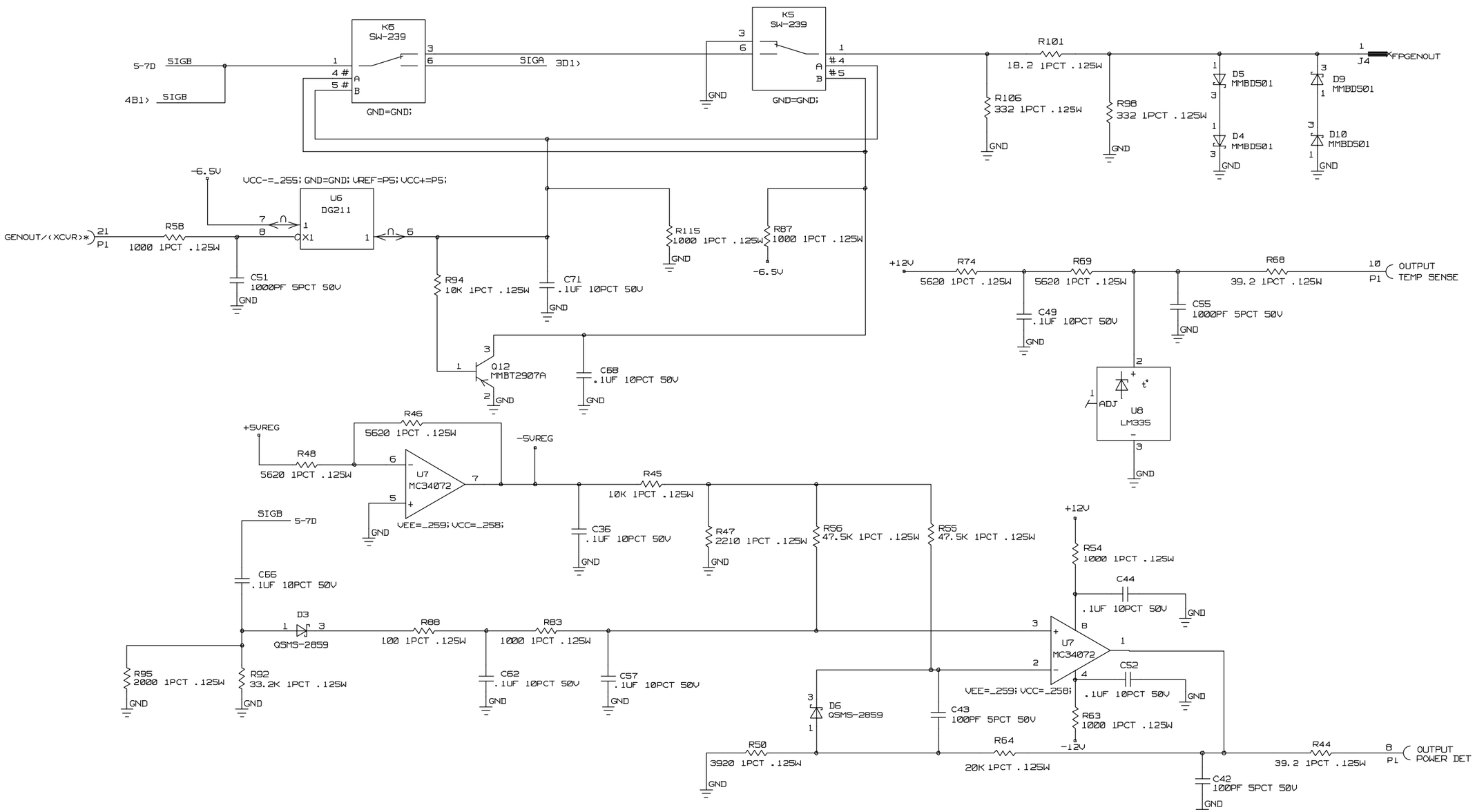




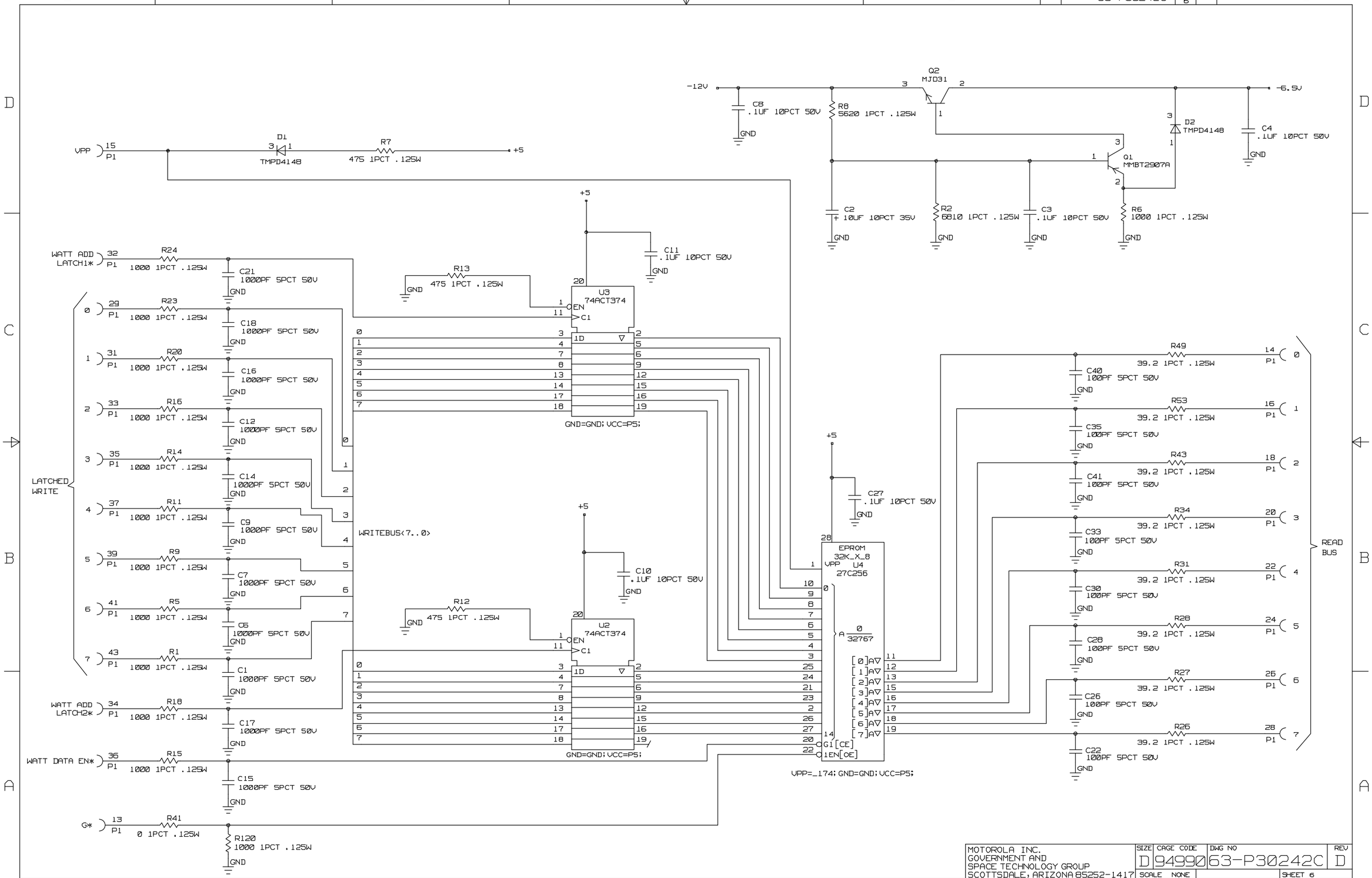
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30242C	REV D
	SCALE NONE			SHEET 2


DWG NO 63-P30242C SH 3
R112 51.1 1PCT .250W
R109 15 1PCT .125W
R113 15 1PCT .125W
R114 100 1PCT .125W
J3 CALRF
C70 .1UF 10PCT 50V
R108 51.1 1PCT .250W
D8 QSMS-2859
R111 51.1 1PCT .250W
GND
U12
58-P30247C001
NOTE: GRAPHICAL DATA ONLY.
J1
-5VREG
R80 10K 1PCT .125W
C54 .1UF 10PCT 50V
R77 2210 1PCT .125W
R119 33.2K 1PCT .125W
R117 18.2K 1PCT .125W
R104 15 1PCT .125W
R118 75 1PCT .125W
R107 75 1PCT .125W
R105 150 1PCT.125W
SIGA 5D6>
R103 68.1 1PCT .125W
R100 68.1 1PCT .125W
R110 22.1 1PCT .125W
+12V
R97 1000 1PCT .125W
C67 .1UF 10PCT 50V
R116 1000 1PCT .125W
C74 1000PF 5PCT 50V
C73 1000PF 5PCT 50V
U11 MC34072
VEE=_252; VCC=_253;
R89 47.5K 1PCT .125W
C69 .1UF 10PCT 50V
R102 1000 1PCT .125W
-12V
C72 1000PF 5PCT 50V
D7 QSMS-2859
C65 100PF 5PCT 50V
U6 DG211
C75 100PF 5PCT 50V
R90 47.5K 1PCT .125W
VCC-=_255; GND=GND; VREF=P5; VCC+=P5;
INPUT-DET GAIN*
R99 5620 1PCT .125W
R91 2000 1PCT .125W
R93 26.7K 1PCT .125W
R65 5620 1PCT .125W
C48 100PF 5PCT 50V
R67 39.2 1PCT .125W
INPUT POWER DET
R81 3320 1PCT .125W
R85 100 1PCT .125W
C59 .1UF 10PCT 50V
R78 3320 1PCT .125W
R79 5620 1PCT .125W
C63 .1UF 10PCT 50V
C60 1000PF 5PCT 50V
U9 MC34072
R96 5620 1PCT .125W
R52 39.2 1PCT .125W
OVERTEMP
R86 3920 1PCT .125W
C64 1000PF 5PCT 50V
VEE=GND; VCC=_251;
R76 10K 1PCT .125W
R82 5620 1PCT .125W
R84 5620 1PCT .125W
R75 1000 1PCT .125W
C56 .1UF 10PCT 50V
U10 LM335
ADJ
C46 1000PF 5PCT 50V
R59 39.2 1PCT .125W
INPUT TEMP SENSE
C5 .1UF 10PCT 50V
P1
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D CAGE CODE 94990 DWG NO 63-P30242C REV D
SCALE NONE SHEET 3


DWG NO 63-P30242C SH 4
NOTE: GRAPHICAL DATA ONLY
GENOUT
J2
L1 15X385
L2 15X50
L3 15X600
L4 15X120
L5 15X490
C13 3.3PF 5PCT 50V
C20 3.3PF 5PCT 50V
C25 3.3PF 5PCT 50V
K1 SW-239
GND=GND;
R33 332 1PCT .125W
R30 56.2 1PCT .125W
R40 56.2 1PCT .125W
K2 SW-239
GND=GND;
VCC-=_255; GND=GND; VREF=P5; VCC+=P5;
U6 DG211
OUTPUT ATTEN 2*
P1
R37 1000 1PCT .125W
C38 1000PF 5PCT 50V
R39 10K 1PCT .125W
C31 .1UF 10PCT 50V
R35 1000 1PCT .125W
R42 1000 1PCT .125W
-6.5V
Q10 MMBT2907A
C29 .1UF 10PCT 50V
+12V
U5 LM317
IN
OUT
ADJ
C24 .1UF 10PCT 50V
+5VREG
C47 .1UF 10PCT 50V
R29 221 1PCT .125W
R32 681 1PCT .125W
R38 22.1K 1PCT .125W
R3 100 1PCT .125W
C19 10UF 10PCT 35V
R4 22.1 1PCT .125W
C76 33UF 20PCT 25V
Q6 MMBT2222A
Q4 MMBT2907A
Q5 MMBT2907A
Q3 MMBT2907A
U1 LM335
ADJ
R10 332 1PCT .125W
R21 22.1 1PCT .125W
R25 1000 30PCT .200W
L6 15X400
C32 1000PF 5PCT 50V
C77 10UF 10PCT 35V
R17 2210 1PCT .125W
Q7 MMBT2907A
Q8 MMBT2907A
R22 3320 1PCT .125W
Q9 MMBT2907A
R19 2670 1PCT .125W
R73 332 1PCT .125W
R71 332 1PCT .125W
R66 332 1PCT .125W
R61 475 1PCT .125W
R62 10 1PCT .125W
R51 475 1PCT .125W
C39 .1UF 10PCT 50V
K3 SW-239
GND=GND;
AR1 UPC167B
2,3,4,6,7
GND=GND; VCC=P5VREG;
C53 .1UF 10PCT 50V
K4 SW-239
GND=GND;
SIGB
+5
C45 .1UF 10PCT 50V
U6 DG211
OUTPUT AMP 1*
P1
R36 1000 1PCT .125W
VCC-=_255; GND=GND; VREF=P5; VCC+=P5;
C34 1000PF 5PCT 50V
C37 .1UF 10PCT 50V
R57 1000 1PCT .125W
-12V
R70 10K 1PCT .125W
C61 .1UF 10PCT 50V
Q11 MMBT2907A
C58 .1UF 10PCT 50V
R72 1000 1PCT .125W
R60 1000 1PCT .125W
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D
CAGE CODE 94990
DWG NO 63-P30242C
REV D
SCALE NONE
SHEET 4



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30242C	REV D
	SCALE NONE		SHEET 5	



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE	CAGE CODE	DWG NO	REV
	D	94990	63-P30242C	D
	SCALE NONE		SHEET 6	

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Return to Section 12

Go to Section 14

13.1 GENERAL DESCRIPTION

The Interface Module (A12) is installed outside the RF cardcage, but connected to the RF Motherboard that is common to other modules inside the RF cardcage.

The Interface Module provides the interface between the RF modules and the Processor Module and functions as the source of DAC outputs to RF modules and all A/D inputs. It also interfaces with the front panel audio signals.

The Interface Module functions are.

- Output control latches for RF system
- Sweep generation
- Microphone interface
- Front panel interface to ports
- Counter interface
- DVM
- 8 bit A/D for scope displays
- 12 bit A/D for more accurate readings
- Trigger control and vertical positioning for scope
- DVM multiplexing
- Attenuation and amplification for A/D conversion
- Peak detection
- Rectification and filtering
- 1KHz notch filtering
- RMS to DC conversion

13.2 SIGNALS SUMMARY

The signals to/from the Interface Module appear here organized in alphabetical order for each connector. Where signals are routed through this module to another connector they are noted as such.

Some signals described here are not used. These are included because of their potential use in future product development.

13.2A Interface Module Signal Descriptions

13.2A.1 P1 (RF Motherboard)

AUDIO LPF 1-2 and *AUDIO HPF 1-2* outputs to the Receiver Module select the desired audio highpass filter (5Hz, 300Hz, 3KHz) and audio lowpass filter (20KHz, 3KHz, 300Hz).

BFO FREQ, BFO TUNE: These signals are not used in the basic Analyzer at this time.

*CAL LATCH 1-2** outputs to the RF Output Module calibrate the output level in the generate path.

*CAL RF/(ANT)** output data line enables either the CAL RF or ANT path (NOTE: this signal is documented as "CAL RF ENABLE at the RF Input Module)

DEMOD CAL AUDIO input from the Receiver Module is the unsquelched demodulated audio signal. The Interface Module does not use this signal and only provides the connection for it from P1 to J2.

*GEN HI/(LO)** output to the Generator enables switching between two VCO bands (<=310.7MHz or >310.7MHz IF frequency).

*GEN OUT/(XCVR)** output is used to enable or disable RF Switches. At The RF Wattmeter, a logic 0 enables the RF I/O port as an output while a logic 1 enables FP Gen Out as an output.

GEN SYNTH DATA output to the Generator Module is the data line for programming the generate synthesizer loops.

HI SYNTH DATA output is the serial data line used to program the High Synthesizer loops (in conjunction with SYNTH CLOCK and SYNTH LATCH).

IF OVERLOAD input from the Receiver Module is not used in the current Analyzer version.

*INPUT ATTEN 1-2** outputs are used to switch attenuation in/out on the RF Input Module.

*INPUT DET GAIN** output to the RF Wattmeter is used to switch in additional amplification at low input power levels.

INPUT POWER DET is a 0 to +5VDC input from the RF Wattmeter that is proportional to the wattmeter's RF Power Level Input.

INPUT TEMP SENSE is a 0 to +5VDC input from the RF Wattmeter that is proportional to the temperature of the wattmeter's input power detector.

LATCHED WRITE 0-7 outputs are used as data lines to write data to the Spectrum Analyzer, RF Output, and RF Wattmeter modules.

LIM 700 KHz input is the limited output of the 700KHz IF at the Receiver Module and is used for frequency error measurement.

LO SYNTH DATA 1-4 These four outputs are used as serial data lines for programming the Low Synthesizer loops 1-4. These outputs are used with SYNTH CLOCK and SYNTH LATCH.

MOD SEL 1-2 output lines select the Generators mode of operation and modulation type (AM, FM, or CW). The MOD SEL 2 signal is used in the Receiver Module to select the receive modulation type (AM or FM).

MOD CAL AUDIO output is routed to P1 (RF Motherboard), oscilloscope circuitry, peak detectors, MOD OUT TO FP, and a selectable amplifier for NB/WB. GEN AUDIO from the Processor Module is capacitively coupled (to eliminate offset voltage) and buffered to create MOD CAL AUDIO.

*OUTPUT AMP 1** output to the RF Wattmeter is used to enable an 18.5dB amplifier stage in the generate path.

*OUTPUT ATTEN 1** output enables or disables a 20dB attenuator in the 310.7MHz path of the RF Output Module.

*OUTPUT ATTEN 2** output is used to insert 22.5dB attenuator into the generate path of the RF Wattmeter.

OUTPUT POWER DET is a 0 to +5VDC input from the RF Wattmeter that is proportional to the RF Power Level output.

OUTPUT TEMP SENSE is a 0 to +5VDC input from the RF Wattmeter that is proportional to the temperature of the Output Power Detector.

OVERTEMP input from the RF Wattmeter indicates when the temperature of the receive input power detector is over a specified level. A logic 1 indicates an over temperature condition.

RCV SPEAKER AUDIO input is the squelched unfiltered demodulated audio from the Receiver Module. The Interface Module does not use this signal, but only acts as the connection for it from P1 to J2.

READ BUS 0-7 inputs are data lines from the RF Wattmeter's EPROM.

SA BW1 & 2 outputs are used to select one of two Spectrum Analyzer bandwidths: 6KHz or 30KHz.

*SA CAL LATCH** output is used to latch data into the Spectrum Analyzer Calibration Level DAC and latch.

SA SWEEP WIDTH 1-4 outputs select the sweep width in Spectrum Analyzer and Sweep Generator modes.

SA SYNTH DATA output is used as the data line for the Spectrum Analyzer's synthesizer. It is used in conjunction with SYNTH CLOCK and SYNTH LATCH.

SA TEMP SENSE input from the Spectrum Analyzer is a 0 to +5VDC level that is proportional to the temperature of the SA's log amp.

SCAN LOCK FREQ from the Spectrum Analyzer Module is the limited output of the SA's 21.4MHz signal divided down. This signal is used for the scan lock function.

SIG STRENGTH input from the Spectrum Analyzer Module is a 0 to +5VDC voltage that is proportional to the strength of the signal present at the RF Input Module's 310.7MHz SA IF line.

SPLITBAND* This signal is not used in the basic analyzer at this time.

SQUELCH input at P1 is generated by the Receiver Module and indicates whether the receiver is squelched. The Interface Module also routes this signal to J2 for the Processor Module.

SQUELCH LEVEL output to P1 The Interface Module does not use this signal and only acts as a connection for it from J2 to P1.

SQUELCHED DEMOD input from the Receiver Module is a squelched version of the demodulated receive signal (Demod Cal Audio). The Interface Module uses this signal in the DVM-To-Range Input MUX and also routes this signal from P1 to J2 for the Processor Module.

SWEEP output sweeps the Spectrum Analyzer VCO during SA and Sweep Generate functions. It is a digitally stepped sawtooth waveform.

SWEEP EN (Sweep Enable) output enables/disables the sweep of Spectrum Analyzer or Sweep Generator modes.

SYNTH CLOCK output is used to clock data into the Low Synthesizer, High Synthesizer, Generator, and Spectrum Analyzer Modules.

SYNTH LATCH output is used to latch the data serially clocked by SYNTH CLOCK.

TRACKING GEN output is used to enable the tracking generator function on the Generator Module.

*VERNIER LATCH 1-2** outputs to the RF Output Module fine tune the output level to finer steps. Each output clocks the data from LATCHED WRITE 0-7 into a latch and 8-bit DAC on the RF Output Module.

*WATT DATA EN** output latches data from the RF Wattmeter Module EPROM into READ BUS 0-7.

*WATT ADD LATCH 1-2** outputs are used to enable the latches that address the RF Wattmeter EPROM. WATT ADD LATCH l* addresses the eight least significant bits and WATT ADD LATCH 2* addresses the seven most significant bits (15 bits total to address the 32K EPROM).

*WB/(NB)** output signal to the Receiver Module and Generator Module selects wideband or narrowband mode and is used by the Interface Module during generation of the MOD OUT TO FP signal. The WB/(NB)* signal is also routed to J2 for the Processor Module.

1500 PLL DATA output is a serial data line for programming the 1500MHz PLL at the High Synthesizer Module.

+5V, -5V, +12V, and -12V supply power to this module.

13.2A.2 J1 (to/from Processor Modulo)

*A/D BUSY** output is used at the Interface Decode Module to generate a DTACK to the processor.

*ATTEN CS** input selects RF Atten latch U75.

*AUDIO FILTER CS** input selects Audio Filter Linearizer latch U79.

BD0 - BD15 are buffered inputs/outputs of the processor data bus.

*BFO CS** input is reserved for possible use in future product development. If used, this signal will select DAC latch U50.

COUNTER output is used at the Processor Module for both the frequency and period counters.

*DVM ATTEN CS** input selects DVM/Atten latch U19.

*DVM SEL CS** input selects DVM Select latch U17.

OPT to COUNTER is not used at this time, but is reserved for possible use in future product development.

*READ SPARE 1&2 CS** inputs axe not used at this time, but are reserved for possible use in future product development.

*RF I/O 2** input is a chip select for the 12-bit A/D.

*RF MODE** input selects RF Mode latch U78.

*RF OUTPUT CS** input selects RF Output latch U76.

*RF READ CS** input selects U62 to allow the processor to read BD 0-7 of the bi-directional data bus.

*RF STATUS CS** input selects U63 to allow the processor to read the state of some RF indications.

*SA CONTROL CS** input selects SA Control latch U74.

*SCOPE ATTEN CS** input selects Scope Atten latch U20.

*SCOPE CS** input selects Scope/PK Det/Counter latch U18.

*STATIC BUS CS** input selects Static Bus latch U64.

*SYNTH CS** input selects the Synth Program latch U65.

*TRIG CS** input selects U52 to latch the upper data bus to D/A converter U39 (provides a trigger voltage level for scope functions).

V BACKUP is the backup voltage to be used by the Analyzer system. When power is on, this line will be the +5V power supply When power is off, this line will be the battery voltage. It is not used by the Interface Module at this time.

*VERT CS** input selects Vertical Position latch U51.

*WRITE BUS CS** input selects RF Static Output latch U77.

+5VDC supplies power to the Interface Decode Module.

13.2A.3 J2 (to/from Processor Module)

A/D DATA 0-7 outputs to the ASIC on the Processor Module are the result of the 8 bit A/D conversion performed for oscilloscope functions.

DC INPUT + input signal is the positive voltage of the external DC Input to the power supply.

DEMOD CAL AUDIO output is the unsquelched demodulated audio signal from the Receiver Module at P1. The Interface Module does not use this signal and only provides the connection for it from P1 to J2.

DVM output is a buffered version of the input to the 12 bit A/D converter.

DVM FROM RANGE output is the attenuated or amplified A/D signal.

EXT MOD IN output is created by amplifying and buffering the FP EXT MOD IN signal from the front panel.

EXT MOD + MIC IN output is the sum of the External Modulation Input and the Microphone Input from the front Panel.

GEN AUDIO input is the calibrated sum of all the audio modulation to be routed to the synthesizer. The Interface Module uses it to create the MOD CAL AUDIO output signal.

HANDSET AUDIO output: The Interface Module does not use this signal, but only acts as the connection for it from J3 to J2.

INT MOD input is the sum of all the Processor Module's internally generated modulation signals including tone or PL, DPL, 1KHz, and DTMF. INT MOD is not used by the Interface Module at this time. This signal is used at the Processor Module during creation of the GEN AUDIO signal.

IACK 1-2, IACK 4-7** inputs indicate an interrupt acknowledge cycle has been issued from the processor These lines are used in conjunction with IRQ 1-7. They are not currently used by the Interface Module.

IRQ 1-2/IRQ 4-7** (interrupt Request) outputs are used as interrupt signals to the MC68000 processor. They are not currently used by the Interface Module.

MIC IN output is created by filtering and amplifying the FP MIC IN signal from the front panel.

RAW MIC output is a buffered version of the FP MIC IN signal.

RCV SPEAKER AUDIO output is the squelched unfiltered demodulated audio from the Receiver Module at P1. The Interface Module does not use this signal, but only acts as the connection for it from P1 to, J2.

*RESET** input indicates that the processor system has been reset. It is not used by the Interface Module.

SAMPLE CLOCK input signal is used to control the data conversion cycles of the 8 bit A/D converter.

SQUELCH output is generated by the Receiver Module and indicates whether the receiver is squelched. The Interface Module also routes this signal from P1 to J2.

SQUELCH LEVEL input is not used on this module. The Interface Module only acts as a connection for it from J2 to P1.

SQUELCHED DEMOD output to the Processor Module is a squelched version of the demodulated receive signal (Demod Cal Audio) from the Receiver Module at P1. The Interface Module uses this signal in the DVM-To-Range input MUX and also routes this signal from P1 to J2 for the Processor Module.

SYSCLK is the 10MHz system clock from the Processor Module. The signal is buffered to create BSYSCLK for other digital timing on the Interface Module.

TIMER CLOCK input is a clock of varying frequency (76Hz to 5MHz). The Interface Module uses this to produce the SWEEP signal at P1.

TRIGGER output signals the ASIC when to start auto sampling the A/D DATA 0-7 signals for oscilloscope functions.

VOL CNTL AUDIO input is the sum of the received or transmitted modulation. It is not used by the Interface Module.

OPT FLASH UNLOCK, Flash Memory, +12Volts for boot sector unlock on option modules. Not used by the Interface Module.

*WB/(NB)** output indicates wideband or narrowband, operation to the Processor Module at J2 and appears at P1 to select wideband or narrowband modes at the Receiver Module and Generator Module. It is also used by the Interface Module during generation of the MOD OUT TO FP signal.

13.2A.4 J3 (to/from Front Panel)

DEMOD OUT TO FP output to the front panel DEMOD OUT connector is created using the SQUELCHED DEMOD signal.

FP EXT MOD IN input is the signal from the front panel EXT MOD IN connector.

FP MIC IN is the microphone input from the front panel. This input is compatible with a Motorola HMN-1056C. This signal is used to create the MIC IN output to the Processor Module.

HANDSET AUDIO input: The Interface Module does not use this signal, but only acts as the connection for it from J3 (Front Panel) to J2 (Processor Module).

MOD OUT TO FP output to the front panel MOD OUT connector is a buffered and amplified version of MOD CAL AUDIO.

PTT is the Push-To-Talk input from the front panel handset connector that indicates when the microphone has been keyed.

13.2A.5 J4 (METER IN from Front Panel)

METER IN from BNC connector at front panel is an input signal to the Spectrum Analyzer, Oscilloscope, DVM, SINAD/Distortion Meter, and the Freq/Period Counter (depending upon which function is selected).

13.2B Interface Module Connector Descriptions

In all of the following connector descriptions the bullet symbol (•) is used to indicate signals that are spares, or reserved for possible use in future product development.

13.2B.1 P1 (120-Pin Edge Conn. to RF Motherboard)

pin	
1,2	GND
3,4	+5V
5,6	-5V
7,8	not used by this module
9	Input Pwr Det
10	Output Pwr Det
11	Input Temp Sense
12	Output Temp Sense
13,14	not used by this module
15	SA BW 1
16	Read Bus 0
17	SA BW 2
18	Read Bus 1
19	SA Sweep Width 1
20	Read Bus 2
21	SA Sweep Width 2
22	Read Bus 3
23	SA Sweep Width 3
24	Read Bus 4
25	SA Sweep Width 4
26	Read Bus 5
27	SA Spare 3 •
28	Read Bus 6
29	SA CAL Latch*
30	Read Bus 7
31	IF Overload
32	Overtemp
33	Squelch
34	Output Atten 1*
35	Output Atten 2*
36	Output Amp 1*
37	Spare •
38	Input Atten 1
39	Input Atten 2
40	RF Atten Spare 2 •
41	RF Atten Spare 1 •
42	Watt ADD Latch 1*
43	Watt ADD Latch 2*
44	Watt Data EN*
45	Read Spare •
46	Vernier Latch 1*
47	Read Spare 2 •
48	Vernier Latch 2*
49	Sweep EN
50	CAL Latch 1
51	Spare Bus •
52	Cal Latch 2*
53	RF Output Spare 1•
54	GEN OUT/(XCVR)*
55	1500 PLL Data
56	CAL RF/(ANT)*
57	Input DET Gain*

58	Tracking Gen
59	Latched Write 0
60	Synth Clock
61	Latched Write I
62	Synth Latch
63	Latched Write 2
64	Gen Synth Data
65	Latched Write 3
66	LO Synth Data 1
67	Latched Write 4
68	LO Synth Data 2
69	Latched Write 5
70	LO Synth Data 3
71	Latched Write 6
72	LO Synth Data 4
73	Latched Write 7
74	HI Synth Data
75	SA Spare I •
76	SA Spare 2 •
77	SA Synth Data
78	WB/(NB)*
79	Splitband •
80	Mod Sel 1
81	ModSel2
82	Gen HI/(LO)*
83	LIM 700KHz
84	Scan Lock Freq
85	BFO Freq •
86	Audio FIL/LIN Spare •
87	Spare •
88	GEN LIN 1
89	GEN LIN2
90	Audio HPF 1
91	Audio HPF 2
92	Audio LPF 1
93	Audio LPF 2
94	Squelch Level
95	RCV Speaker Audio
96	SA Temp Sense
97	not used by this module
98	BFO Tune •
99	SWEEP
100,101	not used by this module
102	SIG Strength
103,104	not used by this module
105	SA DVM Spare •
106	not used by this module
107	Squelched Demod
108	Demod Cal Audio
109,110	not used by this module
111	Mod Cal Audio
112-114	not used by this module
115,116	-12V
117,118	+12V
119,120	GND

13.2B.2 J1 (60-Pin Card Edge Connector)

pin	
1,2	+5VDC output
3	V Backup (backup voltage) •
4-19	BD0-BD15 (buffered bi-directional data lines)
20	GND
21	GND
22	ATTEN CS*
23	RF MODE CS*
24	RF OUTPUT CS*
25	STATIC BUS CS*
26	SA CONTROL CS*
27	WRITE BUS CS*
28	SYNTH CS*
29	GND
30	GND
31	AUDIO FILTER CS*
32	OUTPUT SPARE CS*
33	BFO CS* •
34	VERT CS*
35	TRIG CS*
36	DVM SEL CS*
37	SCOPE CS*
38	DVM ATTEN CS*
39	SCOPE ATTEN CS*
40	RF STATUS CS*
41	RF READ CS*
42	12-Bit A/D BUSY*
43-49	not used
50	READ SPARE 1 CS* •
51	READ SPARE 2 CS* •
52-54	not used
55	RFI/O 2*
56	COUNTER
57	Option to COUNTER •
58-60	not used

13.2B.3 J2 (60-Pin Card Edge Connector)

pin	
1	DVM (12-bit DVM Sel output)
2	GND
3	GEN AUDIO (generator audio)
4	GND
5	OPT to DVM •
6	WB/(NB)* (wideband/narrowband select)
7	DVM From Range
8	GND
9	EXT MOD + MIC IN
10	GND
11	Handset Audio
12	RAWMIC
13	RCV Speaker Audio
14	GND
15	DEMOD CAL AUDIO (demodulated calibrated audio)

16	DC Input + (DC input positive voltage)
17	MIC IN (output to processor module)
18	EXT MOD IN (external modulation input)
19	SQUELCH LEVEL
20	INT MOD (internal modulation) •
21	RESET* •
22	Squelched Demod
23	GND
24	VOL CNTL Audio •
25	GND
26	SYSCLK
27	GND
28	not used by this module
29-32	OPT MOD RTN 1-4 •
33	GND
34	IRQ1* (interrupt request level 1) •
35	IRQ2* (interrupt request level 2) •
36	Squelch
37	IRQ4 (Interrupt request level 4) •
38	IRQ5* (interrupt request level 5) •
39	IRQ6* (Interrupt request level 6) •
40	IRQ7* (interrupt request level 7) •
41	Timer Clock (genl purpose timer clock input)
42-49	A/D Data 7-0
50	IACIK7* (interrupt acknowledge 7) •
51	IACK6* (interrupt acknowledge 6) •
52	IACK5* (interrupt acknowledge 5) •
53	IACK4 (interrupt acknowledge 4) •
54	IACK2* (interrupt acknowledge 2) •
55	IACK1* (interrupt acknowledge 1) •
56	Trigger (A/D trigger)
57	CND
58	Sample Clock (for A/D sampling)
59	GND
60	OPT FLASH UNLOCK

13.2B.4 J3 (8-Pin Header Conn. to Frt Panel BNCs)

pin

1 FP MIC IN (microphone input)
Compatible with Motorola HMN-1056C

2 FP EXr MOD IN (external modulation input)
V[in]: 0 to 1V max
Input Freq: 5Hz to 20KHz
Input Impedance: 600Ω

3 MOD OUT TO FP (modulation output)
Output Level: 0 to ±8V max into open circuit
Dev Output:
12.5KHz/V pk in wideband FM
1.25KHz /V pk in narrowband FM
12.5%/V in AM
Output Impedance: 100Ω nominal

4 DEMOD OUT TO FP (demodulated audio out)
Same specifications as pin 3, Mod Out to FP

5 PTT (push-to-talk)

6 GND

7 HandsetAudio
Routed from J2-2 to J3-7 without modification

8 GND

13.2B.5 J4 (Metering Input from Front Panel)

Input Voltage: +100V max
Input Impedance: 1MΩ±1%
Shunt: 60pf ±5%

Other specifications at J4 vary depending upon the metering mode selected.

13.3 BLOCK DIAGRAM DESCRIPTION

The Interface Module is the interface between the Processor Module (J1/J2), modules found in the RF cardcage (P1), and front panel signals J3/J4).

The Interface Module can functionally be divided into two major areas: 1) decoding of processor data from the Processor Module and 2) providing A/D conversion for oscilloscope and metering input functions.

This module is also assigned to other tasks where an interface is required between the Processor and RF modules or the Processor and external ports. Some examples are: 1) providing microphone and external modulation inputs to the Processor Module, 2) interfacing Processor Module signals to produce the SWEEP output, and 3) routing signals to/from the Processor Module and other modules without modifying these signals in any way.

13.3.1 Processor Data Decoding

Most processor control of modules in the RF cardcage is accomplished through the Interface Module latches. The Processor Module buffers address lines A8 - All, the address strobe, upper and lower data strobes, and I/O read and write lines. These signals enable decode blocks that control output latches on the Interface Module. Some of the latched outputs are sent directly to P1 (RF Motherboard). Other decoded and latched signals are intended only for the Interface Modules own internal use.

13.3.2 Scope/DVM Block

The METERING IN port at the front panel is used for the oscilloscope, SINAD meter, DVM, and distortion meter in the Scope/DVM block.

The Scope/DVM block includes input buffers and ranging. During scope functions the Scope/DVM block allows for AC or DC coupling selectable by the processor. In the DVM mode the Scope/DVM block allows DC or RMS voltages to be measured, selected by the processor.

The block has two A/D converters. One is an 8 bit A/D for scope data acquisition and the other is a 12 bit A/D for general purpose requirements.

Hex I/O Device	Address
**Sweep Atten DAC	6000
Synth Prog Latch	6001
**BFO DAC	6100
RF Static Output Latch	6101
Vertical Position Latch	6200
RF Attenuation Latch	6201
Trigger DAC	6300
RF Mode Latch	6301
DVM Select Latch	6400
RF Output Latch	6401
Scope/PK/CNTR/Latch	6500
Static Bus Latch	6501
DVM/Atten Latch	6600
SA Control Latch	6601
Scope Atten Latch	6700
Audio Filter/LIN Latch	6701
RF/pk det/DVM Status	6801
RF Read Bus	6901
12-bit A/D	

** Not used in current Analyzer version

Figure 13A.1.1 Interface Module I/O Addresses

13.4 DETAILED DESCRIPTION

13.4.1 Basic Processor Interface

Figure 13.4.1.1 shows the addresses used by the Processor Module to select I/O devices located at the Interface Module during processor read and write cycles. All devices in the address range from 6000 to 67FF are output devices (for control) that appear in more detail in figure 13.4.1.2. Addresses 6801, 6901, and 7000-7001 are assigned to input devices used by the processor to read information.

Address decoding is performed by the processor module. The chip select signals are routed to the I/O devices located on the Interface Module.

RF I/O 2* is also routed to the Interface Module where it is used to enable the 12-bit A/D converter U80.

13.4.1.1 Output Latches

Figure 13 4.1.2 summarizes the output signals for each output device selection appearing in figure 13.4.1.1.

13.4.2 Read/Write Operations

13.4.2.1 Write Operation

When the processor performs a write operation, address lines A8-All, control lines RF I/O 1*, LDS*, UDS*, I/O WR*, and R/(W)* are all used at the Processor Module to decode data lines D0-D7 (with LDS*) and D8-D15 (with UDS*).

Decode blocks at the Processor Module decode the processor data to enable/disable Interface Module output latches and D/A converters. Some of these decoded control signals are also sent to the RF Motherboard (via Interface Module) without modification.

Another decode block (at Processor Module) decodes processor data to enable/disable Interface Module input latches and A/D converters in preparation for a processor read. This is performed by the processor while handling a DTACK from the Interface Module's A/D converter (see par 13-4.2.2)

13.4.2.2 Read Operation

The Interface Module's 12 bit A/D converter output BUSY is used at the Processor Module to generate a DTACK to the processor with the proper delay in order to guarantee the validity of the A/D data.

I/O RD* in conjunction with A8-A11, LDS*, RF I/O 1* determine (at the Processor Module) when data lines at the Interface Module on buffer U63 are written to the data bus by U62 during the processor read.

13.4.3 Modulation

13.4.3.1 External Modulation

External modulation from the front panel is summed and amplified with the microphone signal at U1A, prior to being routed to the Processor Module via connector J2. NOTE: The EXT MOD IN+MIC IN output signal is inverted 180° from either FP MIC IN or FP EXT MOD IN inputs.

Microphone amplifier and filtering circuitry is provided on the Interface Module. The microphone is powered by a filtered +9.3 Vdc supplied by zener diode D1 and transistor Q1. The audio signal is put through Instantaneous Deviation Control (IDC) and splatter filtering provided by U9 and U1, respectively. These filters provide bandpass; filtering (f_c = 3KHz) that limits the signal to a level corresponding to 10 KHz in narrow band, and 100KHz in wide band.

IDC FILTER

Type: Bandpass
Center Freq: 3KHz ±500Hz
Highpass: 18dB min atten at 300Hz
Lowpass: 28dB min atten at 20KHz

13.4.3.2 Other Modulation

GEN AUDIO (connector J2) is the processor-switched signal used for modulation in the Generate mode. On the Interface Module, this signal is capacitively coupled (to eliminate offset voltage), and buffered by U49 to become MOD CAL AUDIO.

MOD CAL AUDIO is routed to several places, including: mod scope (via U32); peak detectors (via U47); RF Motherboard connector P1; and a selectable x.l/xl amplifier (U10A) for NB/WB (respectively) operation. This output (MOD OUT TO FP) is buffered for the front panel by U10B and a push-pull amplifier comprised of Q2 and Q4, which are short-circuit protected.

13.4.4 Demodulation

SQUELCHED DEMOD (connector PI) is the demodulated signal from the Receiver module that is under squelch control. It is routed on the Interface module to the following, mod scope (via U32); peak detectors (via U47), Processor Module (via J2); and to a push-pull amplifier comprised of Q3 and Q5 which buffers SQUELCHED DEMOD for the front panel to become DEMOD OUT TO FP This output, as with MOD OUT TO FP, can withstand a short-circuited output indefinitely.

13.4.5 Peak Detectors

The Interface Module has positive and negative peak detectors, which can write simultaneously. The peak detectors have the ability to reset the peak value for both detectors simultaneously to 0V using a processor controlled signal. Specifications for the peak detectors are as follows:

Input level: 0.0 to ±8.0V pk
Input level: 5Hz to 20KHz
Output Accuracy: ±1.0% (all levels and frequencies)
Attack time: within ±1% of final level within 10µsecs of a step level change.
Decay time: output decays no more than 63% from its original value within 800msecs of a step level change without a processor reset of the detectors.
Input Coupling: AC coupled at the input with a single pole no greater than 0.5Hz.

Modulation signals requiring peak detection are selected by multiplexer U47 as inputs to positive and negative peak detector circuits (U45, U55). The circuits are configured for "ideal diode" operation to charge up capacitors to the peak level (D8, D10, C113, C129).

Feedback diodes (D7, D9) hold the output of the op-amps to within 0.6V of the input in order to avoid slew rate problems. The reset function is achieved by shorting the rectifying diodes to convert the circuits to followers. The negative peak value is inverted (U56) in order to be readby the 12 bit A/D.

13.4.6 Scope/DVM Block

The DVM block includes input buffers and ranging. The block has two A/Ds: one 12-bit A/D for general purpose requirements, and one 8-bit A/D for scope data acquisition. The 12-bit A/D is microprocessor controlled and directly readable. The 8-bit A/D is controlled by hardware external to the Interface module.

13.4.6.1 DVM

The Interface Module can measure both DC and RMS voltages, selectable from the processor, and from the METER INPUT when operating in the DVM mode. The DVM has the following specifications for AC and DC digital voltmeter.

AC MODE

Crest Factor: True RMS measured with a maximum crest factor of four.
Freq Range: 50Hz to 20KHz
Accuracy: ±5% of full scale ±1 LSB (1.0V, 10.0V, and 70Vrms scales)

DC MODE

Input Voltage: ±100V maximum
Accuracy: ±5% of fall scale ±1 LSB (1.0V, 10.0V, and 100.0V scales).

13.4.6.2 12-Bit A/D

The 12-Bit A/D is used to take general readings for calibration, power, DVM, and SINAD. The analog input to the A/D is adjustable using the input attenuator. The 12-Bit A/D has the following specifications:

Conversion Time: 100usec max
Resolution: 12 bits
Linearity: plus or minus 1bit
Input Voltage Range: 0 to +5V where 0V=000 and 5V=FFF
Digital Interface: compatible with MC68000

The DVM 12-bit A/D converter clock frequency is 1.25 MHz divided down from the 10 MHz SYSCLK frequency by U66. Offset (R188) and gain (R259) control are provided by buffer U72.

U17, DVM Select Latch

Output	Pin(s)
RF DVM Sel 1-3	9,15,2
DVM Sel 1-3	19,6,12
DVW(Dist)*	5
Dist X1 (X10)*	16

U18, Scope/PK Det/Counter Latch

Output	Pin(s)
Scope AC/(DC)*	6
Dist x8*	12
Counter Sel 1-3	9,15,2
Trig Disable	5
Peak Reset*	19
Sweep Reset	16

U19, DVM/Atten Latch

Output	Pin(s)
DVM to Range Sel 1-3	9,15,2
DVM AC/DC	5
DVM Gain x5	6
DVIVI Gain x1 0	12
DVM Int/Ext	16
DVM Atten Div/2	19

U20, Scope Atten Latch

Output	Pin(s)
Scope Sel 1-3	9,15,2
Scope Atten Div 10*	19
Scope Gain x2*	6
Scope Gain x5*	12
Scope Gainl x10*	5
Scope Gain2 x10*	16

U50, DAC Latch

Interfaces upper data bus (BD8-BD15) to D/A converter U37 for possible use in future product development

U51, Vertical Position Latch

Interfaces upper data bus (BD8-BD15) to D/A converter U38 to provide a vertical position voltage for scope functions.

U52, Trigger DAC

Interfaces upper data bus (BD8-BD15) to D/A converter U39 to provide a trigger voltage level for scope functions.

U64, Static Bus Latch

Output	Pin(s)
Watt Data EN	6
Watt Add Latch 1-2	2,9
Vernier Latch 1-2	5,19
Cal Latch 1-2	16,15
Unused	12

U65, Synth Program Latch

Output	Pin(s)
Synth Clock	2
Synth Latch	9
Gen synth Data	6
Lo Synth Data 1-4	5,19,16,15
Hi Synth Data	12

U74, SA Control Latch

Output	Pin(s)
SA Sweep Width 1-4	6,5,19,16
SA BW 1-2	2,9
SA CAL Latch	12
SA Spare 3	15

U75, RF Atten Latch

Output	Pin(s)
Output Atten 1-3*	2,9,6
Input Aften 1-2	19,16
RF Aften Spare 1-2	12,15
Spare	5

U76, RIF Output Latch

Output	Pin(s)
Input Det Gain*	15
Gen Outl(RF I/O)*	5
CAL RF/(ANT)*	16
Sweep EN	2
1500 PLL Data	19
Spare	12
RF Output Spare 1	6
Spare Bus	9

U77, RF Static Output Latch

Outputs
Latched Write 0-7

U78, RIF Mode Latch

Output	Pin(s)
GEN Hl/(LO)*	12
Mod Sel 1-2	16,15
WB/(NB)*	5
SA Synth Data	6
SA Spare 1-2	2,9

U79, Audio FIL/LIN Latch

Output	Pin(s)
Audio LPF 1-2	15,12
Audio HPF 1-2	19,16
Gen LIN 1-2	6,5
Audio FL/LIN Spare 1-2	2,9

Fig. 13.4.1.2 Interface Module Output Latches

13.4.6.3 Oscilloscope

The DVM block allows for AC and DC coupling selectable by the processor The METER INPUT meets the following specifications when performing an oscilloscope function:

Freq Response: Lowpass filter with attenuation of 3dB ±0.5dB at 100KHz. AC Mode: Highpass filter with attenuation of 3dB ±0.5dB attenuation at 3.3Hz.
Trigger: trigger level is capable of being set over the full screen range: ±one full screen to a fixed voltage.
Input Voltage: ±100Vpp

The output of the scope attenuator range (U43) is filtered and inverted with a gain of 4.0 (U35). This inverted scope signal is applied to the trigger level comparator (U24) negative input such that a rising edge of a signal at METERING INPUT will cause a trigger output. The trigger level input to the positive input of U24 is determined by D/A converter U39, and made bi-polar by summing an offset (with the D/A output) at U40. Similarly, D/A converter U38 develops the vertical position level and is made bi-polar by U40. The vertical D/A circuitry is designed to output approximately +1V with the D/A input set to 128.

The output of U35 (Alias filter output) and U40 (vertical position) are both summed with a fine adjust vertical position (R57) at U23. The output of this unity gain inverter is applied to the 8 bit A/D U31, which has an input range of 0 to -2 volts. R56 adjusts the negative reference voltage for U31, while R120 adjusts the linearity of U31. Output data is routed to the Processor card via connector J2.

13.4.6.4 8-Bit A/D and Interface

The 8-bit A/D converter is used to take measurements for scope, spectrum analyzer, and modulation scope display. The interface to the A/D is external to the Interface module. The analog input to the A/D is adjustable using the input attenuator.

8-BIT A/D

Conversion Time: 50us
Resolution: 8 bits
Non-Linearity: plus or minus one half bit
Input Voltage Range: 0 to -2V, where 0V=FF and -2V=00
Digital Interface: 8 bit parallel

A processor controlled adjustment adds a DC offset to the input to the 8-bit A/D for vertical positioning. The level is programmable from the processor.

Offset Range: -lV ±2V summed at input to 8-Bit A/D => 2 full screens (plus or minus 1/2 full screen)
Offset: 200 steps in 20mV increments

The 8-Bit A/D has an adjustable trigger for the oscilloscope mode with the following specifications:

Trigger Range: 0 to ±3V at trigger input
Trigger; 200 steps in 30mV increments at the 8-Bit A/D input
Trigger Operation: The output is positive-edge triggered and includes sufficient hysteresis to disable the output for signals less than 10mVpp at the trigger input

13.4.7 Dual Attenuator Ranges

Two attenuator ranges are used to provide each A/D converter the optimum signal levels for measurement of internal or external signals. The metering input (external) signal is always divided by 12 in order to protect "following" circuits. Frequency response for DVM, counter, and scope operation is optimized by compensation capacitor C23.

Unity gain buffer U16 drives both the external scope and DVM attenuator paths, both of which can be independently DC or AC coupled (C48, C36, U21). Each selectable gain amplifier is configured to eliminate the effect of the analog switch ON resistance.

13.4.7.1 DVM Attenuator Range

There are 3 input attenuators/amplifiers for optimizing the input voltage to the 12-bit A/D,

DVM Gain x10* control line
0 = x12
1=x1.2
DVM Gain x5* control line
0=x5
1=xl
DVM Atten Div 2* control line
0 = x0.5
1 = x1

The input to the DVM attenuator range is selected for internal or external signals (U21).

U42 and U48 are configured for either x1, x5, or x0.5 gain. In DC mode, capacitors C127 and C155 are shorted to ground through U67 to form a low pass filter with 30dB attenuation minimum at 50Hz. In AC mode the capacitors are disconnected from ground and do not affect the circuit.

U60 and U67 are configured for either x1.2 or x12 gain. This compensates for the divide by 12 at the metering in order to simplify scale factors.

13.4.7.2 Scope Attenuator Range

The input to the scope attenuator range is selected by multiplexer U32 from among these modulation signals:

1) MOD CAL AUDIO
2) SQUELCHED DEMOD
3) SIGNAL STRENGTH (from Spectrum Analyzer)
4) the Scope signal from the metering input that has been divided by 12 and AC or DC coupled.

U33 and U34 are configured for either x1, x10, or x0.1 gain.

Five input attenuators/amplifiers optimize the input voltage to the 8-bit A/D:

Scope Gain x10* control line 1
- 0 = x10
- 1 = x1

Scope Gain x10* control line 2
- 0 = x10
- 1 = xl

Scope Gain x5* control line
- 0 = x5
- 1 = x1

Scope Gain x2* control line
- 0 = x2
- 1 = xl

Scope Atten Div 10* control line
- 0 = x0.1
- 1 = xl

Any stage has the capability to be enabled separately or in conjunction with several other stages, except: 1) Scope Gain x2* and Scope Gain x5* stages, which are mutually exclusive, and 2) Scope Gain x10* control line 1 and Scope Atten Div 10*, which are mutually exclusive.

13.4.8 SINAD/Distortion/DVM Measurement

13.4.8.1 SINAD/Distortion Meter

The Interface Module provides a fixed frequency automatic EIA SINAD/ Distortion measurement function with the following specifications (all specs are for an input signal at the METERING INPUT port):

Frequency: Input freq of 1KHz ±1Hz
Input Level: 0.lVrms to 10Vims
SINAD Accuracy: ±1dB for 12.0dB SINAD input signal
Distortion Accuracy: ±0.5% of distortion for input signal distortion between 1% and 10% (or ±10% of reading, whichever is greater) and ±2.0% of distortion for input signal distortion between 10% and 20%

SINAD and distortion readings are determined by taking the ratio of the signal level at the output of the 1KHz notch filter to the signal level at the input of the filter.

The 1KHz notch filter has the following specifications:

Center freq. 1.0KHz ±10Hz
Rejection at Center freq: 46 dB minimum

-20dB bandwidth:
- 1KHz 10Hz minimum
- 1KHz ±100Hz maximum

Input level: 0.1Vrms to 10Vrms at meter input
Input freq range: 300Hz to 10KHz
Gain: X1, X10 (processor controlled)

13.4.8.2 DVM/Distortion Measurement

U81, U81 select the output of the DVM attenuator range or the notch filter for true RMS-to-DC conversion (U59) in AC DVM mode. In DC DVM mode, negative voltages are converted to positive by the RMS-to-DC converter, and the sign polarity is detected by U71 and routed to the read buffer (U63).

The output of the DVM attenuator range is applied to a notch filter U83, U85). A processor controlled gain factor of 10 (U81, U85) patterned after the attenuator range amplifiers is selected depending on input distortion and signal levels. Notch depth is a minimum of -46 dB (>5%).

The input to the notch filter is also routed to a rectifier/x1.1 circuit (U73), which outputs a DC value corresponding to the RMS value of the input signal. To obtain the percent distortion of a 1KHz input the processor divides the RMS output voltage of the notch filter (Noise plus Distortion) by the output of the rectifier/x1.1 circuit (Signal plus Noise plus Distortion).

13.4.9 SWEEP Signal Generation

The Interface Module generates the sweep signal for the Spectrum Analyzer module. A clock signal (TIMER CLOCK) from the ASIC on the Processor Module controls the rate at which binary counter U27 increments the Sweep DAC, U28, through its gain control. The filtered staircase output is made bi-polar by summing the +8.0V DAC reference voltage (with the DAC output) at U26 with half the gain such that a highly accurate 16Vpp signal centered about zero results.

The sweep generator has a staircase output having the following specifications:

Output Voltage: Sawtooth waveform from –8.0V (all zeroes to the Sweep DAC) to +8.0V (all ones to the Sweep DAC). The output is a digital staircase with the 16V ramp formed in 256 steps. The sweep is always from negative to positive with the capability to reset it at anytime to the negative rail.

Input Freq: 256Hz to 12.8KHz
*Output Freq:*1Hz to 50Hz

Freq Accuracy: Output freq accuracy is equal to that of the system timebase or a maximum error of ±1ppm.

Output Coupling: DC coupled.

13.4.10 Counter

The Interface module provides a counter output (COUNTER) to allow period and frequency counter readings to be made. The counter function can accept input from:

1) LIM 700KHz
2) Scan Lock Freq
3) DVM From Range
4) Spare Inputs

Input Level to Counter MUX at CMOS levels. Input Frequency Range: 5Hz to 1.0MHZ.

Digital multiplexer U30 decodes Counter SEL 1-3 (from U18 output latch) to select the signal to be routed to the counter circuit on the Processor Module. Comparator U44 converts the output of the DVM attenuator range to CMOS levels, and includes hysteresis to desensitize the comparator of noise.

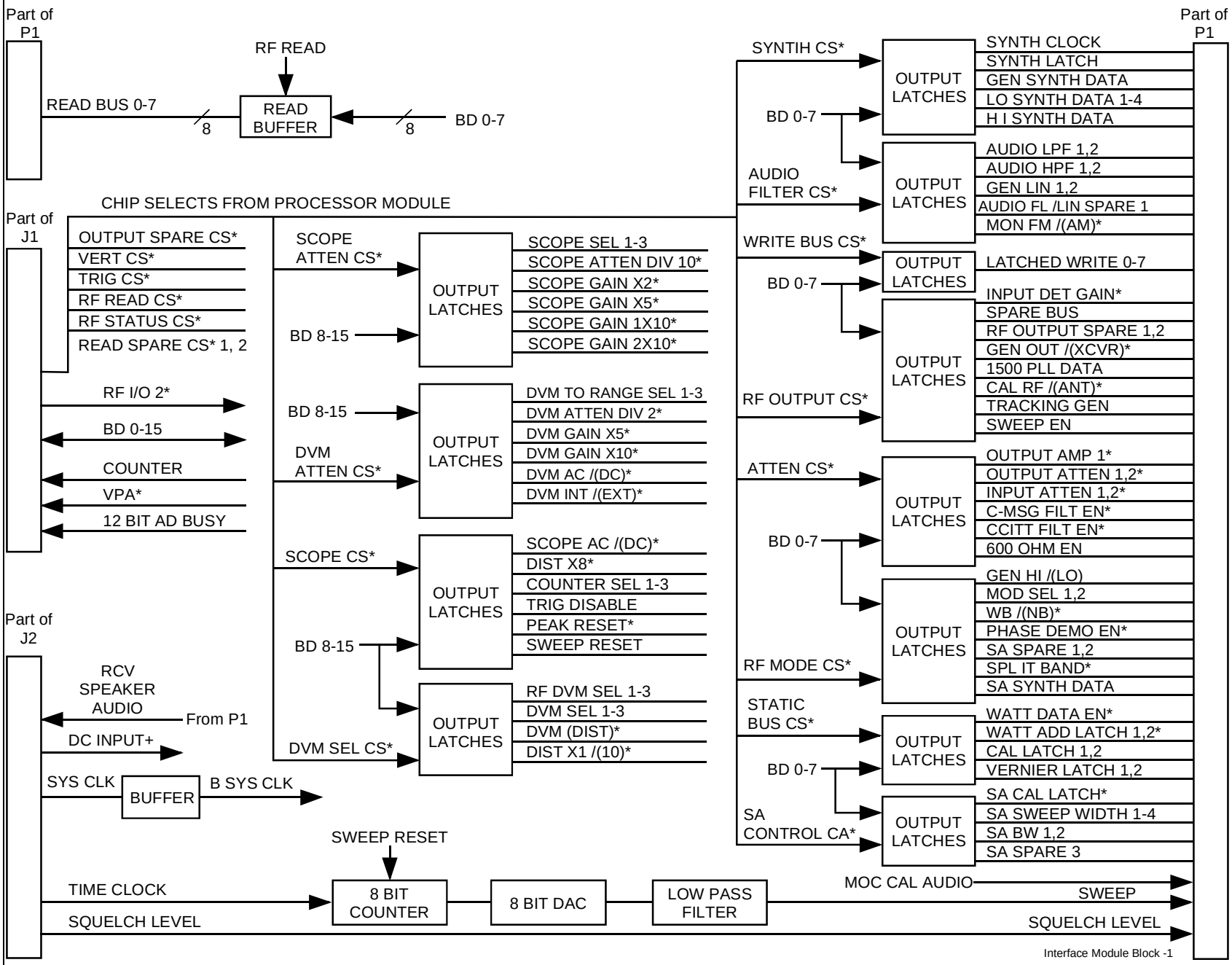


Fig. 13.5 RF Interface Module Block Diagram (1 of 3)

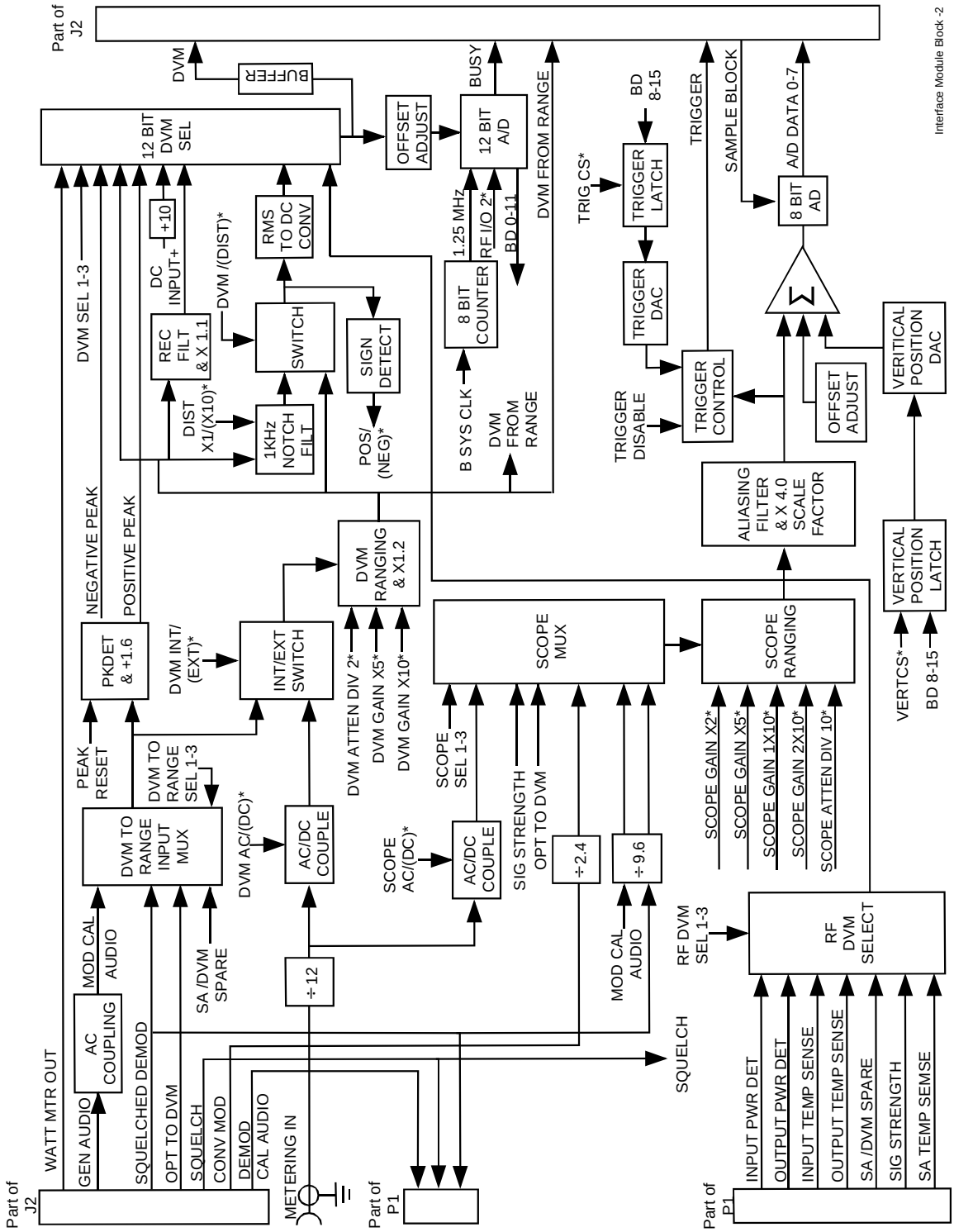
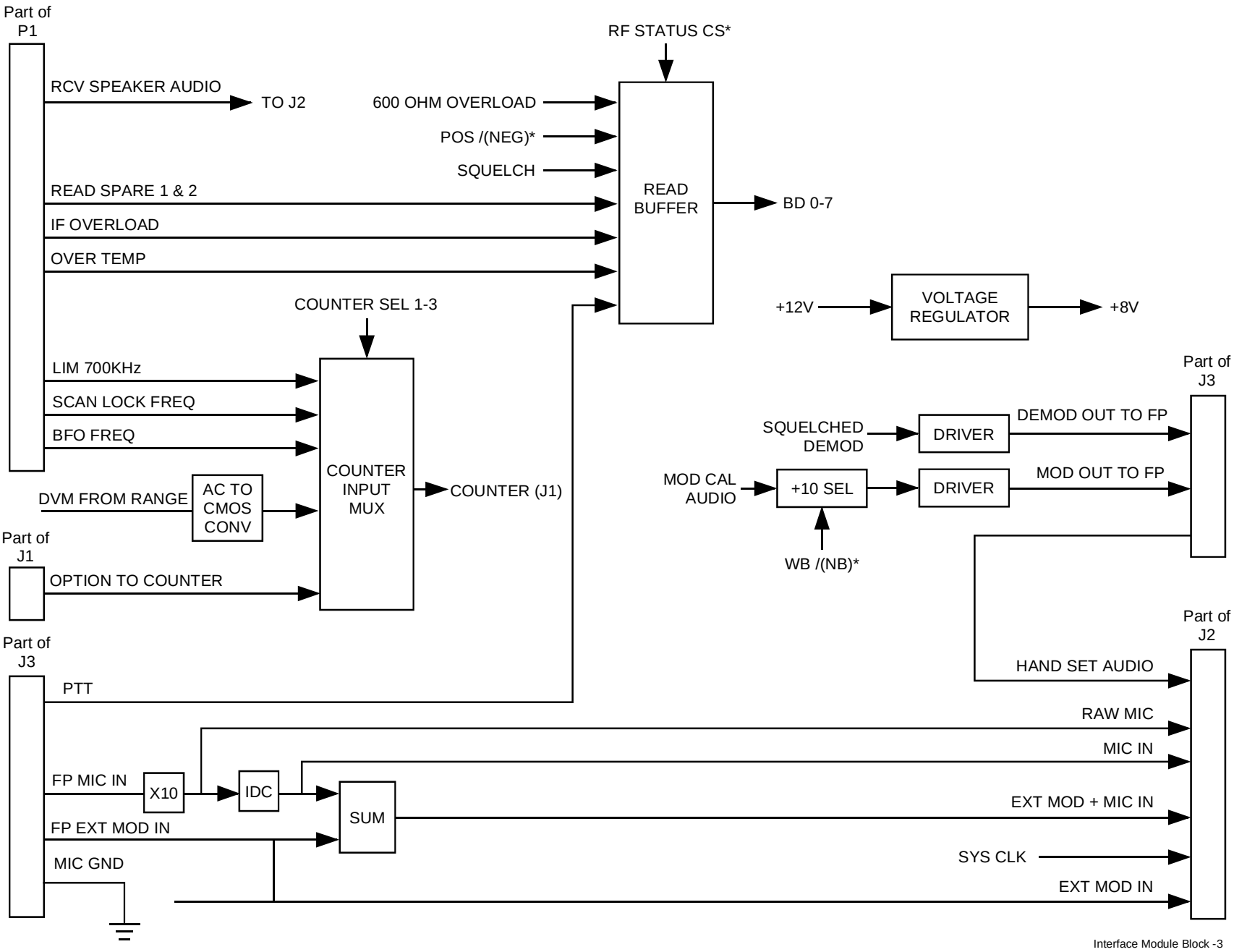
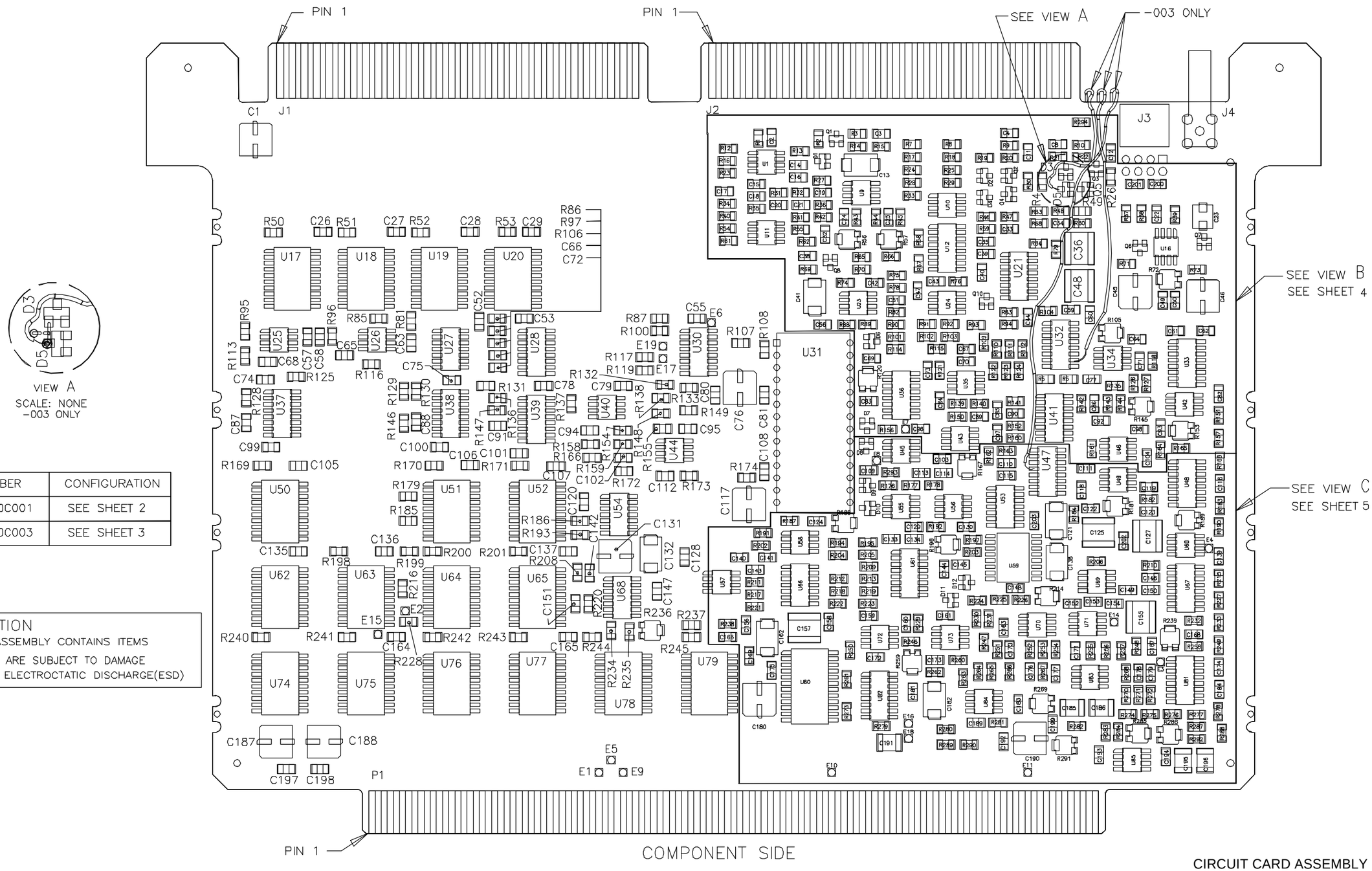


Fig. 13.5 RF Interface Module Block Diagram (2 of 3)

Fig. 13.5 RF Interface Module Block Diagram (3 of 3)





PART NUMBER	CONFIGURATION
01-P30940C001	SEE SHEET 2
01-P30940C003	SEE SHEET 3

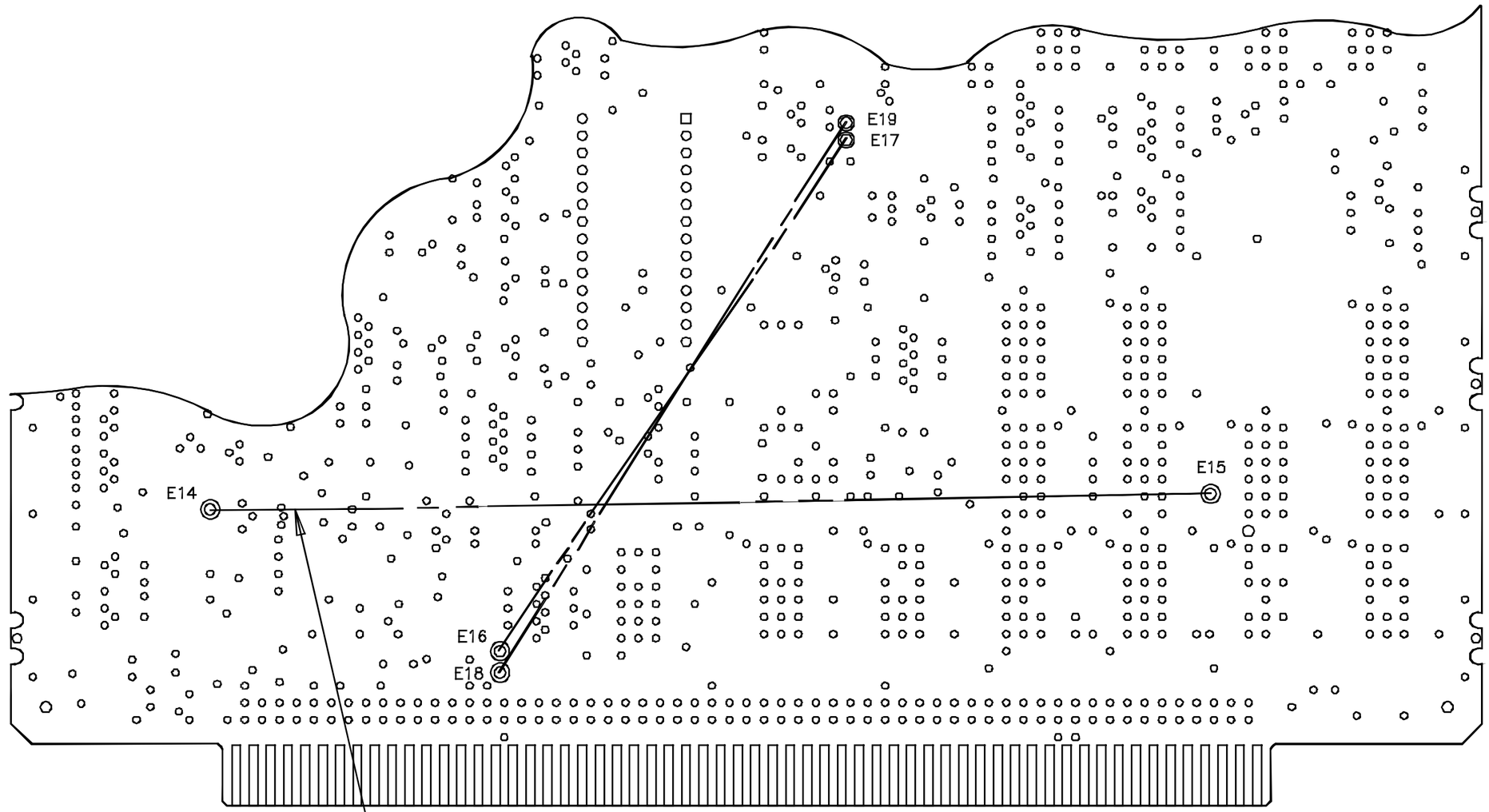
CAUTION
THIS ASSEMBLY CONTAINS ITEMS
WHICH ARE SUBJECT TO DAMAGE
FROM ELECTROCTATIC DISCHARGE(ESD)

CIRCUIT CARD ASSEMBLY
INTERFACE

01-P30940C REV. C

TABLE 1

WIRE LIST	
FROM	TO
E14	E15
E16	E17
E18	E19



SOLDER SIDE

SEE TABLE 1

—001 CONFIGURATION

CAUTION
THIS ASSEMBLY CONTAINS ITEMS
WHICH ARE SUBJECT TO DAMAGE
FROM ELECTROCTATIC DISCHARGE(ESD)

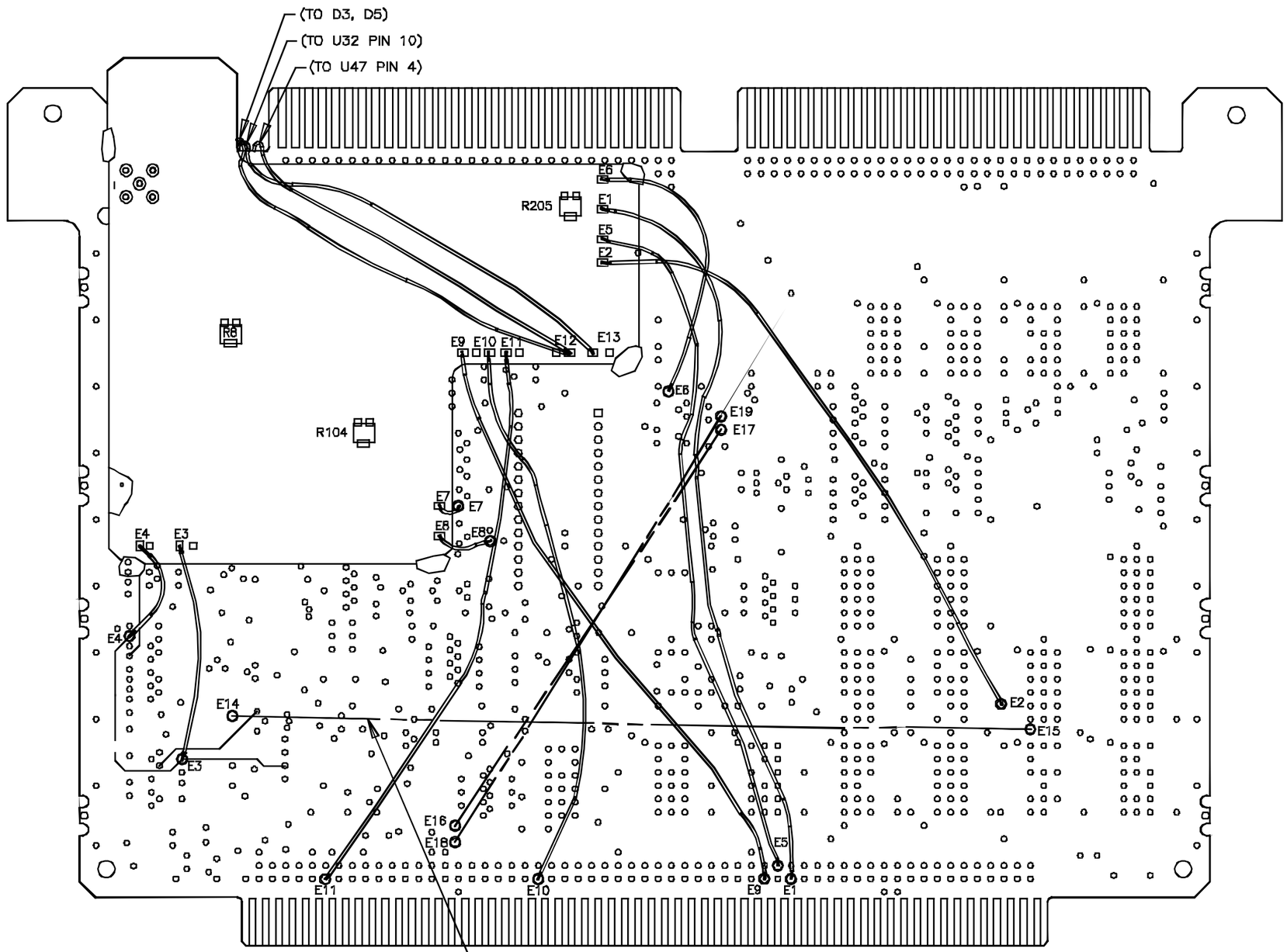
CIRCUIT CARD ASSEMBLY
INTERFACE

01-P30940C REV. C

SHEET 2 OF 5

TABLE 2

WIRE LIST	
FROM	TO
E1	E1
E2	E2
E3	E3
E4	E4
E5	E5
E6	E6
E7	E7
E8	E8
E9	E9
E10	E10
E11	E11
E14	E15
E16	E17
E18	E19



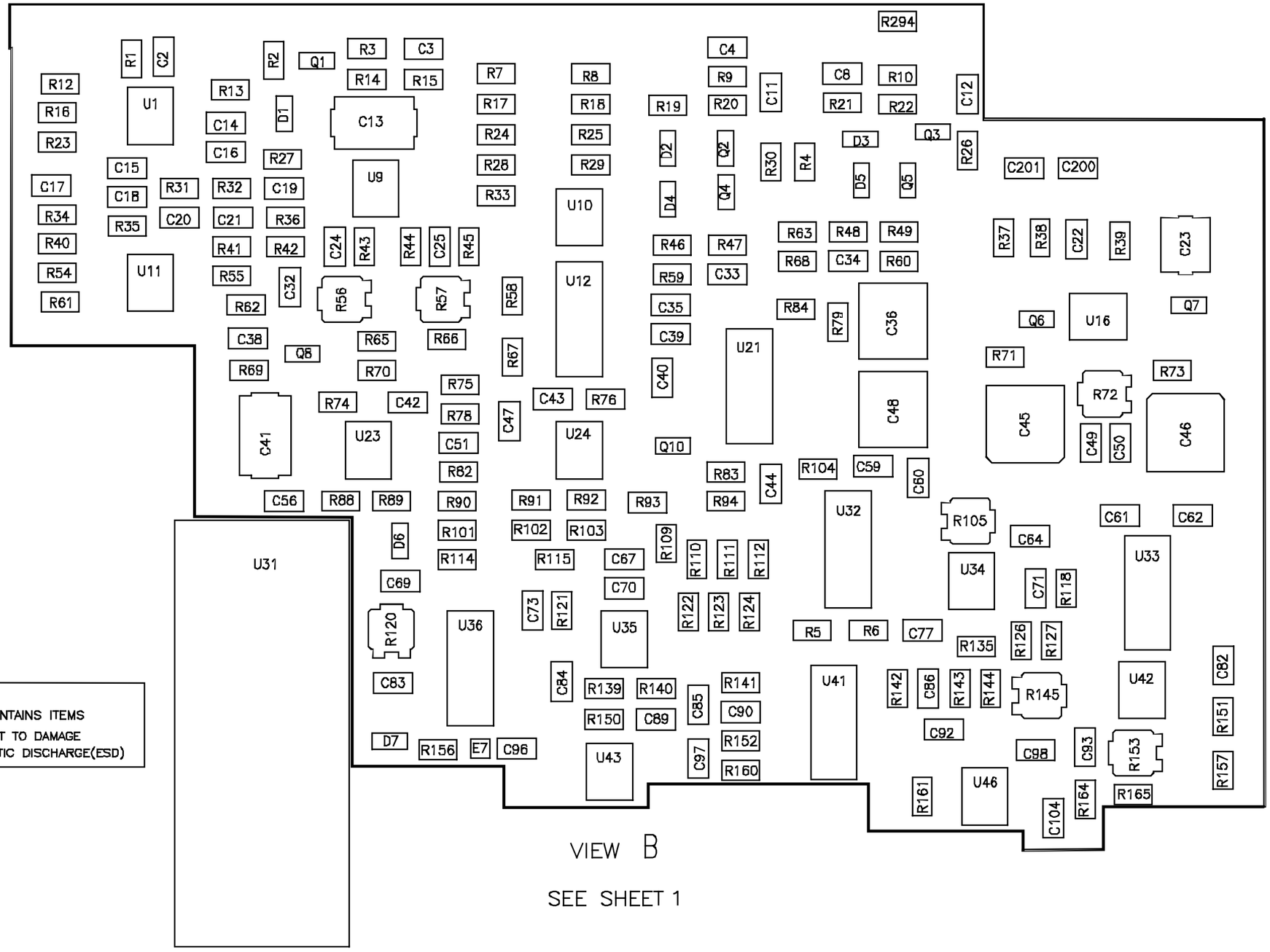
SOLDER SIDE

-003 CONFIGURATION

CAUTION
THIS ASSEMBLY CONTAINS ITEMS
WHICH ARE SUBJECT TO DAMAGE
FROM ELECTROCTATIC DISCHARGE(ESD)

CIRCUIT CARD ASSEMBLY
INTERFACE

01-P30940C REV. C



CAUTION
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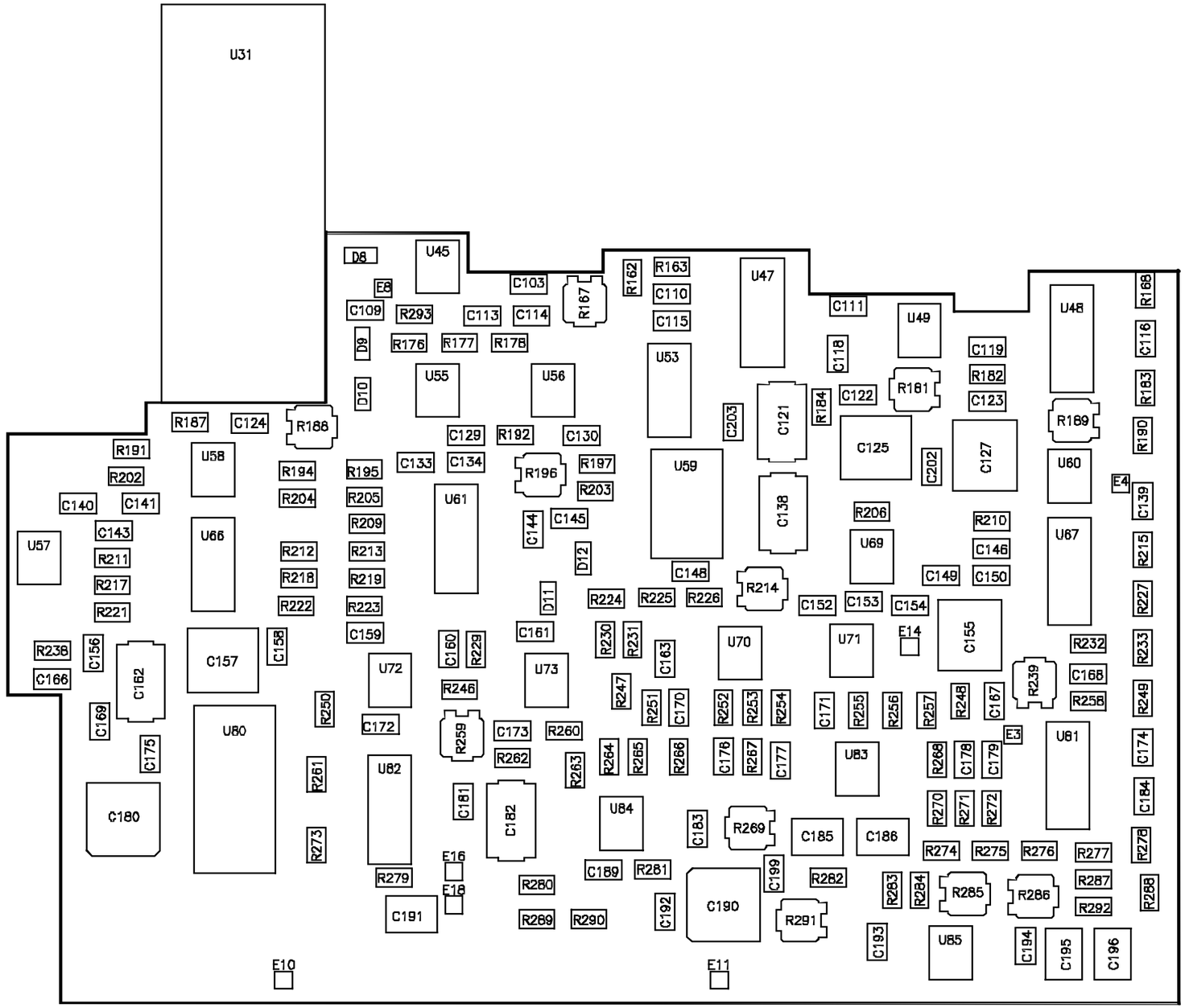
WHICH ARE SUBJECT TO DAMAGE
FROM ELECTROCTATIC DISCHARGE(ESD)

VIEW B

SEE SHEET 1

CIRCUIT CARD ASSEMBLY
INTERFACE

01-P30940C REV. C



CAUTION
THIS ASSEMBLY CONTAINS ITEMS
WHICH ARE SUBJECT TO DAMAGE
FROM ELECTROCTATIC DISCHARGE(ESD)

VIEW C

SEE SHEET 1

CIRCUIT CARD ASSEMBLY
INTERFACE

01-P30940C REV. C

DWG NO 63-P30942C 5A

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
-	INITIAL RELEASE 93-07-15	930728	RJC
A	CO C35881-2 RJC 93-10-07		
B	CO C35955-1 MSM 94-05-31		
C	SEE CO E36174-3 MEW 95-09-12	95-09-13	KOESTNER

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A12.

2. FOR REFERENCE DRAWINGS REFER TO:
   01-P30940C ASSEMBLY
   12-P30943C TEST PROCEDURE.

3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL INDUCTANCE VALUES ARE IN UH.
   ALL VOLTAGES ARE IN DC.

4. TERMINATIONS CODED WITH THE SAME LETTERS OR NUMBERS ARE ELECTRICALLY CONNECTED.

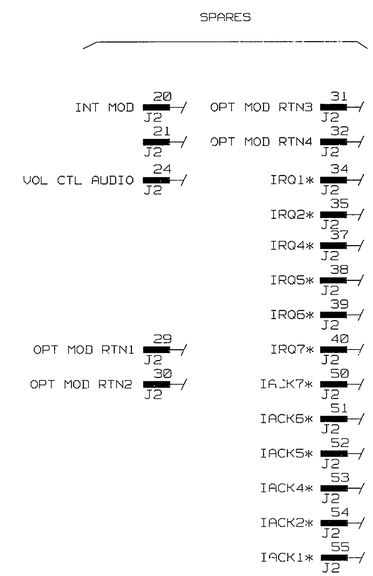
5. DEVICE TYPE NUMBERS AND CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE 1. PORTIONS OF THE TYPE NUMBER MAY BE UNDERLINED AND USED AS A CODE TO IDENTIFY DEVICES ON DIAGRAM.

6. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH MANUFACTURER. ENGINEERING APPROVED EQUIVALENT DEVICE MAY BE USED.

REFERENCE DESIGNATIONS	
HIGHEST NUMBER USED	NOT USED
C203	C5, 6, 7, 9, 10, 30, 31, 37, 54, 126
D12	
E19	E12, E13
FN1	
J4	J1, J2
P1	
Q10	Q9
R294	R11, 64, 77, 80, 98, 99, 134, 175, 180, 207
U85	U2 THRU U8, 13, 14, 15, 22, 29

TABLE 1 (5)

PAGE FOUND ON	REF DES	DEVICE TYPE (6)	+5	-5	GND	+12	-12	AGND	
15	U1	MC34072D				8	4		
15	U9	MC34072D				8	4		
7	U10	MC34072D				8	4		
2, 15	U11	MC34072D				8	4		
7	U12	DG211CSE	12		5	13	4		
8	U16	MC34081D				7 (+12A)	4 (-12A)		
5	U17	74ACT374SC	20		10				
5	U18	74ACT374SC	20		10				
5	U19	74ACT374SC	20		10				
6	U20	74ACT374SC	20		10				
8	U21	DG211CSE	12		5	13	4		
14	U23	MC34072D			5	8	4		
13	U24	LM311D			1	8	4		
2, 11	U25	MC34072D				8	4		
6, 7	U26	MC34072D				8	4		
7	U27	CD74HC393M	14		7				
7	U28	DAC08CD				1	7		
14	U30	74AC151SC	16		8				



ALL SHEETS ARE THE SAME REVISION STATUS

		CONTR	MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417
		ISS B34440-538 90-04-12	
		APPROVALS	TITLE
		DWN B. SCOTT 93-07-15	SCHEMATIC DIAGRAM INTERFACE
		CHKR K. NELSON 93-07-15	
		QA	
		MATL	
01-P30940C	COCHISE	MFG K. CHANEY 93-07-15	SIZE D / CAGE CODE 94990 / DWG NO 63-P30942C
NEXT ASSY	USED ON	ENG A. KOESTNER 93-07-15	
APPLICATION		CUST	SCALE NONE / SHEET 1 OF 15

ASME Y14.1-1995 DRAWING FORMAT - 3/95

DRAWING 63P30942C_C 63P30942C_C

CONCEPT

LAST_MODIFIED=Tue Sep 12 10:16:09 1995

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DSIZEPAGE1HDEC

* 1103

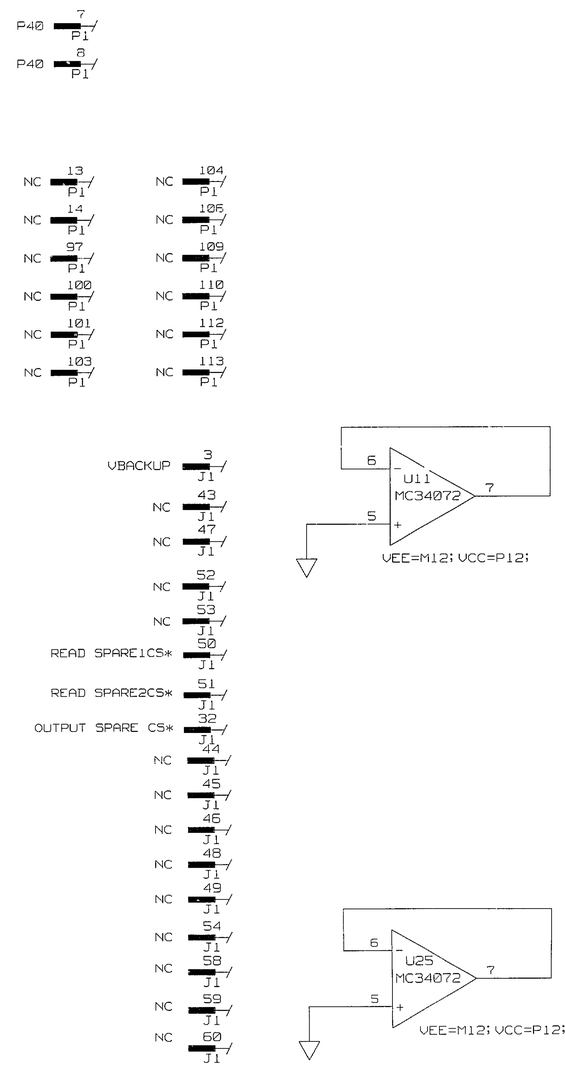
TABLE 1 (5)

PAGE FOUND ON	REF DES	DEVICE TYPE (6)	+5	-5	GND	+12	-12	AGND	NO CONN.
14	U31	ADC-304	6,10	7,8,9	5,11 19,25				20,22 24
6	U32	DG508ADY			14	13	3		
9	U33	DG211CSE	12		5	13	4		
9	U34	MC34081D				7	4		8
13	U35	MC34081D				7	4		8
8,10	U36	DG211CSE	12		5	13	4		
11	U37	DAC08CD				1	7		
13	U38	DAC08CD				1	7		
13	U39	DAC08CD				1	7		
13	U40	MC34072D				8	4		
10	U41	DG211CSE	12		5	13	4		
9	U42	MC34081D				7	4		8
10	U43	MC34081D				7	4		8
14	U44	LM311D			1	8	4		
8	U45	TL072D				8	4		
10	U46	MC34081D				7	4		8
8	U47	DG508ADY			14	13	3		
9	U48	DG211CSE	12		5	13	4		
6	U49	MC34081D				7	4		8
11	U50	74ACT374SC	20		10				
13	U51	74ACT374SC	20		10				
13	U52	74ACT374SC	20		10				
10,11	U53	74AC00SC	14		7				
8,9	U54	74AC04SC	14		7				
8	U55	TL072D				8	4		
8	U56	MC34081D				7	4		8
6	U57	LT1016CD	1	4	6				
12	U58	MC34081D				7	4		8
12	U59	AD637JR			3	13	12		
9	U60	MC34081D			8	7	4		

TABLE 1 (5)

PAGE FOUND ON	REF DES	DEVICE TYPE (6)	+5	-5	GND	+12	-12	AGND	NO CONN.
11	U61	DG508ADY			14	13	3		
5	U62	74ACT244SC	20		10				
5	U63	74ACT244SC	20		10				
6	U64	74ACT374SC	20		10				
4	U65	74ACT374SC	20		10				
12	U66	CD74HC393M	14		7				
9,10	U67	DG211CSE	12		5	13	4		
15	U68	MC1723CD			7	11,12			1,8,9, 14
12	U69	MC34081D				7	4		8
12	U70	MC34081D				7	4		8
12	U71	LM311D			1	8	4		
12	U72	MC34081D				7	4		8
11	U73	MC34072D				8	4		
6	U74	74ACT374SC	20		10				
4	U75	74ACT374SC	20		10				
5	U76	74ACT374SC	20		10				
4	U77	74ACT374SC	20		10				
4	U78	74ACT374SC	20		10				
6	U79	74ACT374SC	20		10				
12	U80	MAX172ACWG	24 (+5A)		3,12		23		
10,11	U81	DG211CSE	12		5	13	4		
8	U82	DG508ADY			14	13	3		
10	U83	MC34072D				8	4		
11	U84	MC34072D				8	4		
10,11	U85	MC34072D				8	4		

SPARES



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30942C	REV C
	SCALE NONE		SHEET 2	

ASME Y14.1-1995 DRAWING FORMAT - 3/95

DRAWING 63P30942C_C 2
63P30942C_C
LAST_MODIFIED=Tue Aug 22 08:29:48 1995

CONCEPT TIFAA 1 DSIZEPAGE2MD2C

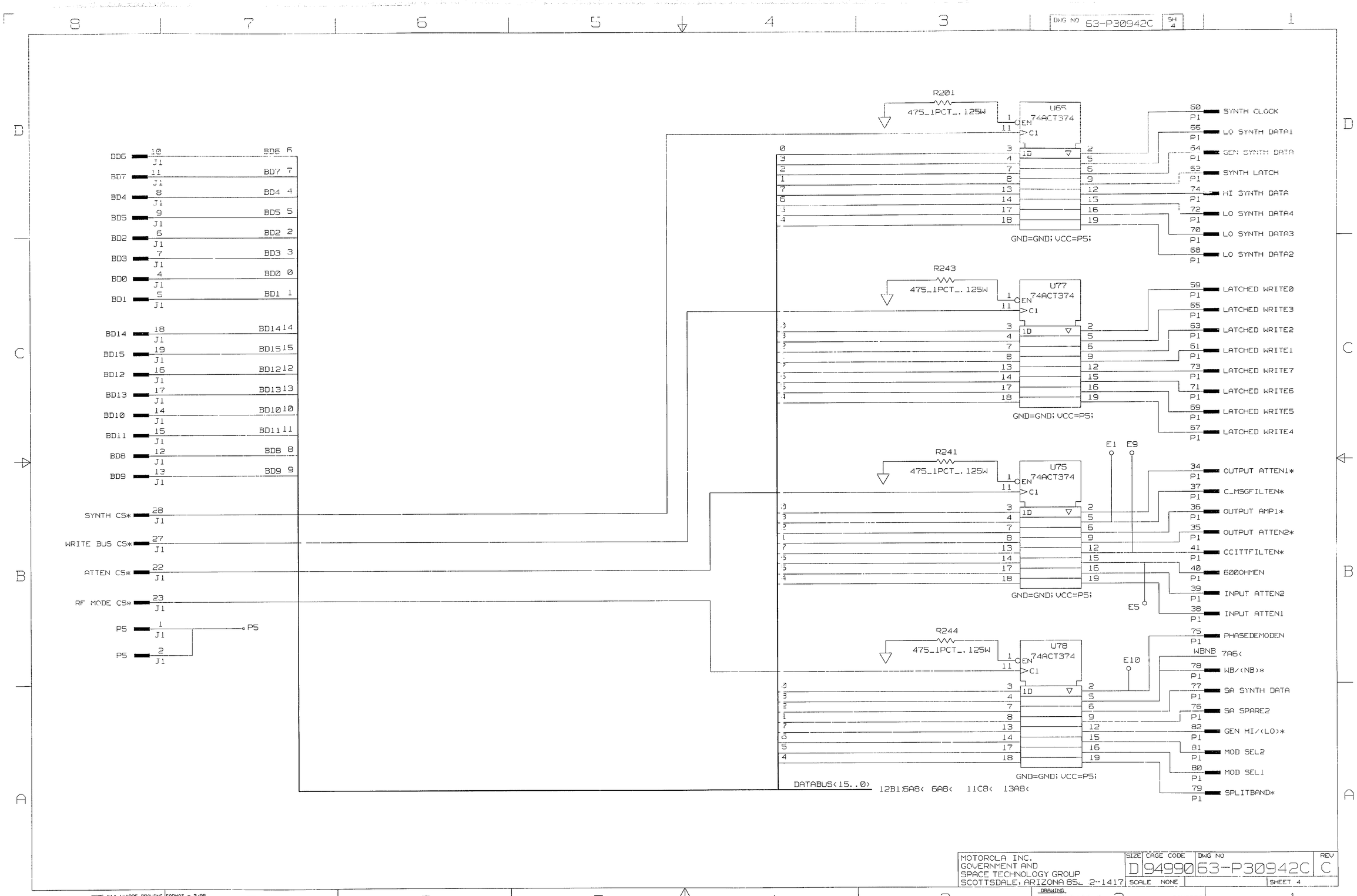
P5 3 P1
P5 4 P1
GND 1 P1
GND 2 P1
GND 119 P1
GND 120 P1
M5 5 P1
M5 6 P1
P12 117 P1
P12 118 P1
25 J2
27 J2
20 J1
21 J1
29 J1
30 J1
M12 115 P1
M12 116 P1
2 J2
4 J2
8 J2
10 J2
14 J2
23 J2
33 J2
57 J2
6 J3
8 J3

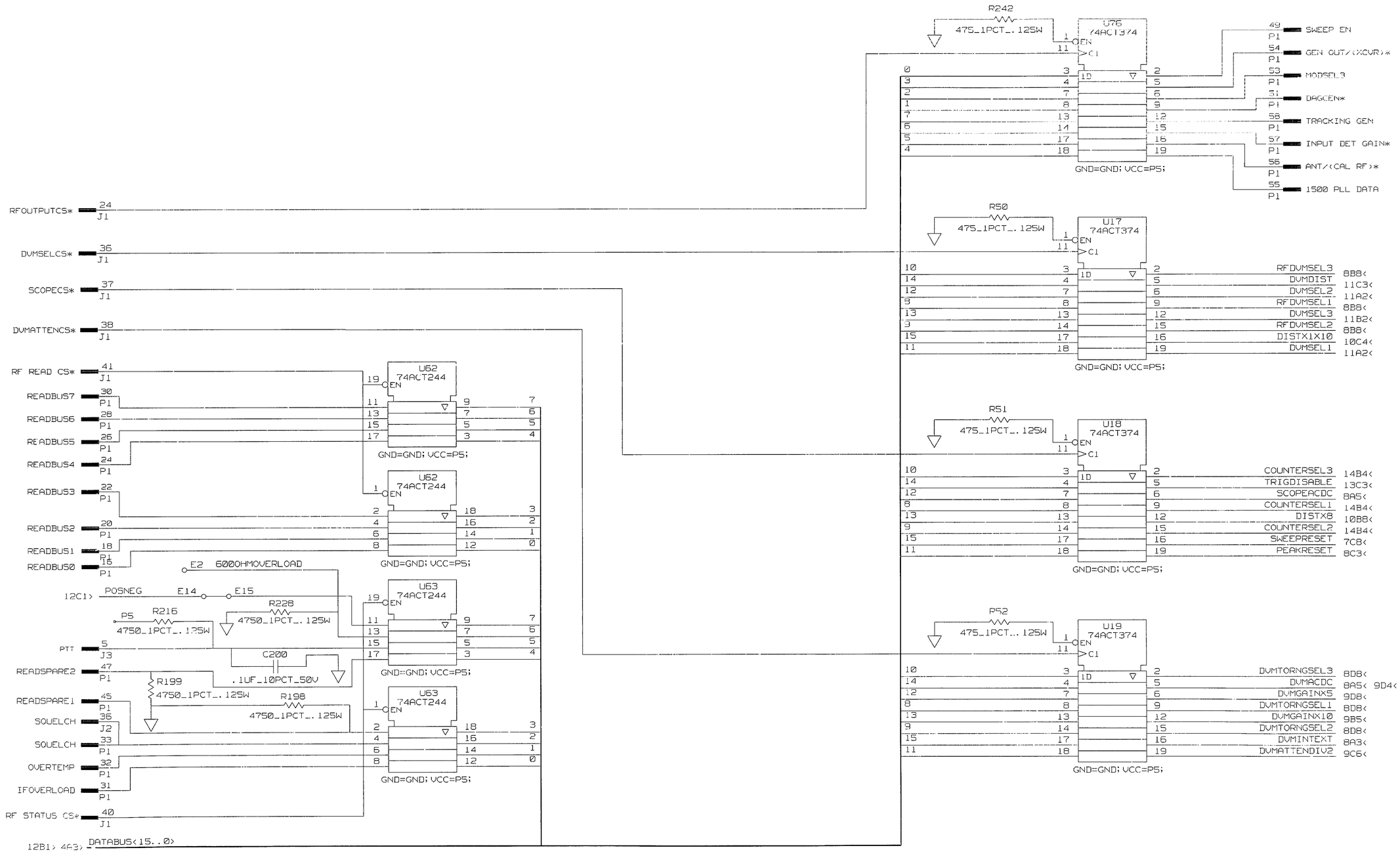
C1 33UF_20PCT_25V
C117 33UF_20PCT_25V U31-10
C167 33UF_20PCT_25V P1-3,4
C26 .1UF_10PCT_50V U17-20
C27 .1UF_10PCT_50V U18-20
C28 .1UF_10PCT_50V U19-20
C29 .1UF_10PCT_50V U20-20
C52 .1UF_10PCT_50V U27-14
C55 .1UF_10PCT_50V U30-16
C81 .1UF_10PCT_50V U31-6
C105 .1UF_10PCT_50V U50-20
C106 .1UF_10PCT_50V U51-20
C107 .1UF_10PCT_50V U52-20
C108 .1UF_10PCT_50V U31-10
C115 .1UF_10PCT_50V U53-14
C120 .1UF_10PCT_50V U54-14
C128 .1UF_10PCT_50V U57-1
C135 .1UF_10PCT_50V U62-20
C136 .1UF_10PCT_50V U63-20
C137 .1UF_10PCT_50V U65-20
C143 .1UF_10PCT_50V U66-14
C164 .1UF_10PCT_50V U75-20
C165 .1UF_10PCT_50V U77-20
C166 .1UF_10PCT_50V U79-20
C197 .1UF_10PCT_50V P1-3,4
C76 33UF_20PCT_25V U31-9
C188 33UF_20PCT_25V P1-5,6
C56 .1UF_10PCT_50V U23-4
C80 .1UF_10PCT_50V U31-9
C140 .1UF_10PCT_50V U57-4
C198 .1UF_10PCT_50V P1-5,6
C2 .1UF_10PCT_50V U1-8
C17 .1UF_10PCT_50V U11-8
C25 .1UF_10PCT_50V U9-8
C35 .1UF_10PCT_50V U10-7
C42 .1UF_10PCT_50V U23-8
C43 .1UF_10PCT_50V U24-8
C44 .1UF_10PCT_50V U21-13
C53 .1UF_10PCT_50V U28-1
C57 .1UF_10PCT_50V U25-8
C60 .1UF_10PCT_50V U32-13
C62 .1UF_10PCT_50V U33-13
C63 .1UF_10PCT_50V U26-8
C64 .1UF_10PCT_50V U34-7
C70 .1UF_10PCT_50V U35-7
C73 .1UF_10PCT_50V U36-13
C74 .1UF_10PCT_50V U37-1
C75 .1UF_10PCT_50V U38-1
C78 .1UF_10PCT_50V U39-1
C79 .1UF_10PCT_50V U40-8
C82 .1UF_10PCT_50V U42-7
C92 .1UF_10PCT_50V U41-13
C95 .1UF_10PCT_50V U44-8
C96 .1UF_10PCT_50V U45-8
C97 .1UF_10PCT_50V U43-7
C98 .1UF_10PCT_50V U46-7
C114 .1UF_10PCT_50V U56-7
C116 .1UF_10PCT_50V U48-13
C118 .1UF_10PCT_50V U47-13
C119 .1UF_10PCT_50V U49-7
C124 .1UF_10PCT_50V U58-7
C139 .1UF_10PCT_50V U60-7
C144 .1UF_10PCT_50V U61-13
C145 .1UF_10PCT_50V U59-13
C149 .1UF_10PCT_50V U69-7
C152 .1UF_10PCT_50V U70-7
C154 .1UF_10PCT_50V U71-8
C160 .1UF_10PCT_50V U72-7
C161 .1UF_10PCT_50V U73-8
C168 .1UF_10PCT_50V U67-13
C174 .1UF_10PCT_50V U81-13
C178 .1UF_10PCT_50V U83-8
C181 .1UF_10PCT_50V U82-13
C183 .1UF_10PCT_50V U84-8
C194 .1UF_10PCT_50V U85-8
C190 33UF_20PCT_25V P1-115,116
C157 .1UF_20PCT_50V U80-23
C15 .1UF_10PCT_50V U1-4
C18 .1UF_10PCT_50V U11-4
C24 .1UF_10PCT_50V U9-4
C39 .1UF_10PCT_50V U10-4
C40 .1UF_10PCT_50V U21-4
C47 .1UF_10PCT_50V U24-4
C59 .1UF_10PCT_50V U32-3
C61 .1UF_10PCT_50V U33-4
C65 .1UF_10PCT_50V U26-4
C68 .1UF_10PCT_50V U25-4
C72 .1UF_10PCT_50V U28-7
C77 .1UF_10PCT_50V U34-4
C83 .1UF_10PCT_50V U36-4
C84 .1UF_10PCT_50V U35-4
C85 .1UF_10PCT_50V U41-4
C93 .1UF_10PCT_50V U42-4
C94 .1UF_10PCT_50V U40-4
C99 .1UF_10PCT_50V U37-7
C100 .1UF_10PCT_50V U38-7
C101 .1UF_10PCT_50V U39-7
C103 .1UF_10PCT_50V U43-4
C104 .1UF_10PCT_50V U48-4
C109 .1UF_10PCT_50V U45-4
C110 .1UF_10PCT_50V U47-3
C111 .1UF_10PCT_50V U46-4
C112 .1UF_10PCT_50V U44-4
C122 .1UF_10PCT_50V U49-4
C130 .1UF_10PCT_50V U56-4
C134 .1UF_10PCT_50V U61-3
C141 .1UF_10PCT_50V U58-4
C146 .1UF_10PCT_50V U60-4
C148 .1UF_10PCT_50V U59-12
C150 .1UF_10PCT_50V U67-4
C153 .1UF_10PCT_50V U69-4
C158 .1UF_10PCT_50V U80-23
C159 .1UF_10PCT_50V U72-4
C163 .1UF_10PCT_50V U70-4
C171 .1UF_10PCT_50V U71-4
C172 .1UF_10PCT_50V U82-3
C173 .1UF_10PCT_50V U73-4
C176 .1UF_10PCT_50V U83-4
C179 .1UF_10PCT_50V U81-4
C189 .1UF_10PCT_50V U84-4
C192 .1UF_10PCT_50V P1-116,117
C193 .1UF_10PCT_50V U85-4

MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252 1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30942C	REV C
	SCALE NONE		SHEET 3	

ASME Y14.1-1995 DRAWING FORMAT - 3/95

DRAWING 63P30942C_C 2
63P30942C_C
LAST_MODIFIED=Fri Aug 18 18:08:35 1995
CONCEPT
DSIZEPAGE2H02C


DWG NO 63-P30942C SH 4
R201
475_1PCT_.125W
U65
74ACT374
EN
C1
1D
GND=GND; VCC=P5;
SYNTH CLOCK
LO SYNTH DATA1
GEN SYNTH DATA
SYNTH LATCH
HI SYNTH DATA
LO SYNTH DATA4
LO SYNTH DATA3
LO SYNTH DATA2
R243
U77
LATCHED WRITE0
LATCHED WRITE3
LATCHED WRITE2
LATCHED WRITE1
LATCHED WRITE7
LATCHED WRITE6
LATCHED WRITE5
LATCHED WRITE4
R241
U75
E1
E9
E5
OUTPUT ATTEN1*
C_MSGFILTEN*
OUTPUT AMP1*
OUTPUT ATTEN2*
CCITTFILTEN*
600OHMEN
INPUT ATTEN2
INPUT ATTEN1
R244
U78
E10
PHASEDEMODEN
WBNB 7A6<
WB/<NB>*
SA SYNTH DATA
SA SPARE2
GEN HI/<LO>*
MOD SEL2
MOD SEL1
SPLITBAND*
DATABUS<15..0>
12B1 5A8< 6A8< 11C8< 13A8<
BD6
BD7
BD4
BD5
BD2
BD3
BD0
BD1
BD14
BD15
BD12
BD13
BD10
BD11
BD8
BD9
SYNTH CS*
WRITE BUS CS*
ATTEN CS*
RF MODE CS*
P5
J1
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85_ 2-1417
SIZE D
CAGE CODE 94990
DWG NO 63-P30942C
REV C
SCALE NONE
SHEET 4
DRAWING
63P30942C_C
63P30942C_C
LAST_MODIFIED=Fri Aug 18 18:11:01 1995
CONCEPT
ASME Y14.1-1995 DRAWING FORMAT - 3/95
DSIZEPAGE2H02C



MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 8525. 1417

SIZE	CAGE CODE	DWG NO	REV
D	94990	63-P30942C	C
SCALE NONE		SHEET 5	

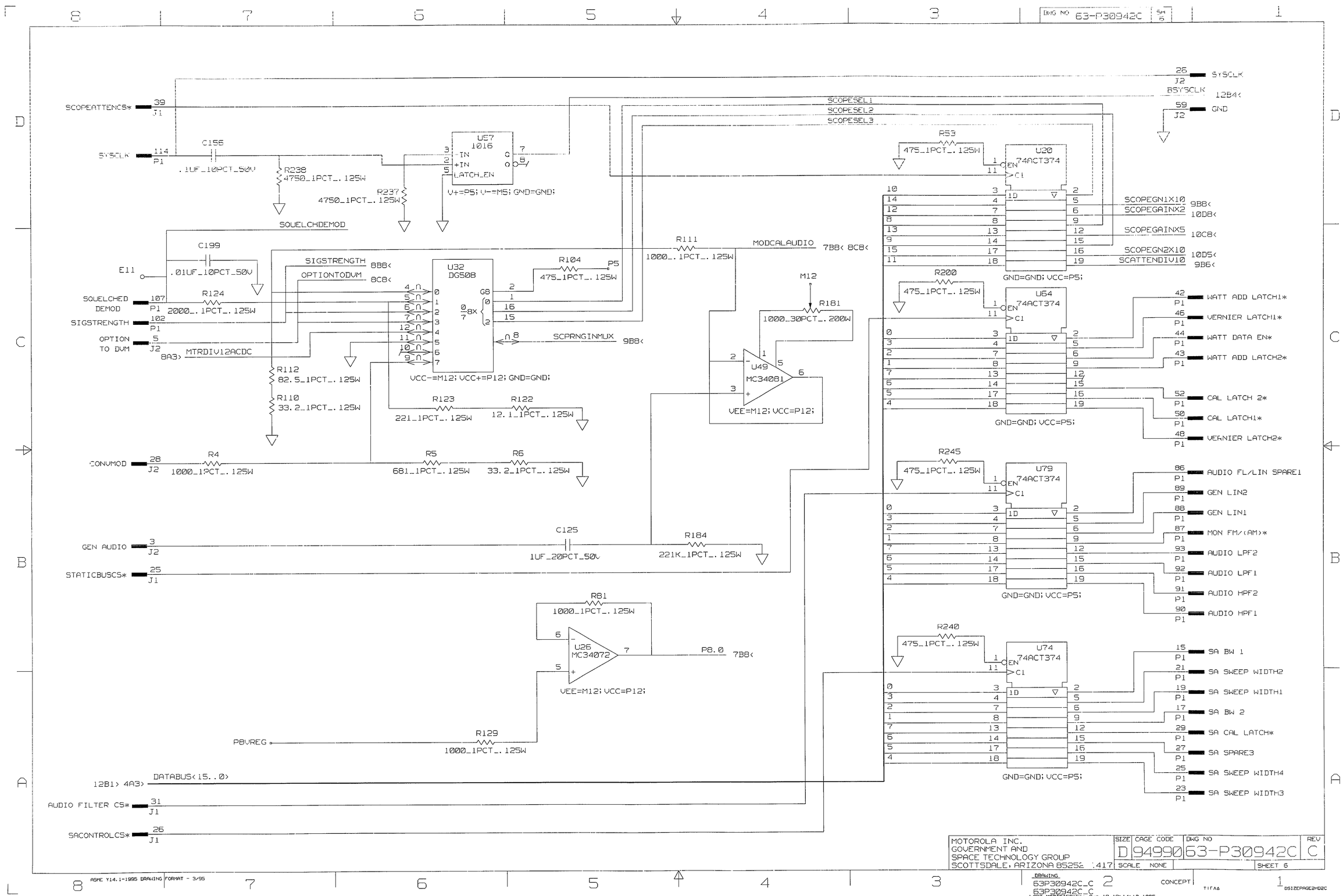
DRAWING
63P30942C_C
63P30942C_C
LAST_MODIFIED=Fri Aug 18 10:12:26 1995

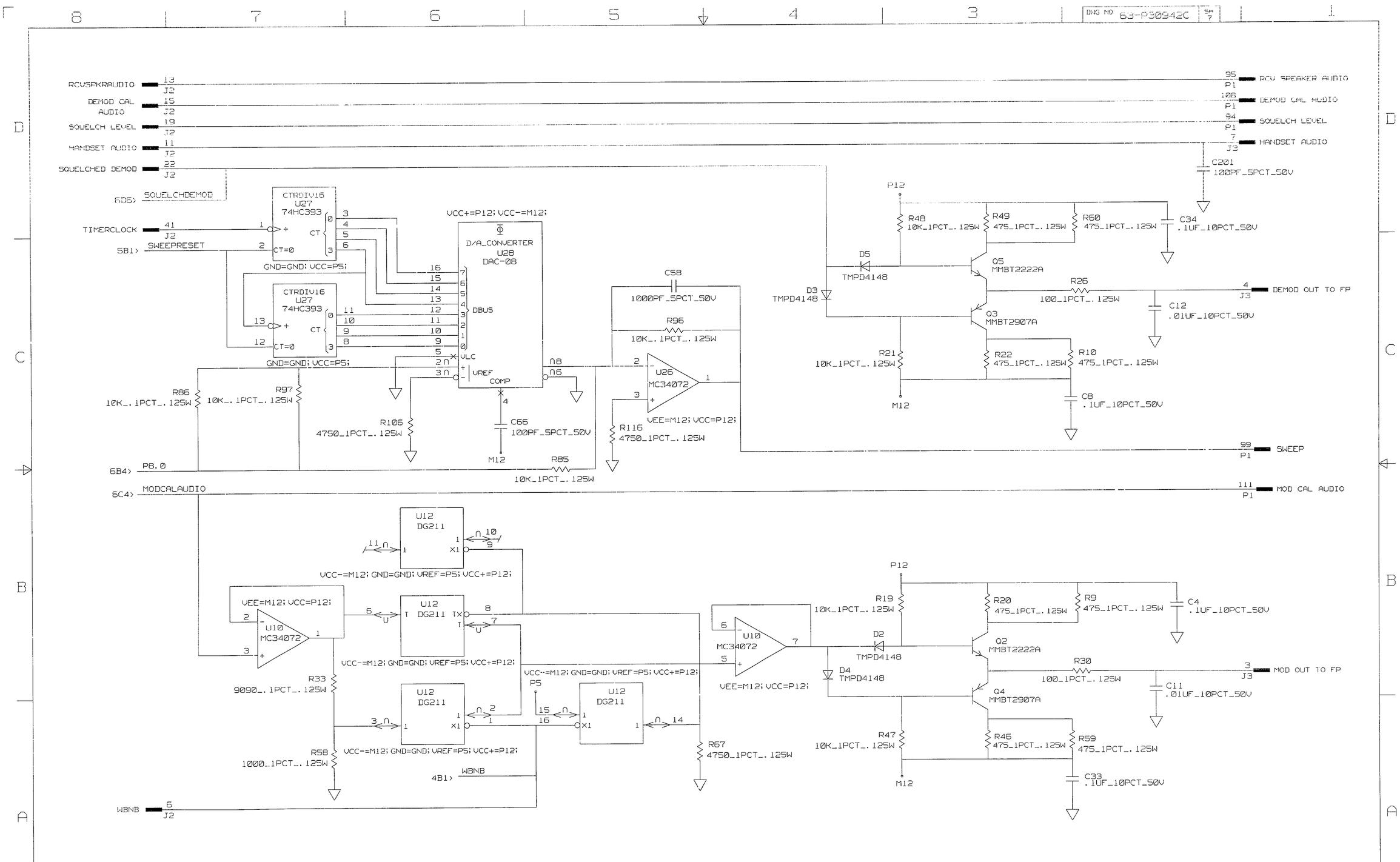
CONCEPT

TITAA

DSIZEPAGE2H-D2C

ASME Y14.1 .995 DRAWING FORMAT - 3/95


DWG NO 63-P30942C
SCOPEATTENCS* 39 J1
SYSCLK 114 P1
C156 .1UF_10PCT_50V
R238 4750_1PCT_.125W
R237 4750_1PCT_.125W
U57 1016
IN
+IN
LATCH_EN
V+=P5; V-=M5; GND=GND;
SQUELCHDEMOD
C199 .01UF_10PCT_50V
E11
SQUELCHED DEMOD 107 P1
SIGSTRENGTH 102 P1
OPTION TO DVM 5 J2
R124 2000_.1PCT_.125W
SIGSTRENGTH 8B8<
OPTIONTODVM 8C8<
MTRDIV12ACDC 8A3>
U32 DG508
VCC-=M12; VCC+=P12; GND=GND;
R104 475_1PCT_.125W
P5
SCPRNGINMUX 9B8<
R112 82.5_1PCT_.125W
R110 33.2_1PCT_.125W
R123 221_1PCT_.125W
R122 12.1_1PCT_.125W
CONVMOD 28 J2
R4 1000_1PCT_.125W
R5 681_1PCT_.125W
R6 33.2_1PCT_.125W
GEN AUDIO 3 J2
C125 1UF_20PCT_50V
R184 221K_1PCT_.125W
STATICBUSCS* 25 J1
R81 1000_1PCT_.125W
U26 MC34072
VEE=M12; VCC=P12;
P8.0 7B8<
P8VREG
R129 1000_1PCT_.125W
12B1> 4A3> DATABUS<15..0>
AUDIO FILTER CS* 31 J1
SACONTROLCS* 26 J1
R111 1000_.1PCT_.125W
MODCALAUDIO 7B8< 8C8<
M12
R181 1000_30PCT_.200W
U49 MC34081
VEE=M12; VCC=P12;
26 J2 SYSCLK
BSYSCLK 12B4<
59 J2 GND
SCOPESEL1
SCOPESEL2
SCOPESEL3
R53 475_1PCT_.125W
U20 74ACT374
GND=GND; VCC=P5;
SCOPEGN1X10 9B8<
SCOPEGAINX2 10D8<
SCOPEGAINX5 10C8<
SCOPEGN2X10 10D5<
SCATTENDIV10 9B6<
R200 475_1PCT_.125W
U64 74ACT374
GND=GND; VCC=P5;
42 P1 WATT ADD LATCH1*
46 P1 VERNIER LATCH1*
44 P1 WATT DATA EN*
43 P1 WATT ADD LATCH2*
52 P1 CAL LATCH 2*
50 P1 CAL LATCH1*
48 P1 VERNIER LATCH2*
R245 475_1PCT_.125W
U79 74ACT374
GND=GND; VCC=P5;
86 P1 AUDIO FL/LIN SPARE1
89 P1 GEN LIN2
88 P1 GEN LIN1
87 P1 MON FM/(AM)*
93 P1 AUDIO LPF2
92 P1 AUDIO LPF1
91 P1 AUDIO HPF2
90 P1 AUDIO HPF1
R240 475_1PCT_.125W
U74 74ACT374
GND=GND; VCC=P5;
15 P1 SA BW 1
21 P1 SA SWEEP WIDTH2
19 P1 SA SWEEP WIDTH1
17 P1 SA BW 2
29 P1 SA CAL LATCH*
27 P1 SA SPARE3
25 P1 SA SWEEP WIDTH4
23 P1 SA SWEEP WIDTH3
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252
SIZE D CAGE CODE 94990 DWG NO 63-P30942C REV C
SCALE NONE SHEET 6
ASME Y14.1-1995 DRAWING FORMAT - 3/95
DRAWING 63P30942C_C
63P30942C_C
LAST_MODIFIED=Fri Aug 18 18:14:12 1995
CONCEPT
DSIZEPAGE2MD2C



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252	SIZE	CAGE CODE	DWG NO	REV
	D	94990	63-P30942C	C
	SCALE NONE		SHEET 7	

ASME Y14.1-1995 DRAWING FORMAT - 3/95

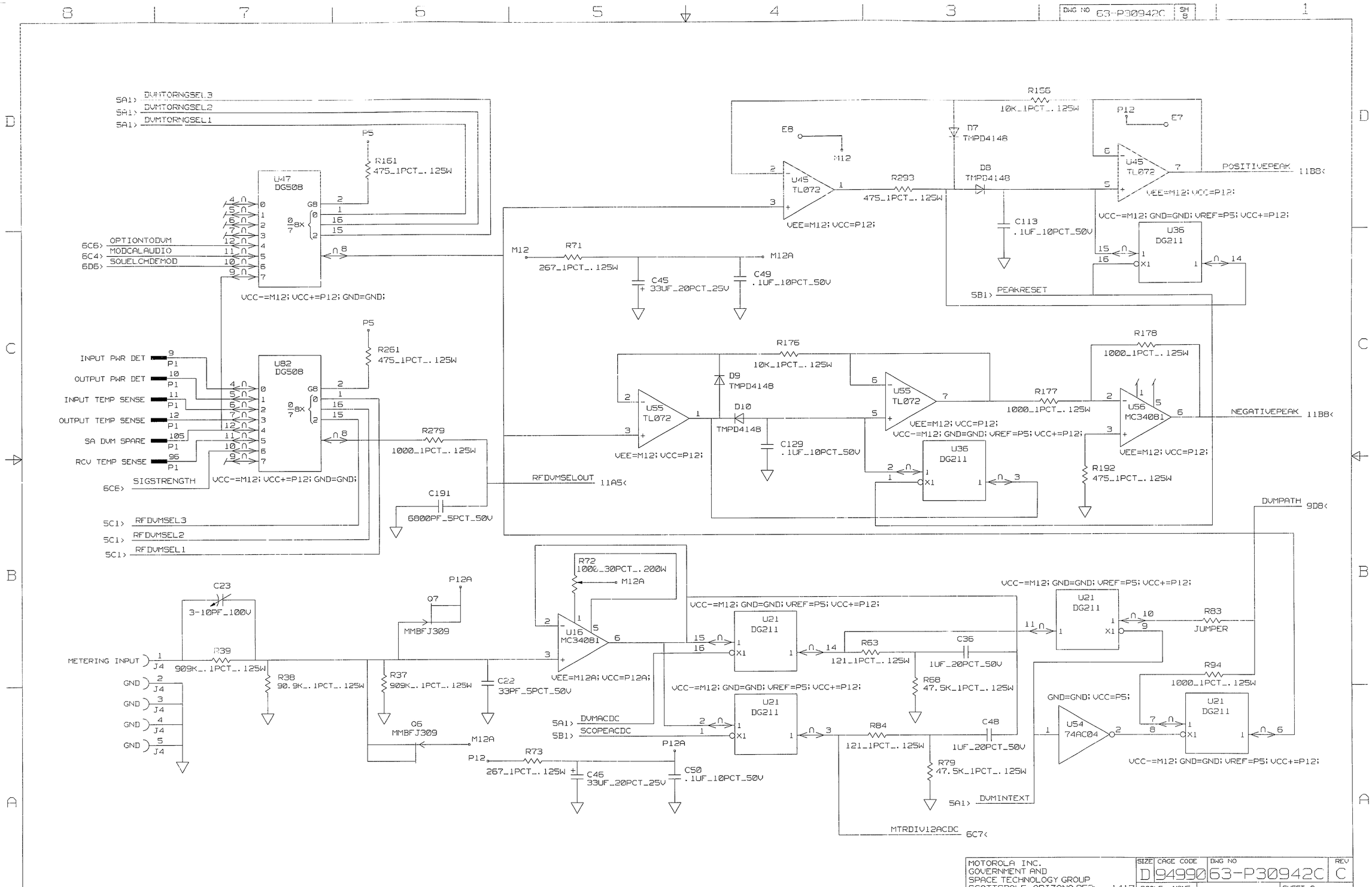
DRAWING 63P30942C_C 63P30942C_C

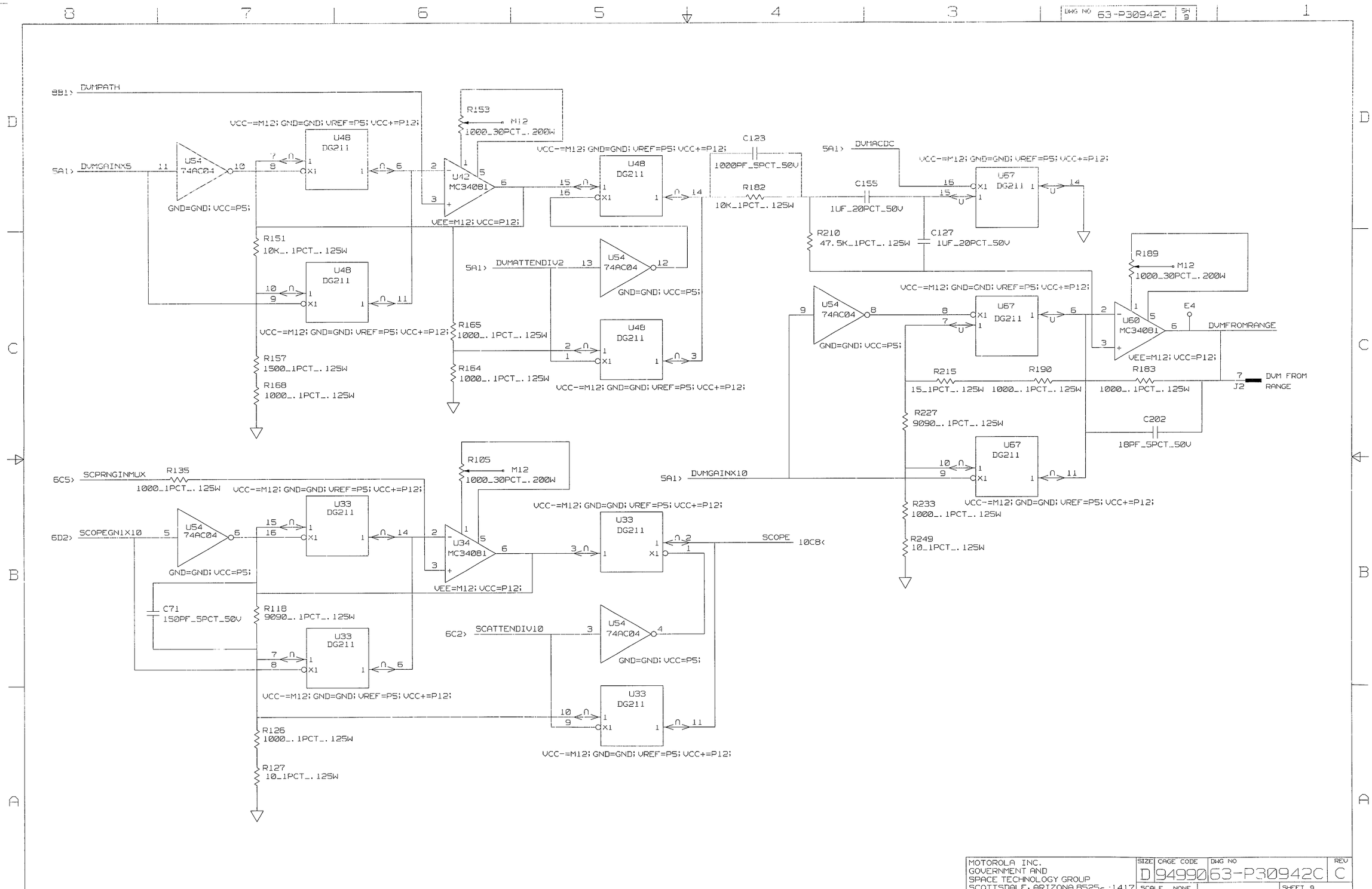
LAST_MODIFIED=Fri Aug 18 18:16:48 1995

CONCEPT

TITAA

DSIZEPAGE2HD2C


DWG NO 63-P30942C SH 8
5A1> DVMTORNGSEL3
5A1> DVMTORNGSEL2
5A1> DVMTORNGSEL1
P5
R161
475_1PCT_.125W
U47
DG508
6C6> OPTIONTODVM
6C4> MODCALAUDIO
6D6> SQUELCHDEMOD
VCC-=M12; VCC+=P12; GND=GND;
U82
DG508
INPUT PWR DET
OUTPUT PWR DET
INPUT TEMP SENSE
OUTPUT TEMP SENSE
SA DVM SPARE
RCV TEMP SENSE
6CE> SIGSTRENGTH
R261
475_1PCT_.125W
R279
1000_1PCT_.125W
C191
6800PF_5PCT_50V
RFDVMSELOUT 11A5<
5C1> RFDVMSEL3
5C1> RFDVMSEL2
5C1> RFDVMSEL1
M12
R71
267_1PCT_.125W
M12A
C45
33UF_20PCT_25V
C49
.1UF_10PCT_50V
R156
10K_1PCT_.125W
D7
TMPD4148
D8
TMPD4148
E8
U45
TL072
R293
475_1PCT_.125W
VEE=M12; VCC=P12;
C113
.1UF_10PCT_50V
P12
E7
POSITIVEPEAK 11B8<
VCC-=M12; GND=GND; VREF=P5; VCC+=P12;
U36
DG211
5B1> PEAKRESET
R176
10K_1PCT_.125W
D9
TMPD4148
D10
TMPD4148
U55
TL072
C129
.1UF_10PCT_50V
R177
1000_1PCT_.125W
R178
1000_1PCT_.125W
U56
MC34081
NEGATIVEPEAK 11B8<
R192
475_1PCT_.125W
DVMPATH 9D8<
C23
3-10PF_100V
METERING INPUT
J4
R39
909K_.1PCT_.125W
R38
90.9K_.1PCT_.125W
GND
Q7
MMBFJ309
P12A
R37
909K_.1PCT_.125W
C22
33PF_5PCT_50V
Q6
MMBFJ309
R72
1000_30PCT_.200W
U16
MC34081
VEE=M12A; VCC=P12A;
5A1> DVMACDC
5B1> SCOPEACDC
R73
267_1PCT_.125W
C46
33UF_20PCT_25V
C50
.1UF_10PCT_50V
R63
121_1PCT_.125W
C36
1UF_20PCT_50V
R68
47.5K_1PCT_.125W
R84
121_1PCT_.125W
C48
1UF_20PCT_50V
R79
47.5K_1PCT_.125W
5A1> DVMINTEXT
MTRDIV12ACDC 6C7<
U21
DG211
R83
JUMPER
R94
1000_1PCT_.125W
GND=GND; VCC=P5;
U54
74AC04
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D
CAGE CODE 94990
DWG NO 63-P30942C
REV C
SCALE NONE
SHEET 8
ASME Y14.1-1995 DRAWING FORMAT - 3/95
DRAWING 63P30942C_C
LAST MODIFIED Fri Aug 18 19:14:36 1995
CONCEPT
TIFAA
DS12CPAGE2HD2C



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30942C	REV C
	SCALE NONE		SHEET 9	

ASME Y14.1-1995 DRAWING FORMAT - 3/95

DRAWING 63P30942C_C 63P30942C_C LAST_MODIFIED:Fri Aug 18 19:07:53 1995

CONCEPT

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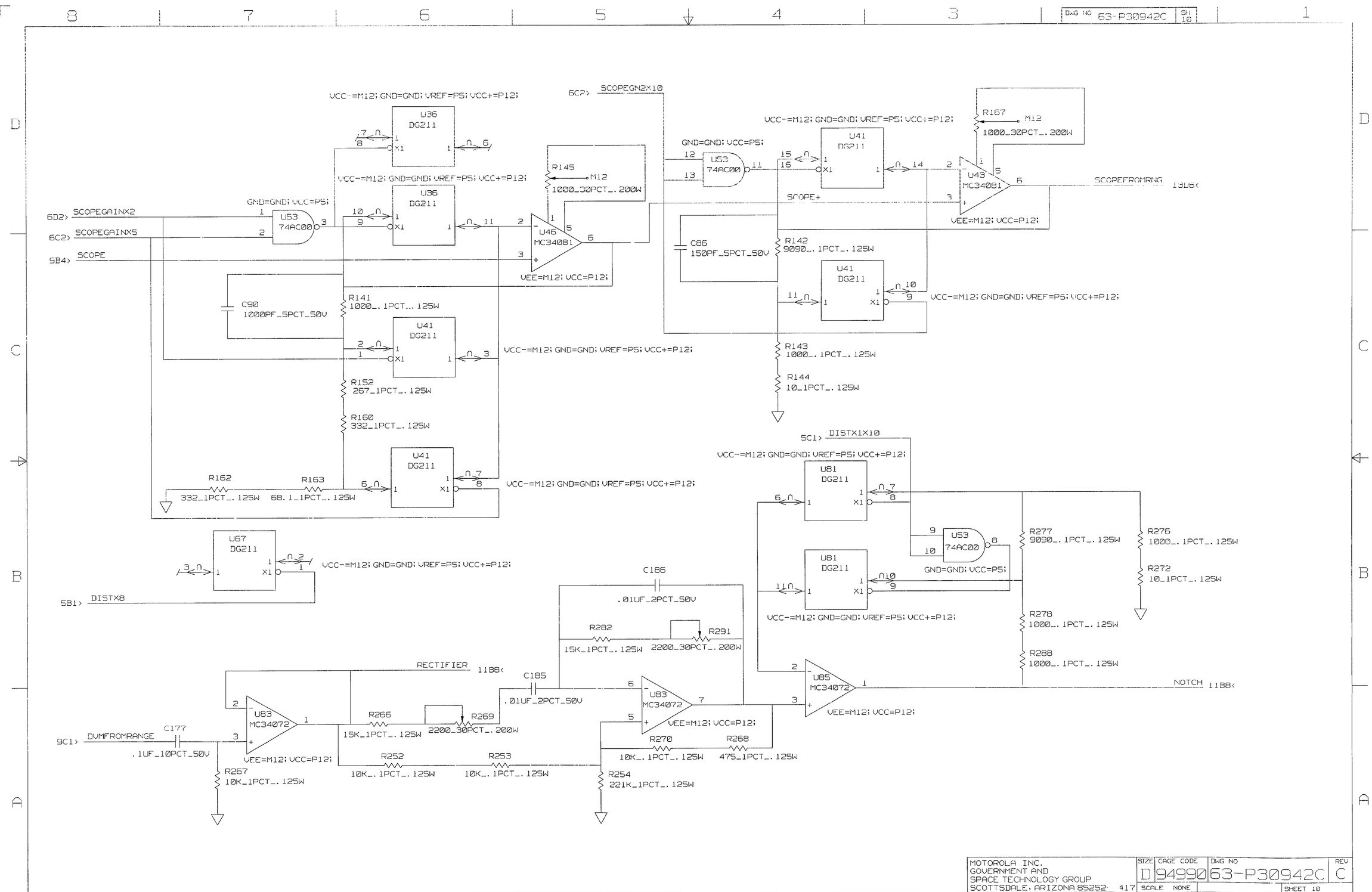
DSIZEPAGE2HD2C



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252 417	SIZE D	CAGE CODE 94990	DWG NO 63-P30942C	REV C
		SCALE NONE		SHEET 10

ASME Y14.1-1995 DRAWING FORMAT - 3/95

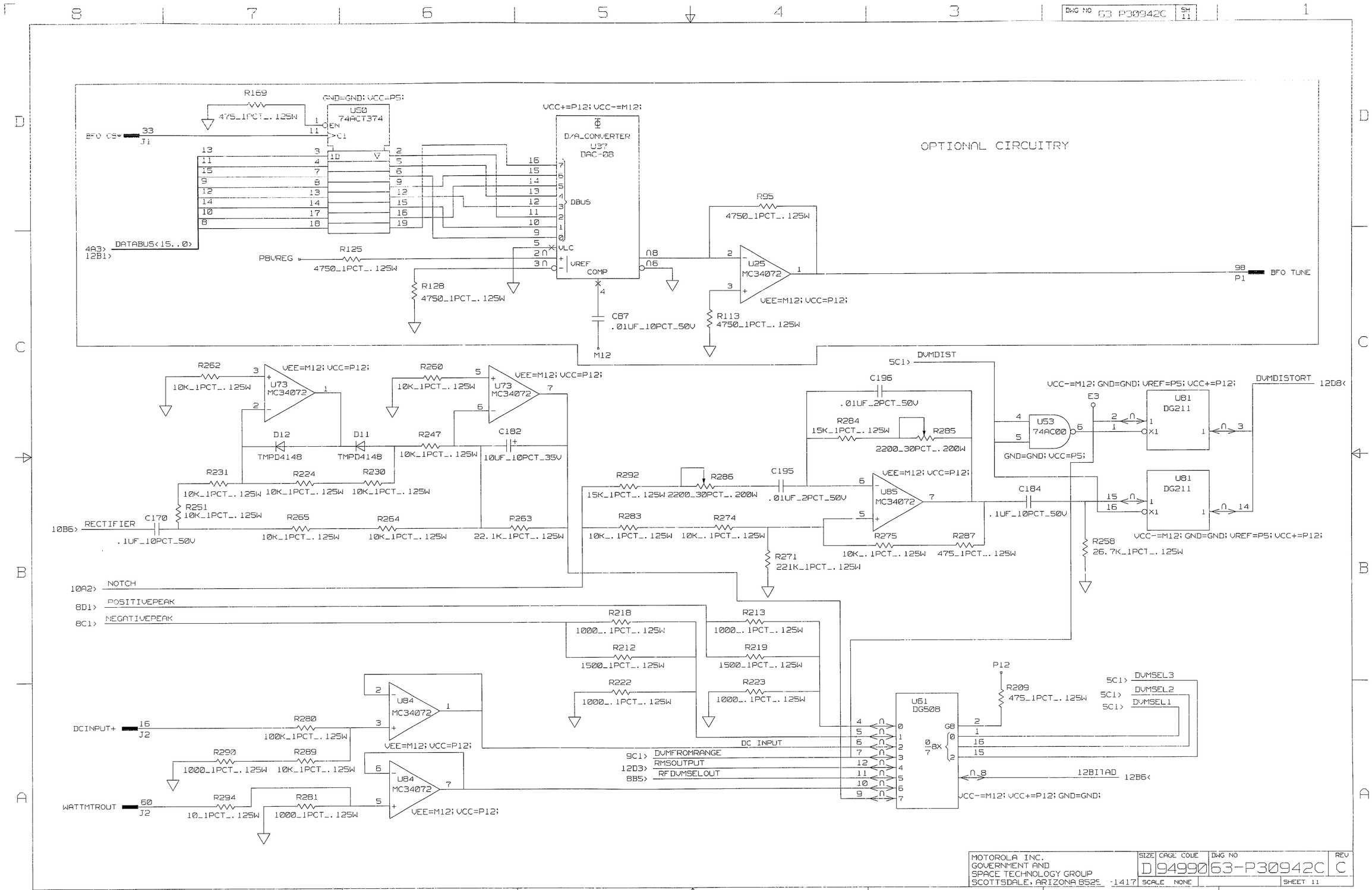
DRAWING 63P30942C_C 63P30942C_C

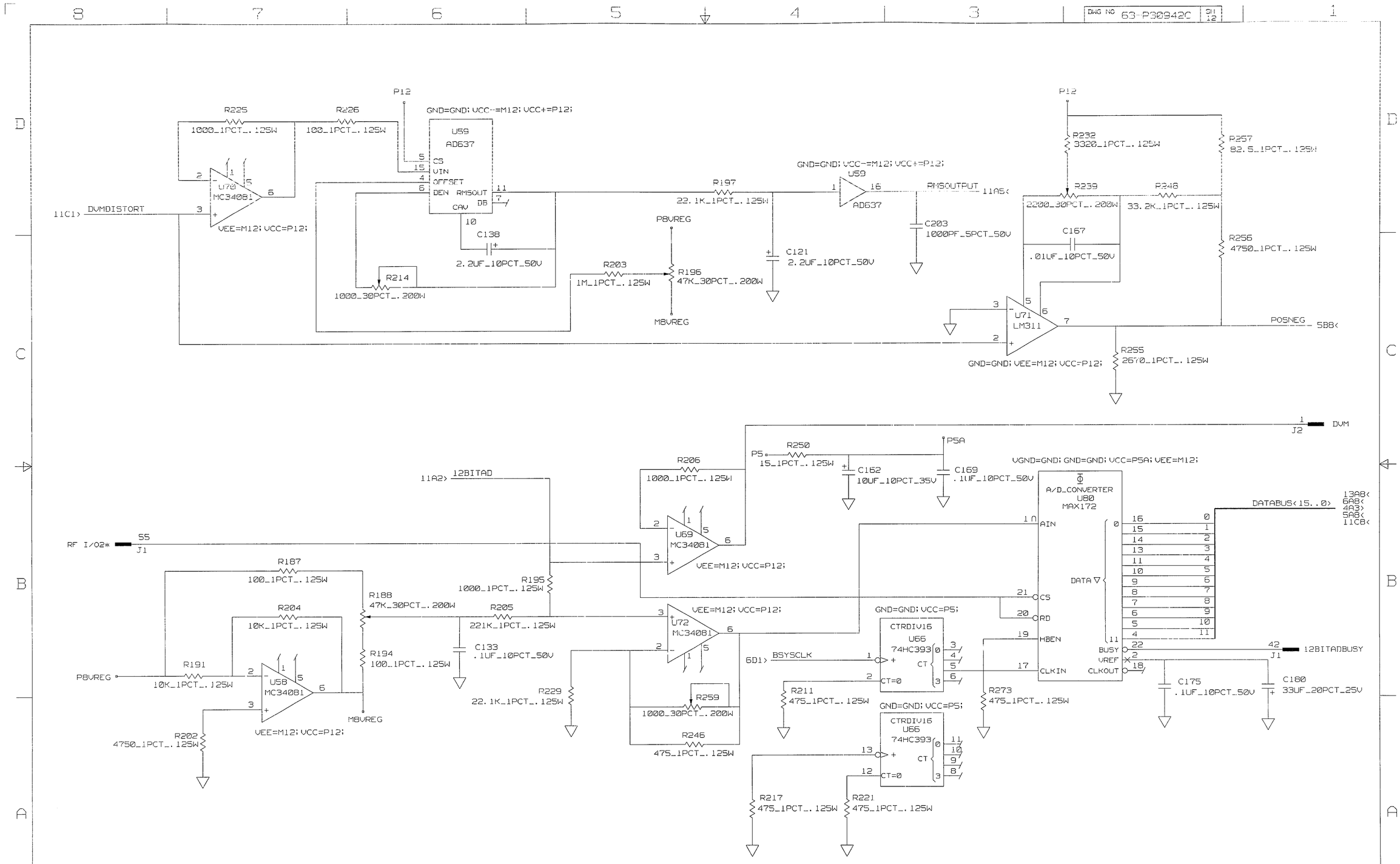
LAST_MODIFIED=Thu Aug 17 12:50:49 1995

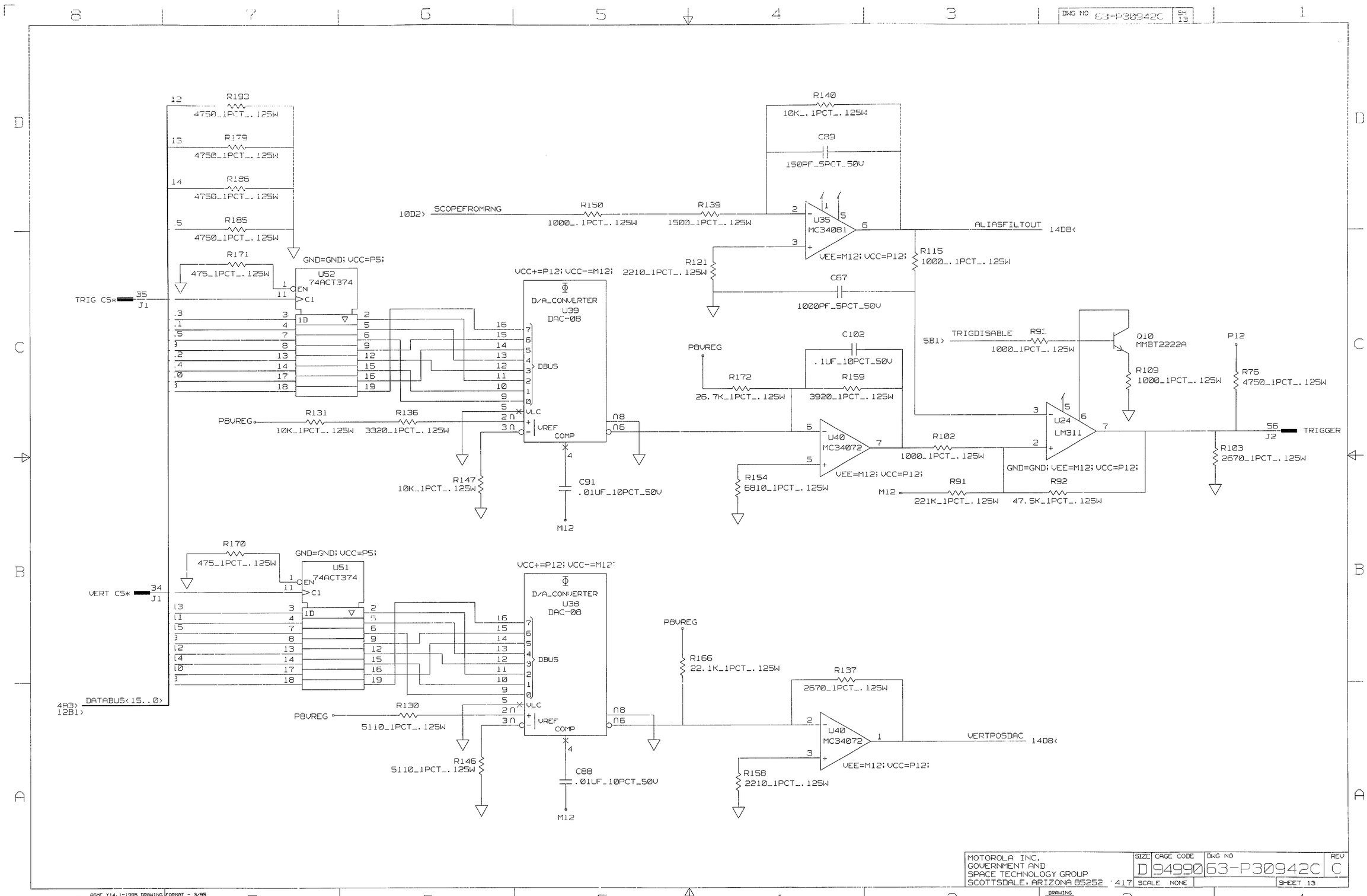
CONCEPT

TIFAA

DSIZEPAGE2HD2C


DWG NO 63 P30942C
SH 11
OPTIONAL CIRCUITRY
R169
475_1PCT_.125W
GND=GND; VCC=P5;
U50
74ACT374
EN
>C1
BFO CS
J1
DATABUS<15..0>
4A3>
12B1>
VCC+=P12; VCC-=M12;
D/A_CONVERTER
U37
DAC-08
DBUS
VLC
VREF
COMP
P8VREG
R125
4750_1PCT_.125W
R128
4750_1PCT_.125W
C87
.01UF_10PCT_50V
M12
R95
4750_1PCT_.125W
U25
MC34072
VEE=M12; VCC=P12;
R113
4750_1PCT_.125W
BFO TUNE
P1
R262
10K_1PCT_.125W
U73
MC34072
VEE=M12; VCC=P12;
R260
10K_1PCT_.125W
D12
TMPD4148
D11
TMPD4148
R247
10K_1PCT_.125W
C182
10UF_10PCT_35V
R231
10K_1PCT_.125W
R224
10K_1PCT_.125W
R230
10K_1PCT_.125W
R251
10K_1PCT_.125W
10B6>
RECTIFIER
C170
.1UF_10PCT_50V
R265
10K_1PCT_.125W
R264
10K_1PCT_.125W
P263
22.1K_1PCT_.125W
R292
15K_1PCT_.125W
R286
2200_30PCT_.200W
C195
.01UF_2PCT_50V
R283
10K_.1PCT_.125W
R274
10K_.1PCT_.125W
R271
221K_1PCT_.125W
5C1>
DVMDIST
C196
.01UF_2PCT_50V
R284
15K_1PCT_.125W
R285
2200_30PCT_.200W
U85
MC34072
VEE=M12; VCC=P12;
R275
10K_.1PCT_.125W
R287
475_1PCT_.125W
C184
.1UF_10PCT_50V
R258
26.7K_1PCT_.125W
VCC-=M12; GND=GND; VREF=P5; VCC+=P12;
U53
74AC00
GND=GND; VCC=P5;
E3
U81
DG211
VCC-=M12; GND=GND; VREF=P5; VCC+=P12;
DVMDISTORT
12D8<
10A2>
NOTCH
8D1>
POSITIVEPEAK
8C1>
NEGATIVEPEAK
R218
1000_.1PCT_.125W
R213
1000_.1PCT_.125W
R212
1500_1PCT_.125W
R219
1500_1PCT_.125W
R222
1000_.1PCT_.125W
R223
1000_.1PCT_.125W
DCINPUT+
J2
R280
100K_1PCT_.125W
U84
MC34072
VEE=M12; VCC=P12;
R290
1000_1PCT_.125W
R289
10K_1PCT_.125W
WATTMTROUT
J2
R294
10_1PCT_.125W
R281
1000_1PCT_.125W
DC INPUT
9C1>
DVMFROMRANGE
12D3>
RMSOUTPUT
8B5>
RFDVMSELOUT
U61
DG508B
P12
R209
475_1PCT_.125W
5C1>
DVMSEL3
DVMSEL2
DVMSEL1
12B11AD
12B6<
VCC-=M12; VCC+=P12; GND=GND;
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 8525 -1417
SIZE D
CAGE CODE 94990
DWG NO 63-P30942C
REV C
SCALE NONE
SHEET 11
ASME Y14.1-1995 DRAWING FORMAT - 3/95
DRAWING
63P30942C_C
63P30942C_C
LAST_MODIFIED=Fri Aug 18 19:05:45 1995
CONCEPT
DSIZEPAGE2HD2C


DWG NO 63-P30942C SH 12
R225 1000_1PCT_.125W
R226 100_1PCT_.125W
P12
GND=GND; VCC-=M12; VCC+=P12;
U59 AD637
CS
VIN
OFFSET
DEN RMSOUT
CAV DB
C138 2.2UF_10PCT_50V
U70 MC34081
VEE=M12; VCC=P12;
11C1> DVMDISTORT
R214 1000_30PCT_.200W
R197 22.1K_1PCT_.125W
R203 1M_1PCT_.125W
P8VREG
R196 47K_30PCT_.200W
M8VREG
C121 2.2UF_10PCT_50V
C203 1000PF_5PCT_50V
RMSOUTPUT 11A5<
R232 3320_1PCT_.125W
R257 82.5_1PCT_.125W
R239 2200_30PCT_.200W
R248 33.2K_1PCT_.125W
C167 .01UF_10PCT_50V
R256 4750_1PCT_.125W
U71 LM311
POSNEG 5B8<
R255 2670_1PCT_.125W
GND=GND; VEE=M12; VCC=P12;
DVM J2
P5A
R250 15_1PCT_.125W
C162 10UF_10PCT_35V
C169 .1UF_10PCT_50V
VGND=GND; GND=GND; VCC=P5A; VEE=M12;
A/D_CONVERTER U80 MAX172
AIN
CS
RD
HBEN
CLKIN
DATA
BUSY
VREF
CLKOUT
DATABUS<15..0> 13A8< 6A8< 2A3> 5A8< 11C8<
12BITADBUSY J1
C175 .1UF_10PCT_50V
C180 33UF_20PCT_25V
11A2> 12BITAD
R206 1000_1PCT_.125W
U69 MC34081
RF I/O2* 55 J1
R187 100_1PCT_.125W
R195 1000_1PCT_.125W
R188 47K_30PCT_.200W
R204 10K_1PCT_.125W
R205 221K_1PCT_.125W
U72 MC34081
C133 .1UF_10PCT_50V
R194 100_1PCT_.125W
P8VREG
R191 10K_1PCT_.125W
U58 MC34081
MBVREG
R202 4750_1PCT_.125W
R229 22.1K_1PCT_.125W
R259 1000_30PCT_.200W
R246 475_1PCT_.125W
6D1> BSYSCLK
CTRDIV16 U66 74HC393
CT=0
R211 475_1PCT_.125W
R273 475_1PCT_.125W
R217 475_1PCT_.125W
R221 475_1PCT_.125W
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-117
SIZE D CAGE CODE 94990 DWG NO 63-P30942C REV C
SCALE NONE SHEET 12
ASME Y14.1-1995 DRAWING FORMAT - 3/95
DRAWING 63P30942C_C 63P30942C_C
LAST_MODIFIED=Fri Aug 18 18:20:02 1995
CONCEPT
DSIZEPAGE=HD2C



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252	SIZE	CAGE CODE	DWG NO	REV
	D	94990	63-P30942C	C
	SCALE NONE		SHEET 13	

ASME Y14.1-1995 DRAWING FORMAT - 3/95

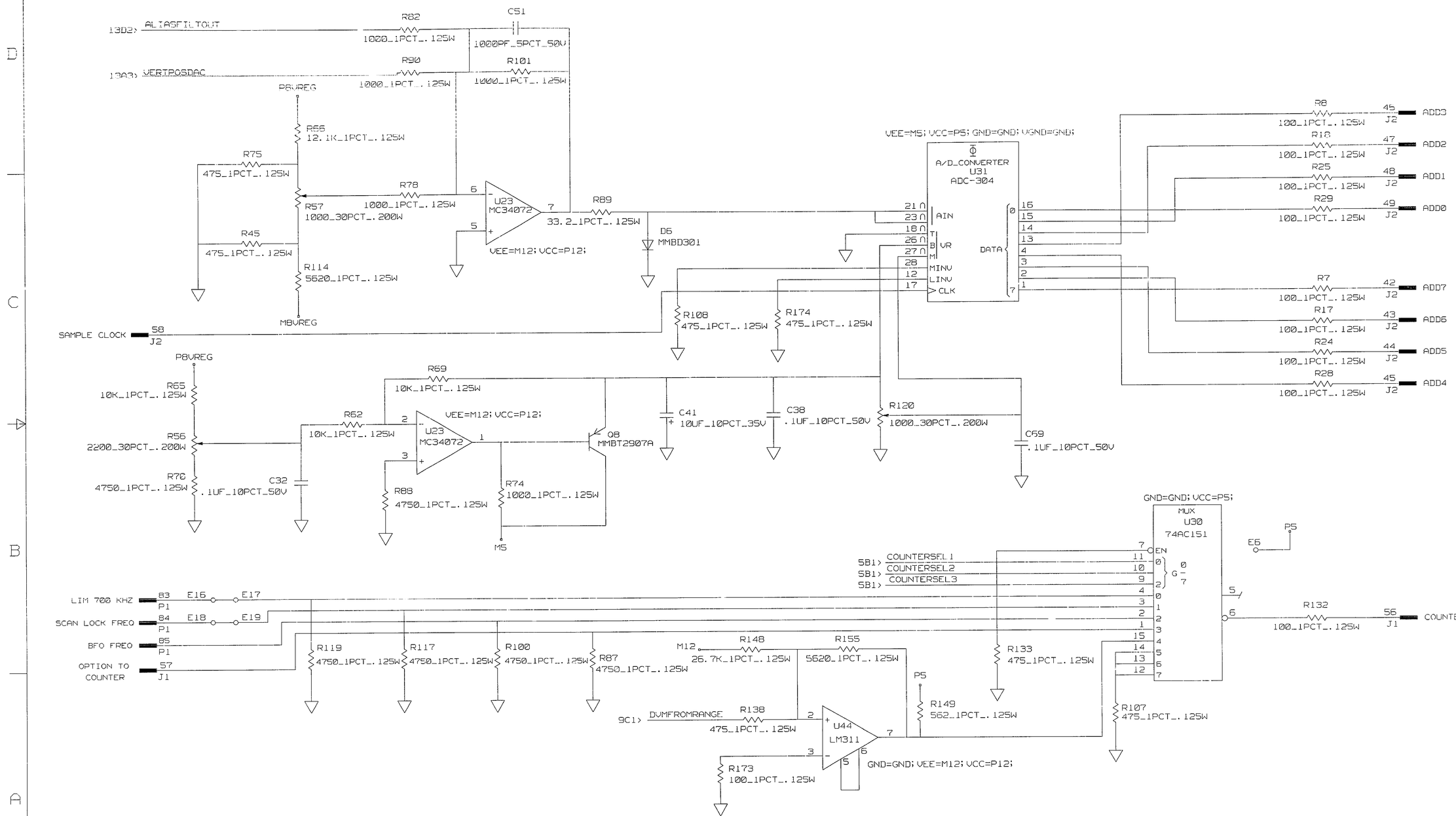
DRAWING 63P30942C_C 63P30942C_C

LAST_MODIFIED=Fri Aug 18 18:21:10 1995

CONCEPT

TITAN

DSIZEPAGE2HDRC



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252	SIZE	CAGE CODE	DWG NO	REV
	D	94990	63-P30942C	C
	SCALE NONE			SHEET 14

ASME Y14.1-1995 DRAWING FORMAT - 3/95

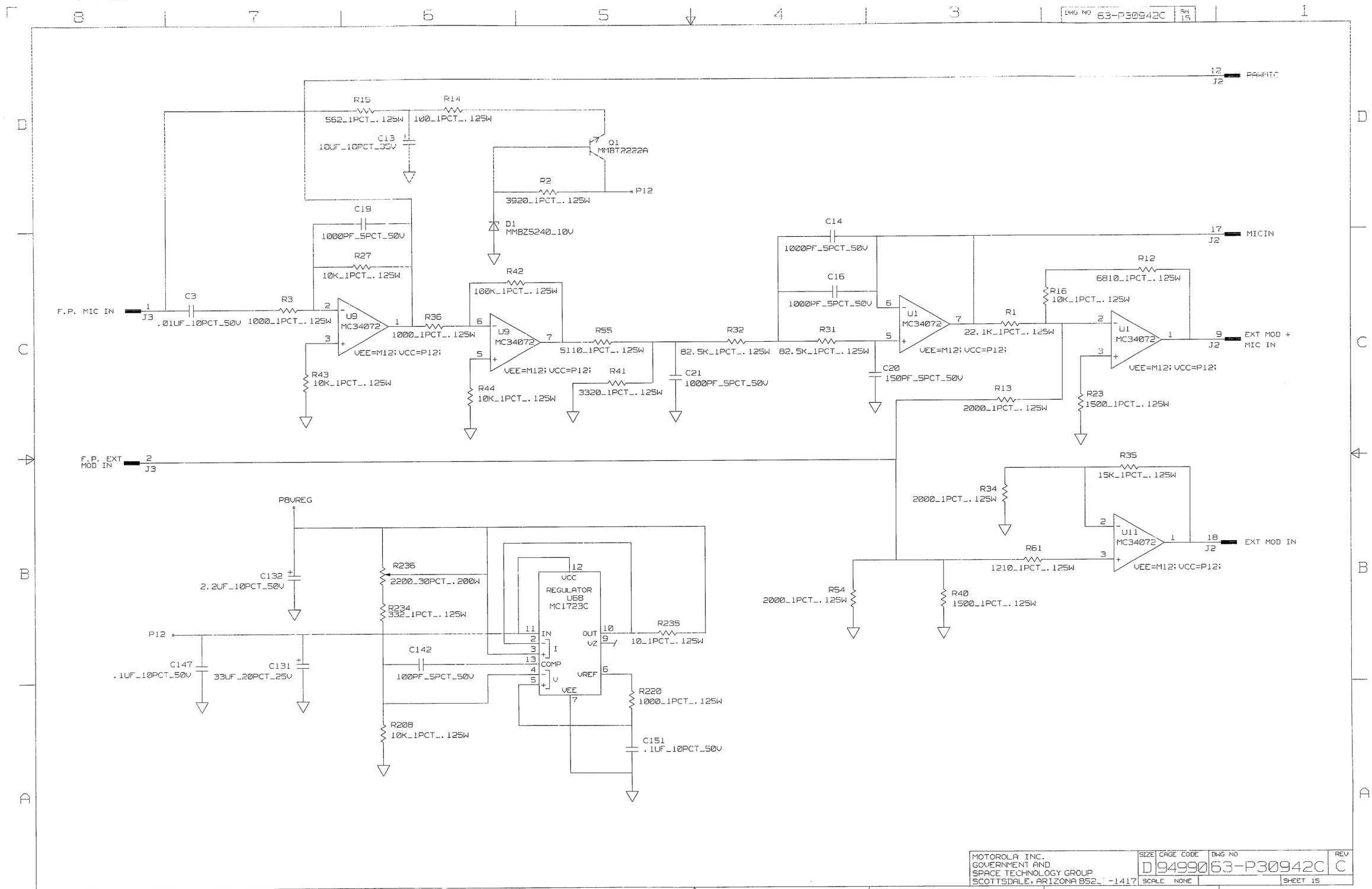
DRAWING 63P30942C_C 63P30942C_C

LAST_MODIFIED=Fri Aug 18 19:03:27 1995

CONCEPT

TITAN

DSIZEPAGE2H02C



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 852_ -1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30942C	REV C
	SCALE NONE		SHEET 15	

ASME Y14.1-1995 DRAWING FORMAT - 3/95

DRAWING 63P30942C_C 63P30942C_C

LAST_MODIFIED=Fri Aug 18 18:25:55 1995

CONCEPT

TIFAA

DSIZEPAGE2HD2C

A.G.R.D.

MOTOROL.
SPACE AND SYSTEMS
TECHNOLOGY GROUP

SIZE SHEETS

ASSOC LIST:
DOC:

	RESP. ENGINEER
SIGNATURES	
DATE	
PHONE/AREA	

9.12.00

FILE
MFG. ENG.
MATL.
QA
TEST

G. X5
EGRA
S/M
S/C
MFG. PLNR.

FROM REPRO :
PDO DIST :
PRINTS DIST :

PRODUCT DEFINITION ORDER

CONTRACT NO.

REFER TO SPP-17 SERIES FOR FORM INSTRUCTIONS

EQUIPMENT P.I.A. NO.(S)	P.I.A.PROGRAM TITLE
10744	COCHISE

DOCUMENTATION CHARGE NO. 10744-1100

	A	DISTRIBUTE PRINT WITH RN
	B	INCORP IMMED AFTER MCO DIST
	C	DIST CHANGED PRINT WITH MCO
	D	ACCUMULATE CHANGE-DISTR MCO
X	E	DISTRIBUTE VA

RETURN DOC ORIG TO: DC

RETURN PDO ORIG TO: DC

DISTRIBUTION CODE	REPRODUCTION QTY C	P	A	D	F
1103-04	5				

CHANGE CLASSIFICATION

X	NOT APPLICABLE
	CLASS I
	CLASS II

GOVT APPVL OF CLASS: N/A DATE

CUST APPROVAL OF CLASS: N/A DATE

INTERCHANGEABILITY STATUS

	NOT APPLICABLE
	TWO-WAY
X	NON

APPROVAL REQUIRED

CUST		YES	X	NO
GOVT		YES	X	NO
PRG MGR		YES	X	NO
PRG MGR		YES	X	NO

PROJECT INCORP CHECK REQUIRED BY EXT

REMARKS:

Carolyn Galligan 441-1824

DOCUMENT OR PART NO. 01-P30940C001,003 CLASSIFIED DOC

PRESENT REVISION	NEW REVISION
C	~

ASSOCIATED LIST PL WL

TITLE CIRCUIT CARD ASSEMBLY INTERFACE

NEXT HIGHER ASSY PART NO(S) 01-P30203C001, 01-P57060J001

APPVL	ORIGINAL	REVISION R1	REVISION R2
ORIG	A. GATTO		
DATE	9/5/00		
EXT NO	1-6924		
R&D	A. Gatto		
DATE	9/5/2000		
MFG	[illegible]		
DATE	9-5-2000		
MATL	W. [illegible]		
DATE	9-5-00		
QA	T. [illegible]		
DATE	9/6/00		
TEST	B. [illegible]		
DATE	9-5-00		
CDM	C. [illegible]		
DATE	9-6-00		

MASTER CHANGE ORDER	MCO			DASH
CHANGE ORDER	CO		-	
RELEASE NOTICE	RN		-	
VARIATION AUTHORITY	VA	X	B35551 -194	
STOP ORDER	SO		-	
INFORMATION MEMO	IM		-	

THERE ARE ✓ RELATED DASH NUMBERS TO BASIC NO

THIS CHANGE CANCELS VA OR SO NO.

SOFTWARE IMPACTS

OPERATIONAL SOFTWARE	YES		NO	X
TEST SOFTWARE	YES		NO	X

HARDWARE EFFECTIVITY

TYPE	FIRM		PLANNED	X	RECORD	
LEVEL	END ITEM		SUB-ASSY	X	PART	
CONT NO	01-P30940C001					
C.I. NO.						
S/N						
LOT						
DATE						
REWORK	NO		YES	X	SEE BELOW	X
RETROFIT						

MAT'L DISPOSITION/MFG. EFFECTS

NONE

EFFECTIVE IMMEDIATELY ON THE FOLLOWING:
1. ALL INTERFACE ASSEMBLIES INSTALLED IN R2600D (01-P57060J) MODELS.
2. INTERFACE ASSEMBLIES USED IN R2600C (01-P30203C) MODELS RETROFITTED TO R2600D SPECIFICATIONS - (01-P57100J PROCESSOR INSTALLED)

NO. B35551-194

SERVICE CENTER DISTRIBUTION YES X NO

FORMAT USED:
CADAM CATIA ALLEGRO PRO-E META
WP5 W5.1 WORD DESIGNER

REASON FOR ORDER:

1. MODIFY INTERFACE CARD TO MAKE IT COMPATIBLE WITH NEW R2600D (01-P57060J) HARDWARE CONFIGURATION.

*COMPUTER GENERATED EXCEL 4.0

B35551-194-01

SPACE SYSTEMS TECHNOLOGY GROUP

PRODUCT DEFINITION ORDER

CONTINUATION SHEET

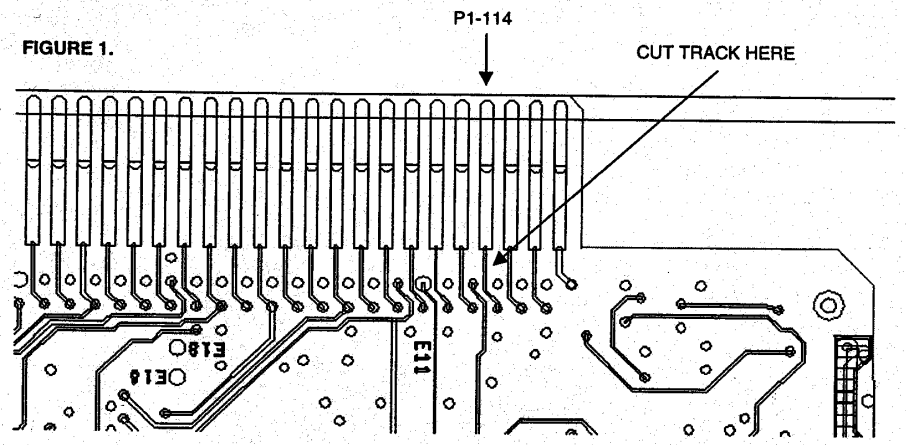
ITEM	DOCUMENT NO.	REV	OWC	DESCRIPTION	DOC SIZE	NEXT HIGHER ASSY.
	01-P30940C	C		CIRCUIT CARD ASSEMBLY - INTERFACE		VARIOUS

			BASIC NO.		REV
MASTER CHANGE ORDER	MCO			DASH	
CHANGE ORDER	CO		-		
RELEASE NOTICE	RN		-		
VARIATION AUTHORITY	VA	X	B35551	- 194	
STOP ORDER	SO		-		
INFORMATION MEMO	IM		-		
DOCUMENT/PART REF NO					

MAT'L DISPOSITION /MFG. EFFECTS CONT.

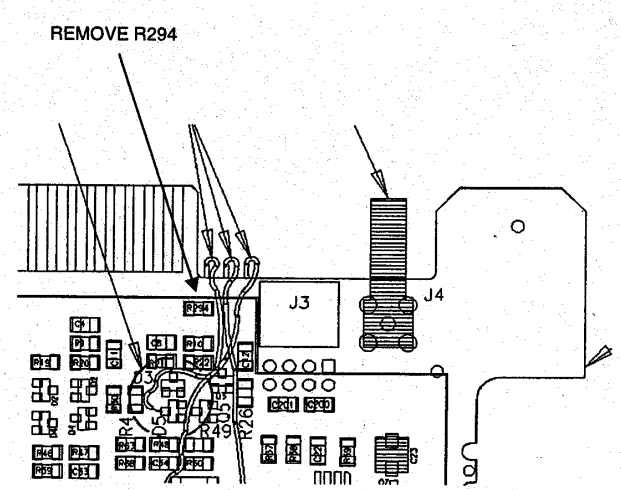
1. CUT TRACK BETWEEN P1-114 AND VIA HOLE ON PWB AS SHOWN IN FIGURE 1.
ON R2600D MODELS "SYSCLK" SIGNAL NOW ORIGINATES ON 01-P57100J MICROPROCESSOR ASSY.
THIS MODIFICATION REDUCES 10 MHZ NOISE IN THE RF CARDCAGE.

FIGURE 1.



2. REMOVE R294 (P/N 0611077D01 10 - 1 - .125) AS SHOWN IN FIGURE 2.
ON R2600D MODELS THIS FREES J2-60 (EXISITING "WATTMTROUT" SIGNAL)
FOR FLASH MEMORY UNLOCK USE. NEW SIGNAL NAME IS "OPTFLASH_UNLOCK"

FIGURE 2.



QTY PER	VENDOR NAME	FIND NO.	QTY REQ	CODE IDENT NO	DRAWING OR DOCUMENT NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	SUPPLEMENTARY PART OR IDENTIFYING NO	NOTES

*COMPUTER GENERATED EXCEL 4.0

NO. B35551-194

MOTOR
SPACE AND SYSTEMS
TECHNOLOGY GROUP

10-20-00

SIZE SHEETS

ASSOC LIST:
DOC:

	RESP. ENGINEER
SIGNATURES	A. Gatto
DATE	10/13/2000
PHONE/AREA	441-6924

FILE
MFG. ENG.
MATL.
QA
TEST

FG. X5
INTEGRA
S/M
S/C
MFG. PLNR.

PRODUCT DEFINITION ORDER

CONTRACT NO.

FROM REPRO :
PDO DIST :
PRINTS DIST :

REFER TO SPP-17 SERIES FOR FORM INSTRUCTIONS

EQUIPMENT P.I.A. NO.(S)	P.I.A.PROGRAM TITLE
10744	COCHISE

DOCUMENTATION CHARGE NO. 10744-1100

	A	DISTRIBUTE PRINT WITH RN
	B	INCORP IMMED AFTER MCO DIST
	C	DIST CHANGED PRINT WITH MCO
	D	ACCUMULATE CHANGE-DISTR MCO
X	E	DISTRIBUTE VA

RETURN DOC ORIG TO DC
RETURN PDO ORIG TO DC

DISTRIBUTION CODE	REPRODUCTION QTY C	P	A	D	F
1103-04	15				

CHANGE CLASSIFICATION

	NOT APPLICABLE
X	CLASS I
	CLASS II

GOVT APPVL OF CLASS: N/A DATE

CUST APPROVAL OF CLASS: N/A DATE

INTERCHANGEABILITY STATUS

	NOT APPLICABLE
X	TWO-WAY
	NON

APPROVAL REQUIRED

CUST		YES	X	NO
GOVT		YES	X	NO
PRG MGR		YES	X	NO
PRG MGR		YES	X	NO

PROJECT INCORP CHECK REQUIRED BY EXT

REMARKS:

Carolyn Galligan 441-1824

DOCUMENT OR PART NO. 01-P30940C001,003 CLASSIFIED DOC

PRESENT REVISION	NEW REVISION
C	~

ASSOCIATED LIST PL WL

TITLE CIRCUIT CARD ASSEMBLY INTERFACE

NEXT HIGHER ASSY PART NO(S) 01-P30203C001, 01-P57060J001

APPVL	ORIGINAL	REVISION R1	REVISION R2
ORIG	A. GATTO		
DATE	10/5/00		
EXT NO	1-6924		
R&D	A. Gatto		
DATE	10/5/2000		
MFG	[illegible]		
DATE	10-6-2000		
MATL	[illegible]		
DATE	10-6-00		
QA	T. Bowers		
DATE	10/17/00		
TEST	B. Watts		
DATE	10-6-00		
CDM	C. Galligan		
DATE	10-17-00		

MASTER CHANGE ORDER	MCO			DASH
CHANGE ORDER	CO			-
RELEASE NOTICE	RN			-
VARIATION AUTHORITY	VA	X	B35551	-197
STOP ORDER	SO			-
INFORMATION MEMO	IM			-

THERE ARE ___ RELATED DASH NUMBERS TO BASIC NO
THIS CHANGE CANCELS VA ___ OR SO ___ NO.

BASIC NO. REV

SOFTWARE IMPACTS

OPERATIONAL SOFTWARE	YES		NO	X
TEST SOFTWARE	YES		NO	X

HARDWARE EFFECTIVITY

TYPE	FIRM		PLANNED	X	RECORD	
LEVEL	END ITEM		SUB-ASSY	X	PART	
CONT NO	01-P30940C001					
C.I. NO.						
S/N						
LOT						
DATE						
REWORK	NO		YES	X	SEE BELOW	X
RETROFIT						

MAT'L DISPOSITION/MFG. EFFECTS

NONE

EFFECTIVE IMMEDIATELY ON ALL R26XX SYSTEMS FORWARD
REWORK/RETROFIT ALL WIP AND BONDED SYSTEMS FOR DELIVERY TO INS CUSTOMER.

REASON FOR ORDER:

MODIFY INTERFACE CARD TO REDUCE NOISE DURING FM DEVIATION MEASUREMENT IN WIDEBAND MODE.
PEAK DETECTOR RESET RECONFIGURED TO REDUCE NOISE SPIKES DURING SAMPLING.

FOR BEST PERFORMANCE THIS MODIFICATION SHOULD BE DONE IN CONJUNCTION WITH MCO L48746 ON PL01-P30680C WHICH UGRADES AN IC AMPLIFIER ON THAT ASSEMBLY TO A LOWER NOISE TYPE.

SERVICE CENTER DISTRIBUTION YES X NO

FORMAT USED:
CADAM CATIA ALLEGRO PRO-E META
WP5 W5.1 WORD DESIGNER

NO. B35551-197

*COMPUTER GENERATED EXCEL 4.0

B35551-197-01

PRODUCT DEFINITION ORDER

CONTINUATION SHEET

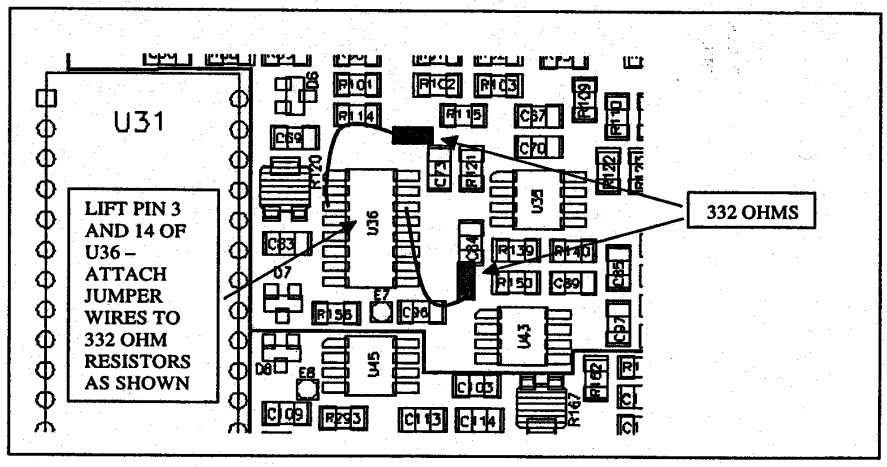
ITEM	DOCUMENT NO.	REV	OWC	DESCRIPTION	DOC SIZE	NEXT HIGHER ASSY.
	01-P30940C	C		CIRCUIT CARD ASSEMBLY - INTERFACE		VARIOUS

			BASIC NO.		REV
MASTER CHANGE ORDER	MCO			DASH	
CHANGE ORDER	CO		-		
RELEASE NOTICE	RN		-		
VARIATION AUTHORITY	VA	X	B35551 - 197		
STOP ORDER	SO		-		
INFORMATION MEMO	IM		-		
DOCUMENT/PART REF NO		01-P30940C001, 003			

MAT'L DISPOSITION /MFG. EFFECTS CONT.

1. Lift pins 3 and 14 of U36 from PWB pads.
2. Solder one side of P/N 06611077E48 (332 - 1 - .125) to PWB ground side of C73 as shown in FIGURE 1.
3. Solder a 30 GAUGE insulated jumper wire from pin 3 of U36 to other side of 332 OHM resistor attached to C73 as shown in FIGURE 1.
4. Solder one side of P/N 06611077E48 (332 - 1 - .125) to PWB ground side of C84 as shown in FIGURE 1.
5. Solder a 30 GAUGE insulated jumper wire from pin 14 of U36 to other side of 332 OHM resistor attached to C84 as shown in FIGURE 1.

FIGURE 1: TOP (COMPONENT SIDE) VIEW OF 01-P30940C PWB.



QTY PER	VENDOR NAME	FIND NO.	QTY REQ	CODE IDENT NO	DRAWING OR DOCUMENT NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	SUPPLEMENTARY PART OR IDENTIFYING NO	NOTES

*COMPUTER GENERATED EXCEL 4.0

NO. B35551-197

MOTOROLA
SPACE AND SYSTEMS
TECHNOLOGY GROUP

SIZE SHEETS
ASSOC LIST:
DOC:

	RESP. ENGINEER
SIGNATURES	A. Gatto
DATE	10/20/2000
PHONE/AREA	1-6924

10-26-00

FILE
MFG. ENG.
MATL.
QA
TEST

G. X5
INTEGRA
S/M
S/C
MFG. PLNR.
FROM REPRO:
PDO DIST:
PRINTS DIST:

PRODUCT DEFINITION ORDER

CONTRACT NO.

REFER TO SPP-17 SERIES FOR FORM INSTRUCTIONS

EQUIPMENT P.I.A. NO.(S)	P.I.A.PROGRAM TITLE
10744	COCHISE

DOCUMENTATION CHARGE NO. 10744-1100

	A	DISTRIBUTE PRINT WITH RN
	B	INCORP IMMED AFTER MCO DIST
	C	DIST CHANGED PRINT WITH MCO
	D	ACCUMULATE CHANGE-DISTR MCO
X	E	DISTRIBUTE VA

RETURN DOC ORIG TO: DC
RETURN PDO ORIG TO: DC

DISTRIBUTION CODE	REPRODUCTION QTY C	P	A	D	F
1103-04	15				

CHANGE CLASSIFICATION

	NOT APPLICABLE
	CLASS I
X	CLASS II

GOVT APPVL OF CLASS: N/A DATE
CUST APPROVAL OF CLASS: N/A DATE

INTERCHANGEABILITY STATUS

	NOT APPLICABLE
X	TWO-WAY
	NON

APPROVAL REQUIRED

CUST		YES	X	NO
GOVT		YES	X	NO
PRG MGR		YES	X	NO
PRG MGR		YES	X	NO

PROJECT INCORP CHECK REQUIRED BY EXT

REMARKS:
Carolyn Galligan 441-1824

DOCUMENT OR PART NO.	CLASSIFIED DOC
01-P30940C001,003	

PRESENT REVISION	NEW REVISION
C	~

ASSOCIATED LIST PL WL

TITLE: CIRCUIT CARD ASSEMBLY INTERFACE

NEXT HIGHER ASSY PART NO(S): 01-P30203C001, 01-P57060J001

APPVL	ORIGINAL	REVISION R1	REVISION R2
ORIG	A. GATTO		
DATE	10/20/00		
EXT NO	1-6924		
R&D	A. Gatto		
DATE	10/20/2000		
MFG	J Planck		
DATE	10-20-2000		
MATL	W. Mathews		
DATE	10-20-00		
QA	T Dayno		
DATE	10/20/00		
TEST	B. Watts		
DATE	10-20-00		
CDM	C. Galligan		
DATE	10-20-00		

MASTER CHANGE ORDER	MCO		DASH
CHANGE ORDER	CO		-
RELEASE NOTICE	RN		-
VARIATION AUTHORITY	VA	X	B35551 -199
STOP ORDER	SO		-
INFORMATION MEMO	IM		-

THERE ARE / RELATED DASH NUMBERS TO BASIC NO
THIS CHANGE CANCELS VA OR SO NO.

SOFTWARE IMPACTS

OPERATIONAL SOFTWARE	YES		NO	X
TEST SOFTWARE	YES		NO	X

HARDWARE EFFECTIVITY

TYPE	FIRM		PLANNED	X	RECORD	
LEVEL	END ITEM		SUB-ASSY	X	PART	
CONT NO	01-P30940C001,003					
C.I. NO.						
S/N						
LOT						
DATE						
REWORK	NO		YES	X	SEE BELOW	X
RETROFIT						

MAT'L DISPOSITION/MFG. EFFECTS

NONE

EFFECTIVE IMMEDIATELY ON ALL R26XX/D SYSTEMS
REWORK/RETROFIT ALL WIP AND BONDED SYSTEMS

REASON FOR ORDER:

MODIFICATION REDUCES RADIATED EMISSIONS AND SUSCEPTIBILITY WHEN EXTERNAL MICROPHONE IS ATTACHED TO R26XX/D SYSTEMS
THIS CHANGE AND THE MODIFICATION OUTLINED IN VA B35551-200 ARE REQUIRED FOR THE NEW R26XX/D MODEL TO MEET CE SPECIFICATIONS FOR RADIATED EMISSIONS AND SUSCEPTIBILITY.

SERVICE CENTER DISTRIBUTION YES X NO

FORMAT USED:
CADAM CATIA ALLEGRO PRO-E META
WP5 W5.1 WORD DESIGNER

NO. B35551-199

*COMPUTER GENERATED EXCEL 4.0

10-26-00 STAT 10-26-00

B35551-199-01

SPACE SYSTEMS TECHNOLOGY GROUP

PRODUCT DEFINITION ORDER

CONTINUATION SHEET

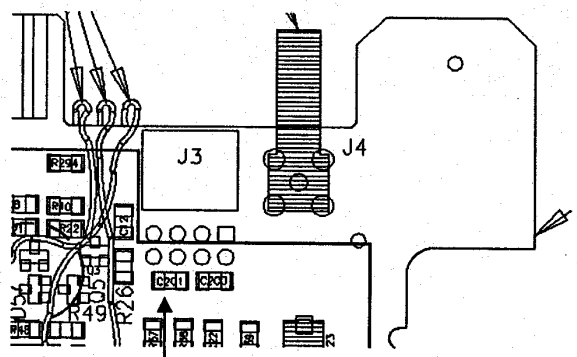
ITEM	DOCUMENT NO.	REV	OWC	DESCRIPTION	DOC SIZE	NEXT HIGHER ASSY.

			BASIC NO.		REV
MASTER CHANGE ORDER	MCO			DASH	
CHANGE ORDER	CO			-	
RELEASE NOTICE	RN			-	
VARIATION AUTHORITY	VA	X	B35551	- 199	
STOP ORDER	SO			-	
INFORMATION MEMO	IM			-	
DOCUMENT/PART REF NO		01-P30940C001, 003			

MAT'L DISPOSITION /MFG. EFFECTS CONT.

1. CHANGE C201 TO P/N 2113740B73 (1000 PF - 5 - 50) AS SHOWN IN FIG. 1.
2. REMOVE .040" TO .060" OF TRACK LEADING TO PIN 7 OF J3 AT LOCATION SHOWN IN FIG. 2A. REMOVE SOLDER MASK APPROX. .040" ON BOTH SIDES OF GAP.
3. SOLDER P/N 24-P26371A112 (.82 UH - 10) ACROSS CUT TRACK AS SHOWN IN FIG. 2B.
4. SOLDER P/N 2113740B73 (1000PF - 5 - 50) ACROSS PIN 1 AND 6 OF J3 AS SHOWN IN FIG. 2B.

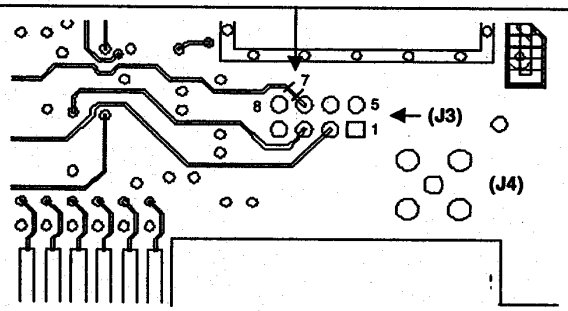
FIG. 1: TOP (COMPONENT SIDE) VIEW OF 01-P30940C PWB.



CHANGE C201 TO P/N 2113740B73 (1000PF - 5 - 50)

FIG. 2A

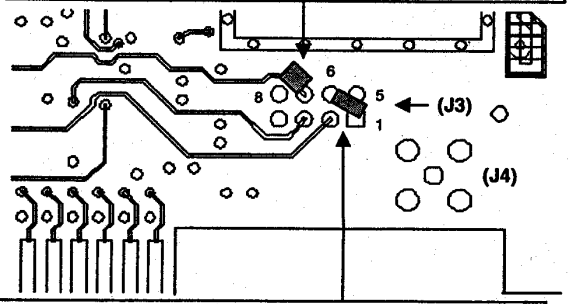
REMOVE .040" TO .060" OF TRACK LEADING TO PIN 7 OF J3 AT LOCATION SHOWN. REMOVE SOLDER MASK APPROX. .040" ON BOTH SIDES OF GAP.



BOTTOM (SOLDER SIDE) VIEW OF 01-P30940C PWB.

FIG. 2B

SOLDER P/N 24-P26371A112 (.82 UH) ACROSS CUT TRACK



SOLDER P/N 2113740B73 (1000PF) ACROSS PIN 1 AND 6 OF J3

QTY PER	VENDOR NAME	FIND NO.	QTY REQ	CODE IDENT NO	DRAWING OR DOCUMENT NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	SUPPLEMENTARY PART OR IDENTIFYING NO	NOTES

*COMPUTER GENERATED EXCEL 4.0

NO. B35551-199

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14.1 GENERAL DESCRIPTION

The Processor Module is designated as A4 and is installed behind the RF card cage.

The Processor Module (part number 01-P57100J) described in this section is used on the R2600D. This Processor module eliminates the CRT interface, PCMCIA interface and the general purpose I/O interface.

This module is the principal controller for the Analyzer. It interfaces with the other modules in the system providing necessary clocks, select lines, and enable lines to perform their specific functions. The Processor Module also performs waveform generation and processing for the baseband audio signals.

14.2 SIGNALS SUMMARY

14.2A Signal Descriptions

14.2A.1 J1 Interface Module (digital signals)

*A/D BUSY** input is used by the processor to generate a DTACK.

*ATTEN CS** output clocks RF Attenuator latch.

*AUDIO FILTER CS** output clocks Audio Filter/ Linearizer latch.

BBD0 – BBD15 bi-directional buffered data of the processor data bus.

*BFO CS** output is reserved for future use.

COUNTER input is used by the processor for both frequency and period counters.

*DVM ATTEN CS** output clocks DVM/Attenuator latch.

*DVM SEL CS** output clocks DVM select latch.

OPTION TO COUNTER pass through signal, not used by processor module.

*OUTPUT SPARE CS** output reserved for future use.

*READ SPARE 1&2 CS** outputs reserved for future use.

*RF I/O 2** output selects the 12 bit A/D converter.

*RF MODE CS** output clocks RF mode latch.

*RF OUTPUT CS** output clocks RF Output latch.

*RF READ CS** output allows processor to read BBD0-7 of the bi-directional data bus.

*RF STATUS CS** output allows processor to read RF status lines.

*SA CONTROL CS** output clocks Spectrum Analyzer Control latch.

*SCOPE ATTENUATOR CS** output clocks Scope Attenuator latch.

*SCOPE CS** output clocks Scope/PK Det/Counter latch.

*STATIC BUS CS** output clocks Static Bus latch.

*SYNTH CS** output clocks the Synth Program latch.

*TRIG CS** output latches upper data bus to D/A converter to provide a trigger voltage level for scope functions.

VBACKUP output from the processor provides +5 volts when the power switch is on and the battery voltage when power is off.

*WRITE BUS CS** output clocks write bus latch.

*VERT CS** output clocks vertical position latch.

14.2A.2 J2 Interface Module and Option Modules (analog signals)

A/D DATA 0-7 inputs to the ASIC are the result of A/D conversion performed on the Interface Module for scope functions.

CONV MOD output is any combination of the internally generated modulation signals, external modulation signals and signals from option modules.

DC INPUT + is routed on the Processor Module from the power connector J7 to J2 and then to the Interface Module where it is monitored.

DEMOD CAL AUDIO input is the unsquelched demodulated audio signal from the Interface Module and is not used by the processor module.

DVM input is a buffered version of the 12 bit A/D input on the Interface Module and is not used by the Processor Module.

DVM FROM RANGE input is the attenuated digital voltmeter signal from the Interface Module.

EXT MOD + MIC IN input is the sum of the External Modulation input and the Microphone input from the Front Panel.

GEN AUDIO output is the calibrated sum of all the audio modulation to be routed to the synthesizer. It is capacitively coupled and buffered by the Interface Module to create MOD CAL AUDIO.

HANDSET AUDIO output signal is from the speaker amplifier and is routed to the Front Panel microphone connector and speaker.

IACK 1-2, IACK 4-7** outputs indicate an interrupt acknowledge cycle has been issued from the processor. These lines are used in conjunction with IRQ 1-7.

INT MOD output is the sum of all internally generated modulation signals.

IRQ 1-2, IRQ 4-7** inputs are the Interrupt Request lines to the MC68000 processor.

OPTION FLASH UNLOCK output is +12 volts for use in boot/sector unlock of flash memory.

MIC IN input from the Interface Module is not used by the processor at this time.

OPT AUDIO RTN 1,2 inputs are reserved for use by the option modules.

OPT MOD RTN 1,3 inputs are reserved for use by the option modules.

OPTION TO DVM output allows signals from option modules to be routed to the DVM.

RAW MIC IN is the microphone input from the Front Panel connector routed through the Interface Module to the Processor Module.

RECEIVE SPEAKER AUDIO input signal is the squelched unfiltered demodulated audio from the receiver routed through the Interface Module.

*BUFFERED RESET** output is used to reset the Analyzer.

SAMPLE CLOCK output signal is the sample clock for the 8-bit A/D on the Interface Module.

SQUELCH input from the Receiver Module indicates whether the receiver is squelched and is used to light a Front Panel LED. This signal is routed through the Interface Module.

SQUELCH LEVEL output is routed through the Processor Module from the Front Panel to the Interface Module. This signal is not used by the processor module.

SQUELCHED DEMOD input is a squelched version of the demodulated receive signal (Demod Cal Audio). It is routed from the Receiver Module through to the Interface Module. This signal is not used by the processor module.

SYSCLK output is the 10MHz reference signal, buffered and reshaped from the Frequency Standard Module.

BUFFERED TIMER CLOCK output is used to generate a clock of varying frequency (76Hz to 5MHz) and is used by the Interface Module to produce the SWEEP signal for the Spectrum Analyzer.

EXT MOD IN input is the buffered external modulation from the front panel.

TRIGGER input signals the ASIC when to start auto sampling the input data (A/D DATA 0-7 from the Interface Module) for scope functions.

VOL CNTL AUDIO output is the sum of the received or transmitted modulation.

*WB/(NM)** input indicates whether the receiver is operating in wideband or narrowband mode.

14.2A.3 J3 Front Panel

ANT PORT ENABLE output indicates which port is enabled when receiving RF. A logic 1 indicates the Antenna Port is enabled and drives a front panel LED.

AUX POWER output is the control signal for the Power Supply (via connector J7). It is routed to a front panel power switch.

BRT H1, BRT ARM, and *BRT LO* are connections for the external brightness potentiometer. The Processor Module only serves as the connection between J3 (front panel) and J6 (Display Processor Module) and does not process these signals in any way.

COL 0-6 input lines are connected to the seven columns of keys at the front panel keypad.

DC OPERATION output indicates when the DC power plug is being used to supply power to the unit. A logic 0 indicates AC operation while a logic 1 indicates DC operation and drives a front panel LED. This signal is a buffered version of the AC/(DC)* Drive Control signal from the power supply.

GEN PORT ENABLE output indicates which port is enabled when generating RF (GEN OUT or RF I/O). A logic 1 indicates the Generator Port is enabled and drives a front panel LED.

OPT A and *OPT B* indicate the phase "A" and phase "B" of the optical tuning knob at the front panel.

POWER ON signal is the Power On control signal returned from the front panel switch passing through to the power supply. Not used by processor assembly.

POWER ON LED output to the front panel drives the Power On LED.

ROW 0-6 input lines are connected to the seven rows of keys at the front panel.

SQUELCH LED output to the front panel drives the Squelch LED.

SQUELCH LEVEL input from the front panel potentiometer indicates the squelch level of the system. The Processor Module does not use this signal and only routes it between J3 (Front Panel) and J2 (Interface Module).

VOL CNTL AUDIO line is the input to the external volume potentiometer This signal is not used on the Processor Module but is routed to other modules.

VOL CNTL AUDIO RTN is the return line from the volume potentiometer.

14.2A.4 J4 RS-232 Interface

This is a full bi-directional RS-232 port with the capability to respond to a serial input. The port serves a dual purpose in that if an RS-232 is not desired, the port can be used as a printer output. Software determines if the port functions as an RS-232 bi-directional port or as an output only printer port.

*DCD** (Data Carrier Detect) input is not used at this time.

*DSR** (Data Set Ready) is a general purpose input that is used for modem control. This line is not used when a printer is connected.

*DTR** (Data Terminal Ready) is a general purpose output to indicate the Analyzer is ready to receive more data on the RXD line.

*RTS** and *CTS** (Request to Send, Clear to Send) are signals used in RS-232 communication.

RXD (Receive Data) input signal is the data received. If this interface is used as a printer output, the RXD signal is not used.

TXD (Transmit Data) output signal is the data being transmitted.

RI (Ring Indicator*)* input signal is not used at this time.

14.2A.5 J5 Frequency Standard Module

SYSTEM CLK input, 10 MHz reference signal.

14.2A.6 J6 Display Processor Module

BOPT0 - BOPT15 I/O, Buffered input/output data lines of the MC68000 processor.

BA1 - BA22 Outputs, Buffered address lines from the MC68000 processor.

*BLDS** Output, Buffered lower data strobe from the MC68000 processor.

*BUDS** Output, Buffered upper data strobe from the MC68000 processor.

*BRW** Output, Buffered read/write* signal from the MC68000 processor.

*IACK6** Output, Interrupt number 6 acknowledgement.

*DTACK** Input, Data transfer acknowledgement.

*BRESET** Output, Buffered reset.

*VPA** Input, Valid peripheral address.

VBACKUP Output, Battery backup voltage.

*IRQ6** Input, Interrupt request number 6.

BRTARM, Wiper arm of brightness potentiometer signal routed from front panel (J3 to J6). Not used by processor module.

BRTLO, Low side brightness potentiometer signal routed from front panel (J3 to J6). Not used by processor module.

BRTHI, High side brightness potentiometer signal routed from front panel (J3 to J6). Not used by processor module.

*SEML** Output, Semaphore flag bit to dual port ram. Not used at this time.

*OPTMEM** Output, Option memory select signal.

*OPTDET4** Input, Option detect number 4 signal.

DPFLASH UNLOCK Output, +12 volts for boot/sector unlock of display processor flash memory.

DP SYSCLK Output, 10Mhz buffered reference clock for the display processor module.

14.2A.7 J7 Power Supply

AC/DC DRIVE CNTL* input indicates if the power supply is using the DC input to power the unit. A logic 0 indicates DC operation and a logic 1 indicates AC operation.

AUX POWER is the auxiliary power control line which is routed to a front panel switch (via connector J3). Not used by processor module.

POWER ON is the power on signal from the power switch on the front panel (via connector J3). Not used by processor module.

DC INPUT+ input signal is the external DC voltage input at the Rear Panel routed to interface module. Not used by processor module.

14.2A.8 J8 Speaker

HANDSET AUDIO output is the audio line that drives the speaker.

14.2A.9 J9 Option Modules (digital interface)

BA1 – BA22 are the buffered outputs from the MC68000 processor address lines.

*BLDS** (Lower Data Strobe) when at a logic 0 indicates that valid data is on the lower eight data lines of the MC68000 processor.

BOPT0 – BOPT15 are the Option Module buffered inputs/outputs of the MC68000 data bus.

*BR/(WR)** is the buffered read/write signal which indicates the direction of data transfer to and from the MC68000 processor.

*BUDS** (Upper Data Strobe) when a logic 0 indicates that valid data is on the upper eight data lines of the MC68000 processor.

*DTACK** (Data Transfer ACKnowledge) input line indicates to the MC68000 processor that a data acknowledge is being issued from a peripheral device or memory device. External inputs are wire-ORed to this pin so all modules can use the same signal.

OPT DET 1,2,3,4 (Option Detect) input to the processor, which signifies the presence of an Option Module. A logic 0 on any one of the four inputs signifies an Option Module is present. Up to two Option Modules can be installed on the unit.

*OPT MEM** (Option Memory) active low output selects option memory space.

OPT TO CNTR (Option to counter) input not used by the processor. This signal is routed on the Processor Module from J9 (Option connector) to J1 (Interface connector).

*VPA** input, valid peripheral address.

VBACKUP output, battery backup voltage.

14.2A.10 J10 IEEE-488 Interface

ATN (Attention) input/output asserted by the controller in charge. Interface commands are sent over DIO data lines when ATN is logic 0. Data is sent over the DIO lines when ATN is logic 1.

DAV (Data Valid) input/output handshake signal to indicate valid data is present on the data bus.

DIO1 – DIO8 input/output data lines.

EOI (End Or Identify) input/output which indicates the end of a message block if ATN is logic 1. If ATN is a logic 0 the controller is requesting a parallel port.

1FC (Interface Clear) input/output signal is sent to set the interface in a known quiescent state.

NDAC (Not Data Accepted) input/output handshake line which is set to a logic 1 when the data lines are latched.

NRFD (Not ready For Data) input/output handshake line sent to indicate readiness for next byte of data.

REN (Remote Enable) input/output selects either remote or local control.

SRQ (Service Request) input/output set to logic 0 to indicate a need for service.

14.2A.11 J11 In-Line Wattmeter

ILWVFWD forward voltage input from the in-line wattmeter.

ILWVRFL reflected voltage input from the in-line wattmeter.

14.2B Connector Descriptions

14.2B.1 J1 (60 pin connector to the Interface Module)

pin	
1,2	+5 volts (Reserved)
3	VBACKUP (Reserved)
4-19	BBD0 – BBD15
20,21	GND
22	ATTEN CS*
23	RF MODE CS*
24	RF OUTPUT CS*
25	STATIC BUS CS*
26	SA CONTROL CS*
27	WRITE BUS CS*
28	SYNTH CS*
29,30	GND
31	AUDIO FILTER CS*
32	OUTPUT SPARE CS*
33	BFO CS* (Reserved)
34	VERT CS*
35	TRIG CS*
36	DVM SEL CS*
37	SCOPE CS*
38	DVM ATTEN CS*
39	SCOPE ATTEN CS*
40	RF STATUS CS*
41	RF READ CS*
42	A/D BUSY*
43-49	Not used
50	READ SPARE 1 CS* (Reserved)
51	READ SPARE 2 CS* (Reserved)
52-54	Not used
55	RF I/O2*
56	COUNTER
57	OPTION TO COUNTER (Reserved)
58-60	Not used

14.2B.2 J2 (60 pin edge connector to interface module and option modules)

pin	
1	DVM (Reserved)
2	GND
3	GEN AUDIO
4	GND
5	OPTION TO DVM
6	WB/(NB)*
7	DVM FROM RANGE
8	GND
9	EXT MOD + MIC IN
10	GND
11	HANDSET AUDIO
12	RAW MIC IN
13	RECEIVE SPEAKER AUDIO
14	GND
15	DEMOD CAL AUDIO (Reserved)
16	DC INPUT+
17	MIC IN (Reserved)
18	EXT MOD IN
19	SQUELCH LEVEL
20	INT MOD
21	RESET*
22	SQUELCHED DEMOD (Reserved)
23	GND
24	VOL CNTL AUDIO
25	GND
26	SYSCLK OUT
27	GND
28	CONV MOD
29	OPT MOD RTN1
30	OPT AUDIO RTN1
31	OPT MOD RTN3
32	OPT AUDIO RTN2
33	GND
34	IRQ1*
35	IRQ2*
36	SQUELCH
37	IRQ4*
38	IRQ5*
39	IRQ6*
40	IRQ7*
41	TIMER CLOCK
42	A/D DATA7
43	A/D DATA6
44	A/D DATA5
45	A/D DATA4
46	A/D DATA3
47	A/D DATA2
48	A/D DATA1
49	A/D DATA0
50	IACK7*
51	IACK6*
52	IACK5*
53	IACK4*
54	IACK2*
55	IACK1*
56	TRIGGER
57	GND
58	SAMPLE CLOCK
59	GND
60	OPTION FLASH UNLOCK

14.2B.3 J3 (40 pin connector to front panel assembly)

pin	
1,2	+5V
3,4	+12V
5-11	COL 0-6
12	Not used
13-19	ROW 0-6
20	Not used
21	OPT A
22	OPT B
23	DC OPERATION
24	GEN PORT ENABLE*
25	ANT PORT ENABLE*
26	AUXPOWER
27	SQUELCHED LED
28	POWER ON LED
29-31	Not used
32	POWER ON
33	BRT HI
34	BRT ARM
35	BRT LO
36	SQUELCH LEVEL
37	VOL CNTL AUDIO
38	VOL CNTL AUDIO RTN
39	GND
40	GND

14.2B.4 J4 (25 pin female "D" connector on Processor Module for RS-232 interface at the side panel)

pin	
1	GND
2	TXD
3	RXD
4	RTS
5	CTS
6	DSR
7	SIG GND
8	DCD*
9-19	Not used
20	DTR*
21	Not used
22	RI
23-25	Not used

14.2B.5 J5 (10 pin connector to frequency standard assembly)

pin	
1,2	+12V
3,4	not used
5,6	-12V
7,8	not used
9	SYS CLKIN
10	GND

14.2B.6 J6 (68 pin high density ribbon cable connector to interface with the Display Processor module)

pin	
1	GND
2-9	BOPT0 – BOPT7
10	GND
11-18	BOPT8 – BOPT15
19	GND
20	Not Used
21-27	BA1 – BA7
28	GND
29-35	BA8 – BA14
36	GND
37-44	BA15 – BA22
45	GND
46	BLDS*
47	BUDS*
48	GND
49	BRW*
50	IACK6*
51	DTACK*
52	BRESET*
53	VPA*
54	VBACKUP
55	IRQ6*
56	BRTARM
57	BRTLO
58	BRTHI
59	SEML*
60	OPTMEM*
61	OPTDET4*
62	DPFLASH_UNLOCK
63	Not Used
64	GND
65	DP_SYSCLK
66	GND
67	Not Used
68	Not Used

14.2B.7 J7 (12 pin connector to interface to the power supply module)

pin	
1	+5V
2	+12V
3	-5V
4	dc input
5,6	GND
7,8	GND
9	AC/DC* DRIVE CNTL
10	-12V
11	AUX POWER
12	POWER ON

14.2B.8 J8 (3 pin connector to the speaker)

pin	
1	HANDSET AUDIO
2	GND
3	Not used

14.2B.9 J9 (60 pin edge connector to option modules)

pin	
1	GND
2-9	BOPT0 - BOPT7
10	GND
11-18	BOPT8 - BOPT15
19,20	GND
21-27	BA1 – BA7
28	GND
29-35	BA8 – BA14
36	GND
37-44	BA15 – BA22
45	GND
46	BLDS*
47	BUDS*
48	GND
49	BR/WR
50	OPT DET1*
51	DTACK*
52	OPT DET2*
53	VPA*
54	OPT DET3*
55	VBACKUP
56	GND
57	OPTMEM*
58	GND
59	OPT TO CNTR
60	GND

14.2B.10 J10 (26 pin connector which provides future IEEE-488 interface)

pin	
1-3	GND
4	ATN
5	GND
6	SRQ
7	GND
8	IFC
9	GND
10	NDAC
11	GND
12	NRFD
13	GND
14	DAV
15	REN
16	EOI
17	DIO8
18	DIO4
19	DIO7
20	DIO3
21	DIO6
97	DIO2
23	DIO5
24	DIO1
25-26	Not used

14.2B.11 J11 (3 pin connector which provides future In-Line Wattmeter interface)

pin	
1	ILWVFWD
2	ILWVRFL
3	GND

14.2B.12 P1 (2 pin header)

pin	
1	+12 Volts
2	DPFLASH_UNLOCK

14.2B.13 P2 (2 pin header)

pin	
1	+12 Volts
2	OPTFLASH_UNLOCK

14.2B.14 P3 (2 pin header)

pin	
1	+12 Volts
2	MPFLASH_UNLOCK

14.3 BLOCK DIAGRAM DESCRIPTION

An MC68000 processor is used with a clock speed of 10MHz. The MC68000 executes instructions stored in non-volatile memory to perform its control of the system.

In addition to providing system management functions, the Processor Module interfaces with:

1. External RS-232 port which can optionally be used as a printer port.
2. Display Processor Module
3. Speaker
4. Front Panel
5. Power Supply
6. Option Module interface. Option Modules attach to the rear of the unit and connect to the Processor Module via ribbon cables.
7. IEEE-488 interface (GPIB)
8. In-Line Wattmeter

14.4 DETAILED DESCRIPTION

The Processor Module can be divided into three interrelated functional areas:

1. System microprocessor functions
2. ASIC functions
3. Audio signal generating and processing

14.4.1 System Microprocessor Functions

The module uses a single Motorola 68000 microprocessor operating at 10MHz. The MC68000 has a 23-bit address bus and a 16-bit data bus. The module is designed to use a single bus controller, therefore the bus request and acknowledge feature is disabled.

An Application Specific Integrated Circuit (ASIC) resides on the processor module. The ASIC was designed especially for this product and simplifies the Analyzer design. The ASIC is divided into eight interrelated blocks, each handling a specific system control function.

The processor address and data lines which are routed to other modules in the system are buffered with ACT244 and FCT245 devices respectively. The lower data byte used by all of the leveling DAC's is also buffered with ACT244 devices. All other onboard address and data lines are used directly from the microprocessor.

14.4.1.1 Read/Write Cycles

During a read cycle, the microprocessor asserts AS*, LDS* and UDS* simultaneously and for on-board cycles the ASIC responds by asserting DTACK*. When reading from other modules, DTACK* may be generated by the ASIC, the XILINX gate array or by an option module and typically is held off for two clock cycles (200ns) to allow time for slower peripherals to place data on the bus. Upon receipt of DTACK* the microprocessor reads the data and raises AS*, LDS* and UDS* which causes the read cycle to end.

During a write cycle, the microprocessor asserts AS* and R/(W)* and places data on the bus. One clock later LDS* and UDS* are asserted which causes DTACK* to be generated. Again DTACK* may be generated by the ASIC, the XILINX gate array or by an option module depending on the function being addressed.

14.4.1.2 Memory

The Processor Module contains several different types of memory. Flash memory, Static RAM, and EEPROM. The address decoding for memory selection is performed by the ASIC. Figure 14.4.1.2 illustrates memory mapping from the processors point of view.

FLASH memory
The Processor module has two flash memories with the option to expand the memory size by replacing those parts with drop-in replacements that are double in size. Initially, each flash memory is an 8megabit part organized as 1meg by 8. The two memories make up a total flash memory size of 2mega bytes. The flash memory is in-circuit re-programmable. The boot sector of the flash memories has been locked to prevent inadvertent erasure or re-programming. The boot sectors may be unlocked by applying +12 volts DC to the reset input on these devices in accordance with the manufacturer recommendations. The flash memories contain all system program code. The boot sector stores the initial stack pointer, reset vector and self test code. The self-test code checks for the presents of a display processor board by writing to its dual port RAM and waiting for DTACK. If this fails the processor module will send a continuous two-beep signal to the speaker.

The Processor module runs other tests on it's flash memory, SRAM, ASIC, checks for the F1 key pressed at power on (initiates flash memory programming), checks for the flash memory boot sector locked and gets software version and check sum information and computes a check sum for comparison.

Static RAM
is used to store stacks and queues for task management, operating system parameters, preset data, calibration data and scratch pad information.

EEPROM
stores non-volatile information such as system configuration, serial ID, unit type, high accuracy, calibration factors for absolute accuracy, and temperature calibration compensation. This information is stored in a 2048-bit serial EEPROM.

14.4.1.3 Supply Power Monitor

The Processor Module contains a supervisory chip to monitor the Vcc supply voltage and monitor microprocessor activity. If the Vcc drops below 4.5 volts, the supervisor chip switches to the battery backup mode to preserve the static RAM contents and then resets the microprocessor. Vcc must be stable again for 140ms for the microprocessor to restart. The supervisor chip contains a watchdog timer which monitors the microprocessor address strobe (AS*) for activity. After reset, if there is no activity for 1.1 seconds, the supervisor chip issues a rest to the microprocessor. Once the supervisor chip sees the first AS*, the watch dog timer switches timeout periods from 1.1 seconds to 281ms.

14.4.1.4 RS-232 INTERFACE

The full duplex RS-232 interface is implemented with a 16550 Universal Asynchronous Receiver Transmitter (UART). The UART accepts 8 bit data from the microprocessor and converts the data to a serial bit stream for transmission. The addition of start bits, stop bits and parity bits is handled internal to the UART. When the 8 bits have been transmitted the UART will interrupt the microprocessor indicating it is ready for the next data byte.

When receiving a serial bit stream, the UART will interrupt the microprocessor after it has received 8 bits of data. Timing is important, as the data must be removed from the UART before the next byte is received. The UART has its own baud rate generator with the baud rate being selectable by programming from the microprocessor. A MAX3241E fully integrated transceiver is used to generate the required RS-232 logic levels and provide ESD protection at the interface connector.

Description	Decode By	Address Range	FC2	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8-A1	A0 (UDS, LDS)	
SRAM Access to RAM blocked for first 8 AS_N	ASIC	000000-003FFF	X	0	0	0	0	0	0	0	0	0	0	X	X	X	X	X	X		
RAMSEL1_N (Even Addresses)																				0	
RAMSEL2_N (Odd Addresses)																					1
EXT MOD DAC SEL_N	ASIC	004000-0041FF	X	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	X		
DTMF DAC SEL_N	ASIC	004200-0043FF	X	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	X		
1KHZ DAC SEL_N	ASIC	004400-0045FF	X	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	X		
DPL TONE_N DPL TONE DAC SEL_N	ASIC	004600-0047FF	X	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	X		
DTMF GEN SEL_N	ASIC	004800-0049FF	X	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	X		
DTMF RCV SEL_N	ASIC	004A00-004BFF	X	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	X		
INT CNTL BLK	ASIC	004C00-004DFF	X	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	X		
EEPROM	ASIC	004E00-004FFF	X	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	X		
SCOPE CNTL BLK	ASIC	005000-0051FF	X	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	X		
NOT USED	ASIC	005200-0053FF	X	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	X		
FREQ PER CNTL BLK	ASIC	005400-0055FF	X	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	X		
TONE GEN BLK	ASIC	005600-0057FF	X	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	X		
LATCH CNTL BLK	ASIC	005800-0059FF	X	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	X		
KEY PD CNTL BLK	ASIC	005A00-005BFF	X	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	X		
VSC BLK	ASIC	005C00-005DFF	X	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	X		
TIMER CNTL BLK	ASIC	005E00-005FFF	X	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	X		
RF I/O 1_N	ASIC	006000-006FFF	X	0	0	0	0	0	0	0	0	0	1	1	0	X	X	X	X		
RF I/O 2_N	ASIC	007000-007FFF	X	0	0	0	0	0	0	0	0	0	1	1	1	X	X	X	X		
NOT USED	ASIC	008000-03FFFF	X	0	0	0	0	0	0	0	0	1	X	X	X	X	X	X	X		
UART CS_N	ASIC	040000-05FFFF	X	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X		
TIMER CS_N	ASIC	060000-07FFFF	X	0	0	0	0	0	1	1	X	X	X	X	X	X	X	X	X		
EXTRA CS_N IEEE488 High Tier Base Latch Audio Select	ASIC	080000-0FFFFF	X	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X		
SRAM Access to RAM blocked for first 8 AS_N	ASIC	100000-1FFFFF	X	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X		
RAMSEL1_N (Even Addresses)																				0	
RAMSEL2_N (Odd Addresses)																					1
VIDEO RAM (NOT USED)	ASIC	200000-2FFFFF	X	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X			
ACQUISITION RAM	ASIC	300000-3FFFFF	X	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X			
FLASH MEMORY	ASIC																				
EPROMSEL1_N Address valid for first 8 AS_N		400000-5FFFFF 000000-003FFF	X	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X			
EPROMSEL2_N		600000-7FFFFF	X	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X			
ANALOG CELLULAR OPTION MEMORY																					
EPROM	Peripheral	800000-83FFFF	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X			
RAM	Peripheral	840000-84FFFF	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X			
EXTERNAL WATTMETER																					
RANGE SELECT	Peripheral	860001	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X			
ZERO ADDRESS	Peripheral	863001	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X			
ANALOG CELLULAR OPTION MEMORY																					
IEEE488	Peripheral	864000-864FFF																			
090 TRUNKING SLICE DPRAM	Peripheral	AC0001-AC0FFF	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X			
090 DIAGNOSTIC SLICE DPRAM	Peripheral	BC0001-BC0FFF	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X			
IDEN SLICE DPRAM	Peripheral	CC0001-CC0FFF	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X			
P57140J DISPLAY PROCESSOR	Peripheral	DC0001-DC0FFF	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X			

X = Don't Care

Fig. 14.4.1.2 Memory Map

14.4.1.5 Programmable Timers

Three uPD71054 timer devices are utilized. One devices is incorporated within the ASIC and the other two are located on the processor module. Each of the timers contain three 16-bit programmable counters. Figure 14.4.1.5 illustrates the addressing and use of the nine timers. Six of them are available for general purpose use.

Each timer operates independently and may be configured in a variety of modes. Two of the general purpose timers use a 10MHz or 100KHz clock and four use a 1KHz clock. With 16-bits the timers can provide a maximum delay of 6.54 ms at 10MHz and 65.54 seconds at 1KHz.

Each of the general purpose timers can be used to generate interrupts after a programmed delay. To enable each counter, the counter must be set to mode 0 operation (see uPD71054 user's manual). The processor can then set the delay time by writing one or two byte count values. The counter decrements from this value and will interrupt when a zero count is reached. A delay of 100ns/10us/1ms is inserted for each count decrement.

Once the processor is interrupted the counter's status can be read from the uPD71054 status register (see uPD71054 user's manual) or read from an internal ASIC location. If the OUT pin for any counter is at a logic high, it must be reset to a low by setting the counter to mode 0 again or by writing a new count value. If the interrupt was generated by a counter internal to the ASIC, the interrupt must be cleared and re-enabled internal to the ASIC in addition to reprogramming counter 0.

Operating modes are as follows:

Software Triggered Strobe
The counter will decrement from the programmed count value to zero, and then the output will go low for one clock cycle. The rising edge will interrupt the microprocessor. This is the most common operating mode.

Interrupt on End of Count
The counter will decrement from the count value to zero, and then the output will change state. The output can be reset low by writing a new count value.

Square Wave Generator
The counter will divide the 10MHz input clock down to a new frequency. Even count values create a 50% duty cycle. Odd count values create a non-symmetrical duty cycle. Programmable output frequencies range from 152.6Hz (FFFF hex count value) to 5MHz (0002 hex count value). The output frequency is the inverse of count value times 100ns.

14.4.1.6 IEEE-488 Interface

The IEEE-488 interface is implemented using a TMS9914A General Purpose Interface Bus (GPIB) controller and SN75160A and SN75161A transceivers.

The TMS9914A contains thirteen registers, which are accessible by the microprocessor. Six of these registers can be read and seven can be written to by the microprocessor. The register information is shown in Figure 14.4.1.6. For further explanation of bit assignment see the TM9914A data manual.

Timer		*Address*	*Counter/Reg*	*Purpose*
1	100KHz or 10MHz clock	5E01	Counter 0	General Purpose
	100KHz or 10MHz clock	5E03	Counter 1	General Purpose
	10MHz clock	5E05	Counter 2	Scope Clock Control
		5E07	Control Register	Counter Mode Programming
2	1KHz clock	60001	Counter 0	General Purpose
	10MHz clock	60003	Counter 1	Spectrum Analyzer
	10MHz clock	60005	Counter 2	not used (spare)
		60007	Control Register	Counter Mode Programming
3	1KHz clock	60009	Counter 0	General Purpose
	1KHz clock	6000B	Counter 1	General Purpose
	1KHz clock	6000D	Counter 2	General Purpose
		6000F	Control Register	Counter Mode Programming

Fig. 14.4.1.5 Programmable Timers

14.4.2 ASIC Functions

The ASIC (Application Specific Integrated Circuit) chip contains eight interrelated blocks each handling a specific system control function.

ASIC BLOCKS:

1. Decode
2. Interrupt Control
3. Scope Control
4. Frequency/Period Counter
5. Tone Generation
6. Video System
7. Keypad Control
8. Latch Control

14.4.2.1 Decode Control

The Decode block handles all address decoding. It receives A1-A23, R/W, AS, UDS, LDS, FC 0-2, and asserts an appropriate chip select based on the defined memory map. Chips selects are low asserted pulses used to clock in data (on rising edge) to internal and external latches.

The ASIC also generates the DTACK signal to the microprocessor either with or without wait states to accommodate slower peripherals.

Other features of the Decode Block include forcing accesses to flash memory during system startup to read the interrupt vector table, and special handshaking requirements for the serial EEPROM chip.

14.4.2.2 Interrupt Control Block

The Interrupt Control Block prioritizes and channels all interrupt requests into the microprocessor IPL 0-2 interrupt inputs. Interrupts are classified as levels 1 through 7, with level 7 being serviced first.

Level 3 are vectored interrupts; meaning that upon asserting the IPL0-2 lines the microprocessor will execute an interrupt acknowledgement cycle and read the vector number from an Interrupt Control Block status register. The vector number is the address of the routine, which services the interrupt. Level 3 interrupts may be individually disabled by writing to the interrupt mask register.

All other interrupt levels are autovectored; meaning that the service routine address is calculated directly from the level number. The Analyzer has eight vectored service routines and six autovectored interrupt service routines as follows:

1ddress											
RS2	RS1	RS0	Register Name	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	Int Status 0	INTO	INT1	B1	B0	END	SPAS	RLC	MAC
0	0	1	Int Status 1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC
0	1	0	Address Status	REM	LLO	ATN	LPAS	TPAS	LADS	TAD S	ulpa
0	1	1	Bus Status	ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN
1	0	0	Not Used								
1	0	1	Not used								
1	1	0	Cmd Pass Thru	D108	D107	D106	D105	D104	D103	D102	D101
1	1	1	Data In	D108	D107	D106	D105	D104	D103	D102	D101
READ REGISTERS											

Address											
RS2	RS1	RS0	Register Name	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	Int Mask 0			B1	B0	END	SPAS	RLC	MAC
0	0	1	Int Mask 1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC
0	1	0	Not Used								
0	1	1	Aux Cmd	cs			f4	f3	f2	f1	f0
1	0	0	Address	edpa	dal	dat	A5	A4	A3	A2	A1
1	0	1	Serial Poll	S8	rsvl	S6	S5	S4	S3	S2	S1
1	1	0	Parallel Poll	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1
1	1	1	Data Out	D108	D107	D106	D105	D104	D103	D102	D101
WRITE REGISTERS											

Fig. 14.4.1.6 IEEE-488 Register Definition

LEVEL	SERVICE ROUTINE
1	Reserved for Options
2	Reserved for Options
3 (vectored)	Key Release IRQ
	Optical Tuning Knob IRQ
	Key Press IRQ
	DTMF Receiver IRQ
	UART Transmit IRQ
	UART Receive IRQ
	General Purpose Timer IRQ
	Freq/Period Counter IRQ
4	Scope IRQ
5	Reserved for Options
6	Reserved for Options
7	Reserved for Options

Priority level 3 is further reduced using a priority encoder external to the processor chip. This only allows priority if more than one device is requesting an interrupt at the same time. If one device is already being serviced, this priority scheme will not allow a device on priority level 3 to interrupt another device on priority level 3. The priority level format for priority level 3 from highest to lowest priority is:

1 Period/Frequency Counter
2 General Purpose Timer
3 Receive Character (for RS232)
4 Transmit Character (for RS232)
5 DTMF Receiver
6 Front Panel Key Press
7 Optical Tuning Knob
8 Front Panel Key Release

14.4.2.3 Scope Control Block

The Scope Control Block communicates with the Interface Module to perform the waveform sampling process for the digital oscilloscope. The sample rate, number of samples acquired, and the sample storage mode are set by the Scope Control Block.

The Interface Module performs analog-to-digital conversion of the waveform and routes the data to the 512 x 8 scope RAM located within the ASIC chip. At the completion of sample acquisition, the microprocessor is interrupted (level 4) to transfer the data from scope RAM to the processor for processing and then passed to the display processor module for display on the LCD Panel.

The scope has two sampling storage modes: normal and min/max. Normal mode stores the acquired sample every sample clock period. Min/max mode observes the samples over multiple sample cycles, and stores the minimum and maximum values. Min/max is the typical mode of operation due to its built in averaging process without expending microprocessor resources. Normal mode is used for slow time bases where multiple sweeps do not overtax the microprocessor.

14.4.2.4 Frequency/Period Counter Block

The frequency counter is directly accessible to the main processor and generates an interrupt on overflow and end of count. Specifications are as follows:

Input Freq Range:	5Hz to 5.0MHz
Resolution:	0.1Hz at 5Hz-6.5KHz
	1Hz at 5Hz-65KHz
	10Hz at 50Hz-650KHz
	100Hz at 500Hz-5.0MHz
Gate Time:	10, 1, 0.1, 0.01, and 0.001 seconds
Update Rate:	As fast as processor can read interrupts
Accuracy:	Equal to timebase ±1 count
Interrupt:	Maskable, vectored priority level 3

The period counter is also directly accessible to the main processor and generates an interrupt on end of count. The period counter's specifications are as follows:

Input Freq Range:	0.5Hz to 20KHz
Resolution:	0.1Hz at 5-500Hz
	1Hz at 500Hz-2KHz
	10Hz at 2-5KHz
	100Hz at 5-20KHz
Clock Time:	10MHz
Update Rate:	Every input frequency cycle counted
Accuracy:	Equal to timebase ±1 count
Interrupt:	Maskable, vectored priority level 3

The Frequency/Period Counter Block uses three 16 bit counters to measure the frequency and period of an input waveform. Each counter has a clock and a gate input. The clock input will decrement the count value but only with the gate enabled. The freq/period counter exploits this feature to achieve accurate timing measurements.

In frequency count mode, one counter is loaded with the full count (FFFF hex). The gate is enabled for a known period of time which is selectable from 1 microsecond to 10 seconds. Upon completion of the gate time, the microprocessor is interrupted to read the counter value. The input frequency can be calculated from full count minus current count divided by the gate period (no. of cycles divided by seconds = Hz). For gate times longer than the counter range (counter overflow), the microprocessor is interrupted and FFFF hex cycles are saved for the "total number of cycles" calculation. Counting continues until the gate time is completed.

Period count mode uses all three counters. Counter #1 and #2 clock inputs operate with a fixed 10MHz clock. The input signal to be measured is routed to the counter gates such that Counter #1 will count the low portion and Counter #2 will count the high portion of the input waveform. The number of 10MHz clocks recorded during the sum of the two gate times is the period of the input signal. Counter #0 is used as an overflow for the other two counters to provide a full 32 bit range. This allows the period counter to measure an 859 second input signal period.

14.4.2.5 Tone Generation Block

The Tone Generation Block creates the baseband tones for Alarm and DPL, and generates the DAC DATA digits for the TONE signal.

The DAC DATA output creates a digitally stepped sinewave by cycling through data from a local 1K x 8 ROM. One sinusoidal cycle is stored in the ROM as 1024 discrete 8 bit data points. The accumulator operates at a fixed 419.4304 KHz sample rate. An increment value is loaded into the tone register, which will determine the output frequency. The 21 bit accumulator is incremented by the register value each sample cycle. The most significant 10 bits of the accumulator output is the ROM address. Thus, the greater the increment value, the farther apart the consecutive ROM addresses and the fewer number of individual data points read from the 1024 available in the ROM. However, since the sample rate is still 419.4304KHz, the ROM will be cycled at a faster rate resulting in a higher output frequency with fewer steps (less resolution) per output cycle. The output frequency resolution is 0.1Hz.

The DPL signal is derived from a 23-bit data word loaded from the microprocessor and processed through a parallel to serial shift register.

The Alarm signal is a square wave alternating between 500Hz and 1KHz at a 2:3 ratio. It is triggered by an over-temperature condition.

The Tone Generation Block also receives the DTMF STROBE and generates the DTMF IRQ for the microprocessor to read the DTMF decoded data.

14.4.2.6 Video System Control Block

Not used in the D module.

14.4.2.7 Keypad Control Block

The Keypad Control Block interfaces to the front panel keypad and optical tuning knob. Its primary task is to sense keypad closures, and optical tuning knob motion and interrupt the microprocessor accordingly.

The microprocessor will read the row and column ports to determine which key was pressed. Releasing the key will interrupt the microprocessor again to inform the software that the key has been released. The debounce time for key closure is 50ms.

Continuous key closure will interrupt the microprocessor every 60ms. The Keypad Control Block also receives two inputs from the optical tuning knob, one for each direction of rotation.

14.4.2.8 Latch Control Block

The Latch Control Block contains two 8 bit latches for chip enable signals. The microprocessor sets these low asserted latches to continuously enable external chips, i.e. analog switches.

14.4.3 XILINX Programmable Gate Array

The XILINX PGA contains circuitry required to communicate with the Interface Module and Option Modules. The PGA provides the following functions.

Generates level 2 interrupt requests for timer 3, IEEE-488 interface and option module interface.

Decodes chip selects for Interface Module latches.

Generates a Data Acknowledge (DTACK) signal for processor read and write cycles to the Interface Module.

Provides a clock divider for 2.5MHz and 1MHz clocks.

14.4.4 Audio Signal Generation and Processing

Audio signal Generation and processing functions include digitally controlled attenuators, analog switches, active filters, oscillators and summing amplifiers.

14.4.4.1 Digitially Controlled Attenuators

The digitally controlled attenuators are used in numerous locations to adjust the amplitude of the analog signal. The typical circuit configuration consists of an ACT374 octal latch, a DAC08 digital to analog converter and an operational amplifier. The octal latch receives 8-bits of data corresponding to decimal 0 to 255 and outputs this data to the DAC08.

The DAC08 also receives an analog input current and attenuates the current by A/255 where A is the decimal equivalent of the 8-bit data value. If the analog current is bipolar, a DC offset must be added since the DAC08 input cannot source current. Most of the attenuator circuits have the DC offset supplied by a local 8Vdc regulated voltage source Vreg).

The output of the DAC08 is an attenuated current which is converted to a voltage by the op amp. The following equation describes the overall function:

Vout=(Iin + Ioffset)*(A/256)*Z1oad

where

Iin=input current (2-4ma)..... Vin/Rin
Ioffset=DC offset current..... Vreg/Rreg
A=attenuation..... 0 to 255
Zload=op amp feedback resistor

14.4.4.2 DTMF Generation

The DTMF generator receives a digital pattern from the microprocessor and outputs a tone which is the sum of the high and low group sinewaves superimposed on a DC offset.

A 3.579545MHz Pierce oscillator provides the clock source for the DTMF generator. The tone duration is 40ms minimum with 40ms between tones. The tone is digitally attenuated followed by an AC coupled high pass filter. The resultant symmetric, +/-8V max waveform, is routed to a summing amplifier.

14.4.4.3 1KHZ Signal Generation

The 1KHz symmetrical square wave is received from the ASIC chip and routed through a bandpass filter to form a 1KHz sinusoidal signal. The sinewave timebase is derived from the system clock internal to the ASIC. The total harmonic distortion of the filter is less than 10%. The sinewave is digitally attenuated followed by an AC coupled highpass filter. The resultant symmetric, +/-8V max sinewave is routed to a summing amplifier.

14.4.4.4 INT MOD Signal Generation

The Processor Module uses an analog switch to select between DPL and TONE signals. The DPL signal is a 23-bit digital pattern. The TONE signal is a digitally generated sinewave.

The processor uses separate lowpass filters to remove high frequency components from each waveform. The selected signal is digitally attenuated followed by an AC coupled highpass filter. The resultant symmetric, +/-8V max waveform is routed to a summing amplifier. The summation of DTMF, 1KHz, and DPL/TONE is the INT MOD signal. INT MOD is routed to a module output pin and to another summing amplifier.

14.4.4.5 CONV MOD Signal Generation

The next level of summing has four inputs: INT MOD, OPT AUDIO RTN 1-2 and another signal which is the attenuated result of RAW MIC IN, EXT MOD IN, or EXT MOD + MIC IN. Each of the four signals pass through an analog switch prior to the summing amplifier. The output is CONV MOD which is routed to a module output pin, to another summing amplifier and to the phase-mod filter.

14.4.4.6 EMPH MOD Signal Generation

CONV MOD passes through a phase modulation filter and the output (EMPH MOD) is routed to a summing amplifier.

14.4.4.7 GEN AUDIO Signal Generation

GEN AUDIO is the sum of CONV MOD, EMPH MOD, OPT MOD RTN 1 and OPT MOD RTN 2. Each of the four signals pass through an analog switch prior to the summing amplifier. The output signal (GEN AUDIO) is passed straight through to a module output pin or can be inverted.

14.4.4.8 VOL CNTL Audio

The speaker audio signal is from a summing amplifier with switched inputs from CONV MOD, RCV SPKR AUDIO, OPT TO DVM and DVM FROM RANGE. The resulting signal VOL CNTL AUDIO is routed to the front panel where it is adjusted by the volume control knob. The returning signal, VOL CNTL AUDIO RTN, passes through a low pass filter before being combined with the ALARM signal at the LM386 power amplifier. The power amplifier drives the speaker.

14.5 BLOCK DIAGRAM

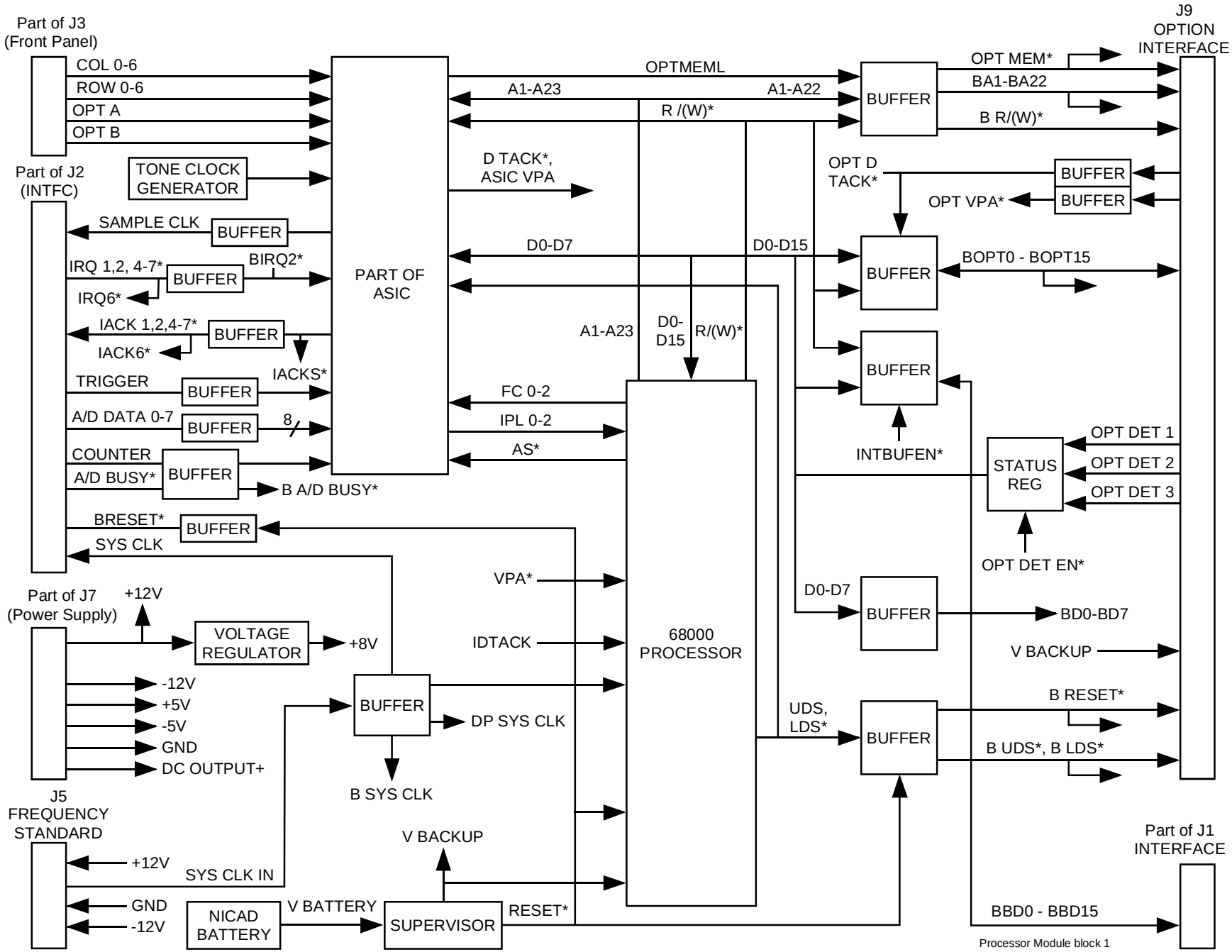


Fig. 14.5 Processor Module Block Diagram (1 of 6)

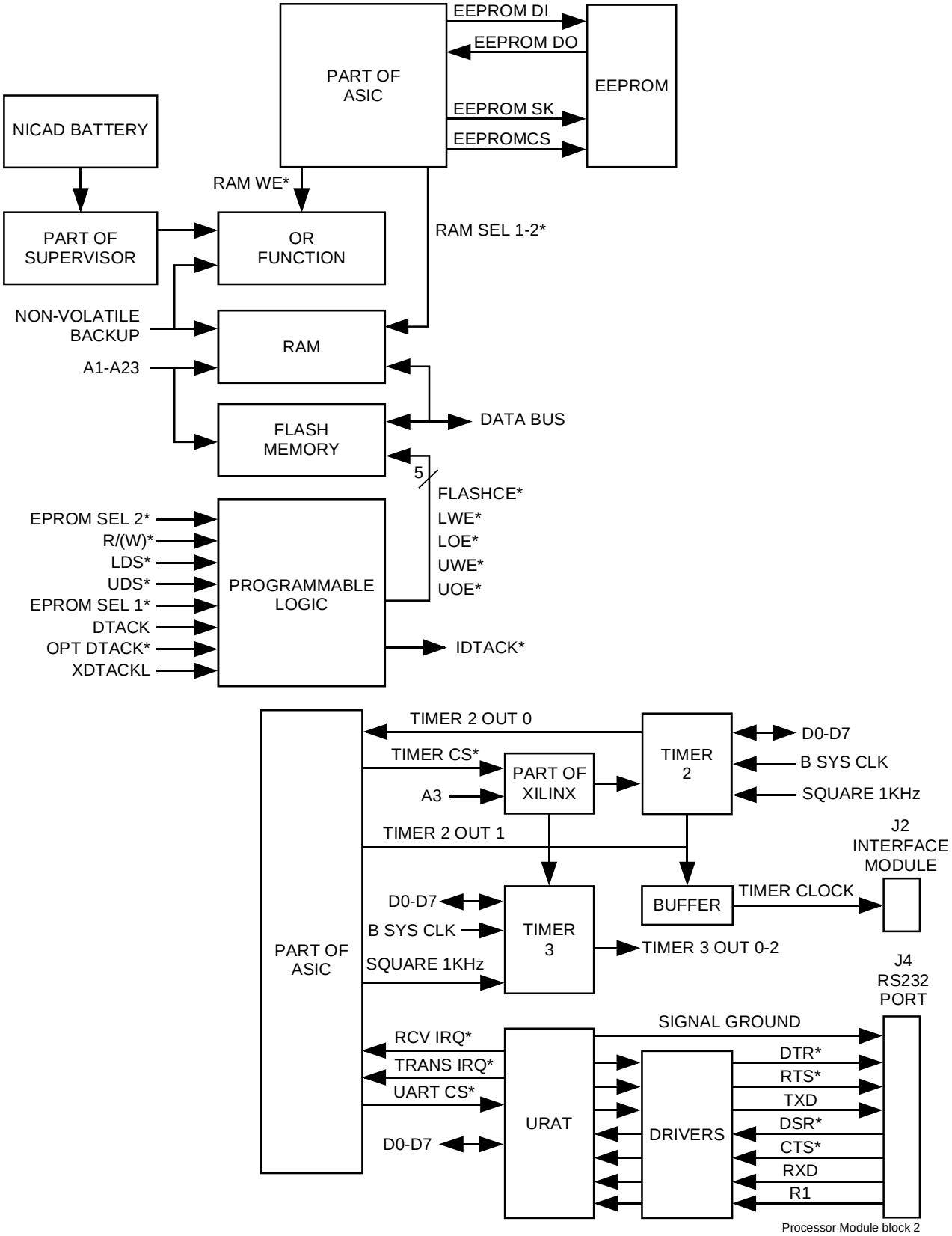
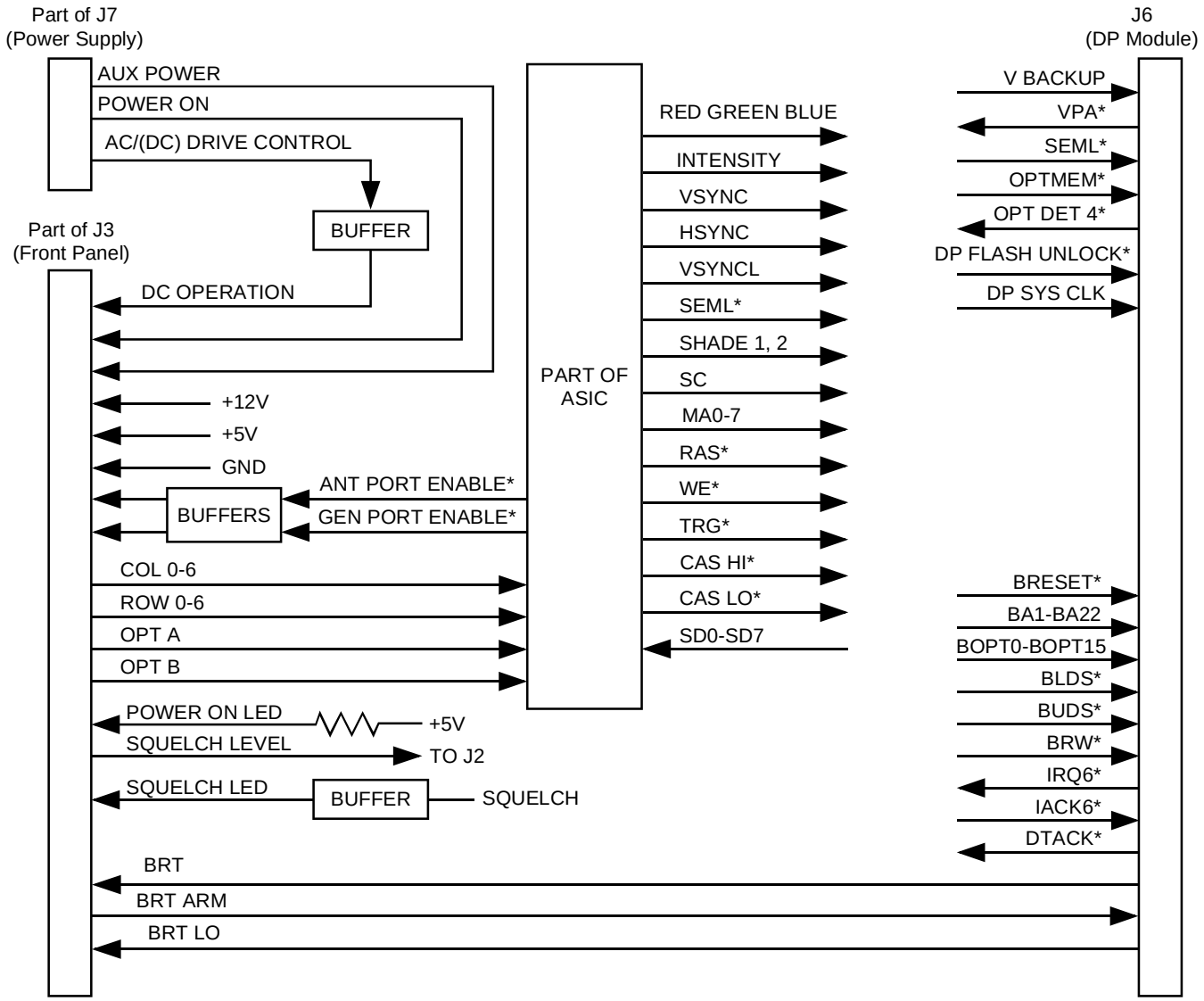


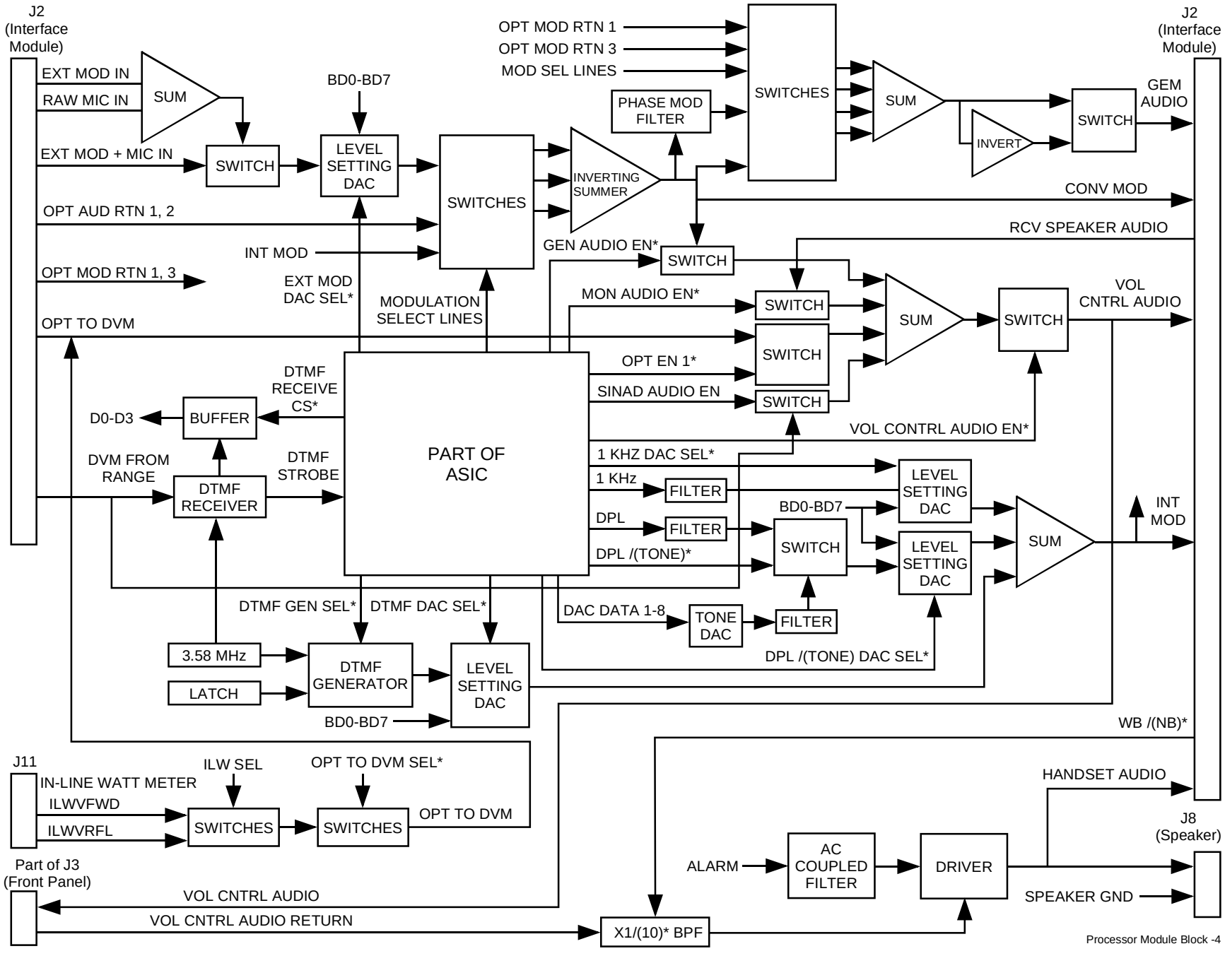
Fig. 14.5 Processor Module Block Diagram (2 of 6)



Processor Module block 3

Fig. 14.5 Processor Module Block Diagram (3 of 6)

Fig. 14.5 Processor Module Block Diagram (4 of 6)



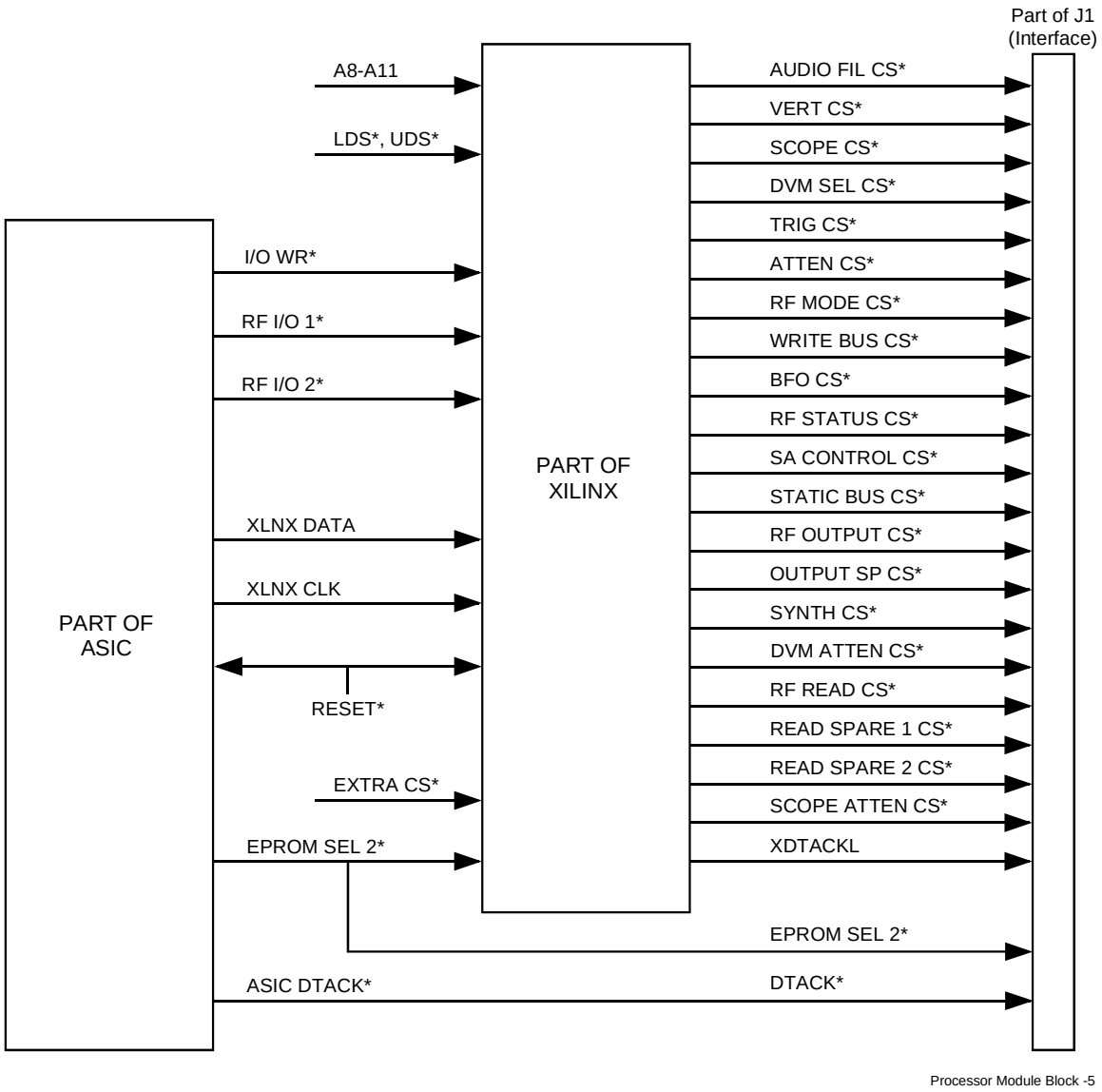


Fig. 14.5 Processor Module Block Diagram (5 of 6)

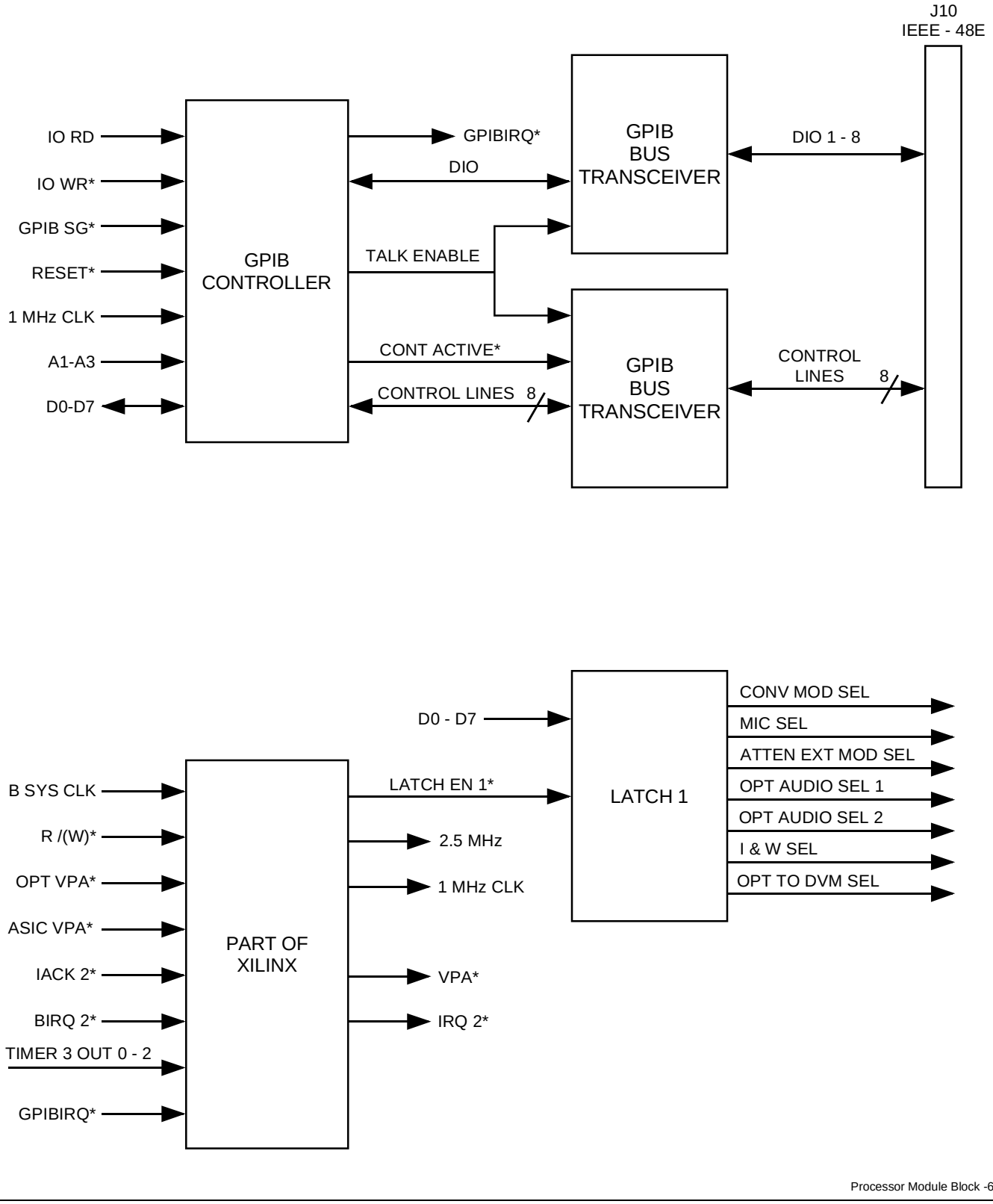
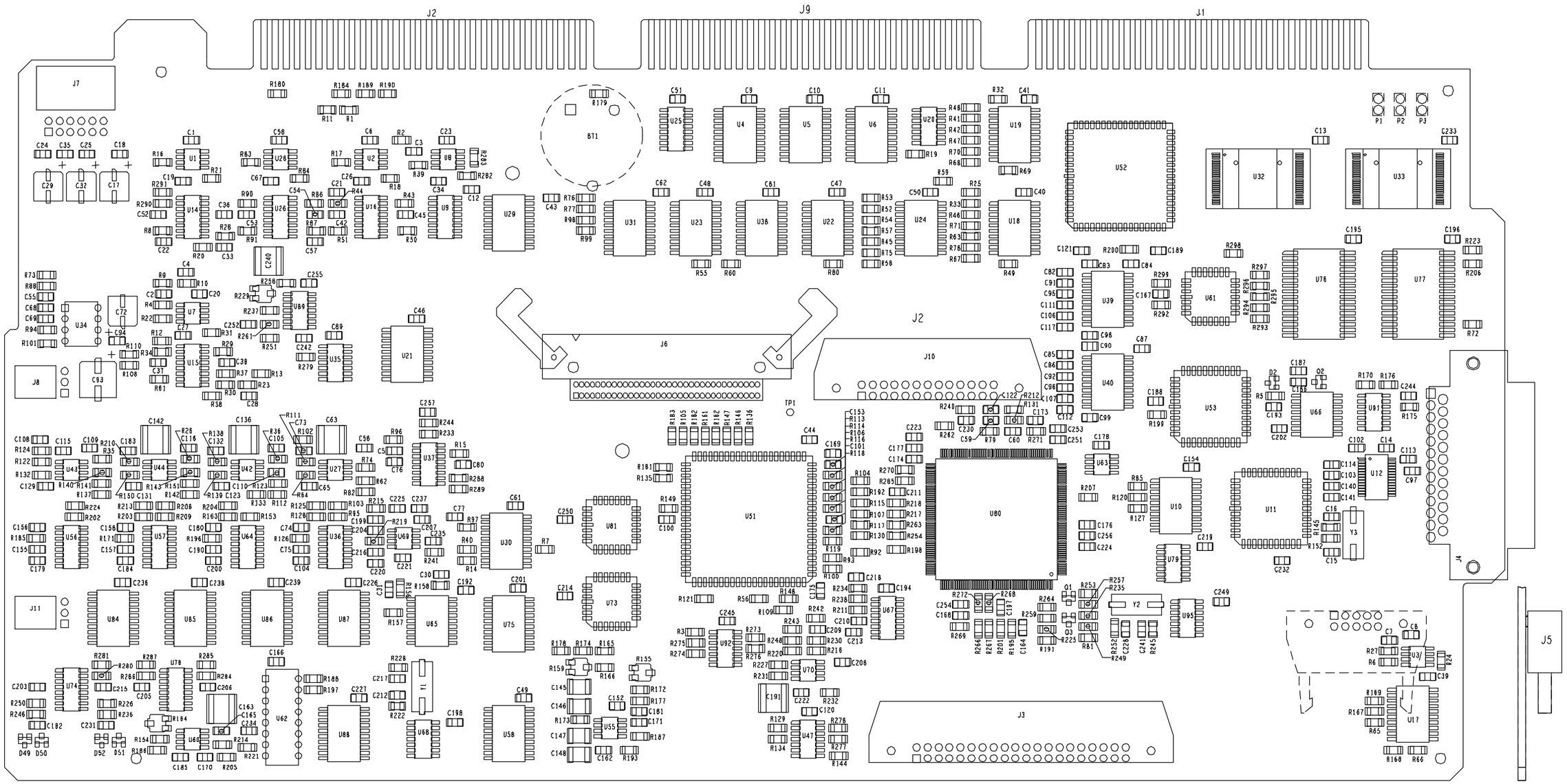


Fig. 14.5 Processor Module Block Diagram (6 of 6)



CIRCUIT CARD ASSEMBLY
MICROPROCESSOR

01-P57100J REV. -

SHEET 1 OF 1

DWG NO 63-P57102J SH 1

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

REVISION HISTORY

REV	DESCRIPTION		DATE	APPROVED
A	CO L48683-2	JFP 05-01-00	05-05-00	T. GATTO
B	CO L48693-2	PLS 06-12-00	06-12-00	T. GATTO

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A4.
2. FOR REFERENCE DRAWINGS REFER TO:
   01-P57100J ASSEMBLY
   12-P57103J TEST PROCEDURE
3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS.
   ALL CAPACITORS ARE IN UF.
   ALL INDUCTORS ARE IN UH.
   ALL VOLTAGES ARE DC.
4. TERMINATIONS CODED WITH THE SAME LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
5. DEVICE TYPE NUMBERS AND CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE 1.
6. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH MANUFACTURER. SEE ASSEMBLY PARTS LIST FOR PROPER PART NUMBER.

7. DO NOT INSTALL AT INITIAL ASSEMBLY.

TABLE 1

REF DES	DEVICE TYPE	+5V	-5V	+12V	-12V	SRAM_V	GND	NO CONNECT	LOCATION
U1	MC34072			8	4				4B3, B5
U2	MC34072			8	4				17B3, C7
U3	LT1016	1	4				6		3B8
U4	ACT244	20					10		3C3, D3
U5	ACT244	20					10		3C4, D4
U6	ACT244	20					10		3C5, D5
U7	MC34072			8	4				8A2, B3
U8	MC34072			8	4				10A6, 17B2
U9	836C191	16					8		14C5
U10	ACT244	20					10		3B3
U11	PC16550D	44					22		6C4
U12	MAX3241	26					25		6B6
U13									
U14	DG211	12		13	4		5		4B2, 7A4, 10A3
U15	DG211	12		13	4		5		4B7, 4C7
U16	DG211	12		13	4		5		17A5, B5
U17	ACT244	20					10		3C7, D7
U18	ACT245	20					10		15D6
U19	ACT245	20					10		15C6
U20									15D5
U21	ACT244	20					10		14B7
U22	ACT244	20					10		3A7, 12D3
U23	74FCT245	20					10		15B6
U24	ACT244	20					10		14C7
U25	836C191	16					8		15B5
U26	DG211	12		13	4		5		4C7, D7
U27	MC34072			8	4				17D2, D4
U28	MC34072			8	4				4D5, 7B5
U29	ACT244	20					10		14D7
U30	ACT244	20					10		12B3, D3
U31	74FCT245	20					10		15B6
U32	AM29F800B	37					27, 46		20C5
U33	AM29F800B	37					27, 46		20C3
U34	LM386			6			4		7B3
U35	ACT04	14					7		4B3, 6C2, 8A5, 10A7, 17C7
U36	DAC08			1	7				17D5
U37	DG211	12		13	4		5		4D7, 10A3, 17C5
U38	ACT374	20					10		17B7
U39	75161B	20					10		19B4
U40	75160B	20					10		19D4
U41									
U42	MC34072			8	4				8C2, C4
U43	MC34072			8	4				9D3, D4
U44	MC34072			8	4				9B3, B4
U45									
U46									
U47	ACT04	14					7		10A7, 13C2, D2, 14C3
U48									
U49									
U50									
U51	XC3042	22, 64						1, 43	16C5
U52	MC68HC000	14, 52					16, 17, 56, 57	18, 31	3C5
U53	TMS9914A	44					22	1, 18, 28, 40	19C6
U54									
U55	MC34072			8	4				7C2, C4
U56	DAC08			1	7				9D5
U57	DAC08			1	7				9C5
U58	ACT244	20					10		3B2
U59									
U60	MC34072			8	4				4A5, 10D3
U61	22V10	28					14	1, 8, 15, 22	20B7

TABLE 1

REF DES	DEVICE TYPE	+5V	-5V	+12V	-12V	SRAM_V	GND	NO CONNECT	LOCATION
U62	TP5089	1					6		10D6
U63	NMC9356	8					5	6, 7	12B3
U64	DAC08			1	7				8D6
U65	CM8870C	18					9		5D6
U66	MAX693	3					4		11D7
U67	DAC08			1	7				5D3
U68	AC02	14					7		5A6, C5, C7
U69	MC34072			8	4				5B2, B3
U70	MC34072			8	4				4A7, 5C2
U71									
U72									
U73	UPD71054	28					14	1, 11, 15, 25	6D4
U74	DG211	12		13	4		5		8A4, A5, 10A5
U75	ACT244	20					10		5C5, D5
U76	HM628128					32	16		11D3
U77	HM628128					32	16		11B3
U78	DG211	12		13	4		5		4B5, 10A4
U79									20C2
U80	6000121	14, 15, 16, 58, 59, 60, 110, 111, 112, 170, 172, 172					24, 25, 26, 70, 71, 72, 124, 125, 126, 186, 187, 188	4, 22, 45, 46, 53, 56, 67, 69, 120	10C2, 12D5, 13D4, 14A5
U81	UPD71054	28					14	1, 11, 15, 25	6B4
U82									
U83									
U84	ACT374	20					10		9D7
U85	ACT374	20					10		9C7
U86	ACT374	20					10		8D7
U87	ACT374	20					10		17D6
U88	ACT374	20					10		10D7
U89	MC1723							1, 8, 14	14D5
U90									
U91	AC32					14	7		11A2, B2, B5, C5
U92	ACT04	14					7		10A8, 19C7, 20B7
U93									
U94									
U95	AC02	14					7		13A2, 13B3

REFERENCE DESIGNATIONS

HIGHEST USED	NOT USED
BT1	
C257	C64, C66, C70, C71, C78, C79, C88, C118, C119, C124-C128, C130, C133-C135, C137-C139, C143, C144, C148-C151, C159-C161, C172, C229, C243, C246-C248
D52	D1, D3-D48
J11	
P3	
Q3	
R299	R6, R89, R160, R194, R239, R247, R255, R258, R260
TP1	
U95	U13, U41, U45, U46, U48-U50, U54, U59, U71, U72, U82, U83, U90, U93, U94
Y3	

ALL SHEETS ARE THE SAME REVISION STATUS

		CONTR NA
		ISS RN B35550-453(-)3-1-00
		APPROVALS
		DWN D. CARPENTER 00-02-11
		CHKR X
		QA T. DAVINO 03-01-00
		MATL W. MCDONALD 03-01-00
01-P57100J	COCHISE	MFG J. HARNISH 02-29-00
NEXT ASSY	USED ON	ENG A. GATTO 02-29-00
APPLICATION		CUST NA

MOTOROLA INC.
GOVERNMENT AND SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

TITLE
SCHEMATIC DIAGRAM
MICROPROCESSOR

SIZE	CAGE CODE	DWG NO
D	94990	63-P57102J

SCALE NONE | SHEET 1 OF 20

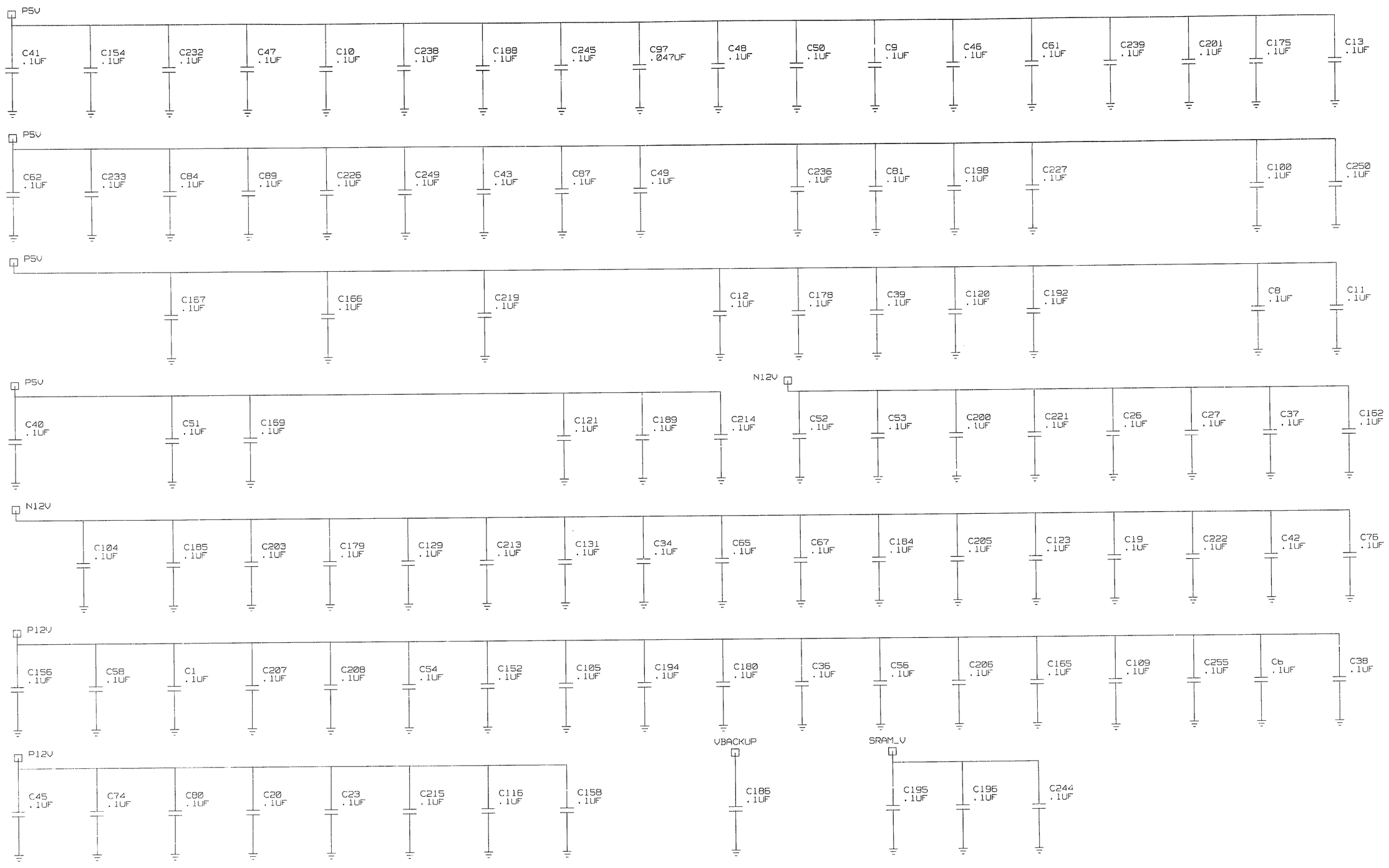
DRAWING 63P57102J_A 63P57102J

CONCEPT

ASME Y14.1-1995 DRAWING FORMAT - 3/95

DSIZEPAGE1P JEC

1-22-2010

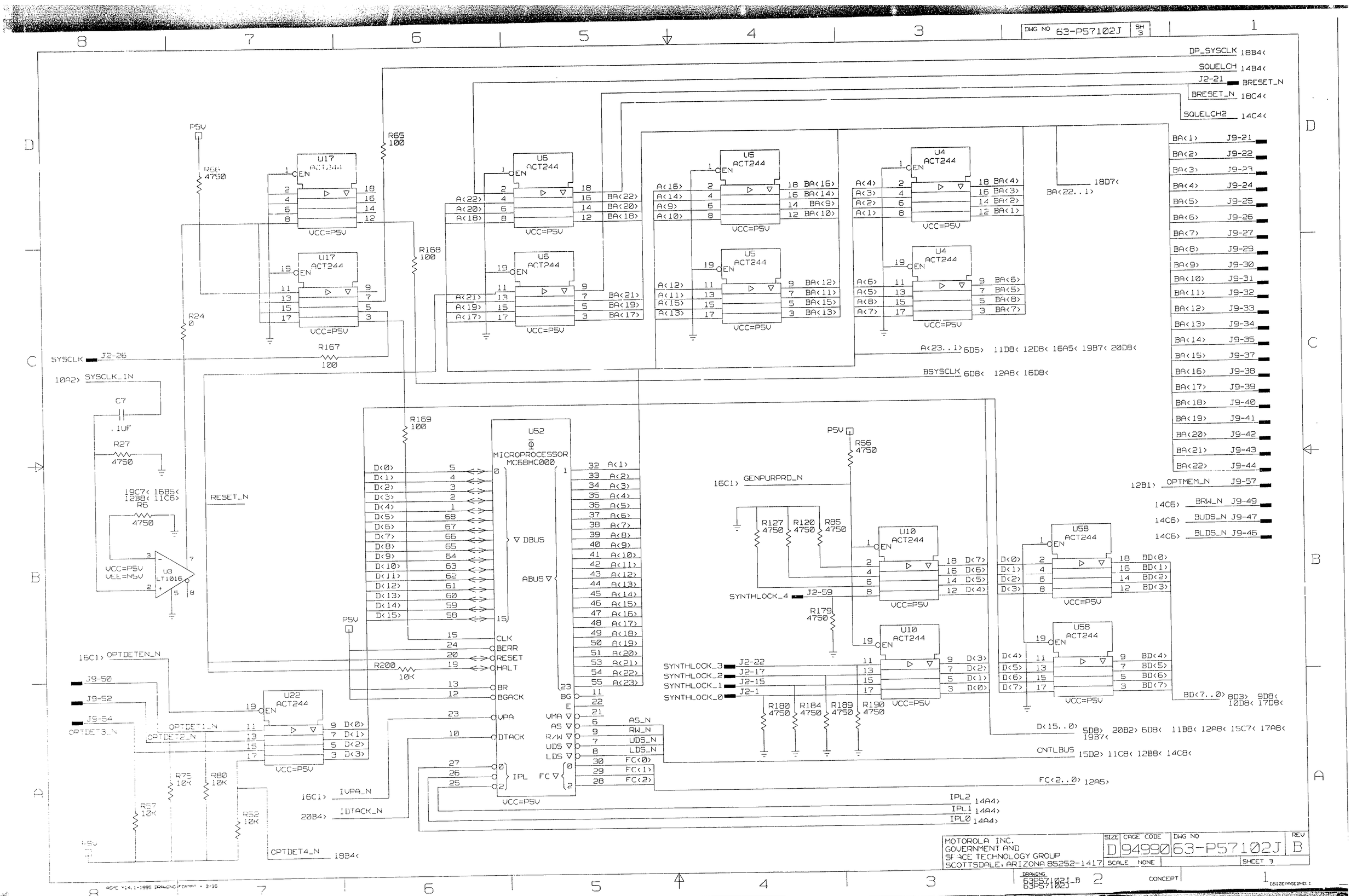


MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57102J	REV B
	SCALE NONE			SHEET 2

ASME Y14.1-1995 DRAWING FORMAT - 3/95

DRAWING 63P57102J-B 63P57102J 2 CONCEPT

DSIZEPAGE2MD2C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SQUELCH 14B4<
J2-21 BRESET_N
BRESET_N 18C4<
SQUELCH2 14C4<
BA<1> J9-21
BA<2> J9-22
BA<3> J9-23
BA<4> J9-24
BA<5> J9-25
BA<6> J9-26
BA<7> J9-27
BA<8> J9-29
BA<9> J9-30
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BA<15> J9-37
BA<16> J9-38
BA<17> J9-39
BA<18> J9-40
BA<19> J9-41
BA<20> J9-42
BA<21> J9-43
BA<22> J9-44
12B1> OPTMEM_N J9-57
14C6> BRW_N J9-49
14C6> BUDS_N J9-47
14C6> BLDS_N J9-46
18D7<
BA<22..1>
A<23..1> 6D5> 11D8< 12D8< 16A5< 19B7< 20D8<
BSYSCLK 6D8< 12A8< 16D8<
P5V
R66 4750
R65 100
R168 100
R24 0
R167 100
SYSCLK J2-26
10A2> SYSCLK_IN
C7 .1UF
R27 4750
19C7< 16B5< 12B8< 11C6>
R6 4750
U3 LT1016
VCC=P5V
VEE=N5V
RESET_N
U17 ACT244
U6 ACT244
U5 ACT244
U4 ACT244
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BA<22> BA<20> BA<18> BA<21> BA<19> BA<17>
A<16> A<14> A<9> A<10> A<12> A<11> A<15> A<13>
BA<16> BA<14> BA<9> BA<10> BA<12> BA<11> BA<15> BA<13>
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BA<4> BA<3> BA<2> BA<1> BA<6> BA<5> BA<8> BA<7>
R169 100
U52 MICROPROCESSOR MC68HC000
D<0> D<1> D<2> D<3> D<4> D<5> D<6> D<7> D<8> D<9> D<10> D<11> D<12> D<13> D<14> D<15>
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ABUS
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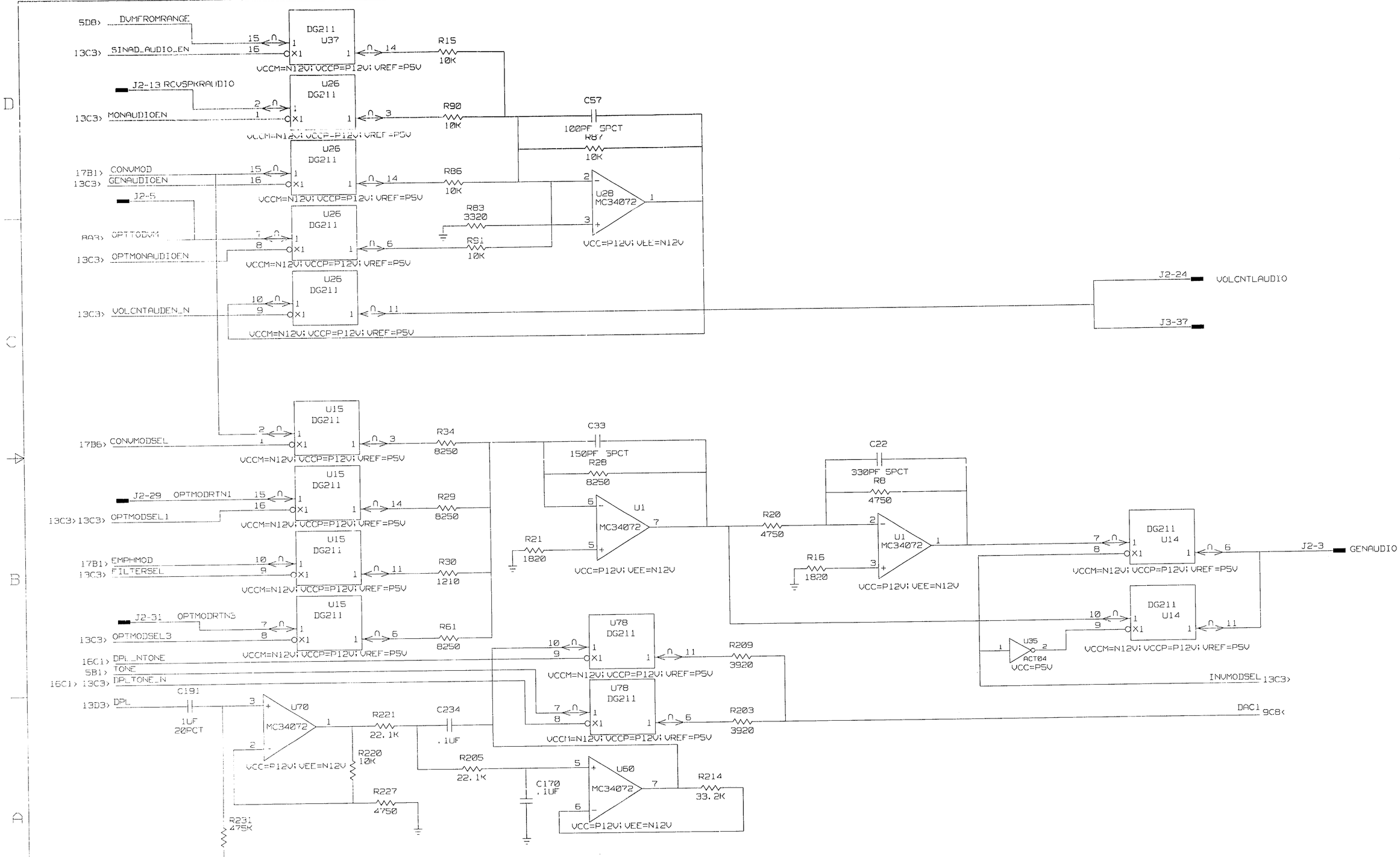
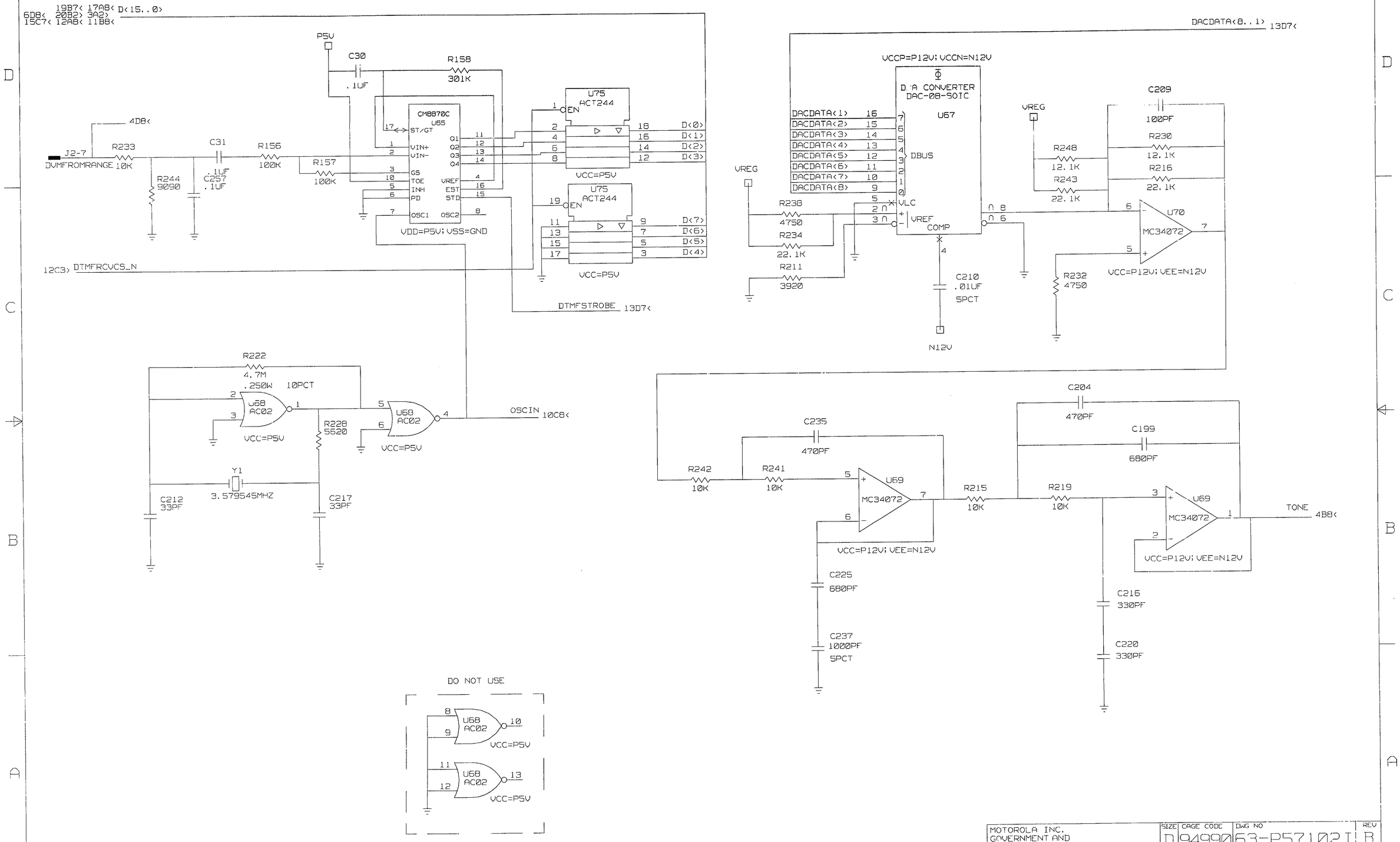
CLK
BERR
RESET
HALT
BR
BGACK
VPA
DTACK
BG
E
VMA
AS
R/W
UDS
LDS
FC
IPL
AS_N
RW_N
UDS_N
LDS_N
FC<0>
FC<1>
FC<2>
R200 10K
16C1> OPTDETEN_N
J9-50
J9-52
J9-54
OPTDET3_N
OPTDET1_N
OPTDET2_N
U22 ACT244
D<0> D<1> D<2> D<3>
R75 10K
R80 10K
R57 10K
R52 10K
16C1> IVPA_N
20B4> IDTACK_N
OPTDET4_N 18B4<
16C1> GENPURPRD_N
R56 4750
R127 4750
R120 4750
R85 4750
U10 ACT244
SYNTHLOCK_4 J2-59
R179 4750
SYNTHLOCK_3 J2-22
SYNTHLOCK_2 J2-17
SYNTHLOCK_1 J2-15
SYNTHLOCK_0 J2-1
R180 4750
R184 4750
R189 4750
R190 4750
D<7> D<6> D<5> D<4> D<3> D<2> D<1> D<0>
U58 ACT244
BD<0> BD<1> BD<2> BD<3> BD<4> BD<5> BD<6> BD<7>
BD<7..0> 8D3> 9D8< 10D8< 17D8<
D<15..0> 5D8> 20B2> 6D8< 11B8< 12A8< 15C7< 17A8< 19B7<
CNTLBUS 15D2> 11C8< 12B8< 14C8<
FC<2..0> 12A5>
IPL2 14A4>
IPL1 14A4>
IPL0 14A4>
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D
CAGE CODE 94990
DWG NO 63-P57102J
REV B
SCALE NONE
SHEET 3
DRAWING 63P57102J-B 63P57102J
CONCEPT
ASME Y14.1-1995 DRAWING FORMAT - 3/95



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57102J	REV B
	SCALE NONE			SHEET 4

DRAWING 63P57102J-B 63P57102J CONCEPT



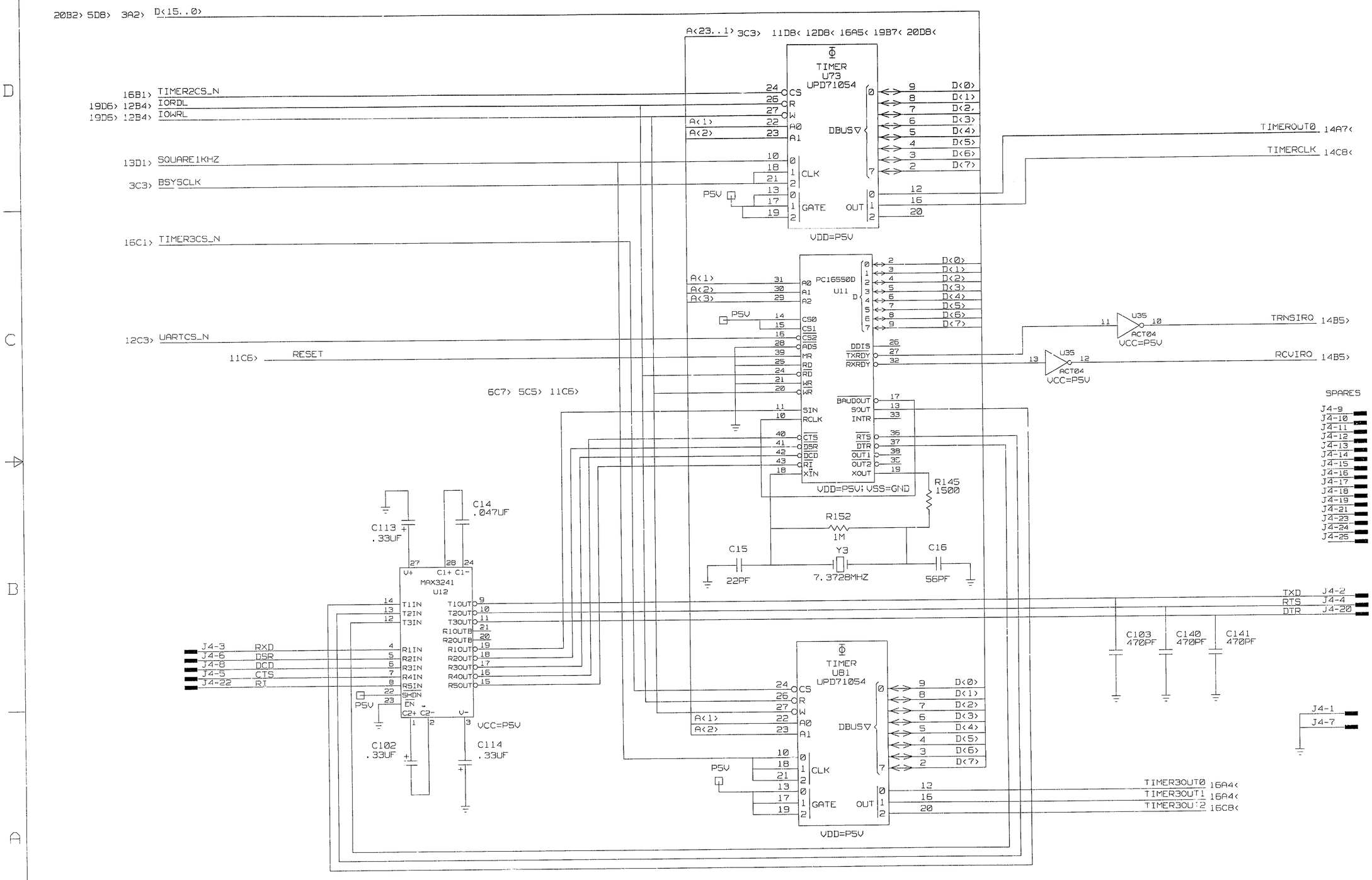
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57102J	REV B
	SCALE NONE		SHEET 5	

DRAWING 63P57102J-B 63P57102J

CONCEPT

ASME Y14.1-1995 DRAWING FORMAT - 3/95

D1SIZEPAGE2MD2C



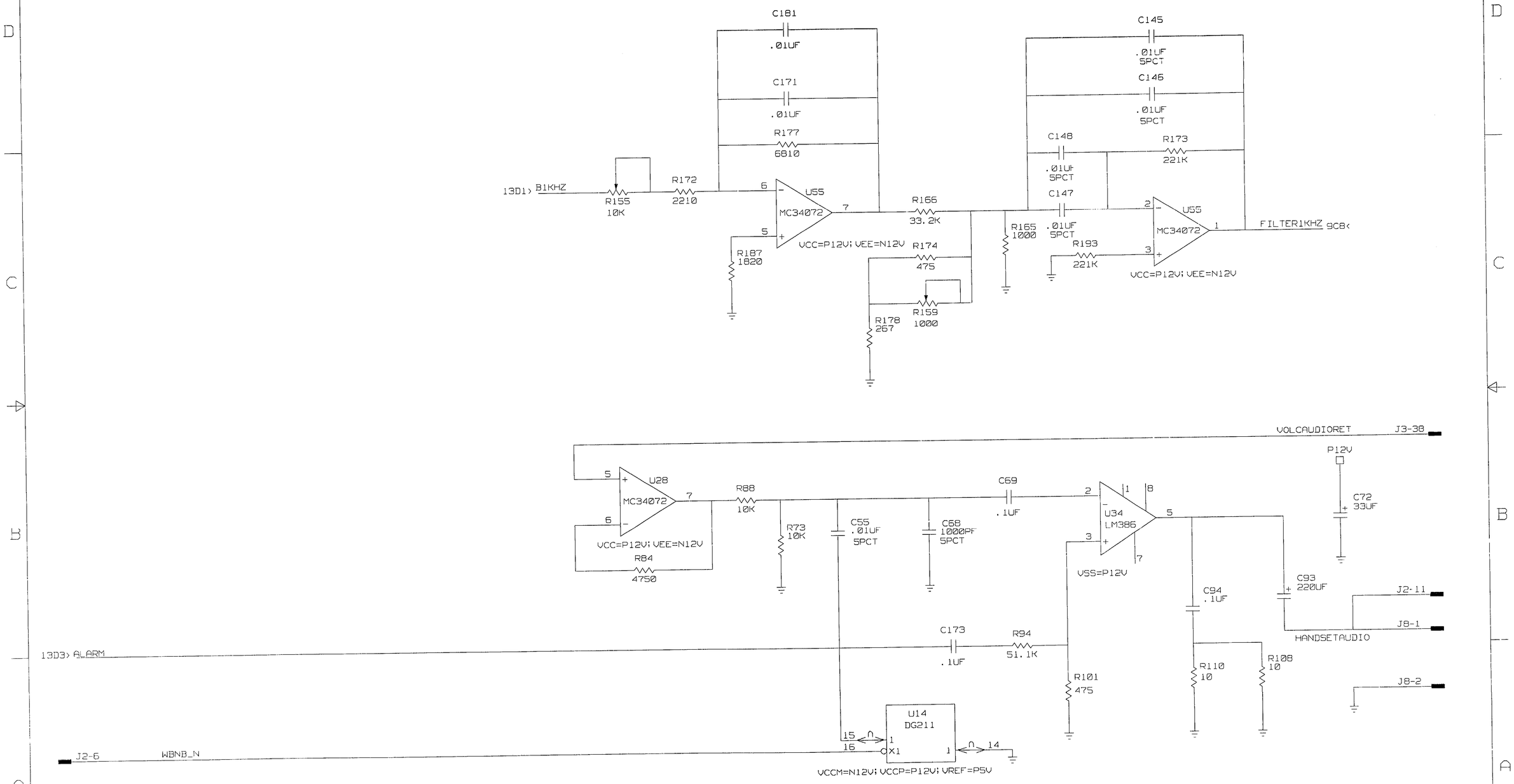
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57102J	REV B
	SCALE NONE		SHEET 6	

ASME Y14.1-1995 DRAWING FORMAT - 3/95

DRAWING 63P57102J-B 63P57102J

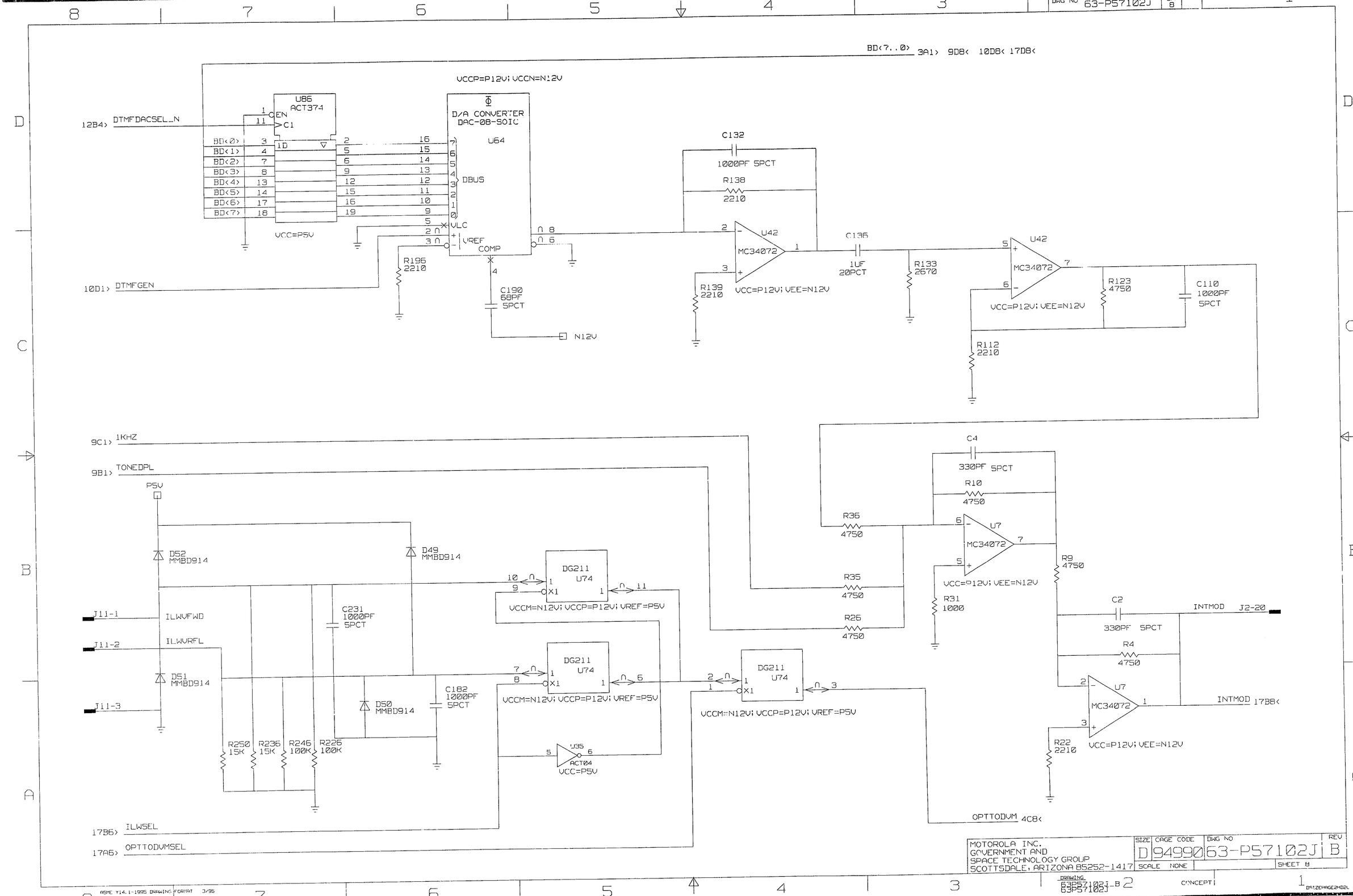
CONCEPT

DSIZEPAGE2MD2C



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57102J	REV B
	SCALE NONE			SHEET 7

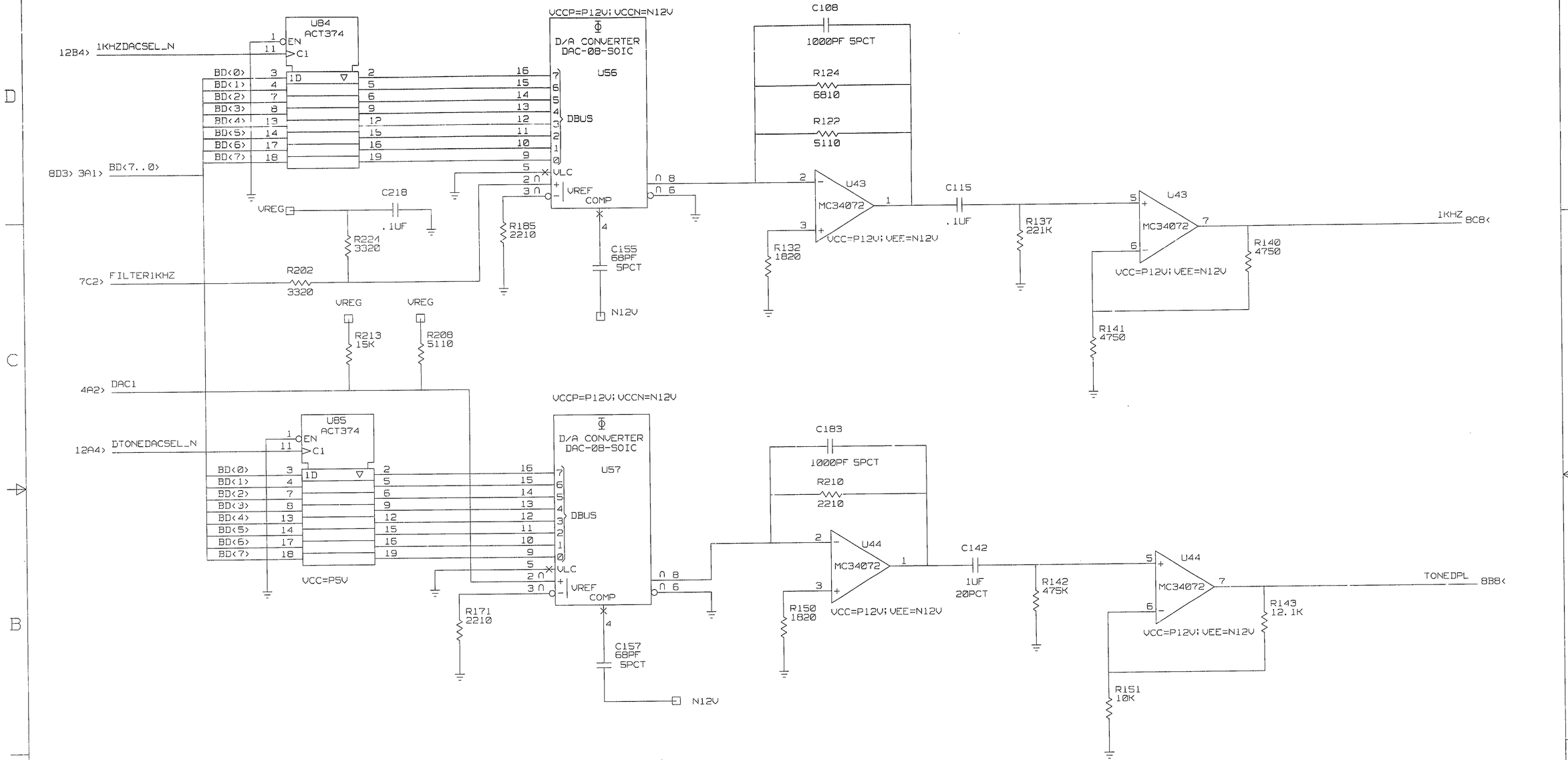
DRAWING 63P57102J-B 63P57102J 2 CONCEPT 1 DSIZEPAGE2HD2C



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57102J REV B
	SCALE NONE		SHEET 8

DRAWING 63P57102J-B 63P57102J 2 CONCEPT 1 DATZEPAGE2HD2L

ASME Y14.1-1995 DRAWING FORMAT D/95



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57102J	REV B
	SCALE NONE		SHEET 9	

ASME Y14.1-1995 DRAWING FORMAT - 3/95

DRAWING 63P57102J-B 2 CONCEPT

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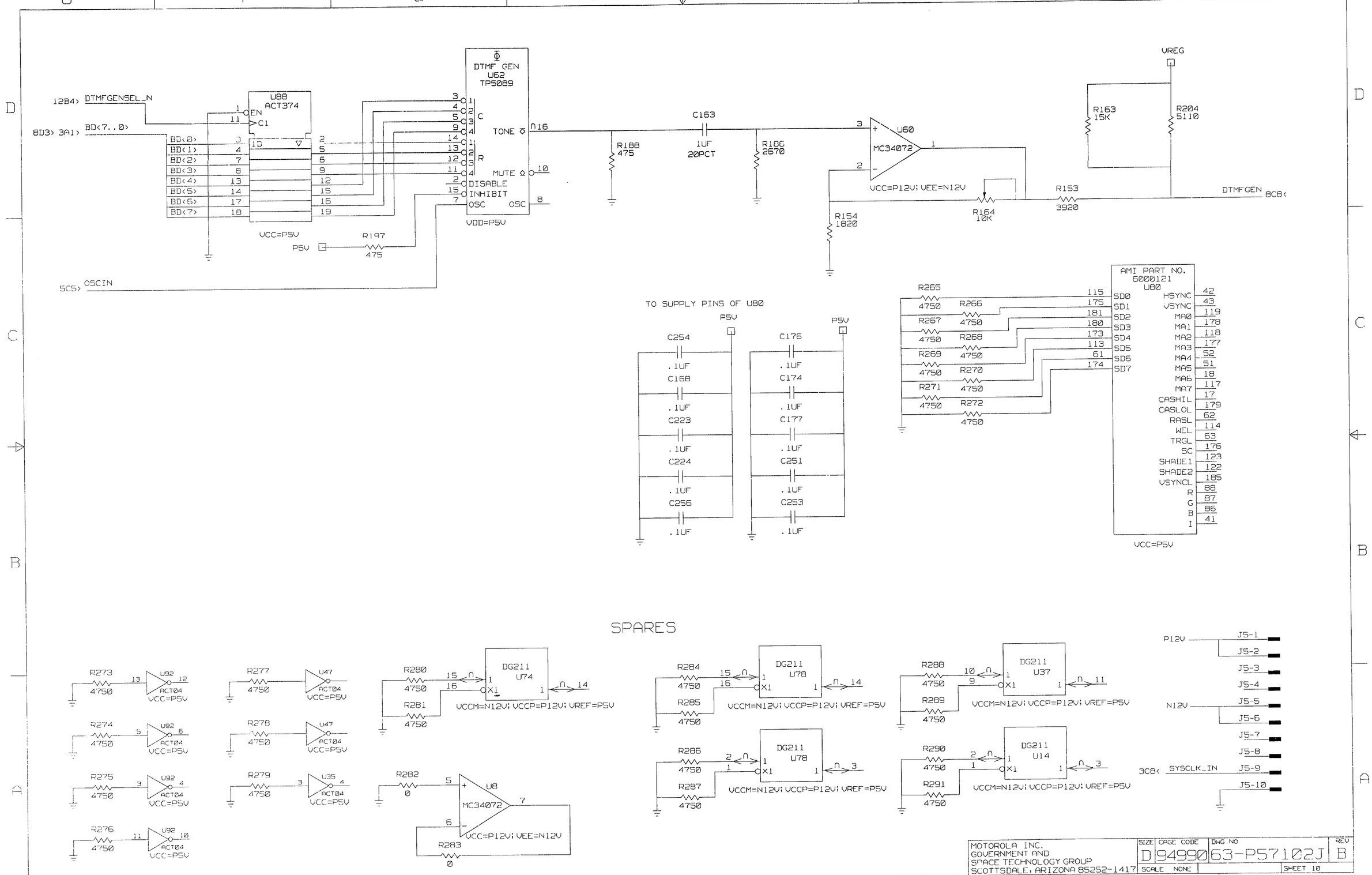

MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57102J	REV B
	SCALE NONE		SHEET 10

DRAWING 63P57102J-B 63P57102J

CONCEPT

ASME Y14.1-1995 DRAWING FORMAT - 3/95

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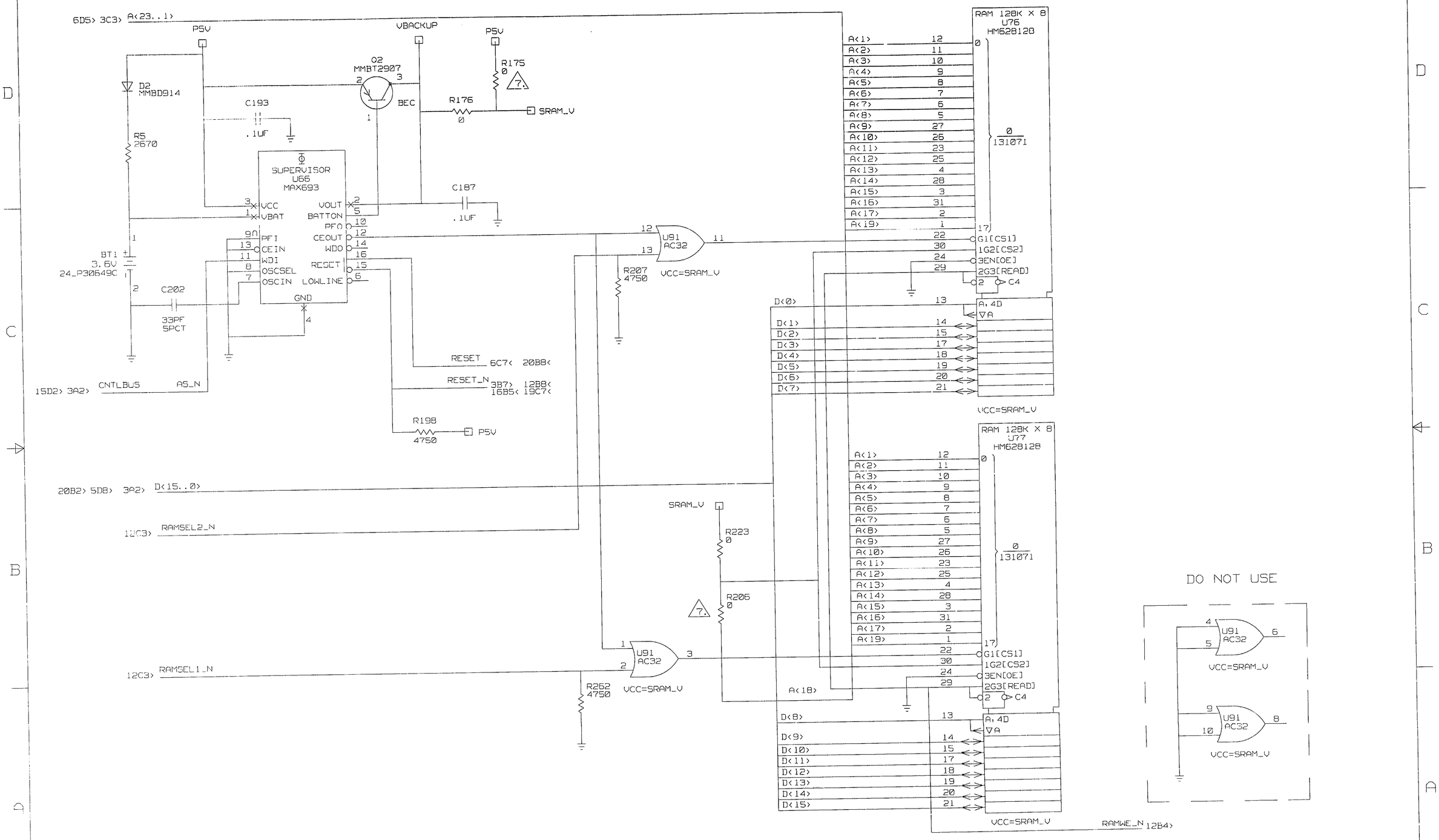
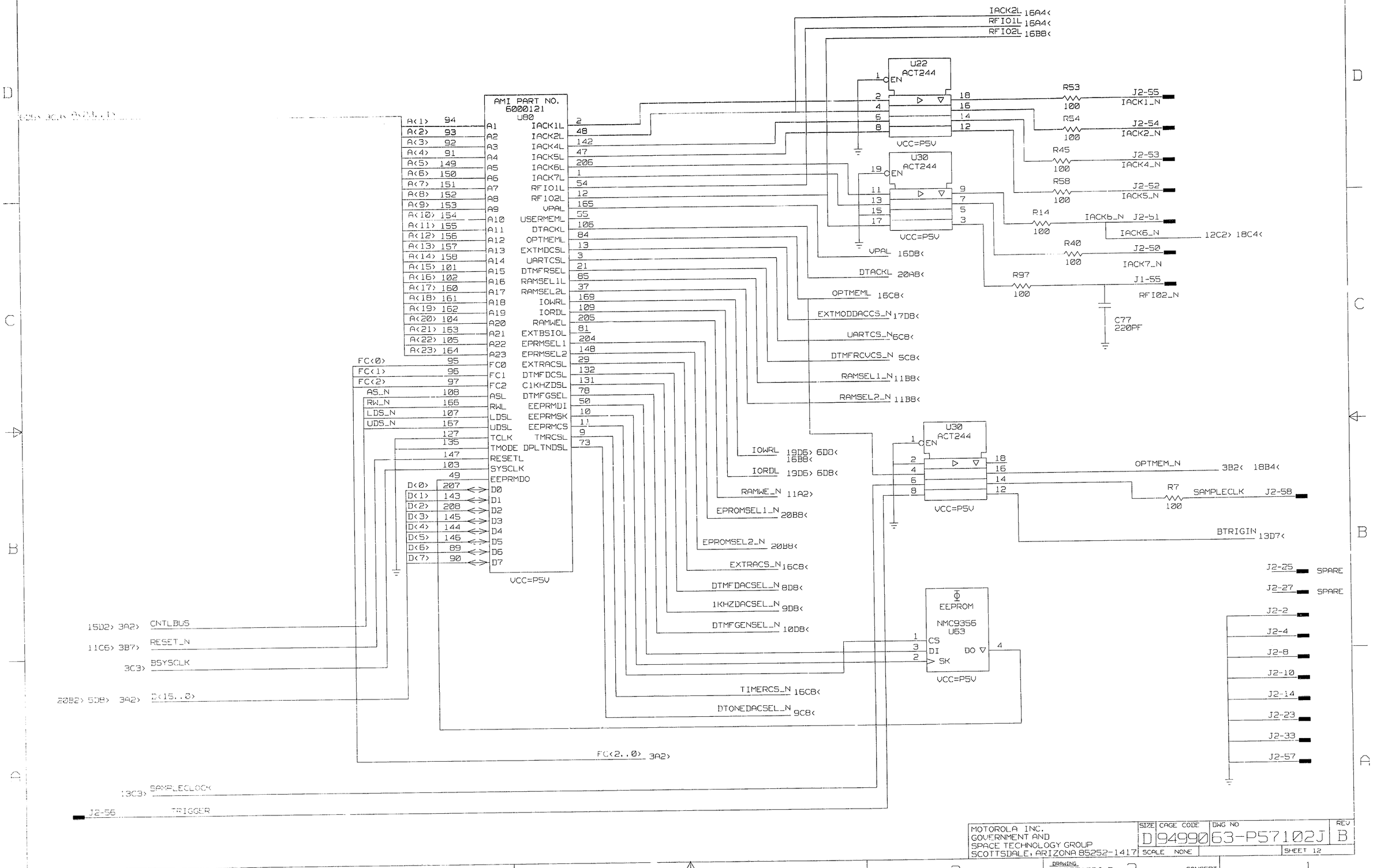


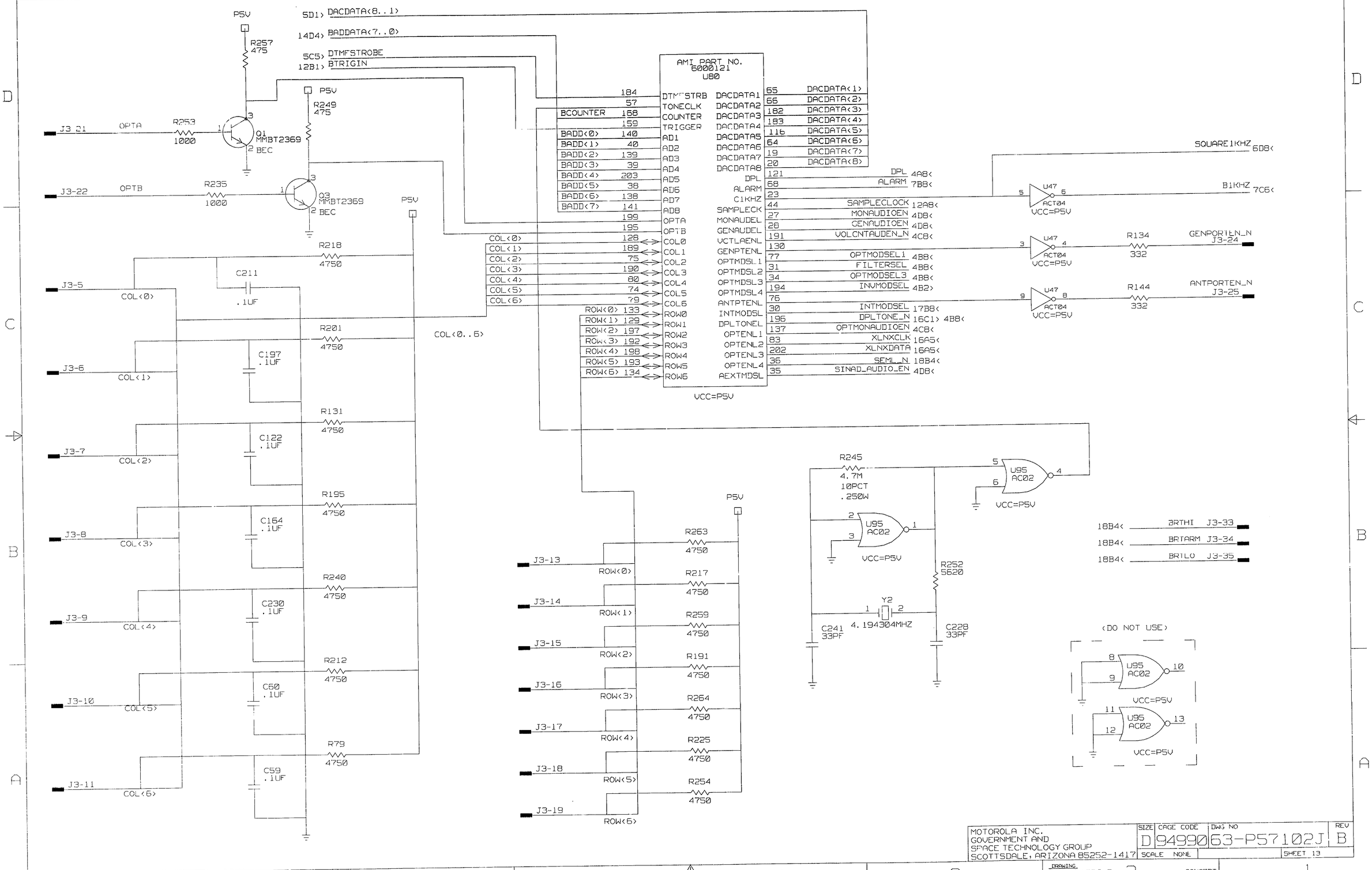
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57102J	REV B
	SCALE NONE		SHEET 11	

DRAWING 63P57102J-B 63P57102J CONCEPT



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57102J	REV B
	SCALE NONE		SHEET 12	

DRAWING 63P57102J-B 63P57102J CONCEPT

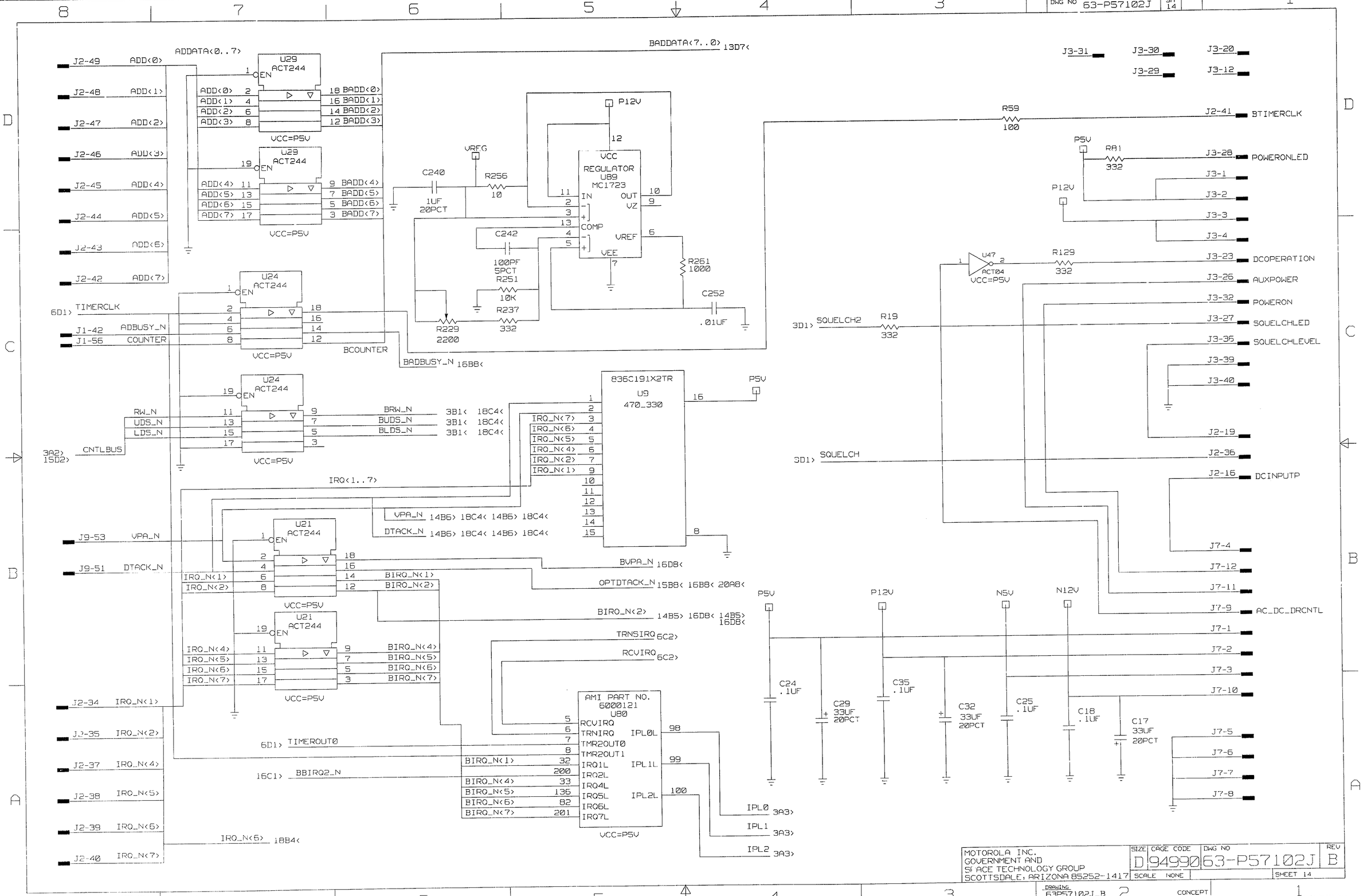


MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

SIZE	CAGE CODE	DWG NO	REV
D	94990	63-P57102J	B

SCALE NONE | SHEET 13

DRAWING 63P57102J-B 63P57102J | CONCEPT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BADDATA<7..0> 13D7<
U29 ACT244
U24 ACT244
U21 ACT244
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J2-49 ADD<0>
J2-48 ADD<1>
J2-47 ADD<2>
J2-46 ADD<3>
J2-45 ADD<4>
J2-44 ADD<5>
J2-43 ADD<6>
J2-42 ADD<7>
BADD<0>
BADD<1>
BADD<2>
BADD<3>
BADD<4>
BADD<5>
BADD<6>
BADD<7>
6D1> TIMERCLK
J1-42 ADBUSY_N
J1-56 COUNTER
BCOUNTER
BADBUSY_N 16B8<
RW_N
UDS_N
LDS_N
3A2>
15D2> CNTLBUS
BRW_N 3B1< 18C4<
BUDS_N 3B1< 18C4<
BLDS_N 3B1< 18C4<
IRQ<1..7>
VPA_N 14B6> 18C4< 14B6> 18C4<
DTACK_N 14B6> 18C4< 14B6> 18C4<
J9-53 VPA_N
J9-51 DTACK_N
BVPA_N 16D8<
OPTDTACK_N 15B8< 16B8< 20A8<
BIRQ_N<2> 14B5> 16D8< 14B5> 16D8<
TRNSIRQ 6C2>
RCVIRQ 6C2>
836C191X2TR
U9
470_330
P5V
IRQ_N<7>
IRQ_N<6>
IRQ_N<5>
IRQ_N<4>
IRQ_N<2>
IRQ_N<1>
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VREG
C240 1UF 20PCT
R256 10
VCC
REGULATOR
U89
MC1723
IN
OUT
VZ
COMP
VREF
VEE
C242 100PF 5PCT
R251 10K
R237 332
R229 2200
R261 1000
C252 .01UF
R59 100
J2-41 BTIMERCLK
P5V
R81 332
J3-28 POWERONLED
P12V
J3-1
J3-2
J3-3
J3-4
U47 ACT04
VCC=P5V
R129 332
J3-23 DCOPERATION
J3-26 AUXPOWER
J3-32 POWERON
3D1> SQUELCH2
R19 332
J3-27 SQUELCHLED
J3-36 SQUELCHLEVEL
J3-39
J3-40
J2-19
3D1> SQUELCH
J2-36
J2-16 DCINPUTP
J7-4
J7-12
J7-11
J7-9 AC_DC_DRCNTL
J7-1
J7-2
J7-3
J7-10
J7-5
J7-6
J7-7
J7-8
J3-31
J3-30
J3-29
J3-20
J3-12
P5V
P12V
N5V
N12V
C24 .1UF
C29 33UF 20PCT
C35 .1UF
C32 33UF 20PCT
C25 .1UF
C18 .1UF
C17 33UF 20PCT
J2-34 IRQ_N<1>
J2-35 IRQ_N<2>
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J2-38 IRQ_N<5>
J2-39 IRQ_N<6>
J2-40 IRQ_N<7>
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U80
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TMR2OUT0
TMR2OUT1
IRQ1L
IRQ2L
IRQ4L
IRQ5L
IRQ6L
IRQ7L
IPL0L
IPL1L
IPL2L
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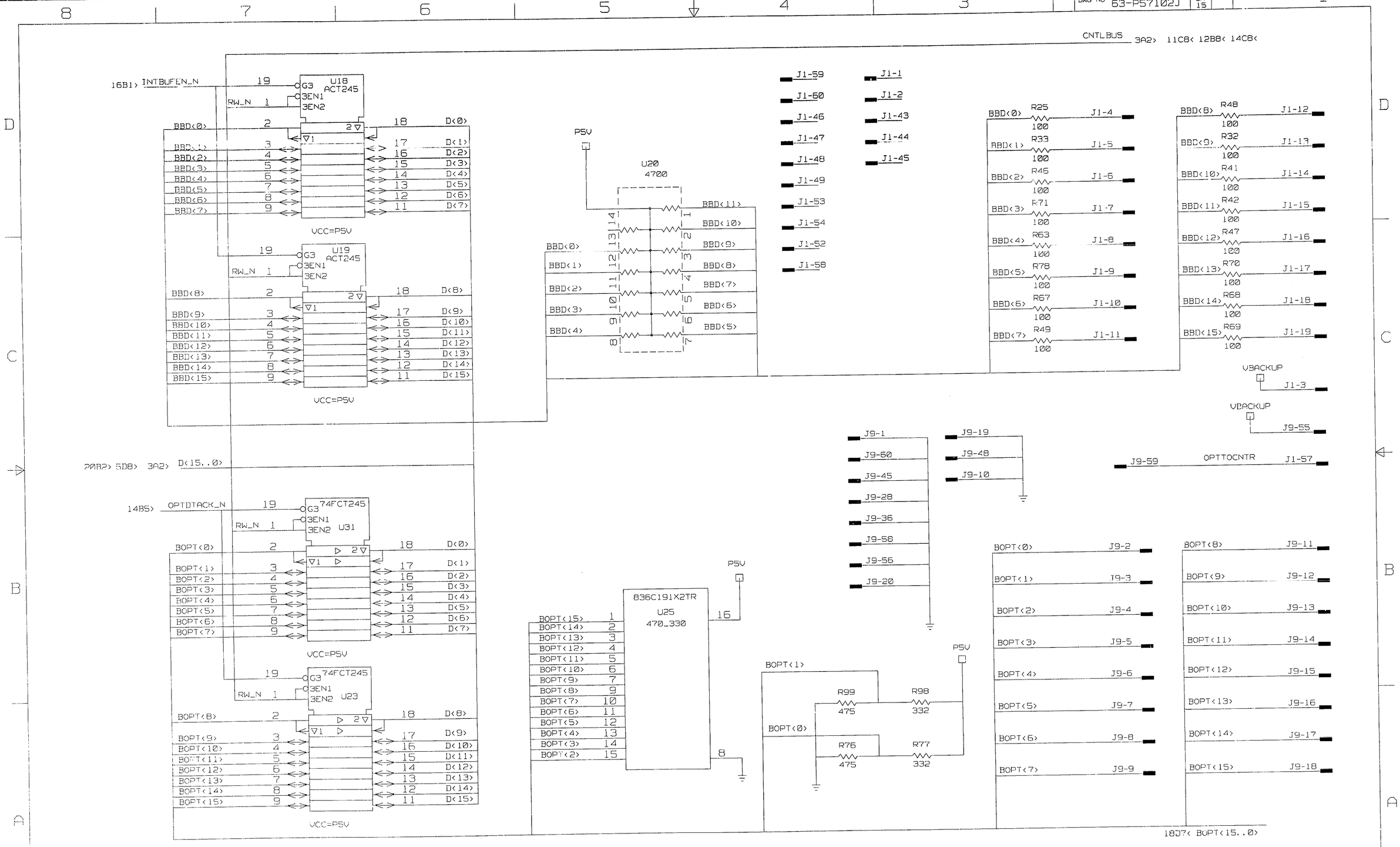
BIRQ_N<4> 33
BIRQ_N<5> 136
BIRQ_N<6> 82
BIRQ_N<7> 201
IPL0 3A3>
IPL1 3A3>
IPL2 3A3>
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D
CAGE CODE 94990
DWG NO 63-P57102J
REV B
SCALE NONE
SHEET 14
DRAWING 63P57102J-B 63P57102J
CONCEPT
ASME Y14.1-1995 DRAWING FORMAT - 3/95



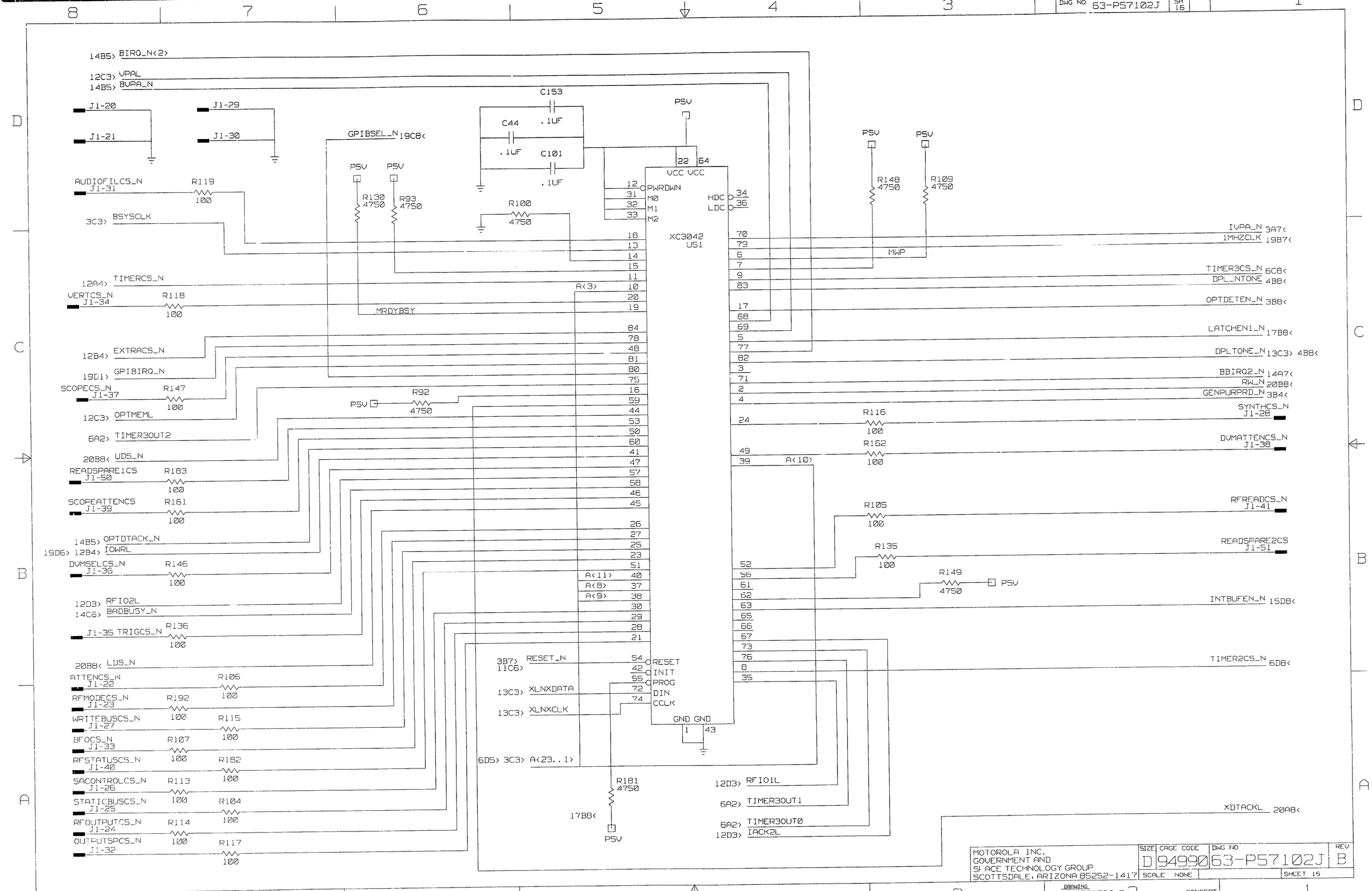
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

SIZE	CAGE CODE	DWG NO	REV
D	94990	63-P57102J	B

SCALE NONE SHEET 15

DRAWING 63P57102J-B 2 63P57102J CONCEPT 1 CSIZEPAGE2MDK

ASME Y14.1-1995 DRAWING FORMAT - 3/95



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57102J	REV B
	SCALE NONE			SHEET 15

ASME Y14.1-1995 DRAWING FORMAT - 3/05

DRAWING 63P57102J-B 63P57102J

CONCEPT

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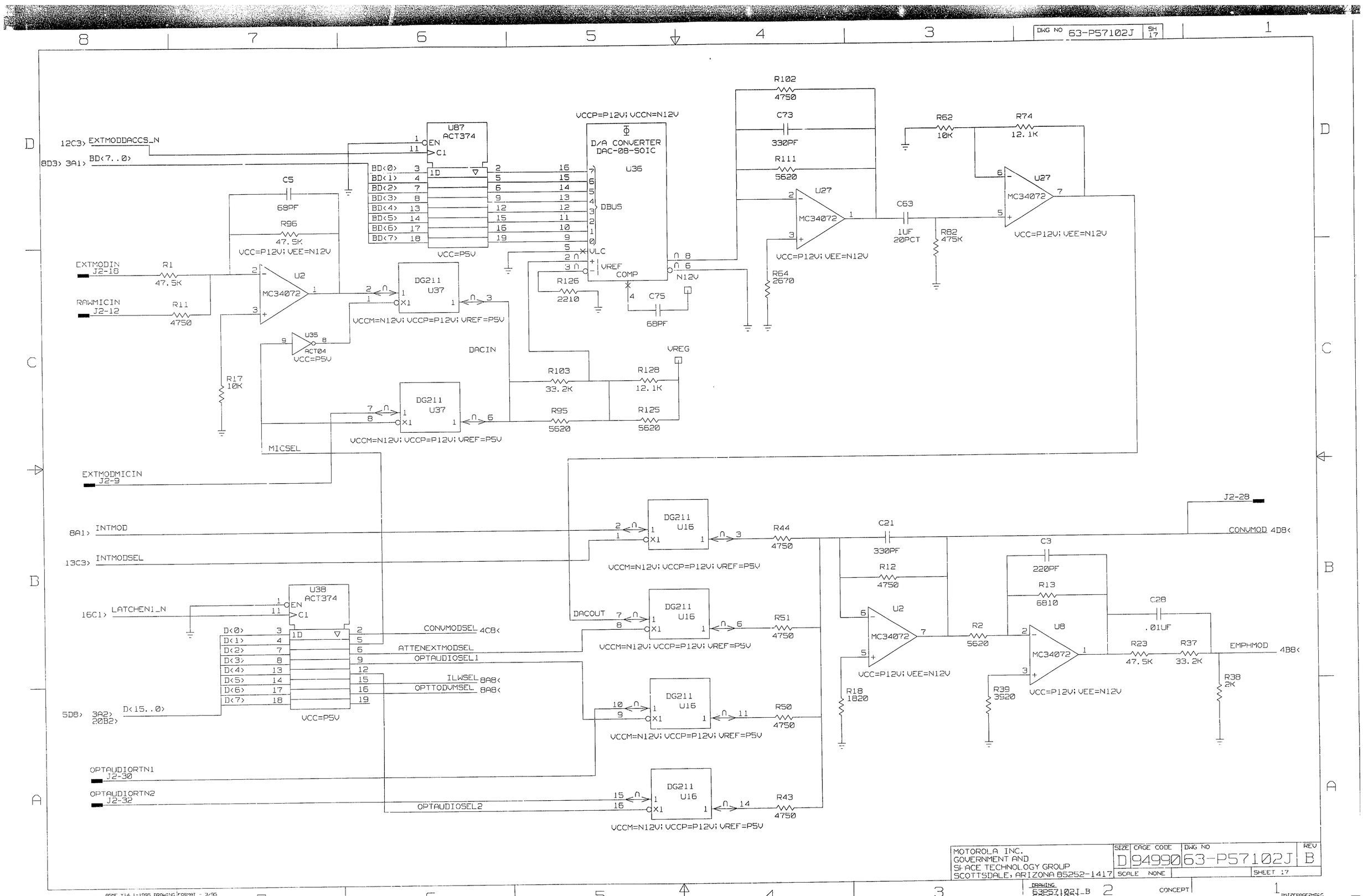
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8D3> 3A1> BD<7..0>
U87 ACT374
EN
C1
1D
BD<0> BD<1> BD<2> BD<3> BD<4> BD<5> BD<6> BD<7>
VCC=P5V
VCCP=P12V; VCCN=N12V
D/A CONVERTER DAC-08-SOIC
U36
DBUS
VLC
VREF
COMP
N12V
R102 4750
C73 330PF
R111 5620
R62 10K
R74 12.1K
U27 MC34072
C63 1UF 20PCT
R82 475K
VCC=P12V; VEE=N12V
R64 2670
C5 68PF
R96 47.5K
EXTMODIN J2-18
R1 47.5K
RAWMICIN J2-12
R11 4750
U2 MC34072
DG211 U37
VCCM=N12V; VCCP=P12V; VREF=P5V
R126 2210
C75 68PF
U35 ACT04
DACIN
VREG
R17 10K
R103 33.2K
R128 12.1K
R95 5620
R125 5620
MICSEL
EXTMODMICIN J2-9
J2-28
8A1> INTMOD
13C3> INTMODSEL
DG211 U16
R44 4750
C21 330PF
R12 4750
CONVMOD 4D8<
C3 220PF
R13 6810
C28 .01UF
16C1> LATCHEN1_N
U38 ACT374
D<0> D<1> D<2> D<3> D<4> D<5> D<6> D<7>
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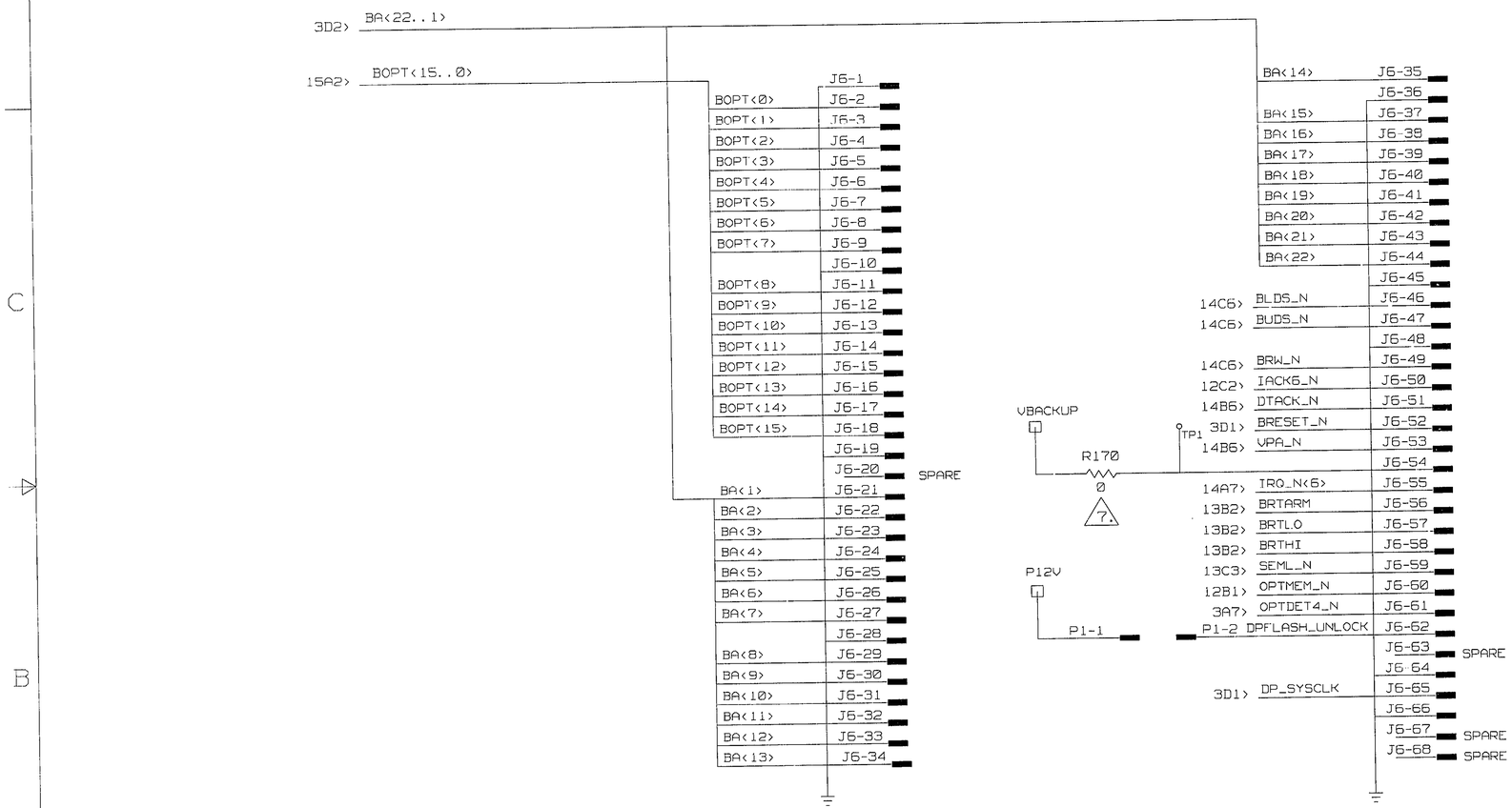
ATTENEXTMODSEL
OPTAUDIOSEL1
ILWSEL 8A8<
OPTTODVMSEL 8A8<
DACOUT
R51 4750
R2 5620
R23 47.5K
R37 33.2K
EMPHMOD 4B8<
R38 2K
R18 1820
R39 3920
5D8> 3A2> 20B2> D<15..0>
R50 4750
OPTAUDIORTN1 J2-30
OPTAUDIORTN2 J2-32
OPTAUDIOSEL2
R43 4750
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D
CAGE CODE 94990
DWG NO 63-P57102J
REV B
SCALE NONE
SHEET 17
DRAWING 63P57102J-B 63P57102J
CONCEPT
ASME Y14.1-1995 DRAWING FORMAT - 3/95



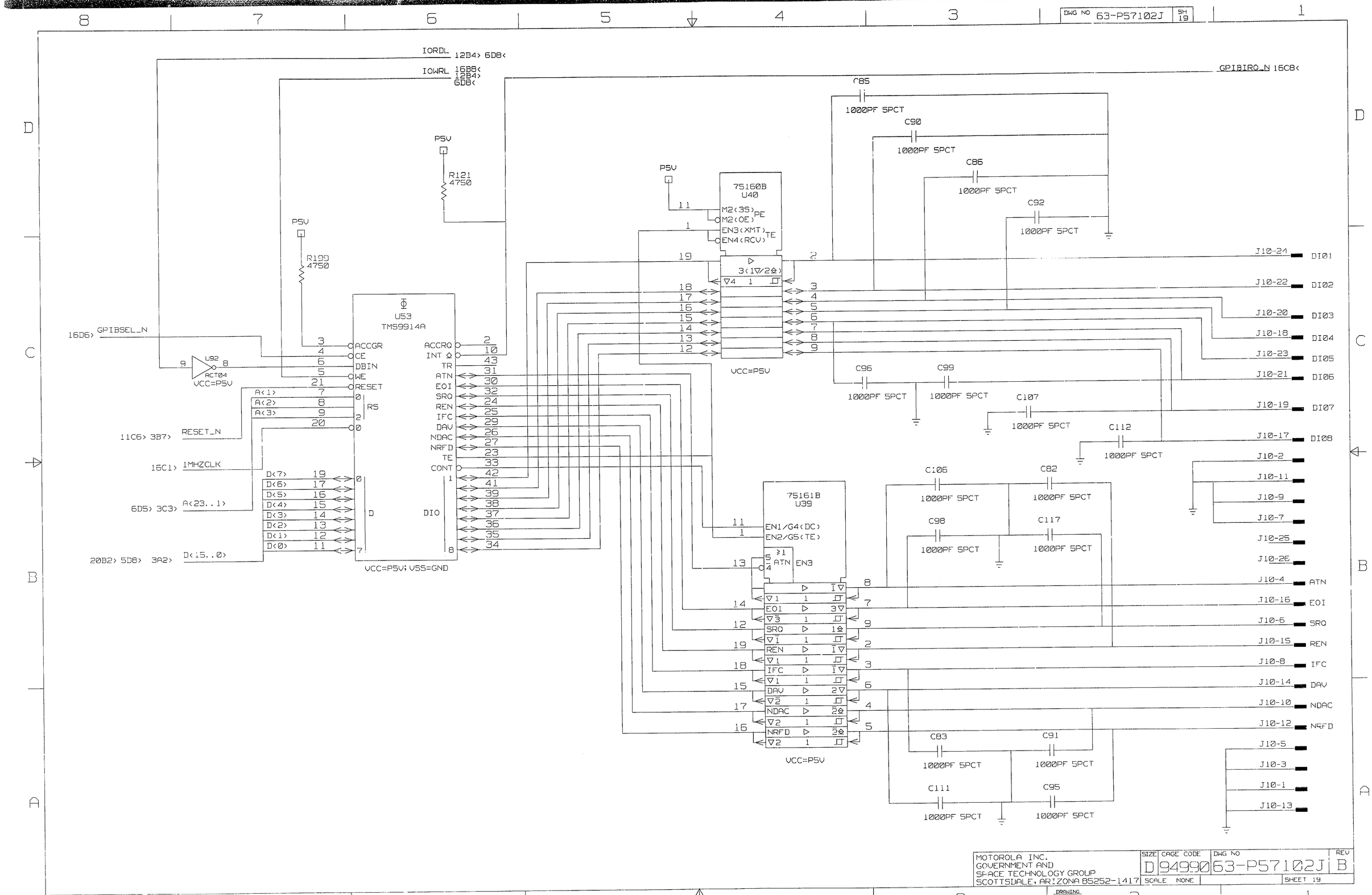
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57102J	REV B
	SCALE NONE		SHEET 18

DRAWING 63P57102J 63P57102J_B

CONCEPT

ASME Y14.1-1995 DRAWING FORMAT - 3/95

DSIZEPAGE2MD2L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IOWRL 16B8< 12B4> 6D8<
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P5V
R121 4750
R199 4750
16D6> GPIBSEL_N
U92 ACT04
VCC=P5V
U53 TMS9914A
ACCGR
CE
DBIN
WE
RESET
RS
ACCRQ
INT
TR
ATN
EOI
SRQ
REN
IFC
DAV
NDAC
NRFD
TE
CONT
DIO
A<1>
A<2>
A<3>
11C6> 3B7> RESET_N
16C1> 1MHZCLK
6D5> 3C3> A<23..1>
20B2> 5D8> 3A2> D<15..0>
D<7>
D<6>
D<5>
D<4>
D<3>
D<2>
D<1>
D<0>
VCC=P5V; VSS=GND
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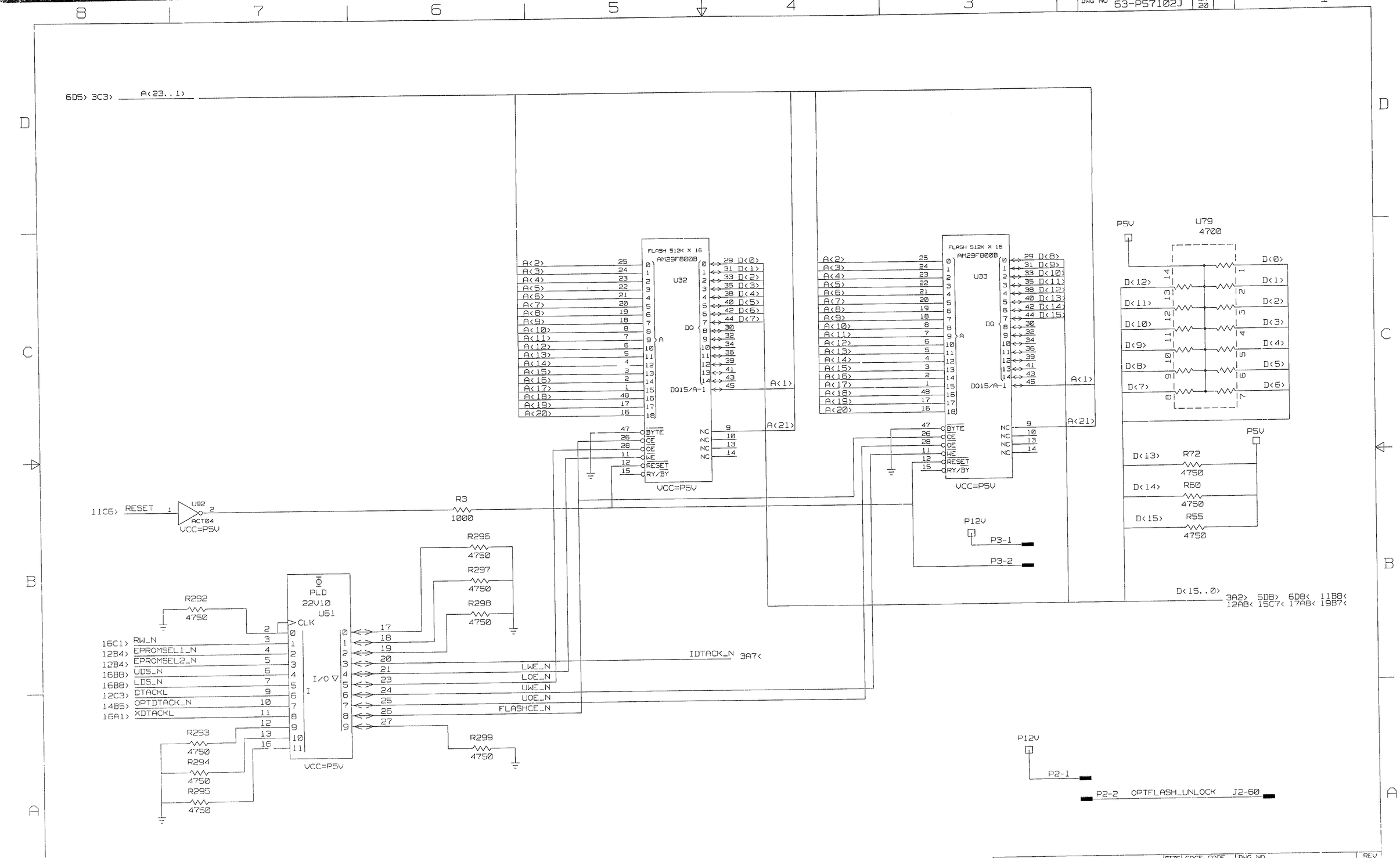
M2<3S>
M2<OE>
PE
EN3<XMT>
EN4<RCV>
TE
3<1▽/2◇>
VCC=P5V
75161B U39
EN1/G4<DC>
EN2/G5<TE>
≥1
ATN
EN3
EOI
SRQ
REN
IFC
DAV
NDAC
NRFD
VCC=P5V
C85 1000PF 5PCT
C90 1000PF 5PCT
C86 1000PF 5PCT
C92 1000PF 5PCT
C96 1000PF 5PCT
C99 1000PF 5PCT
C107 1000PF 5PCT
C112 1000PF 5PCT
C106 1000PF 5PCT
C82 1000PF 5PCT
C98 1000PF 5PCT
C117 1000PF 5PCT
C83 1000PF 5PCT
C91 1000PF 5PCT
C111 1000PF 5PCT
C95 1000PF 5PCT
J10-24 DIO1
J10-22 DIO2
J10-20 DIO3
J10-18 DIO4
J10-23 DIO5
J10-21 DIO6
J10-19 DIO7
J10-17 DIO8
J10-2
J10-11
J10-9
J10-7
J10-25
J10-26
J10-4 ATN
J10-16 EOI
J10-6 SRQ
J10-15 REN
J10-8 IFC
J10-14 DAV
J10-10 NDAC
J10-12 NRFD
J10-5
J10-3
J10-1
J10-13
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D
CAGE CODE 94990
DWG NO 63-P57102J
REV B
SCALE NONE
SHEET 19
DRAWING 63P57103J-B 63P57102J
CONCEPT
ASME Y14.1-1995 DRAWING FORMAT - 3/95



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57102J	REV B
	SCALE NONE		SHEET 20	

MOTORO
SPACE AND SYSTEMS
TECHNOLOGY GROUP

SIZE SHEETS
ASSOC LIST:
DOC:

	RESP. ENGINEER
SIGNATURES	A. Gatto
DATE	10/19/2000
PHONE/AREA	1-6924

10-26-00

FILE
MFG. ENG.
MATL.
QA
TEST

FG. X5
NTEGRA
S/M
S/C
MFG. PLNR.
FROM REPRO :
PDO DIST :
PRINTS DIST :

PRODUCT DEFINITION ORDER

CONTRACT NO.

REFER TO SPP-17 SERIES FOR FORM INSTRUCTIONS

EQUIPMENT P.I.A. NO.(S)	P.I.A.PROGRAM TITLE
10744	COCHISE

DOCUMENTATION CHARGE NO. 10744-1100

	A	DISTRIBUTE PRINT WITH RN
	B	INCORP IMMED AFTER MCO DIST
	C	DIST CHANGED PRINT WITH MCO
	D	ACCUMULATE CHANGE-DISTR MCO
X	E	DISTRIBUTE VA

RETURN DOC ORIG TO DC
RETURN PDO ORIG TO DC

DISTRIBUTION CODE	REPRODUCTION QTY C	P	A	D	F
1103-04	15				

CHANGE CLASSIFICATION

	NOT APPLICABLE
	CLASS I
X	CLASS II

GOVT APPVL OF CLASS N/A DATE

CUST APPROVAL OF CLASS N/A DATE

INTERCHANGEABILITY STATUS

	NOT APPLICABLE
X	TWO-WAY
	NON

APPROVAL REQUIRED

CUST		YES	X	NO
GOVT		YES	X	NO
PRG MGR		YES	X	NO
PRG MGR		YES	X	NO

PROJECT INCORP CHECK REQUIRED BY TONY GATTO EXT 1-6924

DOCUMENT OR PART NO. 01-P57100J CLASSIFIED DOC

PRESENT REVISION	NEW REVISION
-	~

ASSOCIATED LIST PL WL

TITLE CIRCUIT CARD ASSEMBLY MICROPROCESSOR

NEXT HIGHER ASSY PART NO(S) 01-P30203C001, 01-P57060J001

APPVL	ORIGINAL	REVISION R1	REVISION R2
ORIG	A. GATTO		
DATE	10/19/00		
EXT NO	1-6924		
R&D	A. Gatto		
DATE	10/19/2000		
MFG	J Mamx		
DATE	10-20-2000		
MATL	W. Meinhart		
DATE	10-20-00		
QA	T. Downs		
DATE	10/20/00		
TEST	B. Watts		
DATE	10-20-00		
CDM	C. Galligan		
DATE	10-20-00		

MASTER CHANGE ORDER	MCO				DASH
CHANGE ORDER	CO				-
RELEASE NOTICE	RN				-
VARIATION AUTHORITY	VA	X	B35551		-200
STOP ORDER	SO				-
INFORMATION MEMO	IM				-

BASIC NO. REV

THERE ARE / RELATED DASH NUMBERS TO BASIC NO
THIS CHANGE CANCELS VA OR SO NO.

SOFTWARE IMPACTS

OPERATIONAL SOFTWARE	YES		NO	X
TEST SOFTWARE	YES		NO	X

HARDWARE EFFECTIVITY

TYPE	FIRM		PLANNED	X	RECORD
LEVEL	END ITEM		SUB-ASSY	X	PART
CONT NO	01-P57100J001				
C.I. NO.					
S/N					
LOT					
DATE					
REWORK / RETROFIT	NO		YES	X	SEE BELOW X

MAT'L DISPOSITION/MFG. EFFECTS

NONE

EFFECTIVE IMMEDIATELY ON ALL R26XX/D SYSTEMS

REWORK/RETROFIT ALL WIP AND BONDED SYSTEMS

REMARKS:

Carolyn Galligan 441-1824

REASON FOR ORDER:

MODIFICATION REDUCES RADIATED EMISSIONS AND SUSCEPTIBILITY WHEN EXTERNAL MICROPHONE IS ATTACHED TO R26XX/D SYSTEMS
THIS CHANGE AND THE MODIFICATION OUTLINED IN VA B35551-199 ARE REQUIRED FOR THE NEW R26XX/D MODEL TO MEET CE SPECIFICATIONS FOR RADIATED EMISSIONS AND SUSCEPTIBILITY.

SERVICE CENTER DISTRIBUTION YES X NO

FORMAT USED:
CADAM CATIA ALLEGRO PRO-E META
WP5 W5.1 WORD DESIGNER

NO. B35551-200

*COMPUTER GENERATED EXCEL 4.0

B35551-200-01

SPACE SYSTEMS TECHNOLOGY GROUP

PRODUCT DEFINITION ORDER

*CONTINUATION SHEET

ITEM	DOCUMENT NO.	REV	OWC	DESCRIPTION	DOC SIZE	NEXT HIGHER ASSY.

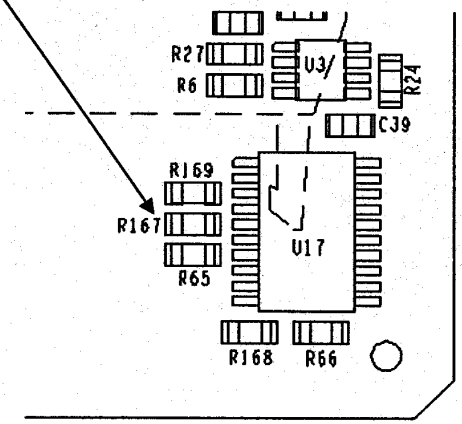
BASIC NO.					REV
MASTER CHANGE ORDER	MCO			DASH	
CHANGE ORDER	CO		-		
RELEASE NOTICE	RN		-		
VARIATION AUTHORITY	VA	X	B35551 - 200		
STOP ORDER	SO		-		
INFORMATION MEMO	IM		-		
DOCUMENT/PART REF NO					

MAT'L DISPOSITION /MFG. EFFECTS CONT.

1. REMOVE R167 (SEE FIG. 1)
2. SOLDER INDUCTOR P/N 24-P26371A105 (2.2 UH - 10) IN LOCATION R167 (SEE FIG.2.)
3. SOLDER ONE END OF CAPACITOR P/N 2113740B49 (100 PF - 5 - 50) TO PIN 1 OF U17 AS SHOWN IN FIG. 2.
4. SOLDER A 30 GAUGE INSULATED JUMPER WIRE TO 100 PF CAPACITOR AND 2.2 UH INDUCTOR AS SHOWN IN FIG. 2.

REMOVE R167

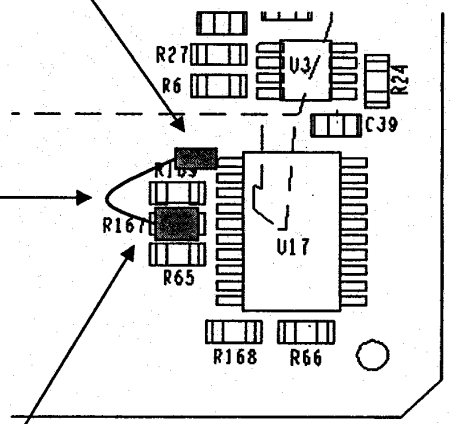
FIG. 1



SOLDER ONE END OF P/N 2113740B49 (100 PF - 5 - 50) TO PIN 1 OF U17

SOLDER A 30 GAUGE INSULATED JUMPER WIRE TO 2.2 UH INDUCTOR AND 100 PF CAPACITOR AS SHOWN

FIG. 2



SOLDER P/N 24-P26371A105 (2.2 UH) IN LOCATION R167

NO. B35551-200

QTY PER	VENDOR NAME	FIND NO.	QTY REQ	CODE IDENT NO	DRAWING OR DOCUMENT NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	SUPPLEMENTARY PART OR IDENTIFYING NO	NOTES

*COMPUTER GENERATED EXCEL 4.0

B35551-200-02

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Go to Section 16

15.1 GENERAL DESCRIPTION

The Front Panel assembly is designated as Al and provides the main operator interface for the Analyzer.

The EMI Filter Module (designated A1A1) is considered part of the Front Panel assembly. It provides filtering for all signals between the Front Panel's J1 connector and the Processor Module's J3 connector.

15.2 SIGNALS SUMMARY

15.2A Signal Descriptions

15.2A.1 J1 (Processor Module)

ANT PORT ENABLE input indicates which port is enabled when receiving RF. It drives the Ant Port Enable LED. A logic 1 indicates the Antenna Port is enabled.

AUX POWER input is routed to the front panel power switch. When the power switch is closed, the POWER ON signal enables the power supply.

BRT, *BRT ARM*, and *BRT LO* are connections for the external brightness potentiometer. The Processor Module only serves as the connection between the Front Panel and the Display Processor board.

COL 0-6 lines connect the seven columns of keys at the front panel keypad with the ASIC at the Processor Module.

DC OPERATION input indicates when the DC power plug is being used to supply power to the unit. A logic 0 indicates AC operation while a logic 1 indicates DC operation. This signal drives the DC Operation LED.

GEN PORT ENABLE input indicates which port is enabled when generating RF. A logic 1 indicates the Generator Port is enabled. This signal drives the Gen Port Enable LED.

OPT A, *OPT B* indicate phase "A" and phase "B" of the optical tuning knob at J2.

POWER ON output signal is routed through the Processor Module to the Power Supply. It is a control voltage to enable/disable the Power Supply.

POWER ON LED input drives the Power On LED.

ROW 0-6 lines connect the seven rows of keys at the front panel keypad with the ASIC at the Processor Module.

SQUELCH LED input drives the Squelch LED.

SQUELCH LEVEL output from the Squelch Level potentiometer indicates the operator-adjusted squelch level of the system. The Processor Module routes this signal to the Interface Module.

VOL CNTL AUDIO and *VOL CNTL AUDIO RTN* are used with the operator-adjusted Volume potentiometer.

15.2A.2 J2 Optical Tuning Knob

OPT A, *OPT B* indicate the phase "A" phase "B" of the optical tuning knob. These signals are routed directly to J1 for use by the ASIC on the Processor Module.

15.2A.3 Front Panel Connectors

DEMOD OUT TO FP drives the BNC "DEMOD OUT" connector. The Interface Module creates this signal using the SQUELCHED DEMOD signal.

FP ANTENNA is the front panel Antenna Port Signal sent to the RF Input Module.

FP EXT MOD IN output to the Interface Module is the signal from the "EXT MOD IN" BNC connector.

FP MIC IN is the microphone input from the front panel that is sent to the Interface Module. This input is compatible with a Motorola HMN-1056C.

FP GEN OUT is the output signal from the RF Wattmeter for the Gen Out port on the front panel.

HANDSET AUDIO is the audio signal provided to the handset from the Processor Module.

METER IN from BNC connector at front panel is sent to the Interface Module. From there, it can be an input signal to the

Spectrum Analyzer, Oscilloscope, Digital Voltmeter, SINAD/Distortion Meter, and the Frequency/Period Counter (depending upon which function is selected).

MOD OUT TO FP drives the MOD OUT connector at the front panel. It is a buffered and amplified version of MOD CAL AUDIO from the Interface Module

PTT is the Push-To-Talk connection from the handset that indicates when the microphone has been keyed.

RF I/O line is a bi-directional signal, which is used as a high level input or low level output port to/from the RF Wattmeter.

15.2B Connector Descriptions

15.2B.1 J1 (Processor Module)

pin	
1,2	+5V
3A	+12V
5-11	COL 0-6 (keyboard columns 0-6)
12	not used
13-19	ROW 0-6 (keyboard rows 0-6)
20	not used
21,22	OPT A and B (optical tuning knob)
23	DC OPERATION (DC operation enabled)
24	GEN PORT ENABLE (for LED)
25	ANT FORT ENABLE (for LED)
26	AUX POWER
27	SQUELCH LED
28	POWER ON LED
29-31	spares
32	POWER ON (power on return)
33-35	BRT, BRT ARM, BRT LO, (for LCD brightness potentiometer connections)
36	SQUELCH LEVEL (from squelch potentiometer)
37	VOL CNTL AUDIO (volume control audio)
38	VOL CNTL AUDIO RTN
39,40	GND
41-48	spare
49	AUX POWER
50	POWER ON (power on return)

15.2B.2 J2 (Optical Tuning Knob)

pin	
1	GND
2,3	OPT A and B
4	+5V
5,6	not used

15.2B.3 External Ports

The Front Panel does not process these signals in any way. Refer to the appropriate section in this manual for detailed information on a specific port.

15.3 DETAILED DESCRIPTION

15.3.1 Operator Indicators

The operator indicators described here are all red LEDs. Consult the operator's manual for a complete description of indications viewed in the LCD displays.

ANT PORT ENABLE is for RF monitor functions and indicates the Analyzer is using the ANTENNA port (upper right comer of front panel) for the RF input signal.

DC OPERATION indicates that the power supply is getting its power source from an external +11 to +18Vdc source. The Analyzer will automatically seek power from the external DC input at the backpanel in the absence of AC power.

GEN PORT ENABLE indicates during generator functions that the RF output signal is available at the front panel GEN OUT port.

POWER ON indicates the power supply is supplying power to the Analyzer.

SQUELCH indicate the received signal strength is strong enough to break squelch (according to the setting of the Squelch Level potentiometer).

15.3.2 Operator Controls

Only brief descriptions are given here. Consult the operators manual for information on how these controls are used. Figures 15.4.2A and 15.4.2B illustrate keypad usage in more detail.

15.3.2.1 KEYPAD

FUNCTION KEYS are used with menu driven displays that appear in the LCD screen.

CURSOR ZONE keys select one of the three display zones (display, RF, audio).

CURSOR POSITION keys select the screen position for operator input.

NUMERIC KEYPAD is used for operator determined input of numeric information.

Consult the operators manual for descriptions of remaining keys.

15.3.2.2 Other Controls

POWER ON switch connects a control voltage to enable the power supply.

BRIGHTNESS potentiometer controls the brightness level of the LCD Display.

SQUELCH LEVEL potentiometer allows the operator to adjust the signal strength required to break squelch.

VOLUME potentiometer sets the speaker volume level.

TUNING knob is used in conjunction with LCD displays. Consult the operators manual for information on the use of the optical tuning knob.

	Col 0	***Col 1***	***Col 2***	***Col 3***	***Col 4***	***Col 5***	***Col 6***
ROW 0	KEY 00	01	02	03	04	05	06
ROW 1	10	11	12	13			
ROW 2	20	21	22	23	24	25	26
ROW 3	30	31	32	33			
ROW 4	40	41	42	43	44	45	
ROW 5	50	51	52	53			
ROW 6	60	61					

Figure 15.3.2.A Keypad Matrix

Key Position		Key Label	Key Function
Key	00	0	Numerical Key Value 0
	01	1	Numerical Key Value 1
	02	2	Numerical Key Value 2
	03	3	Numerical Key Value 3
	04	A	Numerical Key Value 4
	05	5	Numerical Key Value 5
	06	6	numerical Key Value 6
	10	7	Numerical Key Value 7
	11	8	Numerical Key Value 8
	12	9	Numerical Key Value 9
	13	+/-	Toggle sign positive, negative
	20		Softkey #1
	21		Softkey #2
	22		Softkey #3
	23		Softkey #4
	24		Softkey #5
	25		Softkey #6
	26		Softkey #7
	30		Softkey #8
	31	RF	Move cursor to RF zone
	32	MOD	Move cursor to Modulation zone
	33	DISP	Move cursor to Display zone
	40	^	Move cursor upward
	41	v	Move cursor downward
	42	<	Move cursor left
	43	>	Move cursor right
	44	TAB	Move cursor to next field
	45	ALT	Alternate Function
	50	HELP	Help Display
	51	MEM	RF/Audio memory display
	52	SPF	Special Function
	53	F1	Return to Local Mode (if in remote mode)
	60	CAL	Calibration menu
	61	PRT	Print current screen

Figure 15.3.2B Keypad Labels and Functions

15.4 BLOCK DIAGRAMS

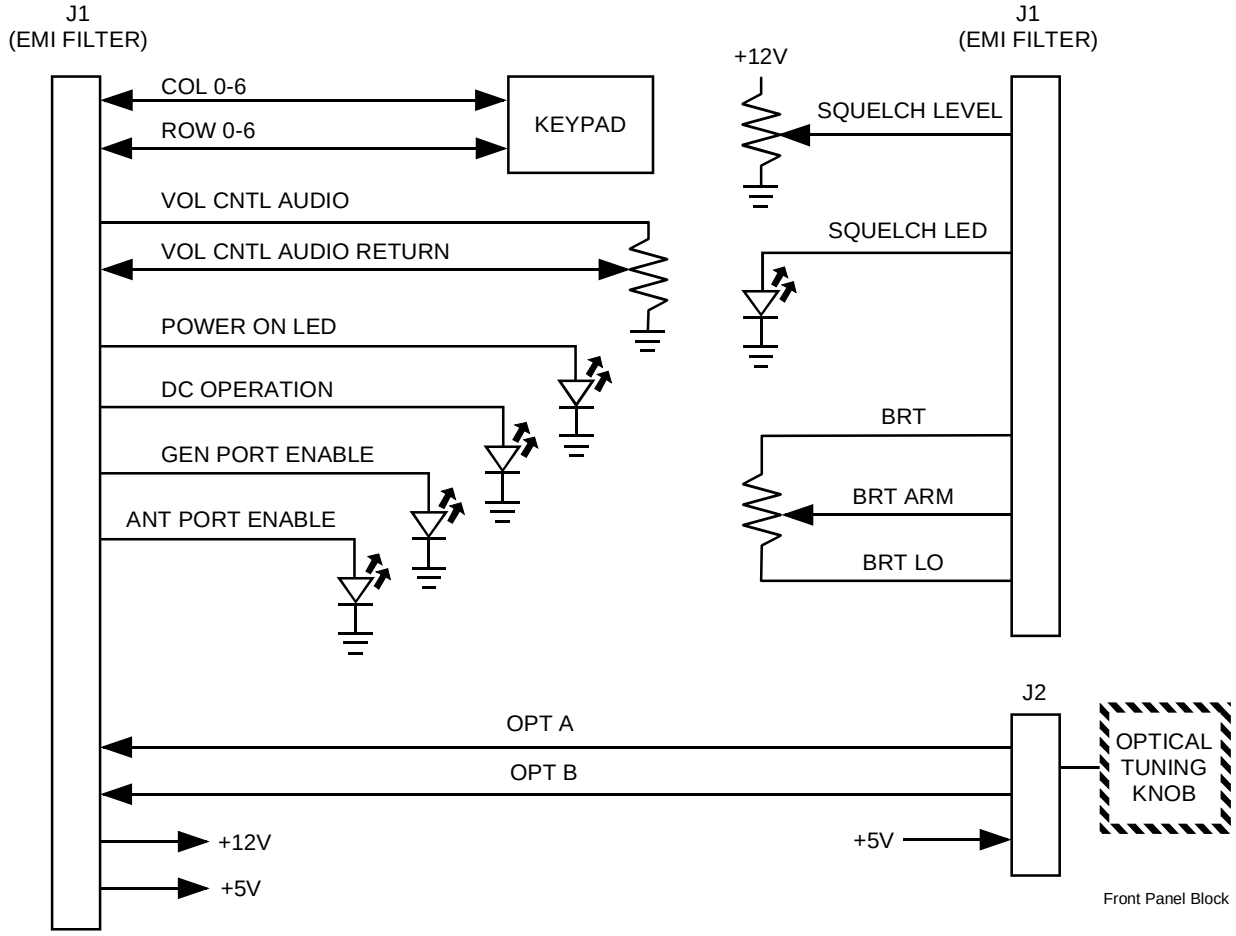


Fig. 15.4A Front Panel Block Diagram

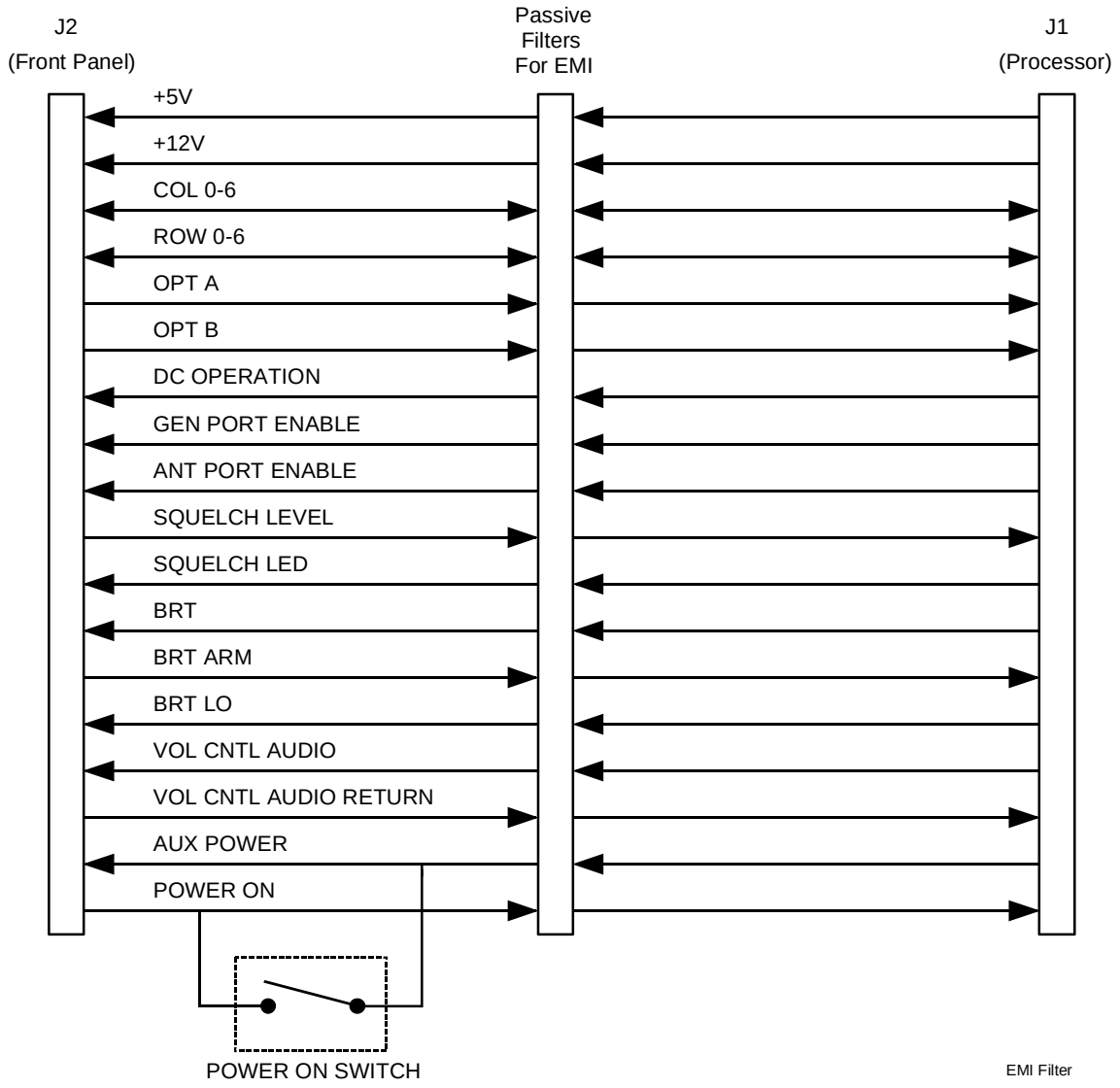
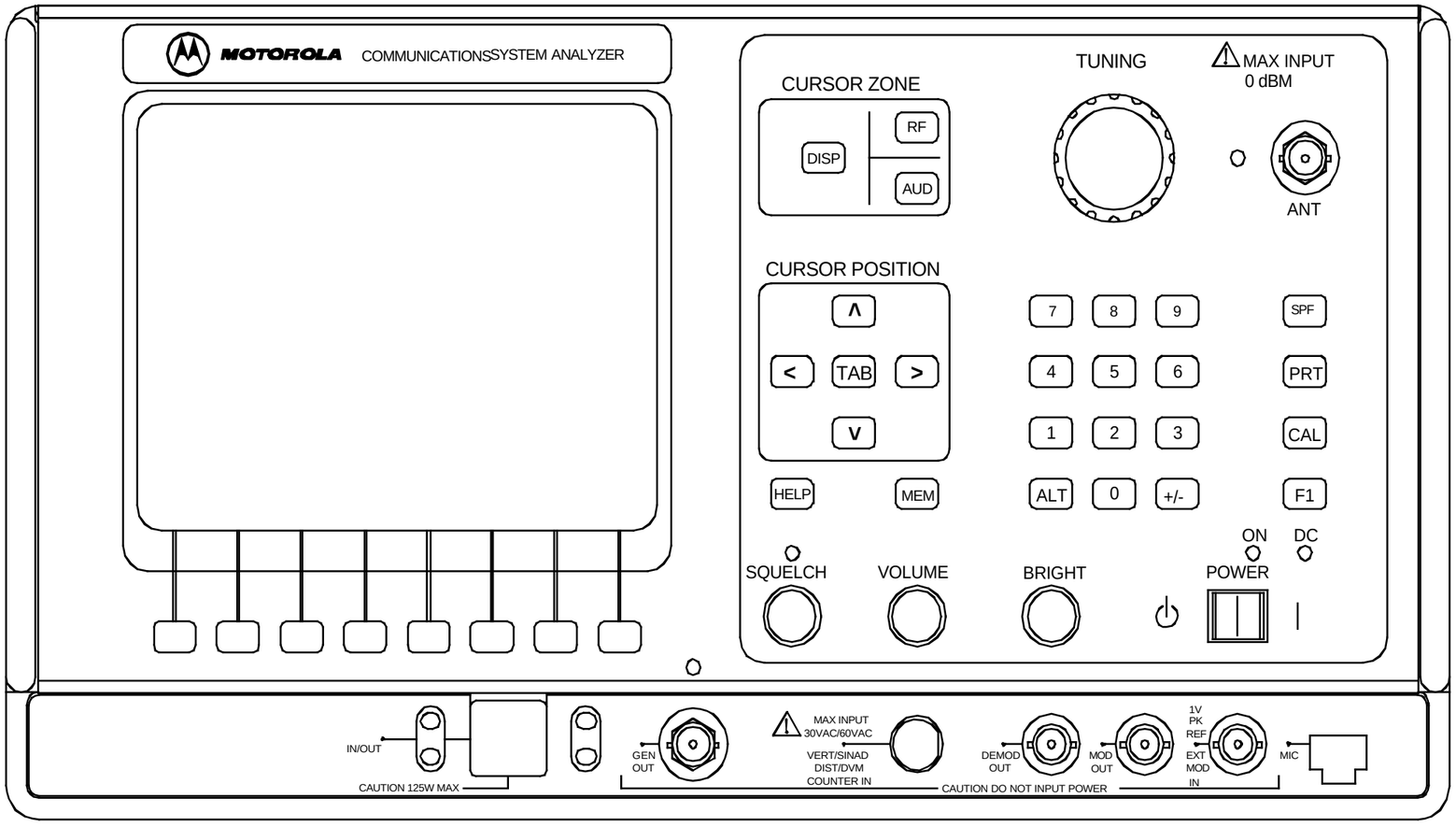
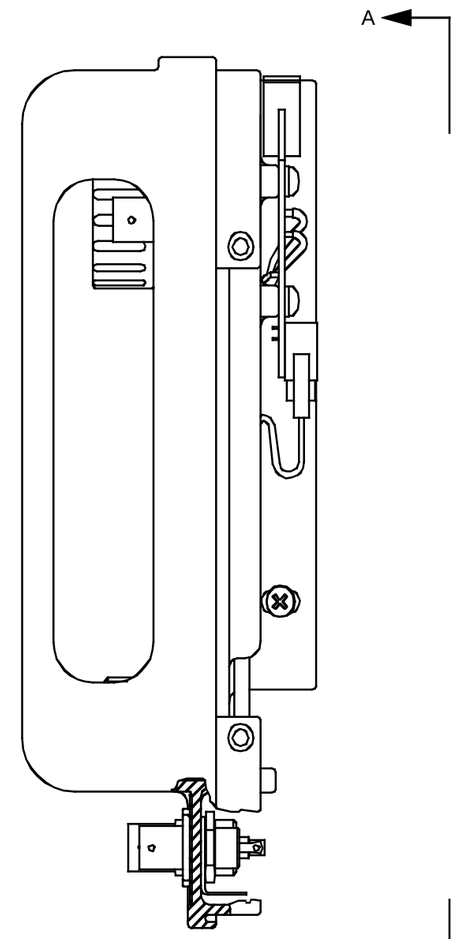


Fig. 15.4B EMI Filter Board Block Diagram

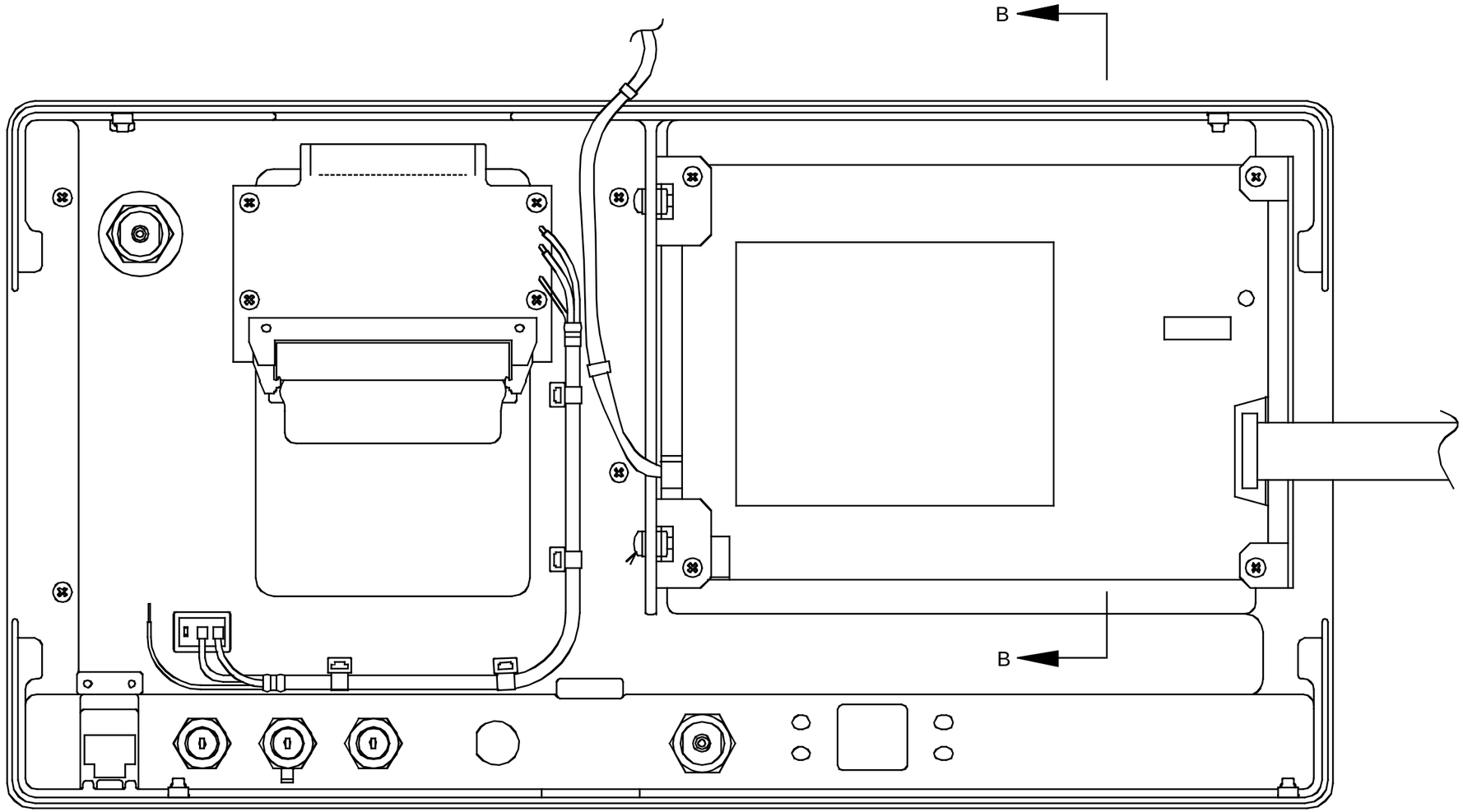




SEE
SHEET 2

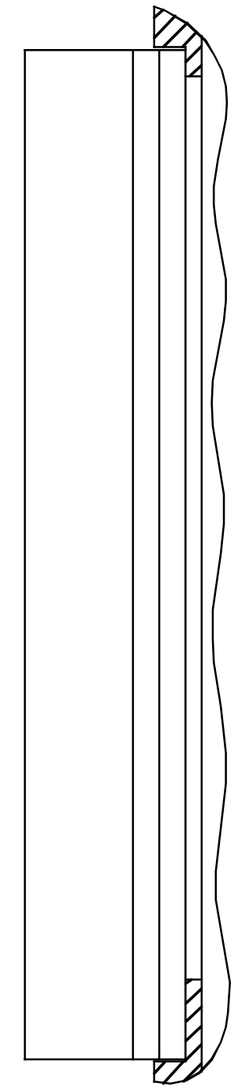
FRONT PANEL ASSEMBLY

01-P57055J REV. -



VIEW A-A

SEE SHEET 1

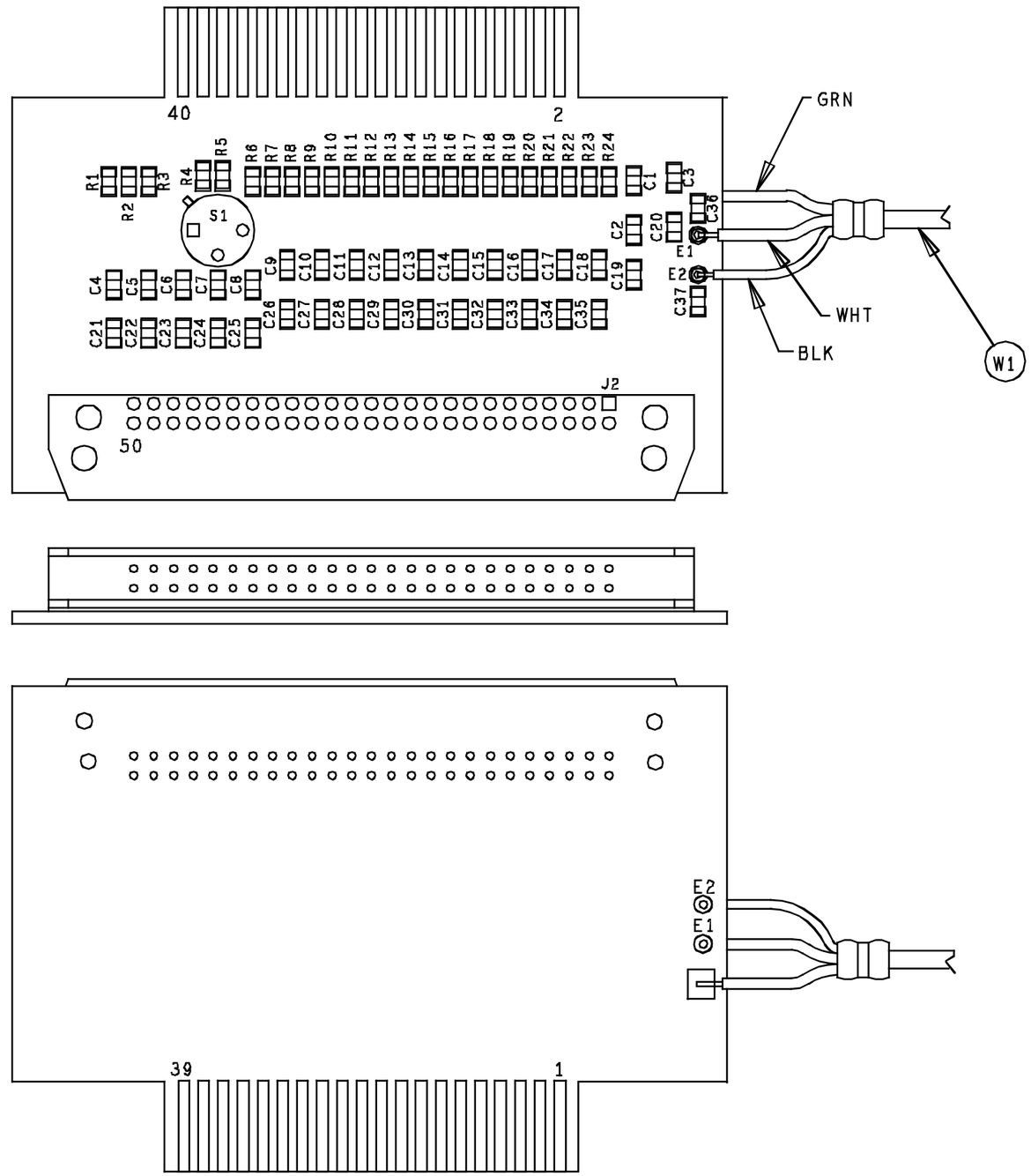


SECTION B-B

FRONT PANEL ASSEMBLY

01-P57055J REV. -

SHEET 2 OF 2



CAUTION
THIS ITEM IS SENSITIVE TO
ELECTROSTATIC DISCHARGE (ESD).

CIRCUIT CARD ASSEMBLY
EMI FILTER

01-P30480C REV. D

SHEET 1 OF 1

DWG NO	63-P30482C	SH 1

REVISION HISTORY

REV	DESCRIPTION	DATE	APPROVED
A	INITIAL REL RENUMBERED 2-27-90		
B	SEE MCO B35578 DG 90-05-11		
C	SEE MCO B35607 BB 90-06-12	90-06-14	D. DUNCAN
D	SEE CO E36152-3 DEB 95-08-07	95-08-07	KOESTNER

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH 1A1A2.

2. FOR REFERENCE DRAWINGS REFER TO:
   01-P30480C ASSEMBLY
   12-P30483C TEST PROCEDURE

3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL INDUCTANCE VALUES ARE IN UH.
   ALL VOLTAGES ARE IN DC.

4. TERMINATIONS CODED WITH THE SAME LETTERS OR NUMBERS ARE ELECTRICALLY CONNECTED.

REFERENCE DESIGNATIONS	
HIGHEST NUMBER USED	NOT USED
C37	
J2	
R24	
S1	

ALL SHEETS ARE THE SAME REVISION STATUS

		CONTR
		ISS B35550-53(A)90-04-17
		APPROVALS
		DWN D. WALKER 89-03-31
		CHKR
		QA J. M. MITCHELL 90-04-12
		MATL
01-P30480C	COCHISE	MFG J. DECAMP 90-04-12
NEXT ASSY	USED ON	ENG D. ZELINKA 90-04-12
APPLICATION		CUST

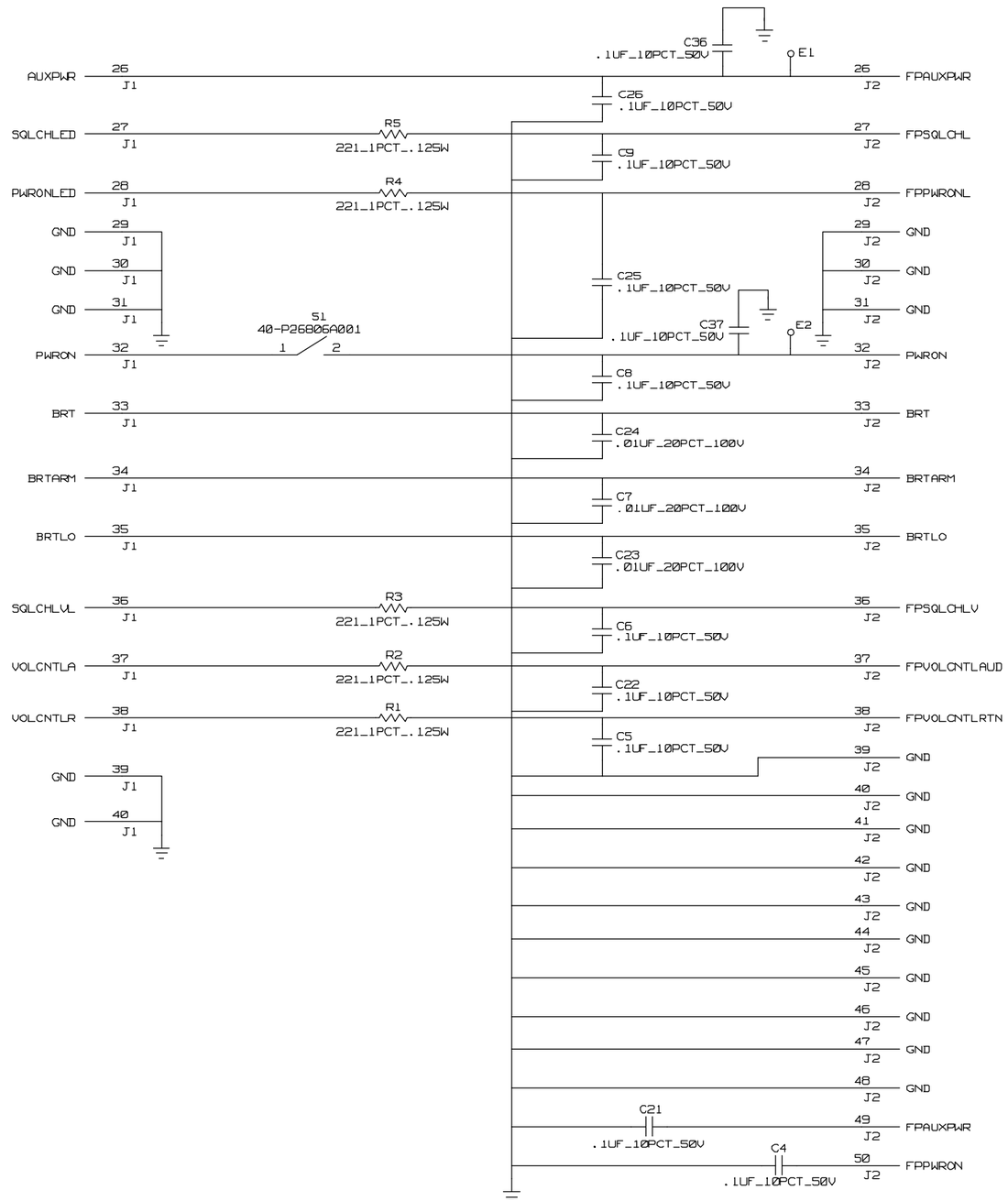
MOTOROLA INC.
GOVERNMENT AND SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

TITLE

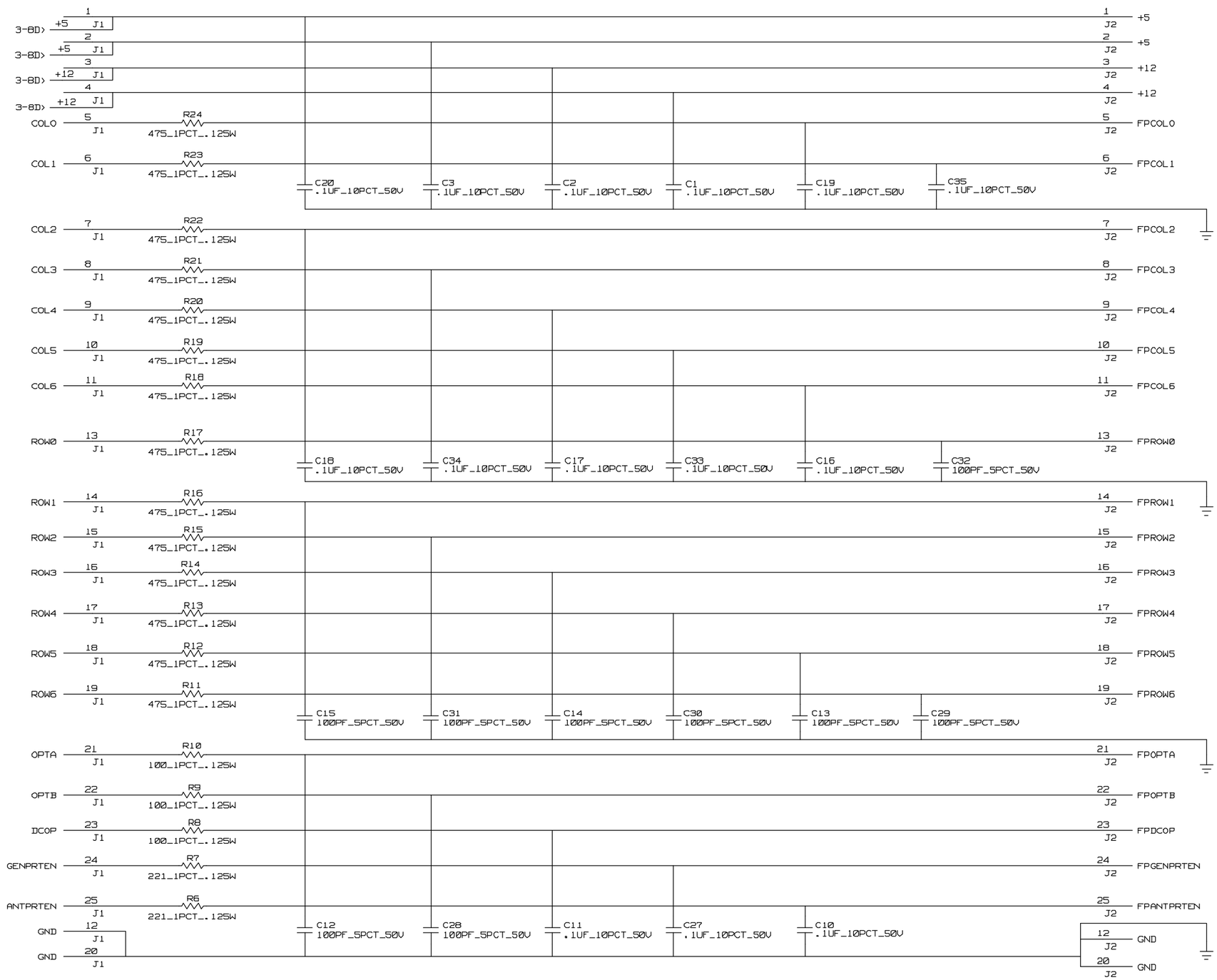
EMI FILTER SCHEMATIC DIAGRAM

SIZE	CAGE CODE	DWG NO
D	94990	63-P30482C

SCALE NONE SHEET 1 OF 3



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30482C	REV D
	SCALE NONE		SHEET 2	



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30482C	REV D
	SCALE NONE		SHEET 3	

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16.1 GENERAL INFORMATION

The Rear Panel Assembly is designated as A14.

This assembly provides the AC and DC power connections for the Analyzer's power supply. AC and DC power supply fuses (3A AC, 10A DC) are also accessible from the Rear Panel. When the optional battery is used, it is attached to the Rear Panel.

The 110/220 Vac selection switch is part of the power supply but is accessible from the bottom of the unit The Analyzer accepts a voltage of 90-132 Vac rms when the switch is in the 110 position and 184-264 Vac rms when in the 220 position. The Analyzer will accept either voltage range at frequencies from 47 to 440 Hz.

Additionally, the 10MHz IN/OUT connection for the Frequency Standard Module is located at the Rear Panel.

16.2 SIGNALS SUMMARY

LINE, GND, NEUTRAL are the external AC line connections routed to an EMI filter at the Rear Panel.

AC INPUT, AC RETURN are connections between the EMI filter plug and the power supply.

DC INPUT + and *DC INPUT*- are the optional DC supply connections (battery or DC operation) routed directly to the power supply.

10 MHz IN/OUT is the external connection with the Frequency Standard Module. IN/OUT operation is selected by switch S1, located at the bottom of the Analyzer. For more information on 10MHz standard, refer to Section 4 of this manual.

16.3 BLOCK DIAGRAM

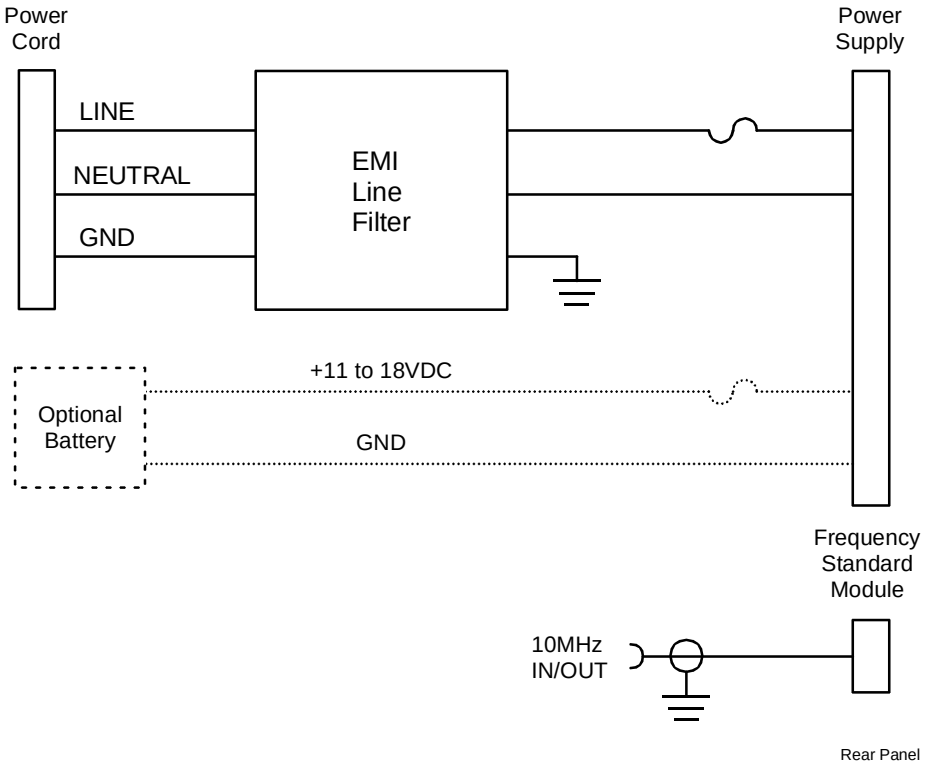
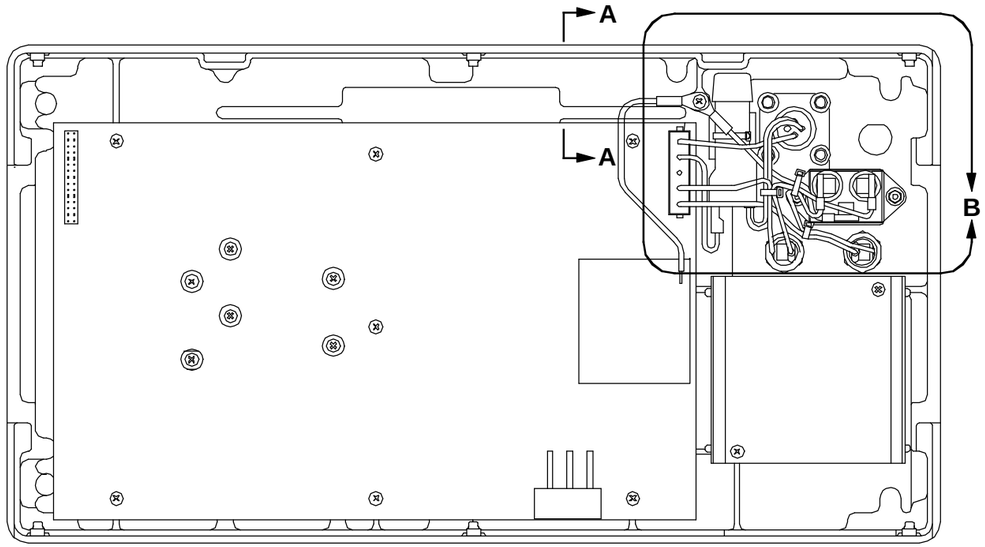
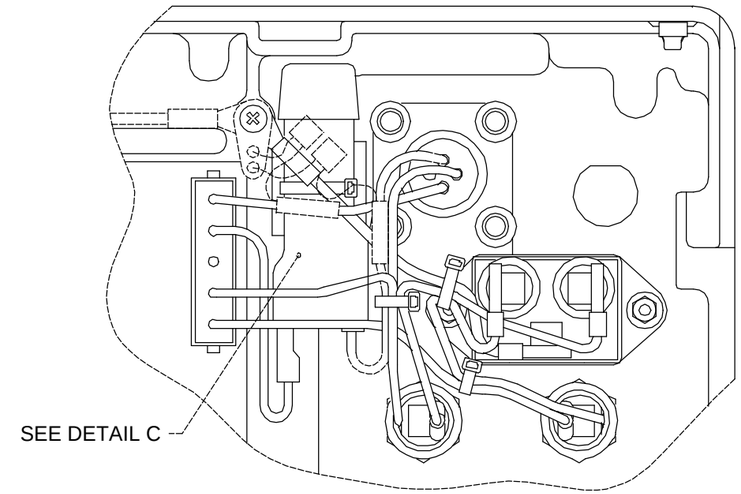
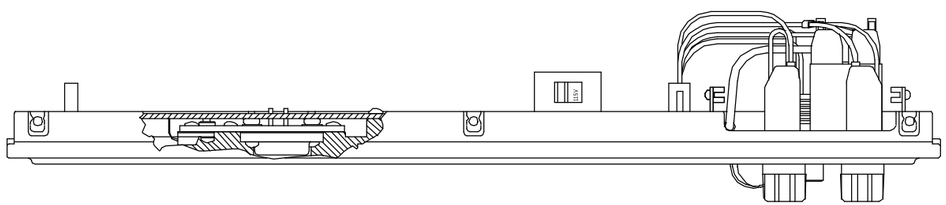
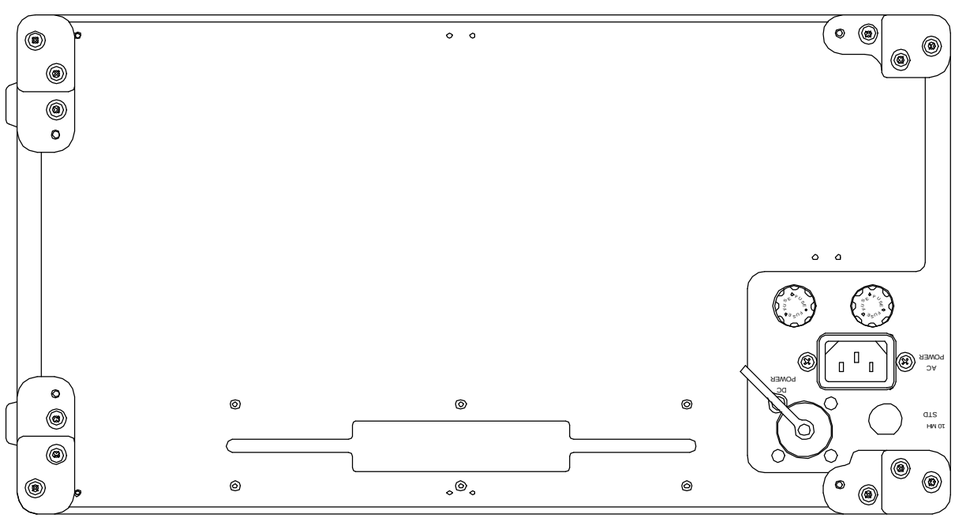


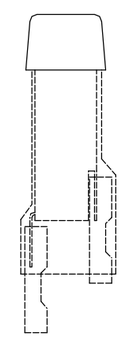
Fig. 16.3 Rear Panel Block Diagram



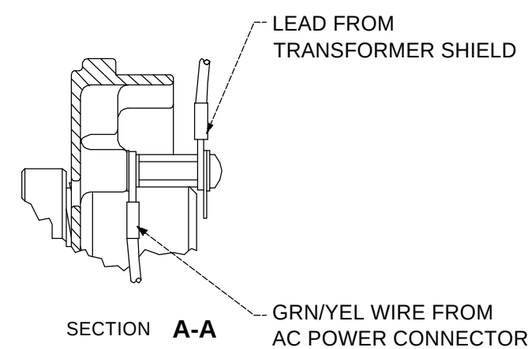








DETAIL C



SECTION **A-A**

REAR PANEL ASSEMBLY

01-P30462C REV. H

SHEET 1 OF 1

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Go to Section 18

17.1 GENERAL DESCRIPTION

The Power Supply Module is designated as A14-Al. It converts an AC or a DC input voltage to the DC voltages required to power the Analyzer,

A 110/220VAC selection switch is accessible through the Analyzer's bottom cover.

17.2 SIGNALS SUMMARY

17.2A Signal Descriptions

17.2A.1 J1 (Back Panel)

DC INPUT + and DC INPUT – are the connections for optionally supplying the Analyzer with a +11 to +18 Vdc source. Max current is 8A.

AC Input, AC Return are the connections for supplying the Analyzer with either 90-132 Vac or 184-264 Vac at 47-440 Hz. Max current is 2.5A rms.

17.2A.2 J2 (Processor/Front Panel)

AC/(DC)* DRIVE CONTROL output to the Processor Module indicates the power supply is operating in either AC or DC mode. This signal is buffered at the Processor Module where it becomes the DC OPERATION signal to drive a front panel LED.

AUX POWER output is a +12Vdc standby voltage routed to the front panel on/off switch.

DC INPUT + output to the Processor Module is the externally applied positive DC voltage from J1.

POWER ON input is the +12Vdc control line from the front panel on/off switch.

+5Vdc, -5Vdc, +12Vdc, -12Vdc, and +40Vdc are the output voltages that supply power to the Analyzer system.

17.2B Connector Descriptions

17.2B.1 J1 (Back Panel)

pin	
1	DC Input - (optional)
2	DC Input + (optional)
3	not used
4	AC Return
5	AC Input

17.2B.2 J2 (Processor Module/Front Panel)

pin	
1	POWER ON (+12VDC In)
2	AC/(DC)* Drive Control
3-5	+5VDC
6,7	-5VDC
8-11	+12VDC
12-14	-12VDC
15	+40VDC
16	AUX POWER (+12VDC Out)
17	DC INPUT + (Battery Voltage)
18	+5VDC
19-21	GND
22	-5VDC
23	+12VDC
24-30	GND

17.3 BLOCK DIAGRAM DESCRIPTION

In AC mode, the power supply is operated as an off-line, half bridge converter for inputs of 90-132Vac rms or 184-264Vac rms at 47 to 440Hz. When connected to an AC power source, the power supply automatically switches to AC operating mode.

In. the DC mode, the power supply operates as a push-pull converter for inputs of +11 to +18Vdc.

The power supply contains protection circuitry for:

a) Shorts on the power supply output lines
b) Transients on the input lines
c) Input overvoltage protection when the 115/230 voltage selection switch is in the 115 position
d) Output overvoltage protection on the +5V output
e) Thermal overload of Line Transformer T1.

115 VAC	***230 VAC***	***Battery***
90-132VAC	184-264VAC	+11 to + 18 VDC
47-440 Hz	47-440 HZ	

Figure 17.3 Prime Power Inputs

17.4 DETAILED DESCRIPTION

17.4.1 Line Transformer/Housekeeping Supply

The line transformer (T1) has two primary windings and a single, center-tapped secondary. The two primary windings are connected in series. Switch S1 connects the AC input across both windings (in 220 mode) or one winding (in 110 mode), maintaining the same volts per turn on the Primary This provides the same voltage on the secondary winding for 110 and 220 Vac input operation. The secondary output is full wave rectified and filtered by C13 and is used as the power source for two voltage regulators (U3 and U7). The regulators are set at +12 volts.

U3 provides a housekeeping supply for the power supply unit. The housekeeping supply is output to the AUX POWER line. AUX POWER is connected to the front panel on/off switch along with return line POWER ON. When the switch is in the ON position, the AUX POWER voltage is returned on the POWER ON line.

The return line is then used to power the pulse width modulator U1 and driver U2. When the power switch is in the OFF position, the input bridge rectifier and housekeeping supply are still active but the output drivers are turned off. U7 provides an "AC Present" supply used for AC/DC switch-over.

AUX POWER output c6ntrol line
Voltage: +11VDC ±5%
Load Current Max: 100mA

POWER ON input control line
Voltage: +11VDC ±5%
Load Current Max: 100mA

17.4.2 AC/DC Switchover

When there is an AC input source, line transformer (T1) is active and diode D2 is turned on. The "AC Present" regulator (U7) output energizes relay K1 and disconnects the DC CENTER TAP drive When there is no AC input source, the relay de-energizes and switches the DC input to the chopping transformer.

The "AC Present" regulator output is also used as a logic control signal to enable the correct pair of drivers in U2 for the AC or DC switching transistors. Q2 acts as an inverter such that when AC is present, U2 pins 11 and 13 are enabled while U2 pins 10 and 12 are disabled. The (AC/DC)* drive control output (J2 pin 2) is controlled by Q1 which uses the power supply +5V output for its supply so that no voltage is present on the line if the power supply is not on.

17.4.3 Latch, Pulse Width Modulator (PWM)

Pulse Width Modulator IC U1 uses the +12V output as a reference. The PWM controls the duty cycle of the two 50KHz complimentary outputs depending on the error signal. The +12V is used as the reference since several modules require ±1% on the +12V. It can be adjusted using R40.

U1 uses the timing capacitor C2 to soft-start the power supply. When the on/off switch is on, the reset circuitry (R37, C21, D8) holds the output of latch U6 low (inactive) while U1, U5, and U6 are powering up. This holdoff ends prior to the soft-start of the PWM. If an overcurrent or overvoltage (+5V) condition occurs, the output of U6 is latched high to shut down the power supply until it is reset.

17.4.4 Chopping Transformer

The chopping transformer T3 has two primary windings. (one for AC, and one for DC operation) and a multiple output secondary which provides +5V, -5V, +12V, -12V, and +40V.

17.4.4.1 During AC Operation

The half bridge switching transistors (Q5 and Q6) drive the chopping transformer. The transistors alternate pulling the ends of the primary low, while the center tap remains high (push/pull). To ensure that both Q5 and Q6 are off, dead time between these two transistors is maintained. Without dead time, there would be a short circuit across the primary winding.

The primary current is monitored by the current sensing transformer T4. The ratio for the current sensing transformer is 100 to 1, and the secondary is loaded with 221 ohms. This produces a secondary output of 2VA of primary current in the chopping transformer. If the primary current in the chopping transformer rises above 1.5A (due to an excessive load or a short on the secondaries), the power supply will shut down until the condition is removed.

17.4.4.2 During DC Operation

The push/pull. switching transistors Q7 and Q8 drive the chopping transformer and a DC voltage is applied to the center tap from relay K1. The nominal DC voltage at the DC CENTER TAP is 11.7Vdc for an input of 12.0Vdc. The primary current in DC operation is monitored using R9 and U5.

17.4.5 Outputs

The secondary winding outputs of the chopping transformer are all full wave, center tapped rectified.

Each of the outputs is filtered by an LC lowpass filter. All the output filter inductors are wound on the same core to improve cross regulation.

The output voltages and rated currents are shown in figure 17.4.5. The voltages specified are with the +12V output adjusted to +12.lV±1%.

17.4.6 Overvoltage Protection

The +5V output is monitored by a programmable zener (U4), which is set to conduct when the +5V output reaches +6.2V. Q3 and Q4 are then turned on, pulling “+5V O.V." (+5V OverVoltage) low and setting latch U6 high, thereby shutting down the PWM (U1).

Nominal Output Voltage	Minimum	LOW	Nominal	High	Maximum
+5V ±5%	300mA	320mA	490mA	2.71A	4.8A
-5.2V ±5%	100mA	530mA	800mA	890mA	990mA
+12.1V ±1%	1A	2.51A	3.8A	4.4A	4.8A
- 12.3V ±5%	100mA	380mA	570mA	680mA	740mA
+45V ±1 0%	10mA	40mA	60mA	70mA	75mA
Approx Output Power	16W	40W	60W	80W	98W

Figure 17.4.5 Output Voltages and Load Levels

17.5 BLOCK DIAGRAM

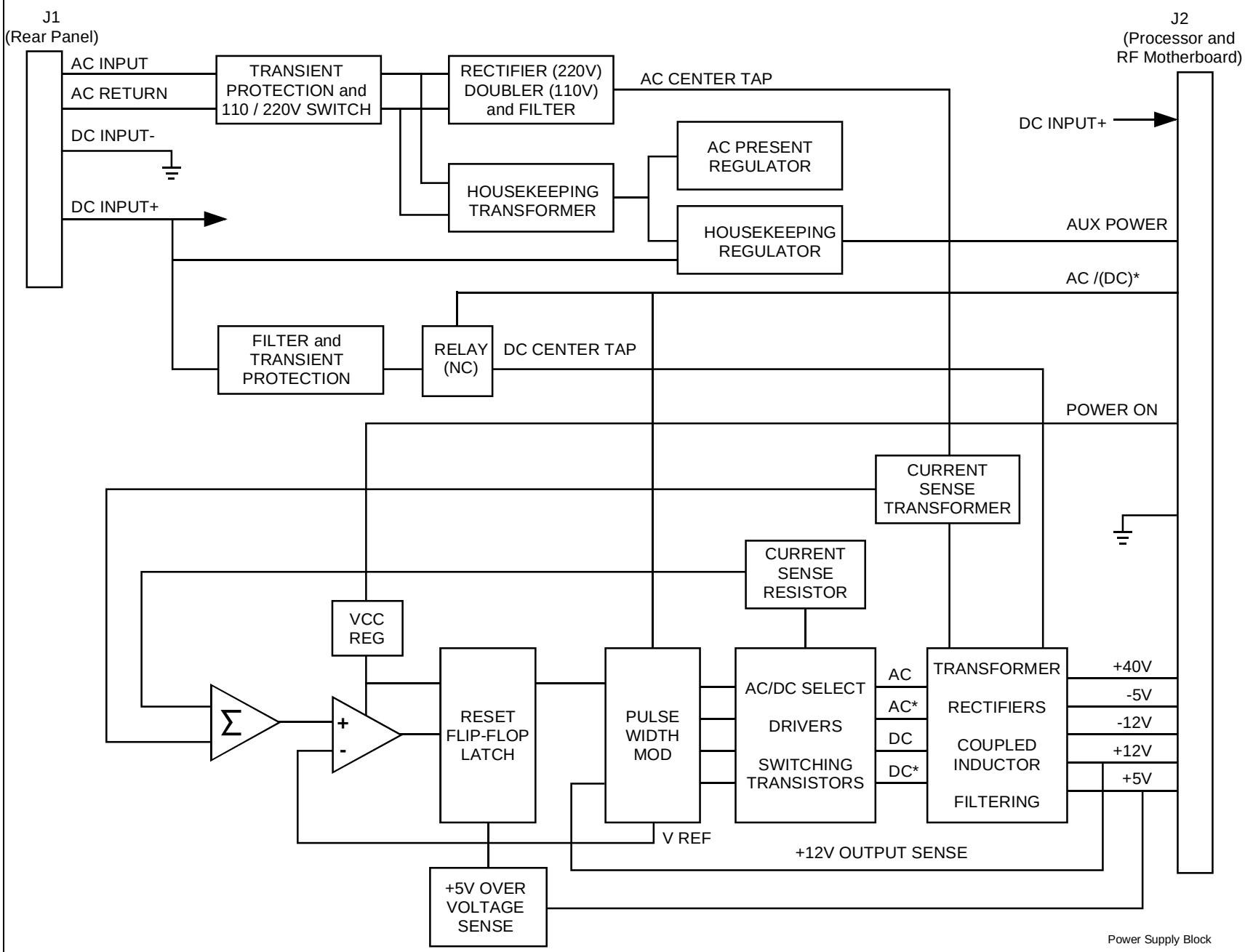
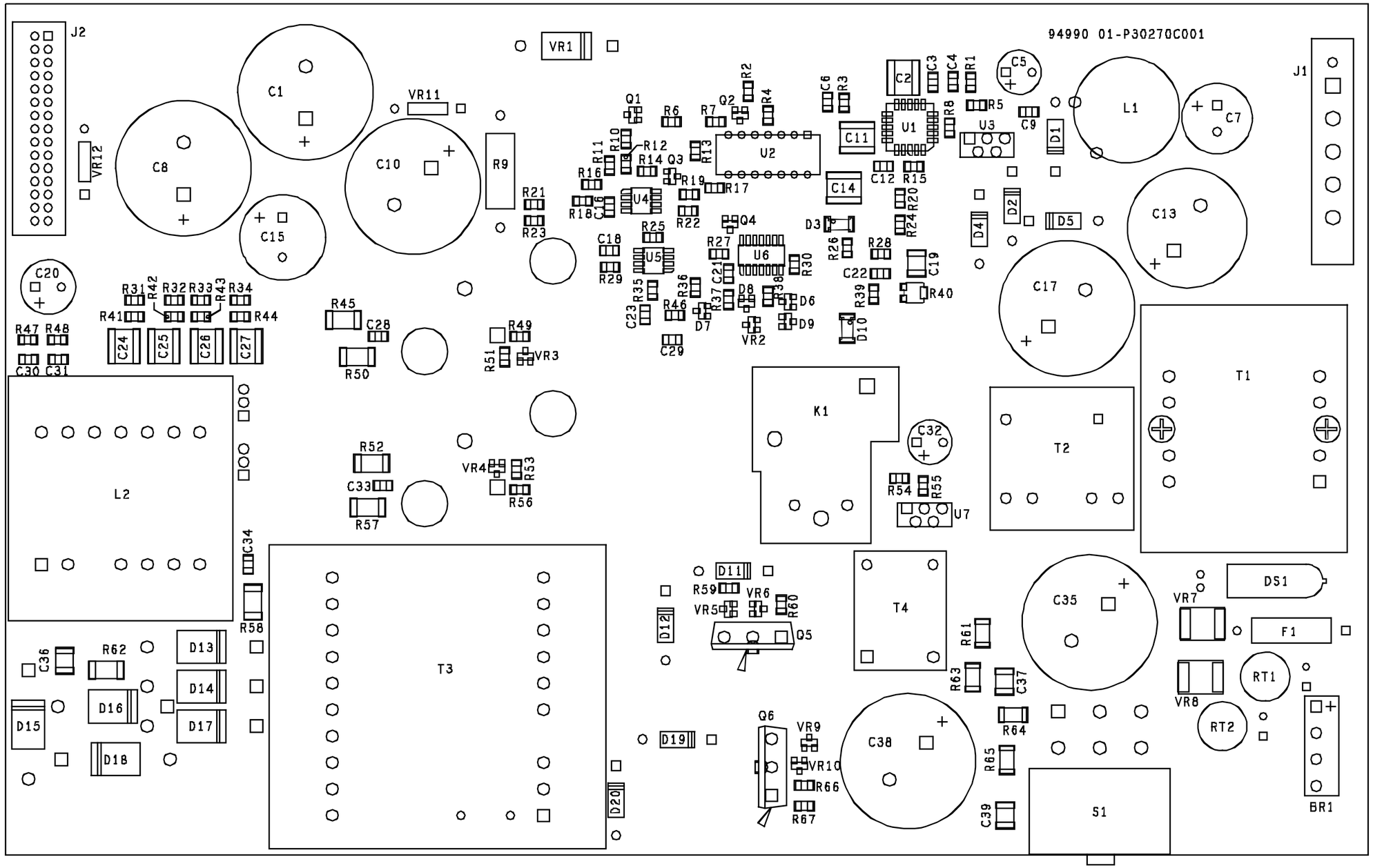


Fig. 17.5 Power Supply Block Diagram



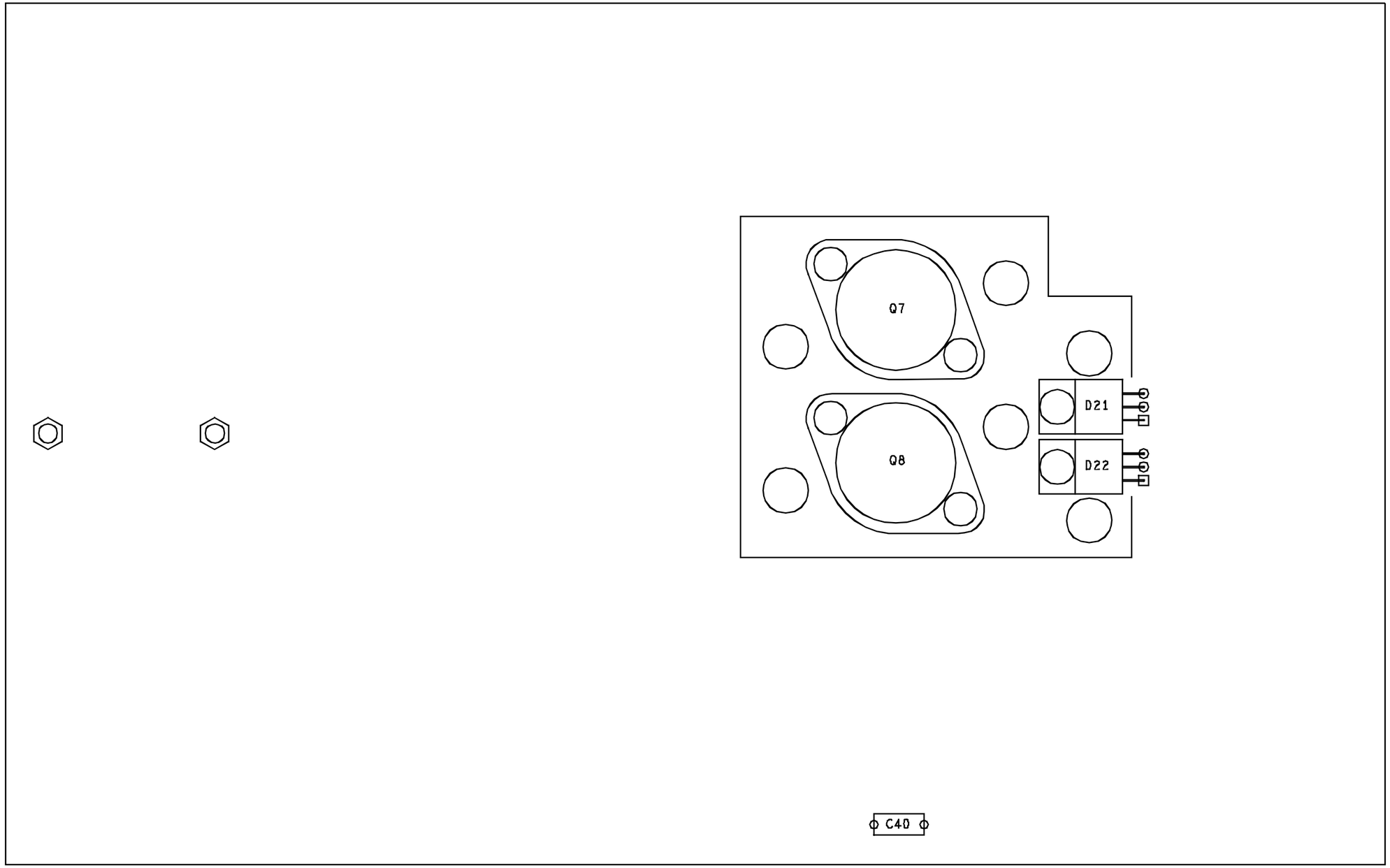
COMPONENT SIDE

CAUTION
THIS ASSEMBLY CONTAINS ITEMS
WHICH ARE SUBJECT TO DAMAGE
FROM ELECTROSTATIC DISCHARGE (ESD)

CIRCUIT CARD ASSEMBLY
POWER SUPPLY

01-P30270C REV. D

SHEET 1 OF 2



SOLDER SIDE

CAUTION
THIS ASSEMBLY CONTAINS ITEMS
WHICH ARE SUBJECT TO DAMAGE
FROM ELECTROSTATIC DISCHARGE (ESD)

CIRCUIT CARD ASSEMBLY
POWER SUPPLY

01-P30270C REV. D

SHEET 2 OF 2

DWG NO 63-P30272C SH 1

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
B	INITIAL REL AND RENUMBERED 3-1-90		
C	SEE MCO B35608 GD 90-06-13	90-07-09	D. DUNCAN
D	SEE CO E36159-3 LRS 95-08-22	95-08-24	KOESTNER

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A14.
2. FOR REFERENCE DRAWINGS REFER TO:
   01-P30270C ASSEMBLY
   12-P30273C TEST PROCEDURE
3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL INDUCTANCE VALUES ARE IN UH.
   ALL VOLTAGES ARE IN DC.
4. TERMINATIONS CODED WITH THE SAME LETTERS OR NUMBERS ARE ELECTRICALLY CONNECTED.

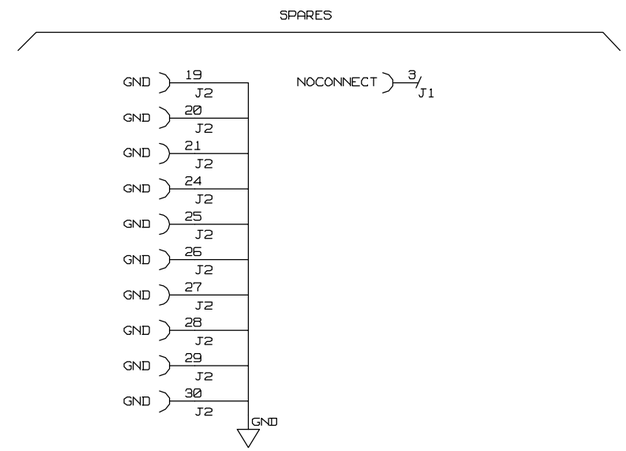
5 DEVICE TYPE NUMBERS AND CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE 1. PORTIONS OF THE TYPE NUMBER MAY BE UNDERLINED AND USED AS A CODE TO IDENTIFY DEVICES ON DIAGRAM.

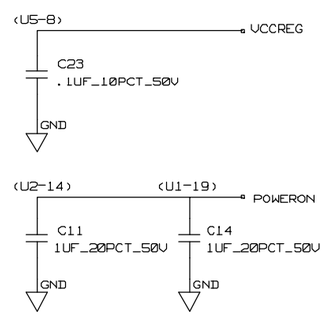
6 DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH MANUFACTURER. ENGINEERING APPROVED EQUIVALENT DEVICE MAY BE USED.

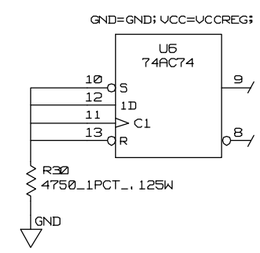
TABLE 1 5

REF DES	DEVICE TYPE 6	+5	GND	NO CONN.	VCCREG	POWER ON	VCU3
U1	UC3825Q		13,15			19	17
U2	D469ADJ		7			14	
U3	LM2931CT		3				
U4	TL431CD						
U5	MC34072D		4		8		
U6	74AC74SC		7		14		
U7	LM2931CT		3				

REFERENCE DESIGNATIONS	
HIGHEST NUMBER USED	NOT USED
BR1	
C40	
D22	
DS1	
F1	
J2	
K1	
L2	
Q8	
RT2	
R67	R62
S1	
T4	
U7	
VR12	







ALL SHEETS ARE THE SAME REVISION STATUS

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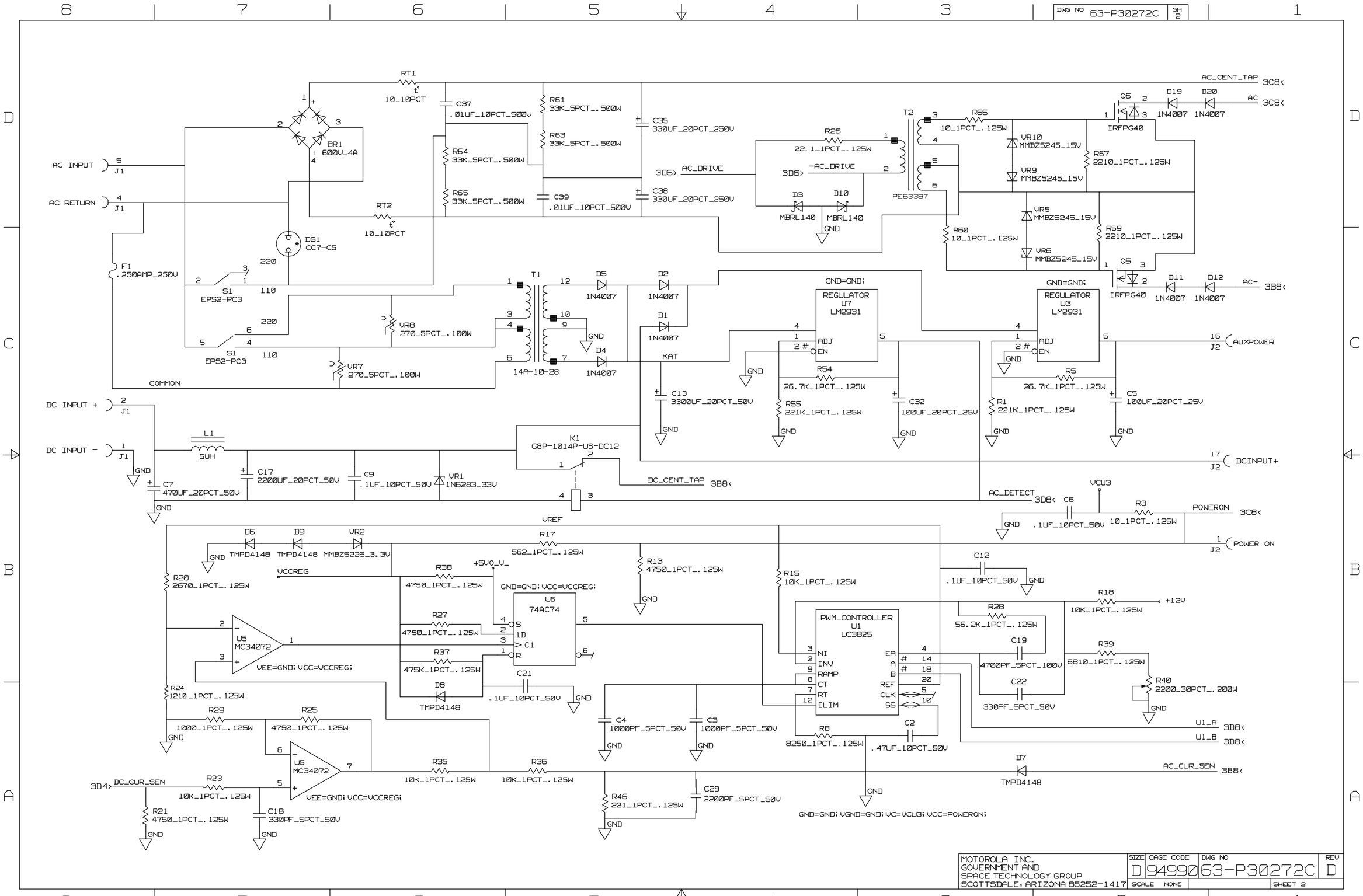
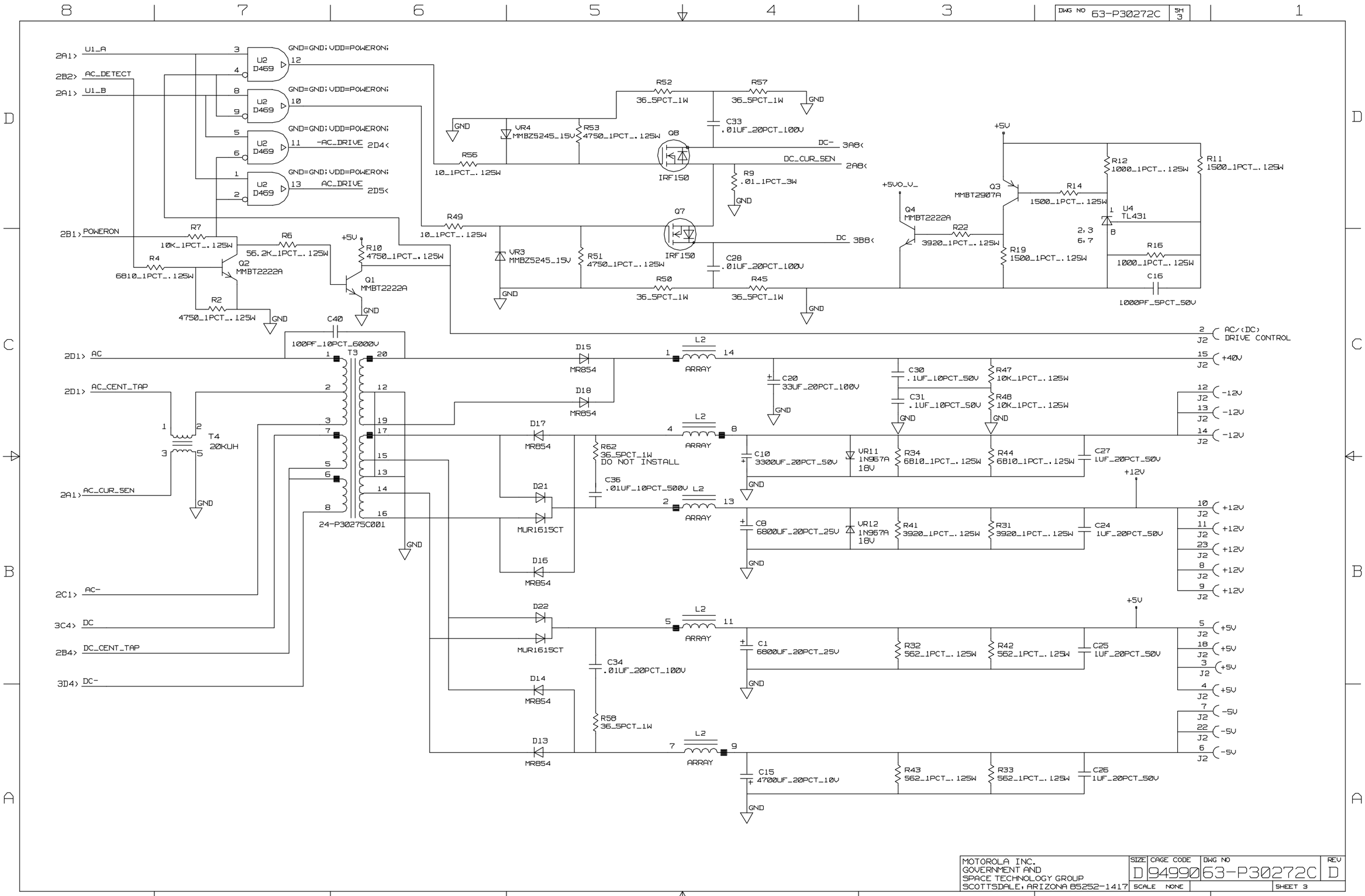
		ISS B33350-53(B)90-04-17	
		APPROVALS	TITLE
		DWN D. GREER 90-02-05	POWER SUPPLY SCHEMATIC DIAGRAM
		CHKR K. NELSON 90-04-12	
		QA	
		MATL	
01-P30272C	COCHISE	MFG J. DECAMP 90-04-12	SIZE D CAGE CODE 94990 DWG NO 63-P30272C
NEXT ASSY	USED ON	ENG D. ZELINKA 90-04-11	
APPLICATION		CUST	SCALE NONE SHEET 1 OF 3



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30272C	REV D
	SCALE NONE		SHEET 2


DWG NO 63-P30272C SH 3
2A1> U1_A
2B2> AC_DETECT
2A1> U1_B
U2 D469
GND=GND; VDD=POWERON;
-AC_DRIVE 2D4<
AC_DRIVE 2D5<
2B1> POWERON
R7 10K_1PCT_.125W
R6 56.2K_1PCT_.125W
R4 6810_1PCT_.125W
Q2 MMBT2222A
R2 4750_1PCT_.125W
+5V
R10 4750_1PCT_.125W
Q1 MMBT2222A
C40 100PF_10PCT_6000V
2D1> AC
2D1> AC_CENT_TAP
T3
T4 20UHK
2A1> AC_CUR_SEN
24-P30275C001
2C1> AC-
3C4> DC
2B4> DC_CENT_TAP
3D4> DC-
D15 MR854
D18 MR854
D17 MR854
D21 MUR1615CT
D16 MR854
D22 MUR1615CT
D14 MR854
D13 MR854
L2 ARRAY
R62 36_5PCT_1W DO NOT INSTALL
C36 .01UF_10PCT_500V
C34 .01UF_20PCT_100V
R58 36_5PCT_1W
C20 33UF_20PCT_100V
C30 .1UF_10PCT_50V
C31 .1UF_10PCT_50V
R47 10K_1PCT_.125W
R48 10K_1PCT_.125W
C10 3300UF_20PCT_50V
VR11 1N967A 18V
R34 6810_1PCT_.125W
R44 6810_1PCT_.125W
C27 1UF_20PCT_50V
C8 6800UF_20PCT_25V
VR12 1N967A 18V
R41 3920_1PCT_.125W
R31 3920_1PCT_.125W
C24 1UF_20PCT_50V
C1 6800UF_20PCT_25V
R32 562_1PCT_.125W
R42 562_1PCT_.125W
C25 1UF_20PCT_50V
C15 4700UF_20PCT_10V
R43 562_1PCT_.125W
R33 562_1PCT_.125W
C26 1UF_20PCT_50V
+12V
AC/(DC) DRIVE CONTROL
+40V
-12V
+12V
+5V
-5V
R52 36_5PCT_1W
R57 36_5PCT_1W
VR4 MMBZ5245_15V
R53 4750_1PCT_.125W
C33 .01UF_20PCT_100V
DC- 3A8<
DC_CUR_SEN 2A8<
Q8 IRF150
R9 .01_1PCT_3W
R56 10_1PCT_.125W
R49 10_1PCT_.125W
VR3 MMBZ5245_15V
R51 4750_1PCT_.125W
Q7 IRF150
DC 3B8<
C28 .01UF_20PCT_100V
R50 36_5PCT_1W
R45 36_5PCT_1W
+5VO_V_
Q4 MMBT2222A
R22 3920_1PCT_.125W
Q3 MMBT2907A
R14 1500_1PCT_.125W
R19 1500_1PCT_.125W
R12 1000_1PCT_.125W
R11 1500_1PCT_.125W
U4 TL431
R16 1000_1PCT_.125W
C16 1000PF_5PCT_50V
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D
CAGE CODE 94990
DWG NO 63-P30272C
REV D
SCALE NONE
SHEET 3

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18.1 GENERAL DESCRIPTION

The RF Motherboard is designated as A3 and is attached to the bottom of the RF Cardcage.

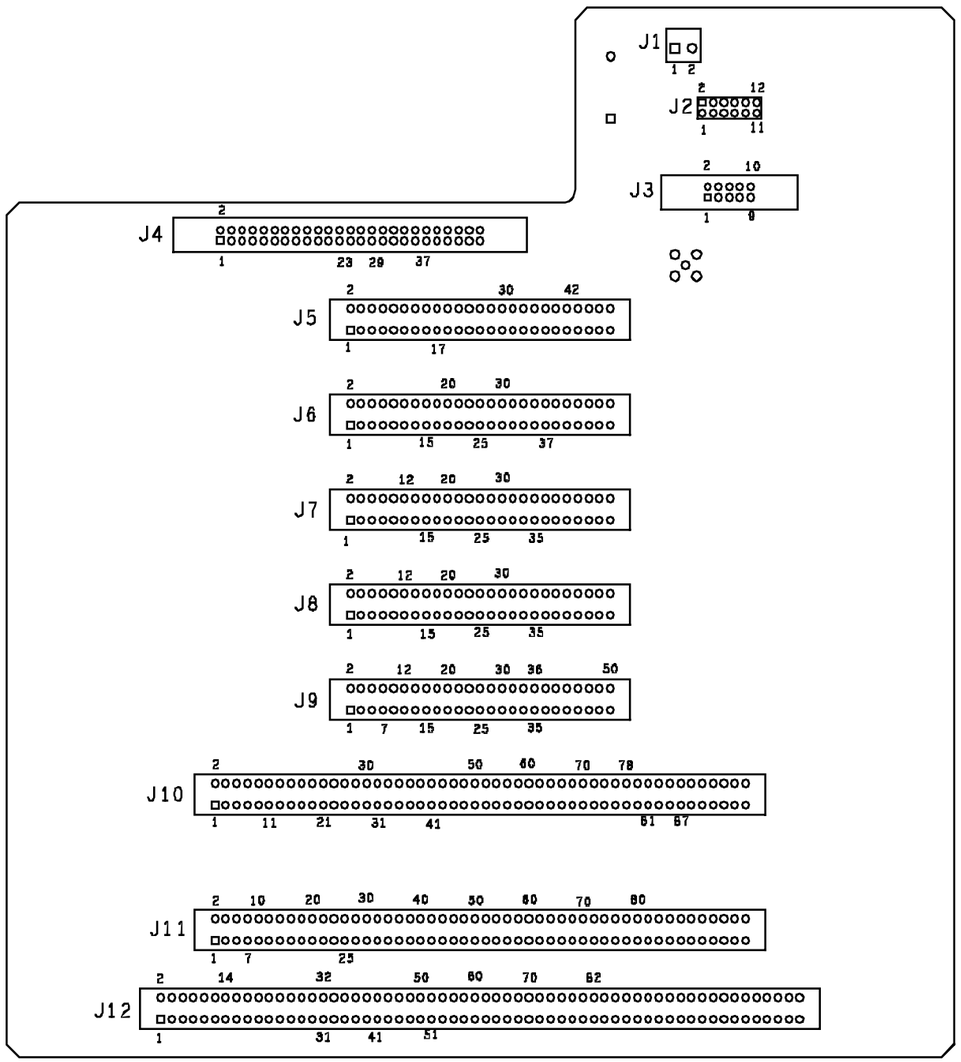
This board provides the interconnections between modules inside the RF Cardcage. It also includes a slot outside the cardcage for interconnection to the Interface Module. The RF Wattmeter (located underneath the LED assembly) is also connected to the RF Motherboard.

Figure 18.1 summarizes the RF Motherboard's connector assignments.

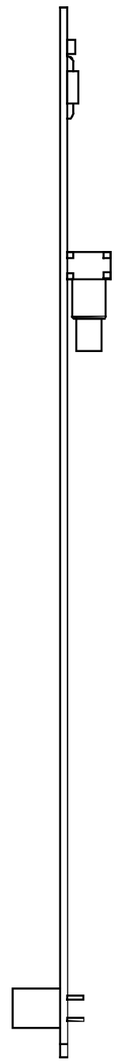
Refer to the interconnect diagram for specific pin/signal assignments.

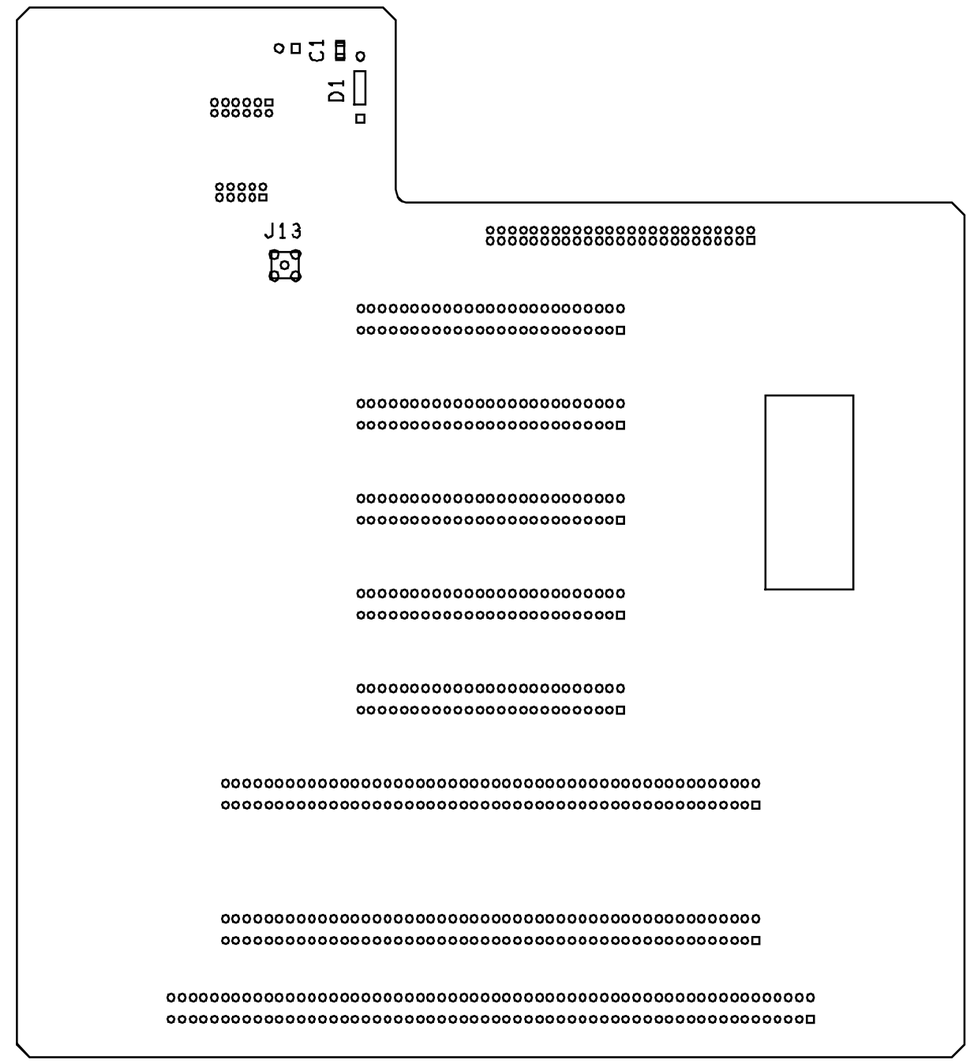
Connector	*Module Name/Designation*	
J1	Fan	
J2	Power Supply	A14A1
J3	Frequency Standard	A13
J4	RF Wattmeter	A2
J5	Generator	A5
J6	RF Output	A6
J7	High Synthesizer	A7
J8	RF Input	A8
J9	Low Synthesizer	A9
J10	Receiver	A10
J11	Spectrum Analyzer	A11
J12	Interface Module	A12
J13	Synth 10 MHz Ref	

Figure 18.1 RF Motherboard Connections



COMPONENT SIDE





SOLDER SIDE

CIRCUIT CARD ASSEMBLY
MOTHER BOARD

01-P30380C REV. B

SHEET 1 OF 1

DWG NO 63-P30383C SH 1

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

REVISION HISTORY

REV	DESCRIPTION	DATE	APPROVED
D	INITIAL RELEASE		

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS PREFIX WITH 1A3.

2 FOR REFERENCE DOCUMENTS REFER TO :

01-P30380C ASSEMBLY

3. ON -001 CONFIGURATION, INSTALL WIRE, FIND NUMBER 5. ON -002 CONFIGURATION, INSTALL D1.

ALL SHEETS ARE THE SAME REVISION STATUS

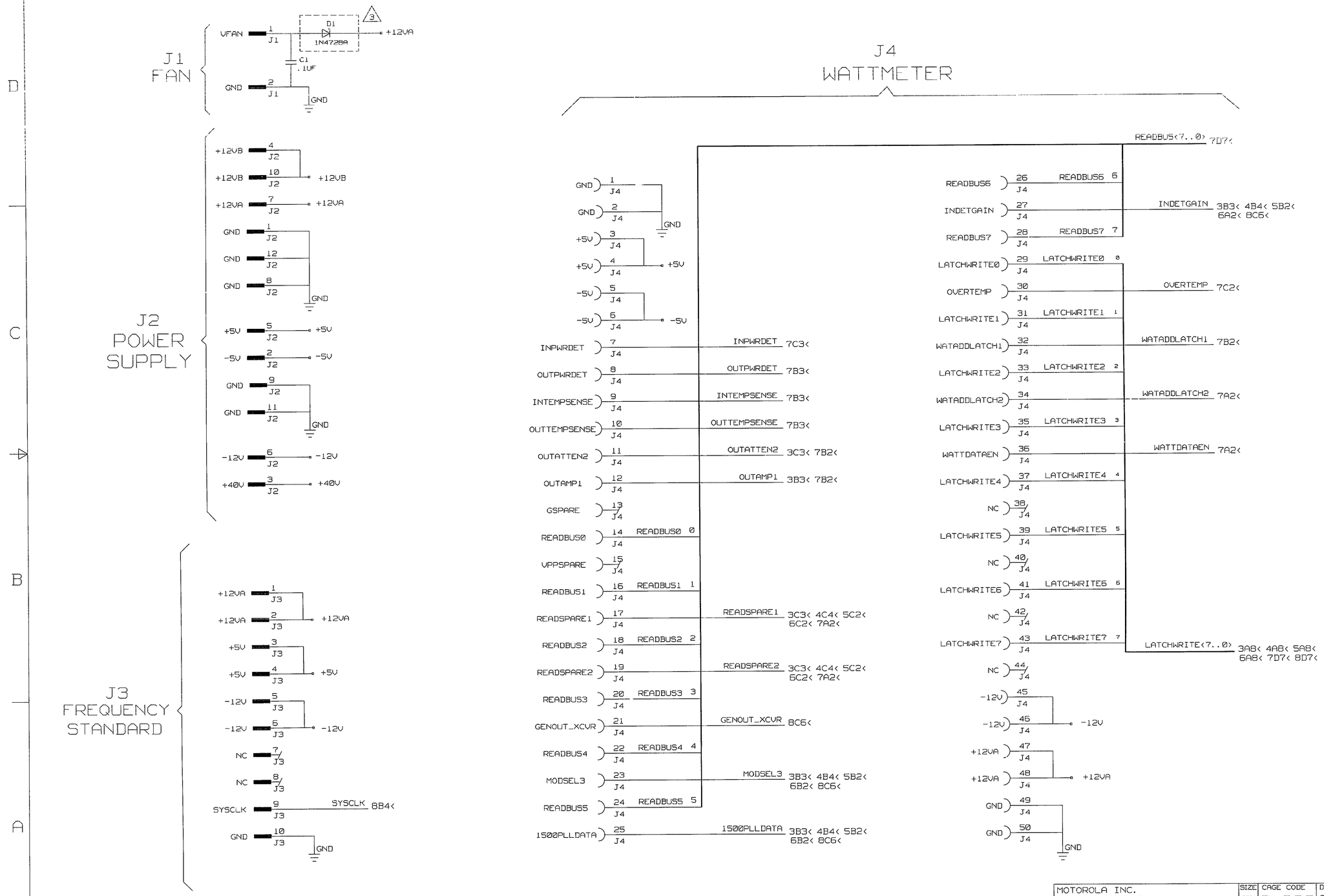
		CONTR	MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417
		ISS B35550-331(D)95-07-06	
		APPROVALS	TITLE
		DWN F. DEPIERRO 95-05-23	SCHEMATIC DIAGRAM
		CHKR	
		QA K. NELSON 95-07-06	MOTHERBOARD
		MATL M. MCDONALD 95-07-06	
01-P30380C	COCHISE	MFG S. CASH 95-7-06	SIZE D / CAGE CODE 94990 / DWG NO 63-P30383C
NEXT ASSY	USED ON	ENG A. KOESNTER 95-07-06	
APPLICATION		CUST	SCALE NONE / SHEET 1 OF 8

ASME Y14.1-1995 DRAWING FORMAT - 3/95

CONCEPT TICKD

DSIZEPAGE1HDEC

C *1103-22-4



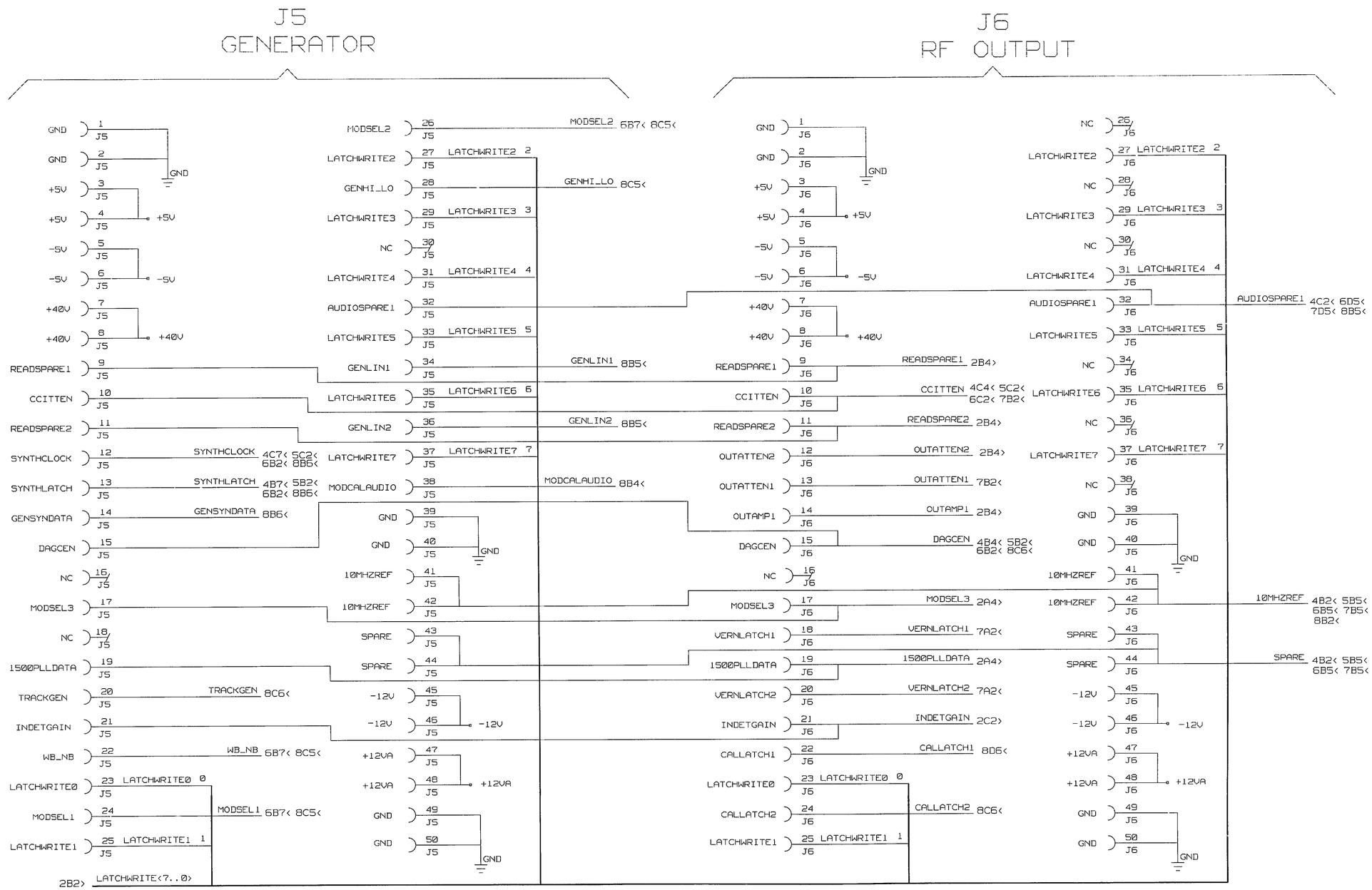
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE	CAGE CODE	DWG NO	REV
	D	94990	63-P30383C	D
	SCALE NONE		SHEET 2	

ASME Y14.1-1995 DRAWING FORMAT - 3/95

CONCEPT

TICKO

DSIZEPAGE2HD2C



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	SCALE NONE		SHEET 3	

ASME Y14.1-1995 DRAWING FORMAT - 3/95

CONCEPT TICKD

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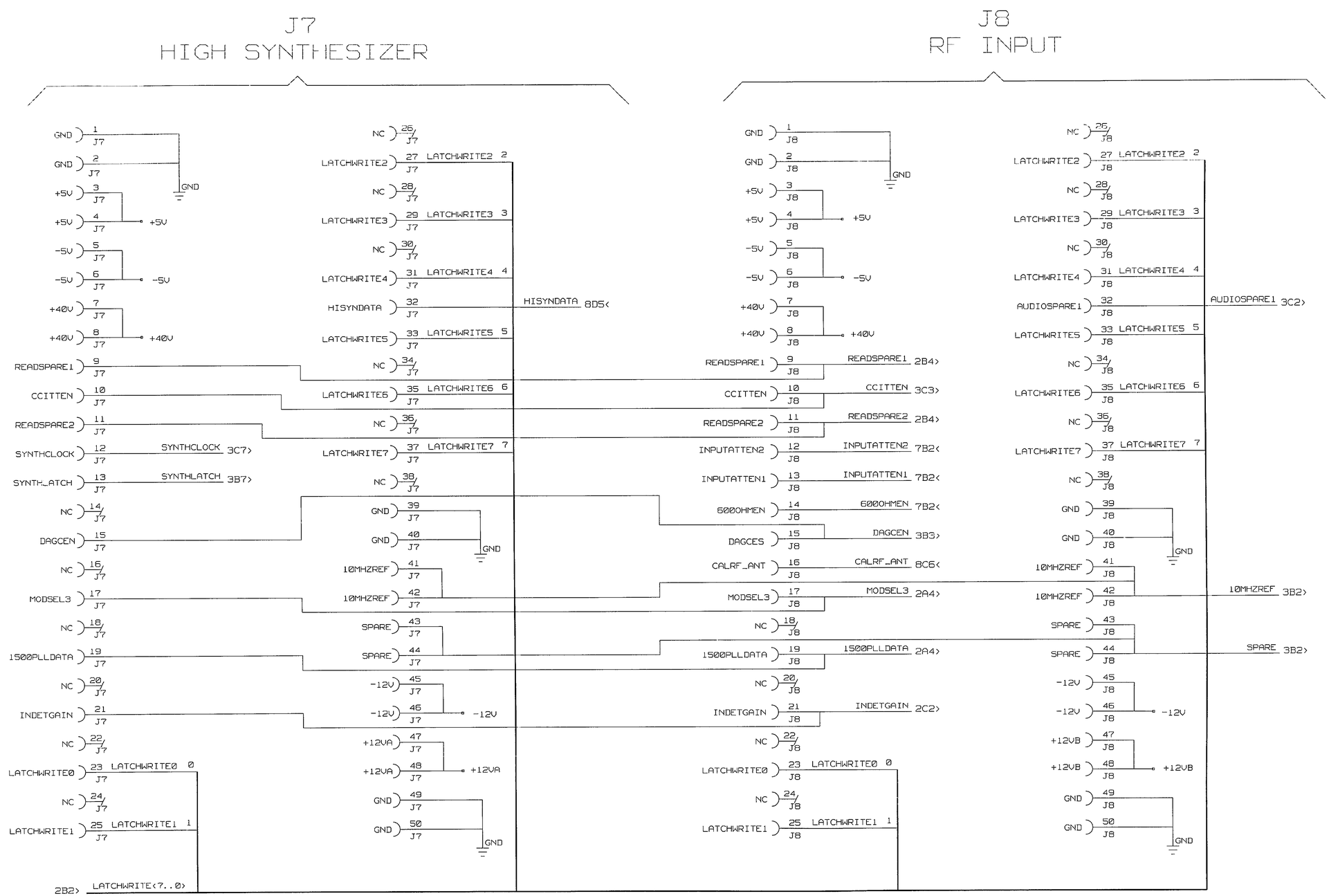
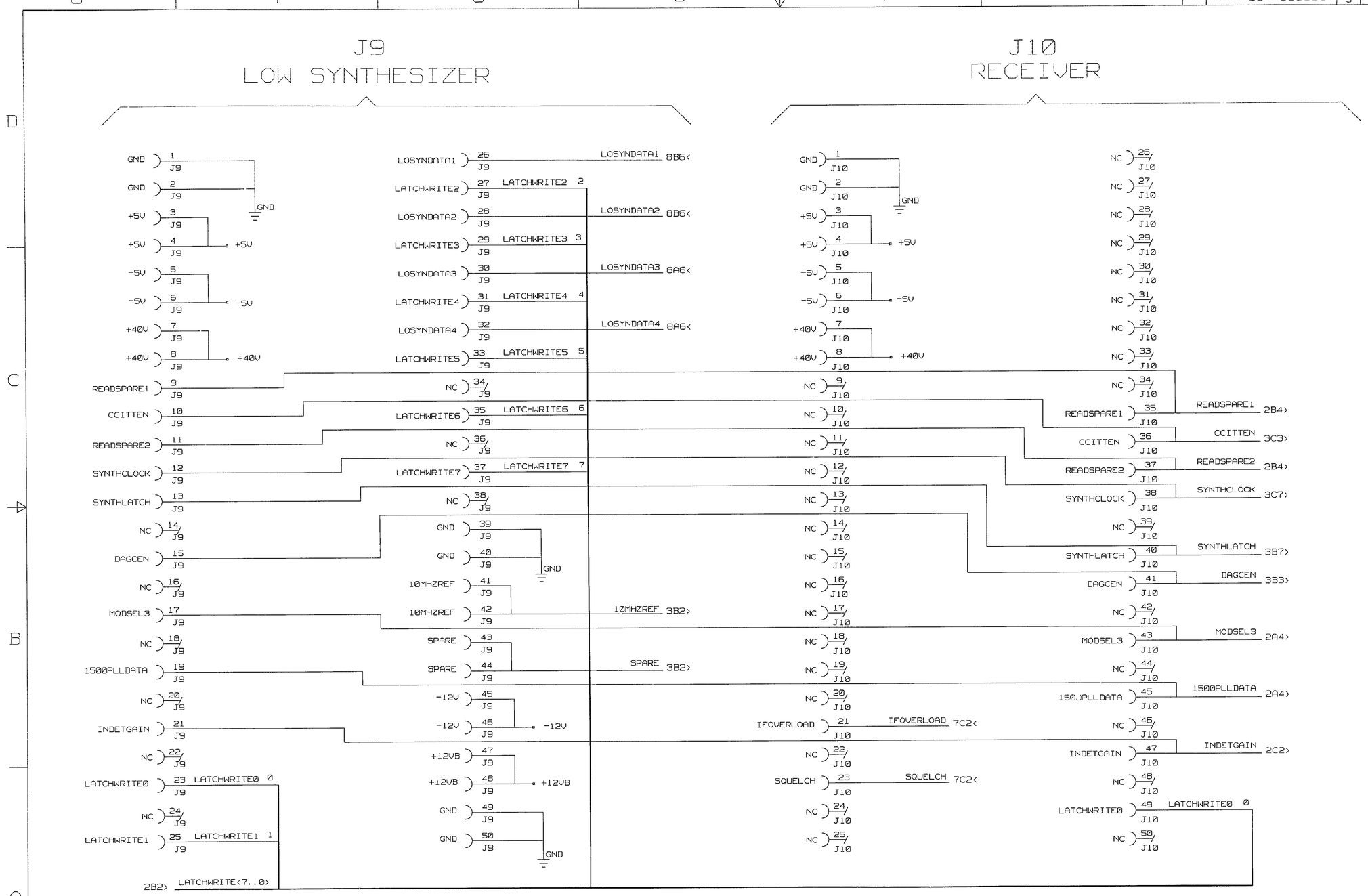


MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30383C	REV D
	SCALE NONE			SHEET 4

ASME Y14.1-1995 DRAWING FORMAT - 3/95

CONCEPT TICKD

DSIZEPAGE2HD2C

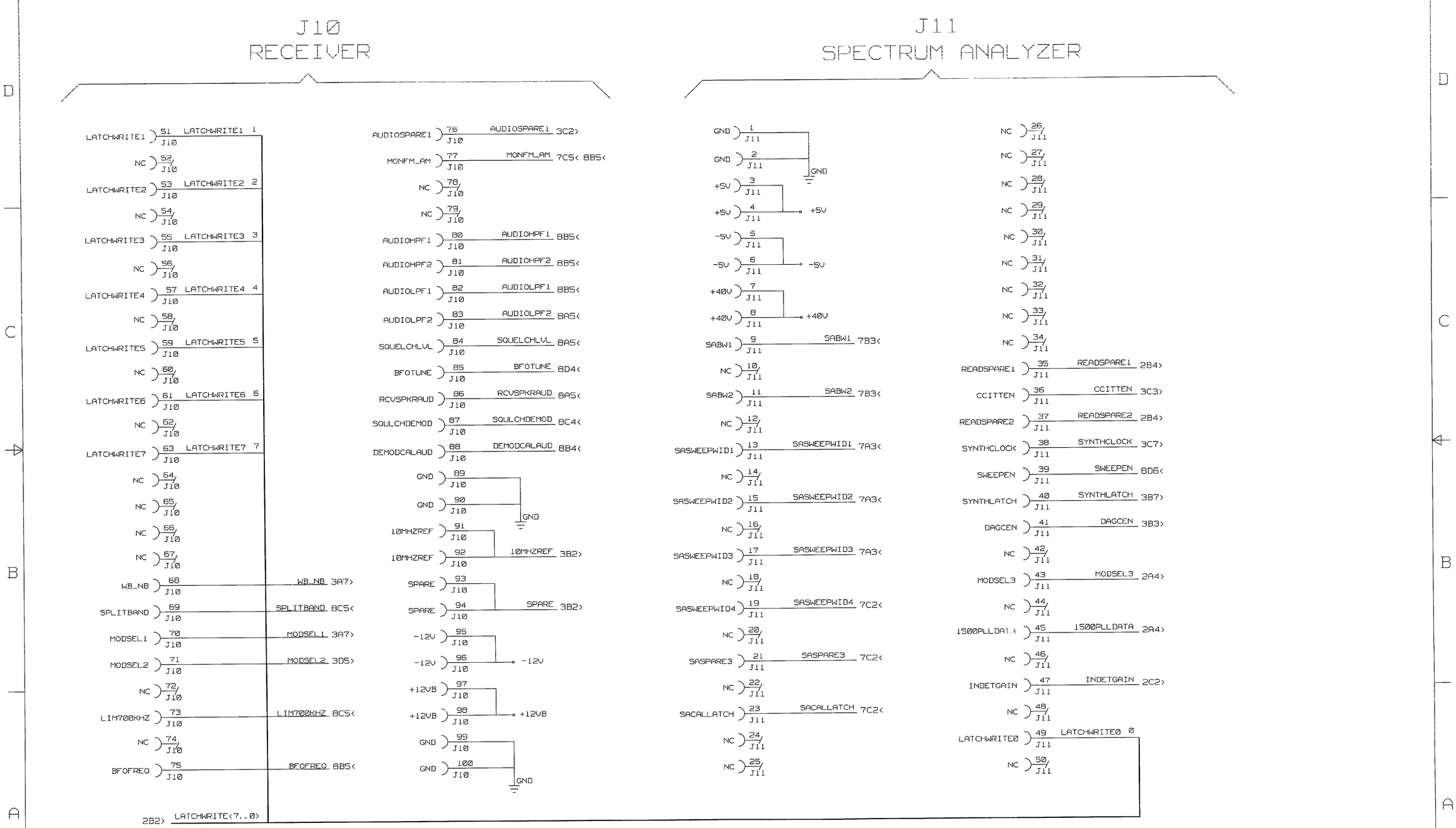


MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30383C	REV D
	SCALE NONE		SHEET 5	

ASME Y14.1-1995 DRAWING FORMAT - 3/95

CONCEPT TICKD

DSIZEPAGE2HD2C



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30383C	REV D
	SCALE NONE		SHEET 6	

J11 SPECTRUM ANALYZER

2D2> READBUS<7..0>
2B2> LATCHWRITE<7..0>

Signal	Pin	Net	Destination
LATCHWRITE1	51	LATCHWRITE1 1	
NC	52		
LATCHWRITE2	53	LATCHWRITE2 2	
NC	54		
LATCHWRITE3	55	LATCHWRITE3 3	
NC	56		
LATCHWRITE4	57	LATCHWRITE4 4	
NC	58		
LATCHWRITE5	59	LATCHWRITE5 5	
NC	60		
LATCHWRITE6	61	LATCHWRITE6 6	
NC	62		
LATCHWRITE7	63	LATCHWRITE7 7	
NC	64		
PHASEDEMODEN	65	PHASEDEMODEN	8C5<
SASPARE2	66	SASPARE2	8C5<
SASYNTHDATA	67	SASYNTHDATA	8C5<
NC	68		
NC	69		
NC	70		
NC	71		
NC	72		
NC	73		
SCANLOKFREQ	74	SCANLOKFREQ	8B5<
NC	75		
AUDIOSPARE1	76	AUDIOSPARE1	3C2>
MONFM_AM	77	MONFM_AM	6D5>
NC	78		
SATEMPSENSE	79	SATEMPSENSE	8A5<
NC	80		
NC	81		
SWEEP	82	SWEEP	8C4<
NC	83		
NC	84		
SIGSTRENGTH	85	SIGSTRENGTH	8C4<
NC	86		
NC	87		
SADVMSPARE	88	SADVMSPARE	8C4<
GND	89	GND	
GND	90	GND	
10MHZREF	91		
10MHZREF	92	10MHZREF	3B2>
SPARE	93		
SPARE	94	SPARE	3B2>
-12V	95		
-12V	96	-12V	
+12VB	97		
+12VB	98	+12VB	
GND	99	GND	
GND	100	GND	

J12 INTERFACE

Signal	Pin	Net	Destination
GND	1	GND	
GND	2	GND	
+5V	3		
+5V	4	+5V	
-5V	5		
-5V	6	-5V	
+40V	7		
+40V	8	+40V	
INPWRDET	9	INPWRDET	2C4>
OUTPWRDET	10	OUTPWRDET	2C4>
INTEMPSENSE	11	INTEMPSENSE	2C4>
OUTTEMPSENSE	12	OUTTEMPSENSE	2C4>
NC	13		
NC	14		
SABW1	15	SABW1	6C4>
READBUS0	16	READBUS0 0	
SABW2	17	SABW2	6C4>
READBUS1	18	READBUS1 1	
SASWEEPWID1	19	SASWEEPWID1	6B4>
READBUS2	20	READBUS2 2	
SASWEEPWID2	21	SASWEEPWID2	6B4>
READBUS3	22	READBUS3 3	
SASWEEPWID3	23	SASWEEPWID3	6B4>
READBUS4	24	READBUS4 4	
SASWEEPWID4	25	SASWEEPWID4	6B4>
READBUS5	26	READBUS5 5	
SASPARE3	27	SASPARE3	6B4>
READBUS6	28	READBUS6 6	
SACALLATCH	29	SACALLATCH	6A4>
READBUS7	30	READBUS7 7	
IFOVERLOAD	31	IFOVERLOAD	5B4>
OVERTEMP	32	OVERTEMP	2C2>
SQUELCH	33	SQUELCH	5A4>
OUTATTEN1	34	OUTATTEN1	3B3>
OUTATTEN2	35	OUTATTEN2	2B4>
OUTAMP1	36	OUTAMP1	2B4>
C_MSGEN	37		
INPUTATTEN1	38	INPUTATTEN1	4B4>
INPUTATTEN2	39	INPUTATTEN2	4C4>
600OHMEN	40	600OHMEN	4B4>
CCITTEN	41	CCITTEN	3C3>
WATADDLATCH1	42	WATADDLATCH1	2C2>
WATADDLATCH2	43	WATADDLATCH2	2C2>
WATTDATAEN	44	WATTDATAEN	2B2>
READSPARE1	45	READSPARE1	2B4>
VERNLATCH1	46	VERNLATCH1	3B3>
READSPARE2	47	READSPARE2	2B4>
VERNLATCH2	48	VERNLATCH2	3B3>

J12 INTERFACE

2B2> LATCHWRITE<7..0>

SWEEPEN	49 J12		SWEEPEN 6B2>	LATCHWRITE7	73 J12	LATCHWRITE7 7	NC	97 J12	
CALLATCH1	50 J12		CALLATCH1 3A3>	HISYNDATA	74 J12	HISYNDATA 4C5>	BFOTUNE	98 J12	BFOTUNE 6C5>
DAGCEN	51 J12		DAGCEN 3B3>	PHASEDEMODEN	75 J12	PHASEDEMODEN 7B7>	SWEEP	99 J12	SWEEP 7C5>
CALLATCH2	52 J12		CALLATCH2 3A3>	SASPARE2	76 J12	SASPARE2 7B7>	NC	100 J12	
MODSEL3	53 J12		MODSEL3 2A4>	SASYNTHDATA	77 J12	SASYNTHDATA 7B7>	NC	101 J12	
GENOUT_XCVR	54 J12		GENOUT_XCVR 2A4>	WB_NB	78 J12	WB_NB 3A7>	SIGSTRENGTH	102 J12	SIGSTRENGTH 7C5>
1500PLLDATA	55 J12		1500PLLDATA 2A4>	SPLITBAND	79 J12	SPLITBAND 6B7>	NC	103 J12	
CALRF_ANT	56 J12		CALRF_ANT 4B4>	MODSEL1	80 J12	MODSEL1 3A7>	NC	104 J12	
INDETGAIN	57 J12		INDETGAIN 2C2>	MODSEL2	81 J12	MODSEL2 3D5>	SADVMSPARE	105 J12	SADVMSPARE 7B5>
TRACKGEN	58 J12		TRACKGEN 3B7>	GENHI_LO	82 J12	GENHI_LO 3D5>	NC	106 J12	
LATCHWRITE0	59 J12	LATCHWRITE0 0		LIM700KHZ	83 J12	LIM700KHZ 6A7>	SQULCHDEMOD	107 J12	SQULCHDEMOD 6C5>
SYNTHCLOCK	60 J12		SYNTHCLOCK 3C7>	SCANLOKFREQ	84 J12	SCANLOKFREQ 7A7>	DEMODCALAUD	108 J12	DEMODCALAUD 6B5>
LATCHWRITE1	61 J12	LATCHWRITE1 1		BFOFREQ	85 J12	BFOFREQ 6A7>	NC	109 J12	
SYNTHLATCH	62 J12		SYNTHLATCH 3B7>	AUDIOSPARE1	86 J12	AUDIOSPARE1 3C2>	NC	110 J12	
LATCHWRITE2	63 J12	LATCHWRITE2 2		MONFM_AM	87 J12	MONFM_AM 6D5>	MODCALAUDIO	111 J12	MODCALAUDIO 3B5>
GENSYNDATA	64 J12		GENSYNDATA 3B7>	GENLIN1	88 J12	GENLIN1 3C5>	NC	112 J12	
LATCHWRITE3	65 J12	LATCHWRITE3 3		GENLIN2	89 J12	GENLIN2 3C5>	NC	113 J12	
LOSYNDATA1	66 J12		LOSYNDATA1 5D5>	AUDIOHPF1	90 J12	AUDIOHPF1 6C5>	SYSCLK	114 J12	SYSCLK 2A6>
LATCHWRITE4	67 J12	LATCHWRITE4 4		AUDIOHPF2	91 J12	AUDIOHPF2 6C5>	-12V	115 J12	
LOSYNDATA2	68 J12		LOSYNDATA2 5D5>	AUDIOLPF1	92 J12	AUDIOLPF1 6C5>	-12V	116 J12	-12V
LATCHWRITE5	69 J12	LATCHWRITE5 5		AUDIOLPF2	93 J12	AUDIOLPF2 6C5>	+12VB	117 J12	
LOSYNDATA3	70 J12		LOSYNDATA3 5C5>	SQUELCHLVL	94 J12	SQUELCHLVL 6C5>	+12VB	118 J12	+12VB
LATCHWRITE6	71 J12	LATCHWRITE6 6		RCVSPKRAUD	95 J12	RCVSPKRAUD 6C5>	GND	119 J12	
LOSYNDATA4	72 J12		LOSYNDATA4 5C5>	SATEMPSENSE	96 J12	SATEMPSENSE 7C5>	GND	120 J12	GND

J13

10MHZREF	1 J13	10MHZREF 3B2>
GND	2 J13	
GND	3 J13	
GND	4 J13	
GND	5 J13	GND

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19.1 GENERAL DESCRIPTION

The Base Unit Chassis Assembly includes all other modules/subassemblies in the Analyzer, including associated hardware, brackets, screws, nuts/bolts, etc. not covered in other sections of this manual.

19.2 LIQUID CRYSTAL DISPLAY (LCD)

The LCD Module Assembly provides a visual interface to the operator of the Analyzer system. It is controlled via the Display Processor Module located opposite the LCD Module.

The LCD resolution is 640 horizontal by 480 vertical pixels. The Display Processor Module provides the timing signals along with digital RGB color and intensity data required to operate the display. A CCFL (Cold Cathode Fluorescent Lamp) backlight within the LCD is powered by either an internal or external DC to AC inverter.

To extend CCFL life, a blanking function has been incorporated. If the user has not selected any front panel keys or turned the optical tuning knob for approximately 30 minutes, the LCD will be blanked under processor control. The LCD will remain blanked until the user selects any front panel key or turns the optical tuning knob. This key press or the first optical tuning knob interrupt will cause the LCD display to be restored to its configuration just prior to blanking, but for all other purposes will be ignored.

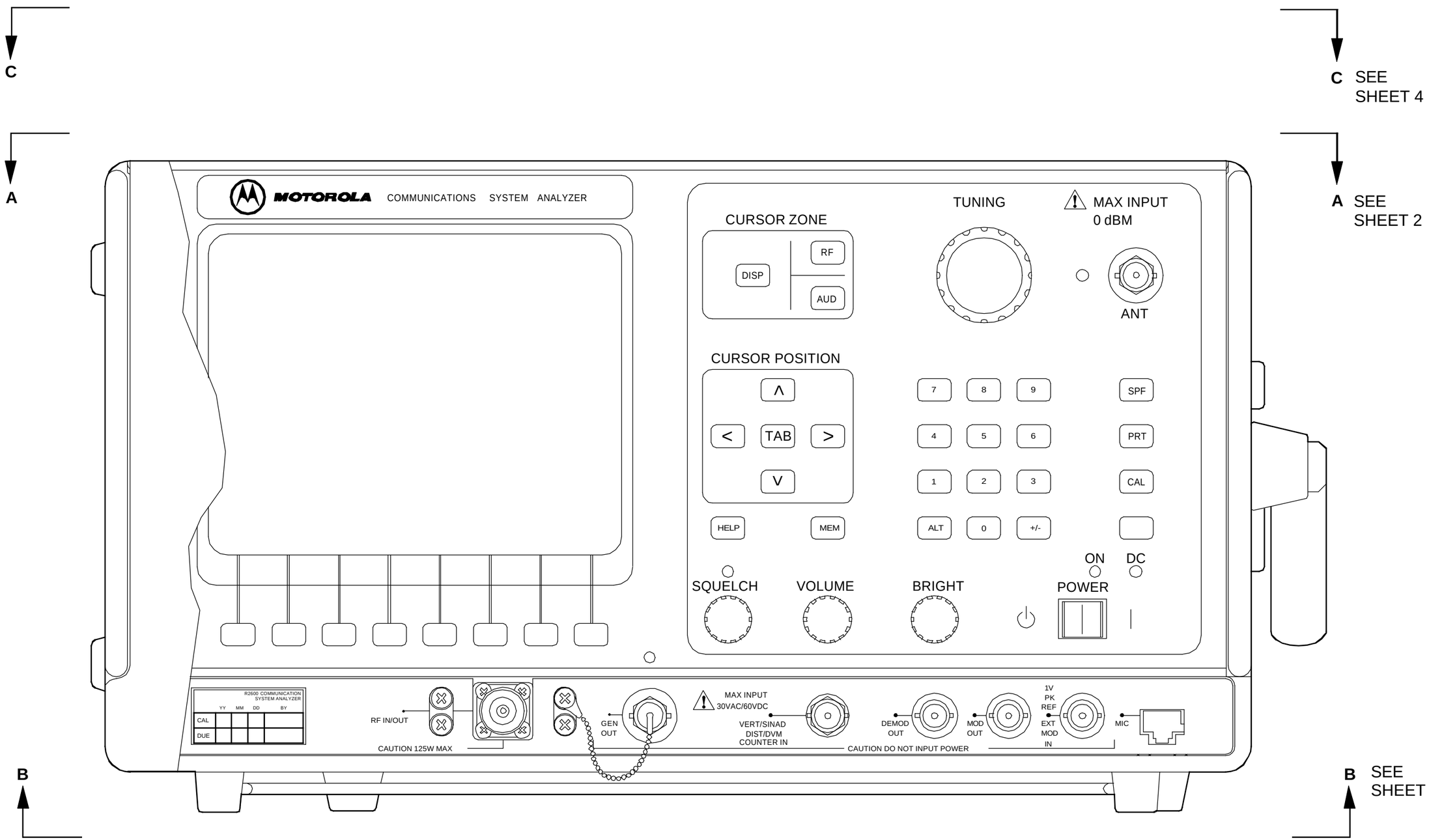
NOTE

LCD repair is limited to replacement of the entire unit assembly.

19.2.1 LCD Brightness Control

BRT, BRT ARM, and BRT LO (See Front Panel Section) are connections for the external brightness potentiometer. The Processor Module only serves as the connection between J3 (front panel) and J6 (Display Processor Board)) and does not process these signals in any way.

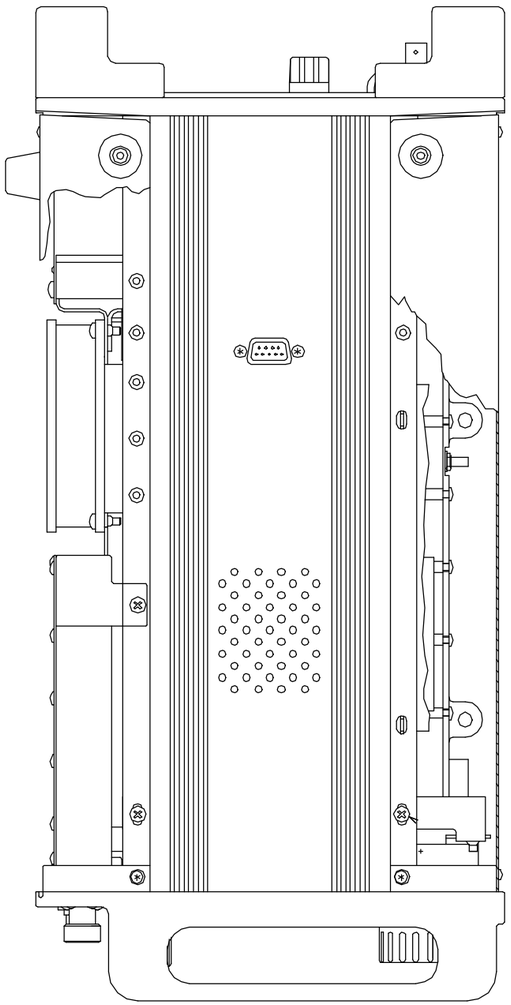
The signals are passed to the backlight inverter, which regulates CCFL current per the brightness potentiometer settings.

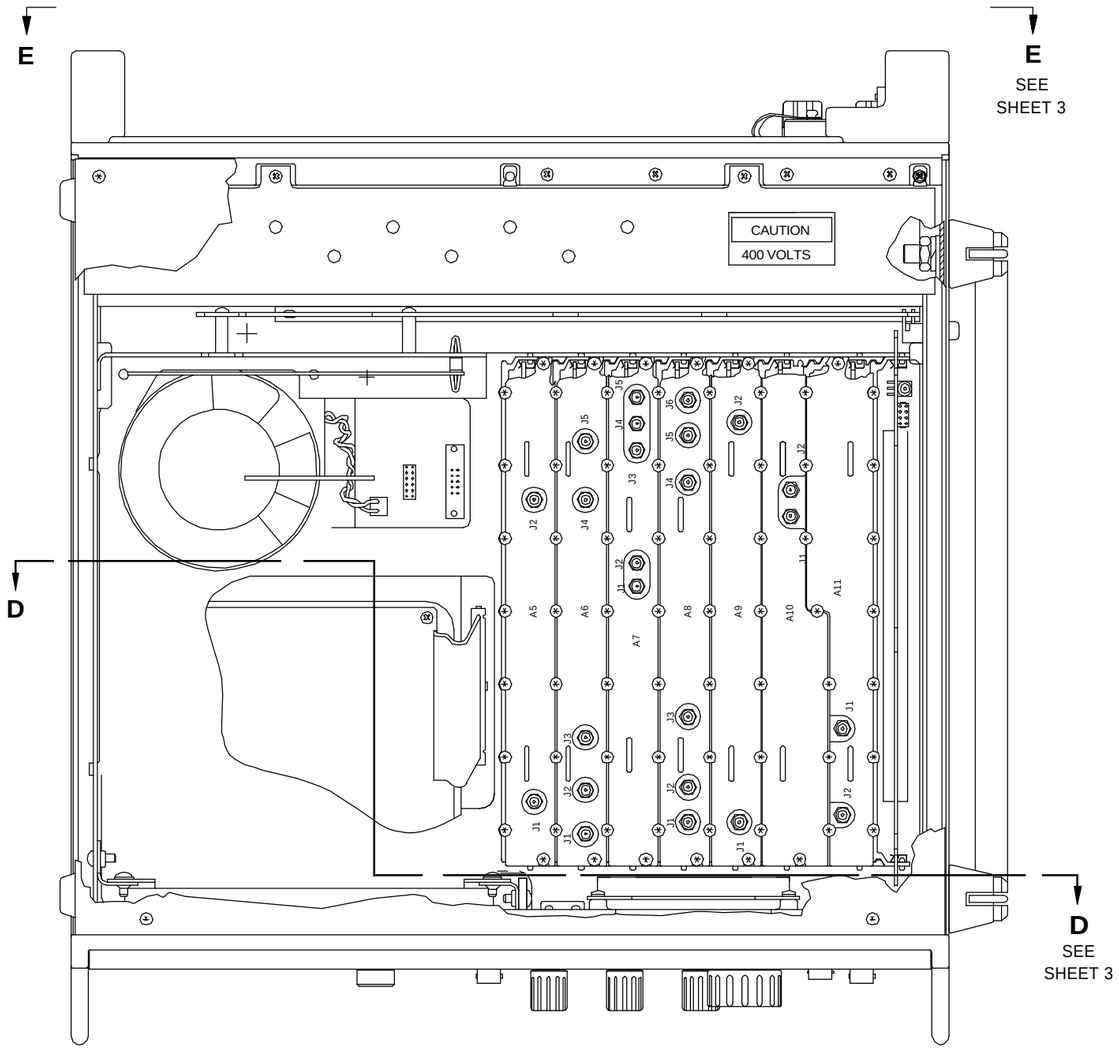


BASE UNIT ASSEMBLY
R2600D (HIGH-TIER)

01-P57060J REV. A

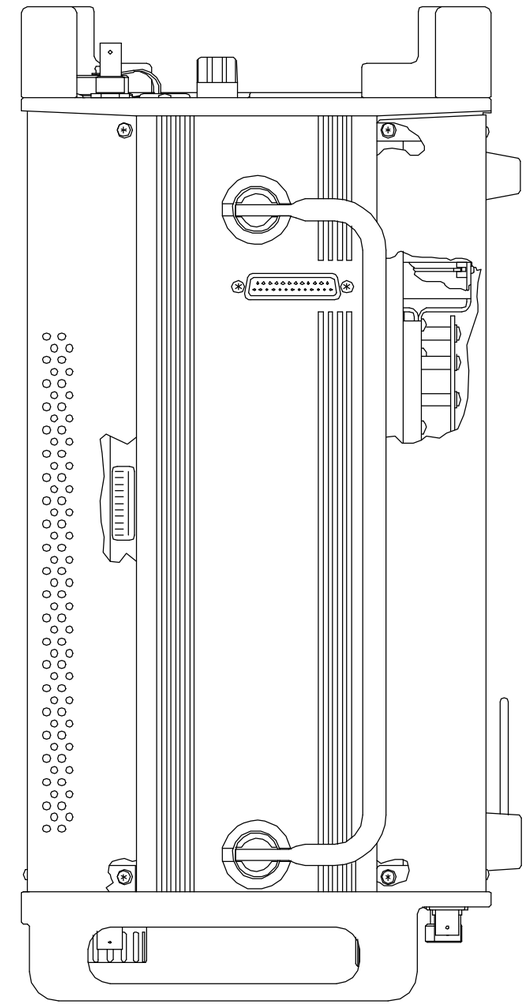
SHEET 1 OF 4





VIEW A-A

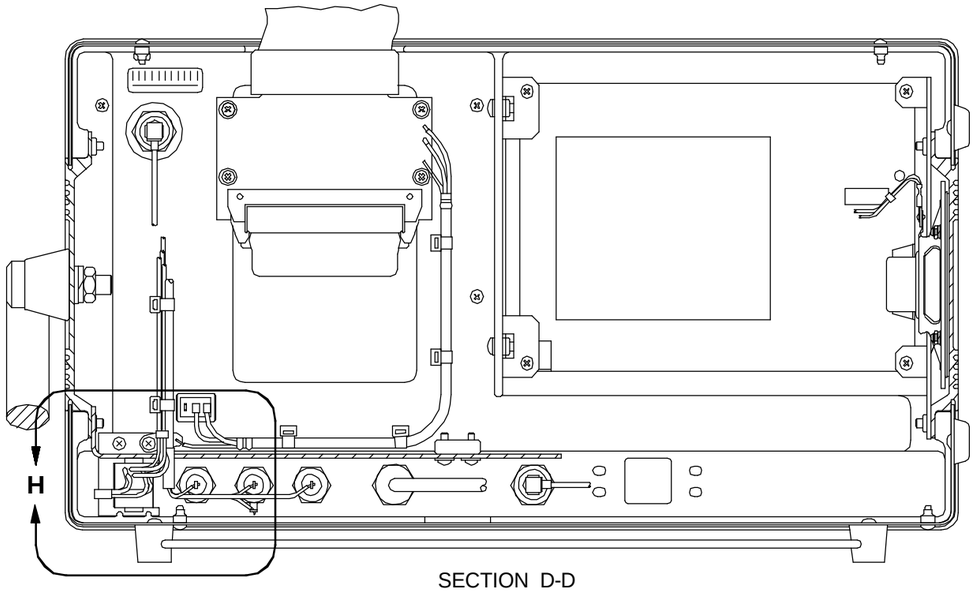
SEE SHEET 1



BASE UNIT ASSEMBLY
R2600D (HIGH-TIER)

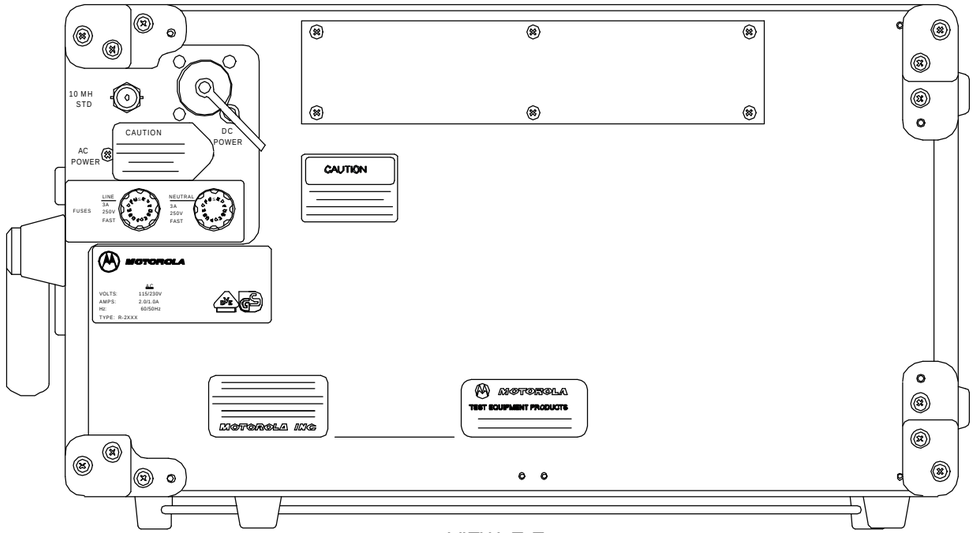
01-P57060J REV. A

SHEET 2 OF 4



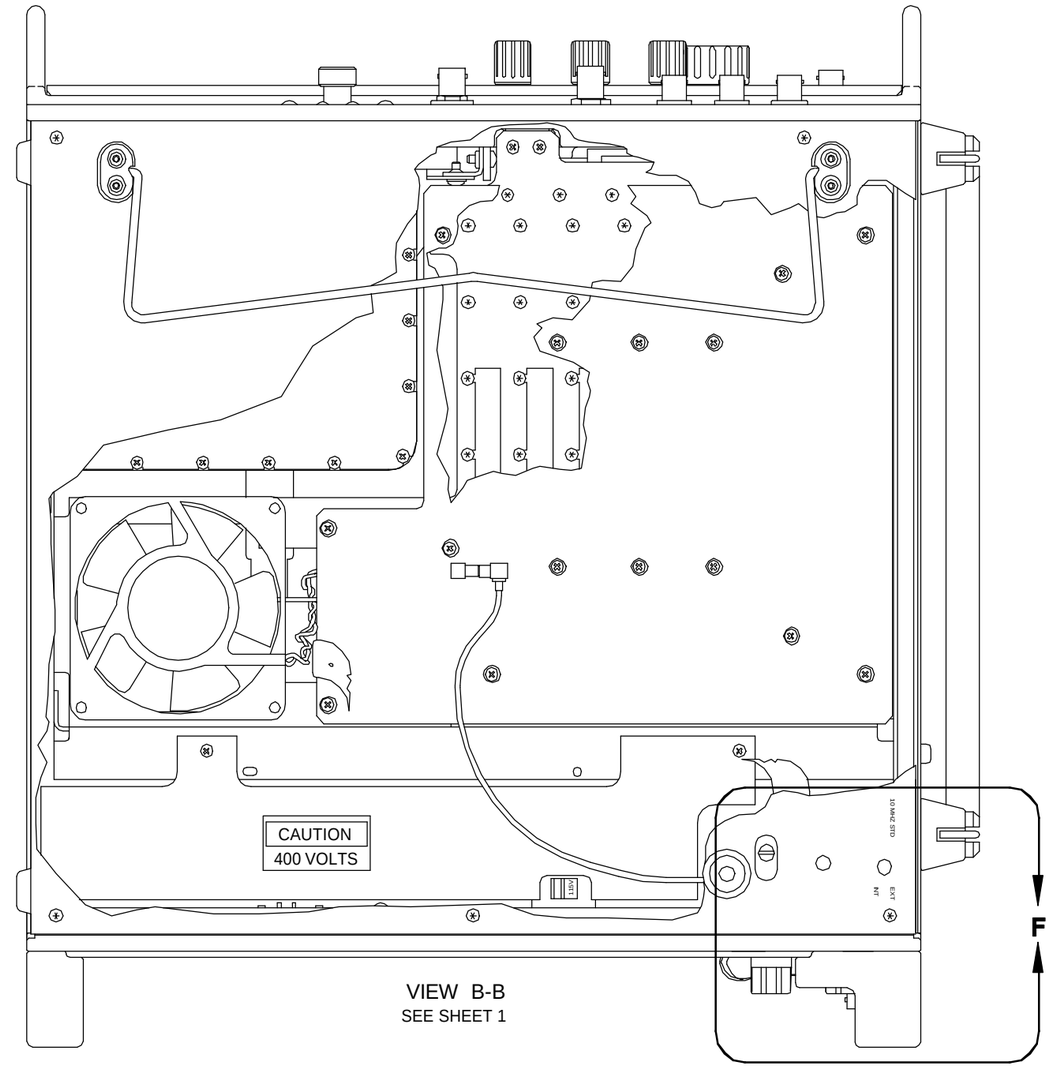
SECTION D-D

ROTATED 180°
SEE SHEET 2



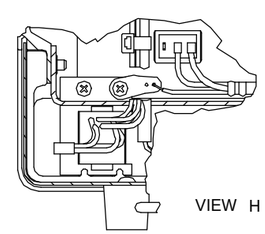
VIEW E-E

ROTATED 180°
SEE SHEET 2

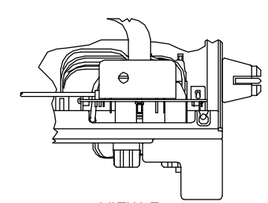


VIEW B-B

SEE SHEET 1



VIEW H

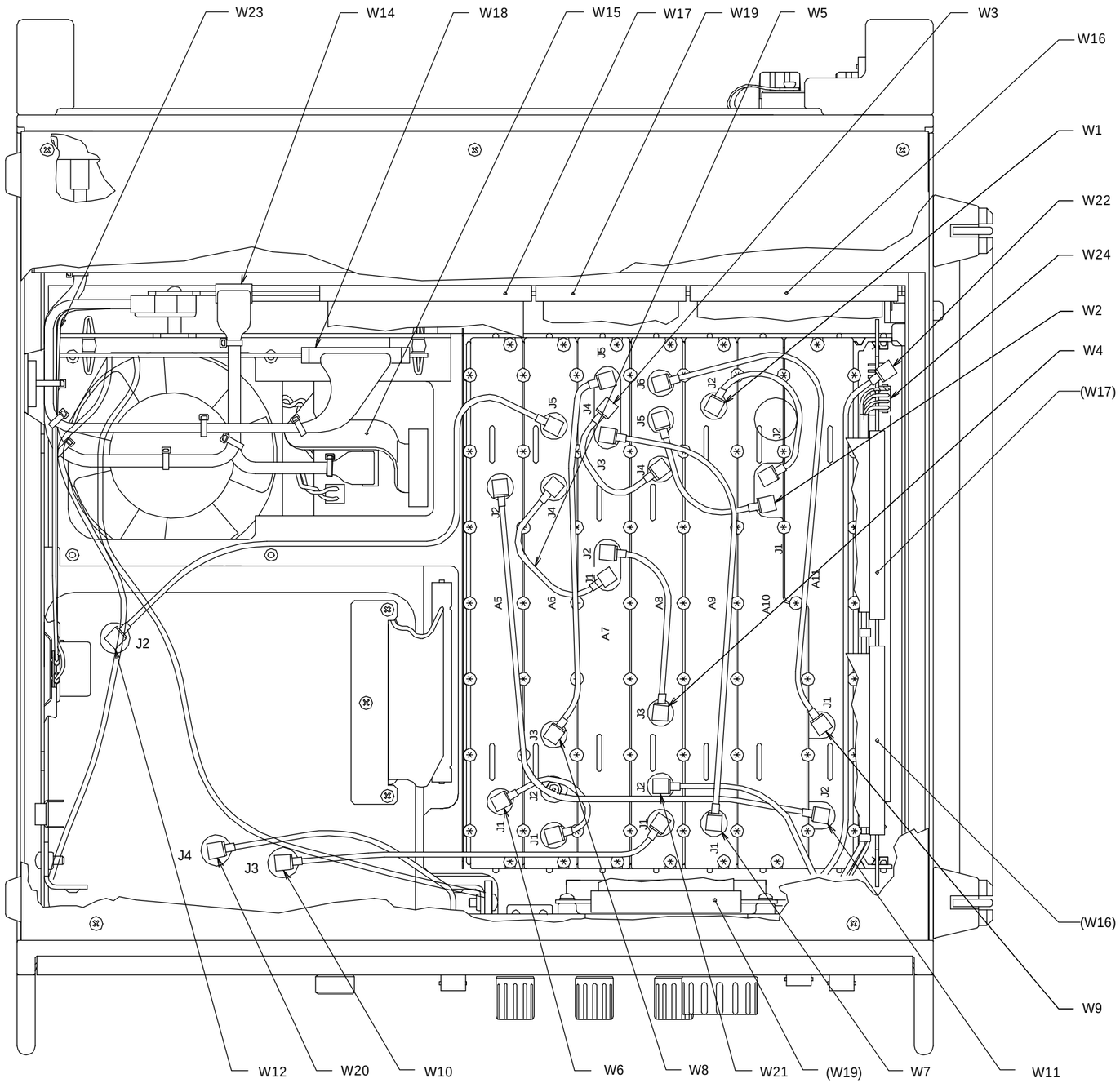


VIEW F

BASE UNIT ASSEMBLY
R2600D (HIGH-TIER)

01-P57060J REV. A

SHEET 3 OF 4



VIEW C-C

BASE UNIT ASSEMBLY
R2600D (HIGH-TIER)

01-P57060J REV. A

SHEET 4 OF 4

Section 20
DISPLAY PROCESSOR

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20.1 GENERAL DESCRIPTION

The Display processor module is designated A15 and is mounted to the bulkhead behind the LCD display.

The Cochise Display Processor Board is a new board that utilizes the Motorola's PowerPC, MPC823e. Its main function is to process and display video information to a color TFT LCD. The Main Processor Board previously performed this function. It has onboard Flash memory to enable remote update of the firmware. The board also has a separate LCD Controller to drive simultaneously a TFT LCD and an external CRT monitor. The board has interfaces to provide emulation and development support through a BDM port, a special EST emulator port, and a logic analyzer port. The board was designed to drive TFT LCD panels manufactured by AND or NEC.

20.2 SIGNALS SUMMARY

The signals to/from the Display Processor Module appear here organized in alphabetical order for each connector. Where signals are routed through this module to another connector they are noted as such.

Some signals described here are not used. These are included because of their potential use in future product development.

20.2A Display Processor Signal Descriptions

20.2A.1 J1 Main Processor

MPBA1 – MPBA22 (Main Processor Buffered Address) are the buffered outputs from the MC68000 processor address lines.

MPBRESET_N (Main Processor Buffered RESET) input is used to reset the Display Processor Module.

MPBLDS_N (Main Processor Lower Data Strobe) when at a logic 0 indicates that valid data is on the lower eight data lines of the MC68000 processor.

MPBOPT0 – MPBOPT15 are the Display Processor buffered inputs/outputs of the MC68000 data bus.

MPBRTARM is wiper arm of brightness potentiometer routed from front panel through main processor module for LCD panel display.

MPBRTLO is low side of brightness potentiometer signal routed from the front panel through the main processor module for the LCD panel display.

MPBRTHI is the high side of brightness potentiometer signal routed from the front panel through the main processor module for the LCD panel display.

MPBRW_N (Main Processor Buffered Read/Write) is the buffered read/write signal which indicates the direction of data transfer to and from the MC68000 processor.

MPBUDS_N (Main Processor Upper Data Strobe) when a logic 0 indicates that valid data is on the upper eight data lines of the MC68000 processor.

MPDP SYSCLK is the buffered 10MHz clock input.

MPDTACK_N (Main Processor Data Terminal ACKnowledge) output line indicates to the MC68000 processor that a data acknowledge is being issued from the Display Processor.

MPFLASH UNLOCK is +12V input for boot/sector unlock of Display Processor Flash Memory.

MPIACK6_N (Main Processor Interrupt ACKnowledge) input that signifies that the main processor has acknowledged an interrupt request number 6 cycle.

MPIRQ6_N (Main Processor Interrupt Request) output of an interrupt request number 6 to the MC68000 processor.

MPOPTDET4_N (Main Processor Option Detect) input to the MC68000 processor which signifies the presence of the Display Processor module. A logic 0 on this line signifies that the Display Processor is present.

MPOPTMEM_N (Main Processor Option Memory) active low output selects option memory space.

MPVBACKUP is the battery backup voltage input. (+3.6Vdc nominal)

MPVPA_N (Main Processor Valid Peripheral Address) output signal

MPSEML_N is Semaphore flag bit input to dual-port RAM. Not used at this time.

20.2A.2 J3 RS232

RX is the receive data input signal.

TX is the transmit data output signal.

20.2A.3 J4 CPLD

TCK (Test Clock) This input is used to clock programming information into the CPLD device from the in-circuit programming cable.

TDI (Test Data Input) This input receives the programming data for the CPLD device from the in-circuit programming cable.

TDO (Test Data Output) This output supplies data from the CPLD device to the in-circuit programming cable for use in verifying the CPLD was correctly programmed.

TMS (Test Mode Select) This signal controls the mode of operation when using the TAP (Test Access Port), i.e. boundary scan, in-circuit programming etc.

+3.3V The +3.3 volts supplies the in-circuit programming interface cable/module with power.

20.2A.4 J7 TDK Inverter

MPBRTHI is the high side brightness potentiometer signal that has been passed from the front panel through the Main processor to the Display processor where it is modified for use with the external inverter.

MPBRTLO is the low side brightness potentiometer signal that has been passed from the front panel through the Main processor to the Display processor where it is modified for use with the external inverter.

SCN BLANK turns the inverter off to prolong the life of the back light assembly in the LCD panel.

+12V The +12 volts supplies main power to the inverter assembly.

20.2A.5 J8 AND Inverter

MPBRTARM is the brightness potentiometer wiper signal that has been passed from the front panel through the Main processor to the Display processor where it is modified for use with the internal inverter.

SCN BLANK turns the inverter off to prolong the life of the back light assembly in the LCD panel.

+12V The +12 volts supplies main power to the inverter assembly.

20.2A.6 J9 NEC LCD

DRDY Display enable output.

FPDAT0 – FPDAT14 Flat Panel Data bits 0 through 14.

FPFRAME Flat Panel Frame pulse.

FPLINE Flat Panel Line pulse.

FPSHIFT Flat Panel Shift clock.

+5V The +5 volts supplies power to the internal flat panel logic.

20.2A.7 J10 AND LCD

DRDY Display enable output.

FPDAT0 – FPDAT14 Flat Panel Data bits 0 through 14.

FPFRAME Flat Panel Frame pulse.

FPLINE Flat Panel Line pulse.

FPSHIFT Flat Panel Shift clock.

+5V The +5 volts supplies power to the internal flat panel logic.

+5V PULLUP Sets the right/left and up/down orientation of the panel.

20.2A.8 J11 EXT VGA MONITOR

HSYNC output provides the horizontal synchronization pulses used to synchronize each scan line.

RED, GREEN, BLUE are the video signals required to drive a VGA monitor.

VSYNC output provides the monitor with vertical synchronization.

20.2A.9 J12, J13 EST Emulator

Note

The J12 and J13 connectors are for engineering development and are not placed on production modules.

A6 – A31 Address bus connected to the Power PC processor through 0 ohm resistors.

Note

These resistors are not placed on production units.

AT0 – AT3 Address Type bits 0 through 3. Driven by the Power PC when it owns the external bus to provide additional information about the address on the current transaction.

BB_N Bus Busy signal asserted by a master to show it owns the bus.

BDIP_N Burst Data In Progress signal asserted by the master on the bus to indicate the data beat in front of the current one is the one requested by the master.

BG_N Bus Grant signal is asserted in response to a bus request.

BHRESET_N Buffered Hard Reset signal causes the Power PC to enter the hard reset state.

BR_N Bus Request is asserted when a possible master requests ownership of the bus.

BSRESET_N Buffered Soft Reset signal causes the Power PC to enter the soft reset state.

BURST_N Burst transaction is driven by the bus master to indicate that the current initiated transfer is a burst one.

CS0_N – CS7_N Chip Selects 0 through 7 are used to access peripheral devices at specific addresses.

CLKOUT3 Buffered clock output from the Power PC.

Note

A zero ohm resistor is used to make this connection. Resistor is not placed on production units.

D0 – D31 Data bus connected to the Power PC processor through 0 ohm resistors.

Note

These resistors are not placed on production units.

DP0 – DP3 Data Parity bits 0 through 3 provide parity generation and checking for the data bus.

DSCK Development Serial Clock is the clock for the debug port interface.

DSDI Development Serial Data Input is the input data pin for the debug port interface.

DSDO Development Serial Data Output is the output data pin for the debug port interface.

GPL_A0 – GPL_A5 General Purpose line bits 0 through 5 from the user programmable machine A. Outputs reflects the value specified in the UPMA in the memory controller when an external transfer to a slave is controlled by UPMA.

GPL_B4 General Purpose line 4 from the user programmable machine B. Outputs reflects the value specified in the UPMB in the memory controller when an external transfer to a slave is controlled by UPMB.

IRQ0_N – IRQ7_N Interrupt Request lines 0 through 7 used to request service by a peripheral device.

MODCLK1, MODCLK2 Mode Clock 1 and 2 are sampled at PORESET_N negation to configure the PLL/clock mode of operation.

PB29, PB30 General purpose I/O port B bits 29 and 30.

PORESET_N Power On Reset when asserted causes the Power PC to enter the power on reset state.

TA_N Transfer Acknowledge indicates a slave device addressed in the current transaction has excepted the data from the master.

TEA_N Transfer Error Acknowledge indicates a bus error occurred in the current transaction.

TEXP Timer EXPired.

TMS Test Mode Select controls the mode of operation when using the TAP (Test Access Port).

TRST Test Reset asynchronously resets the TAP machine on the JTAG interface.

TS_N Transfer Start is asserted by the bus master to indicate the start of a bus cycle that transfers data to or from a slave device.

TSIZ0, TSIZ1 Transfer Size bits 0 and 1 are used to indicate the number of operand bytes waiting to be transferred in the current bus cycle.

VF0 – VF2 Visible instruction queue flushes status bits 0 through 2 indicate the number of instructions flushed from the instruction queue in the internal core.

VFLS0, VFLS1 Visible history flushes status bits 0 and 1 report the number of instructions flushed from the history buffer in the internal core.

WE0_N – WE3_N Write Enable bits 0 through 3.

WR_N Read/Write is driven by the bus master to indicate the direction of the bus's data transfer. A logic one indicates a read and a logic 0 indicates a write.

+3.3V provides power to the emulator.

20.2A.10 J14 Debug Port

BHRESET_N Buffered Hard Reset signal causes the Power PC to enter the hard reset state.

DSCLK Development Serial Clock is the clock for the debug port interface.

DSDO Development Serial Data Output is the output data pin for the debug port interface.

DSDI Development Serial Data Input is the input data pin for the debug port interface.

BSRESET_N Buffered Soft Reset signal causes the Power PC to enter the soft reset state.

VFLS0, VFLS1 Visible history flushes status bits 0 and 1 report the number of instructions flushed from the history buffer in the internal core.

+3.3V provides power to the emulator.

20.2A.11 J15, J16, J17 Logic Analyzer

Note

The J15, J16 and J17 connectors are for engineering development and are not placed on production modules.

A6 – A31 Address bus connected to the Power PC processor through 0 ohm resistors.

Note

These resistors are not placed on production units.

BB_N Bus Busy signal asserted by a master to show it owns the bus.

BDIP Burst Data In Progress signal asserted by the master on the bus to indicate the data beat in front of the current one is the one requested by the master.

BI_N Burst Inhibit indicates the device addressed in the current burst transaction is unable to support burst transfers.

BR_N Bus Request is asserted when a possible master requests ownership of the bus.

BHRESET_N Buffered Hard Reset signal causes the Power PC to enter the hard reset state.

BSRESET_N Buffered Soft Reset signal causes the Power PC to enter the soft reset state.

BURST_N Burst transaction is driven by the bus master to indicate that the current initiated transfer is a burst one.

CLKOUT3 Buffered clock output from the Power PC.

Note

A zero ohm resistor is used to make this connection. Resistor is not placed on production units.

CS0 – CS7 Chip Selects 0 through 7 are used to access peripheral devices at specific addresses.

D0 – D31 Data bus connected to the Power PC processor through 0 ohm resistors.

Note

These resistors are not placed on production units.

GPL_A0 – GPL_A5 General purpose line bits 0 through 5 from the user programmable machine A. Outputs reflects the value specified in the UPMA in the memory controller when an external transfer to a slave is controlled by UPMA.

MODCLK1, MODCLK2 Mode Clock 1 and 2 are sampled at PORESET_N negation to configure the PLL/clock mode of operation.

OE_N is asserted when the power PC initiates a read access to an external slave controlled by the GPCM in the memory controller.

TA_N Transfer Acknowledge indicates a slave device addressed in the current transaction has excepted the data from the master.

TEA_N Transfer Error Acknowledge indicates a bus error occurred in the current transaction.

TS_N Transfer Start is asserted by the bus master to indicate the start of a bus cycle that transfers data to or from a slave device.

TSIZ0, TSIZ1 Transfer Size bits 0 and 1 are used to indicate the number of operand bytes waiting to be transferred in the current bus cycle.

WE0_N – WE3_N Write Enable bits 0 through 3.

WR_N Read/Write is driven by the bus master to indicate the direction of the bus's data transfer. A logic one indicates a read and a logic 0 indicates a write.

20.2B Display Processor Connector Descriptions

20.2B.1 J1 (68 pin connector to Main Processor Board)

pin	
GND	
2	MPBOPT (0)
3	MPBOPT (1)
4	MPBOPT (2)
4	MPBOPT (3)
6	MPBOPT (4)
7	MPBOPT (5)
8	MPBOPT (6)
9	MPBOPT (7)
10	GND
11	MPBOPT (8)
12	MPBOPT (9)
13	MPBOPT (10)
14	MPBOPT (11)
15	MPBOPT (12)
16	MPBOPT (13)
17	MPBOPT (14)
18	MPBOPT (15)
19	GND
20	spare
21	MPBA (1)
22	MPBA (2)
23	MPBA (3)
24	MPBA (4)
25	MPBA (5)
26	MPBA (6)
27	MPBA (7)
28	GND
29	MPBA (8)
30	MPBA (9)
31	MPBA (10)
32	MPBA (11)
33	MPBA (12)
34	MPBA (13)
35	MPBA (14)
36	GND
37	MPBA (15)
38	MPBA (16)
39	MPBA (17)
40	MPBA (18)
41	MPBA (19)
42	MPBA (20)
43	MPBA (21)
44	MPBA (22)
45	GND
46	MPBLDS_N
47	MPBUDS_N
48	GND
49	MPBRW_N
50	MPIACK6_N
51	MPDTACK_N
52	MPBRESET_N
53	MPVPA_N
54	MPVBACKUP
55	MPIRQ6_N
56	MPBRTARM
57	MPBRTLO
58	MPBRTHI
59	MPSEML_N
60	MPOPTMEM_N
61	MPOPTDET4_N
62	MPFLASH_UNLOCK
63	spare
64	GND
65	MPDP_SYSCLK
66	GND
67,68	spare

20.2B.2 J2 (6 pin connector for power)

pin	
+5v	
+12v	
–5V	
–12V	
5,6	GND

20.2B.3 J3 (9 pin RS-232 connector)

pin
not used
TX
RX
Not used
GND
not used

20.2B.4 J4 (8 pin header for CPLD)

pin
+3.3V
TDO
TDI
decoupling capacitor
No connection
TMS
GND
TCK

20.2B.5 J5 (3 pin header for MODCK2 polarity)

jumper
MODCK2 High
MODCK2 Low

20.2B.6 J6 (3 pin header for 5MHz clock enable)

jumper
Select 5MHz Clock
Disable 5MHz Clock

20.2B.7 J7 (5 pin connector for TDK inverter)

pin
+12V
GND
SCN BLANK
MPBRTLO
MPBRTHI

20.2B.8 J8 (5 pin connector for AND Inverter)

pin
+12V
+12V
MPBRTARM
4,5 GND
SCN BLANK

20.2B.9 J9 (31 pin connector for NEC LCD)

pin	controller	LCD
1	GND	GND
2	FPSHIFT	CLK
3	FPLINE	HSYNC
4	FPFRAME	VSYNC
5	GND	GND
6	FPDAT1	R2
7	FPDAT0	R3
8	FPDAT9	R0
9	FPDAT2	R1
10	FPDAT1	R2
11	FPDAT0	R3
12	GND	GND
13	FPDAT4	G2
14	FPDAT3	G3
15	FPDAT11	G0
16	FPDAT5	G1
17	FPDAT4	G2
18	FPDAT3	G3
19	GND	GND
20	FPDAT7	B2
21	FPDAT6	B3
22	FPDAT14	B0
23	FPDAT8	B1
24	FPDAT7	B2
25	FPDAT6	B3
26	GND	GND
27	DRDY	DE
28,29	+5V	VCC
30	not used	not used
31	GND	GND

20.2B.10 J10 (30 pin connector for AND LCD)

pin	controller	LCD
1	FPSHIFT	CLK
2	FPLINE	HSYNC
3	FPFRAME	VSYNC
4	GND	GND
5	GND	R0
6	GND	R1
7	FPDAT9	R3
8	FPDAT2	R4
9	FPDAT1	R5
10	FPDAT0	R6
11	GND	GND
12	GND	G0
13	GND	G1
14	FPDAT11	G2
15	FPDAT5	G3
16	FPDAT4	G4
17	FPDAT3	G5
18	GND	GND
19	GND	B0
20	GND	B1
21	FPDAT14	B2
22	FPDAT8	B3
23	FPDAT7	B4
24	FPDAT6	B5
25	GND	GND
26	DRDY	DENB
27	+5V	VCC
28	+5V	VCC
29	+5 PULLUP	R/L_N
30	+5 PULLUP	U/D_N

20.2B.11 J11 (15 pin connector for external CRT)

pin
RED
GREEN
BLUE
not used
AGND
not used
AGND
11,12 not used
HSYNC
VSYNC
not used

20.2B.12 J12 (80 pin connector for EST Emulator 1)

Note

This connector is not placed

pin	
1	A31
2	A30
3	A29
4	A28
5	GND
6	A27
7	A26
8	A25
9	A24
10	A23
11	A22
12	A21
13	A20
14	A19
15	A18
16	A17
17	A16
18	GND
19	A15
20	A14
21	A13
22	A12
23	A11
24	A10
25	A9
26	A8
27	D31
28	D30
29	D29
30	GND
31	D28
32	D27
33	D26
34	D25
35	D24
36	D23
37	D22
38	D21
39	D20
40	GND
41	GND
42	D19
43	D18
44	D17
45	D16
46	WE3_N
47	CS0_N
48	CS1_N
49	CS2_N
50	CS3_N
51	CS4_N
52	GND
53	CS5_N
54	CS6_N
55	DP3
56	DP2
57	DP1
58	DP0
59	BG_N
60	BR_N
61	PORESET_N
62	CLKOUT3
63	GND
64	WR_N
65	TSIZ1
66	TSIZ0
67	TA_N
68	TEA_N
69	TS_N
70	MODCK1
71	VF2
72	VF0
73	BSRESET_N
74	VFLS0
75	BHRESET_N
76	GND
77	DSDI
78	DSCK
79	DSDO
VFLS1	

20.2B.13 J13 (80 pin connector for EST Emulator 2)

Note

This connector is not placed

pin	
1	D15
2	D14
3	D13
4	D12
5	GND
6	D11
7	D10
8	D9
9	D8
10	D7
11	D6
12	D5
13	D4
14	D3
15	D2
16	D1
17	D0
18	GND
19	A7
20	A6
21	GPL_A5

22	GPL_B4
23	GPL_A4
24	GPL_A2
25	GPL_A1
26	GPL_A0
27	WE2_N
28	VF1
29	GND
30	WE1_N
31	WE0_N
32	CS7_N
33	AT3
34	AT2
35	AT1
36	AT0
37	PB30
38	PB29
39	GPL_A3
40,41	GND
42	N/C
43	IRQ7_N
44	IRQ6_N
45	IRQ4_N
46	N/C
47	IRQ2_N
48	IRQ1_N
49	IRQ0_N
50	BB_N
51	BURST_N
52	GND
53-57	N/C
58	TMS
59-62	N/C
63	GND
64	N/C
65-68	3.3V
69	N/C
70	TRST
71	BDIP_N
72	MODCK2
73-75	N/C
76	GND
77-79	N/C

TEXP

20.2B.14 J14 (10 pin header for Debug Port)

pin
VPLS0
SRESET_N
GND
DSCK
GND
VFLS1
BHRESET_N
DSDI
+3.3V
DSDO

20.2B.15 J15 (38 pin connector for Logic Analyzer)

Note

This connector is not placed.)

pin

1,2	not used
3	GND
4	not used

TSIZ0
TSIZ1
GND
A16
GND
A17
GND
A18
GND
A19
GND
A20
GND
A21
A6
A22
A7
A23
A8
A24
A9
A25
A10
A26
A11
A27
A12
A28
A13
A29
A14
A30
A15
A31(LSB)

20.2B.16 J16 (38 pin connector for Logic Analyzer)

Note

This connector is not placed

pin

1,2	not used
3	GND

not used
CLKOUT3

not used
D0(MSB)
D16
D1
D17
D2
D18
D3
D19
D4
D20
D5
D21
D6
D22
D7
D23
D8
D24
D9
D25
D10
D26
D11
D27
D12
D28
D13
D29
D14
D30
D15
D31(LSB)

20.2B.17 J17 (38 pin connector for Logic Analyzer)

Note

This connector is not placed

pin
1,2 not used
GND
not used
TA_N
TEA_N
BHRESET_N
CS0_N
BSRESET_N
CS4_N
MODCLK2
CS2_N
MODCLK1
CS3_N
GPL_A0
CS1_N
GPL_A4
OE_N
GPL_A3
GPL_A5
GPL_A2
CS7_N
BG_N
not used
BB_N
not used
BR_N
not used
BI_N
not used
BDIP
WE0_N
BURST_N
WE1_N
WR_N
WE2_N
TS_N
WE3_N

20.2B.18 JP1 (2 pin header for backup voltage select)

Note

This feature is not used

pin
1 BATT
2 MPVBACKUP

20.2B.19 JP3 (2 pin header for Flash memory unlock select)

pin
1 +12 Volts
2 MPFLASH_UNLOCK

20.3 BLOCK DIAGRAM DESCRIPTION

The Display Processor can functionally be divided into three distinct sections as follows:

- The dual port RAM interface used to communicate between the Main Processor and the Display Processor.
- The core MCP823e Power PC processor and it's associated buffers, memory, and interfaces used for waveform processing, message processing, and display formatting of grids, bar graphs, cursors, and text.
- The Epson SED1355 LCD controller and it's associated memory and interfaces used for generating data, control, and timing signals for the LCD panel, and a standard VGA monitor output.

20.4 DETAILED DESCRIPTION

20.4.1 Reset

20.4.1.1 Power On Reset (PORESET_N)

At power on, the reset circuit asserts a Power-On Reset (PORESET). The Power Monitor circuit, MAX793, monitors the +3.3V on power on and asserts the PORESET until the +3.3V reaches its proper level plus 200ms. The MAX793 has a min/max voltage threshold of 3.00/3.15V. It will assert a PORESET if +3.3V falls below this level during normal operations. The power supply monitoring IC also gates the chip select for the SRAM's. This feature can be used with the battery backup to prevent the SRAM's data from being corrupted during a power drop or loss. Currently the battery backup is not in use.

20.4.1.2 Hardware Reset (HRESET_N)

The HRESET_N signal is a bi-directional, active low, open-collector I/O signal. The PORESET_N causes the MPC823e internally to assert the HRESET_N and SRESET_N. During this time, the MPC823e will sample the configuration from the data bus. The processor can only sample an external assertion of HRESET_N if it occurs while the processor is not internally asserting HRESET_N. When the processor detects a HRESET_N, it also drives the SRESET_N low.

20.4.1.3 Soft Reset (SRESET_N)

SRESET_N is used for development purposes along with emulators or debuggers. The SRESET_N is open drain and the processor will drive it to 0 if it detects a HRESET_N.

20.4.1.4 Power-On Reset Configuration

When PORESET_N is negated by the external logic, the power-on reset configuration, which include the MODCK[1:2] pins, are sampled. These pins determine the clock operation mode of the MPC823e. The selected mode is 1:5 PLL operation via an onboard clock generator (5.0MHz).

20.4.1.5 Hard Reset Configuration

During a hard reset sequence when RSTCONF_N is asserted, the processors data bus is sampled to acquire the processor hard reset configuration. Pull-up or pull-down resistors determine the reset configuration word. The board provides for both on data bits D[0:15] for flexible configuration. RSTCONF_N is always driven low. The system parameter defaults during a power-on reset, are listed below:

Arbitration – None, D0=0
Interrupt Prefix – EVT located at 0XFFF00000, D1=0
Memory controller – enable CS0, D3=0
Boot Port Size – 32 bits, D4=D5=0
Initial Internal Space Base – IMMR at FF000000, D7=1, D8=0
Debug Pin Configuration – Program tracking functions, D9=1, D10=1
Debug Port Pin Configuration – Select DBGC + Dev. Support Comm, D11=D12=0
Extended Bus Division Factor – CLKOUT is GCLK2 divided by 2. D13=0, D14=1.

20.4.2 Clock Generator

The clock for the MPC823e uses a 5.0MHz clock oscillator via the EXTCLK pin, 1:5 PLL mode.

To enable this mode use jumpers J6 and J5. The combination outputs driven to the MODCK lines during power-on reset and to the connection of an appropriate capacitor between the MPC823e's XFC and VDDSYN inputs must match the PLL's multiplication factor. A 4700pF capacitor is chosen for this mode. With the 5.0MHz clock oscillator, the MF can be set for the system clock to run from 25MHz in multiples of 5Mhz up to 75MHz.

20.4.3 Buffering

To ensure that the MPC823e's capacitive drive capability is met (50pF) on the address and data bus, buffers for address bus and transceivers for data bus are provided. The 74LCX buffers/transceivers used are 3.3V and 5V tolerant. This type of buffer reduces onboard noise caused by the reduced transitions' amplitude.

20.4.4 MPC823e

20.4.4.1 Chip-Select Generator

The MPC823e memory controller is used as a chip-select generator to access onboard memories. The chip-select assignment for the various memories on this board is shown in Table 20-1. Chip select CS0 is further decoded for the two banks of flash memories.

CHIP-SELECT:	ASSIGNMENT
CS0_N	Flash Memory
CS1_N	SRAM
CS2_N	DUAL PORT RAM
CS3_N	SDRAM
CS4_N	LCD CONTROLLER
CS[5:7]	Unused, but available

FIGURE 20-1 MPC823e Chip-Select Assignment

20.4.4.2 Dedicated I/Os

The processor provides dedicated I/Os for control and monitoring the different parts of the Display Board. These signals are given as follows:

BATTOK_N (PD15): This is an input signal from the power-on reset IC, MAX793, which indicates the health of the battery. At this time, this function is not implemented and is for a future option on this board.

BUSYR (PD14): This is an input signal from the Dual Port RAM to indicate that the memory device is being access from the other port and is busy.

SEMR (PD13): This is an output signal to the Dual Port RAM to set the Semaphore flag in the memory device.

RS232_INVALID (PD11): This input signal is enabled high if a valid RS-232 level is present on the receiver input.

BLANKING (PD10): This general I/O is buffered, but not used for any purpose at this time. This is for future use.

PFO_N (PD10): This input signal is from the power-on reset IC to indicate the Power-Fail Comparator Output. When PFI is less than Vpft or when Vcc falls below Vsw, PFO goes low: otherwise, PFO remains high. Vpft is set to 2.98V while Vsw is 2.82V typical, 2.69V Min, and 2.95V Max. This input monitors the health of the +5V supply.

DISPLAY TYPE (PD8): This input is normally tied high to indicate one type of display, AND. To configure the board for the NEC display, install resistors R273 and R276. Remove resistors R271 and R274.

20.4.5 CPLD

A CPLD (Complex Programmable Logic Device) provides address and strobe decoding for the Main Processor's interface. In addition, it decodes the chip selects for the on-board flash and the data buffers. The CPLD is in-circuit programmed via an external header. The equations for the CPLD are listed below:

FCE0_N = A9 & !CE0_N
(Upper flash chip select, 400000 -> 7FFFFF)

FCE1_N = !A9 & !CE0_N
(Lower flash chip select, 0 -> 3FFFFF)

CSA_N = CE0_N & CE1_N & CE2_N
(Data buffer enable for flash, dual-port RAM, & SRAM)

DTACK := DISPLAYSEL
(One clock delayed of DISPLAYSEL)

DISPLAYSEL.D := DOPTMEM * LABUSS22 * !LABUSS21 * LABUSS20
(Synchronize data buss to local clock, DXXXXX)

DISPLAYSEL.AR = BRW*BLDS*BUDS
(Latch clear)

DISPLAYSEL.C = BSYSCLK
(Latch clock @ 10MHz)

DPRAMRDWR_N = !(DISPLAYSEL * !DTACK * BRW)
(RAM read/write)

DPRAMSEL_N = !(DISPLAYSEL * LABUSS19 * LABUSS18 * !LABUSS17 * !LSBUSS16 * !BLDS)
(DUAL PORT RAM select, XCXXXX)

VPA = IRQ6 * !BIACK6
(ACK for 68K processor)

IRQ6 = !INT
(Interrupt 68K processor)

DPRW_N = !BRW_N
(Need to invert R/W for DPRAM data buss)

OENR=CS2_N*OEN
(Not used)

20.4.6 Static RAM, SRAM

The Display Processor Board has SRAM comprised of two chips with a total memory of 1MB. Each chip is 256K x 16-bit wide to make up 256K x 32 total memory. The memory is set up to write on a word basis (32-bit word at a time) and has an access time of 85ns max, which requires four wait states at 37.5MHz from the processor.

20.4.7 Flash Memory

The Display Processor Board has 2M x 32 of Main Flash. The four 1M x 16 devices make up the 32-bit wide bus. The Flash devices are 3.3V technology, AT49LV1614, Sector Flash with either 90 to 110ns access time. Depending which device is used, the wait states will change to accommodate either device. With a 90ns part, the number of wait states required is four. Address space covers from FFC00000 to FFFFFFFF.

The Flash provides a boot or start-up facility, to prep the system and get it ready for the targeted OS to run on the board. The application code can be copied onto the SDRAM for execution.

20.4.8 Synchronous DRAM, SDRAM

The Display Processor contains 16MB of SDRAM that is made up of two 4M x 16 devices. 4K refreshing are used via CAS before RAS refreshing to lower current consumption compared to 1K refreshing devices. The SDRAM is unbuffered from the processor, which cuts down on the delay associated with address and data buffers. No support is provided for battery back up and parity checking of the SDRAM array. The SDRAM devices are 3.3V technology, UPD4564163G6-A80 (NEC). The UPMA of the MPC823e is programmed as the SDRAM controller. The PTA, periodic timer A, of the MAMR register is set to hex 49 for a 15.63us refresh period.

20.4.9 Dual Port RAM, DPRAM

A 4K x 16 wide dual port static RAM is provided to interface with the Main Processor (68K) to the MPC823e. The device is an IDT70V24 from IDT with a 25ns access time. The number of wait states for this device is calculated to be two. The memory chip has interrupt and semaphore features to provide flexibility for both processors to interface to each other. The address decoding for the dual port RAM is programmed in the CPLD. When the Display Processor is addressed by the Main Processor, the dual port ram is selected and all messages pass through this device.

20.4.10 LCD Controller

The SED1355 is a color LCD graphics controller that interfaces to the MPC823e in a seamless matter. This device is made by Epson. The controller supports the 9/12-bit TFT LCD. It also has an embedded RAMDAC for direct analog CRT drive. The controller requires a 1M x 16 EDO DRAM and an external clock generator of between 25.08538MHz and 25.36431MHz with 25.175MHz being the preferred frequency. Since this part is a 3.3V part, the fastest data rate between the MPC823e processor and itself is specified at 40Mhz. However, since the MPC823e will run at 75Mhz, the clock out has been divided by 2 and the fastest rate is therefore 37.5Mhz which is the same clock for the SDRAM.

20.4.11 Memory Map

FLASH: FFC00000 – FFFFFFFF
CE0: FFC00000 – FFFFFFFF (4Meg)
CE1: XXXXXX – XXXXXX (not used at this time)
SRAM: 04000000 – 040FFFFF
DPRAM: 04400000 – 04401FFF
SDRAM: 00000000 – 00FFFFFF
LCD CONTROLLER BUFFER: 05200000 – 053FFFFF

20.5 BLOCK DIAGRAM

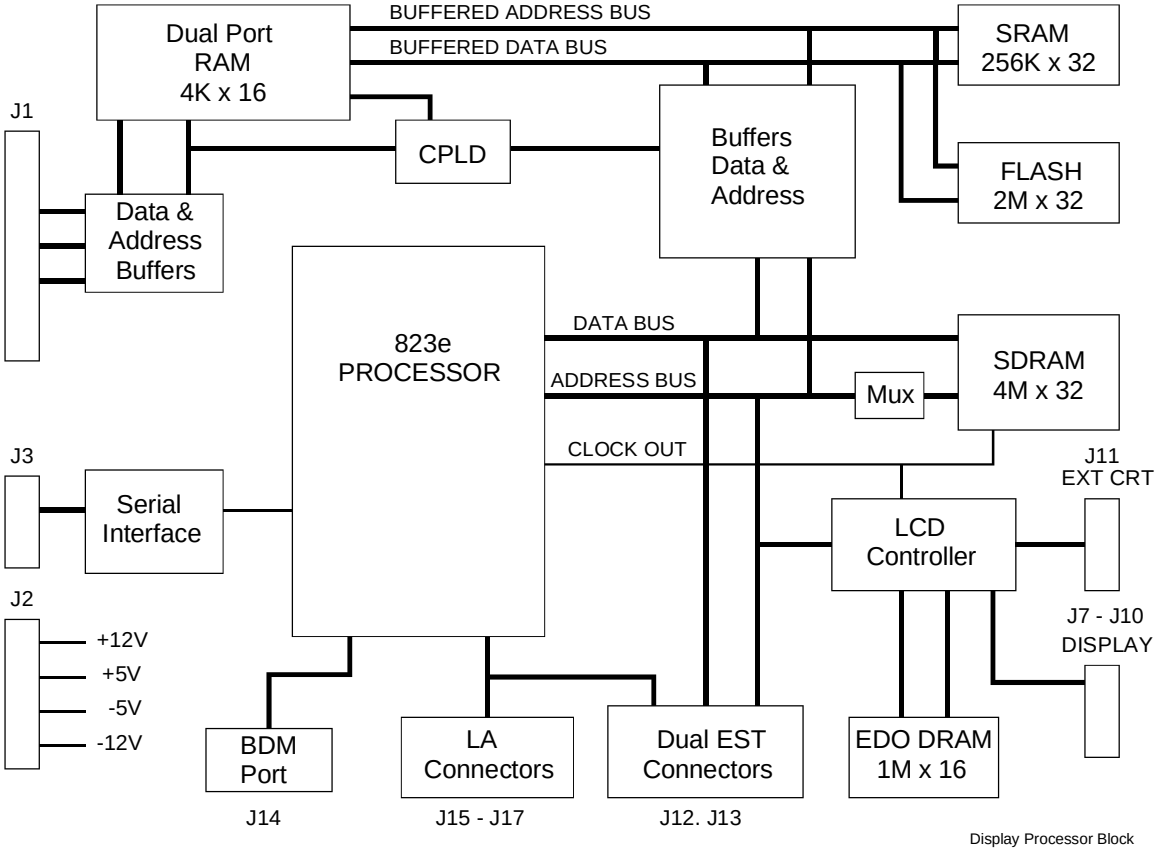
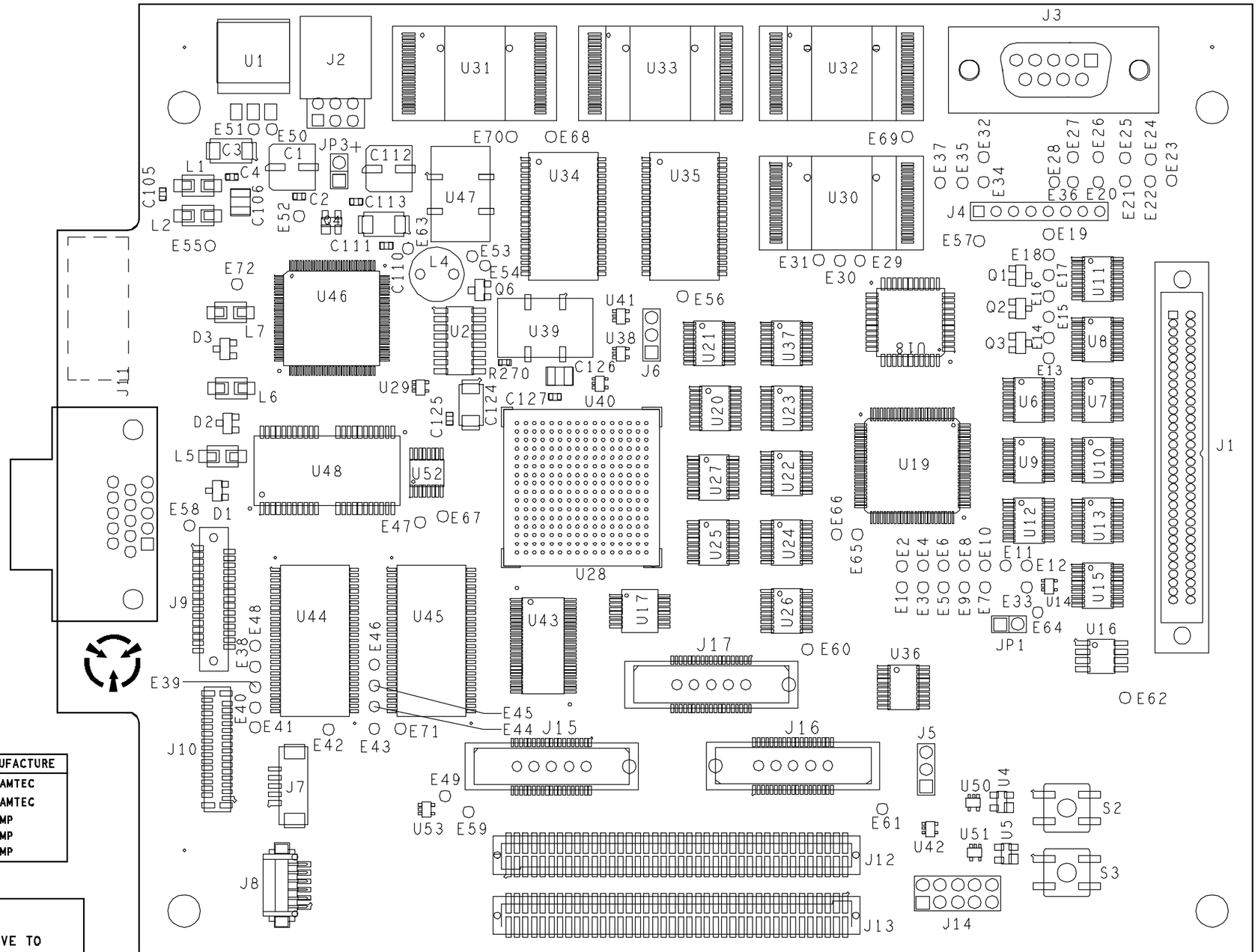


Figure 20.5 Display Processor Block Diagram



REF DES	PART NUMBER	MANUFACTURE
J12	TFM140-02-S-DLC	SAMTEC
J13	TFM140-02-S-DLC	SAMTEC
J15	2-767004-2	AMP
J16	2-767004-2	AMP
J17	2-767004-2	AMP

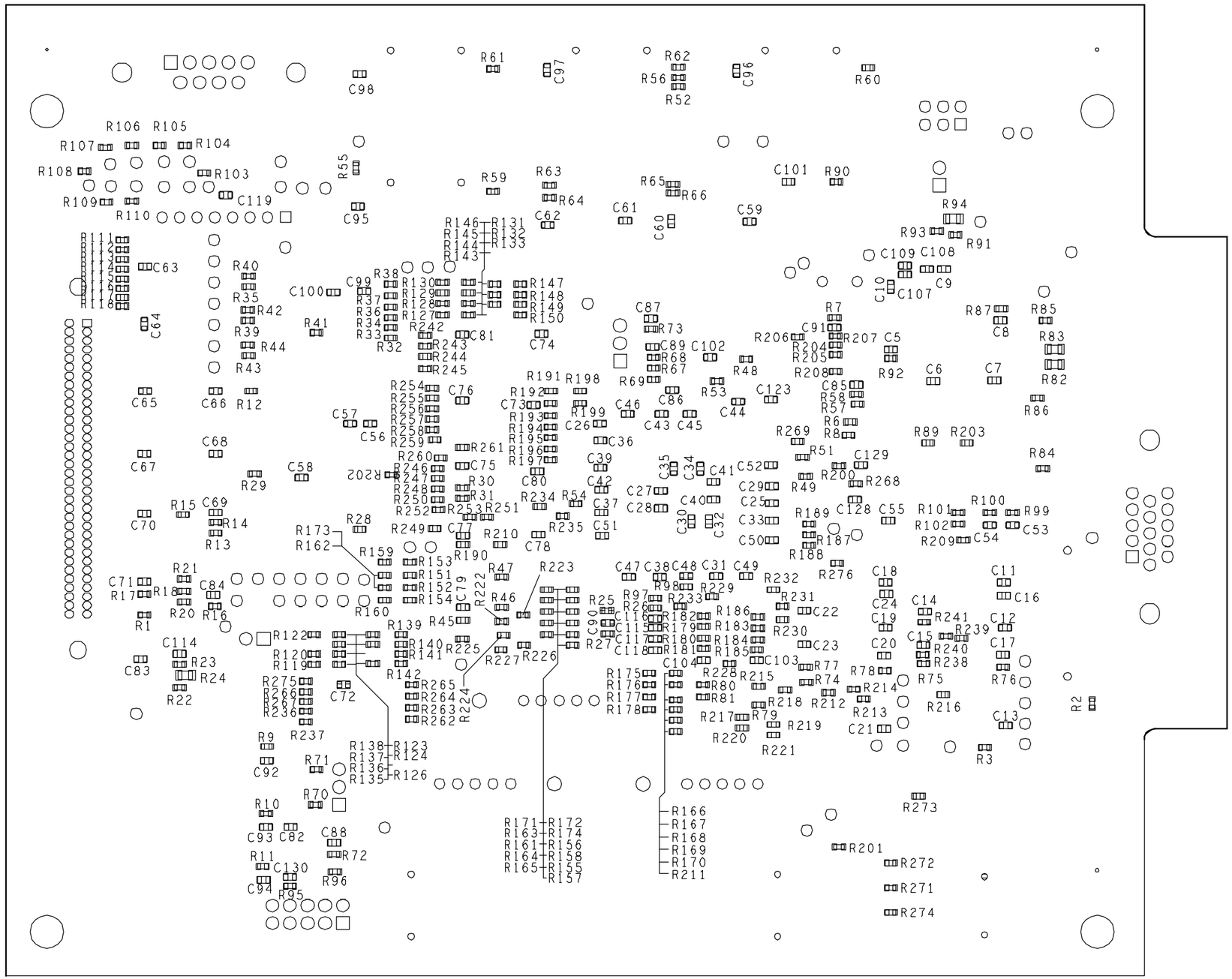
CAUTION

THIS ITEM IS SENSITIVE TO ELECTROSTATIC DISCHARGE (ESD)

CIRCUIT CARD ASSEMBLY
DISPLAY PROCESSOR

01-P57140J REV. A

SHEET 1 OF 2



BACK

CIRCUIT CARD ASSEMBLY
DISPLAY PROCESSOR

01-P57140J REV. A

SHEET 2 OF 2

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
A	CO L48752-3 IDB 00/11/01	00/10/16	A.GATTO

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A1.
2. FOR REFERENCE DRAWINGS REFER TO:
   ASSEMBLY 01-P57140J
   TEST PROCEDURE 12-P57143J
3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS +/-1PCT, .0625 WATTS.
   ALL CAPACITANCE VALUES ARE +/-10PCT, 16V.
   ALL INDUCTANCE VALUES ARE IN
   ALL VOLTAGES ARE IN VDC.
4. TERMINATIONS CODED WITH THE SAME LETTERS OR NUMBERS ARE ELECTRICALLY CONNECTED.
5. DEVICE TYPE NUMBERS AND CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE I.
6. DEVICE TYPE IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH MANUFACTURER. ENGINEERING APPROVED EQUIVALENT DEVICE MAY BE USED.
7. COMPONENT VALUE SELECTED IN TEST. NOMINAL VALUE SHOWN.
8. SYMBOL > FOLLOWING AN OFFPAGE REFERENCE INDICATES THAT THE SIGNAL IS DRIVEN BY THE CORESPONDING SIGNAL ON THE PAGE REFERENCED. SYMBOL < INDICATES THAT THE SIGNAL DRIVES THE CORESPONDING SIGNAL ON THE PAGE REFERENCED.
9. SYMBOL —/ REPRESENTS A COMPONENT TERMINAL THAT HAS NO CONNECTION.
10. FOR AND DISPLAY INSTALL RESISTORS R271 AND R274 AND LEAVE OUT RESISTORS R273 AND R276.
11. FOR NEC DISPLAY INSTALL RESISTORS R273 AND R276 AND LEAVE OUT RESISTORS R271, AND R274.
12. INSTALL 0-OHM RESISTOR FOR 4M MEMORY.
13. DO NOT JUMPER FOR NORMAL OPERATIONS.
14. JUMPER 1-2 FOR 5.0MHZ CLOCK INPUT.
    JUMPER 2-3 FOR CRYSTAL INPUT.
15. JUMPER 1-2 FOR 5.0MHZ CLOCK INPUT.
    JUMPER 2-3 FOR CRYSTAL INPUT.
16. FOLLOWING RESISTORS ARE NOT USED: R119, R120, R122, R123, R124, R127, R142, R144, R145, R130, R131, R132, R149.
17. LEAVE OUT R210-R235, R269 FOR PRODUCTION.
18. LEAVE OUT J12 AND J13 FOR PRODUCTION.
19. LEAVE OUT R236-R267 FOR PRODUCTION.
20. LEAVE OUT J15-J17 FOR PRODUCTION.
21. USE J8 AND J10 FOR "AND DISPLAY"
22. USE J9 AND J7 FOR "NEC DISPLAY"
23. LEAVE OUT R268 FOR PRODUCTION.
24. VALUE OF R272 SHOWN IS FOR AND DISPLAY REPLACE R272 WITH 100K OHMS FOR NEC DISPLAY.

TABLE I (5)

REF DES	DEVICE TYPE (6)	P3.3V CONNECTION		P5V CONNECTION		NSV CONNECTION		GND		
		CONN	VOLTS	CONN	VOLTS	CONN	VOLTS	AGND CONNECTION	CONNECTION	NO CONNECTION
U1	LT1086	-	-	3	VIN	-	-	1	-	-
U2	MAX6319	5	VCC	-	-	-	-	2	-	-
U3	MAX6816	4	VCC	-	-	-	-	1	-	-
U4	MAX6816	4	VCC	-	-	-	-	1	-	-
U5	MAX6816	4	VCC	-	-	-	-	1	-	-
U6	LCX374	20	VCC	-	-	-	-	10	-	-
U7	LCX244	20	VCC	-	-	-	-	10	-	-
U8	LCX245	20	VCC	-	-	-	-	10	-	-
U9	LCX374	20	VCC	-	-	-	-	10	-	-
U10	LCX244	20	VCC	-	-	-	-	10	-	-
U11	LCX245	20	VCC	-	-	-	-	10	-	-
U12	LCX374	20	VCC	-	-	-	-	10	-	-
U13	LCX244	20	VCC	-	-	-	-	10	-	-
U14	NC7SZ00	5	VCC	-	-	-	-	3	-	-
U15	LCX244	20	VCC	-	-	-	-	10	-	-
U16	LT1016	-	-	1	VCC	4	VEE	6	-	-
U17	MAX3221E	15	VCC	-	-	-	-	14	-	-
U18	M4A3-32/32	16, 38	VCC	-	-	-	-	6, 17, 26, , 28, 39	-	-
U19	IDT70V24	12, 17, 88	VCC	-	-	-	-	12, 17, 88	-	1-4, 22-25, 43, 51-54, 72-75, 82
U20	LCX245	20	VCC	-	-	-	-	10	-	-
U21	LCX245	20	VCC	-	-	-	-	10	-	-
U22	LCX245	20	VCC	-	-	-	-	10	-	-
U23	LCX245	20	VCC	-	-	-	-	10	-	-
U24	LCX541	20	VCC	-	-	-	-	10	-	-
U25	LCX541	20	VCC	-	-	-	-	10	-	-
U26	LCX541	20	VCC	-	-	-	-	10	-	-
U27	LCX541	20	VCC	-	-	-	-	10	-	-
U28	MPC823E	E5-E12, F5, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L12, M5-M12	VDDH	-	-	-	-	F6-F11, G6-G11, H6-H11, J6-J11, K6-K11, L6-L11	-	A16, C1, C6, E14, J13, N9, N13, P1, P10
U29	NC7SZ00	5	VCC	-	-	-	-	3	-	-
U30	AT49BV1614	37	VCC	-	-	-	-	27, 46	-	-
U31	AT49BV1614	37	VCC	-	-	-	-	27, 46	-	-
U32	AT49BV1614	37	VCC	-	-	-	-	27, 46	-	-
U33	AT49BV1614	37	VCC	-	-	-	-	27, 46	-	-
U34	KER4016V	11, 33	VCC	-	-	-	-	VSS: 12, 34	-	-
U35	KER4016V	11, 33	VCC	-	-	-	-	VSS: 12, 34	-	-
U36	LCX244	20	VCC	-	-	-	-	10	-	-
U37	LCX244	20	VCC	-	-	-	-	10	-	-
U38	NC7SZ125	5	VCC	-	-	-	-	3	-	-
U39	SG-8002JA	4	VDD	-	-	-	-	2	-	-
U40	NC7SZ08	5	VCC	-	-	-	-	3	-	-
U41	NC7SZ125	5	VCC	-	-	-	-	3	-	-
U42	NC7SZ125	5	VCC	-	-	-	-	3	-	-
U43	CBT16233	14, 43	VCC	-	-	-	-	13, 44	-	-
U44	U4564163	1, 14, 27	VDD	-	-	-	-	VSSQ: 5, 12, 46, 52 VSS: 28, 41, 54	-	36, 40
U45	U4564163	1, 14, 27	VCC	-	-	-	-	VSSQ: 5, 12, 46, 52 VSS: 28, 41, 54	-	36, 40
U46	SED1355	12, 33, 55, 72, 97, 109	VDD	-	-	-	-	VSS: 14, 34, 50, 63, 78, 87, 96, 110	98, 105	-
U47	SG-8002JA	4	VDD	-	-	-	-	2	-	-
U48	KM416V1004C	1, 6, 22	VCC	-	-	-	-	VSS: 23, 39, 44	-	11, 12, 13, 33, 34
TRUE U50	NC7SZ125	5	VCC	-	-	-	-	3	-	-
U51	NC7SZ125	5	VCC	-	-	-	-	3	-	-
U52	QS5925	4, 16	VCCQ VCCN	-	-	-	-	3, 10, 15	-	-

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

REFERENCE DESIGNATIONS	
HIGHEST NUMBER USED	NOT USED
C130	C121, C120, C122, C123
D3	
J17	
JP3	JP2
L7	
Q5	
R276	R4, R5, R88, R121, R125, R134
U53	U3, U49
S3	S1

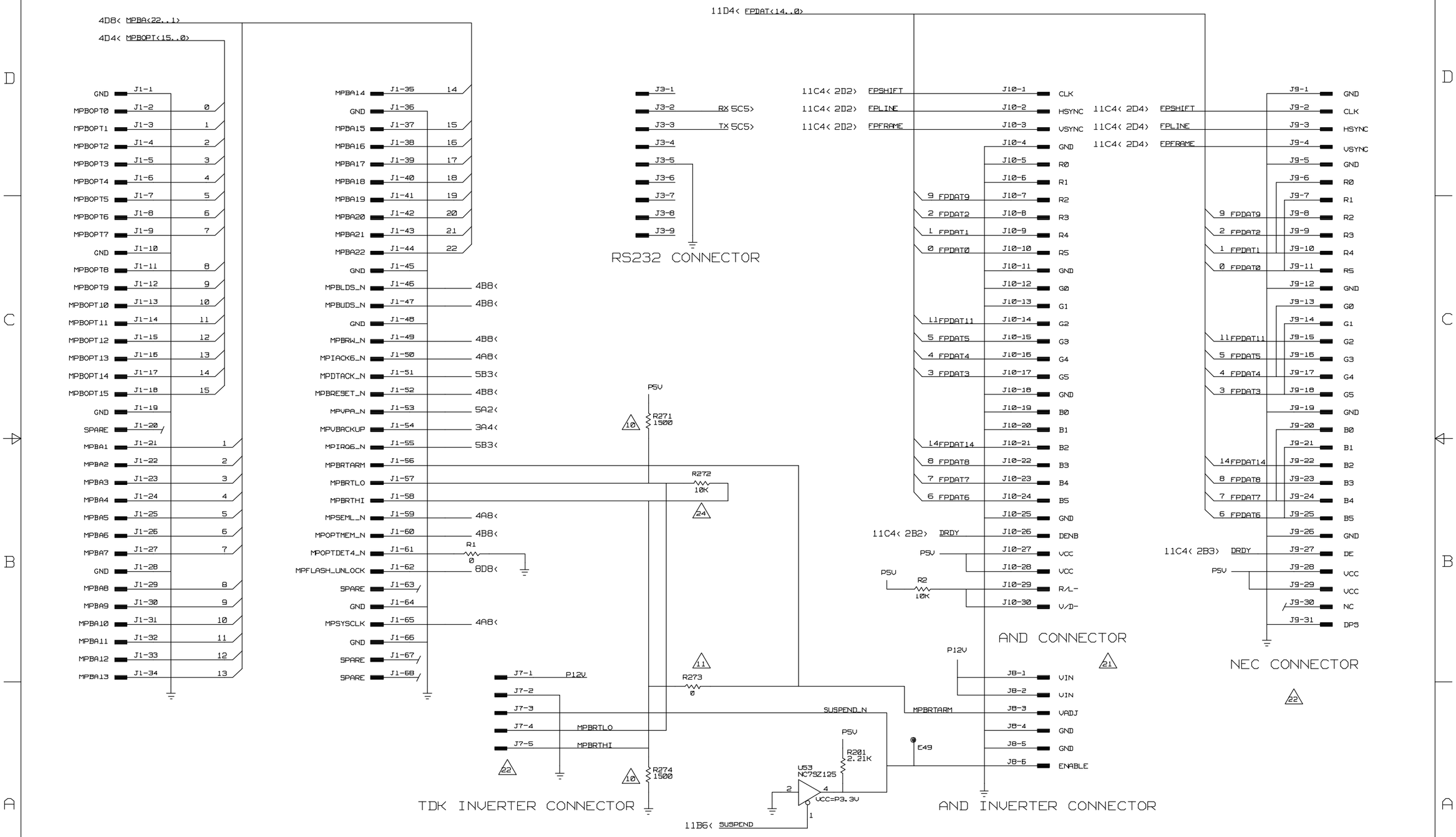
ALL SHEETS ARE THE SAME REVISION STATUS

		CONTR
		ISS RN B35550-484(-)00-8-8
		APPROVALS
		DWN P. SCOTT 00-03-03
		CHKR
		QA T.DAVIS 00-08-08
		MATL W.MCDONALD 00-08-08
01-P57140J	COCHISE	MFG B.WATTS 00-08-08
NEXT ASSY	USED ON	ENG A.GATTO 00-08-08
APPLICATION		CUST

MOTOROLA, INC.
SCOTTSDALE, ARIZONA 85252-1417

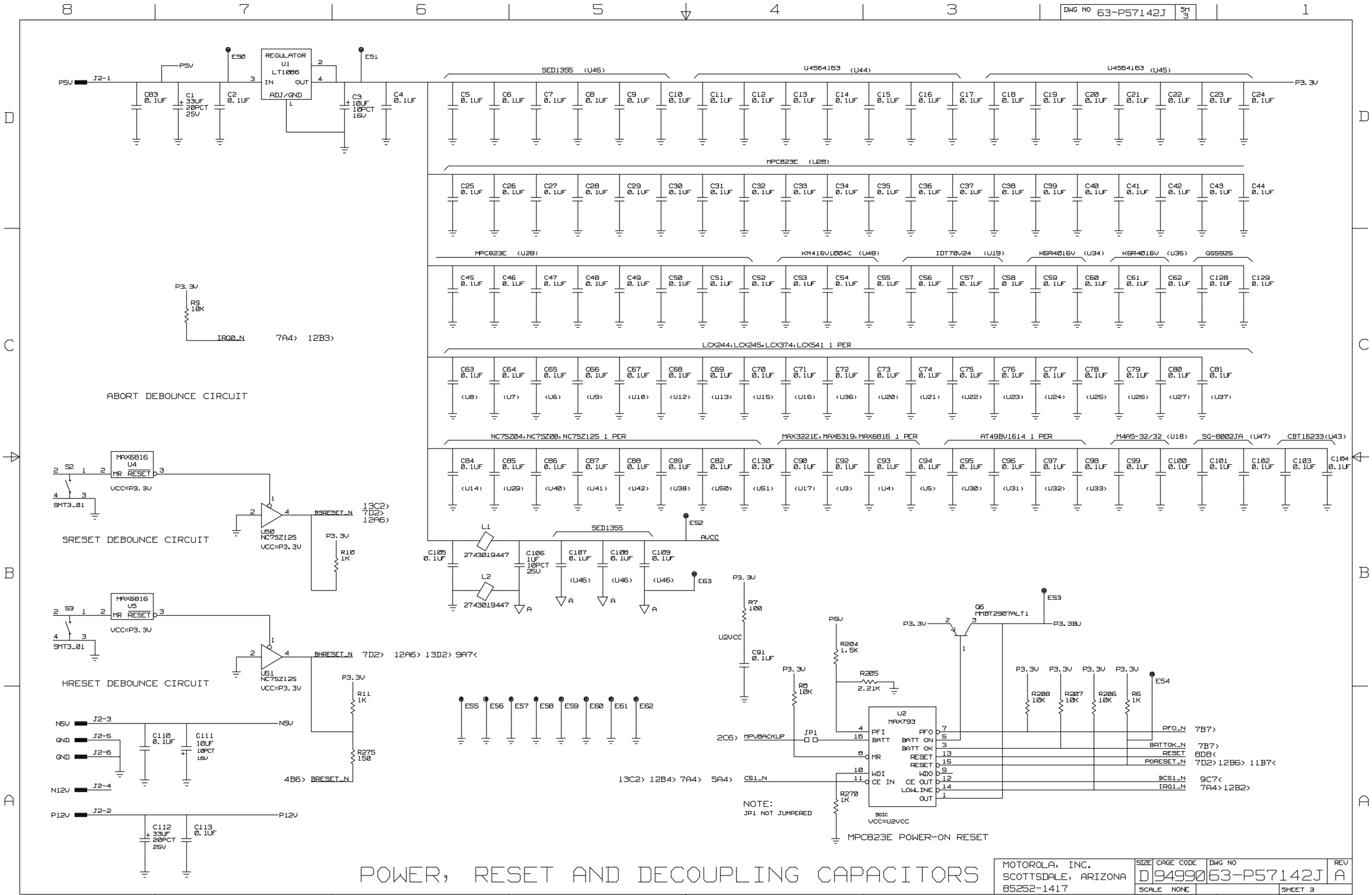
TITLE
SCHEMATIC DIAGRAM
DISPLAY PROCESSOR

SIZE	CAGE CODE	DWG NO
D	94990	63-P57142J
SCALE NONE		SHEET 1 OF 14



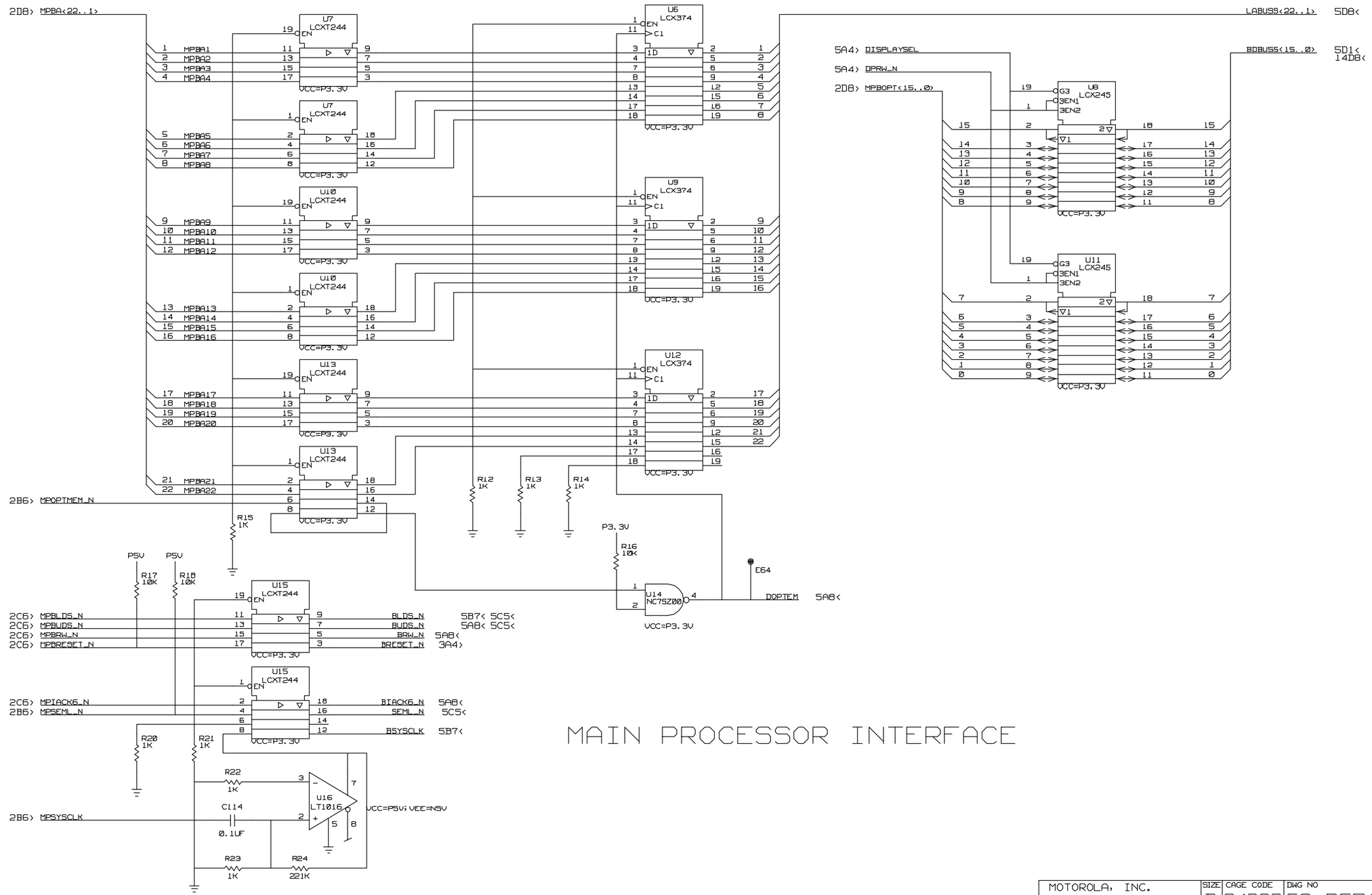
MAIN AND DISPLAY CONNECTORS

MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57142J	REV A
	SCALE NONE		SHEET 2	



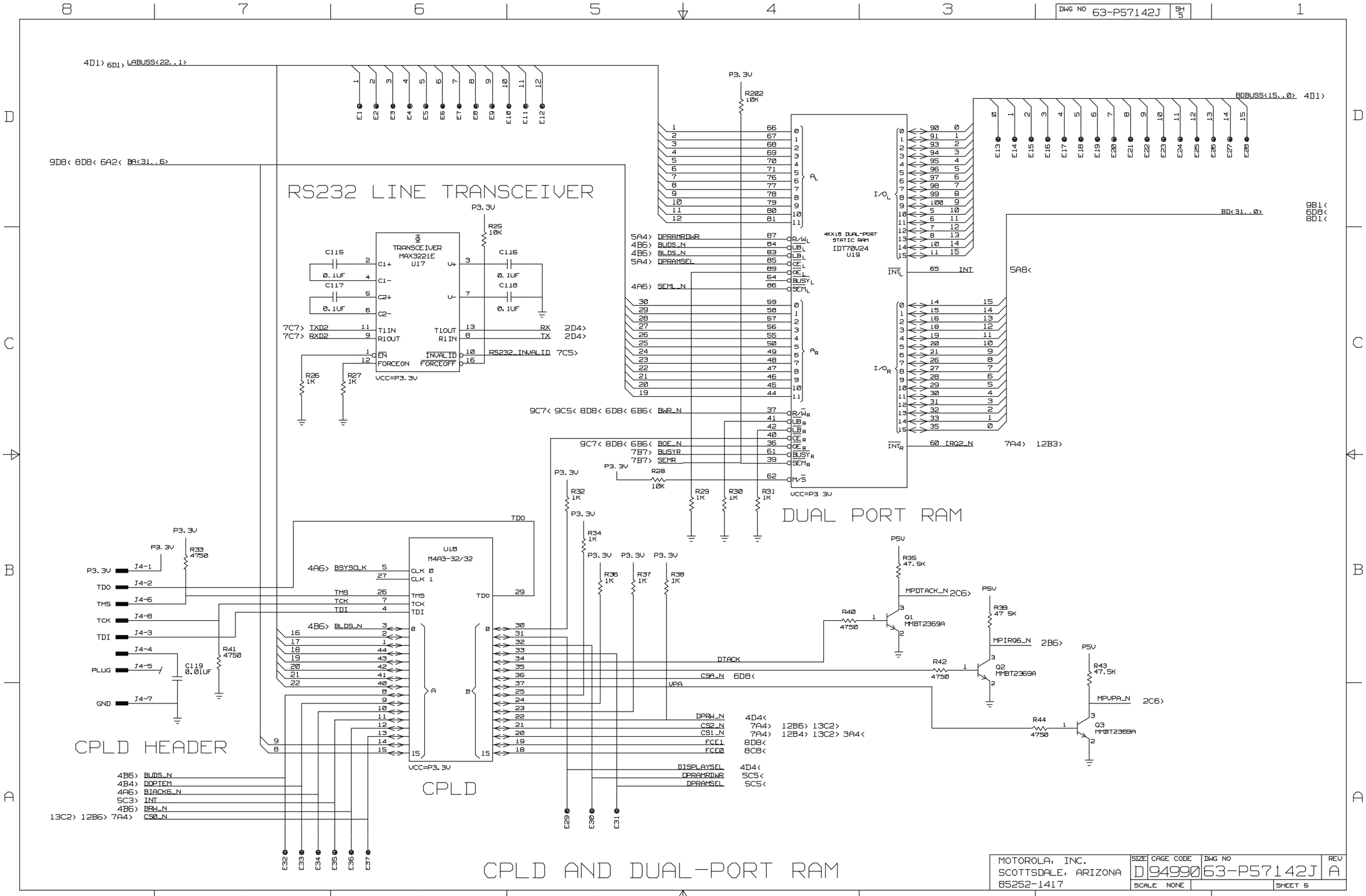
POWER, RESET AND DECOUPLING CAPACITORS

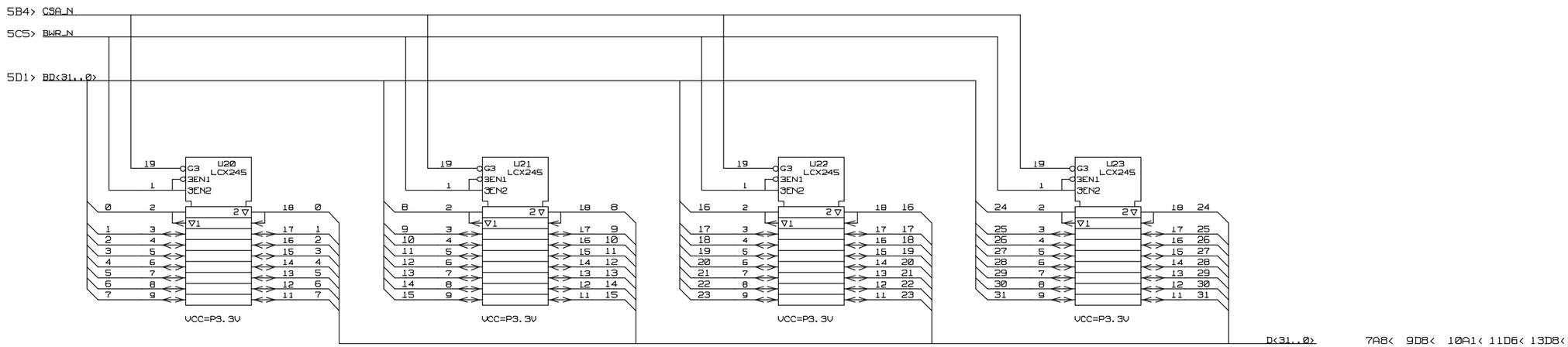
MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57142J	REV A
	SCALE NONE		SHEET 3	



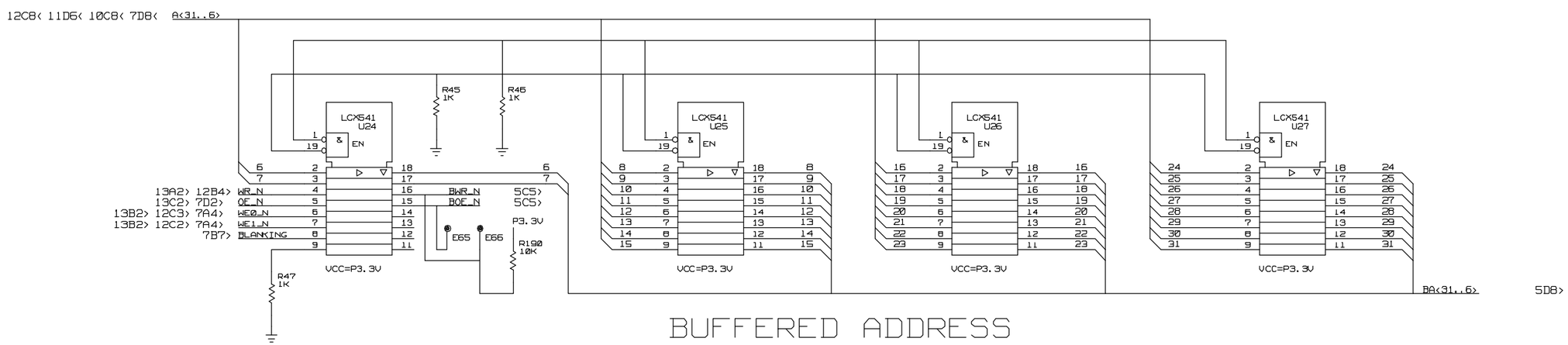
MAIN PROCESSOR INTERFACE

MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57142J	REV A
	SCALE NONE		SHEET 4	


DWG NO 63-P57142J
SH 5
RS232 LINE TRANSCEIVER
TRANSCEIVER MAX3221E U17
VCC=P3.3V
DUAL PORT RAM
4KX16 DUAL-PORT STATIC RAM IDT70V24 U19
VCC=P3 3V
CPLD HEADER
U18 M4A3-32/32
CPLD
CPLD AND DUAL-PORT RAM
MOTOROLA, INC.
SCOTTSDALE, ARIZONA
85252-1417
SIZE D
CAGE CODE 94990
DWG NO 63-P57142J
REV A
SCALE NONE
SHEET 5



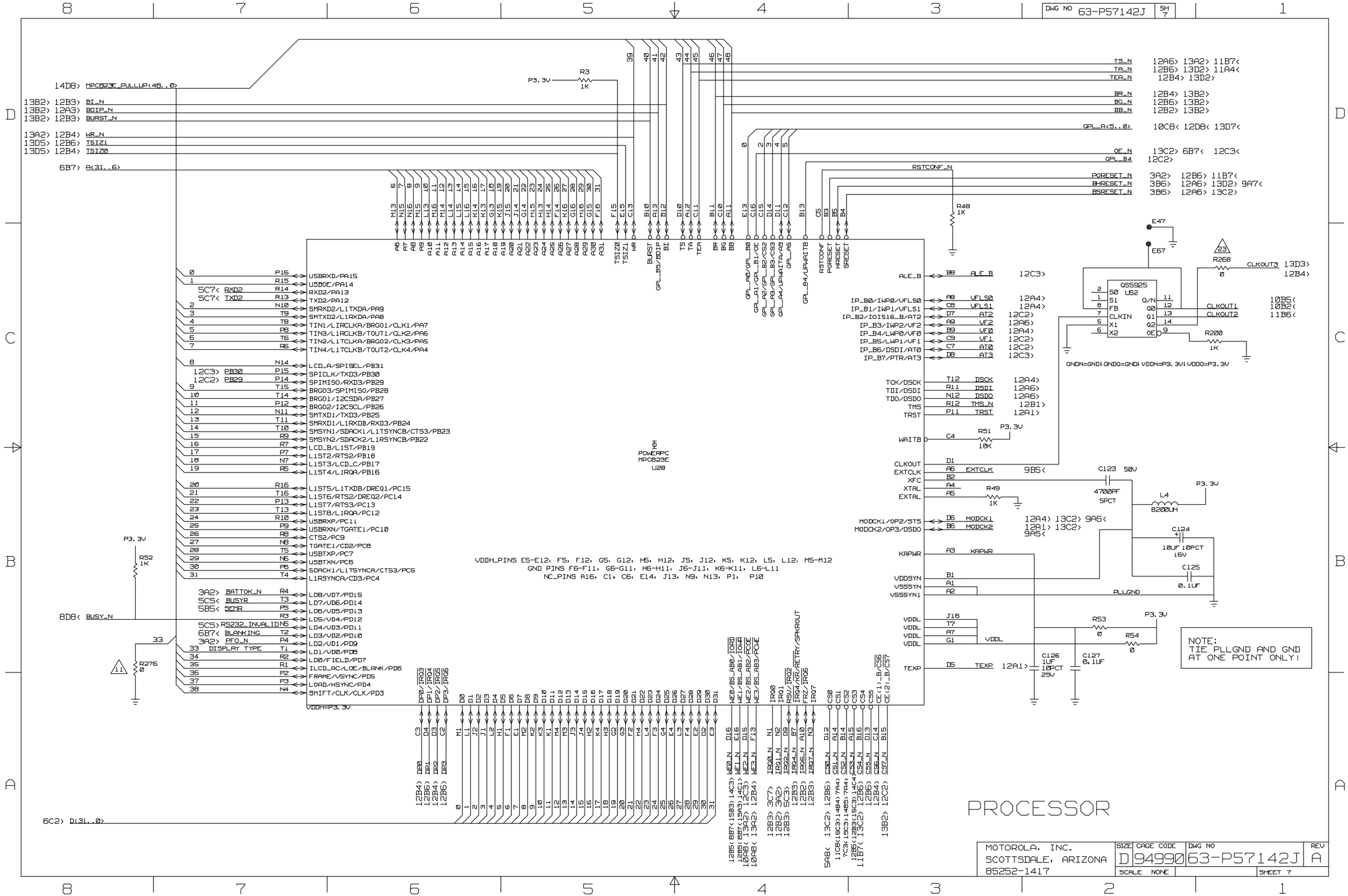
BUFFERED DATA

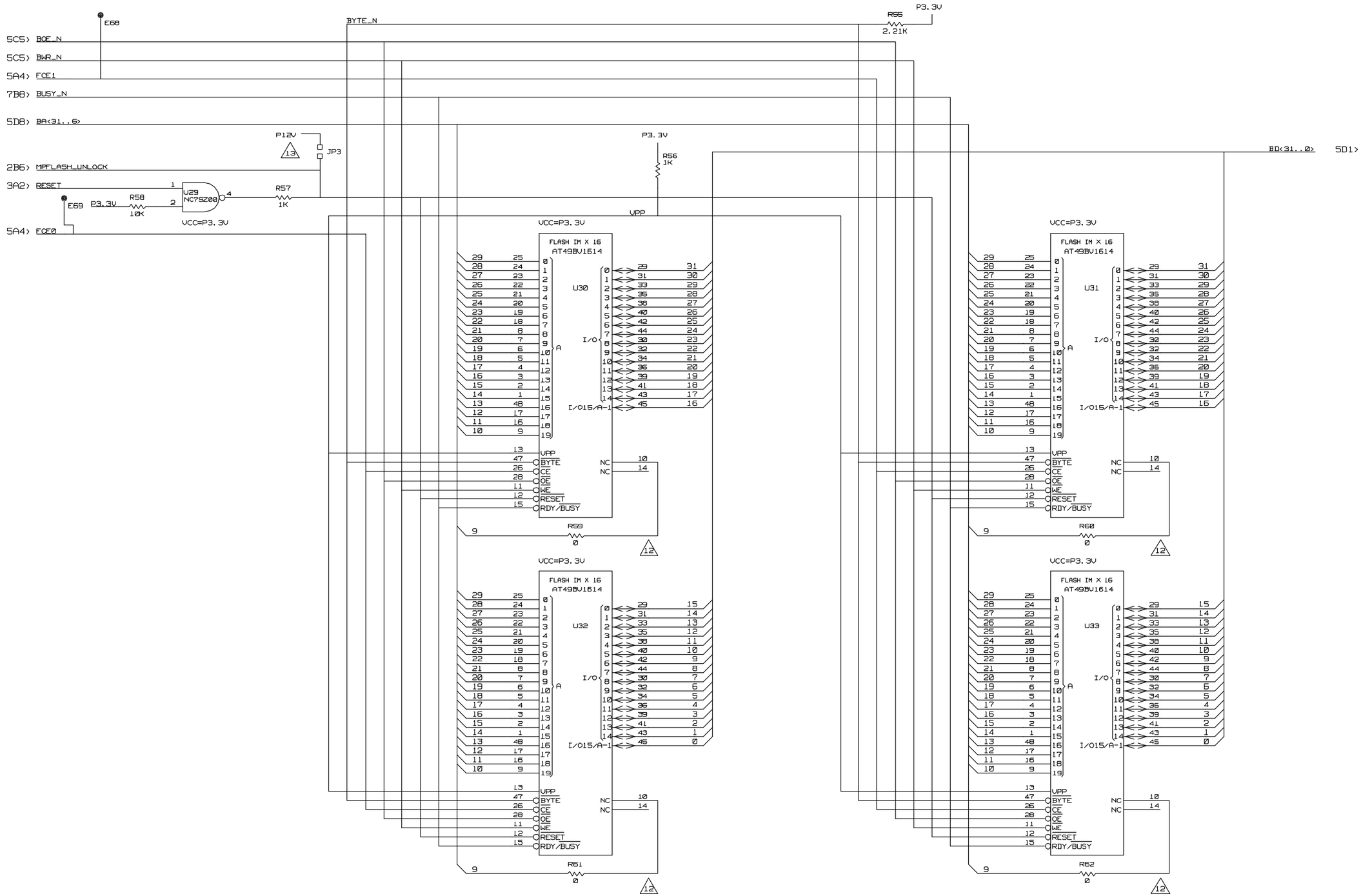


BUFFERED ADDRESS

BUFFERED DATA AND ADDRESS INTERFACE

MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57142J	REV A
	SCALE NONE			SHEET 6

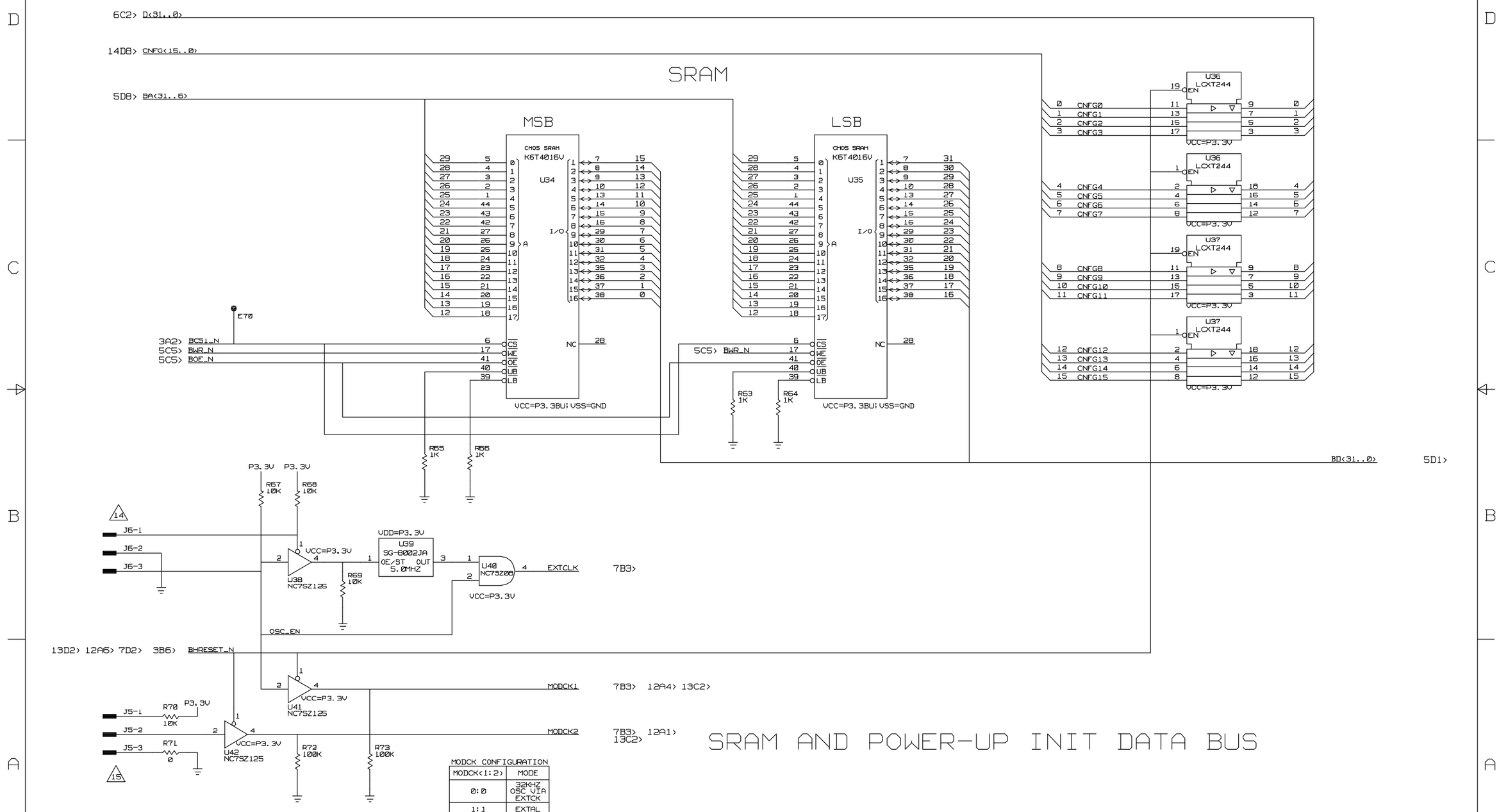

DWG NO 63-P57142J
SH 7
POWERPC
MPC823E
U28
VDDH_PINS E5-E12, F5, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L12, M5-M12
GND PINS F6-F11, G6-G11, H6-H11, J6-J11, K6-K11, L6-L11
NC_PINS A16, C1, C6, E14, J13, N9, N13, P1, P10
Q55925 U52
GNDN=GND; GNDO=GND; VDDN=P3.3V; VDDO=P3.3V
NOTE:
TIE PLLGND AND GND
AT ONE POINT ONLY!
PROCESSOR
MOTOROLA, INC.
SCOTTSDALE, ARIZONA
85252-1417
SIZE D
CAGE CODE 94990
DWG NO 63-P57142J
REV A
SCALE NONE
SHEET 7



FLASH MEMORY

MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57142J	REV A
	SCALE NONE		SHEET 8	

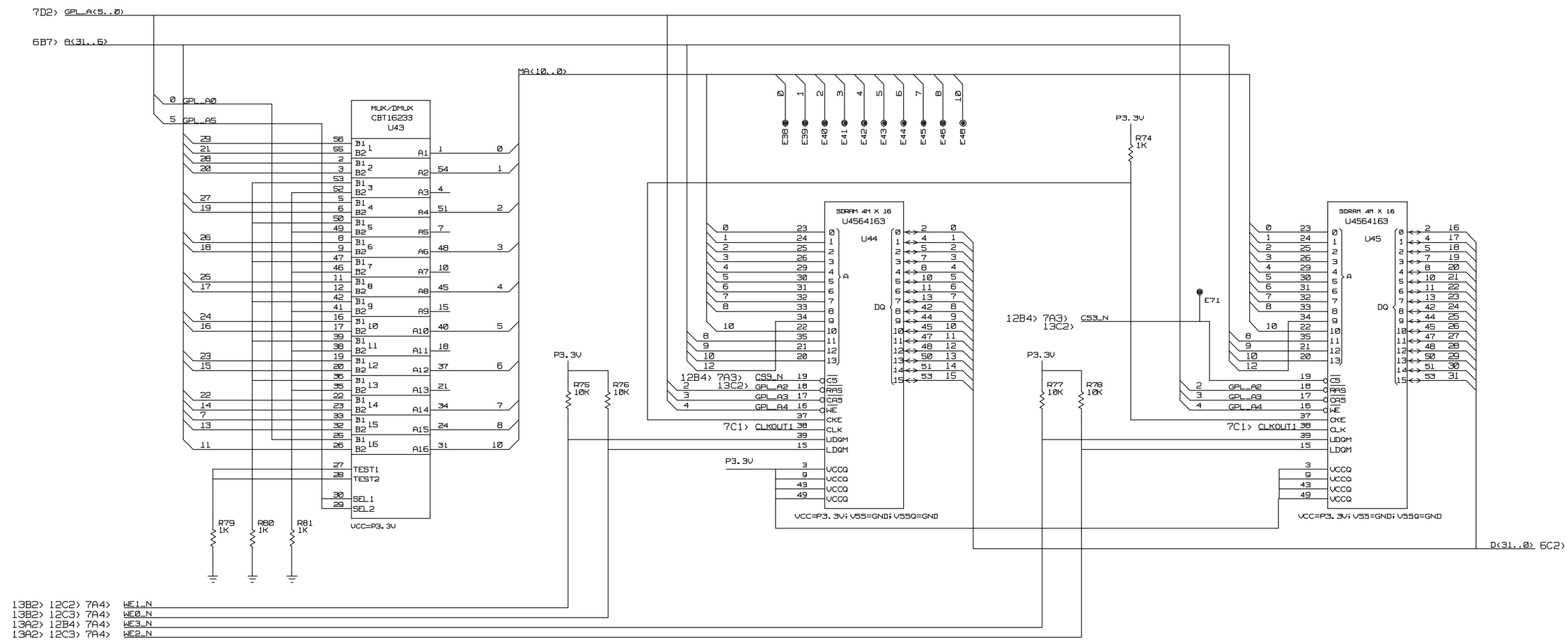
NOTE:
USE EITHER 100K PULL-UP RESISTOR OR 1K OHM PULL-DOWN RESISTOR TO CONFIGURE PROCESSOR ON POWER UP



MODCK CONFIGURATION

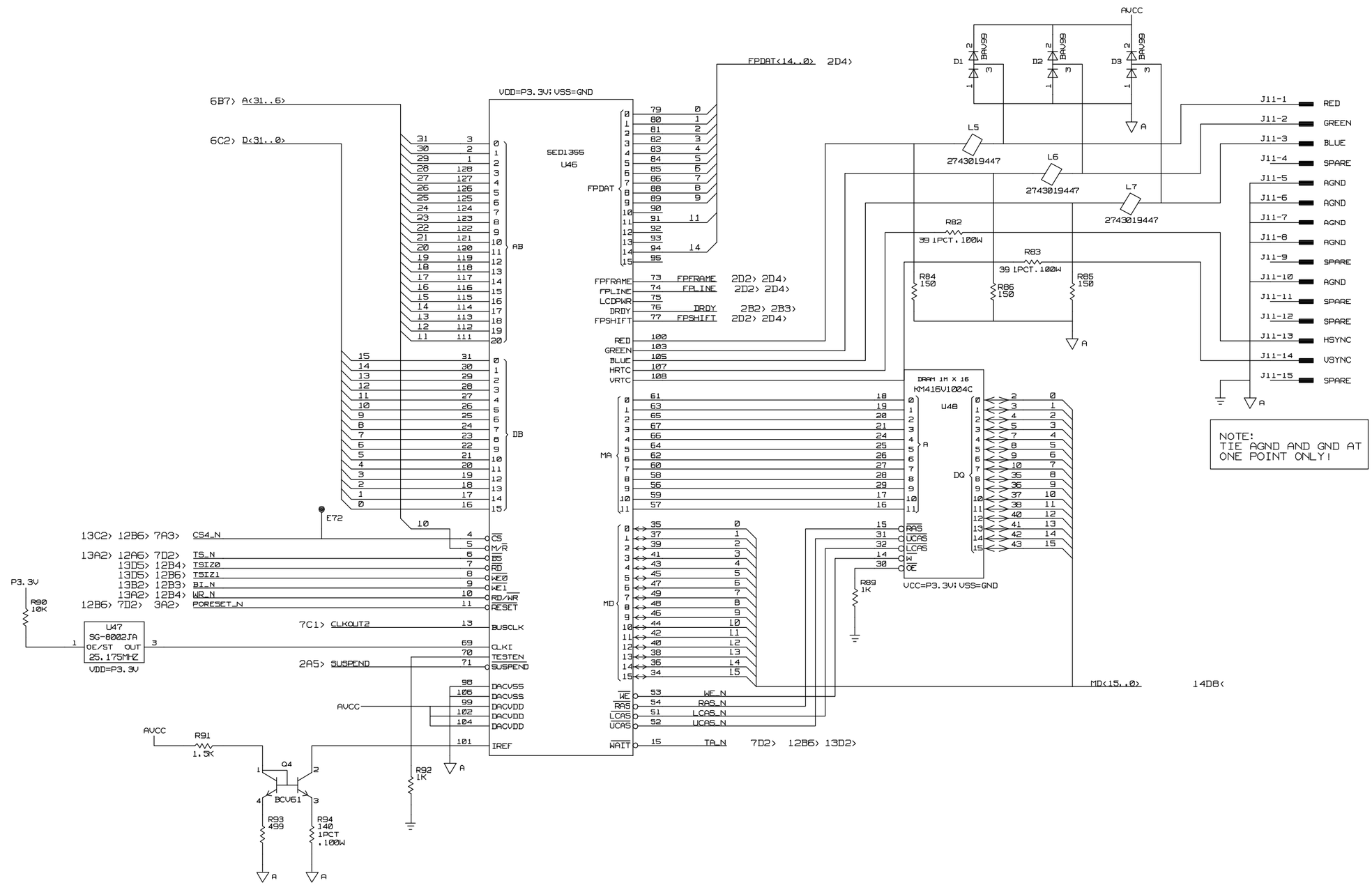
MODCK<1:2>	MODE
0:0	32KHZ OSC VIA EXTCK
1:1	EXTAL

SRAM AND POWER-UP INIT DATA BUS



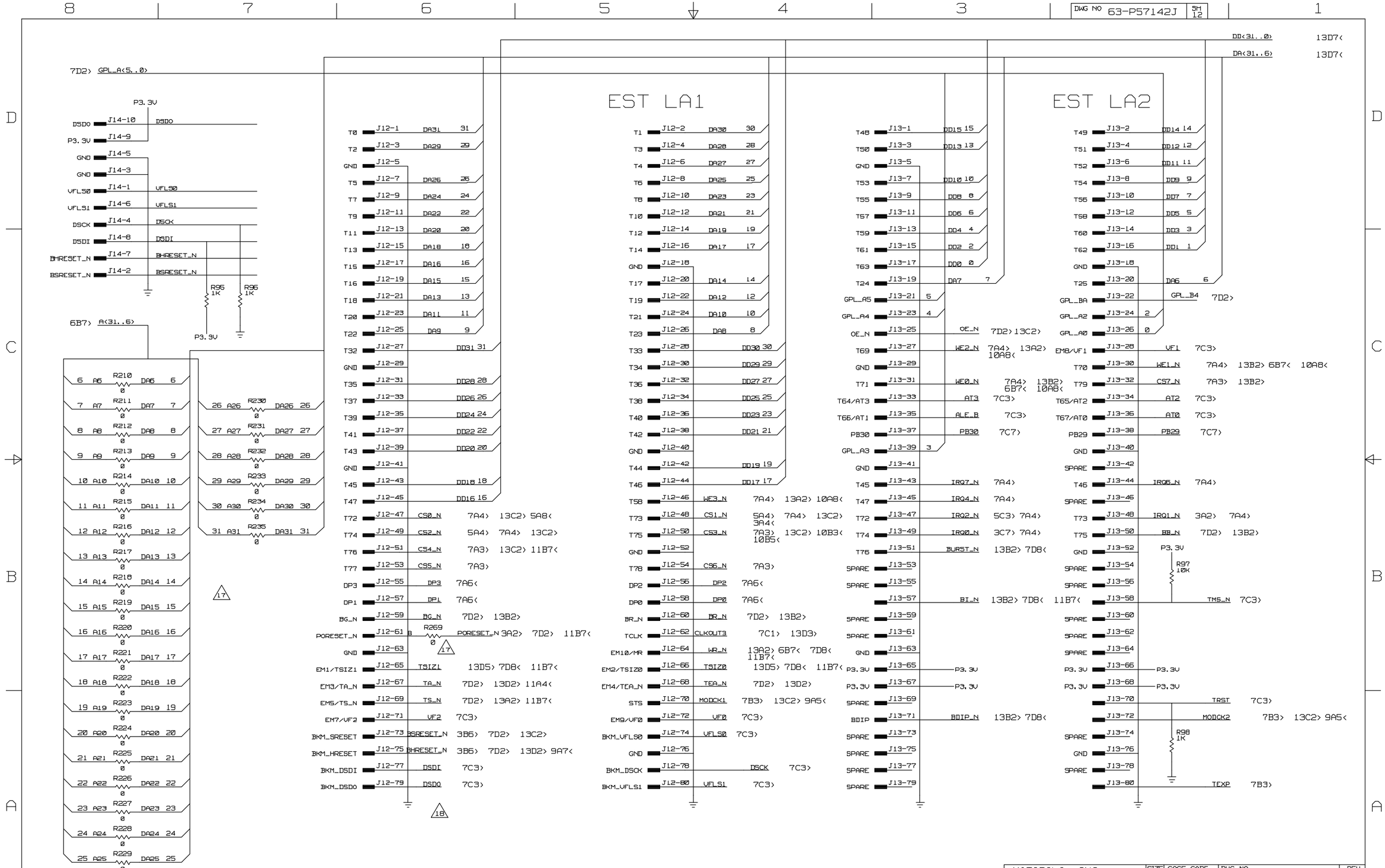
SDRAM

MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57142J	REV A
	SCALE NONE			SHEET 10



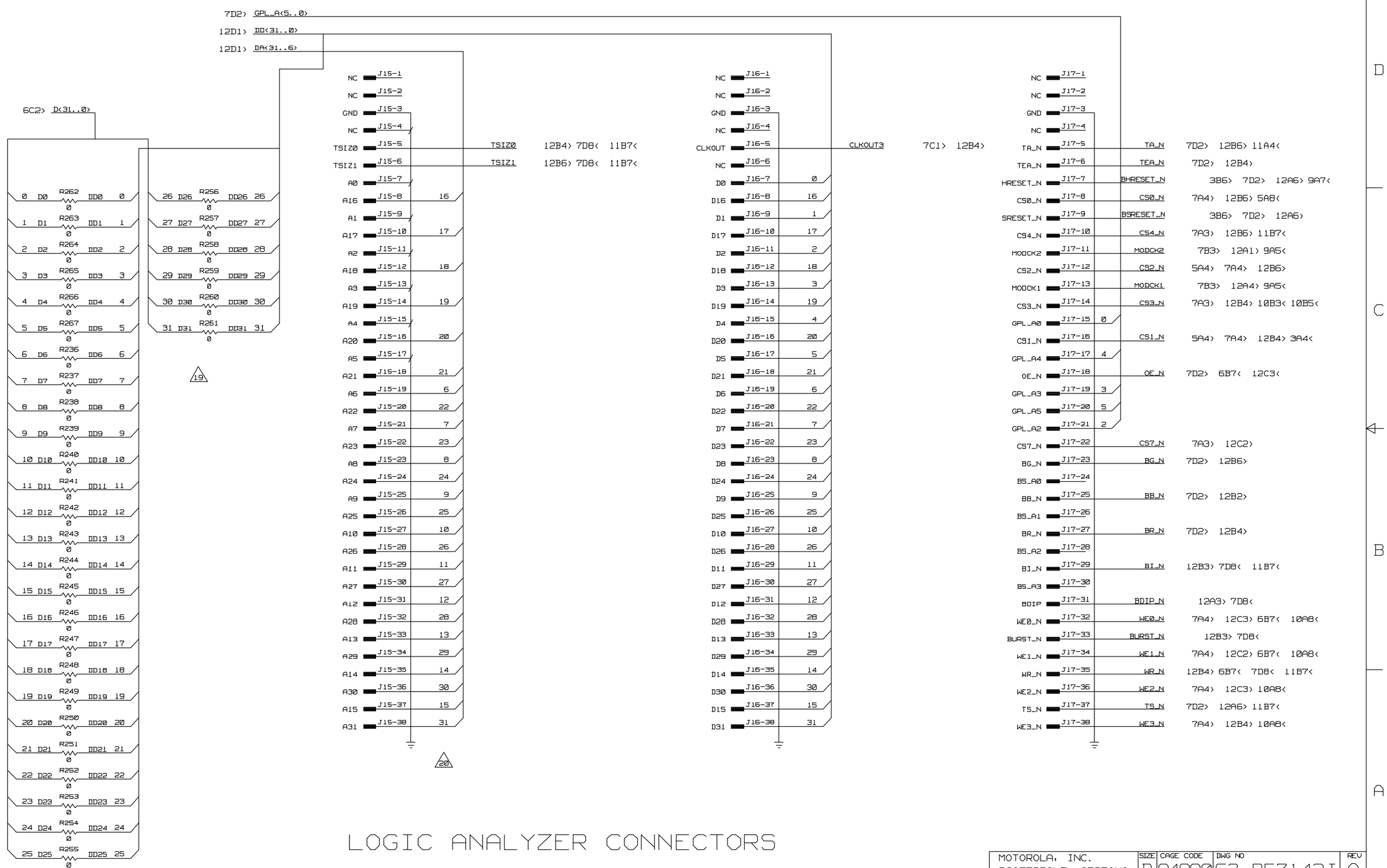
LCD CONTROLLER

MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57142J	REV A
	SCALE NONE		SHEET 11	



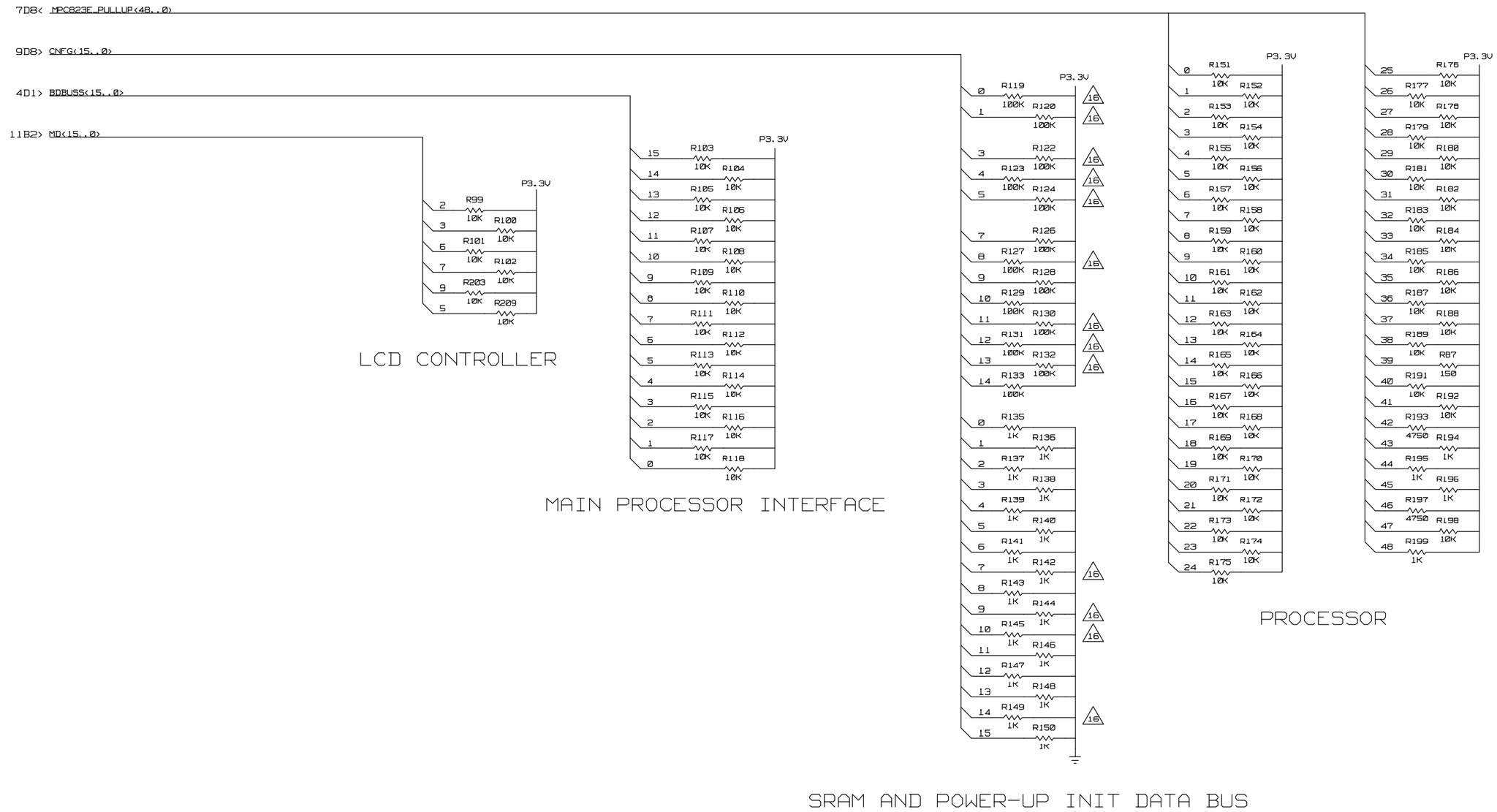
EST EMULATOR CONNECTORS

MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57142J	REV A
	SCALE NONE			SHEET 12



LOGIC ANALYZER CONNECTORS

MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57142J	REV A
	SCALE NONE		SHEET 13	



PULL-UP AND PULL-DOWN RESISTORS

MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57142J	REV A
	SCALE NONE			SHEET 14

Appendix A
INTERFACE FILTER
PHASE DEMOD BOARD

TABLE OF CONTENTS

Return to main TABLE OF CONTENTS

Go to Appendix B

Appendix A INTERFACE FILTER PHASE DEMOD BOARD

A.1 GENERAL DESCRIPTION

The Interface Filter/Phase Demod (IF/PD) board is an option to the basic Analyzer and is installed on the Interface Module. Module designations are.

A12: Interface Module
A12A1: Interface Filter/Phase Demod Board

The IF/PD board provides the Analyzer with three optional DVM characteristics for audio tests, and the capability for converting FM demodulation to phase demodulation.

A.2 SIGNALS SUMMARY

A.2A Signal Descriptions

A.2A.1 P1

METER is the DVM input at the Analyzer's Front Panel, named 'Metering Input' at the Interface Module.

A.2A.2 Connections to/from Interface Module

*CCITT FILT EN** input enables and selects the routing of the DVM FROM RANGE signal from the Interface Module (interrupted by track cut) through the CCITT filter on this module.

*C-MSG FILT EN** is an input to the IF/PD board. It enables and selects the routing of the DVM FROM RANGE signal from the Interface Module through the C-Message filter on the IF/PD board.

DVM FROM RANGE Input is the DVM FROM RANGE signal on the Interface Module, and is from the source side of the track cut of the signal line.

DVM FROM RANGE Output is either a filtered version of the DVM FROM RANGE INPUT (using the C-Message or CCITT filter) or a unity gain unfiltered version. This output is connected to the return side of the track cut of the signal line on the Interface Module.

*PHASE DEMOD EN** enables and selects the routing of the SQUELCHED DEMOD input.

SQUELCHED DEMOD Input is the squelched demodulated audio from the receiver.

SQUELCHED DEMOD Output is either the squelched demodulated audio from the receiver put through a de-emphasis filter yielding a phase demodulated signal, or a unity gain unfiltered version.

SCOPE SQUELCHED PHASE DEMOD output is a resistively divided output of SQUELCHED DEMOD, scaled for use by the Scope Range circuit on the Interface Module.

600Ω OVERLOAD output, when high, indicates that the DVM input voltage has exceeded a predetermined maximum level for the 600Ω load. This latched output resets when the reset softkey is pressed in the special function screen.

600Ω ENABLE input enables the connection of a 600Ω resistance to the Front Panel METER INPUT of the Analyzer. The 600Ω resistance is placed in parallel with the lMΩ input impedance of the Analyzer's METER INPUT.

A.2B Connector Descriptions

A.2B.1 P1, METER

See par. A.2A.l.

A.2B.2 Connections to Interface Module

The IF/PD board and the Interface Module are connected together through a group of soldered wires. The 'E' numbers here indicate the connecting pad on the IF/PD board.

El	C-MSG FILT EN*
E2	600Ω OVERLOAD
E3	DVM FROM RANGE output
E4	DVM FROM RANGE input
E5	600Ω ENABLE
E6	+5V
E7	+12V
E8	-12V
E9	CCITT FILT EN*
E10	PHASE DEMOD EN*
Ell	SQUELCHED DEMOD input
E12	SQUELCHED DEMOD output
E13	SCOPE SQUELCHED PHASE DEMOD

Connections at the Interface Module are as follows:

El	U75-5 (PI-37)
E2	U63-13
E3	track cut
E4	track cut
E5	U75-15 (Pl-40)
E6	+5V
E7	+12V
E8	- 12V
E9	U75-12 (Pl-41)
E10	U78-2 (PI-75)
Ell	U47-10 (P1-107)
E12	U47-4
E13	U32-10

A.3 BLOCK DIAGRAM DESCRIPTION

The IF/PD board contains circuitry for implementing the following:

- a selectable 600Ω input impedance to the DVM.
- a selectable C-Message or CCITT filter in series with the selectable 1KHz notch filter located on the Interface Module.
- a de-emphasis filter to provide phase demodulation when coupled with the FM demodulator of the Analyzer.

A.4 DETAILED DESCRIPTION

A.4.1 600Ω Load

The IF/PD board detects a positive and negative input voltage of greater than 25V (±3V) peak at the METER input. If this occurs while the 600Ω load is enabled, the 600Ω OVERLOAD output is latched high, which disconnects the 600Ω load.

A.4.2 C-Message Filter

When the C-MSG FILT EN* control line is set low, the DVM FROM RANGE Input signal is routed through a bandpass audio filter to the DVM FROM RANGE Output, where it is used on the Interface Module for SINAD, External Distortion, and AC DVM readings.

The first three stages provide low pass filtering and gain setting, while the remaining stages provide high pass filtering. The circuit is adjusted for 0dB (unity gain) at 1KHz).

A.4.3 CCITT Filter

When the CCITT FILT EN* control line is set low, the DVM FROM RANGE Input signal is routed through a bandpass audio filter to the DVM FROM RANGE Output, where it is used on the Interface Module for SINAD, External Distortion, and AC DVM readings.

The first three stages provide low pass filtering and gain setting, while the remaining stages provide high pass filtering. The circuit is adjusted for 0dB (unity gain) at 800Hz.

A.4.4 Phase Demod De-Emphasis Filter

When the PHASE DEMOD EN* control line is set low, SQUELCHED DEMOD is routed through the phase demod de-emphasis filter to provide phase demodulation in the 100Hz to 3KHz range.

The gain is adjusted at the system level by receiving an RF signal modulated with a lKHz tone at 4KHz deviation, equaling 4.0 radians.

The output is routed to the DVM and Scope circuits on the Interface Module via the SQUELCHED DEMOD output and SCOPE SQUELCHED PHASE DEMOD signals, respectively. The SQUELCHED DEMOD output is also routed to the DEMOD OUT to Front Panel circuitry so that frequency or phase demodulation is available at the front panel, depending on the selection.

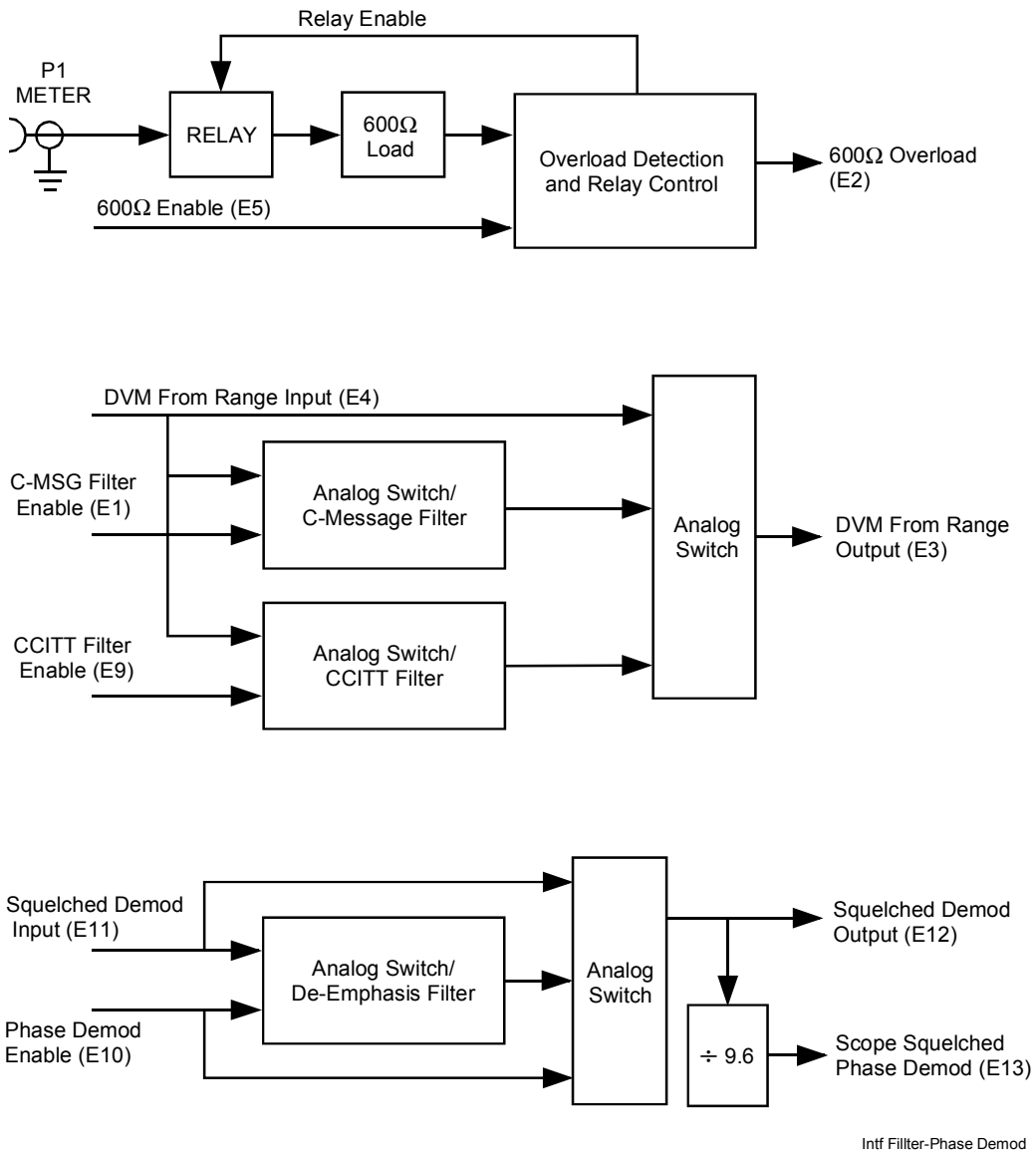


Fig. A.5 Interface Filter/Phase Demod Board, Block Diagram

A.6 CALIBRATION/ALIGNMENT

Ensure that the Analyzer has been warmed up to operating temperature before performing any adjustments.

All other general statements concerning calibration and alignment found in the Calibration/Alignment section of this manual (Section 3) are applicable to this section and will not be repeated here.

A.6.1 General

Use an R26XX as a hot bed, with the Interface Module on an extender card. Extenders for the Ribbon cables, DVM input, and Front Panel connections to the Interface Module will be necessary also.

A.6.2 C-Message Filter

1. At the R26XX Front Panel, connect the R26XX MOD OUT output to the R-2600 DVM input.

2. Put the R26XX into wideband monitor mode with the audio generator set for TONE A, continuous, 1KHz, and output at 1.0V.

3. Set the R26XX meter display for AC VOLTS. Note the reading.

4. Select C-MSG filter option at the bottom of the special function screen (accessed through SPF key).

5. Adjust R8 on the Interface Filter Phase Demod board so the value in the AC VOLTS display area is within +/- 1mV of the reading taken in step 3.

A.6.3 CCITT Filter

1. At the R26XX Front Panel, connect the R26XX MOD OUT output to the R26XX DVM input.

2. Put the R26XX into wideband monitor mode with the audio generator set for TONE A, continuous, 800Hz, and output at 1.0V.

3. Set the R26XX meter display for AC VOLTS. Note the reading.

4. Select CCITT filter option at the bottom of the special function screen (accessed through SPF key).

5. Adjust R104 on the Interface Filter Phase Demod board so the value in the AC VOLTS display area is within +/- 1mV of the reading taken in step 3.

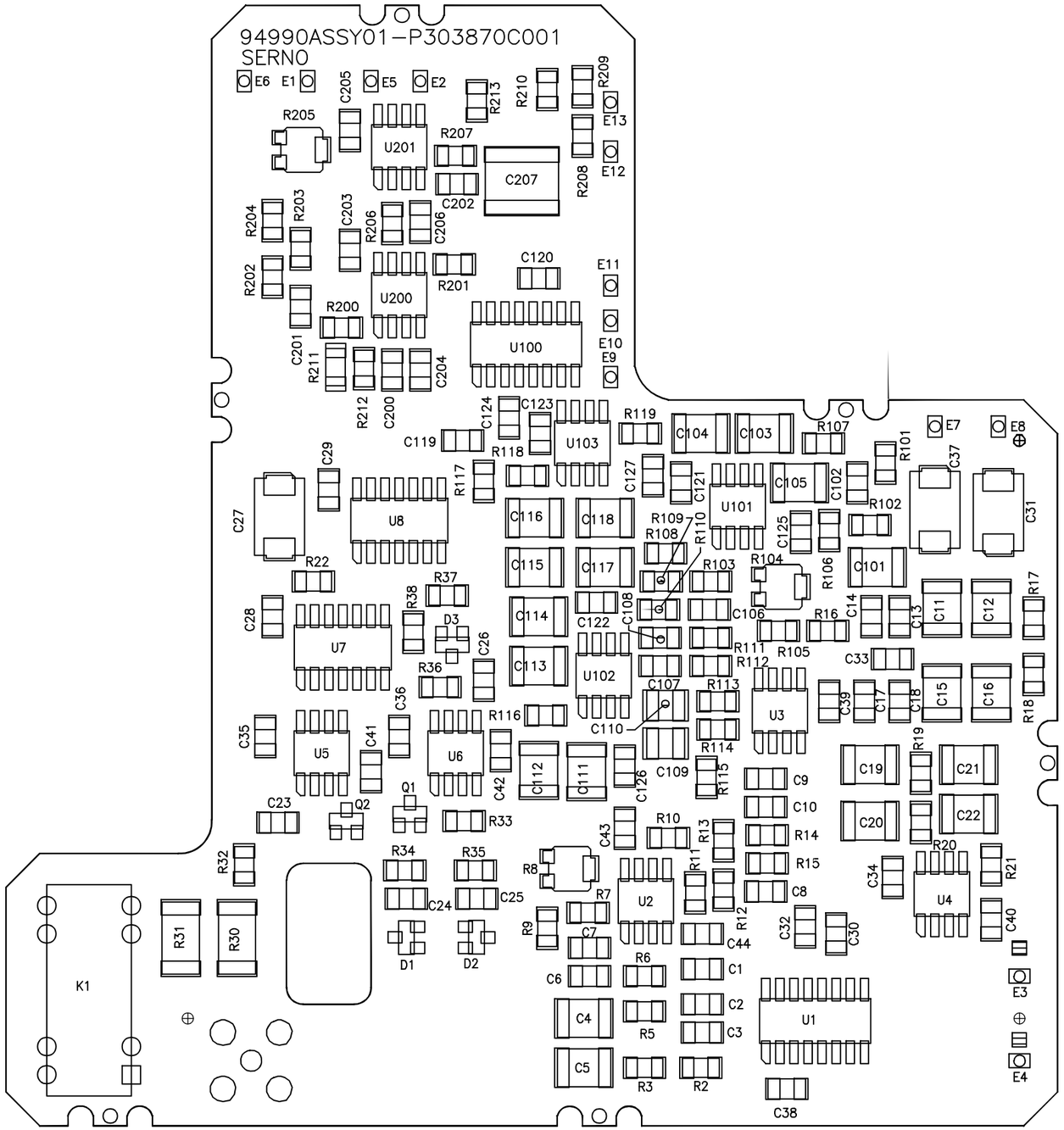
A.6.4 Phase Demod

1. Using an RF signal generator (HP8640 or equivalent) apply a -50dBm signal at 453.0MHz to the Analyzer's antenna port. Modulate the signal at 4KHz deviation with a 1KHz tone.

2. Configure Analyzer for monitor mode at the antenna port with no attenuation, narrow band. Enable the 300Hz high pass and 3KHz low pass filters in the Special Function screen (accessed via SPF key).

3. Select PM and WB at the Analyzer's RF control zone and select RF display in the metering zone.

4. Adjust R205 for 4.00 radians as displayed on the R26XX display.



CAUTION
THIS ASSEMBLY CONTAINS ITEMS
WHICH ARE SUBJECT TO DAMAGE
FROM ELECTROSTATIC DISCHARGE (ESD)

CIRCUIT CARD ASSEMBLY
INTERFACE FILTER / PHASE DEMOD

01-P30870C REV. C

SHEET 1 OF 1

DWG NO	SH
63-P30872C	1

REVISION HISTORY

REV	DESCRIPTION	DATE	APPROVED
B	INITIAL RELEASE		

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH A1.
2. FOR REFERENCE DRAWINGS REFER TO: 01-P30870C ASSEMBLY
3. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE IN OHMS, ± PCT, 1/8 WATT. ALL CAPACITORS ARE IN UF. ALL VOLTAGES ARE DC.
4. TERMINATIONS CODED WITH THE SAME LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
5. DEVICE TYPE NUMBERS AND CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE 1.
6. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH MANUFACTURER. SEE ASSEMBLY PARTS LIST FOR PROPER PART NUMBER.
7. OPTIONAL PART NOT INSTALLED AT THIS TIME.

REFERENCE DESIGNATIONS	
HIGHEST NUMBER USED	NOT USED
C206	C45-C100, C128-C199
D3	
K1	
Q2	
R213	R1, R4, R23-R29, R39-R100, R120-R199
U201	U9-U99, U104-U199

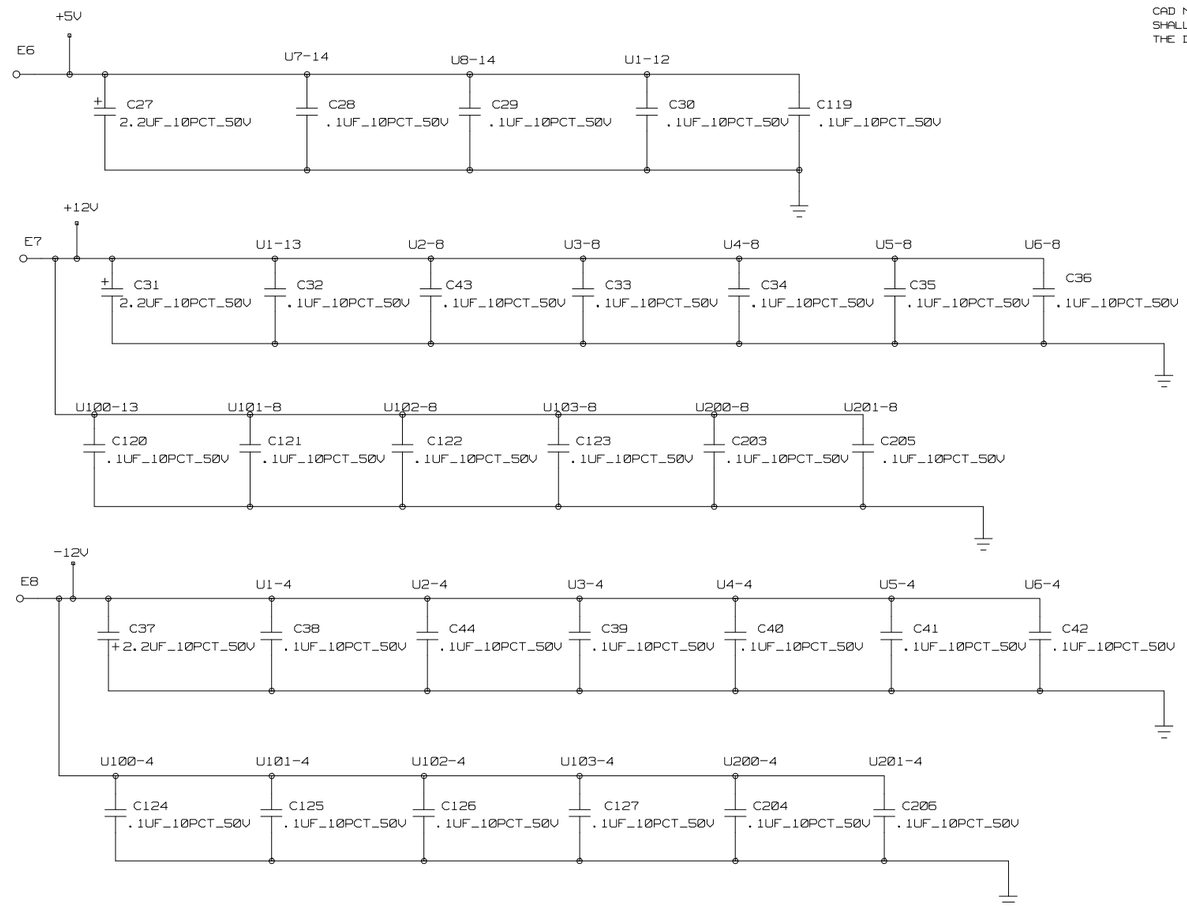
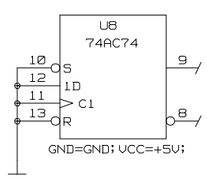


TABLE 1 SEE NOTE 5 AND 6

REF DES	DEVICE TYPE	VCC CONNECTION		GND CONNECTION	NO CONNECTION
		CONN	VOLTS		
U1, U100	DG211CSE	13 12 4	+12V +5V -12V	5	
U2-U4 U101-U103 U200, U201	MC34072D	8 4	+12V -12V		
U5, U6	LM311D	8 4	+12V -12V	1	
U7	74AC00SC	14	+5V	7	
U8	74AC74SC	14	+5V	7	
K1	DL1A05				9, 13

SPARES



ALL SHEETS ARE THE SAME REVISION STATUS

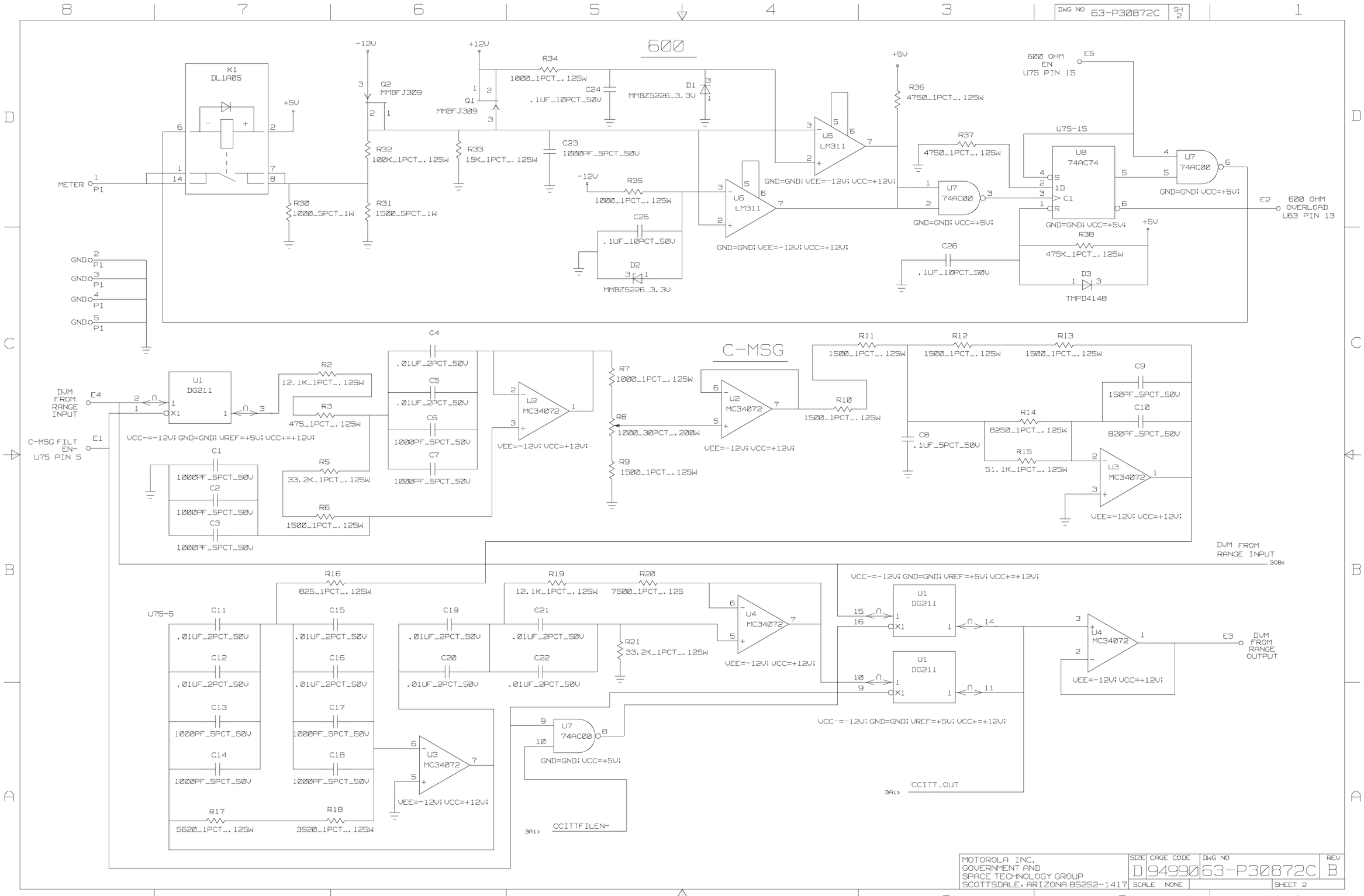
		CONTR	
		ISS B35550-329(B)95-09-26	
		APPROVALS	
		DWN W. R. SCOTT 92-10-10	
		CHKR	
		QA J. MURPHY 95-09-26	
		MATL W. B. MCDONALD 95-09-25	
01-P30870C	COCHISE	MFG S. CASH 95-09-25	
NEXT ASSY	USED ON	ENG A. F. KOESTNER 95-09-21	
APPLICATION		CUST	

MOTOROLA INC.
GOVERNMENT AND SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

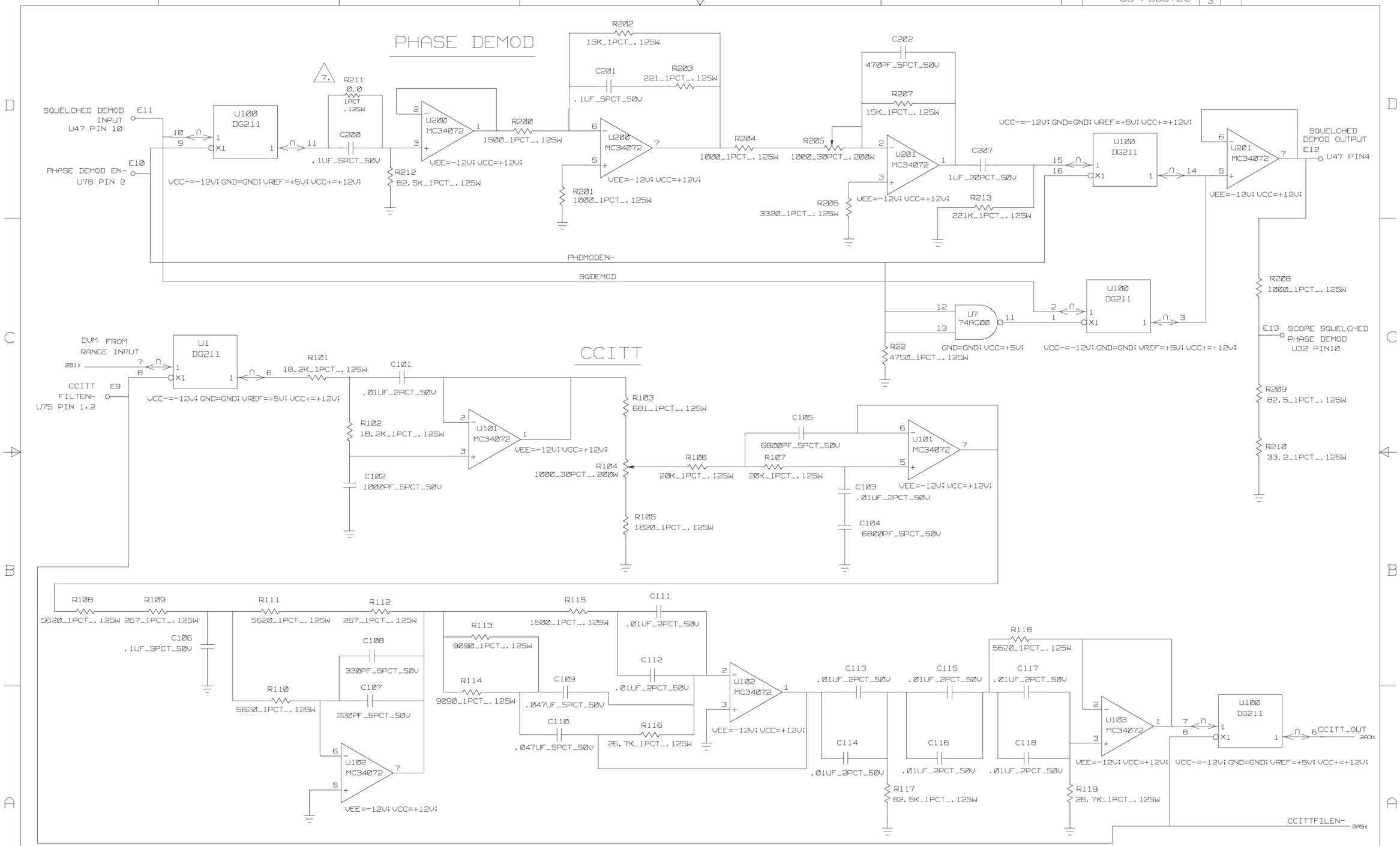
TITLE
SCHEMATIC DIAGRAM
INTERFACE FILTER/
PHASE DEMOD

SIZE	CAGE CODE	DWG NO
D	94990	63-P30872C

SCALE NONE SHEET 1 OF 3



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30872C	REV B
	SCALE NONE		SHEET 2	



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P30872C	REV B
	SCALE NONE		SHEET 3	

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Return to Appendix A

Go to Appendix C

B.1 GENERAL DESCRIPTION

The Battery Pack Assembly is installed on the rear panel of the Analyzer. It can be ordered separately under kit number RPN-4000A. This assembly provides portable power to the Analyzer through the DC power connector. The assembly also routes AC power to the Analyzer, and recharges the batteries when an AC source is connected.

The Battery Pack Assembly contains two 12 volt, 5 Amp-hour batteries, and a regulated charging circuit on a printed circuit board. An AC voltage switch inside the assembly is used to configure the charger for 110Vac or 220Vac operation.

It is recommended that batteries be recharged every five months if the Pack is removed from the unit, or if the unit is not turned on during that period. To recharge, connect the battery pack and turn the unit on for eight or more hours.

B.2 SIGNALS SUMMARY

The Battery Pack Assembly has three input/output cable assemblies/connectors to interface with the Analyzer and the AC power source. Below is a listing and brief description of each signal.

B.2A Signal Descriptions

AC Hot, Neutral, GND provide the AC power source for the analyzer. When the Battery Pack Assembly is installed, AC voltage is routed through the Battery Park for connection to the Analyzer. The AC voltage may be 110Vac or 220Vac. Be sure that the proper voltage is selected at the Battery Pack Assembly *and* at the Analyzer's bottom panel.

+12VDC, GND are outputs of the Battery Pack Assembly and provide DC power to the Analyzer for use when AC power is not available.

B.2B Connector Descriptions

B.2B.1 J1, AC Power Connector

... for connection to AC power source.

pin	
El	AC Hot (110 or 220Vac)
E2	GND
E3	AC Neutral

B.2B.2 W1, AC Power Connector

... for routing AC power source to Analyzer.

pin	
E4	AC Hot (110 or 220Vac)
E5	GND
E6	AC Neutral

B.2B.3 P1, DC Power Connector

... DC power source to Analyzer.

pin	
1,2	+12VDC
4	GND

B.3 BLOCK DIAGRAM DESCRIPTION

Not applicable to this option. See Fig. B.6.

B.4 DETAILED DESCRIPTION

B.4.1 Line Transformer/Rectifier

With the Battery Pack Assembly installed on the Analyzer, AC power enters J1, and continues out to the Analyzer on W1. The AC power also connects to pads E1, E2, and E3 on the circuit card assembly.

AC Power continues through fuse F1 (250V, 0.5A) and Thermal Fuse TFI to the AC transformer T1, and the voltage configuration switch S1. Switch S1 is used to connect the two windings in the primary of transformer T1 in series for 220Vac operation, or in parallel for 110Vac operation.

Neon lamp DS1 protects the Battery Pack Option if 220VAC is applied to the Analyzer when the voltage selection switch is set for 110VAC. In this situation fuse F1 is blown.

AC power is transformed to 22Vac RMS in the secondary of transformer T1, and rectified to 21Vdc by rectifier bridge BR1.

B.4.2 Filter/Regulator

The 21Vdc from bridge BR1 is filtered by C1 and sent to power transistors Q1, Q2, and regulator U2. Zener diode D1 protects capacitor C1 from an overvoltage condition. As Vcc enters the regulator U2, pin 10 delivers a positive voltage to the bases of Q1 and Q2 which allows them to turn on and deliver voltage to the DC outputs.

As the DC output rises, a feedback voltage is delivered to a voltage divider (R12, R13, R14). R13 is used to adjust the level into U2-4, which is the inverting input to an internal differential amplifier. U2-5 is the non inverting input to the differential amplifier, connected to the 7.15V reference voltage at U2-6.

As the voltage on the inverting input reaches the voltage on the non inverting input, the output on U2-10 begins to regulate the on-levels of the pass transistors Q1 and Q2. This in turn regulates the output voltage to 14.8Vdc.

R4 and R5 are 1Ω resistors on the emitters of Q1 and Q2 to balance the current sharing of the pass transistors.

B.4.3 Current Limit/Charge LED

R8 is a 1Ω resistor in series with the regulated DC voltage. This resistor develops a voltage across it, based on the current passing through it. This current sense voltage is fed into the current limit input to the regulator (U2-2, U2-3). This current limit level is set by the formula; Iout = 0.66/R8 = 0.66 Amps.

B.4.4 Batteries

Batteries BT1 and BT2 are connected in parallel to the charging circuit through connections E10/E11 (+) and E12/E13 (-).

B.5 CALIBRATION/ALIGNMENT

Ensure that the Analyzer has been warmed up to operating temperature before performing any adjustments.

All other general statements concerning calibration and alignment found in the Calibration/Alignment section of this manual (Section 3) are applicable to this section and will not be repeated here.

B.5.1 Output Voltage Adjustment

1. Disconnect P1 from the Analyzer (DC voltage output from Battery Pack charging board).

2. With AC power applied, adjust R14 for 14.8Vdc between P1 pin 1 or 2 (+Vdc, same as E7 or E8 on board) and P1 pin 3 (GND, same as E9).

B.6 BLOCK DIAGRAM

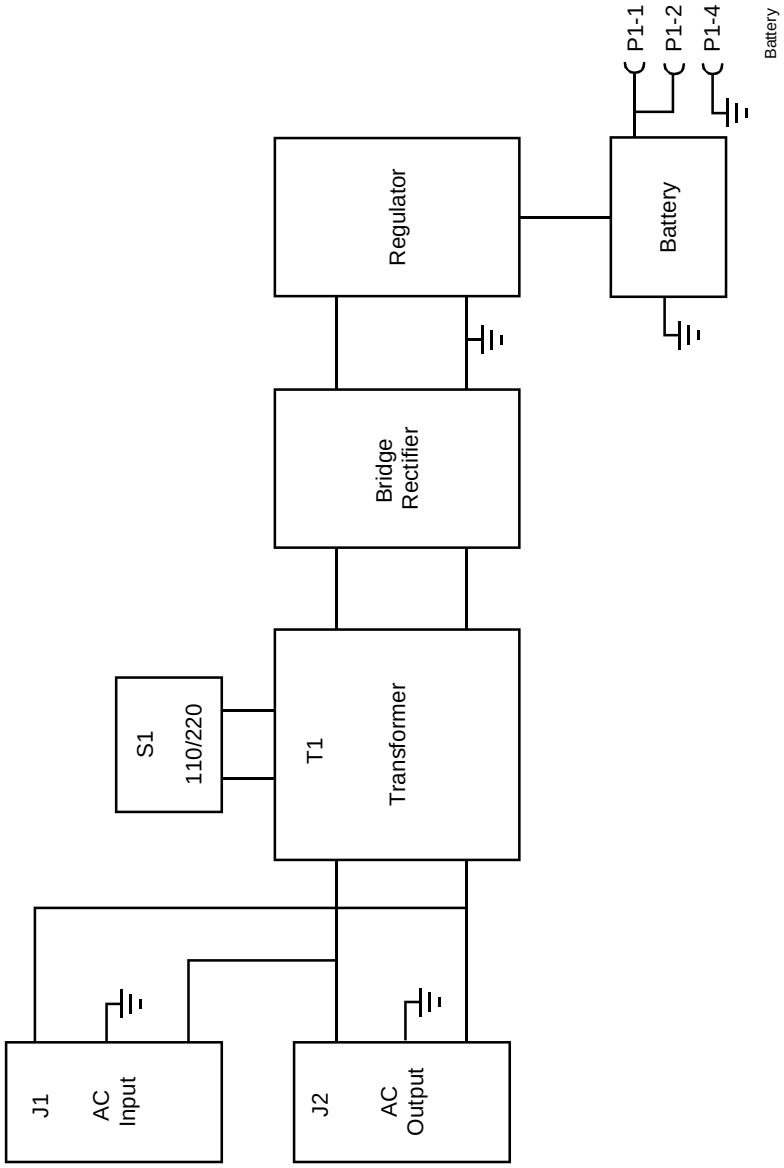
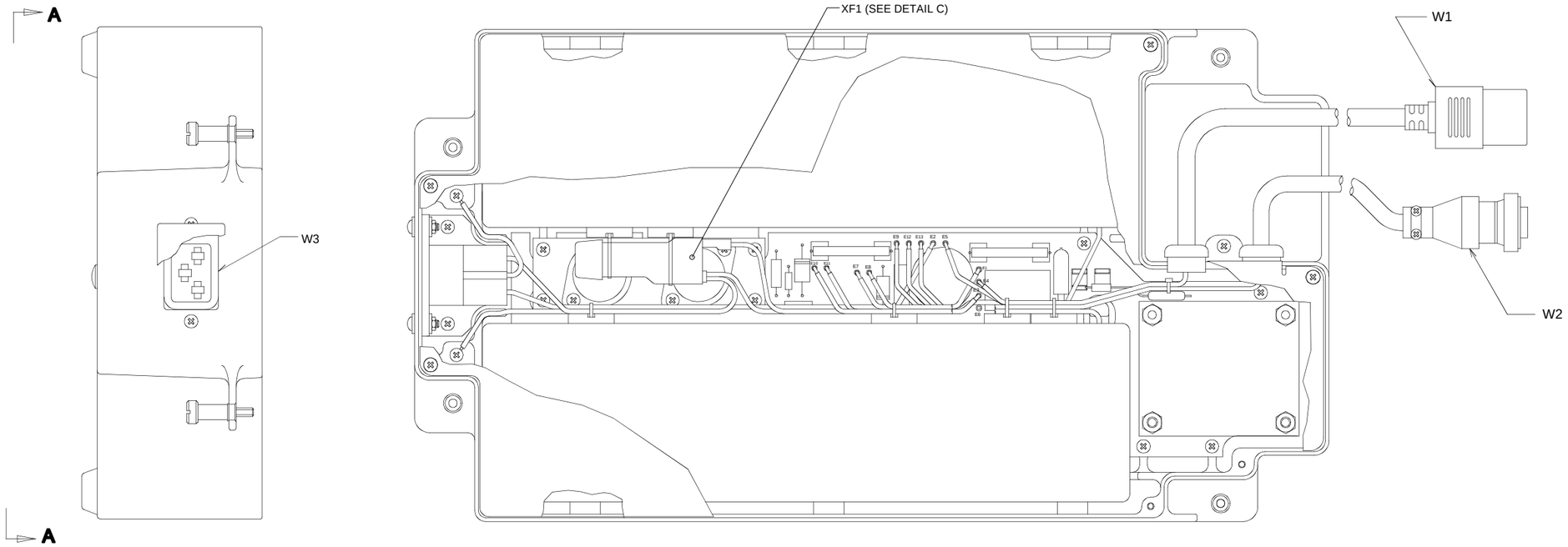
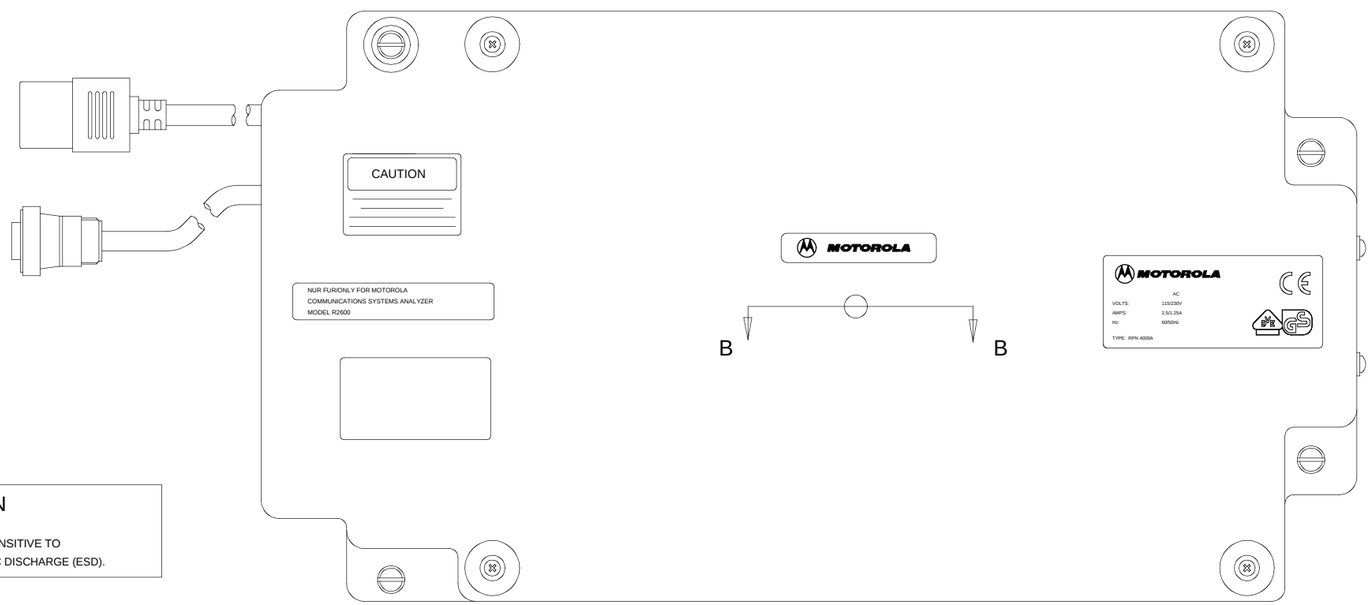
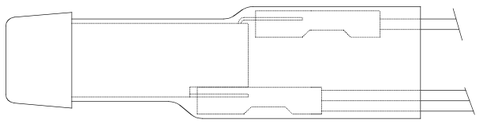


Fig. B.6 Battery Pack Assembly Block Diagram

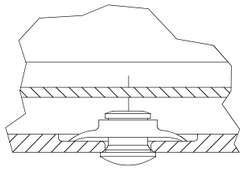




VIEW A-A



DETAIL C



SECTION B-B

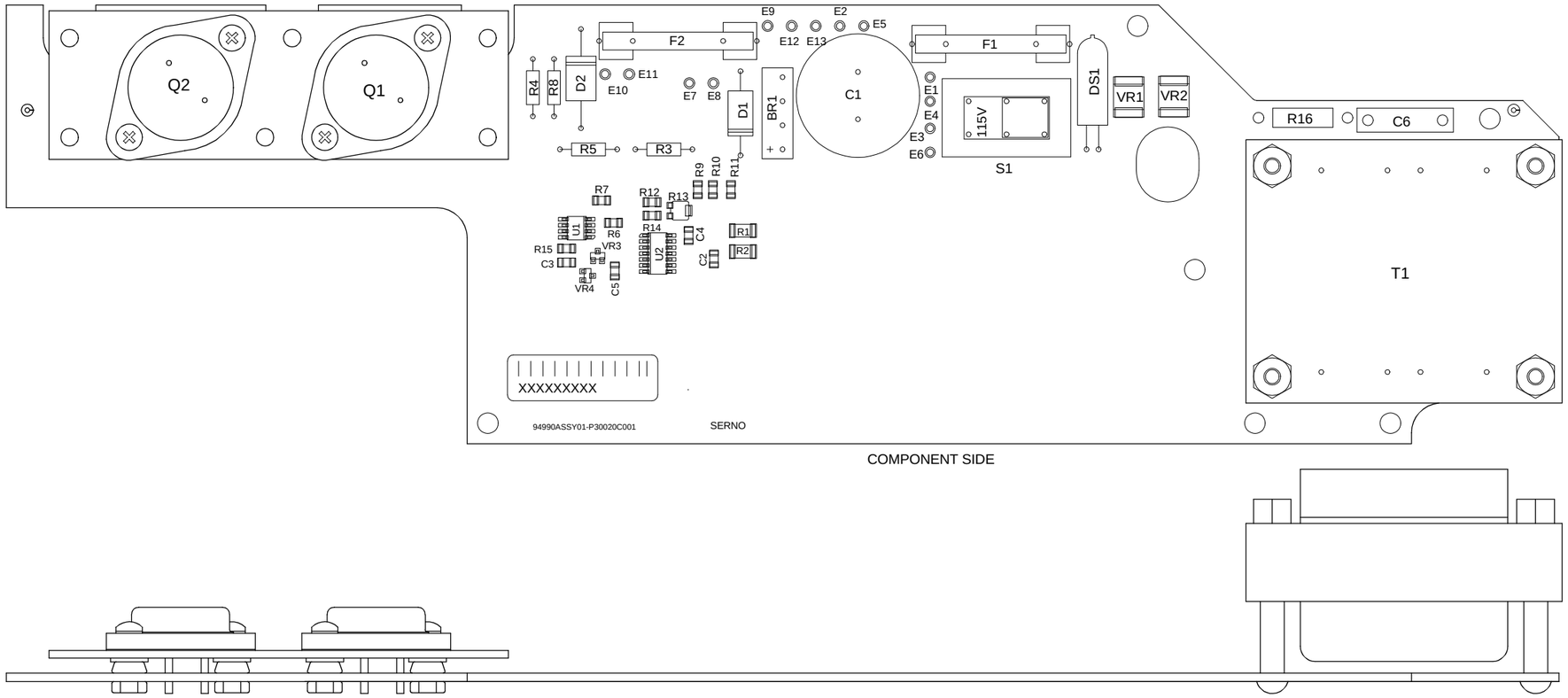
CAUTION

THIS ITEM IS SENSITIVE TO
ELECTROSTATIC DISCHARGE (ESD).

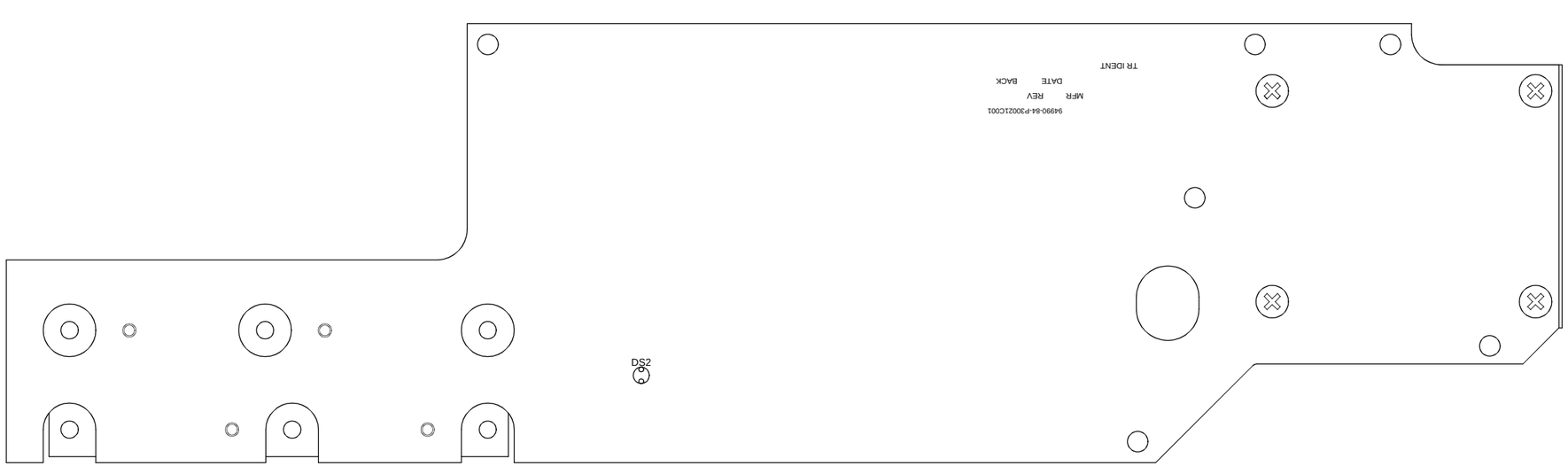
BATTERY UNIT ASSEMBLY

01-P30020C REV. H

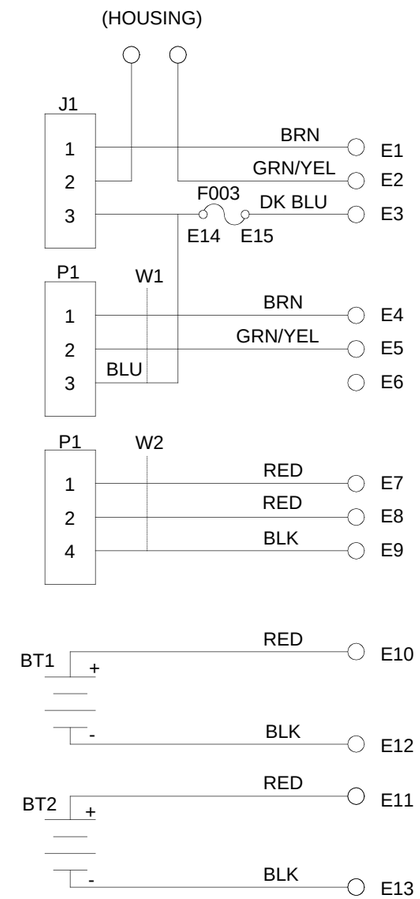
SHEET 1 OF 2



COMPONENT SIDE



BACK SIDE



INTERCONNECT DIAGRAM

CAUTION

THIS ITEM IS SENSITIVE TO ELECTROSTATIC DISCHARGE (ESD).

BATTERY UNIT ASSEMBLY

01-P30020C REV. H

SHEET 2 OF 2

DWG NO 63-P30022C SH 1

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
A	MCO C35945 RJC 94-03-02	94-07-28	P.MURPHY
B	MCO E36119 FAD 95-02-02		

NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH A1A16.
2. FOR REFERENCE DRAWINGS REFER TO:
   01-P30020C ASSEMBLY
   12-P30023C TEST PROCEDURE
3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ±1PCT, 1/8 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL INDUCTORS ARE IN UH.
   ALL VOLTAGES ARE IN DC.
4. TERMINATIONS CODED WITH THE SAME LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
5. DEVICE TYPE NUMBERS AND CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE 1.

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

TABLE 1

REF DES	DEVICE TYPE	VCC CONNECTION		GND CONN
		PIN	VOLTS	
U1	LM311DR2	8		7
U2	MC1723CDR2	11,12		

TABLE 2

REFERENCE DESIGNATIONS	
HIGHEST NUMBER USED	NOT USED
BR1	
C5	
D2	
DS2	
E13	
F2	
J1	
Q2	
P5	
R15	
S1	
T1	
U2	
VR4	
W1	

ALL SHEETS ARE THE SAME REVISION STATUS

		CONTR 3980
		ISS B35550-131(-) 91-04-26
		APPROVALS
		DWN R.SPARANESE 90-24-04
		CHKR D.W.ROBBINS 91-09-24
		QA J.MITCHELL 91-04-24
		MATL C.MUNZERT 91-04-24
		MFG J.DECAMP 91-04-24
NEXT ASSY	USED ON	ENG D.W.ROBBINS 91-04-24
APPLICATION		CUST

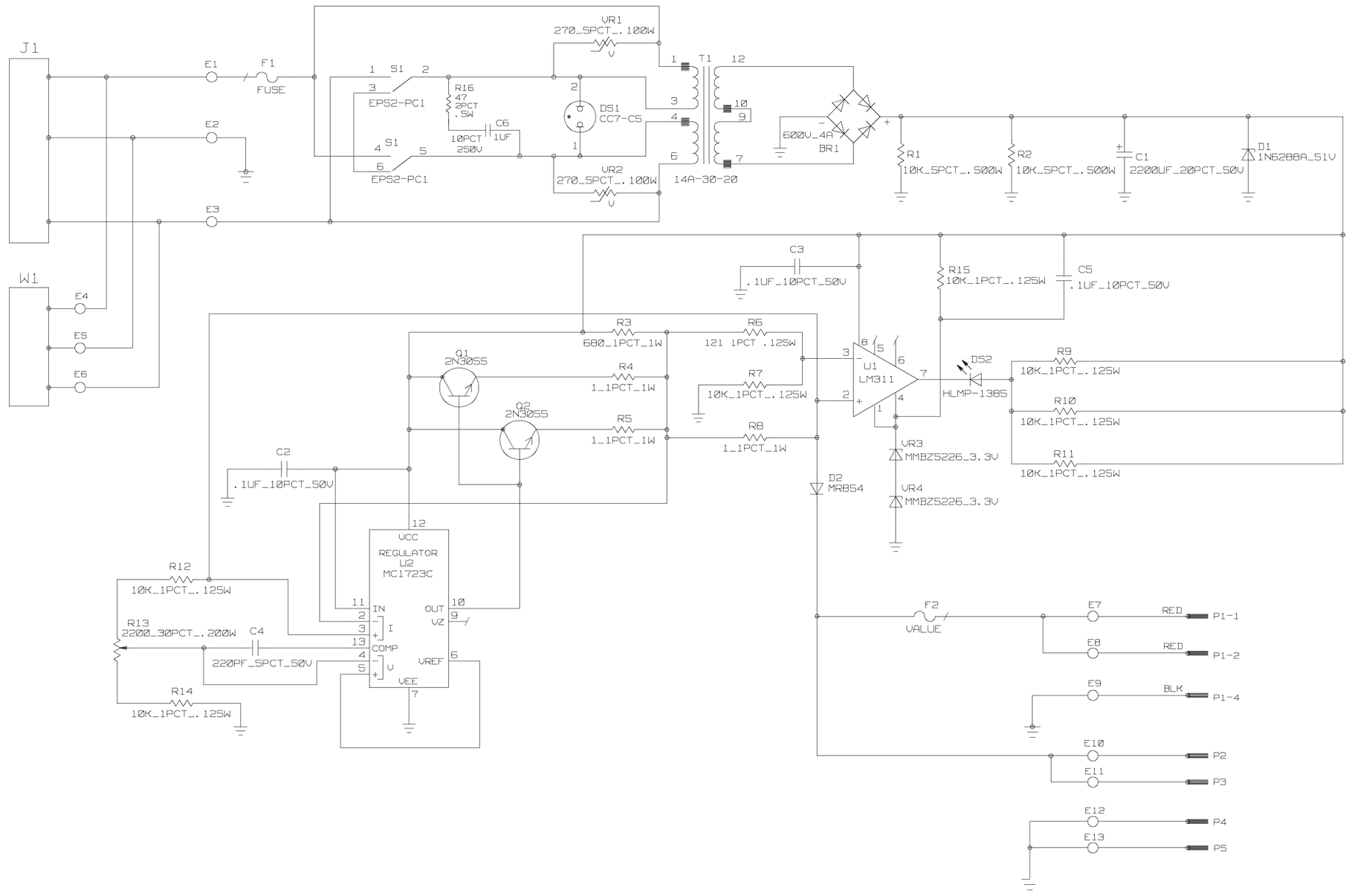
MOTOROLA INC.
GOVERNMENT AND SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

TITLE

BATTERY UNIT SCHEMATIC DIAGRAM

SIZE	CAGE CODE	DWG NO
D	94990	63-P30022C

SCALE NONE SHEET 1 OF 2



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE	CAGE CODE	DWG NO	REV
	D	94990	63-P30022C	B
	SCALE NONE			SHEET 2 OF 2

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Go to Appendix D

C.1 GENERAL DESCRIPTION

The FDMA Digital module is designated as A18 and is mounted on the rear of the R2670 Communications Analyzer.

This module currently provides a platform for testing ASTRO and Securenet subscriber radios and base station, Trunked Systems, and to provide other FDMA Digital features. The FDMA Digital module contains two processors, each having a companion support IC. The host processor is an MC68HCllFl with port expansion provided by a Support Logic IC (SLIC). The Digital Signal Processor is a DSP56002 which is supported by an ADSIC custom IC to provide an interface between the DSP and ABACUS IC. The ABACUS/DSP chip set provides all necessary functions required for a digital radio. Communication with the main R2670 Analyzer is via a byte wide dual port RAM. The Main system MC68HC000 processor has access to the dual port on one side and the FDMA Digital Host processor has access to the dual port on the other side.

A frequency synthesizer daughterboard is installed on the FDMA Digital module. It provides a duplex offset RF frequency for use as a control channel in Trunked System test mode.

Optional Secure hybrids can be installed to support testing of various Securenet Radios.

This appendix to the RLN5237 Maintenance Manual is intended only as an aid for technicians who must repair the FDMA Digital Option. Operation of the installed FDMA Digital Option is covered in "Operator's Manual, FDMA Digital Option", order number 68-803091F17.

The part numbers and configurations of this module are as follows:

01-P57130J001	FDMA Digital Circuit Card Assembly (CCA)
01-P30089C001	Analog and ASTRO trunking option slice (CCA and housing)
01-P30097C001-2	Securenet option slice (CCA and housing)
01-P30089C005	MPT1327 for R2680 (CCA and housing)

C.2 SIGNALS SUMMARY

C.2A Signal Descriptions

C.2A.1 J1 Power Supply

+5V is the regulated +5V DC voltage from the main system power supply used for digital circuit Vcc.

-5V is the regulated –5V DC voltage from the main power supply used for input comparator negative supply voltage.

+12V is the regulated +12V DC voltage from the main power supply and is the positive supply voltage for the analog circuitry.

-12V is the regulated –12V DC voltage from the main power supply and is the negative supply voltage for the analog circuitry.

GND is the circuit ground and is connected to chassis ground when the circuit card is installed in its housing and attached to the main system.

C.2A.2 J2 Processor Analog Interface

A/D DATA 0-7 are inputs to the R2670 processor from the Interface module and are not used by the FDMA Digital module.

CONV MOD input is any combination of the R2670 internally generated modulation signals, external modulation signals and signals from other option modules.

DC INPUT + is the positive voltage of the DC Input to the R2670 Power Supply and is not used by the FDMA Digital module.

DEMOD CAL AUDIO is the unsquelched demodulated audio signal from the R2670 Interface Module and is not used by the FDMA Digital module.

DVM is a buffered output of the 12 bit A/D input on the R2670 Interface module and is not used by the FDMA Digital module.

DVM FROM RANGE is the attenuated digital voltmeter signal from the R2670 Interface module and is not used by the FDMA Digital module.

EXT MOD + MIC IN is the sum of the External Modulation input and the Microphone input from the R2670 Front Panel and is not used by the FDMA Digital module.

EXT MOD IN input from the R2670 interface is the amplified and buffered EXT MOD IN from the Front Panel. This signal is not used by the FDMA Digital module.

GEN AUDIO is the calibrated sum of all the audio modulation to be routed to the synthesizer. The summation is performed by the R2670 Processor module and its output capacitively coupled and buffered by the Interface module to create MOD CAL AUDIO. This signal is not used by the FDMA Digital module.

HANDSET AUDIO signal is from the R2670 Processor speaker amplifier and is routed to the Front Panel microphone connector. This signal is not used by the FDMA Digital module.

IACK 1-2, IACK 4-7** inputs indicate an interrupt acknowledge cycle has been issued from the R2670 Processor. These lines are used in conjunction with IRQ 1-7. IACK 6* is used by the FDMA Digital module to acknowledge dual port RAM interrupts.

INT MOD is the sum of all R2670 internally generated modulation signals. This signal is not used by the FDMA Digital module.

IRQ 1-2, IRQ 4-7** inputs are the Interrupt Request lines to the R2670 MC68HC000 processor. IRQ 6* is used to request a dual port RAM interrupt.

MIC IN input from the R2670 Interface module is not used by the FDMA Digital module.

OPT AUDIO RTN 1,2 outputs are audio signals generated by the option modules and sent to the R2670 Processor for summation into CONV MOD.

The OPT AUD RTN 1 signal is the D to A converted and filtered output from the FDMA Digital DSP.

OPT MOD RTN 1,3 outputs are modulation signals from the option modules to the R2670 Processor where they are summed to provide GEN AUDIO. OPT MOD RTN 3 is used by the FDMA Digital module.

OPTION TO DVM output is to route selected signals from the FDMA Digital and other Option modules to the R2670 Interface module for DVM measurement.

RAW MIC IN is the microphone input from the R2670 Front Panel connector routed through the Interface module to the Processor module. This signal is not used by the FDMA Digital module.

RECEIVE SPEAKER AUDIO signal is the squelched unfiltered demodulated audio from the R2670 receiver routed through the Interface module and is not used by the FDMA Digital module.

*RESET** is used to reset the R2670 Analyzer and FDMA Digital module.

SAMPLE CLOCK signal is the sample clock for the 8-bit A/D on the R2670 Interface module and is not used by the FDMA Digital module.

SQUELCH signal from the R2670 Receiver module indicates whether the receiver is squelched and is used to light a Front Panel LED. This signal is routed through the Interface module and is not used by the FDMA Digital module.

SQUELCH LEVEL signal is routed to through the R2670 Processor module from the Front Panel to the Interface module and is not used by the FDMA Digital module.

SQUELCHED DEMOD is a squelched version of the demodulated receive signal (DEMOD CAL AUDIO). It is routed from the R2670 Receiver module through the Interface module. This signal is not used by the FDMA Digital module.

SYSCLK input is the 10MHz reference signal from the R2670 Frequency Standard Module (via the Processor Module).

TIMER CLOCK is used to generate a clock of varying frequency (76Hz to 5MHz) and is used by the R2670 Interface module to produce the SWEEP signal for the Spectrum Analyzer. This signal is not used by the FDMA Digital module.

TRIGGER input signals the R2670 Processor ASIC when to start auto sampling the input data (A/D DATA 0-7 from the Interface module) for scope functions. This signal is not used by the FDMA Digital module.

VOL CNTL AUDIO output is the received audio signal from the FDMA Digital module.

WATTMETER OUT This signal is not used by the FDMA Digital module.

*WB/(NB)** input indicates whether the receiver is operating in wideband or narrowband mode and is not used by the FDMA Digital module.

C.2A.3 J3 Processor Digital Interface

Al - A22 are address inputs from the R2670 MC68HC000 processor.

*BR/(WR)** is the buffered read/write signal which indicates the direction of data transfer to and from the R2670 MC68HC000 processor.

D0 – D15 are the inputs/outputs of the R2670 MC68HC000 data bus.

*DTACK** (Data Transfer ACKnowledge) Output indicates to the R2670 MC68HC000 processor that a data acknowledge is being issued from the FDMA Digital module. DTACK is wire-ORed so all modules can use the same signal.

*LDS** (Lower Data Strobe) When at a logic 0 indicates that valid data is on the lower eight data lines of the R2670 MC68HC000 processor.

OPT DET 1,2,3,4 (Option Detect) Input to the processor which signifies the presence of an Option Module. A logic 0 on any one of the four inputs signifies an Option Module is present. Up to two Option Modules can be installed on the unit. The FDMA Digital module uses OPT DET 2.

*OPT MEM** (Option Memory) Active low output from the R2670 Processor selects option memory space.

OPT TO CNTR (Option To Counter) This signal is routed on the Processor module from J9 (Option connector) to J1 (interface connector). This signal is not used by the FDMA Digital module.

*UDS** (Upper Data Strobe) A logic 0 indicates that valid data is on the upper eight data lines of the R2670 MC68HC000 processor.

VBACKUP is the battery backup voltage when the unit is unpowered. This voltage is not used on the FDMA Digital module.

C.2A.4 J4 IF Interface

10.7MHz This signal from the R2670 receiver is routed to the FDMA Digital module where it is fed into a mixer with an 11.15MHz oscillator to produce a 450KHz IF signal to the ABACUS.

C.2A.5 J5 Encryption Keying Interface

*EMCWE** Active low output signal which indicates a write enable to an externally connected radio.

*KEYFAIL** Output data stream to an externally connected radio or an input data stream to the encryption modules depending on mode selected.

*KEYLOAD** A logic 0 indicates to the FDMA Digital module that a keyloader is attached.

KID Output bit sync signal to an externally connected radio.

C.2A.6 J6 Serial Interface

CTSI Clear To Send Input for wireline and becomes Request To Send Input when RS-232 is selected. Not currently implemented.

MODE SEL when a logic 0 places the Host Processor in a Bootstrap mode for loading Flash memory. Not currently implemented.

RTSO Request To Send Output for wireline and becomes Clear To Send Output when RS-232 is selected. Not currently implemented.

RXCLKI Receive Clock Input for synchronous transfer of wireline data. Not currently implemented.

RXDI Receive Data Input for asynchronous RS-232 or synchronous Wireline interface depending on mode selected. Not currently implemented.

SCIRX Serial Communications Interface Receive data input used to bootload Flash memory. Not currently implemented.

SCITX Serial Communications Interface Transmit data output used to bootload Flash memory. Not currently implemented.

TXCLKO Transmit Clock Output for synchronous transfer of wireline data. Not currently implemented.

TXDO Transmit Data Output for asynchronous RS-232 or synchronous Wireline interface depending on mode selected. Not currently implemented.

C.2A.7 J8 Encryption Module Interface #1

*EMC EN 1** enables encryption module #1 for data transfer via the Host processor SPI port.

*EMC REQ 1** Interrupt request for service from encryption module #1 to the Host processor.

EMC RXD 1 Receive data to the DSP SCI port.

EMC TXD 1 Transmit data from the DSP SCI port.

EMC WAKE UP 1* Active low signal from the FDMA Digital Host processor to place the Encryption module in an active state.

*KEYFAIL 1** Input data stream from a keyloader to encryption module #1.

MISO Master In Slave Out signal to the Host processor SPI port.

MOSI Master Out Slave In signal from the Host processor SPI port.

SCK clock from the Host processor for transfer of data to/from the Host processor via the SPI port.

VREG Input voltage of +7.5V.

C.2A.8 J9 Encryption Module Interface #2

*EMC EN 2** Enables encryption module #2 for data transfer via the Host processor SPI port.

*EMC REQ 2** Interrupt request for service from encryption module #2 to the Host processor.

EMC RXD 2 Receive data to the DSP SCI port.

EMC TXD 2 Transmit data from the DSP SCI port.

EMC WAKE UP 2* Active low signal from the FDMA Digital Host processor to place the Encryption module in an active state.

KEYFAIL 2 Input data stream from a keyloader to encryption module #2.

MISO Master In Slave Out signal to the Host processor SPI port.

MOSI Master Out Slave In signal from the Host processor SPI port.

SCK clock from the Host processor for transfer of data to/from the Host processor via the SPI port.

VREG Input voltage of +7.5V.

C.2A.9 J10 Synthesizer Interface

AUX D/A Output from the FDMA Digital module to the Synthesizer and is the D/A converted and filtered out of the DSP.

FREF is a 2.5MHz clock from the FDMA Digital module.

MISO Master In Slave Out signal to the Host processor SPI port.

MOSI Master Out Slave In signal from the Host processor SPI port.

NBVVO Modulation output from ADSIC D/A which has been passed through a narrow band filter.

SCK clock from the Host processor for transfer of data to/from the Host processor via the SPI port.

*SYNTH EN** Active low synthesizer enable signal from Host processor.

*SYNTH SEL** Active low synthesizer select signal from SLIC port.

WBVVO Modulation output from ADSIC D/A which has been passed through a wide band filter.

C.2A.10 Synthesizer J2 RF Output

310.7MHz This output from the control channel synthesizer is routed to the A6 RF Output module, J2, where it is coupled into the main 310.7MHz input

C.2B Connector Descriptions

In all of the following descriptions the word “reserved” after the signal name is used to indicate a reserved pin used by another module or a pin reserved for future use.

C.2B.1 J1 (20 pin connector to interface to the power supply cable)

pin	
1-3,11-13	GND
4,14,8,18	NC
5,15	-12V
6,16	+12V
7,17	-5V
9,10,19,20	+5V

C.2B.2 J2 (60 pin connector from the R2670 Processor)

pin	
1	DVM Reserved
2	GND
3	GEN AUDIO Reserved
4	GND
5	OPTION TO DVM
6	WB/(NB)* Reserved
7	DVM FROM RANGE Reserved
8	GND
9	EXT MOD + MIC IN Reserved
10	GND
11	HANDSET AUDIO Reserved

12	RAW MIC IN Reserved
13	RECEIVE SPEAKER AUDIO Reserved
14	GND
15	DEMOD CAL AUDIO Reserved
16	DC INPUT + Reserved
17	MIC IN Reserved
18	EXT MOD IN Reserved
19	SQUELCH LEVEL Reserved
20	INT MOD Reserved
21	RESET*
22	SQUELCHED DEMOD Reserved
23	GND
24	VOL CNTL AUDIO
25	GND
26	SYSCLK
27	GND
28	CONV MOD
29	OPT MOD RTN1 Reserved
30	OPT AUDIO RTN1
31	OPT MOD RTN3
32	OPT AUDIO RTN2 Reserved
33	GND
34	IRQ1* Reserved
35	IRQ2* Reserved
36	SQUELCH Reserved
37	IRQ4 Reserved
38	IRQ5* Reserved
39	IRQ6*
40	IRQ7* Reserved
41	TIMER CLOCK Reserved
42	A/D DATA7 Reserved
43	A/D DATA6 Reserved
44	A/D DATA5 Reserved
45	A/D DATA4 Reserved
46	A/ D DATA3 Reserved
47	A/D DATA2 Reserved
48	A/D DATA1 Reserved
49	A/D DATA0 Reserved
50	IACK7* Reserved
51	IACK6*
52	IACK5* Reserved
53	IACK4* Reserved
54	IACK2* Reserved
55	IACK1* Reserved
56	TRIGGER Reserved
57	GND
58	SAMPLE CLOCK Reserved
59	GND
60	OPTFLASH UNLOCK

C.2B.3 J3 (60 pin edge connector from the R2670 Processor)

pin	
1-9	DO - D7
10	GND
11-18	D8 - D15
19,20	GND
21-27	Al-A7
28	GND
29-35	A8 - A14
36	GND
37-44	A15 - A22
45	GND
46	LDS*
47	UDS*
48	GND
49	BR/WR*
50	OPT DET1 Reserved
51	DTACK*
52	OPT DET2
53	VPA*
54	OPT DET3 Reserved
55	VBACKUP Reserved
56	GND
57	OPTMEM*
58	GND
59	OPT TO CNTR Reserved
60	GND

C.2B.4 J4 (SMB connector from the R2670 receiver module)

pin	
1	10.7MHz
2	GND(shield)

C.2B.5 J5 (5 pin connector to/from external Radio/Keyloader)

1	KEYLOAD*
2	GND
3	KEYFAIL*
4	EMCWE*
5	KID

C.2B.6 J6 (25 pin D connector for external serial interface)

pin	
1,7	GND
2	TXD
3	RXD
4	RTS
5	CTS
6,8-13	NC
14	SCITX
15	NC
16	SCIRX
17	RXCLKI
18-23	NC
24	TXCLKO
25	MODE SEL

C.2B.7 J8 (25 pin board to board connector to encryption module #1)

pin	
1,2,20	VREG
3	EMCRXDI
4	EMCTXD1
5	NC
6,21,22	GND
7	MISO
8	MOSI
9	SCK
10	EMCEN1*
11	EMCREQ1*
12	EMCWAKEUP1*
13,14	NC
15	KEYFAIL1*
16-19	NC
23-25	NC

C.2B.8 J9 (25 pin board to board connector to encryption module #2)

pin	
1,2,20	VREG
3	EMCRXD2
4	EMCTXD2
5	NC
6,21,22	GND
7	MISO
8	MOSI
9	SCK
10	EMCEN2*
11	EMCREQ2*
12	EMCWAKEUP2*
13,14	NC
15	KEYFAlL2*
16-19	NC
23-25	NC

C.2B.9 J10 (25 pin board to board connector for synthesizer)

pin	
1,2,20	+5V
3	SYNTHSEL*
4	FREF
5,13	-12V
6,21,22	GND
7	MISO
8	MOSI
9	SCK
10	SYNTHEN*
11	NC
12	WBVVO
14,18	AGND
15	NC
16	NBVVO
17,19	+12V
23	AUXD/A
24,25	+5VA

C.3 BLOCK DIAGRAM DESCRIPTION

The FDMA Digital module contains several major functional blocks which:

1. Provide an interface to the main R2670 system (Dual Port RAM).
2. Manage system functions and control data and signal flow (Host MC68HClIFl and SLIC).
3 Perform all baseband signal processing of transmit and receive signals (DSP56002).
4. Provide mixing, digitization, filtering, FM discrimination and D/A conversion for receive signals (ADSIC/ABACUS).
5. Provide A/D conversion, and D/A conversion for transmit signals (ADSIC).
6. Provide the capability to test encrypted messages (Encryption Modules).
7. Allow input/output of baseband signals into the DSP (ADC/DAC).
8. Provide duplex frequency used in Trunked System testing as a control channel.

External interfaces to the FDMA Digital module include a serial port attached to the HC11 SCI for RS-232 peripherals, a synchronous serial port which uses HDLC protocol for wireline hookup to a modem, and a keyloader interface which accepts keys from a DX keyloader or outputs test keys to Securenet radio equipment.

C.4 DETAILED DESCRIPTION

C.4.1 Dual Port RAM Interface

The FDMA Digital module communicates with the R2670 via a Byte wide dual port RAM (DPRAM) interface. The R2670 Processor (MC68HC000) and the FDMA Digital Host processor (MC68HC11F1) have read and write access to the DPRAM so that messages and commands can be passed from one processor to the other.

The DPRAM is organized as 2K x 8 bits. Each processor has the ability to interrupt the other processor by writing to specific locations of the processor's DPRAM space, as shown in Figure C.1 The interrupt request can be cleared by reading the corresponding interrupt control DPRAM locations.

C.4.1.1 Read/Write Cycles

R2670 side

During a read cycle, the R2670 Processor asserts OPTMEM* (option address space ANDed with address strobe), LDS* and UDS* simultaneously and the FDMA Digital module responds by asserting DTACK*. The assertion of DTACK* is held off for two clock cycles (200ns) to allow time for DPRAM data to be placed on the bus. Upon receipt of DTACK* the R2670 Processor reads the data and raises OPTMEM*, LDS* and UDS* which causes the read cycle to end.

During a write cycle, the R2670 Processor asserts OPTMEM* and R/(W)* and places data on the bus. One clock later LDS* and UDS* are asserted which causes DTACK* to be generated by the FDMA Digital module.

FDMA Digital side

DPRAM read and write cycles on the FDMA Digital Host processor side are performed during an HC11 E clock cycle. RAM address and chip select (CSIO2) are asserted at the beginning of an E clock cycle and data is read on the falling edge of the E clock cycle.

Data is written to the DPRAM at the end of an E clock cycle using a write pulse generated by the SLIC.

C.4.1.2 Memory Map

The memory map for the DPRAM is shown in Figure C.1. Two 128 byte address blocks are allocated to interrupts.

FDMA			R2670
$1800 $1B7F	R2670 TO FDMA Digital Message, Messages (896 Bytes)		$AC0001 $AC06FF
$1B80 $1BFF	Write by FDMA Digital Host processor generates a level-6 interrupt request to the R2670 Processor	Read by the R2670 processor clears the level-6 interrupt request	$AC0701 $AC07FF
$1C00 $1F7F	FDMA Digital to R2670, Messages (896 Bytes)		$AC0801 $AC0EFF
$1F80 $1FFF	Read by FDMA Digital Host processor clears the interrupt request	Write by the R2670 processor generates an interrupt request to the FDMA Digital Host processor	$AC0F01 $AC0FFF

Figure C.1 Dual Port Ram Memory Map

C.4.2 Host Processor Functions

The MC68HCllFl FDMA Digital Host processor controls the analog signal paths and digital data flow between the FDMA Digital module and its internal and external interfaces. The host processor main data bus is 8-bits wide and is used to:

1. Communicate to the R2670 by accessing DPRAM
2. Access Flash Memory and RAM.
3. Interface to the SLIC for port expansion.
4. Pass data, control messages between the host and DSP.
5. Provide a wireline interface via the serial communications controller (SCC).
6. Write to Control Latches to control signal flow.
7. Attenuate analog output from DSP DAC by using a leveling DAC.

The Host processor uses the synchronous serial SPI bus to:

1. Configure the ADSIC.
2. Interface to Encryption modules and Trunking Synthesizer.

The Host processor can address up to 64K-bytes which can be expanded by programming bank bits FA14-FA19 via the CPLD. A clock frequency of 7.3728MHz is used to produce an E-clock frequency of 1.8432MHz. Read and write cycles occur during an E-clock period.

Other functions supported by the Host processor include an RS-232 interface via the SLIC ACIA port, and controlling and processing the keyloader interface.

C.4.2.1 Host Flash Memory

The Host program code is stored in a 8 megabit Flash Memory configured as 1M x 8 bits.

C.4.2.2 Host RAM

The Host RAM is as 32K x 8 bits. RAM locations are accessed by direct addressing from the HC11.

C.4.2.3 Memory Map

The Host processor memory map is shown in Figure C.2. 16K of Flash Memory can be directly addressed by the processor or by programming the FA14-FA19 bank bits, 1M of Flash Memory can be accessed as 64 banks of the 16K address block (logical address $8000-BFFF).

NAME	HC 11 ADDRESS RANGE
FLASH MEMORY	$8000 - $FFFF
COMMON BOOT AREA	$C000 - $FFFF
BANKED AREA	$8000 - $BFFF
RAM	$2000 - $7FFF
DPRAM	$1800 - $1FFF
MEMORY PAGE CONTROL	$1700 - $17FF
SERIAL CONTROLLER	$1600 - $16FF
HOST INTERFACE	$1500 - $15FF
LEVELING DAC	$1400 - $14FF
CONTROL REGISTER 2	$1300 - $13FF
CONTROL REGISTER 1	$1200 - $12FF
SLIC	$1060 - $11FF
INTERNAL REGISTER BLOCK	$1000 - $105F
INTERNAL EEPROM	$0E00 - $0FFF
EXTERNAL (not used)	$0400 - $0DFF
INTERNAL RAM	$0000 - $03FF

Figure C.2 Host Processor Memory Map

C.4.2.4 Analog Signal Path Control Latches

The host processor controls analog signal flow by writing to two 8-bit latches. The latch outputs are used to enable SPST analog switches and to control analog multiplexers.

C.4.2.5 Serial Peripheral Interface

The SPI is a high-speed synchronous serial I/O bus with the Host processor assigned master. The SPI bus allows the host processor to configure the ADSIC, transfer data to/from the encryption modules, and provide communication with the trunking synthesizer. Three signals are associated with the SPI bus: the master-out-slave-in (MOSI), master-in-slave-out (MISO) and the serial clock (SCK). In addition, a unique select is used for each of the slaves.

C.4.2.6 Serial Communications Interface (SCI)

The host processor SCI port is not used during normal operation. During bootstrap mode, the resident boot loader program in the host processor allows a program to be loaded into on-chip RAM through the SCI port.

The SCI is an asynchronous serial data interface which uses Transmit data (TxD) and receive data (RxD) signals only. Baud rate is derived from the crystal clock circuit and is selected by programming the HC11 host processor.

C.4.2.7 External Serial Interfaces

Two serial interfaces are multiplexed on to the 25 pin "D" connector (J6). These are an asynchronous RS-232 port and a synchronous HDLC wireline port. Neither of these interfaces are used in the current configuration.

The ACIA feature of the SLIC is used for the RS-232 interface and a dedicated serial communication controller (Z85230) is used for the wireline interface.

C.4.2.8 Keyloader Interface

The keyloader Interface accepts inputs from a DX keyloader or outputs test keys to a Securenet radio. Input/Output selection is controlled by the Host processor. The 12KHz test key output signals are generated by the DSP in response to a 24KHz interrupt from the programmable clock. The KEYFAIL* input from the DX keyloader goes directly to the encryption modules.

C.4.2.9 Programmable Clocks

The programmable clock is used as a DSP interrupt to provide timing for capturing or generating data in the DSP. The clock is programmable from the Host processor. Currently implemented is a 24KHz clock used by the DSP to generate 12KHz Keyload signals. The ADC/DAC implementation will require a 200KHz clock. Other clock frequencies are available for future FDMA Digital Features.

C.4.2.10 Leveling DAC

The leveling DAC is an 8-bit multiplying DAC with an external input latch which is used to attenuate the analog signal output of the DSP DAC. The analog signal is applied to the DAC voltage reference input and a digital attenuation value written to the latch from the Host processor. An offset voltage is added to the analog input signal for bi-polar operation.

C.4.3 Support Logic IC (SLIC)

The SLIC is a companion chip to the Host processor (MC68HC11Fl). It provides I/O expansion and interrupt control. In addition, an ACIA port is included to provide RS-232 capability for future use.

The SLIC contains four 8-bit expansion ports which can be accessed by the host processor. Three of these ports (J,K,L) are bi-directional and the other (H), input only. Interrupts to the host processor from the DPRAM, encryption modules, DSP, and wireline are routed through the SLIC.

Three bits from port K are, configured as chip selects and are used to allow data bus transfers between the host and DSP, control latches, leveling DAC and wireline SCC. Chip selects for the DPRAM and RAM come directly from the host processor.

C.4.4 Host/DSP Interface

The Host processor communicates with the DSP using the HC11 8-bit data bus and three address lines. The DSP contains separate transmit and receive data registers which are double buffered to allow the DSP CPU and host processor to transfer data efficiently at high speed.

The Host Interface appears to the host processor as a memory mapped peripheral occupying eight bytes in host processor address space. The communication sequence starts by asserting the three host interface address lines to select the register to be read or written. The read/write* (SLICR/W*) is asserted to determine the direction of data transfer. The data is then strobed using Host enable (HEN*).

C.4.5 DSP Functions

The Digital Signal Processor (DSP56002) operates at a 33MHZ clock rate. It contains four data interface ports; two parallel and two serial.

The Host/DSP port is 8-bits wide and interfaces to the host(HC11) processor. The expansion port is 24-bits wide and connects the RAM, Flash Memory, and ADSIC to the DSP. The SSI port is a full-duplex synchronous serial interface that is used to pass data between the DSP and the ADSIC. The SCI port is a full duplex asynchronous serial interface that is used to pass signals to and from the encryption modules.

The DSP performs all baseband signal processing of transmitted and received signals. Typical functions performed by the DSP for baseband transmit are as follows:

1. Encode the digitized voice
2. Encrypt blocks of encoded data by managing the interface to the encryption modules
3. Perform error correction
4. Assemble blocks of embedded data and encoded voice into voice frames
5. Convert the resulting bit stream into symbol samples if required
6. Filter the baseband bit or symbol stream
7. Manage the ADSIC interface for D/A conversion

Typical functions performed by the DSP for baseband receive are:

1. Filter the baseband samples from the ADSIC
2. Achieve symbol or bit synchronization
3. Message recognition
4. Message disassembly
5. Error correction decode
6. Decryption by sending the signal to the encryption modules
7. Passed the resulting digitized voice back to the ADSIC D/A

C.4.5.1 DSP Flash Memory

The DSP Flash Memory is 1M x 8 bits and contains program code for the DSP. When reading the Flash Memory, the DSP allows three wait states for accessing data.

C.4.5.2 DSP RAM

The DSP RAM is organized as 24K x 24 bits and uses two 64K x 16 bit RAM devices. RAM device chip selects are decoded DSP addresses.

C.4.5.3 Memory Map

The memory map for the DSP is shown in Figure C.3. The 1M x 8 Flash Memory is divided into 64 banks of the 16K address space allocated. Flash Memory address banks are selected using bank bits (BNK0-2) from the ADSIC and DSPA18 and DSPA19 from the HC11 host processor. Program Memory Select (PS*) is used to distinguish between program memory and data memory.

$0000 $1FFF	Internal Memory
$2000 #3FFF	ADC/DAC
$4000 $9FFF	External DSP RAM
$A000 $DFFF	External Flash Memory, banked (Physical address $00000-FFFF)
$E000 $FFFF	ADSIC

Figure C.3 DSP Memory Map

C.4.5.4 Synchronous Serial Interface (SSI)

The DSP SSI is a full duplex interface that is used to transfer information to and from the ADSIC. The interface consist of six signals: clock, frame sync and data line for transmit and receive.

In the receive mode the SSI transfers ABACUS in-phase (I) and quadrature (Q) samples from the ADSIC to the DSP. The receive frame sync is one bit wide which generates an interrupt to the DSP. Data is shifted out at 20 or 33 1/3 Ksps using a 2.4MHz clock, or 60 Ksps using a 4.8MHz clock.

In the transmit mode the SSI is used to transfer 16-bit audio samples to the ADSIC VCO D/A converter. The transmit clock rate is 1.2MHz with a frame sync of 48KHz at 50% duty cycle.

C.4.5.5 Serial Communications Interface (SCI)

The DSP SCI port is used to transfer information to and from the encryption modules. The interface operates in an asynchronous mode using transmit (TXD) and receive (RXD) only. A multiplexer is used to select between encryption modules.

C.4.5.6 Analog to Digital Converter (ADC)

The 12-bit high speed ADC is read from the DSP parallel bus. The selected analog signal source is passed through a selectable 8KHz or a 50KHz filter and clocked at a 3.686MHz rate. Conversion time of the ADC is 13 clock cycles or 3.53 micro seconds.

The programmable clock can be set at a 200KHz (5uS) rate and is used to interrupt the DSP. When interrupted the DSP reads the 12-bit digital value from the ADC.

C.4.5.7 Digital to Analog Converter (DAC)

The DAC is a high speed 12-bit device with internal input data latches that are connected to the DSP parallel bus. The resulting analog signal is passed through a selectable 8KHz or 50KHz Filter, attenuated by a leveling DAC and sent to the Trunking Synthesizer connector or returned to the R2670 on OPT AUD RTN.

The programmable clock is used to interrupt the DSP which then writes to the DAC.

C.4.6 ADSIC

The purpose of the ADSIC is to provide an interface between the ABACUS IC and the DSP The ADSIC has four different interfaces:

1. The SPI bus for ADSIC configuration.
2. The SSI bus for transmit and receive data to and from the DSP.
3. A 16-bit parallel bus for transferring microphone and speaker D/A samples, and for DSP control of SSI modes.
4. An ABACUS interface which is really two separate interfaces; one for receiving I and Q samples and the other for ABACUS configuration.

The ADSIC contains an ABACUS differential line receiver, an IF filter, discriminator and SSI interface for receive signals. It also contains an SSI interface and D/A converter for transmit signals. A D/A is included for converting speaker samples from the DSP and outputting the audio signal to the main R2670 system speaker or for display. An A/D is used to convert the microphone or other analog signal into digital samples to be read by the DSP

C.4.7 Abacus

The incoming 10.7MHz IF is mixed down to 450KHz and then digitized by the ABACUS IC. The resulting digital signal is filtered and decimated to produce in-phase(I) and quadrature(Q) samples which are sent serially through a differential driver to the ADSIC at a 20KHz rate.

C.4.8 2.1 MHz Reference

The 2.1MHz Reference is used to provide an accurate clock for the ABACUS. The clock frequency is accurately set by a 16.8MHz crystal oscillator and divided by 8 to achieve 2.1MHz.

C.4.9 Signal Paths

Signal routing on the FDMA Digital module is controlled by the Host Processor and depends on the functions being performed and the modes selected. The following paragraphs describe the signal paths for ASTRO receive and transmit.

C.4.9.1 Received Audio Signal Path

For monitoring of ASTRO RF signals, the R2670 main system provides the FDMA Digital module with the 10.7MHz IF signal from the receiver. The 10.7MHz is mixed down to 450KHz and routed to the IF input of the ABACUS IC. After digitization, the signal is mixed down to baseband and filtered resulting in I and Q samples which are output over a serial interface from the ABACUS to the ADSIC at a 20KHz rate.

The ADSIC performs IF filtering and FM detection on the signal and then passes the resulting signal to the DSP over the SSI interface at a 20KHz rate.

The DSP filters the digital samples and performs symbol to bit conversion. The message is then disassembled and decrypted by sending it to the encryption modules. The received embedded data stream is then sent to the HC11 Host processor via the Host/DSP interface and back to the main R2670 via the DPRAM for display on the LCD. The decrypted voice message is sent to the ADSIC D/A via the DSP/ADSIC 16-bit parallel interface.

The resulting analog voice signal is routed from the ADSIC back to the main R2670 on VOL CNTR AUDIO and out to the speaker, or to the Display or DVM function on the OPT TO DVM line depending on the test being performed.

C.4.9.2 Transmit Audio Signal Path

The source for ASTRO transmit signals can be the R2670 front panel microphone, the front panel EXT MOD IN, or the signal can be an internally generated waveform. The selected signal is routed from the R2670 to the FDMA Digital module as CONV MOD. This audio signal is input to the ADSIC A/D and passed to the DSP via the 16-bit parallel interface.

The digitized audio signal is encoded and assembled into voice frames with blocks of embedded data sent from the host processor. The encoded data is sent to the encryption modules for encryption and then converted to 4-level symbol samples.

The symbol stream is filtered and sent to the ADSIC D/A converter via the SSI interface at a 48KHz frame rate. The resulting analog signal (VVO) is returned to the main R2670 system on OPT MOD RTN3 and then to the Modulator on signal MOD CAL AUDIO.

C.4.10 Control Channel Synthesizer

The option frequency synthesizer daughterboard includes a 5 volt regulator (Ul), a frequency synthesizer (U2) and a VCO/Buffer I.C. (U3). The VCO/Buffer I.C. contains two independent VCO's. One covers the lower half of the required tuning range (245MHz to 310MHz) and the other covers the upper half (310MHz to 375MHz). Switching of the VCO's is controlled by the frequency synthesizer through AUX3. All inputs to the synthesizer are through J1 (J10 on the FDMA Digital board). The RF output is J2. Programming is through SPI signals, MOSI, SCK, and SYNTHEN-. The outputs of the two VCO's are summed together by a resistive network, R5, R6, R10 and R11.

C.4.10.1 Modulation

See figure C.4 diagram below. The option frequency synthesizer use a "two spot" modulation technique. The modulation is at a 3600 baud rate with frequency components well within and above the loop bandwidth. The low frequency modulation path, for frequencies within the loop bandwidth (less than 800 Hz), is through the normal control path. For frequency components above the loop bandwidth, the loop filter is too narrow for the control voltage to modulate the VCO so a second path around the loop filter is employed. The modulation for the higher frequency components is via VR3 and VR4.

C.4.10.2 Deviation

The modulation gain for frequencies within the loop filter bandwidth is known but the gain for frequencies above the loop filter bandwidth varies from unit to unit, with temperature and with frequency. Two separate settings are required to achieve the desired deviation during operation. One is the amplitude of the modulation signal sent to the option synthesizer and the other is the setting of the internal attenuator inside the fractional N chip. A calibration table calculates the required amplitude of the input signal and the setting of the internal attenuator based on operator selections from the front panel.

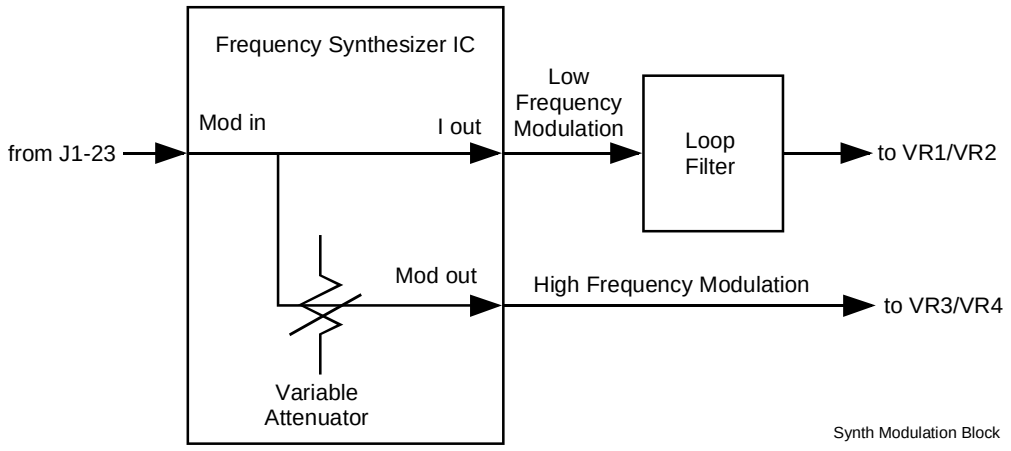


Figure C.4 Synthesizer Modulation Diagram

C.5 BLOCK DIAGRAM

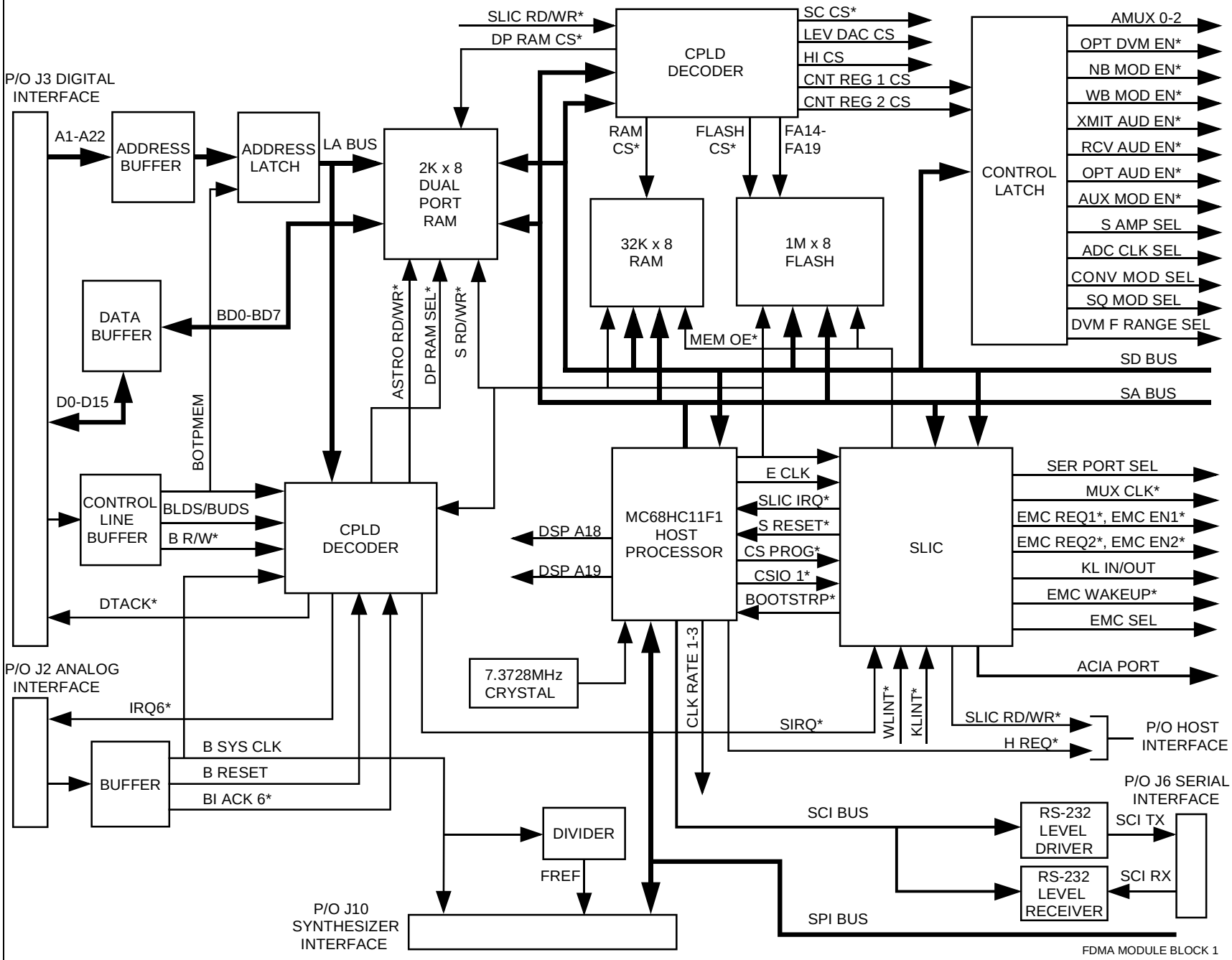


Figure C.5 FDMA Digital Block Diagram (1 of 6)

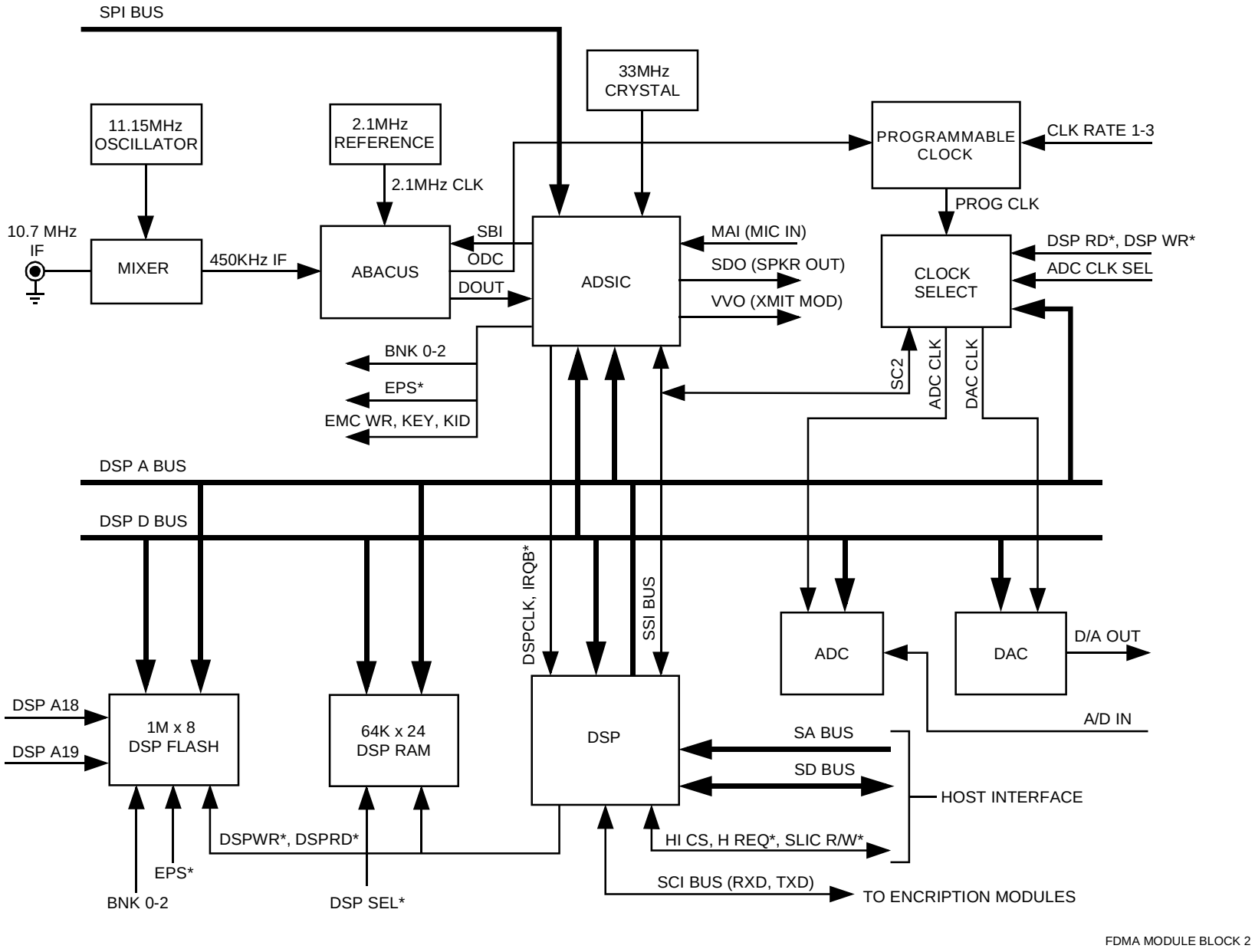
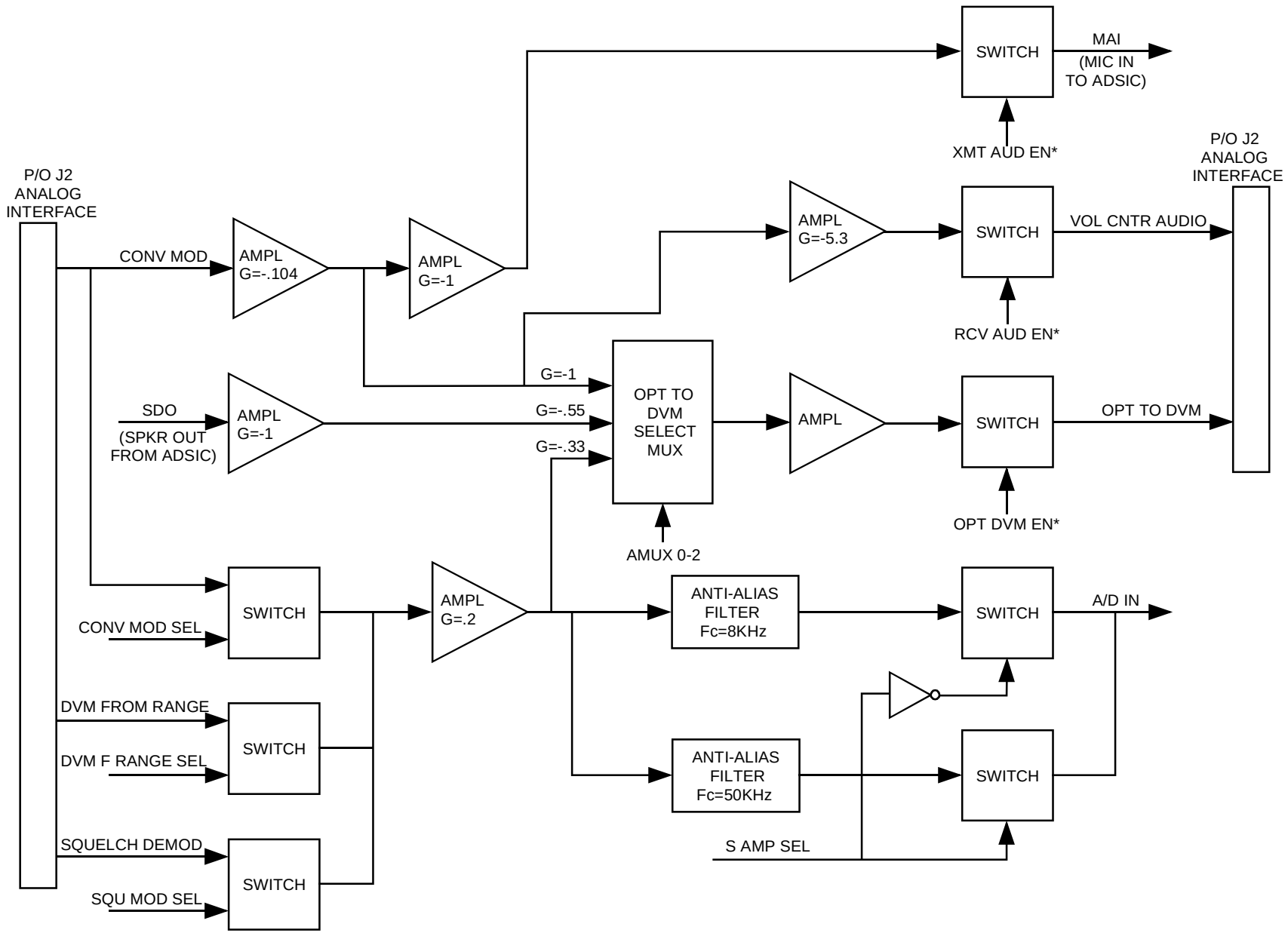


Figure C.5 FDMA Digital Block Diagram (2 of 6)

Figure C.5 FDMA Digital Block Diagram (3 of 6)



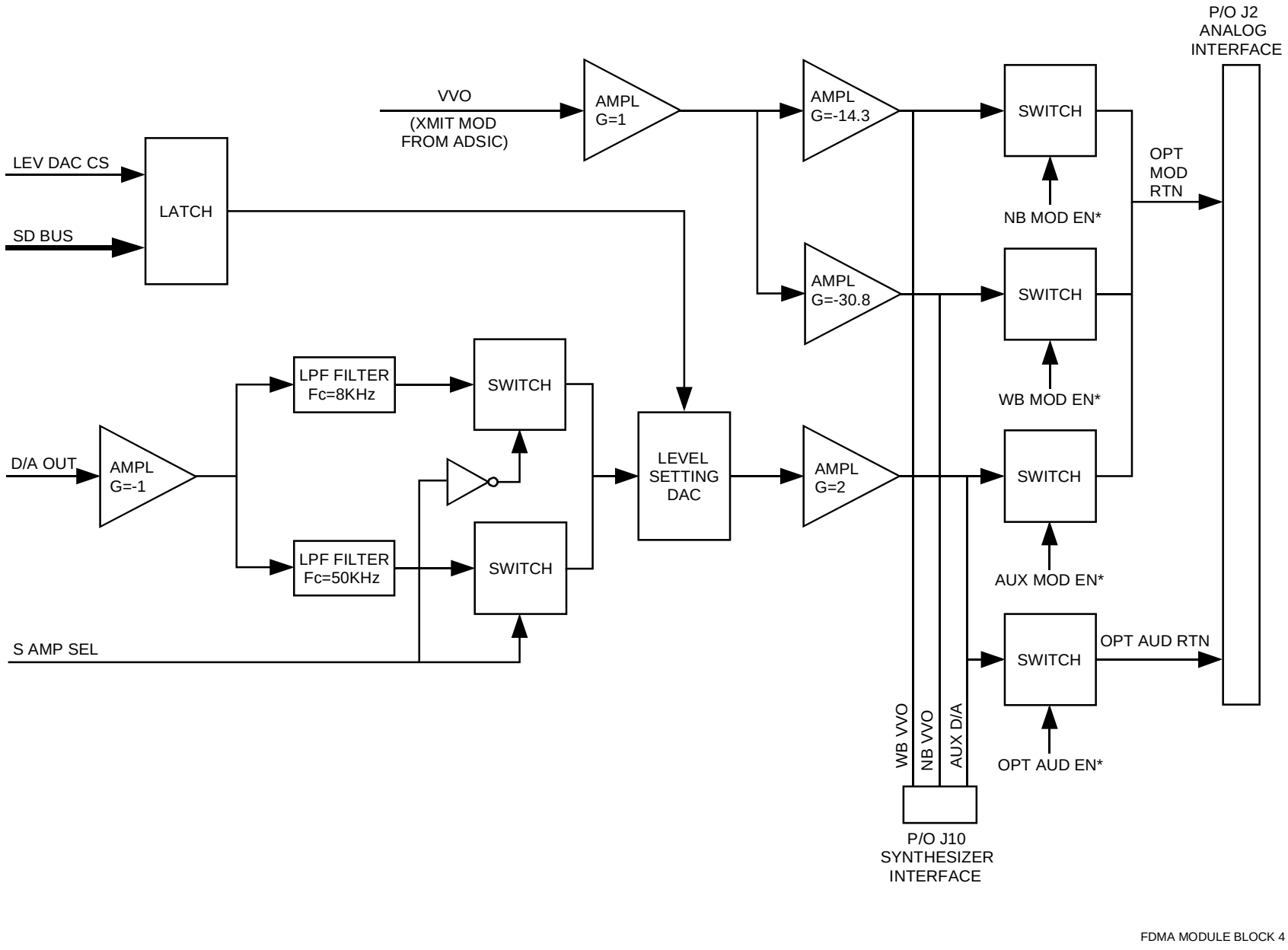
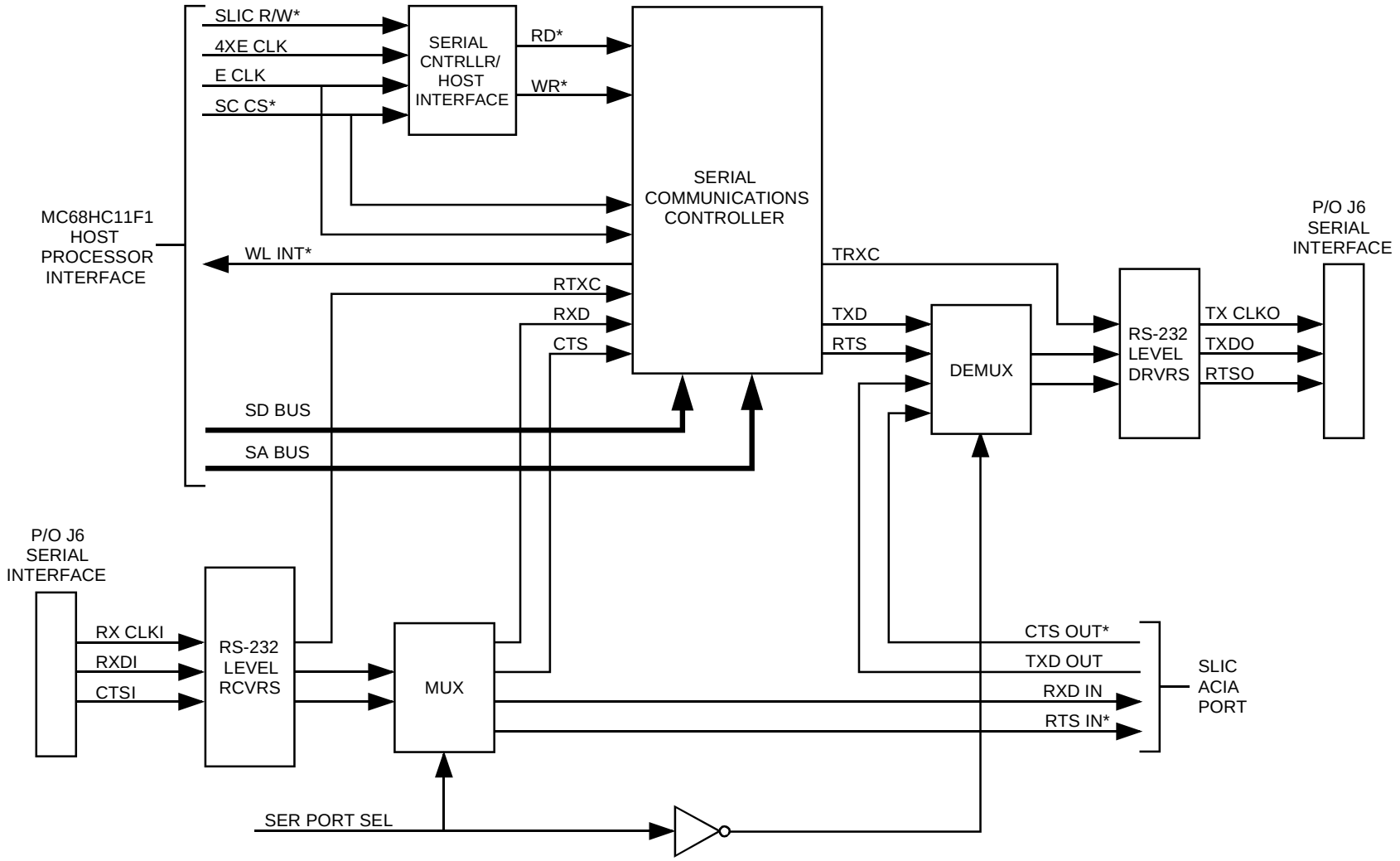


Figure C.5 FDMA Digital Block Diagram (4 of 6)

Figure C.5 FDMA Digital Block Diagram (5 of 6)



FDMA MODULE BLOCK 5

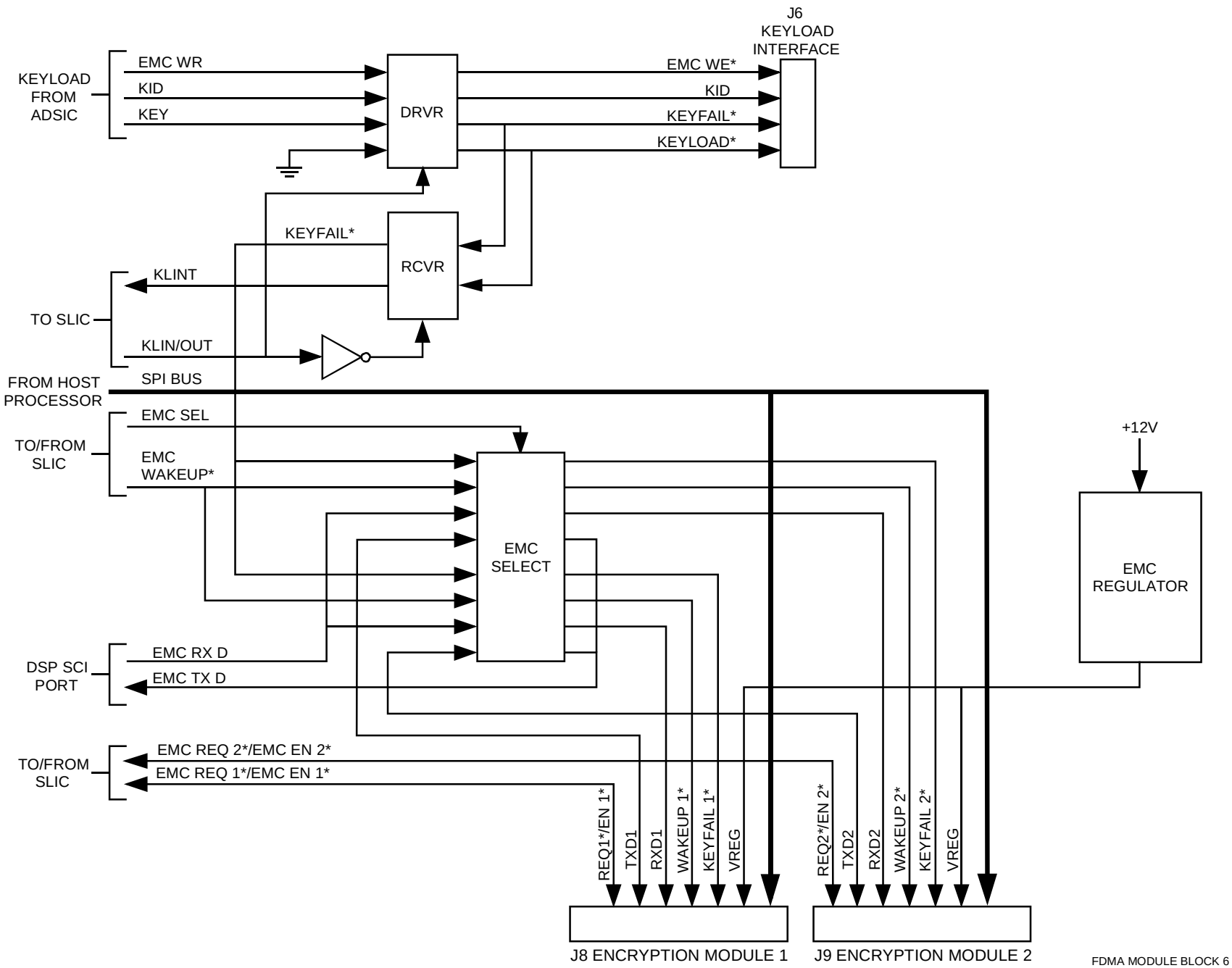
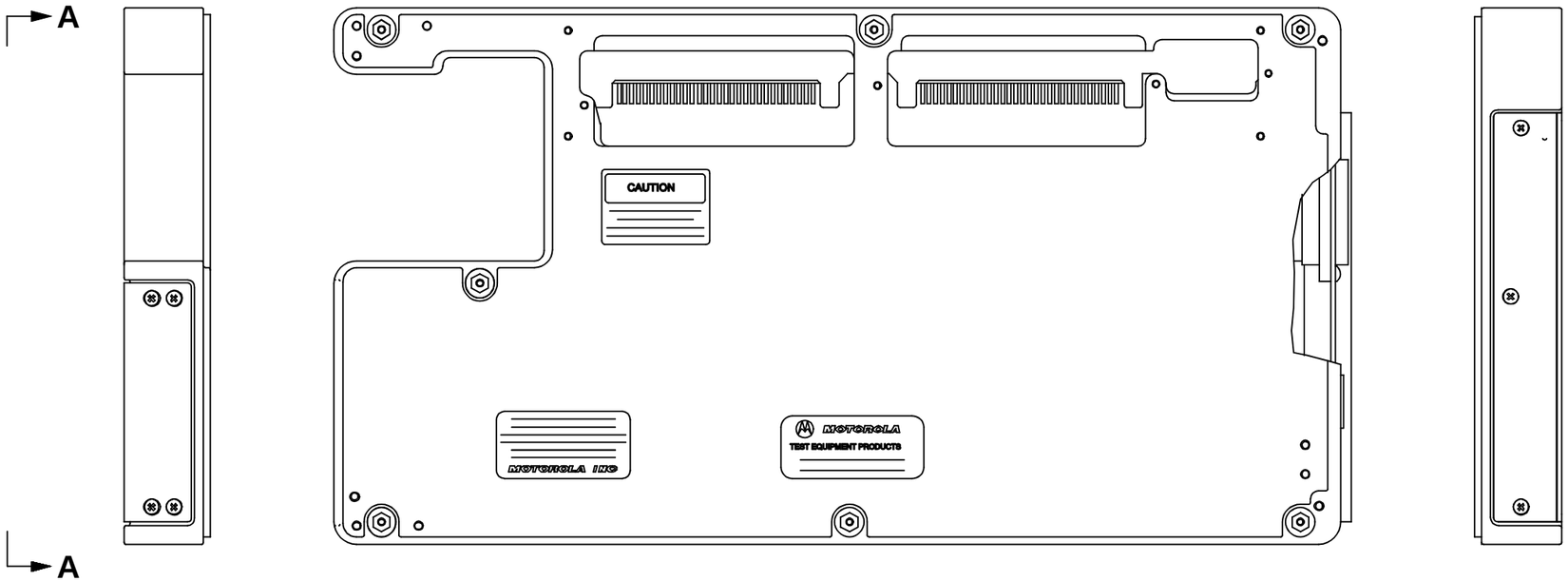
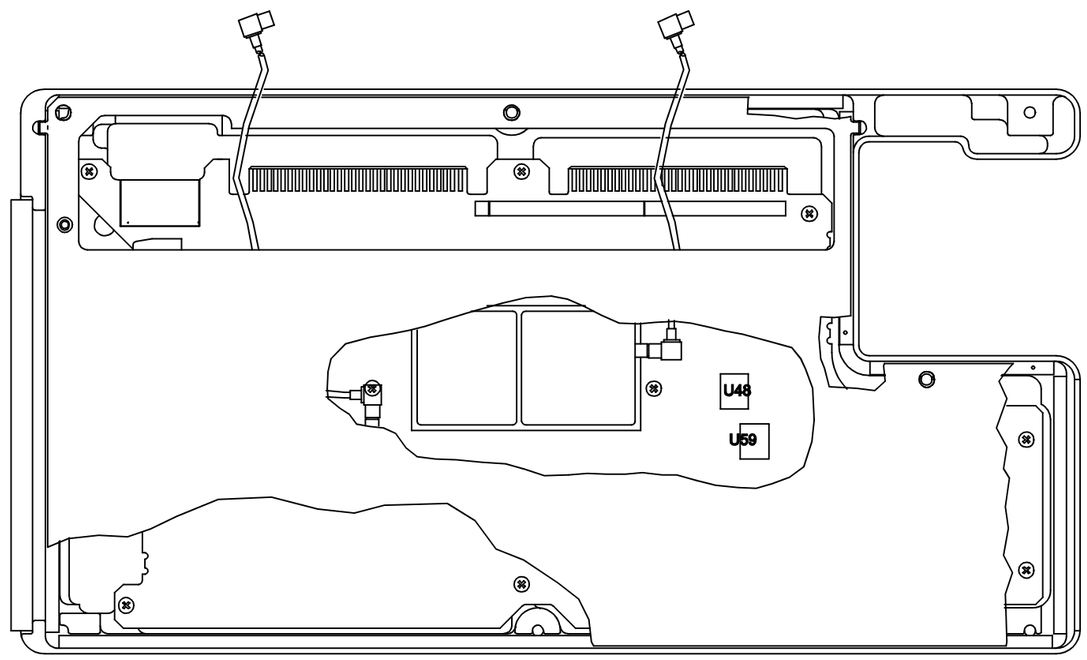


Figure C.5 FDMA Digital Block Diagram (6 of 6)



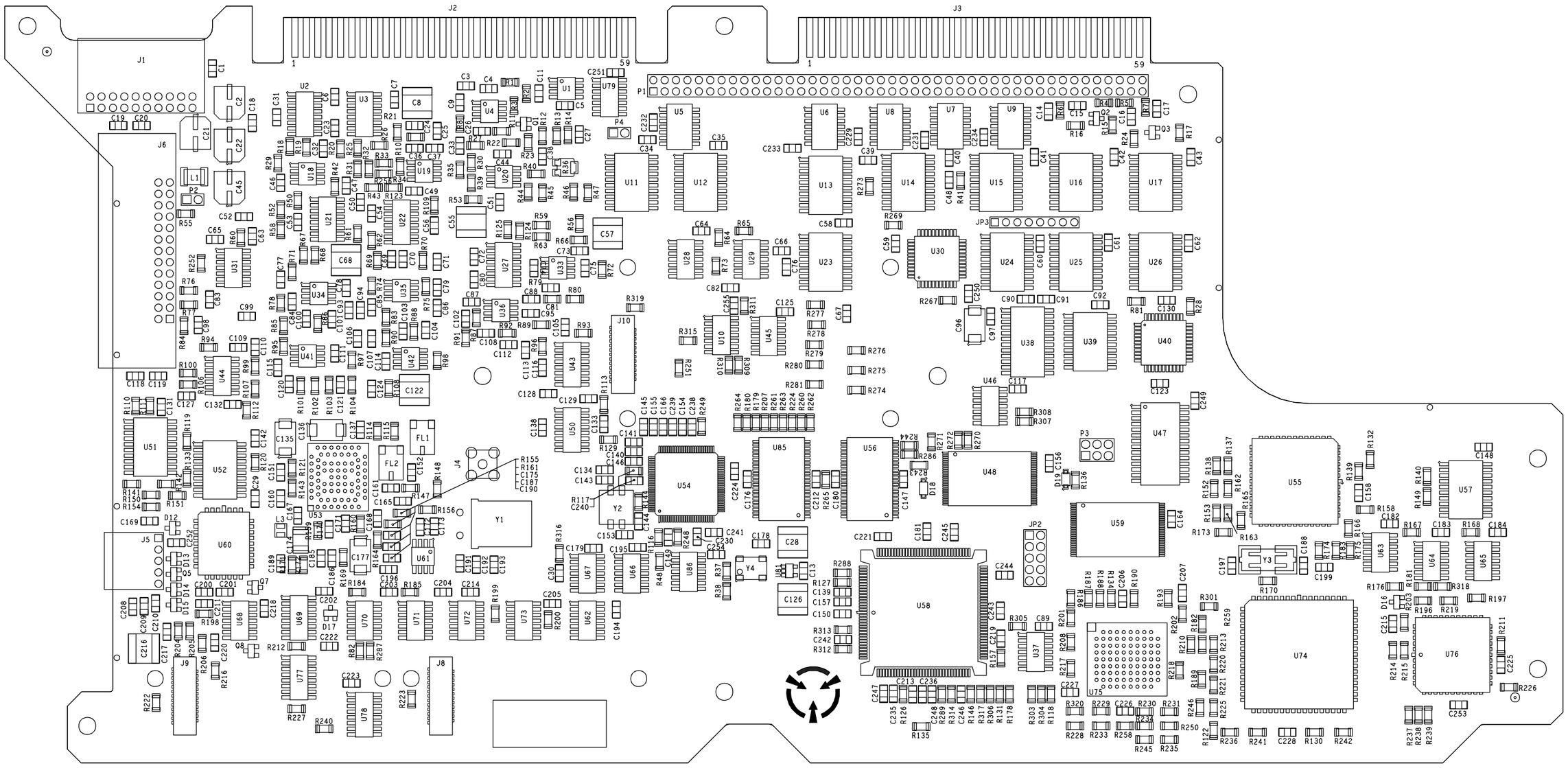


VIEW A-A

OPTION ASSEMBLY
HIGH-TIER

P30089C REV. H

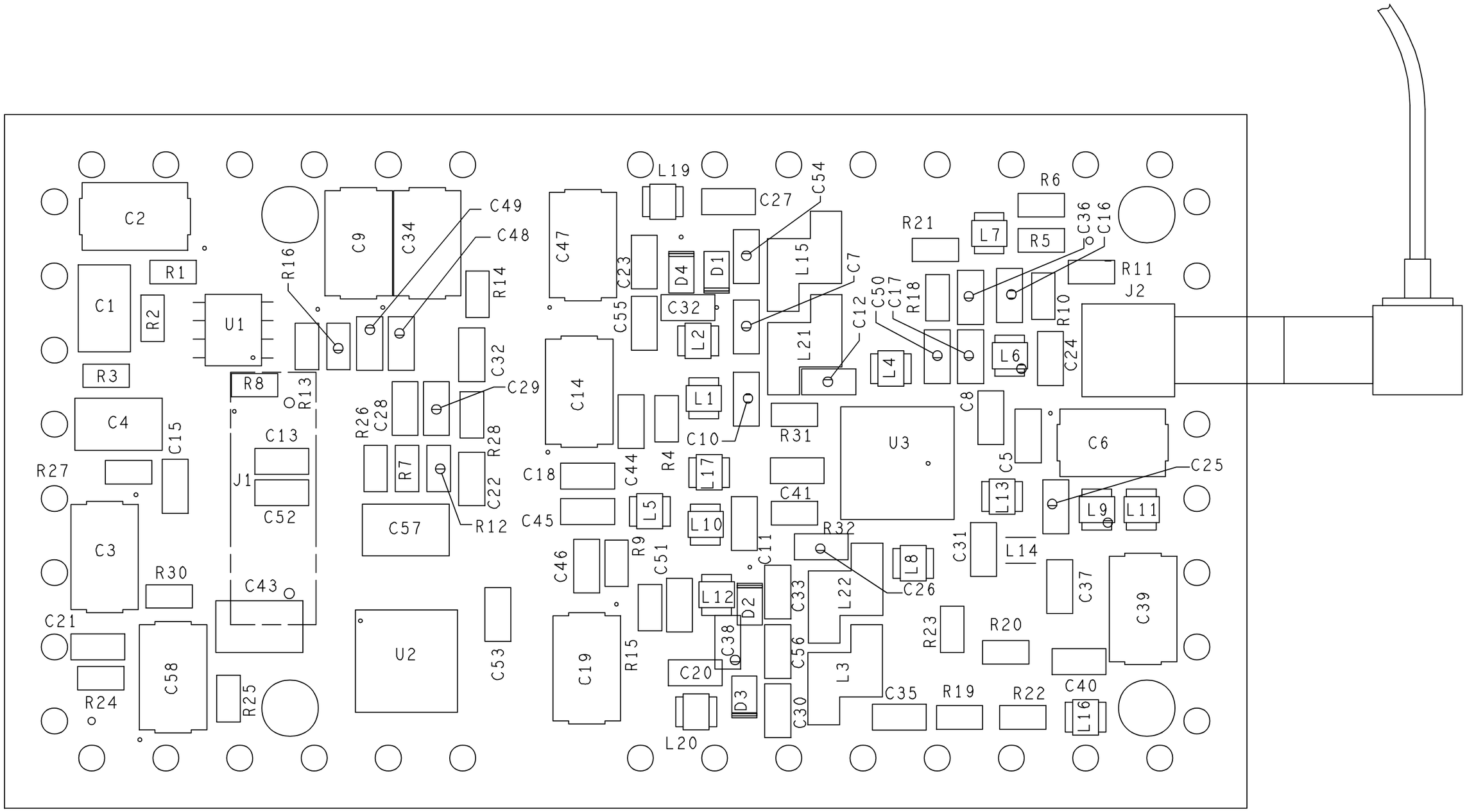
SHEET 1 OF 1



CIRCUIT CARD ASSEMBLY
HIGH - TIER

01-P57130J REV. D

SHEET 1 OF 1



CARD ASSEMBLY CONTROL
CHANNEL SYNTHESIZER

01-P30060C REV. D

SHEET 1 OF 1

DWG NO	63-P57132J	SH 1

REVISION HISTORY				
REV	DESCRIPTION		DATE	APPROVED
-	INITIAL RELEASE		03-01-00	C.GALLIGAN
A	MCO L48691-2	JFP 06-12-00	06-13-00	A.GATTO
B	PER CO L48767-3	LLB 00-12-08	00-12-12	A.GATTO
C	PER CO L48791-3	LLB 01-02-06	01-02-09	A.GATTO

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A18.

2. FOR REFERENCE DRAWINGS REFER TO:
   01-P57130J ASSEMBLY
   12-P57133J TEST PROCEDURE

3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS 1PCT .125W.
   ALL VOLTAGES ARE IN DC.
   ALL CAPACITORS ARE IN MICROFRAUDS 5PCT 50V.
   ALL INDUCTORS ARE IN MICROHENRYS 10PCT.

4. TERMINATIONS CODED WITH THE SAME LETTER ARE ELECTRICALLY CONNECTED.

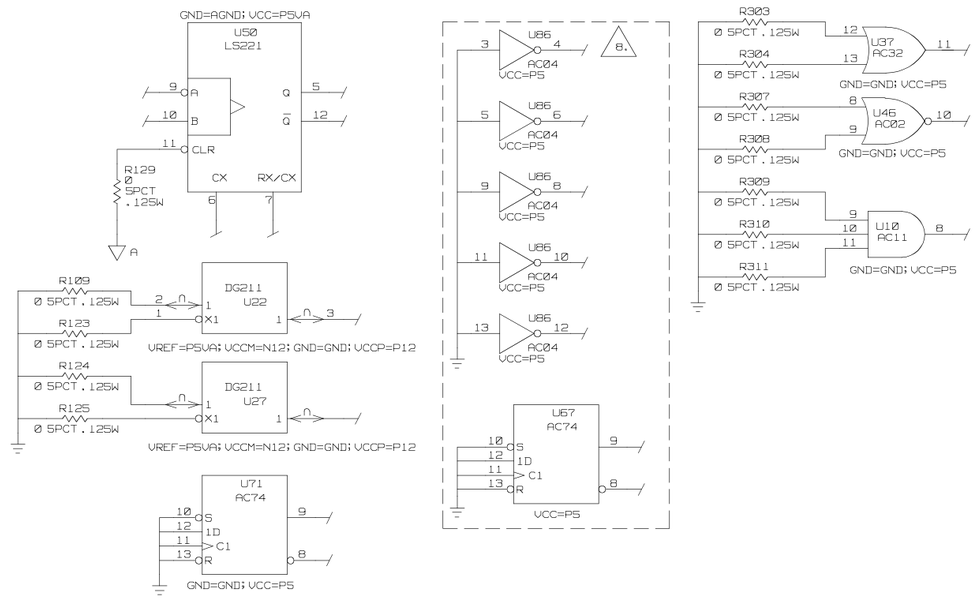
5. DEVICE TYPE NUMBERS AND CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE I.

6. DO NOT INSTALL.

7. FOR -001 CONFIGURATION, P3-4 TO P3-2, P3-3 TO P3-1.
   FOR -002 CONFIGURATION, P3-4 TO P3-6, P3-3 TO P3-5.

8. IF PENDULUM OSCILLATOR U60 IS USED, DO NOT INSTALL.

9. SYMBOL > FOLLOWING AN OFFPAGE REFERENCE INDICATES THAT THE SIGNAL IS DRIVEN BY THE CORESPONDING SIGNAL ON THE PAGE REFERENCED. SYMBOL < INDICATES THAT THE SIGNAL DRIVES THE CORESPONDING SIGNAL ON THE PAGE REFERENCED.



NC J1-4	OPTAUDIORTN2 J2-32	IACK2_N J2-54	NC J6-21	NC J9-16
NC J1-8	GND J2-33	IACK1_N J2-55	NC J6-23	NC J9-17
NC J1-14	IRQ_N(1) J2-34	TRIGGER J2-56	NC J6-25	NC J9-18
NC J1-18	IRQ_N(2) J2-35		NC J6-26	NC J9-19
	IRQ_N(4) J2-37	OPTDET1_N J3-50		NC J9-23
DVM J2-1	IRQ_N(5) J2-38	GND J3-56	NC J8-13	NC J9-24
GENAUDIO J2-3	IRQ_N(7) J2-40	OPTTOCNTR J3-59	NC J8-14	NC J9-25
WBNB_N J2-6	BTIMERCLK J2-41		NC J8-16	
EXTMODMICIN J2-9	ADD(7) J2-42	NC J6-4	NC J8-17	
HANDSETAUDIO J2-11	ADD(6) J2-43	NC J6-10	NC J8-18	
RAWMICIN J2-12	ADD(5) J2-44	NC J6-11	NC J8-19	
RCVSPKRAUDIO J2-13	ADD(4) J2-45	NC J6-12	NC J8-23	
DEMOD CAL AUDIO J2-15	ADD(3) J2-46	NC J6-14	NC J8-24	
DCINPUTP J2-16	ADD(2) J2-47	NC J6-15	NC J8-25	
MIC IN J2-17	ADD(1) J2-48	NC J6-16	NC J8-5	
EXTMODIN J2-18	ADD(0) J2-49	NC J6-17		
SQUELCHED DEMOD J2-19	IACK7_N J2-50	NC J6-18	NC J9-5	
INTMOD J2-20	IACK5_N J2-52	NC J6-19	NC J9-13	
OPTMODRTN1 J2-29	IACK4_N J2-53	NC J6-20	NC J9-14	

REFERENCE DESIGNATIONS	
HIGHEST NUMBER USED	NOT USED
C255	C10, C12, C158, C162, C163, C198, C237
D19	D1-D11
FL2	
J10	J7
JP3	JP1
L4	L2, L4
P2	
Q8	Q4, Q6
R320	R9, R49, R51, R54, R57, R105, R128, R145, R177, R191, R192, R194, R195, R209, RR232, 247, R253-R255, R257, R266, R268, R282-R285, R290-R300, R302
TP21	TP1, TP21
U300	U32, U49, U80, U82-U84, U88-U300
Y4	

ALL SHEETS ARE THE SAME REVISION STATUS

		CONTR	
		ISS	B35550-452(-)00-03-01
		APPROVALS	
		DWN	I.DEL BARCO 00-02-02
		CHKR	
		QA	T.DAVINO 00-03-01
		MATL	W.MCDONALD 00-03-01
01-P57130J	COCHISE	MFG	J.HARNISH 00-02-29
NEXT ASSY	USED ON	ENG	A.GATTO 00-02-29
APPLICATION		CUST	

MOTOROLA, INC.
SCOTTSDALE, ARIZONA 85252-1417

TITLE
SCHEMATIC DIAGRAM, HI-TIER

SIZE	CAGE CODE	DWG NO
D	94990	63-P57132J

SCALE NONE SHEET 1 OF 23

TABLE I 5.

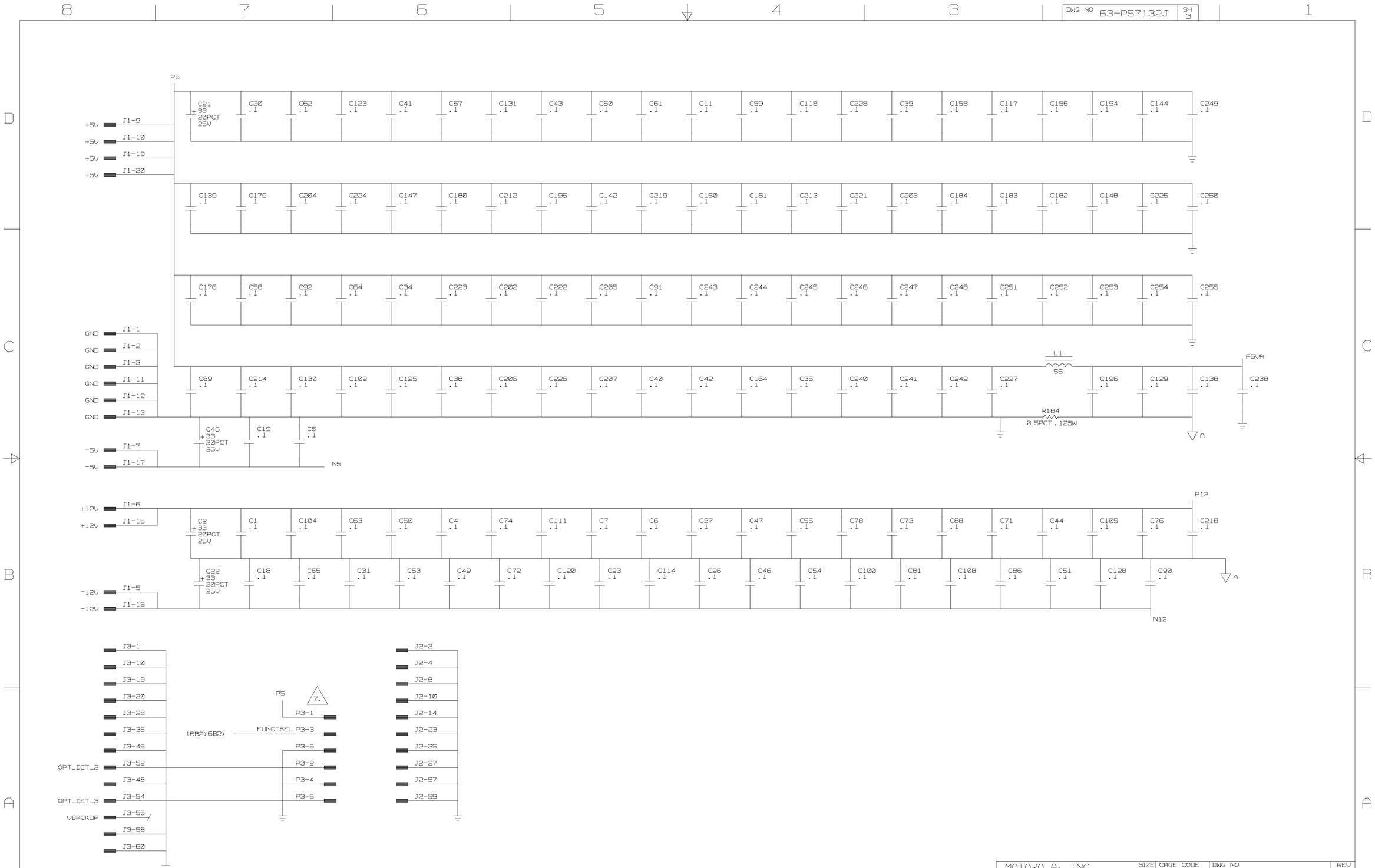
REF DES	DEVICE TYPE	VCC CONNECTION		GND	AGND	N/C CONNECT	PAGE FOUND ON
		CONN	VOLTS				
U1	LT1016	1,4	+5	6			5
U2	DG211	13	+12	5			19,23
		4	-12				
		12	+5VA				
U3	DG211	13	+12	5			19,20
		4	-12				
		12	+5VA				
U4	MC34072	8	+12				19,20
		4	-12				
U5	1405-331/471G						7
U6	1405-331/471G						7
U7	1405-331/471G						7
U8	1405-331/471G						7
U9	1405-331/471G						7
U10	74AC11D	14	+5	7			10
U11	74ACT374	20	+5	10			13
U12	74ACT374	20	+5	10			13
U13	74ACT245	20	+5	10			6
U14	74ACT244	20	+5	10			5
U15	74ACT244	20	+5	10			4
U16	74ACT244	20	+5	10			4
U17	74ACT244	20	+5	10			4
U18	MC34072	8	+12				19
		4	-12				
U19	MC34072	8	+12				19,20
		4	-12				
U20	MC34072	8	+12				23
		4	-12				
U21	DG508	13	+12		14		19
		3	-12				
U22	DG211	13	+12	5			20,23
		4	-12				
		12	+5VA				
U23	74ACT374	20	+5	10			23
U24	74ACT374	20	+5	10			4
U25	74ACT374	20	+5	10			4
U26	74ACT374	20	+5	10			4
U27	DG211	13	+12	5			19,20,23
		4	-12				
		12	+5VA				

TABLE I 5.

RES DES	DEVICE TYPE	VCC CONNECTION		GND	AGND	N/C CONNECT	PAGE FOUND ON
		CONN	VOLTS				
U28	74AC04	14	+5	7		+5	10,18 20,23
U29	MC1723	12	+12	7		+12	20
U30	M4A5-32/32-5VC	16,38	+5	6,17,28,39		+5	5
U31	DS14C88	14	+12	7			21
		1	-12				
U33	MC34072	8	+12				23
		4	-12				
U34	MC34072	8	+12				20
		4	-12				
U35	MC34072	8	+12				23
		4	-12				
U36	MC34072	8	+12				23
		4	-12				
U37	74AC32	14	+5	7		+5	18
U38	AD7572A	24	+5	12	3		18
		23	-12				
U39	PM7545	18	+5	3	2		23
U40	M4A5-32/32-5VC	16,38	+5	6,17,28,39			6
U41	MC34072	8	+12				19
		4	-12				
U42	MC34072	8	+12				19
		4	-12				
U43	DAC08	1	+12				23
		7	-12				
U44	DS14C89A	14	+5	7			21
U45	74AC00	14	+5	7			12
U46	74AC02	14	+5	7			4.8.10
U47	M5M5256	28	+5	14			13
U48	AM29F800BT-55	37	+5	27,46			8
U50	74LS221	3,16	+5VA		1,8		20
U51	74ACT244	20	+5	10			14
U52	74ACT244	20	+5	10			15
U53	5105457W20						11
U54	5105457W19	A7	+5	K10,L2, A6,A9			9
U55	IDT7132	52	+5	26			8
U56	IDT71016S12PH		+5				10
U57	74ACT244	20	+5	10			21
U58	DSP56002	9,12,20, 27,40,50 58,66,81, 89,93,103 115,123, 129,140	+5	7,14,21,23, 29,34,42,47 54,57,69,79, 85,90,94,99, 105,112,118, 124,125,132, 137,143			12
U59	AM29F800BT-55	37	+5	27,46			13
U60	KXN1155AF	13	+5	26			11

TABLE I 5.

RES DES	DEVICE TYPE	VCC CONNECTION		GND	AGND	N/C CONNECT	PAGE FOUND ON
		CONN	VOLTS				
U61	NE602	8	+5VA		3		17
U62	74AC04	14	+5	7			8,9,13, 14,17
U63	74AC04	14	+5	7			14,21
U64	74AC74	14	+5	7			21
U65	74AC10	14	+5	7			21
U66	74AC74	14	+5	7			11
U67	74AC74	14	+5	7			11
U68	MC1723	12	+12	7			15
U69	74AC163	16	+5	8			17
U70	74AC04	14	+5	7			8,15,17
U71	74AC74	14	+5	7			17
U72	74AC00	14	+5	7			17,18
U73	74AC74	14	+5	7			17
U74	MC68HC11F1	34	+5	1			16
U75	5105750U31	12,35, 52,75	+5	21,43,44,66			14
U76	Z85230	10	+5	35			21
U77	74AC163	16	+5	8			17
U78	74AC163	16	+5	8			17
U79	74AC74	14	+5	7			22
U81	LT1761-3	1	+5	2			11
U85	IDT71016S12PH						10
U86	74AC04	14	+5	7			11



MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57132J	REV C
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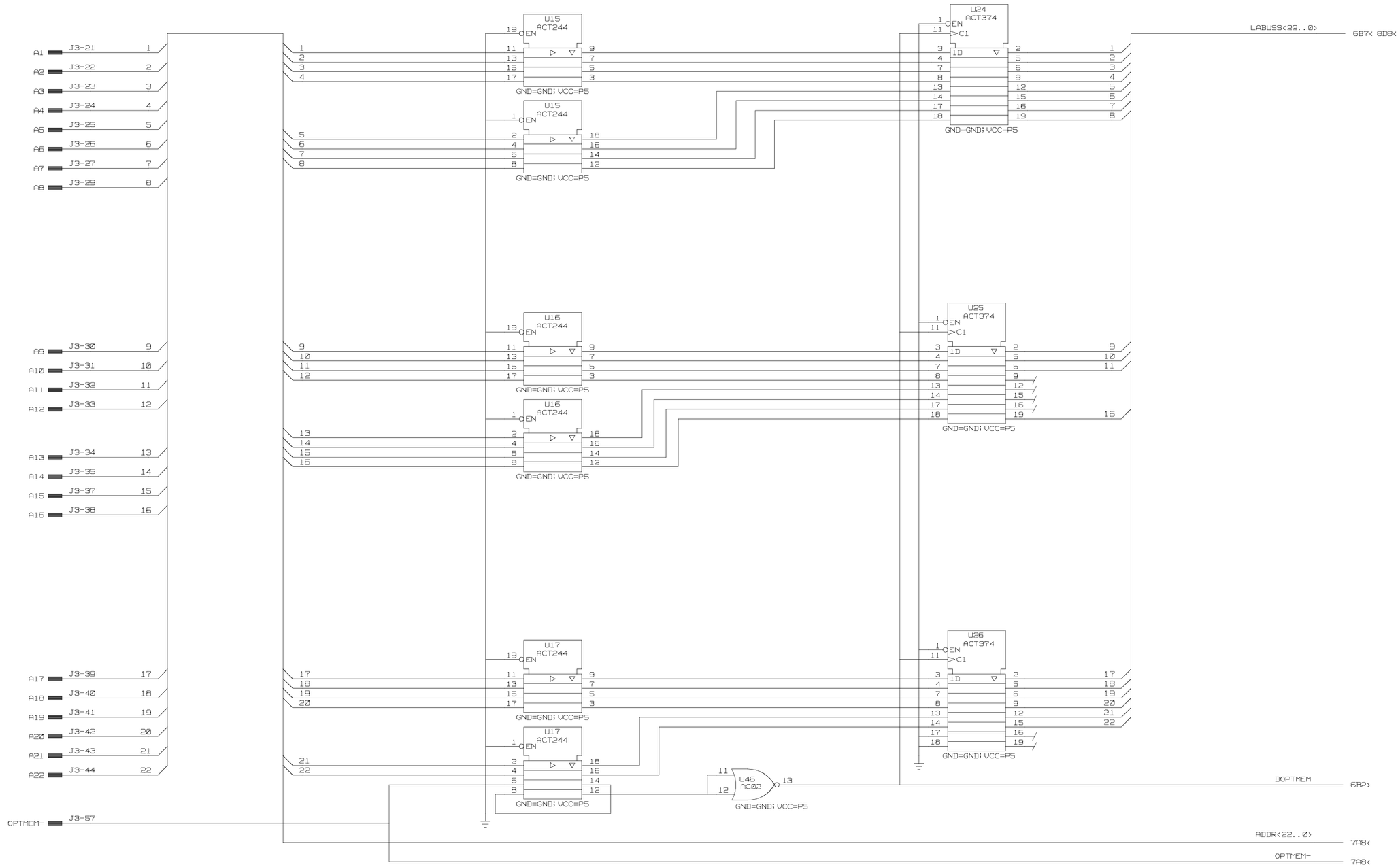
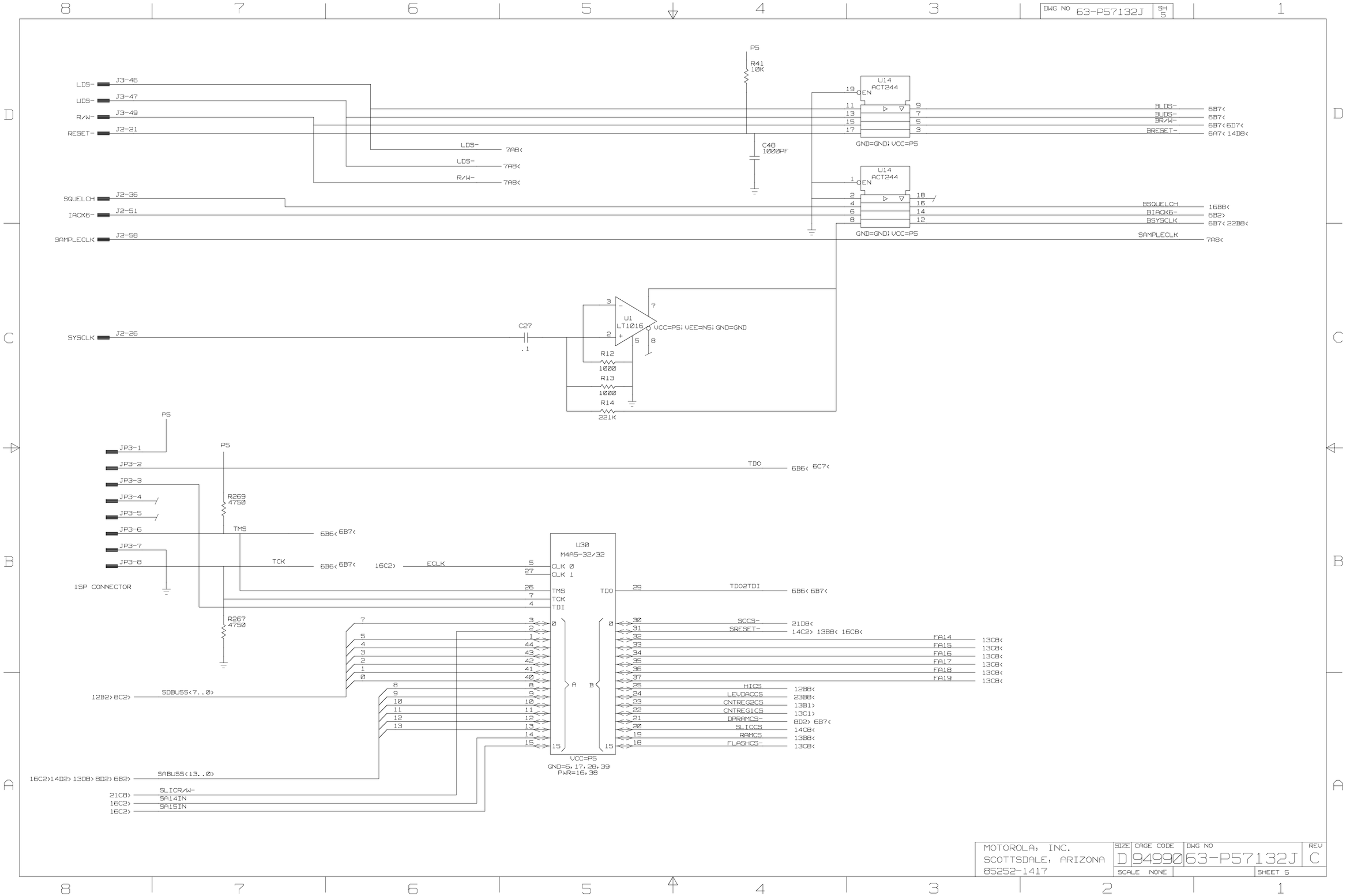
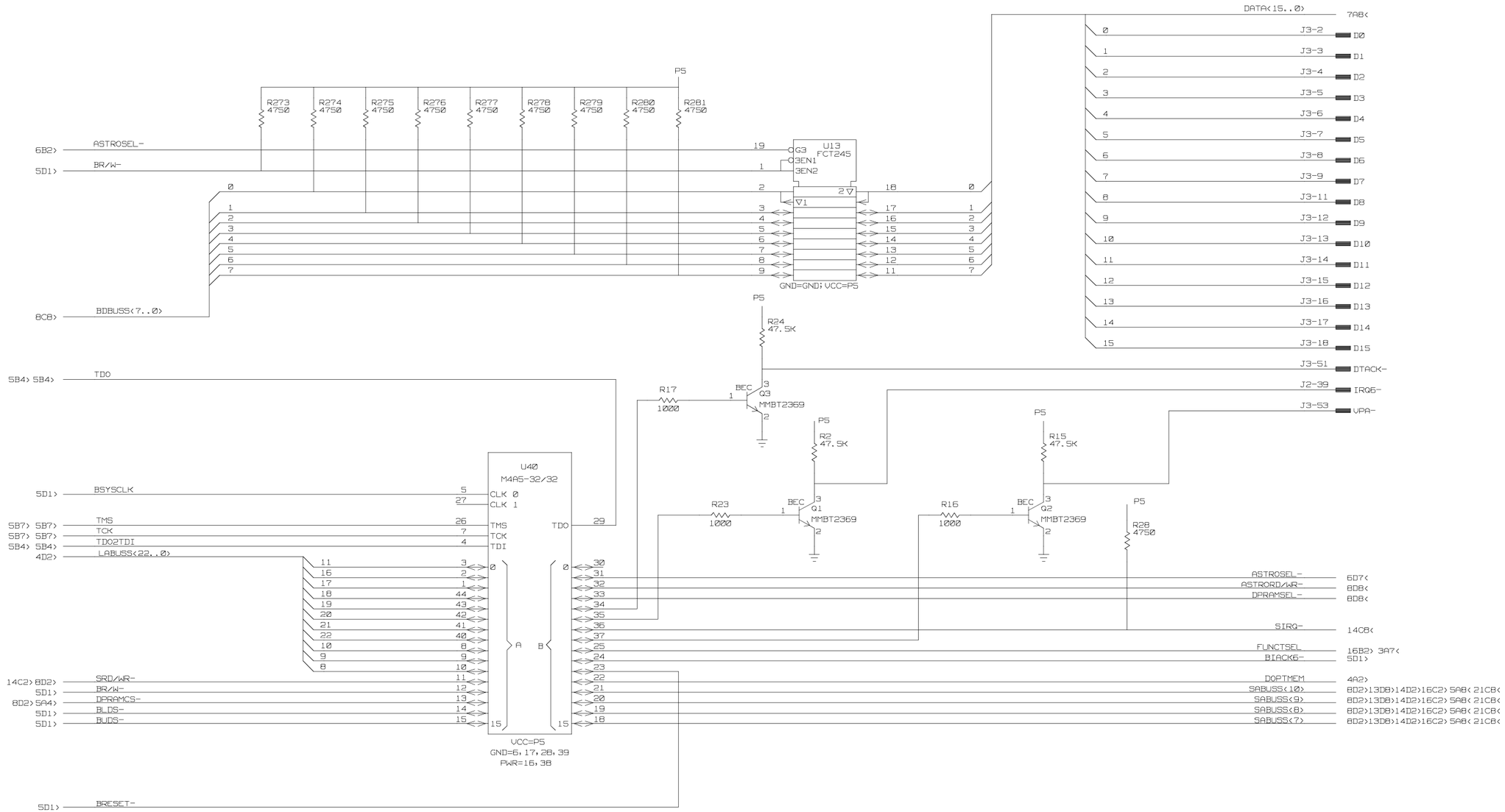


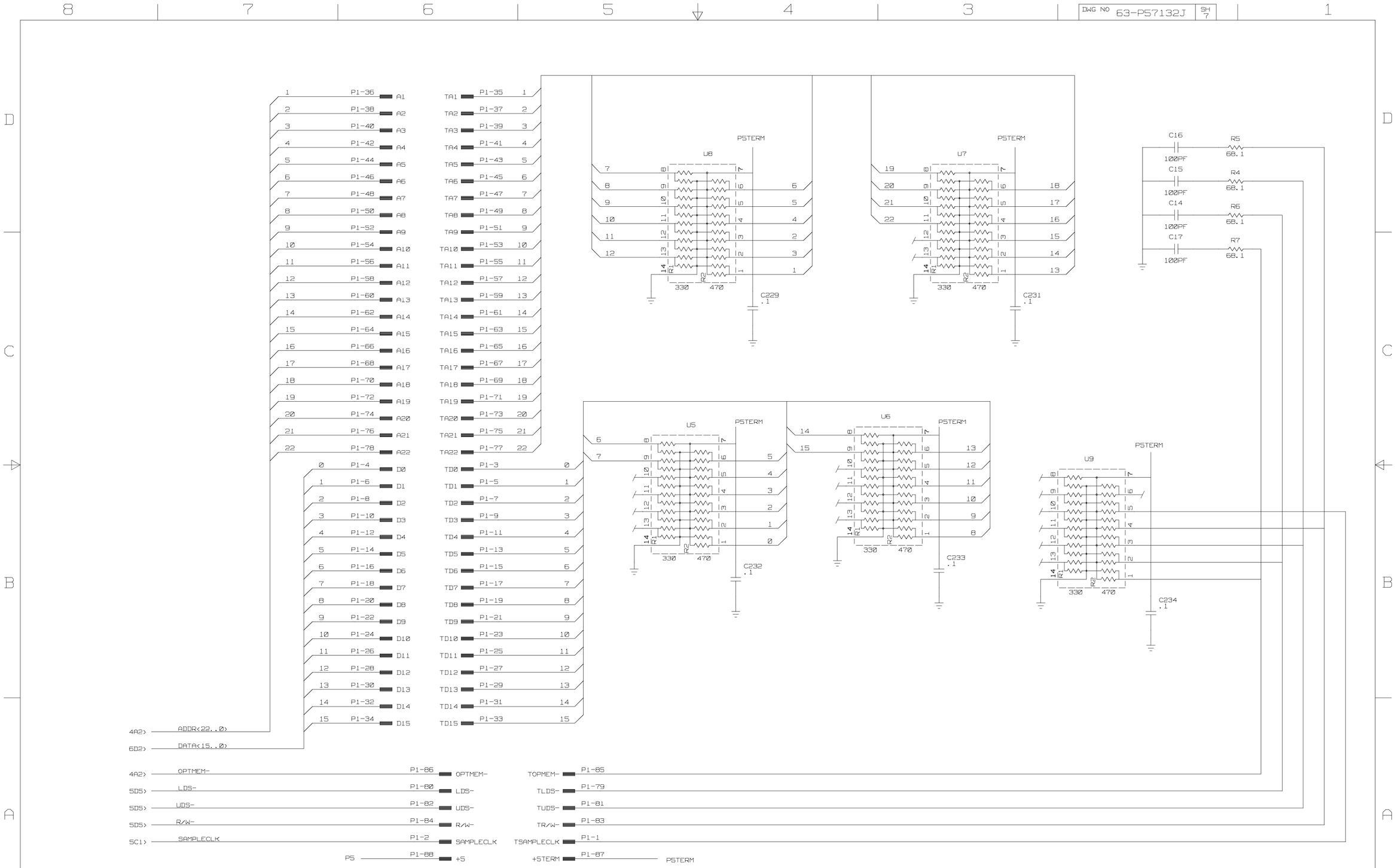
MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57132J	REV C
	SCALE NONE		SHEET 4	



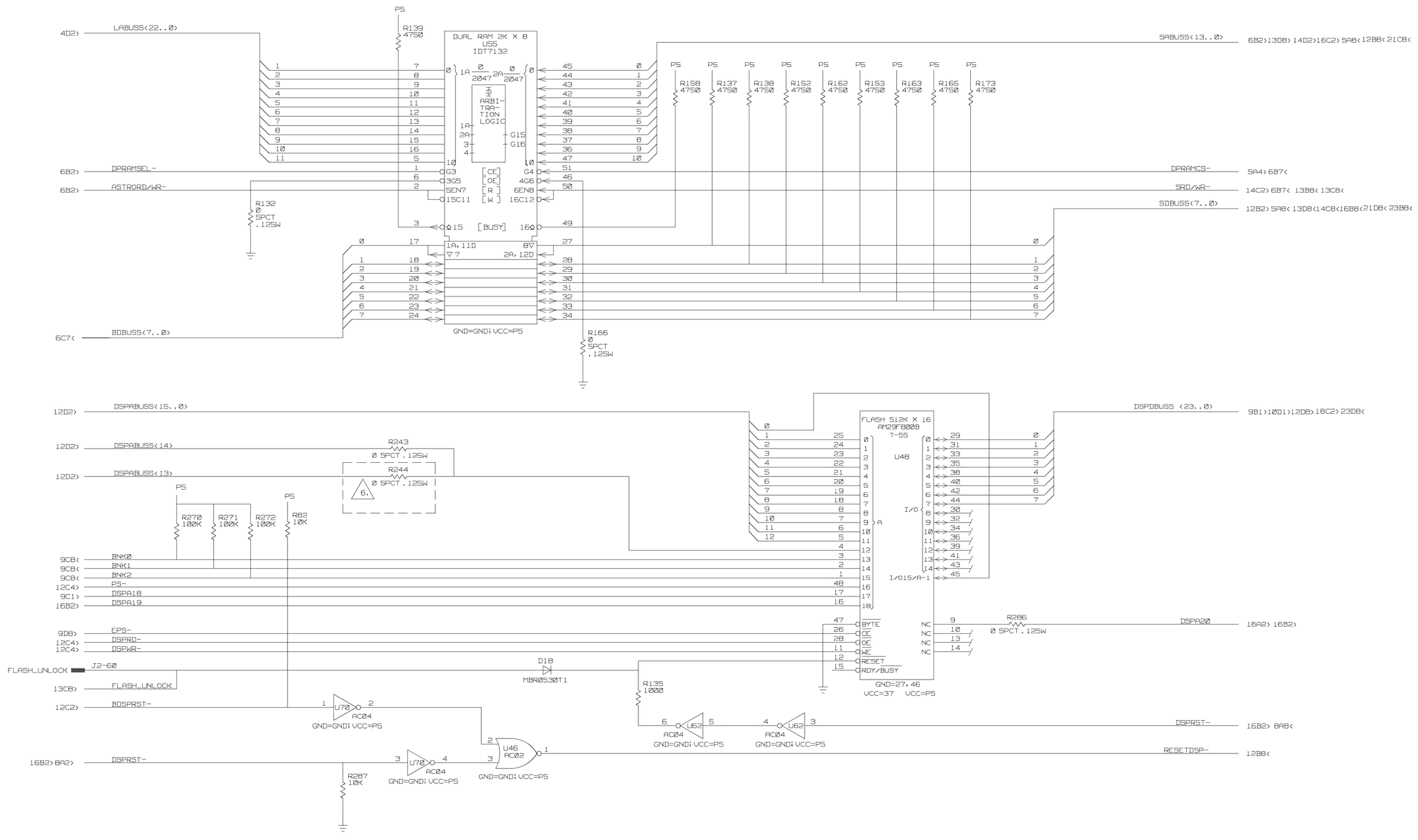
MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57132J	REV C
	SCALE NONE			SHEET 5



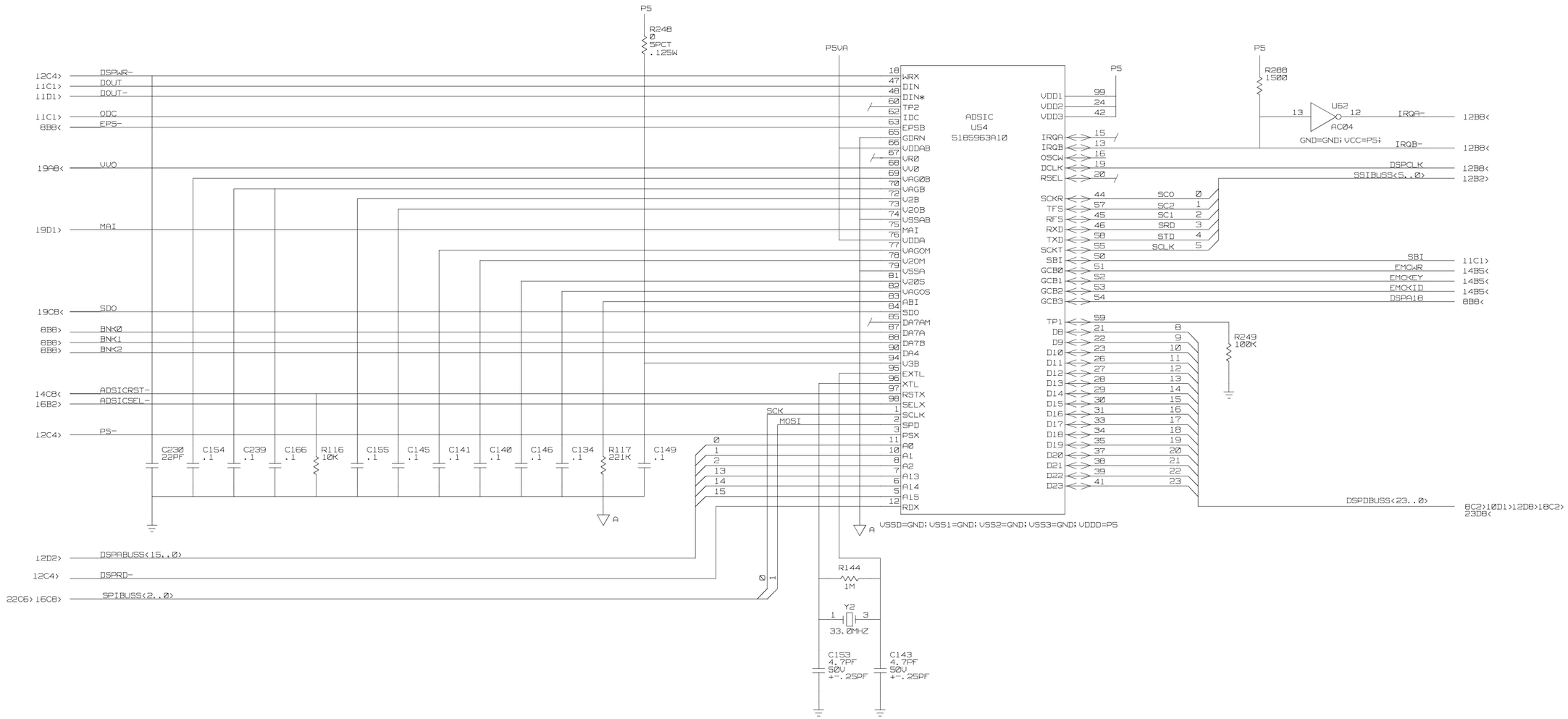
MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57132J	REV C
	SCALE NONE		SHEET 6	



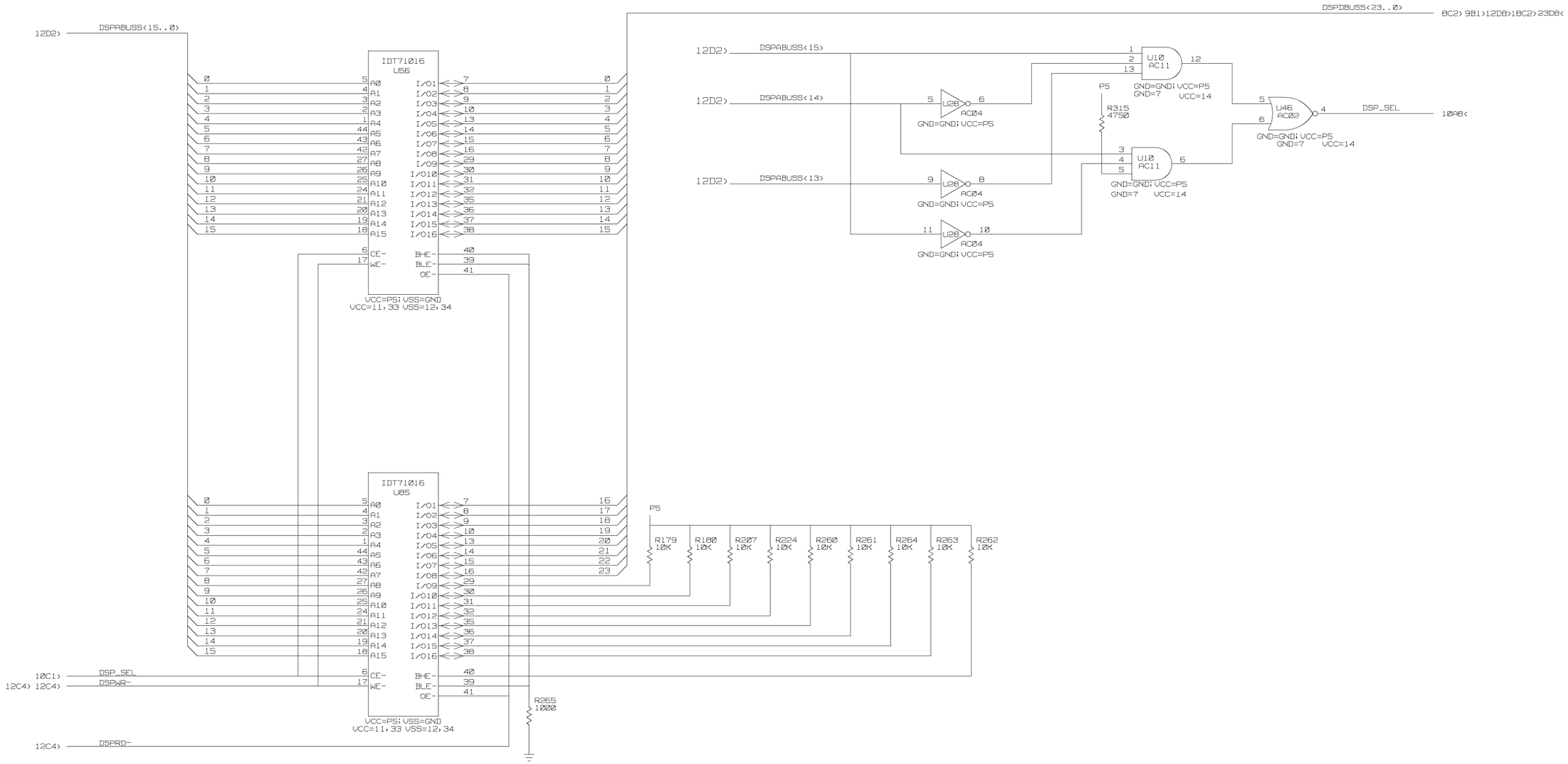
MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57132J	REV C
	SCALE NONE		SHEET 7	



MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57132J	REV C
	SCALE NONE		SHEET 8	



MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57132J	REV C
	SCALE NONE		SHEET 9	



MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57132J	REV C
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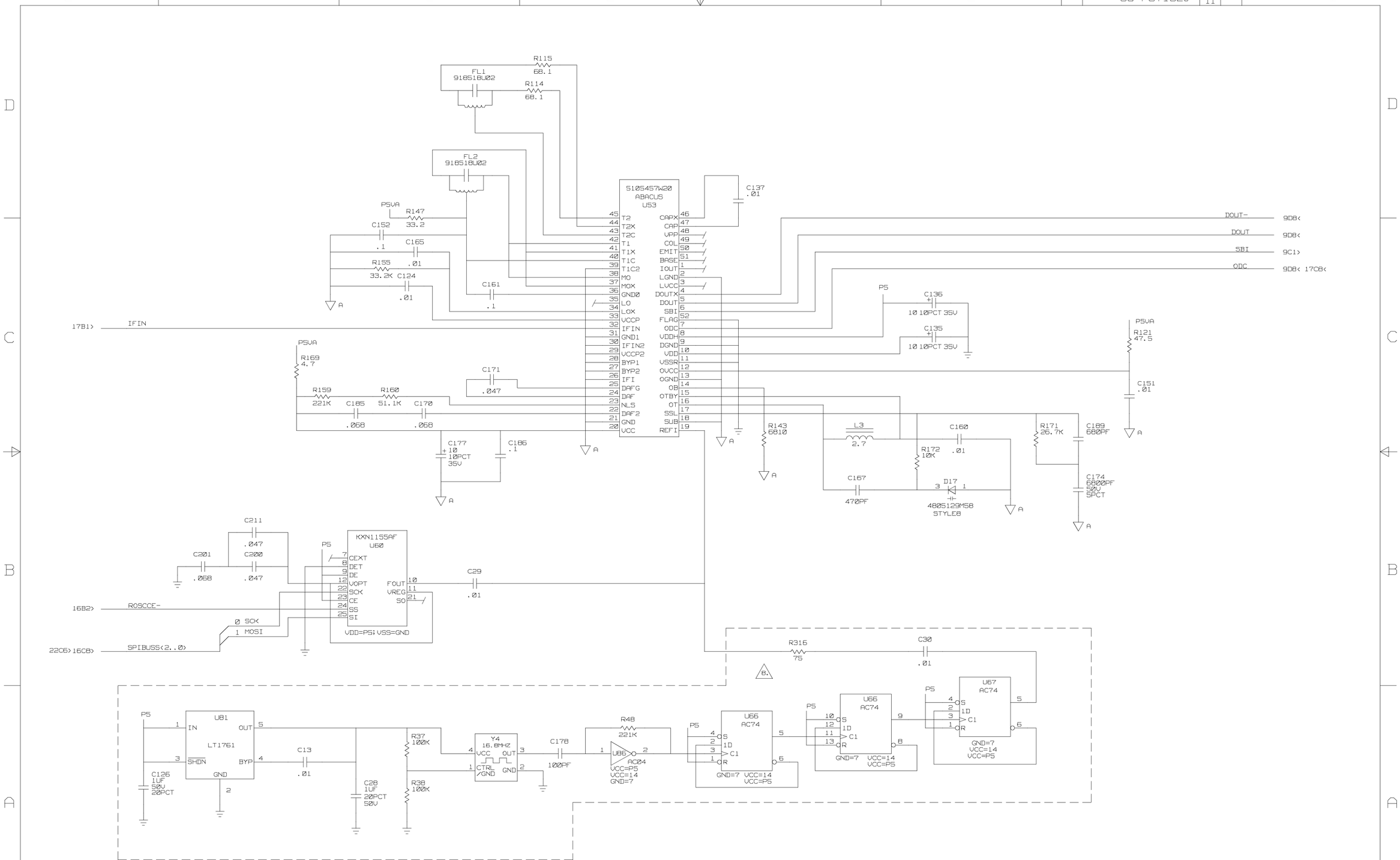
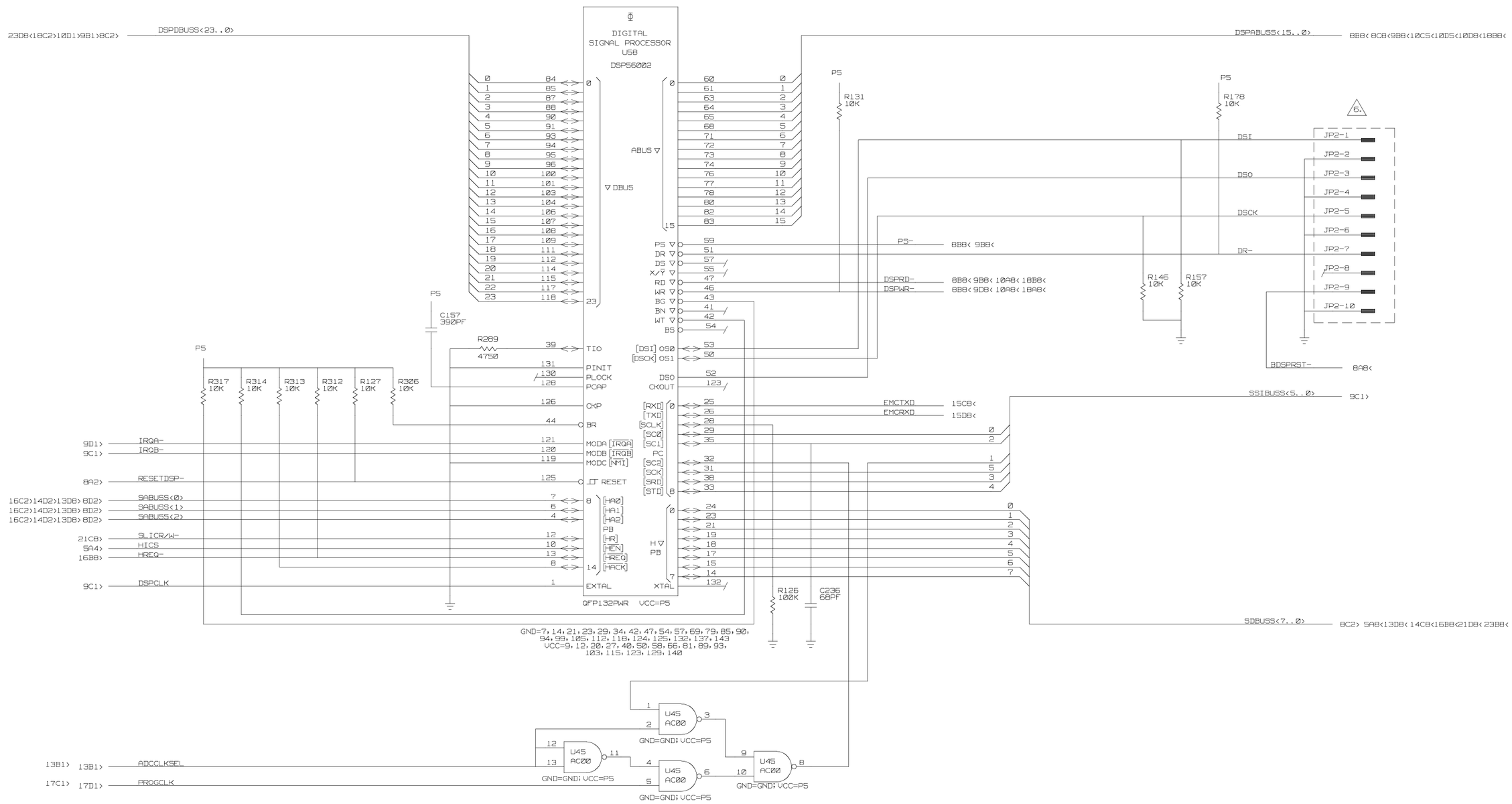
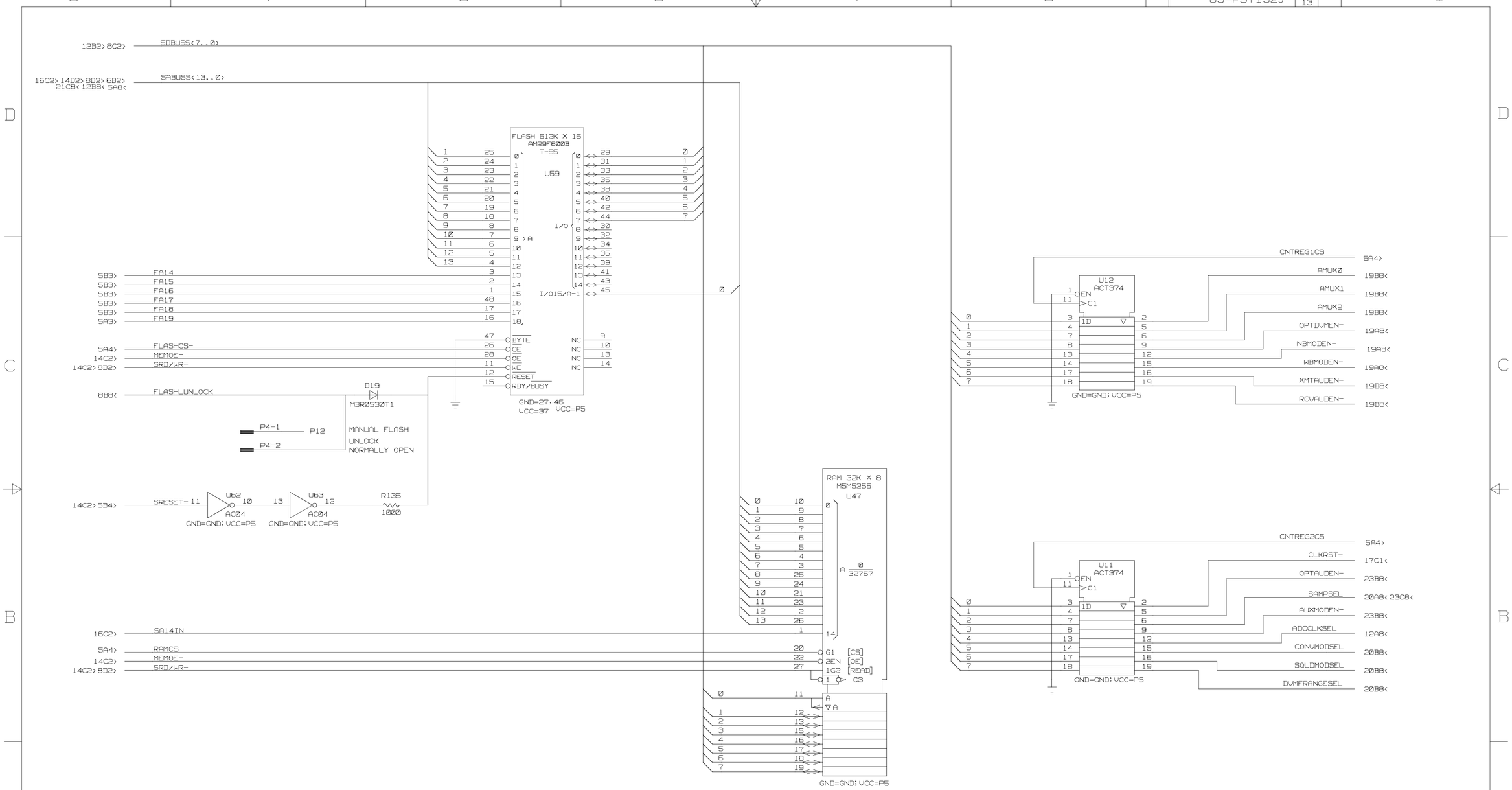


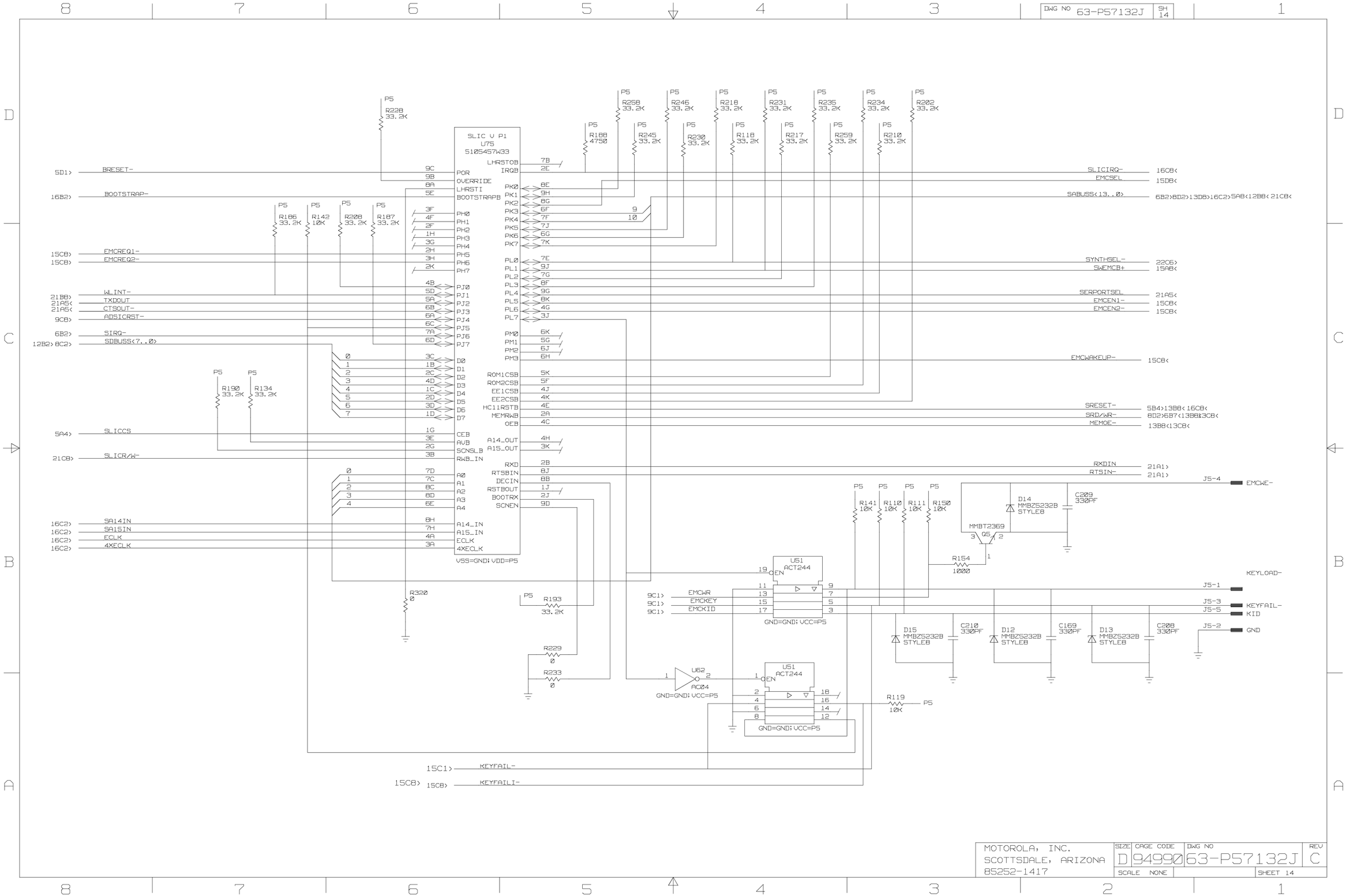
MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57132J	REV C
	SCALE NONE		SHEET 11	



MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57132J	REV C
	SCALE NONE		SHEET 12	



MOTOROLA, INC. SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P57132J	REV C
	SCALE NONE		SHEET 13	



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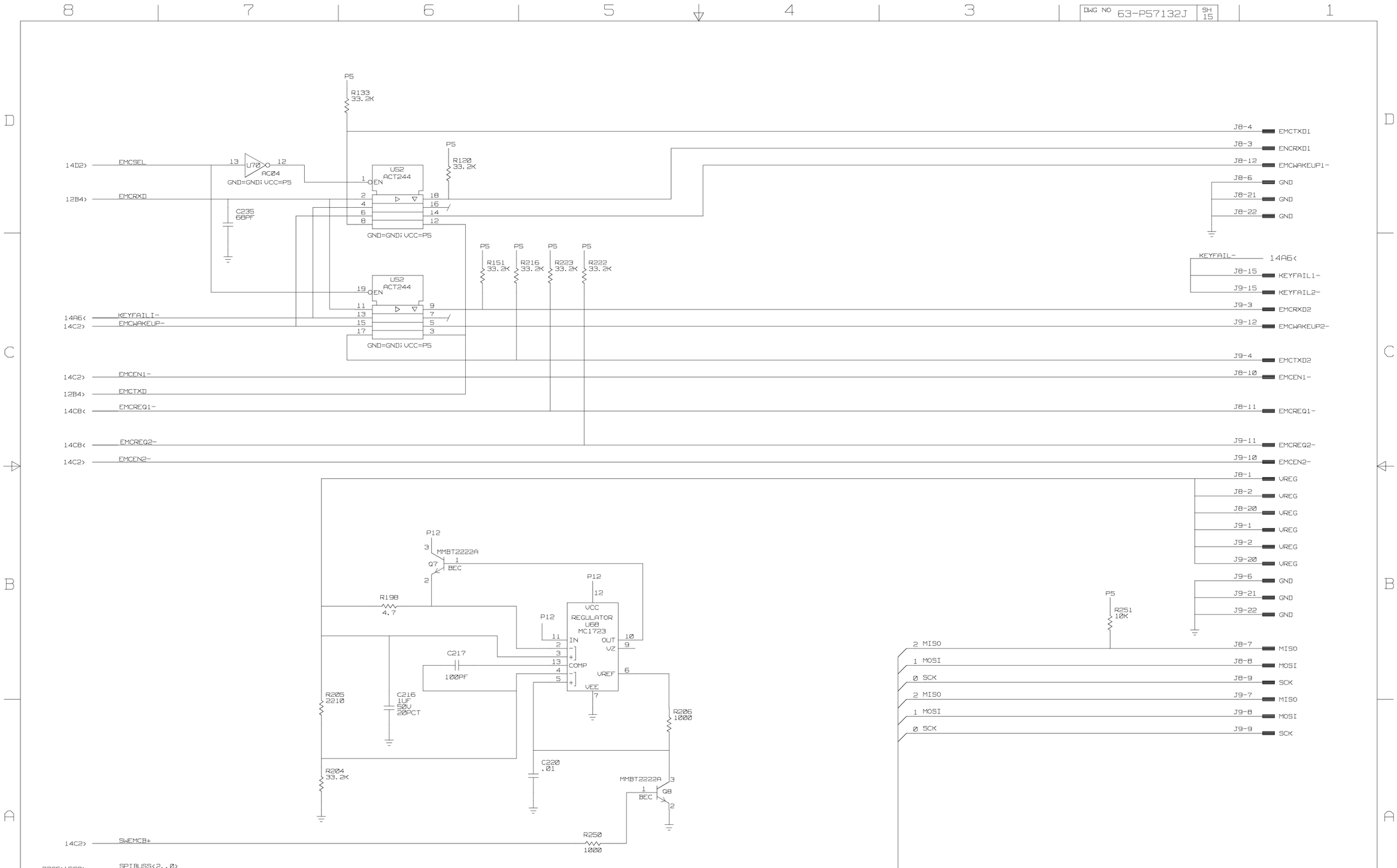

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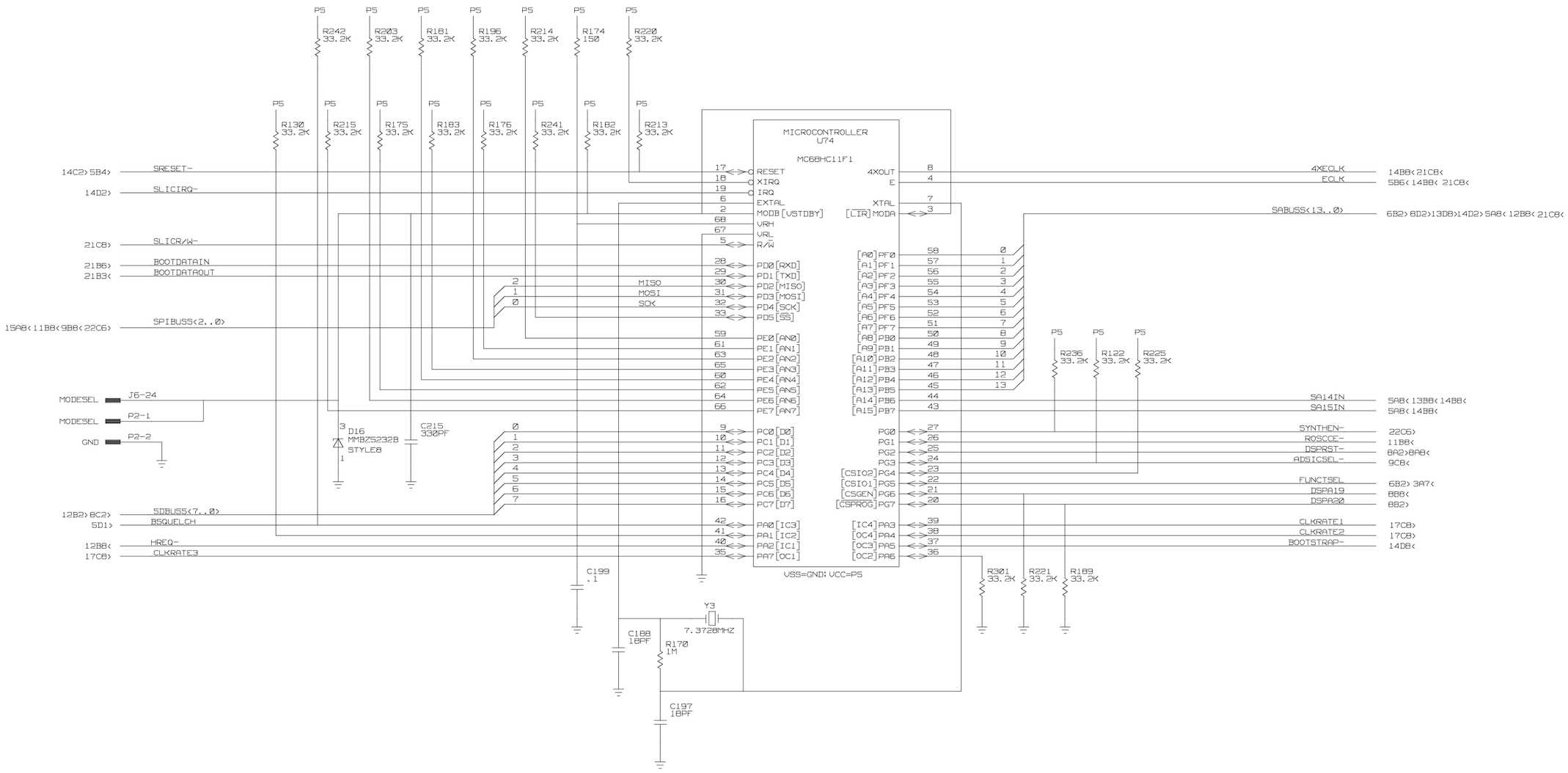

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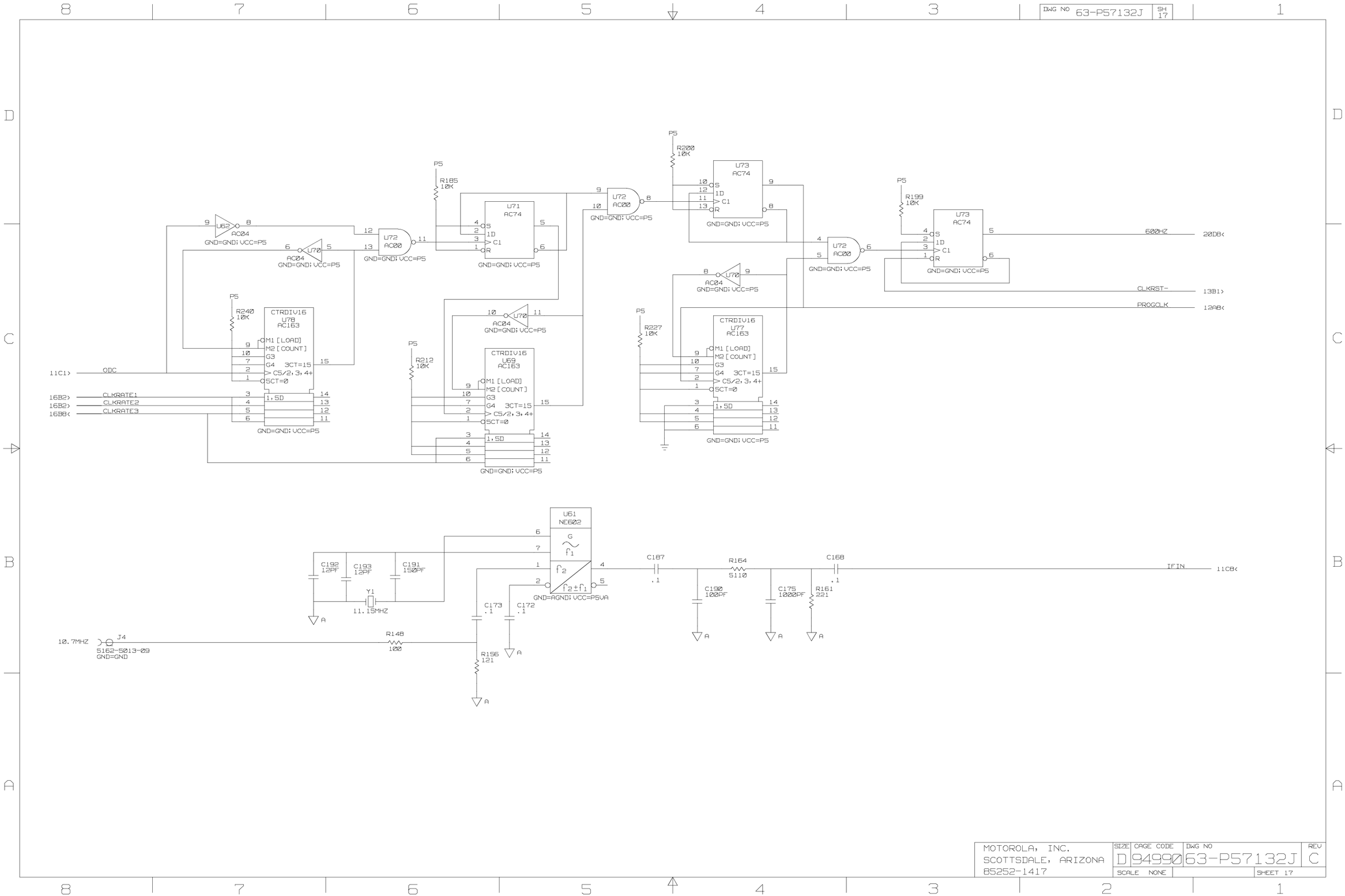

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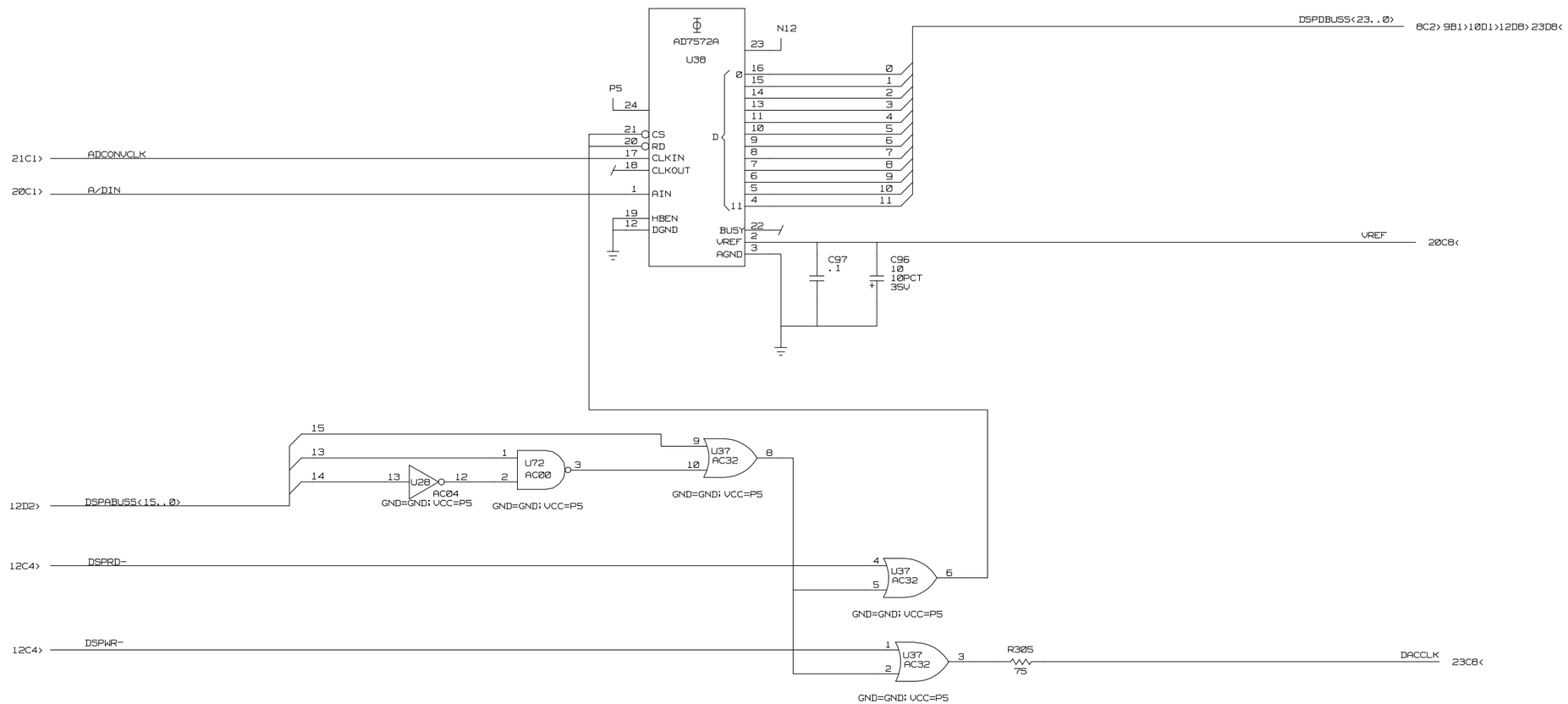

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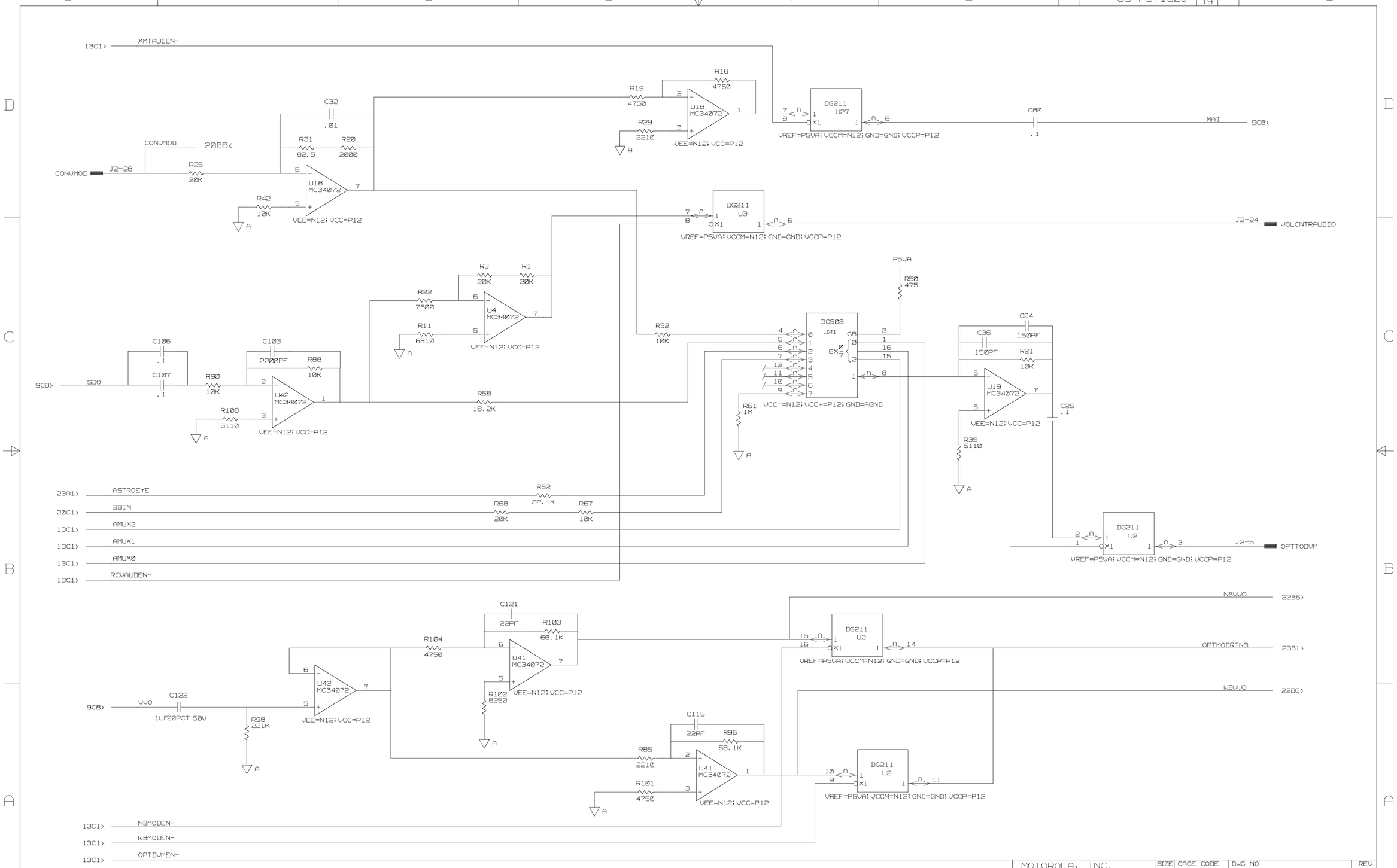

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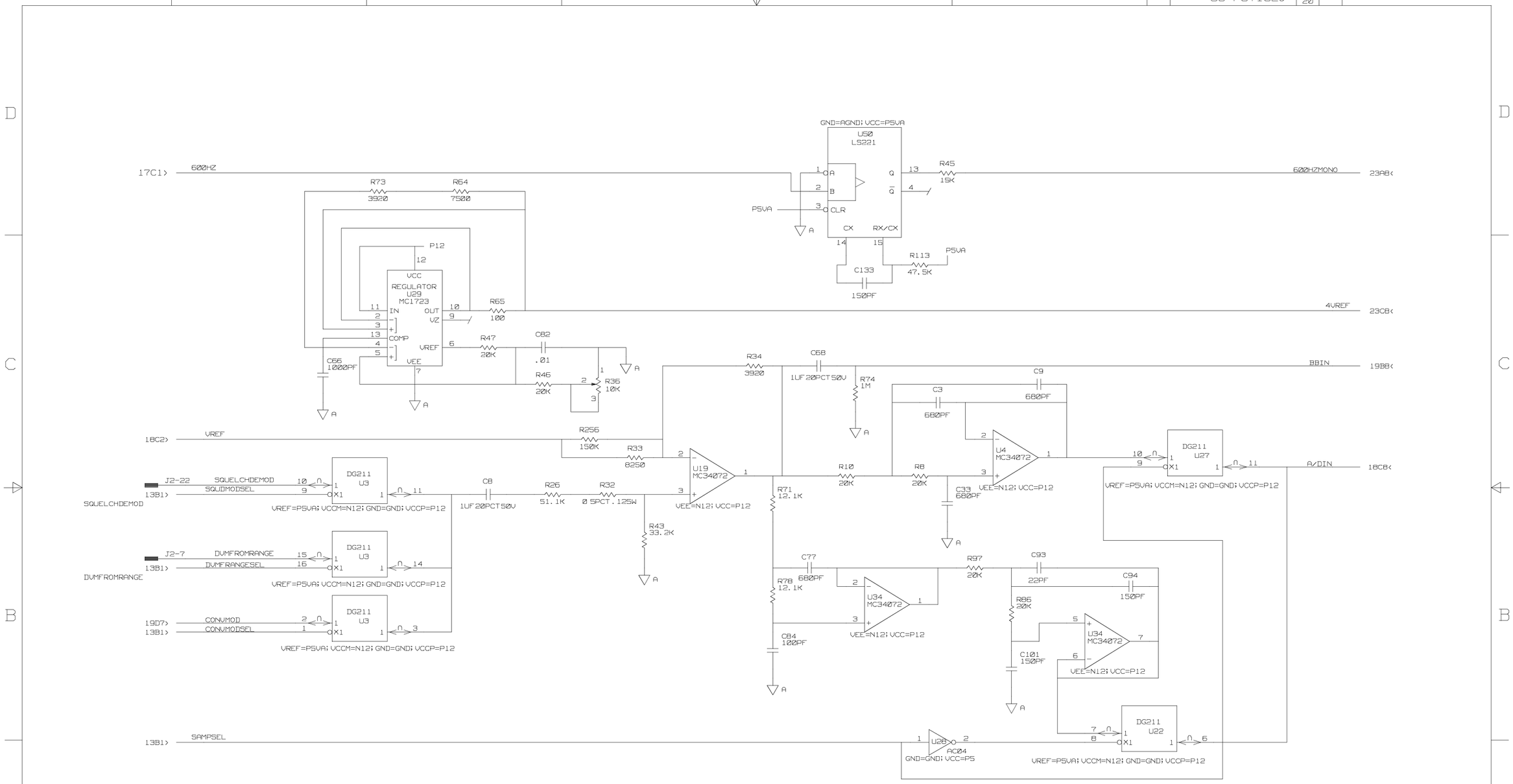

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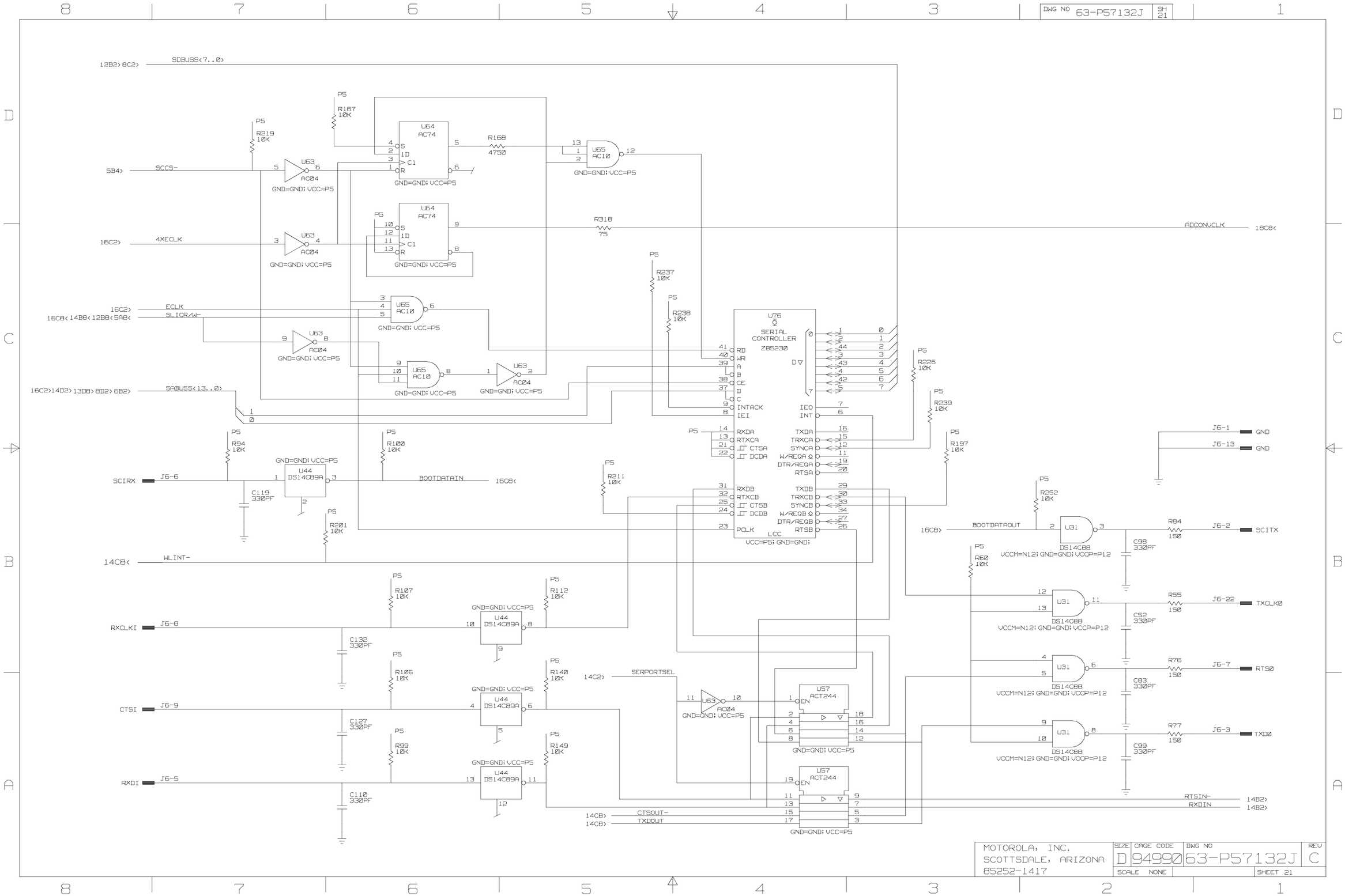

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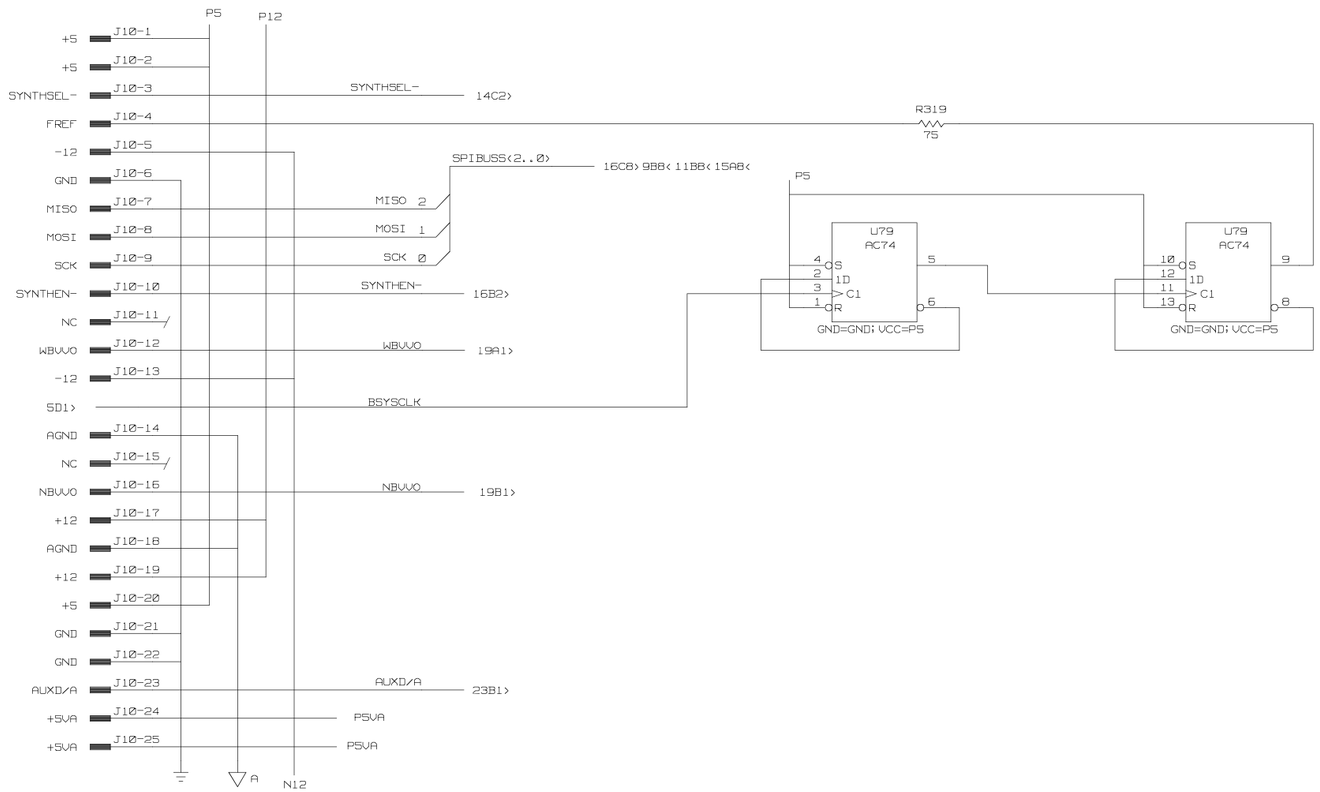

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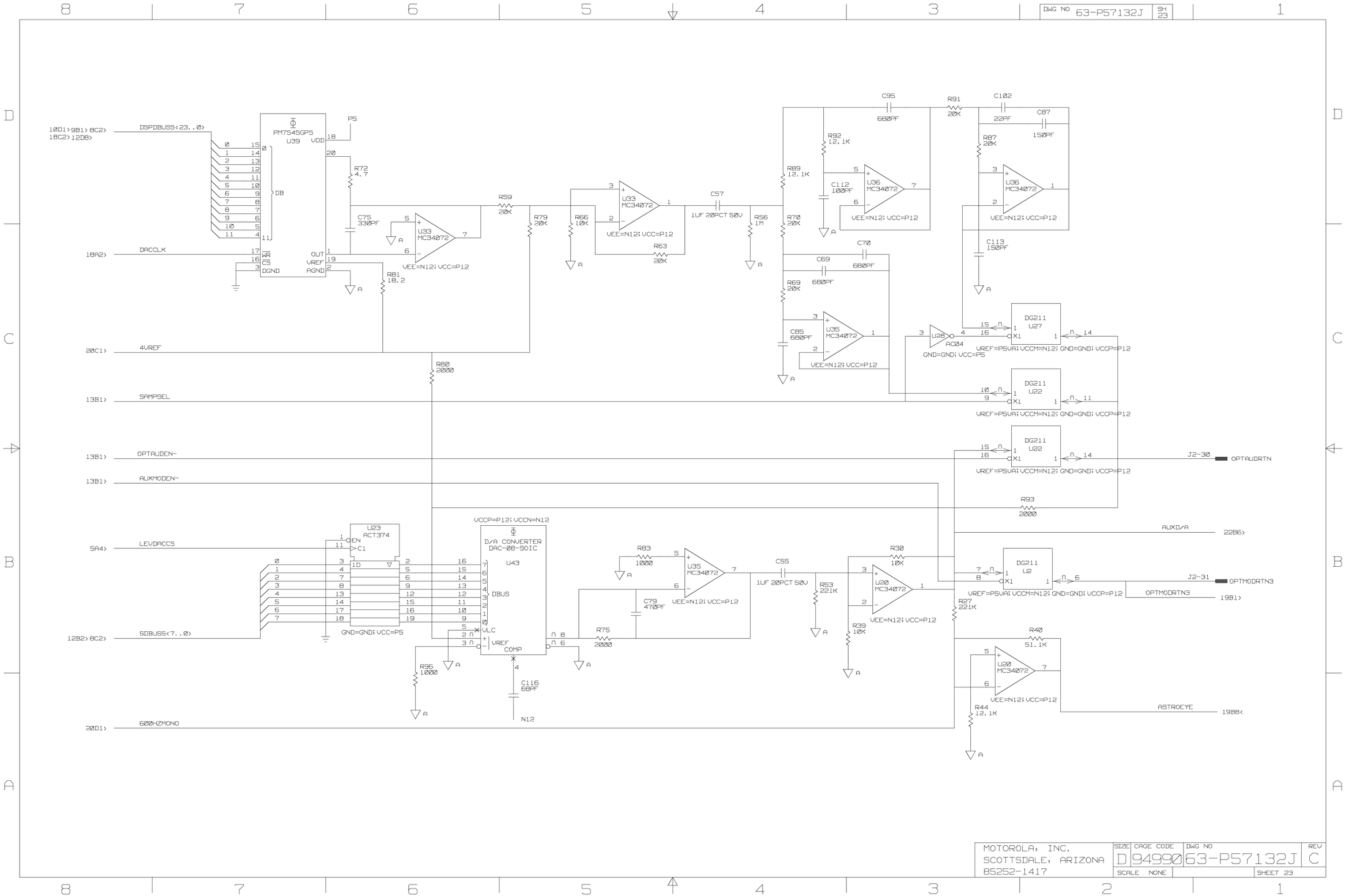

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	SCALE NONE		SHEET 23	

DWG NO.	SH
63-P30062C	1

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
	–	INITIAL RELEASE	94-03-30	J.NICKLES
	A	CO E36093-1 VAH 94-11-28	94-12-01	A.KOESTNER
	B	CO E36549-1 DEB 00-05-01	00-05-01	A.GATTO

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
   FOR COMPLETE DESIGNATION, PREFIX WITH 1A18A1.

2. FOR REFERENCE DRAWINGS REFER TO:
   01-P30060C ASSEMBLY
   62-P30071C REQ'S AND INTERFACE SPEC

3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS.
   ALL CAPACITORS ARE IN PF.
   ALL INDUCTORS ARE IN NH.
   ALL VOLTAGES ARE DC.

4. TERMINATIONS CODED WITH THE SAME LETTER
   COMBINATIONS ARE ELECTRICALLY CONNECTED.

5. DEVICE TYPE NUMBERS AND CONNECTIONS
   NOT SHOWN ON SYMBOL ARE LISTED IN TABLE 1.

6. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY.
   THE NUMBER VARIES WITH MANUFACTURER.
   SEE ASSEMBLY PARTS LIST FOR PROPER PART NUMBER.

7. C17, C25, R6, AND R11 NOT INSTALLED.

8. C32 AND C38 HAND SOLDER AS DESCRIBED
   ON DRAWING 01-P30061C.

REFERENCE DESIGNATIONS	
HIGHEST NUMBER USED	NOT USED
C58	C42
J2	
L22	L6, L9
R34	R29
U3	
TP3	
VR4	

ALL SHEETS CARRY THE SAME REVISION

01-P30060C	COCHISE
NEXT ASSY	USED ON
APPLICATION	

PROJ NO. 10744

INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS LISTED IN DOD-STD-100

DWN BY P.AMMON 94/02/10
DOC CHK BY
DSGN CHK BY J.NICKLES 94/02/10
CONTR NO. NA
ISSUED RN B35550-258(–)94/03/02
QA APVD K.NELSON 94/02/10
MATL APVD W.B.MCDONALD 94/02/10
MFG APVD S.CASH 94/02/10
ENGRG APVD J.NICKLES 94/02/10
CUST APVD

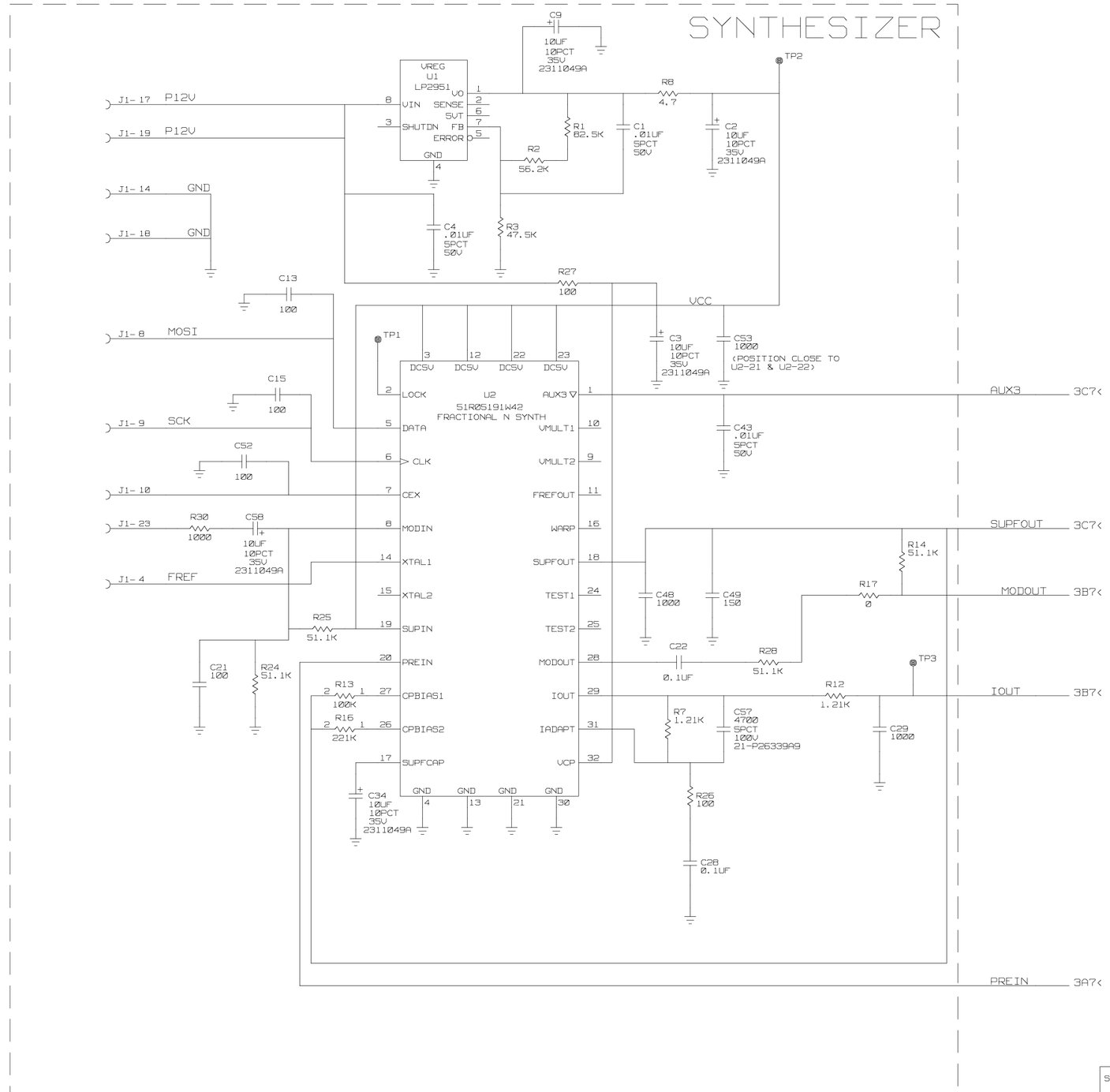
MOTOROLA INC. G.E.G.
COMMUNICATIONS DIVISION
8201 E.MC DOWELL RD.,P.O.BOX 1417
SCOTTSDALE, ARIZONA 85252-1417

SCHEMATIC DIAGRAM CONTROL CHANNEL SYNTHESIZER

SIZE	CAGE CODE	DWG NO.
D	94990	63-P30062C

SCALE NONE | SHEET 1 OF 3

SYNTHESIZER



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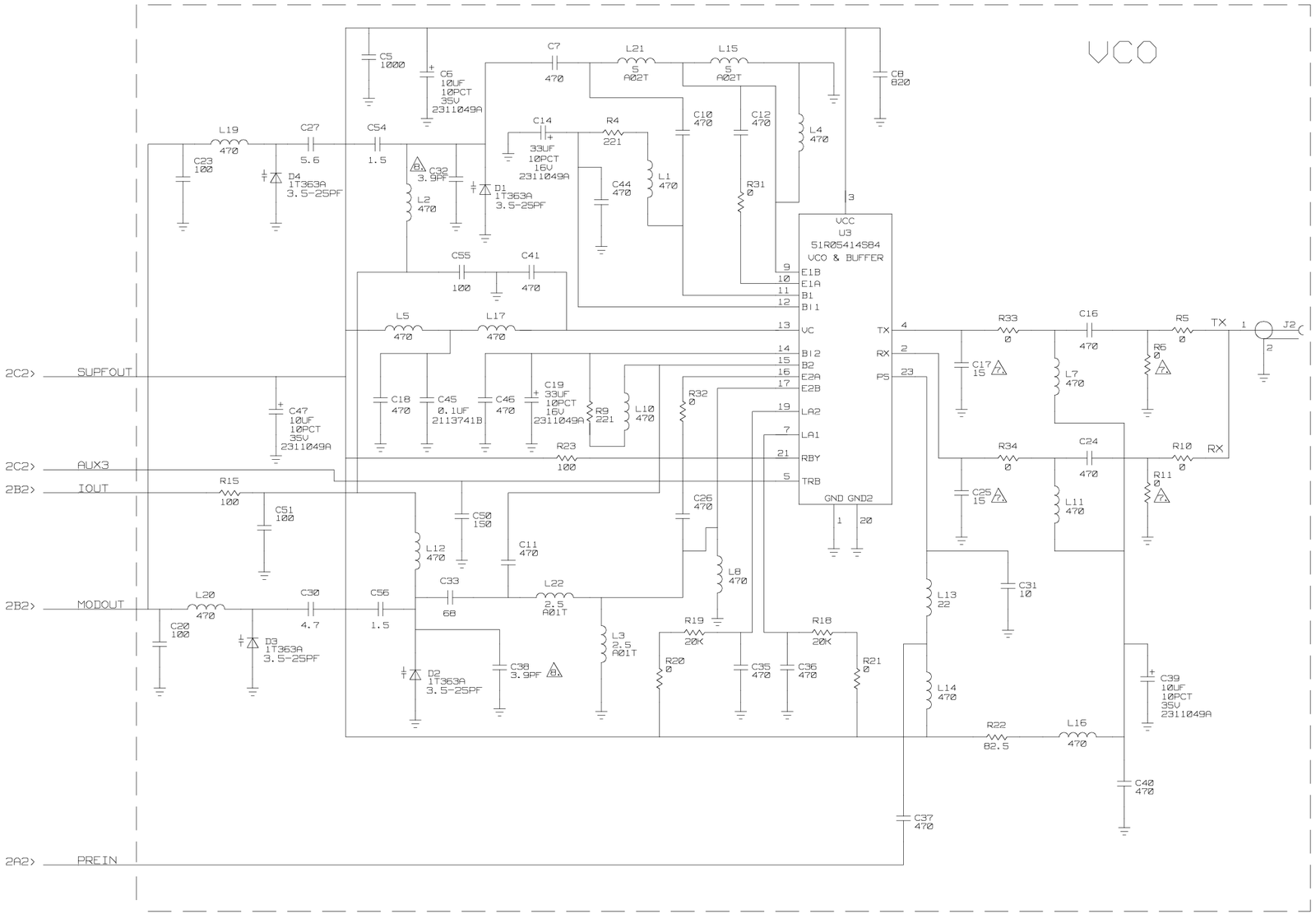

SIZE	CAGE CODE	DWG NO.	REV
D	94990	63-P30062C	B
SCALE NONE	WT	SHEET 3	

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D.1 GENERAL DESCRIPTION

This appendix is intended as an aid to technicians who must repair R2660 iDEN Option Slices. Operation of the R2660 is covered in the R2660 Operator Manual. The R2660 provides four modes of operation:

Standard: Standard mode provides features provided by the R2600.

iDEN BER Test: In iDEN BER Test mode, the analyzer provides the capability to generate and monitor test signals to perform bit error rate (BER) testing of iDEN base and mobile radio transmitters and receivers. The analyzer measures the equipment under test transmitted BER, frequency error, power level and signal quality estimate (SQE). The analyzer generates signals to be used in BER testing of iDEN receivers. In BER Test mode, DJSMR and DMCA signal formats are supported. Other diagnostic functions such as oscilloscope and voltmeters are available in iDEN BER Test mode.

iDEN Base: In iDEN Base mode, the analyzer provides the capability to monitor outbound signals transmitted by a live base site. The analyzer measures frequency error, transmitted power and SQE. Other diagnostic functions such as oscilloscope and voltmeters are available in iDEN Base mode.

iDEN Mobile: In iDEN Mobile mode, the analyzer simulates iDEN fixed end base sites to support testing of mobile radios operating in their functional mode. The analyzer simulates fixed end equipment to support initial registration, group dispatch and interconnect call testing. With the radio operating in its functional mode, the analyzer determines radio configuration data and measures transmit power and signal quality. Other diagnostic features such as oscilloscope and voltmeters are available in iDEN Mobile mode.

D.2 FUNCTIONAL DESCRIPTION

This portion of the maintenance manual provides a top level functional description of the iDEN Option Slice. Not all signals are shown, refer to the circuit board descriptions for detailed information. The module provides the hardware platform necessary to generate and monitor iDEN signals. The iDEN Option Slice consists of two circuit boards contained in one housing. The iDEN RF module contains RF modulator and demodulator circuits and custom digital ASIC circuits. The iDEN Digital module provides the signal processing platform to perform modulation, demodulation and vocoder algorithms. The iDEN Digital module also provides control to the iDEN RF module and performs all communication to the standard system 68000 microprocessor.

The following functional description assumes that the reader is familiar with complex modulation and demodulation techniques. A discussion of this subject is readily available in communication systems literature.

The following terms are used throughout this iDEN Option maintenance manual, appendix, and are defined below:

Standard System: Standard System refers to the R2660 hardware platform excluding the iDEN Option Slice.

iDEN Option Slice: iDEN Option Slice refers to the combination of the iDEN Digital Board, iDEN RF Board and option housing.

iDEN Digital Board: iDEN Digital Board refers to the digital signal processing platform which interfaces to the standard system and performs all iDEN digital signal processing functions. This board is located behind the iDEN RF Board in the option housing.

iDEN RF Board: The iDEN RF Board refers to the board containing the RF hardware including the complex modulator and digital receiver. The board is located on top of the iDEN Digital Board in the option housing.

I Modulation Samples: Samples of the I channel baseband modulation waveform at rate of 48KHz. Digital to analog conversion of the samples is performed to generate the analog I channel baseband modulation waveform for input to the complex modulator.

Q Modulation Samples: Samples of the Q channel baseband modulation waveform at a rate of 48KHz. Digital to analog conversion of the samples is performed to generate the analog Q channel baseband modulation waveform for input to the complex modulator.

Complex Modulator: A complex modulator is a device with four signal inputs. Two quadrature LO's and analog I and Q channel modulating signals. The complex modulator performs multiplier and summing functions to generate a XMIT IF signal based on the signal inputs. For the case of iDEN, the output signal is M16-QAM.

Digital Receiver. A Digital Receiver digitizes the receive IF signal to generate I and Q channel demodulation samples. The iDEN Digital module performs digitization at a rate of 60KHz. Digital signal processing algorithms operate on the I and Q samples to demodulate the received signal.

D.2.1 iDEN RF Board Functions

The following functions are provided by the iDEN RF board:

- Receive IF Down Conversion LO and Modulation Calibration Synthesizer.
- Generator
- Receiver

D.2-1.1 Receive IF Down Conversion LO and Modulation Calibration Synthesizer

This block represents circuits generating LOs used for down conversion of the receive IF and for calibration of the iDEN Digital Module modulation circuits. The LOs are phaselocked to the system 10MHz reference.

D.2.1.2 Generator

The Generator block contains all functions necessary to generate an M16-QAM transmit IF signal using the standard system XMIT IF and I and Q modulation data from the iDEN Digital Board.

90 Degree Power Splitter: The 90 degree power splitter divides the standard system XMIT IF into two LOs separated in phase by 90 degrees. The quadrature LOs are input to the complex modulator.

TRANLIN: I and Q modulation samples are input to the TRANLIN from the iDEN Digital board. The TRANLIN performs digital to analog conversion and smoothing filtering of the I and Q samples to generate analog I and Q baseband modulation waveforms. The data interface is a low level differential digital serial data interface.

Amplitude and Offset Adjustment: This block represents circuits performing amplitude scaling and DC offset, of the analog I and Q modulation waveforms to optimize the carrier suppression and I/Q balance of the generated transmit IF. Adjustment programming values are determined during system calibration.

Complex Modulator: The Complex Modulator receives the quadrature LOs and analog I and Q modulation waveforms; as inputs. It generates an M16-QAM transmit IF output.

Calibration Mixer: During calibration of the complex modulator, the standard system spectrum analyzer is used to make quality measurements on the generated signal. The XMIT IF must be 310.7MHz for the analyzer to make the measurement. Therefore when calibrating ±45MHz duplex offsets, the XMIT IF must be converted to 310.7MHz. The calibration mixer performs this function using the LO generated on the iDEN RF board.

XMIT IF Switch: The XMIT IF switch selects one of three signals for input to the standard system. The STD XMIT IF is selected if the analyzer is operating in standard mode. The iDEN RF Board buffers the IF and routes it back to the standard system. The CAL IF is selected if the unit is performing self test and calibration. The iDEN XMIT IF is selected if the unit is operating in one of the three iDEN modes.

D.2.1.3 Receiver

The Receiver block contains all functions necessary to digitize the receive IF and pass I and Q channel demodulation samples to the iDEN Digital Board.

Power Splitter: The power splitter divides the standard system 10.7MHz RX IF (without automatic gain control) into two signals. One signal is used by the iDEN Digital module. The other is a buffered output that can be used for future expansion.

Program Attenuator: The programmable attenuator sets the level of the RX IF to prevent overdriving the Digital Receiver IC. The attenuator programming is based on standard system receiver attenuator and spectrum analyzer sensitivity selections.

450KHz Down Converter: The 450KHz down conversion mixer down converts the 10.7MHz receive IF to 450KHz for input to the Digital Receiver IC.

RX LPF: The RX LPF filters the down converted receive IF signal prior to input to the Digital Receiver IC. The cutoff frequency of the filter is approximately 1MHz.

Digital Receiver IC: The Digital Receiver IC digitizes the 450KHz receive IF at a rate of 60KHz and outputs I and Q demodulation samples to the iDEN Digital board for processing. The interface is a low level, differential digital serial data interface.

D.2.2 iDEN Digital Board Functions

The following functions are provided by the iDEN Digital board.

- Receive Data Multiplexer
- Transmit Data Multiplexer
- Receive DSP
- Transmit DSP
- Transmit/Receive DSP
- 68302 Controller Processor
- Timing Signal Generator

D.2.2.1 Receive Data Multiplexer

The Receive Data Multiplexer (RX Data Mux) multiplexes I and Q demodulation samples received from the iDEN RF board to the RX DSP or the TXRX DSP dependent on the operational mode of the analyzer.

D.2.2-2 Transmit Data Multiplexer

The Transmit Data Multiplexer (TX Data Mux) multiplexes I and Q modulation samples from either the TX DSP or the TXRX DSP to the iDEN RF board dependent on the operational mode of the analyzer.

D.2.2.3 Receive DSP

The Receive DSP (RX DSP) block represents the Motorola DSP56002 signal processor, associated memory and control circuits and firmware executed by the DSP. The RX DSP executes different algorithms and performs different functions for each analyzer mode of operation.

iDEN BER Test: The RX DSP performs test signal demodulation based on I and Q channel demodulation samples received from the iDEN RF board. Additionally, the RX DSP measures the frequency error, bit error rate (BER) and signal quality estimate (SQE) on the received signal. Measurement reports are passed to the 68302 on a per slot basis via the host interface.

iDEN Mobile: The RX DSP performs demodulation of the mobile transmitted inbound signal base on I channel and Q channel demodulation samples received from the iDEN RF board. The RX DSP transfers I and Q signal state decisions to the TX DSP The TX DSP performs the remaining decode and error correction functions to recover the mobile transmitted data.
iDEN Base: The RX DSP is not used when the analyzer is operating in iDEN Base mode.

Standard: The RX DSP is not used when the analyzer operates in standard mode.

D.2.2.4 Transmit DSP

The Transmit DSP (TX DSP) block represents the Motorola DSP56002 signal processor, associated memory and control circuits and firmware executed by the DSP. The TX DSP executes different algorithms and performs different functions for each analyzer mode of operation.

iDEN BER Test: The TX DSP generates test signal I and Q channel modulation samples for output to the iDEN RF board.

iDEN Mobile: The TX DSP generates outbound signal I and Q channel modulation samples for output to the iDEN RF board. The message data to be transmitted in the outbound signal is input to the TX DSP from the 68302 host processor via the host interface.

The TX DSP also performs a portion of the receiver functions. It performs decoding and error correction based on I and Q signal state decision data. The TX DSP receives signal state decision data from the RX DSP. The TX DSP passes the recovered message data to the 68302 via the host interface.

iDEN Base: The TX DSP is not used when the analyzer operates in iDEN Base mode.

Standard: The TX DSP is not used when the analyzer operates in standard mode.

D.2.2.5 Transmit/Receive DSP

The Transmit/Receive DSP (TXRX DSP) block represents the Motorola DSP56166 signal processor, associated memory and control circuits and firmware executed by the DSP. Note that the DSP contains on-board A/D and D/A to digitize transmit audio and synthesize receive audio. The TXRX DSP executes different algorithms and performs different functions for each analyzer mode of operation.

iDEN BER Test: The TXRX DSP is not used when the analyzer operates in iDEN BER Test mode.

iDEN Mobile: In iDEN Mobile mode, the TXRXDSP performs vocoder functions. It synthesizes received audio from demodulated VSELP data for output to the system speaker or for display to the Internal Audio Generate Signal Oscilloscope. The DSP generates VSELP data for output over the outbound channel based on audio source inputs VSELP data is passed between the 68302 microprocessor and the TXRX DSP via the host interface.
iDEN Base: The TXRX DSP performs live base site outbound signal demodulation based on I and Q channel demodulation samples received from the iDEN RF board. The RX DSP measures the frequency error and signal quality estimate (SQE) on the received signal. The results are passed to the 68302 microprocessor on a per slot basis via the host interface.

Standard: The TXRX DSP is not used when the analyzer operates in standard mode.

D.2.2.6 68302 Controller Processor

The 68302 Controller Processor block represents the Motorola 68302 microprocessor, associated memory and control circuits and firmware executed by the processor. The 68302 performs all communication of configuration data and measurements to the standard system 68000 microprocessor. It controls all activities of the iDEN Digital Board including signal routing, download of software to all DSPs, control of the DSPs and configuration of the iDEN RF Board. It provides the interface to pass VSELP data from the TXRX DSP to the inbound and outbound channels received and generated by the RX and TX DSPs.

D.2.2.7 Timing Signal Generator

The Timing Signal Generator generates 7.5ms and 15ms tick marks to the RX DSP and the TX DSP to synchronize the slot timing of the inbound and outbound channels. It also generates several other clocks required by circuits on both the iDEN RF and the iDEN Digital Boards.

D.2.3 Operational Examples

The following section provides a description of the events and signal and data flow for each mode of operation.

D.2.3.1 iDEN BER Test Mode

1) The standard system 68000 communicates with the 68302 to command the iDEN, Digital module for iDEN BER Test configuration.

2) The 68302 configures the RF and Digital Boards for iDEN BER Test operation and downloads the appropriate algorithms to the DSPs.

Generate Signal

3. The TX DSP executes modulation algorithms and generates I and Q modulation samples at a rate of 48KHz and passes the signal samples to the iDEN RF Board.

4. The TRANLIN performs digital to analog conversion of the I and Q modulation samples generating analog baseband I and Q modulation signals.

5. The modulation signals are input to the complex modulation along with the quadrature LOs to generate an M16-QAM BER Test signal.

6) The M16-QAM iDEN XMIT IF is routed to the standard system through the XMIT IF Switch.

7) The standard system performs frequency conversion and level setting functions and outputs the signal through the front panel.

Monitor

8) The STD SYS RCV IF 10.7MHz signal is routed to the iDEN, Digital module through the power splitter.

9) The receive IF is down converted to 450KHz IF by mixing with the 11.15MHz LO.

10) The 450KHz IF is low pass filtered and input to the Digital Receiver IC.

11) The Digital Receiver digitizes the 450KHz IF at a rate of 60KHz and passes the I and Q demodulation samples to the RX DSP.

12) The RX DSP executes demodulation algorithms and detects received data.

13) During the demodulation process, the RX DSP measures frequency error, SQE and BER of the recovered data and passes the results to the 68302.

14) The 68302 averages the measurement reports and passes the results to the standard system for display to the operator.

D.2.3.2 iDEN Mobile mode

1) The standard system 68000 communicates with the 68302 to command the iDEN Digital module for iDEN Mobile configuration.

2) The 68302 configures the iDEN RF and Digital Boards for iDEN Mobile operation and downloads the appropriate algorithms to the DSPs.

iDEN RF Board operation is the same as for iDEN BER Test mode. Therefore this description will highlight the functions of the iDEN Digital Board.

3) The 68302 maintains the call scenario state and generates all data packets to be transmitted on the outbound channel (to radio under test). It decodes all data packets received on the inbound channel (from radio under test).

Outbound Channel Generation

4) 68302 passes data packet for transmission to the TX DSP via the host interface.

5) TX DSP generates outbound signal I and Q modulation samples.

6) Modulation samples are passed to the RF cards for XMIT IF generation and routing to the standard system.

7) If a traffic channel is active, vocoder operations are performed. The TXRX DSP generates VSELP data packets based on audio signal inputs from the standard system and passes the VSELP data to the 68302 via the host interface. The 68302 inputs the VSELP data to the data packets sent to the TX DSP for transmission.

Inbound Channel Monitor

8) I and Q demodulation samples are passed to the RX DSP from the iDEN RF Board.

9) The RX DSP executes demodulation algorithms to generate I and Q state values.

10) I and Q state values are passed to the TX DSP.

11) The TX DSP performs receive decode functions and passes data packet to the 68302 via the host interface.

12) If a traffic channel is active, the received data packets contain VSELP data.

13) Received VSELP data is passed from the 68302 to the TXRX DSP.

14) The TXRX DSP performs audio synthesis and digital to analog conversion functions to generate received audio.

15) Received audio is input to the standard system for monitor on the speaker or display on the internal audio scope.

D.2.3.3 iDEN Base Mode

1) The standard system 68000 communicates with the 68302 to command the iDEN Digital module for iDEN Base configuration.

2) The 68302 configures the RF and Digital boards for iDEN Base operation and downloads the appropriate algorithms to the TXRX DSP.

3) The STD SYS RCV IF 10.7MHz signal is routed to the iDEN Digital Board through the power splitter.

4) The receive IF is down converted to 450KHz IF by mixing with the 11.15MHz LO.

5) The 450KHz IF is low pass filtered and input to the Digital Receiver IC.

6) The Digital Receiver digitizes the 450KHz IF at a rate of 60KHz and passes the I and Q demodulation samples to the RX DSP.

7) The TXRX DSP executes demodulation algorithms measures the frequency errror and SQE of the received signal. The measurement results are passed to the 68302 via the host interface.

8) The 68302 averages the measurement reports and passes them to the standards system for display to the operator.

D.2.4 Physical Block Diagram

The physical block diagram shown in Figure D.2 indicates the signal connection and interfaces between the iDEN RF and Digital boards and the interface of the iDEN Digital Module to the standard system.

D.3 GENERAL DESCRIPTION

The iDEN RF Board (1A19Al) is installed in the iDEN Option Slice above the iDEN Digital Board.

The iDEN RF Board generates an M16-QAM XMIT IF for up conversion by the standard system. The iDEN RF Board also digitizes the standard system 10.7MHz RX IF providing an output of I and Q samples to the iDEN Digital Board.

D.4 SIGNALS SUMMARY

D.4A Signal Descriptions

D.4A.1 J1 GEN IF IN

This input from the Generator Module located in the standard system shall be unmodulated in iDEN mode. The signal can be either modulated or unmodulated in STANDARD mode.

D.4A.2 J2 GEN IF OUT

This output from the Generator Module located in the standard system is a iDEN modulated (M16-QAM) signal in iDEN mode. This signal has the same modulation as GEN IF IN in STANDARD mode.

D.4A.3 J3 10.7MHZ_IN

This input from the Receiver Module located in the standard system is a iDEN modulated (M16-QAM) signal without AGC in iDEN mode.

D.4A.4 J4 10.7MHz OUT

This output has the same signal characteristics as 10.7MHz IN and allows daisy-chaining the 10.7MHz RX IF to additional option slices.

D.4A.5 J5 10MHz REF

This input from the Frequency Standard Module located in the standard system is used to synthesize the 223MHz PLL.

D.4A.6 J6 iDEN RF Module and iDEN Digital Module Interface

ATTEN MUX CNTRL input controls whether the state of the receiver attenuator is controlled by RX ATTEN SW<0> and RX ATTEN SW<1> or Rl AGC, R2 AGC, R3 AGC, and R4 AGC.

CLKI and *CLKIB* inputs are the differential 4.8MHz clock inputs by which I and Q data is clocked into the Tranlin IC.

DOUT and *DOUTX* contain the output of the Abacus decimation filters (in I & Q format), AGC value, imbedded sync pattern, and fill bits.
IQ EXT SEL input controls whether the I and Q outputs of the Tranlin IC or an auxiliary source are selected.

I EXT and *Q EXT* inputs are auxiliary analog I and Q signals received from the iDEN Digital Module. These inputs are currently reserved for test purposes and future expansion.

MODCAL input controls whether the vector modulator is being calibrated for the duplex generator mode or generator mode.

ODC output is the 4.8MHz signal used to clock the SBI. It is also used to clock DOUT and DOUTX at an I/Q sampling rate of 60 Ksamples/sec.

OP MODE<0> input controls whether the standard system XMIT IF path or iDEN XMIT IF path is selected.

+12V,-5V, -12V, and *+5V* supply power to the module.

QDAC CS N input allows selection of the quad D/A converter for programming.

RF STDBY input is a control signal placing the module in a standby (low power) mode.

RX ATTEN SW<0> and *RX ATTEN SW<1>* inputs control the state of the step attenuator in the 10.7 MHz RX IF path.

R1AGC, R2AGC, R3AGC, R4AGC inputs control the state of the step attenuator in the 10.7 MHz RX IF path.

SBI input is used to program the Abacus IC with a 32-bit word.

SPI MOSI, SPI MISO, and *SPI SCK* are serial peripheral interface (SPI) signals used to program the Tranlin IC, 223 MHz PLL, and quad D/A converter.

SSI and *SSIB* inputs supply data to the Tranlin IC consisting of word sync bits, frame sync bits, I and Q words, and fill bits.

TRANLIN CS N input allows selection of the Tranlin IC for programming.

TRANLIN RESET N input is a master reset signal for the Tranlin IC.

223MHz PLL CS N input allows selection of the 223MHz PLL for programming.

2.1MHz input is a reference required by the Abacus IC and is used to synthesize the output data clock, ODC.

D.4A.7 J7 and J8 IOUT and QOUT

IOUT and QOUT are buffered analog baseband I and Q outputs made available whenever the iDEN generator or duplex generator is selected.

D.4B Connector Descriptions

SMB Connectors

D.4B.1 J1 GEN IF IN

Input Freq.

(iDEN):	310.7MHz ±0, ±45,±48MHz
(STANDARD):	255.5MHz to 365.7MHz
Input Level:	-17.5dBm ± 2.5dB
Input Impedance:	50 ohms nominal
VSWR:	2:1 maximum
Phase Noise (iDEN):	≤2.0 rms (300Hz - 3 KHz BW)

D.4B.2 J2 GEN IF OUT

Output Freq.

(iDEN):	310.7MHz ±0, ±45, ±48MHz
(STANDARD):	255.5MHz to 365.7MHz
Output Level:	-17.5dBm ± 2.5 dB
Output Impedance:	50 ohms nominal
VSWR:	2:1 maximum

D.4B.3 J3 10.7MHZ IN

Input Freq.:	10.7MHz
Input Level:	-90dBm to -15dBm
Input Impedance:	50 ohms nominal
VSWR:	2:1 maximum

D.4B.4 J4 10.7MHZ_OUT

Output Freq.:	10.7MHz
*Gain:	0 ± 2 dB
Output Impedance:	50 ohms nominal
VSWR:	2:1 maximum

*Gain from 10.7MHz_IN to 10.7MHz_OUT

D.4B.5 J5 10MHz REF

Input Freq.:	10.0MHz
Input Level:	CMOS compatible
Input Duty Cycle:	40% to 60%
Input Impedance:	≤250 ohms

D.4B.6 J6 (50 Pin Connector to iDEN Digital Board)

pin	
1,2	+12V
3	-5V
4	not used
5	-12V
6	+5V
7	GND
8	not used
9,10	GND
11	not used
12	SPARE1
13	ODC
14	GND
15	DOUT
16	DOUTX
17	GND
18	not used
19	RX ATTEN SW<0>
20	TRANLIN RESET N
21	R1 AGC
22	RX ATTEN SW<l>
23	R3 AGC
24	R2 AGC
25	OP MODE<0>
26	R4 AGC
27	ATTEN MUX CNTRL
28	SBI
29	GND
30	2.1MHZ
31	IQ EXT SEL
32	GND
33	Q EXT
34	I EXT
35	MODCAL
36	GND
37	SPI SCK
38	RF STDBY
39	SPI MOSI
40	SPI MISO
41	QADC CS N
42	SPARE2
43	223MHZ PLL CS N
44	GND
45	SSI
46	SSIB
47	TRANLIN CS N
48	GND
49	CLKI
50	CLKIB

3 Pin Headers to Option Housing BNC Connectors

D.4B.7 J7 IOUT

Output Level:	0.6-1.0Vpp*
Coupling:	DC
DC Offset:	≤ 10mV*
Output Impedance:	50 ohms ± 2%
Amplitude Balance:	3%*
Phase Balance:	1*

D.4B.8 J8 QOUT

Output Level:	0.6-1.0Vpp*
Coupling:	DC
DC Offset:	≤ 10mV*
Output Impedance.	50 ohms ± 2%
Amplitude Balance:	3%*
Phase Balance:	1*

*when using internal (Tranlin) I and Q source

iDEN RF BOARD

D.5 BLOCK DIAGRAM DESCRIPTION

The iDEN RF Board generates a iDEN XMIT IF for input to the standard system based on I and Q modulation samples, from the iDEN Digital Board using the standard systems XMIT IF as an LO. Analog I and Q modulating signals are generated from the I and Q samples using the Tranlin IC. A complex modulator generates M16-QAM based on these signals and the quadrature LO. The complex modulator requires digital tuning to achieve the required performance. A XMIT IF switch provides for selection of the iDEN XMIT IF or routing of the standard system XMIT IF input directly back to the standard system without modification.

The iDEN RF Board receives the standard system 10.7MHz RX IF and down converts it to 450KHz for input to the Abacus IC using an 11.15MHz LO. The Abacus IC digitizes the 450KHz IF and outputs I and Q samples and AGC information in serial data format to the iDEN Digital Board.

D.6 DETAILED DESCRIPTION – RF BOARD

The three main sections are the synthesizer, generator, and receiver sections.

D.6.1 Receiver IF Down Conversion LO/Modulator Calibration Synthesizer

The synthesizer section consists of a phase-locked loop capable of tuning to 223MHz and 225MHz, a divide-by-5 prescaler used to generate a 45MHz LO during modulator calibration, and a divide-by-20 prescaler used to generate a 11.15MHz LO for down conversion of the 10.7MHz RX IF to 450KHz. Except during calibration, the PLL is locked at 223MHz. The PLL has three sections; the RF, digital, and loop filter sections.

D.6.1.1 RF Section

The 223MHz signal is created by a discrete VCO followed by a buffer amplifier. The amplifier's output is split using a two-way resistive power divider. One signal goes to a divide-by-32/33 prescaler (U15) contained in the feedback loop of the PLL. The prescaler's output then drives the N/A counter that is part of the loop's digital section. The other signal is again split using another resistive divider. One of the signals goes to a UHF divide-by-20 prescaler (U35) whose output is 11.15MHz when the PLL is locked at 223MHz. The other signal goes to a divide-by-5 prescaler (U41) whose output is 45MHz when the PLL is locked at 225MHz during iDEN modulator calibration. Power is supplied to the divide-by-5 prescaler only during modulator calibration of duplex IF frequencies. The 45 MHz signal is amplified using a discrete amplifier and supplied to the LO port of a mixer (U31). During iDEN modulator calibration, this LO is used to remove duplex offset from the XMIT IF.

D.6.1.2 Digital Section

The digital section contains the N/A counter, phase/freq detector, and the reference divider functions, which are realized using the divide-by-32/33 dual modulus prescaler (U15) and the PLL IC (U43).

To program the PLL IC, two sets of data must be serially clocked in. One set programs the reference divider (R) and the other set programs the N and A divider. The last data bit entered determines which counter storage latch is activated: a logic 1 selects the R divider and a logic 0 selects the N and A divider. The R divider is always set to 50. To lock the PLL at 223MHz, the N divider is set to 34 and the A divider is set to 27. To lock the PLL at 225MHz, the N divider is set to 35 and the A divider is set to 5.

The N/A counter divide ratios are set at 1115 (223MHz/1115 = 200KHz) and 1125 (225 MHz/1125 = 200KHz) for 223MHz and 225MHz respectively. The reference divide ratio is set at 50 to provide the reference frequency going into the phase/frequency detector (10MHz/50 = 200KHz). The two outputs of the detector (r and v) drive the loop filter. Each of these is normally high (5V) and pulses low (0V) to steer the loop filter.

D.6.1.3 Loop Filter Section

The loop filter section consists of an active loop filter followed by a notch filter. The loop filter contains a differential topology for the r and v inputs. The VCO control voltage is limited to between -10V and +8.5V by the op-amp's negative supply voltage and a diode damp circuit. The notch filter is designed to attenuate the 200KHz reference frequency.

D.6.2 Generator Section

The generator section consists of the Tranlin IC, modulator, and XMIT IF routing sections.

D.6.2.1 Tranlin IC

The Tranlin IC (U44) is a custom chip which generates analog I and Q modulating waveforms based on I and Q samples and configuration data received from the iDEN Digital Assembly. The Tranlin IC is programmed using a serial peripheral interface (SPI). A 240MHz LO between 0 and -3 dBm is supplied to the Tranlin IC to correctly bias the part to minimize offset drift. This LO is generated using a discrete oscillator.

In order to write to the Tranlin IC registers, TRANLIN CS N is pulled low. An address and subsequent bytes of data to be written sequentially into registers beginning at that address are then sent out. For example, a hexadecimal sequence of 05, 3F, D8, 2C sent will result in 3F, D8, and 2C being written into registers 5,6, and 7 respectively.

After sending the last byte, TRANLIN CS N is pulled high. This causes a checksum to be calculated. The checksum is defined as the 16 bit sum of all of the Tranlin IC registers with the MSB being "1" for a valid sum and "0" otherwise.

The Tranlin IC contains 26 programmable registers, which are addressed from $00 to $19. It takes one cycle of the system clock, CLKI, to read and add the contents of one register. Allowing five extra cycles to sync up to a synchronous signal, a total time of thirty-one system clock cycles are required to obtain a valid checksum. So, the minimum time that the host must wait until it can select the Tranlin IC again is thirty-one times one cycle of the system clock or about 6.46 microseconds.

Data is simultaneously shifted in and out of the Tranlin IC. The first and second bytes shifted out are the most and least significant bytes, respectively of the checksum from the previous write session. The next four bytes are test bytes from the Tranlin IC's internal test registers. After the test bytes, the checksum is sent out again and then the test bytes again and so on until the TRANLIN CS N is pulled high.

SSI/SSIB and CLKI/CLKIB are low level differential (current and voltage) input pairs. CLKI is the 4.8MHz system clock by which I and Q data is clocked in through the SSI input. Data on SSI changes on the rising edge of CLKI and is latched on the falling edge. Each data sample sent on SSI consists of a pair of I and Q words. Each word (I or Q) is preceded with a word sync of five 1's and a frame sync bit of 1 for the I word and 0 for the Q word. A word is 16 bits long with a fill bit of 0 following every fourth data bit. The Tranlin IC requires that each data sample takes up a frame of 100 bits. Since it takes only 26 bits to represent the I or Q portion of the data sample, one or more fill bits (of 0) can be placed between I and Q portions such that each I word sync is exactly 100 bits from the next I word sync. The Tranlin IC expects to receive SSI data in the order of MSB first and LSB last. In addition the I word must precede the Q word in each data sample sent. At a bit rate of 4.8MHz, data is received at a rate of 48K samples/second.

D.6.2-2 Modulator

The complex modulator generates M16-QAM based on the analog I and Q modulation waveforms generated by the Tranlin IC and an LO supplied by the Generator Module.

The differential I and Q waveforms produced by the Tranlin IC and the auxiliary I and Q waveforms received from the iDEN Digital Board are passed through unity gain buffers prior to being input to analog multiplexers (U20 and U22). The +5V CMOS signal IQ EXT SEL controls the state of the multiplexers and is toggled low to select the waveforms produced by the Tranlin IC. The differential outputs of the analog multiplexers are passed through unity gain buffers (U18 and U21) and routed to two different locations.

The first location to which the differential I and Q signals are routed are discrete output driver circuits, which convert the differential signals to single-ended signals, IOUT and QOUT, for output to BNC connectors located on the iDEN Option housing. The outputs are designed to drive 50 ohm loads at a level of 0.6 to 1.0Vpp when using the Tranlin IC as the I and Q source.

The second location to which the differential I and Q signals are routed are calibration circuits designed to adjust dc offset and amplitude balance, prior to supplying the signals to the complex modulator IC. The differential outputs of the unity-gain buffers following the analog multiplexers are converted into single-ended signals, IMOD and QMOD, using U24.

Next, I MOD is scaled by a nominal value of 0.2349 using a fixed resistive divider followed by a unity gain buffer (U6). I channel amplitude is subsequently scaled using a serial interface 8-bit D/A converter (U38) as a variable resistor. The scaling ratio ranges from 0.8 to 1.2. During unit calibration, amplitude balance is adjusted for optimum I/Q balance. QMOD is scaled by a nominal value of 0.1958 using a fixed resistive divider.

The complex modulator IC (U45) requires a nominal DC bias of +2.5 volts on the I and Q channel inputs. Summing amplifiers (U4 and U23) are used to obtain the necessary bias required at the inputs of the modulator IC and allow for fine tuning of DC offset voltages. During unit calibration, two 8-bit D/A converters (U38) are used to fine tune I and Q channel DC offset voltages for maximum carrier suppression. The outputs of the D/A converter range from 0 to 5 volts. U19 is used to shift and scale levels to produce IOFFSET and QOFFSET, ranging from -1.25 to +1.25 volts. These voltages are further scaled by the summing amplifiers to yield an differential adjustment range from approximately -30mV to +30mV at the inputs to the modulator 1C.

To obtain the quadrature LO required by the modulator IC, the XMIT IF from the Generator Module is amplified using a monolithic amplifier (AR1) and input to a 6dB hybrid quadrature power splitter (U40). Shunt varactors (D11 and D12) are located on the outputs of the quadrature splitter prior to input to the complex modulator IC (U45). During unit calibration, phase balance is adjusted for optimum I/Q balance. Phase adjustment occurs by simultaneously tuning the DC voltages across the varactors using a D/A converter (U38). The output of the D/A converter ranges from 0 to 5 volts. U26 is used to shift and scale the voltage to produce an output from -4 to +4 volts. U27 is then used to produce a voltage range from +1 to +9 volts across the varactors. As the voltage across one of the varactors increases, the voltage across the other varactor linearly decreases.

D.6.2.3 XMIT IF Routing

Once the transmit IF from the Generator Module enters the iDEN RF module, the IF is routed in one of two general paths depending upon the operating mode selection. The routing is controlled using two GaAsFET switches (U36 and U39) which are switched simultaneously. The +5V CMOS signal OP MODE<0> controls the state of the switches and is toggled high whenever one of the iDEN operating modes is selected. For non-iDEN operating modes, this control bit is low, selecting an RF path containing a discrete amplifier with a nominal 9dB gain. The nominal gain from J1 to J2 is 0 dB when not in iDEN mode.

When the iDEN path is selected, the XMIT IF is amplified using a monolithic amplifier (AR1) and input to a hybrid quadrature power divider (U40). The quadrature LOs produced by the power splitter are applied to the LO inputs of the complex modulator (U45). The modulator IC contains two identical RF outputs, (on the schematic, VMOD OUT A and VMOD OUT B), the outputs being M16-QAM signals at the same frequency as the LO.

Two sub-paths exist within the iDEN path. The first path is used for normal iDEN operation and calibration of the iDEN modulator for a XMlT IF frequency of 310.7MHz. The second path is used only during calibration of the modulator for XMIT IF frequencies of 265.7MHz and 355.7MHz. (±45MHz offsets for Duplex operation).

The first path consists of routing VMOD OUT A to a GaAsFET switch (U37) without frequency translation. The second path consists of routing VMOD OUT B to the RF port of mixer (U31). During unit calibration, when the modulator is being calibrated for generator duplex offsets, a 45MHz is produced at the LO port of mixer. This LO is used to mix 265.7MHz and 355.7MHz transmit IF frequencies to 310.7MHz. After performing the frequency conversion, the signal is filtered to attenuate low frequency mixer products, amplified using a discrete amplifier with a nominal gain of 16dB, and input to GaAsFET switch, U37. The +5V CMOS signal MODCAL controls the state of the switch and is toggled low to select the path without frequency translation. MODCAL simultaneously disables the LO to mixer, U31, by switching off power to the divide-by-5 prescaler, U41, when the path without frequency translation is selected. The output of U37 is amplified using a monolithic amplifier (AR2) prior to being input to the GaAsFET switch (U36) controlling whether or not the iDEN path is selected.

D.6.3 Receiver Section

The receiver section down converts the 10.7MHz RX IF to 450KHz for input to the Abacus IC, which digitizes the signal and provides an output of I and Q samples to the iDEN Digital Assembly. Prior to the down conversion, a programmable attenuator is used to control signal level into the Abacus IC. The 223MHz output of the PLL is divided down using U35 to obtain the 11.15MHz LO required for the down conversion. After the signal is mixed to 450KHz, the signal is filtered and input to the Abacus IC. In addition to supplying the 10.7MHz RX IF to the iDEN receiver, a daisy-chained output is provided for other options requiring 10.7MHz RX IF without AGC.

D.6.3.1 Programmable Attenuator

A three-step programmable attenuator is designed to control the signal level into the Abacus IC. Only two of the steps are used, 0dB and 10dB. The attenuator has the capability to be programmed by two different sources dependent upon the state of the +5V CMOS control bit ATTEN MUX CNTRL. Only one source is currently used, resulting in ATTEN MUX CNTRL always remaining in the low state. The attenuator is set to 10dB by toggling RX ATTEN SW<0> and RX ATTEN SW<1> low. The attenuator is set to 0dB by toggling both of these signals high. Other settings are not used. The iDEN attenuator setting is set to 10dB whenever a front panel monitor attenuation of 20dB or 40dB is selected. If a front panel monitor attenuation of 0dB is selected, the iDEN attenuator setting becomes dependent upon the spectrum analyzer sensitivity setting. For MAX sensitivity, the iDEN attenuator is set to 0 dB and for MIN sensitivity, it is set to 10dB.

Future expansion capability is provided for separate control of the attenuator by the 68302 processor and base RX DSP located on the iDEN Digital Board. In iDEN TEST mode and iDEN BASE mode, the attenuator would be controlled by the 68302 processor based on the power level measured by the standard system wattmeter. In iDEN MOBILE mode, the unit would emulate a iDEN base and perform synchronized software gain control. For this mode, the base RX DSP would calculate the received signal strength and program the attenuator.

G-6.3.2 Abacus IC

The Abacus IC digitizes the 450KHz RX IF and outputs I and Q samples and AGC information in serial data format at a 4.8 MHz rate over a differential low level interface. The 4.8MHz sample clock (ODC) is generated by a digital PLL on the IC using a 2.1MHz reference input from the iDEN Digital Board.

The SBI input is used to program the Abacus IC with a 32 bit word. This word controls the functions of the Abacus IC. The SBI word must be preceded by a low (0) start bit and followed by a low (0) stop bit creating an actual word length of 34 bits. The ODC is used to clock the SBI. On every fourth rising transition, a new bit of SBI is represented. The data rate for the SBI is 1.2Mbits/second with ODC at 4.8MHz. Thus, with ODC at 4.8MHz, the word duration is 28.3 usec. The input data is formatted MSB first [31:0].

The differential DOUT and DOUTX output data contains the output of the Abacus decimation filters (in I & Q format), the AGC value, the imbedded sync pattern, and fill bits. The I & Q information from the decimation filters is MSB first and formatted 16 bit words (excluding the 3 sync bits). The I word is preceded by a 6 bit packet of 1's and every sixth bit is a 1 in the data and AGC information. The Q word is preceded by a 6 bit packet of 0's and every sixth bit is a 0 in the data and AGC information. The AGC value contains a flag bit (the SWAS bit, for switched amp state) indicating whether the Abacus first IF amplifier is in the low or high gain state (SWAS=1, amp gain is in high gain; SWAS=0, amp gain is 10 dB lower) and the eight bit word of the AGC DAC. A total of 80 bits with ODC at 4.8MHz results in an I/Q sampling rate of 60 Ksamples/sec.

D.6.3.3 Daisy-Chained 10.7MHz Output

The iDEN receiver uses the 10.7MHz RX IF input without AGC from the Receiver Module located in the standard system. In order to allow other options to be installed on the same system as the iDEN option, a daisy-chained output is provided. The 10.7MHz input is split into two paths upon module entry using a resistive divider. While one path is routed through the programmable attenuator for down conversion and use by the Abacus IC, the other path is routed through a discrete amplifier and pad for output at J4.

D.6.4 Modulator Calibration Sequence Section

During unit calibration, the iDEN complex modulator is calibrated for maximum carrier suppression and optimum I/Q balance. Calibration is performed for the generator XMIT IF frequency of 310.7MHz and for the duplex generator XMIT IF frequencies of 310.7+45MHz.

The same cal factors obtained for the +45MHz and -45MHz duplex offsets are used for +48MHz and -48MHz duplex offsets, respectively. Modulator calibration consists of tuning four 8-bit D/A converters contained on a single chip (U38). The first two D/A converters independently control I and Q channel DC offset voltages. These influence carrier suppression. The third D/A converter controls amplitude balance by fine tuning I channel amplitude. The fourth D/A converter controls phase balance by fine tuning the phase difference of the quadrature modulator LOs. Amplitude and phase balance influence I/Q balance.

During the iDEN OPTION portion of calibration, carrier suppression precedes I/Q balance. When performing carrier suppression calibration, the Tranlin IC generates a carrier-only test pattern. A XMIT IF of 355.7MHz (310.7+45MHz) is produced by the generator module. After exiting the complex modulator IC, this signal is mixed to a XMIT IF of 310.7MHz. The Spectrum Analyzer Module located in the standard system is used to measure signal level. DC offsets are adjusted until minimum signal level is obtained. This procedure is repeated for a XMIT IF of 265.7MHz (310.7-45MHz) with the signal being mixed to 310.7MHz after exiting the complex modulator IC as before. Carrier suppression calibration of the generator 310.7MHz XMIT IF occurs last. No frequency translation is required for this case.

Next, I/Q balance is calibrated. For this, the Tranlin IC generates a +10KHz single-sideband test pattern. A XMIT IF of 355.71MHz (310.71 + 45MHz) is produced by the generator module. After exiting the complex modulator IC, this signal is mixed to a XMIT IF of 310.71MHz, resulting in the undesired sideband being located at 310.7MHz. The Spectrum Analyzer Module located in the standard system is used to measure the undesired signal level sideband. Amplitude balance and phase balance are adjusted until minimum signal level is obtained. This procedure is repeated for XMIT IF frequencies of 265.71 MHz and 310.71 MHz in the same manner as described above for carrier suppression.

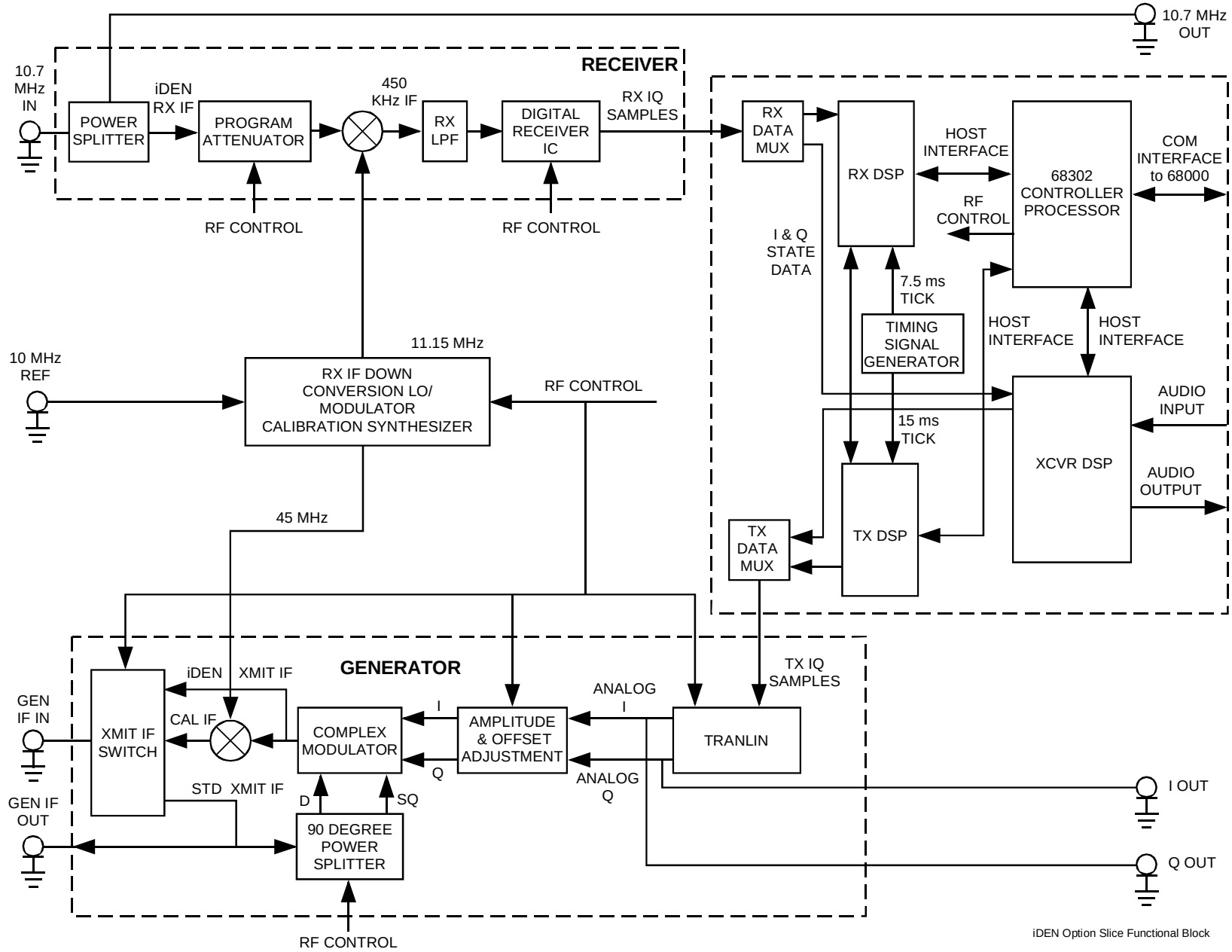


Figure D.1 iDEN Option Slice Functional Block Diagram

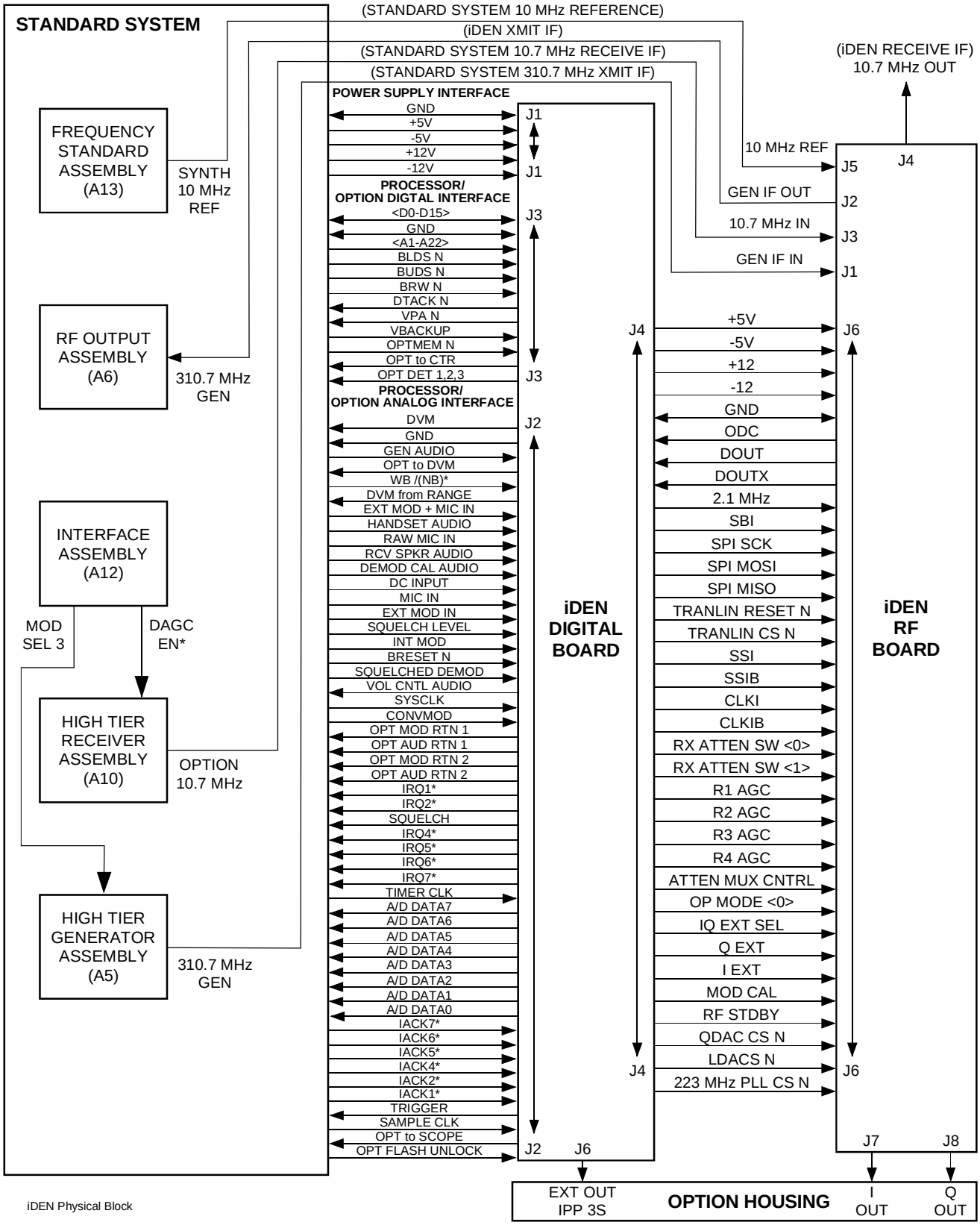
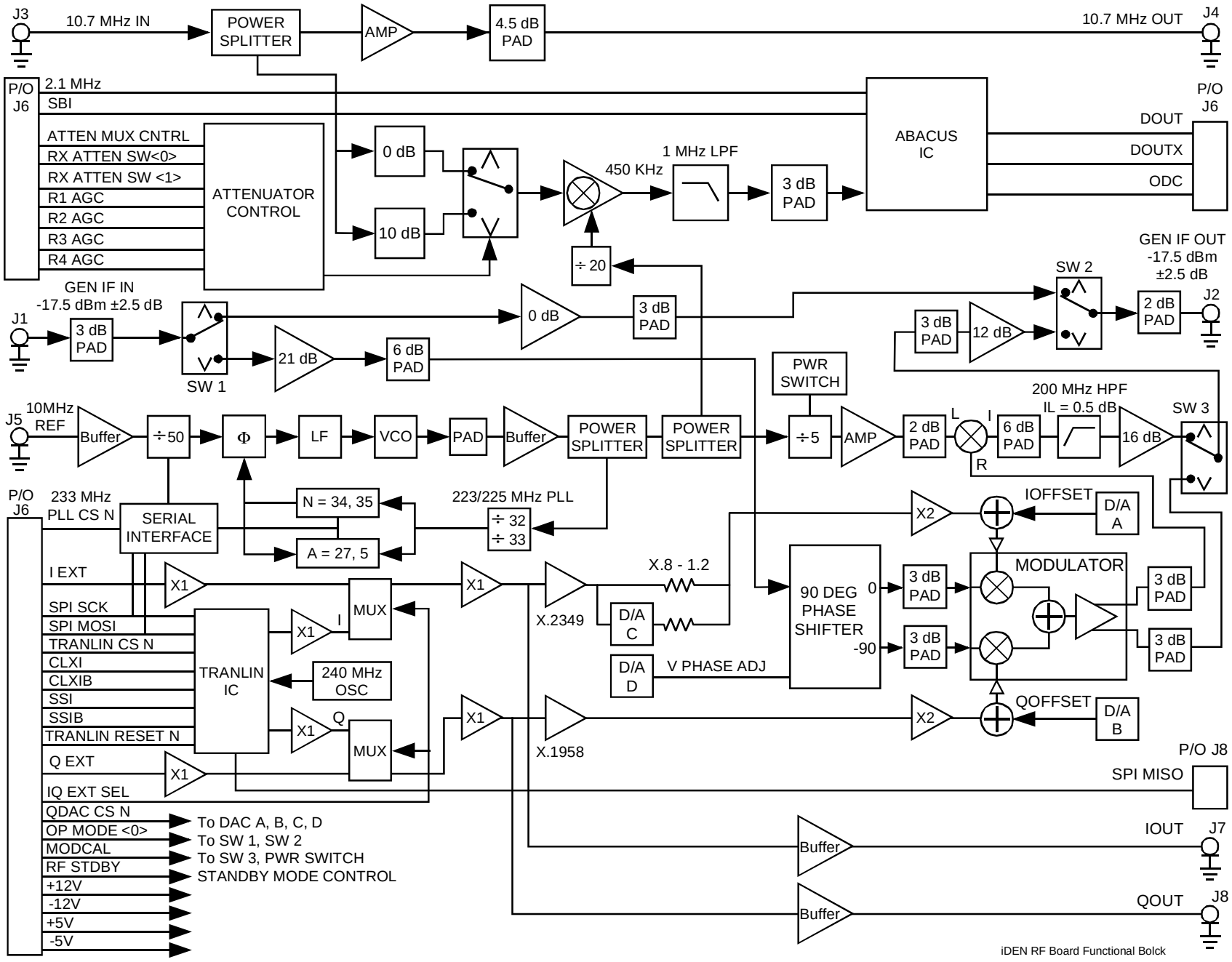


Figure D.2 iDEN Physical Block Diagram

Figure D.3 iDEN RF Board Functional Block Diagram



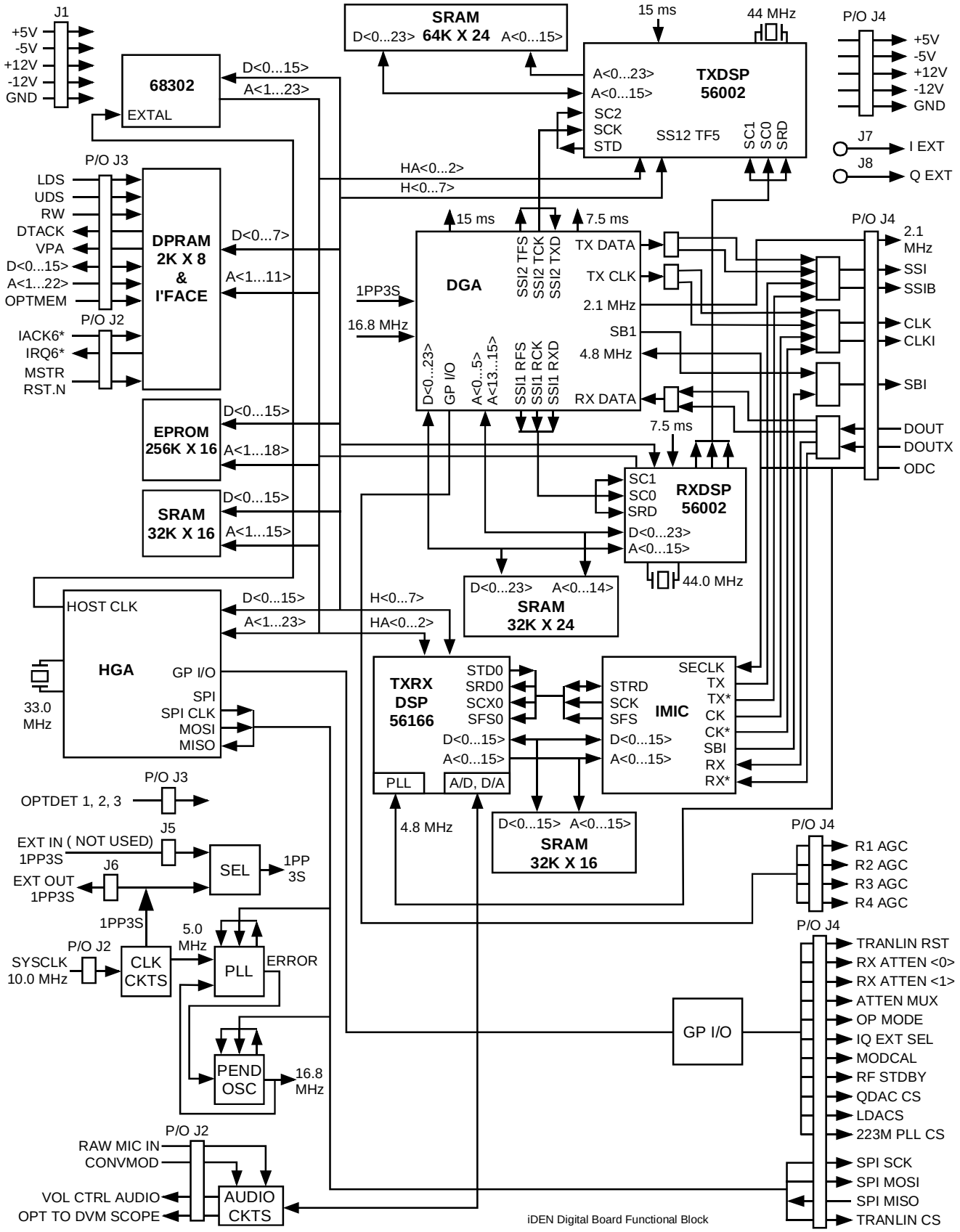
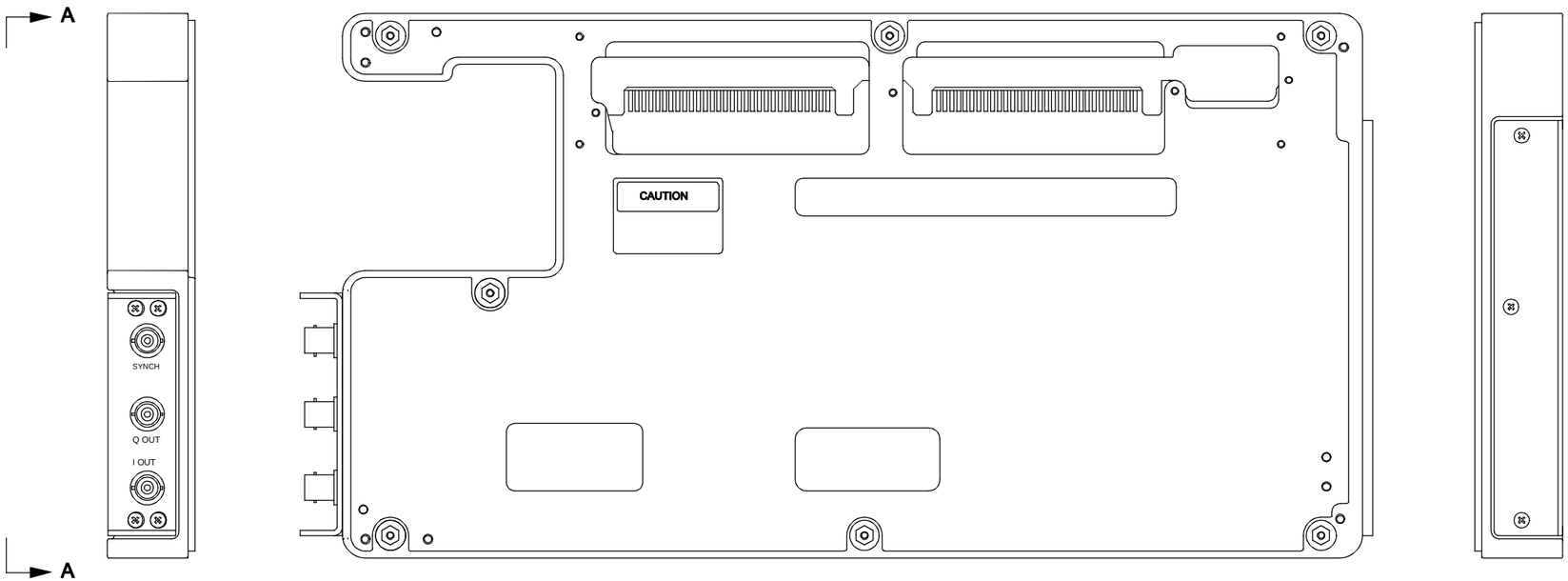
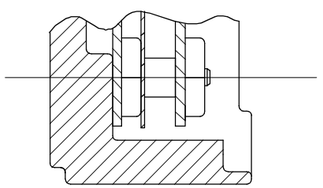
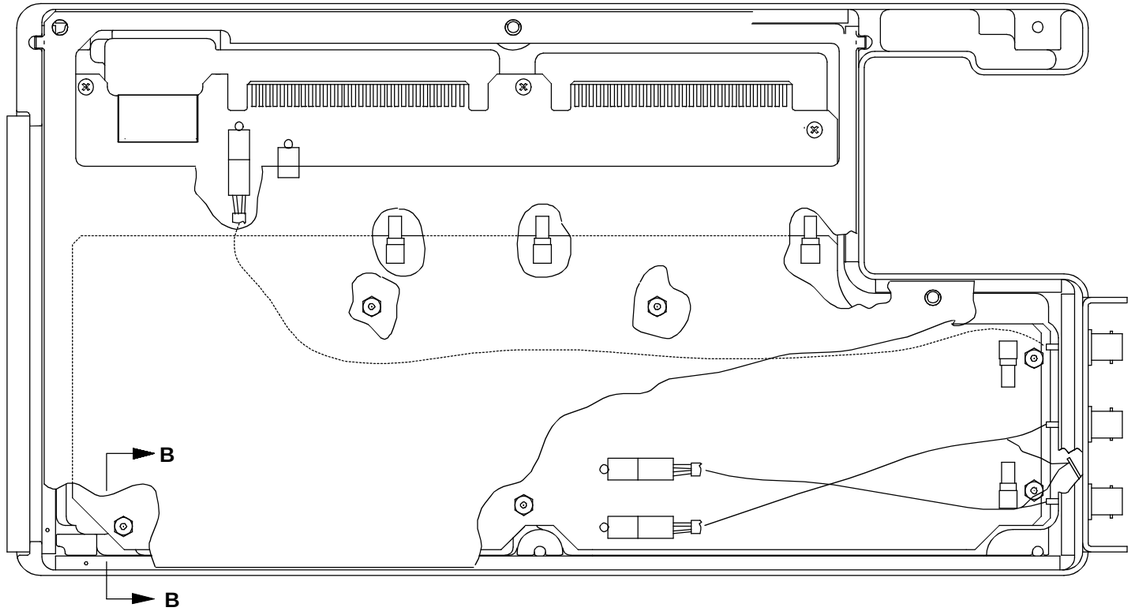


Figure D.4 iDEN Digital Board Functional Block Diagram





SECTION B-B



VIEW A-A

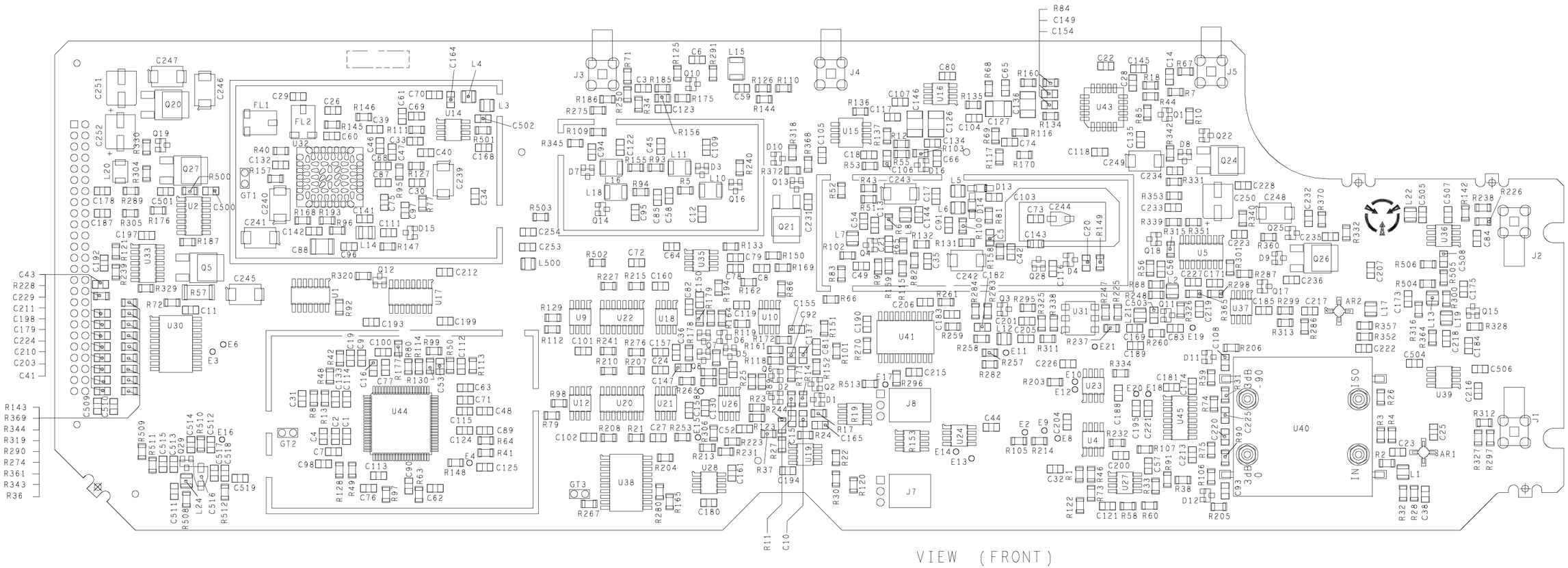
TABLE 1		
WIRE NO	FROM	TO
1	A2J6	SYNCH
2	A1J7	Q OUT (STRIPED WIRE)
2A	A1J7	E1 (SOLID WIRE)
3	A1J8	I OUT (STRIPED WIRE)
3A	A1J8	E1 (SOLID WIRE)
4	A1J1	A5J1 (SYSTEM)
5	A1J2	A6J1 (SYSTEM)
6	A1J3	A10J3 (SYSTEM)
7	A1J5	A13J2 (SYSTEM)

CAUTION
THIS ITEM IS SENSITIVE TO ELECTROSTATIC DISCHARGE (ESD).

OPTION ASSEMBLY MIRS

01-P37900N REV. A

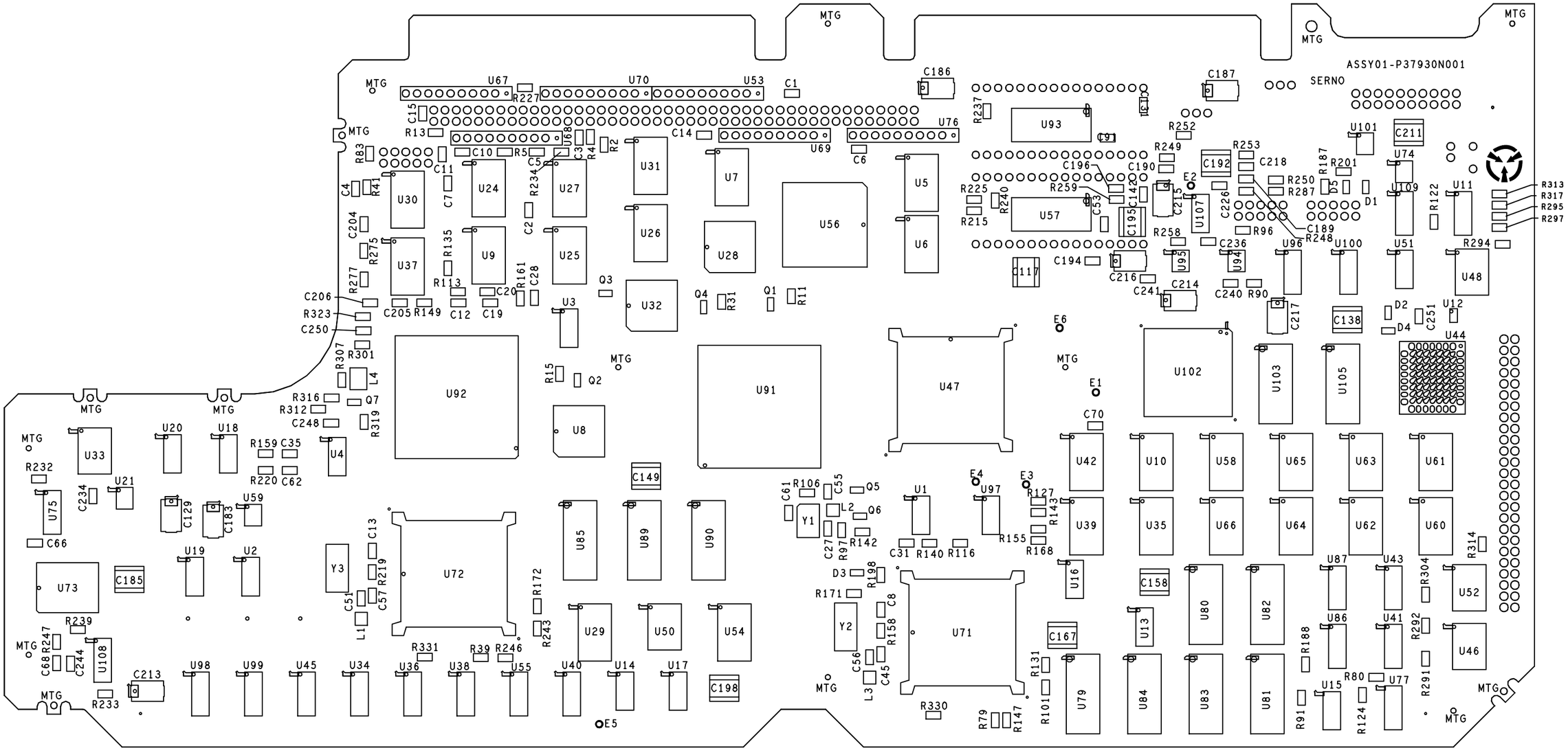
SHEET 1 OF 1



CIRCUIT CARD ASSEMBLY
iDEN RF

01-P37920N REV. E

SHEET 1 OF 1



FRONT, COMPONENT SIDE

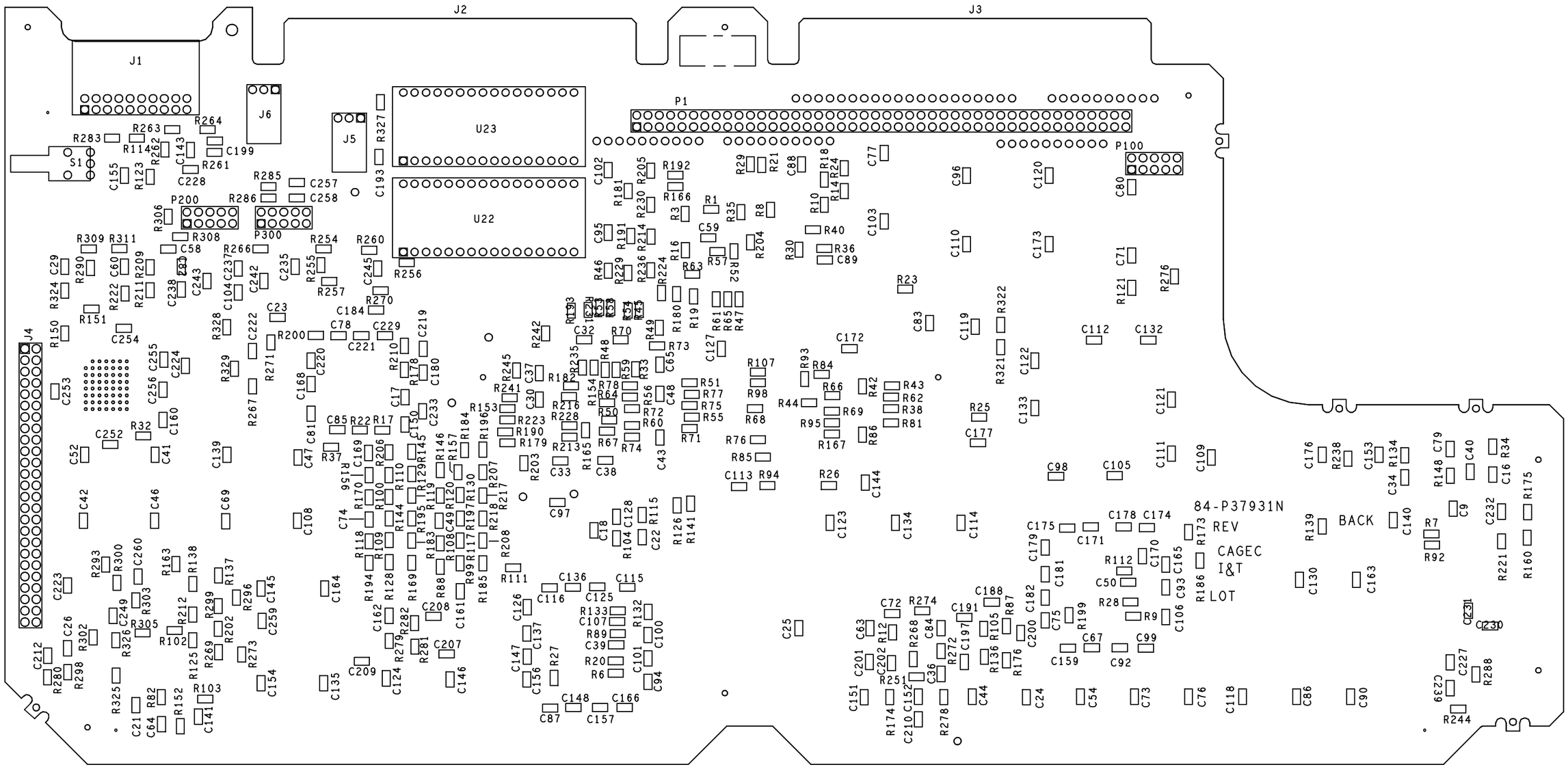
CAUTION

THIS ITEM IS SENSITIVE TO ELECTROSTATIC DISCHARGE (ESD)

CIRCUIT CARD ASSEMBLY
i DEN DIGITAL

01-37930N REV. B

SHEET 1 OF 2



BACK, SOLDER SIDE

CAUTION

THIS ITEM IS SENSITIVE TO ELECTROSTATIC DISCHARGE (ESD)

CIRCUIT CARD ASSEMBLY
i DEN DIGITAL

01-37930N REV. B

SHEET 2 OF 2

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED
-	INITIAL RELEASE		
A	SEE MCO E36124 VAH 95-04-05	95-04-06	A. KOESNTER
B	SEE CO E36541-1 CJN 00-02-03	00-02-03	A. GATTO
C	SEE CO L48754-3 IDB 00-11-20	00-11-20	A. GATTO

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A19A1.

2. FOR REFERENCE DRAWINGS REFER TO:
   ASSEMBLY 01-P37920N
   TEST PROCEDURE 12-P37923N

3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS +/-1PCT, .125WATTS.
   ALL CAPACITANCE VALUES ARE +/- 5PCT, 50V.
   ALL VOLTAGES ARE IN VDC.

4. TERMINATIONS CODED WITH THE SAME LETTERS OR NUMBERS ARE ELECTRICALLY CONNECTED.

5. DEVICE TYPE NUMBERS AND CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE I.

6. DEVICE TYPE IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH MANUFACTURER. ENGINEERING APPROVED EQUIVALENT DEVICE MAY BE USED.

7. COMPONENT VALUE SELECTED IN TEST. NOMINAL VALUE SHOWN.

8. DO NOT INSTALL COMPONENT IF EXTERNAL I/Q INPUT CAPABILITY IS REQUIRED.

9. THIS IS AN OPTIONAL COMPONENT AND MAY OR MAY-NOT BE INSTALLED ON THIS ASSEMBLY.

REFERENCE DESIGNATIONS	
HIGHEST NUMBER USED	NOT USED
AR2	
C519	C50, C51, C55, C99, C129, C148, C152, C153, C156 C159, C170, C208, C237, C238, C255-C499
D16	
E21	E5, E7
FL2	
GT3	
J8	
L500	L9, L25-L499
Q29	Q9
R513	R78, R140, R202, R209, R211, R212, R216, R217, R218, R220, R221, R222, R229, R230, R242, R243 R245, R246, R251, R252, R254, R255, R263, R264, R266, R268, R269, R277, R278, R279, R281, R292, R293, R294, R309, R310, R321, R323, R333, R336, R346, R347, R348, R354, R356, R362, R363, R371, R373-R499
U45	U3, U7, U11, U13, U29, U34, U42

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

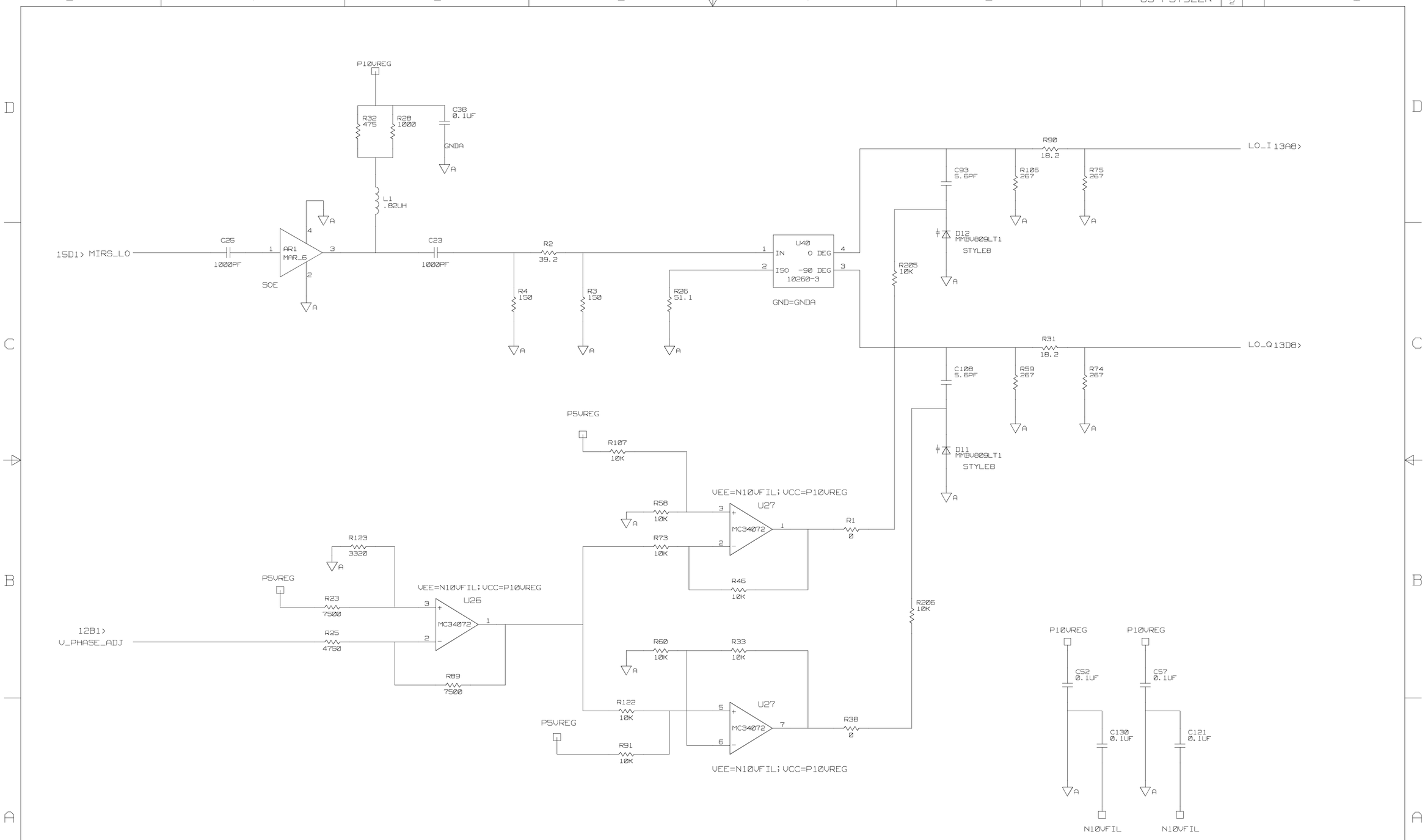
ALL SHEETS ARE THE SAME REVISION STATUS

		CONTR	
		ISS RN B35550-271	
		APPROVALS	
		DWN P. AMMON 94-07-20	
		CHKR M. MILLER 94-07-20	
		QA K. NELSON 94-07-20	
		MATL W. MCDONALD 94-07-20	
01-P39720N	COCHISE	MFG S. CASH 94-07-20	
NEXT ASSY	USED ON	ENG A. KOESNTER 94-07-20	
APPLICATION		CUST	

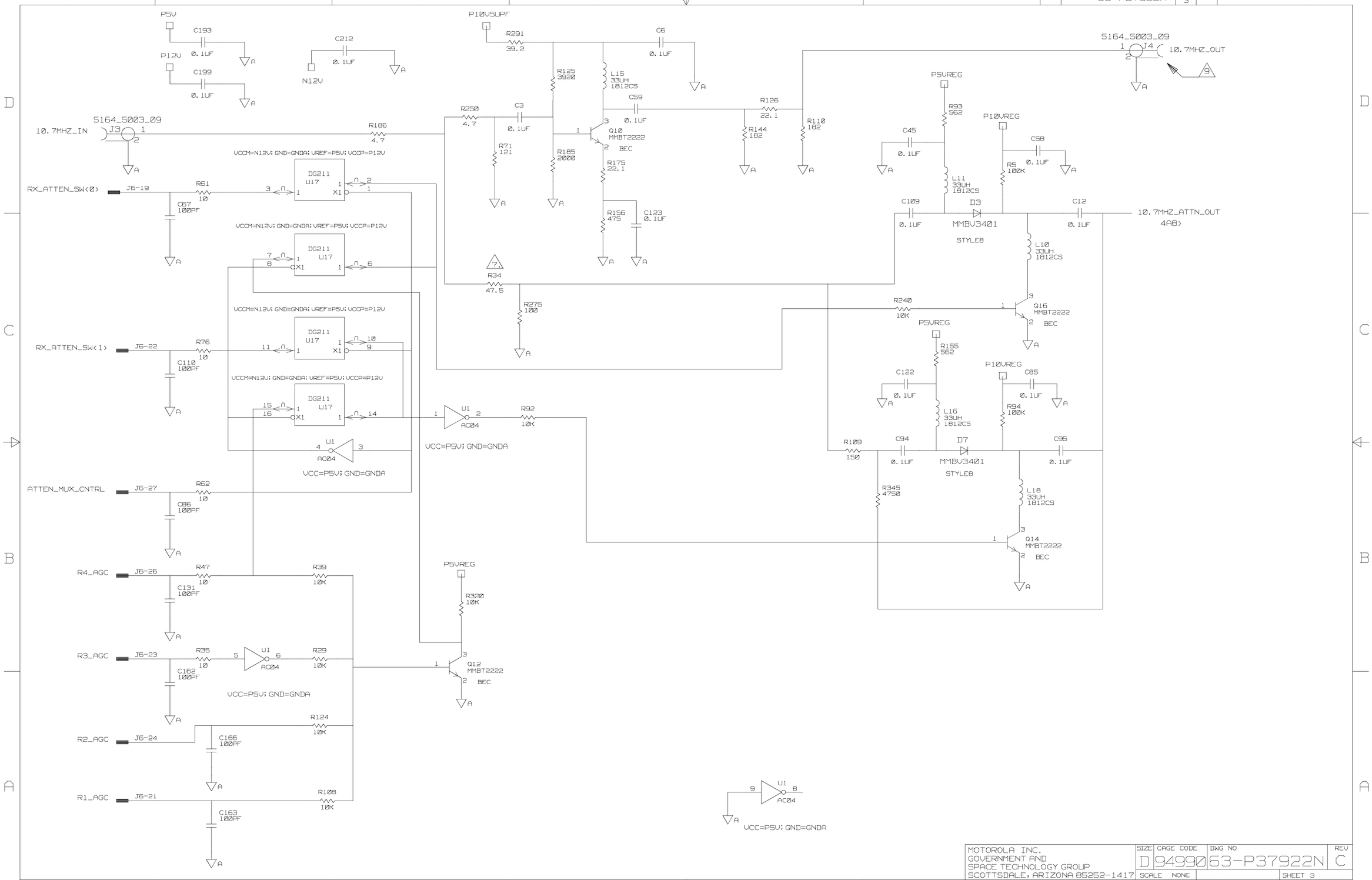
MOTOROLA INC.
GOVERNMENT AND SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

TITLE
SCHEMATIC DIAGRAM IDEN RF

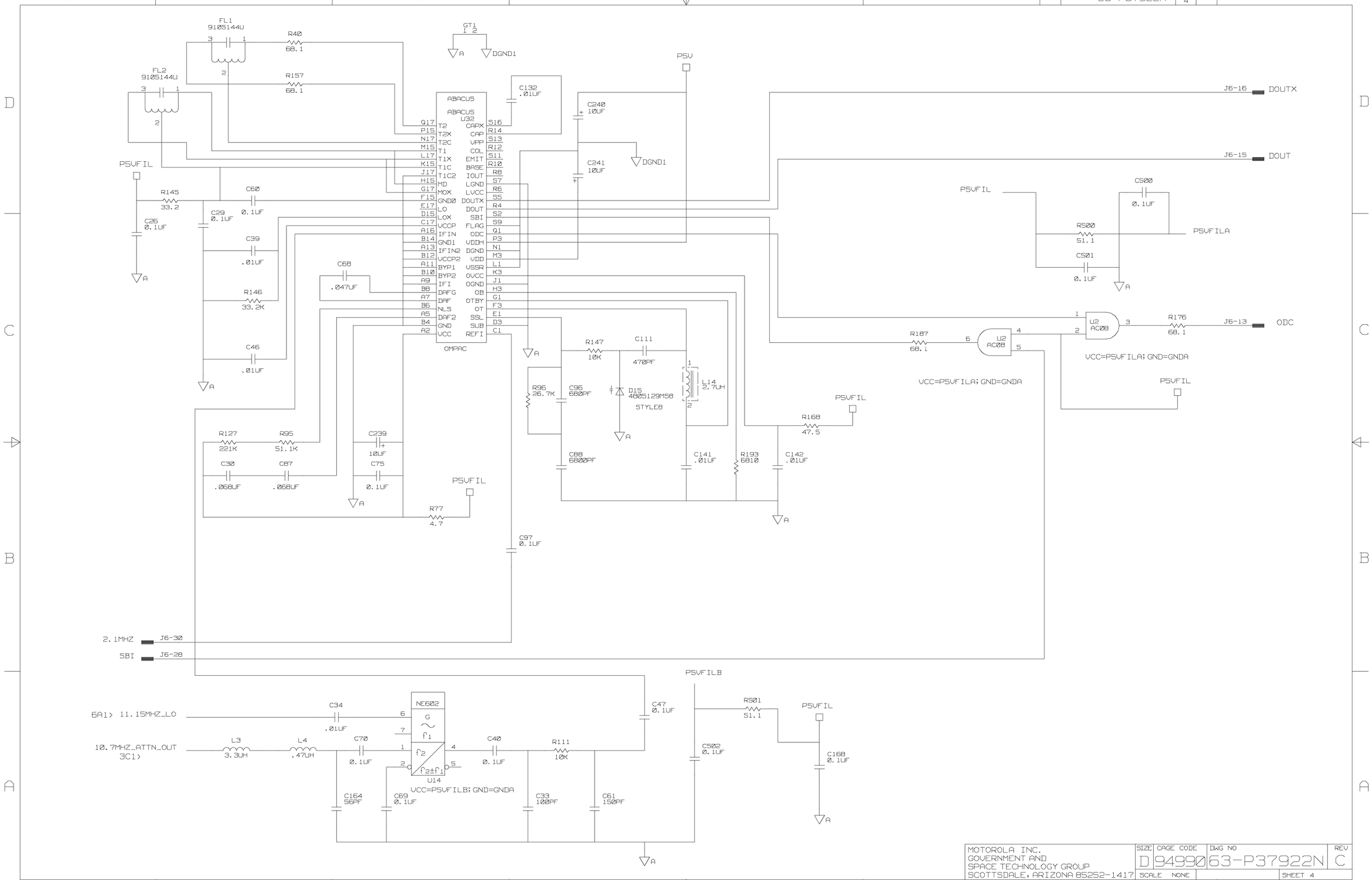
SIZE	CAGE CODE	DWG NO
D	94990	63-P37922N
SCALE NONE		SHEET 1 OF 18



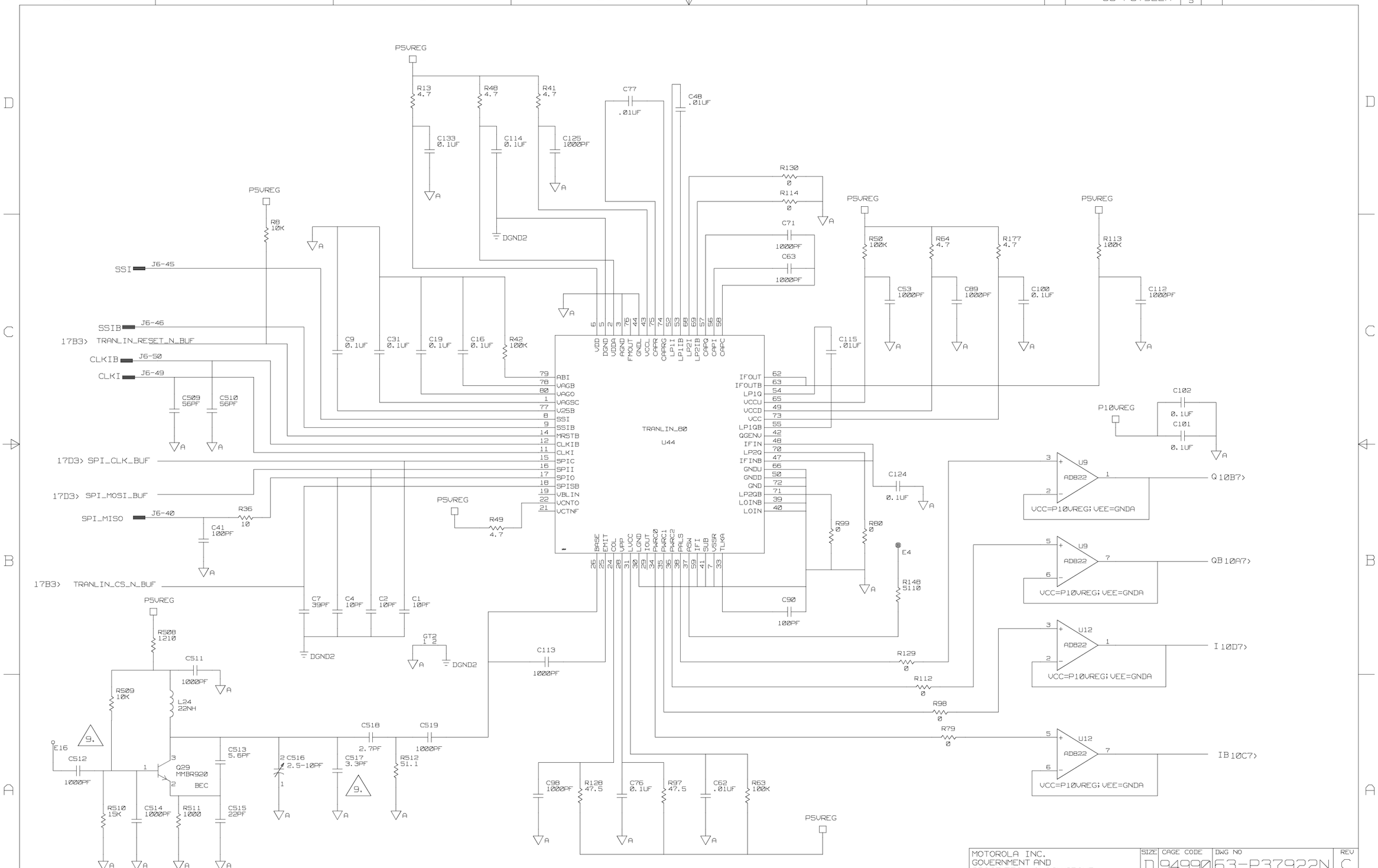
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37922N	REV C
	SCALE NONE		SHEET 2	

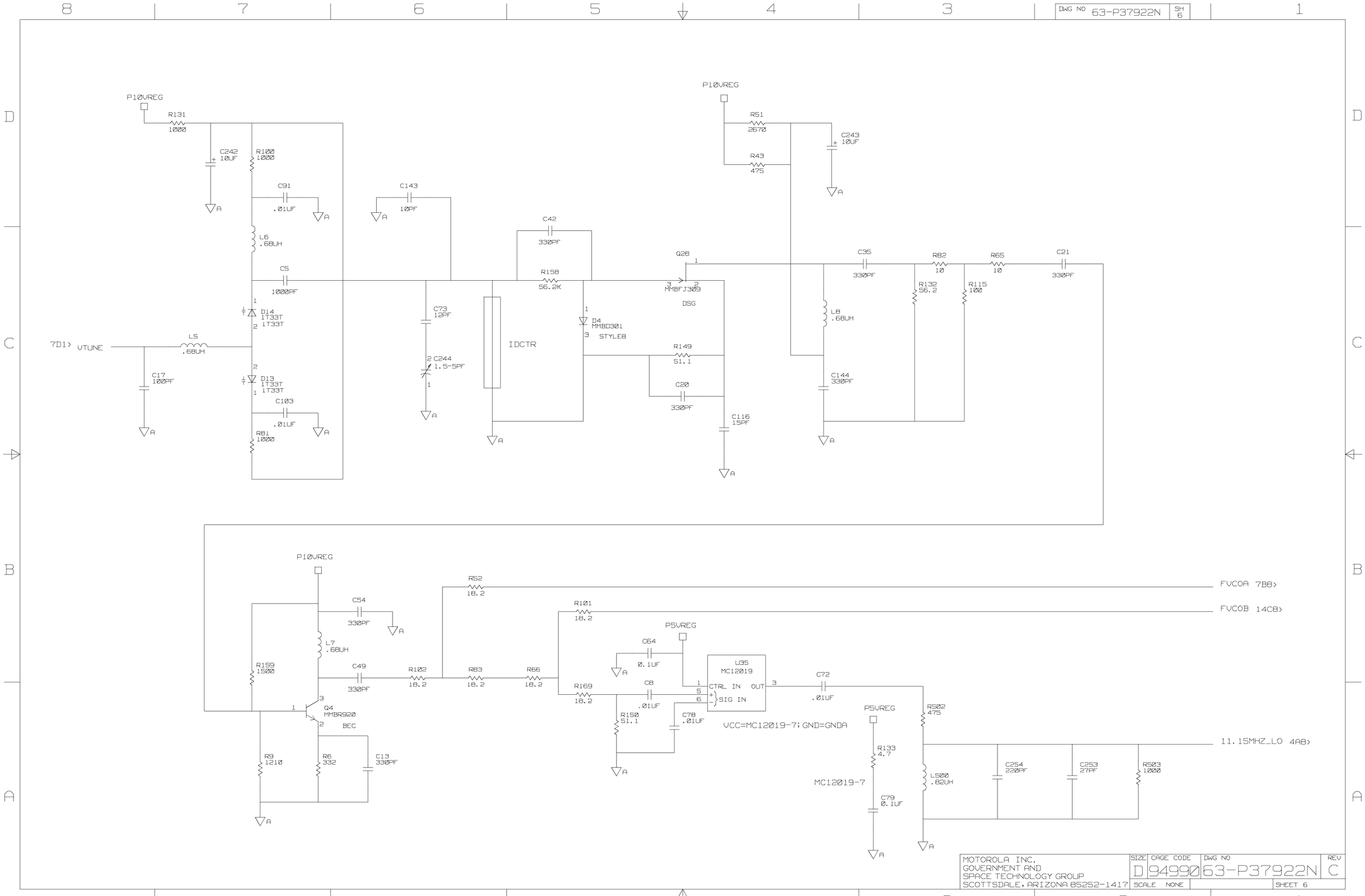


MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37922N	REV C
	SCALE NONE		SHEET 3	

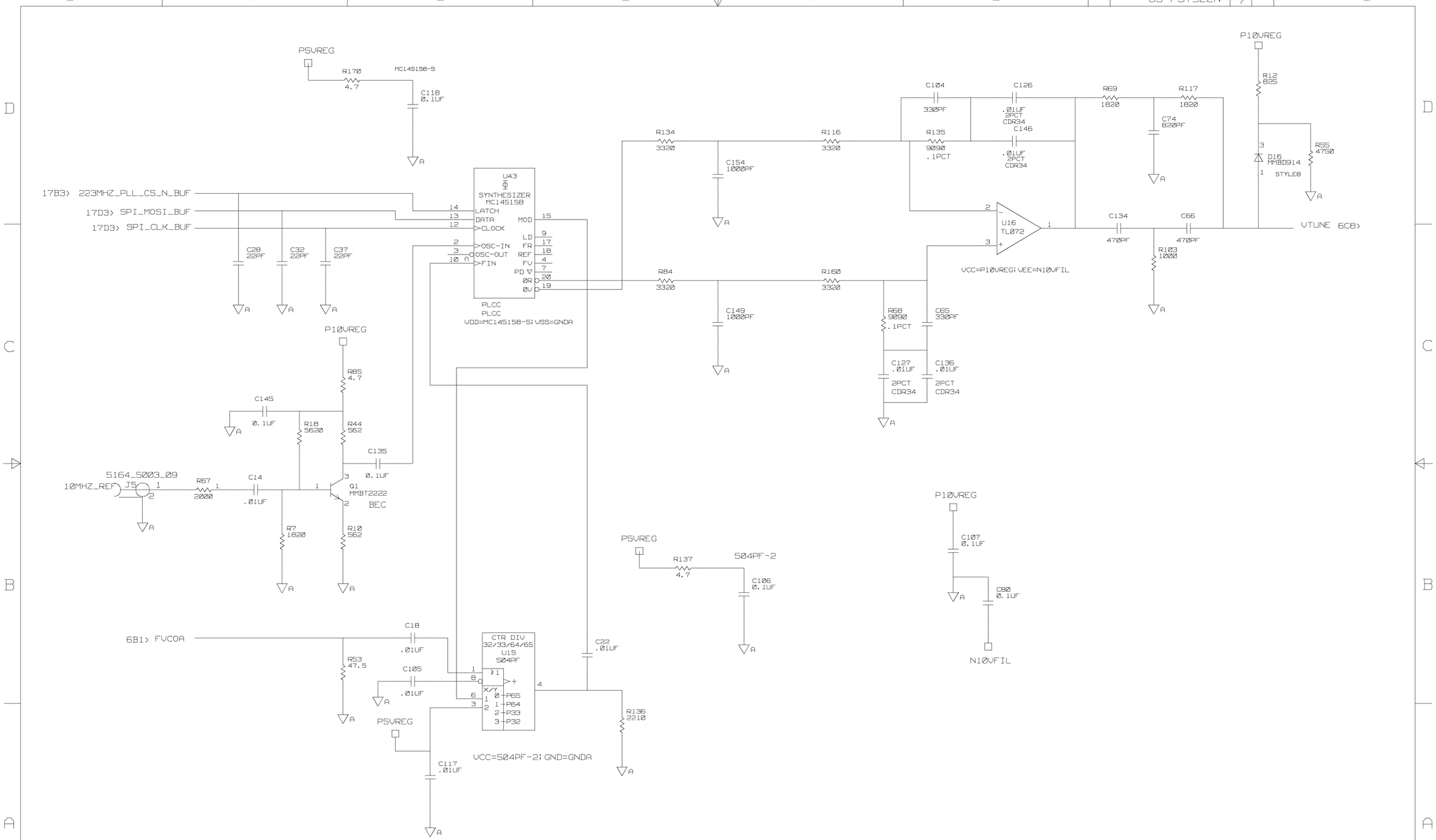


MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37922N	REV C
	SCALE NONE		SHEET 4	

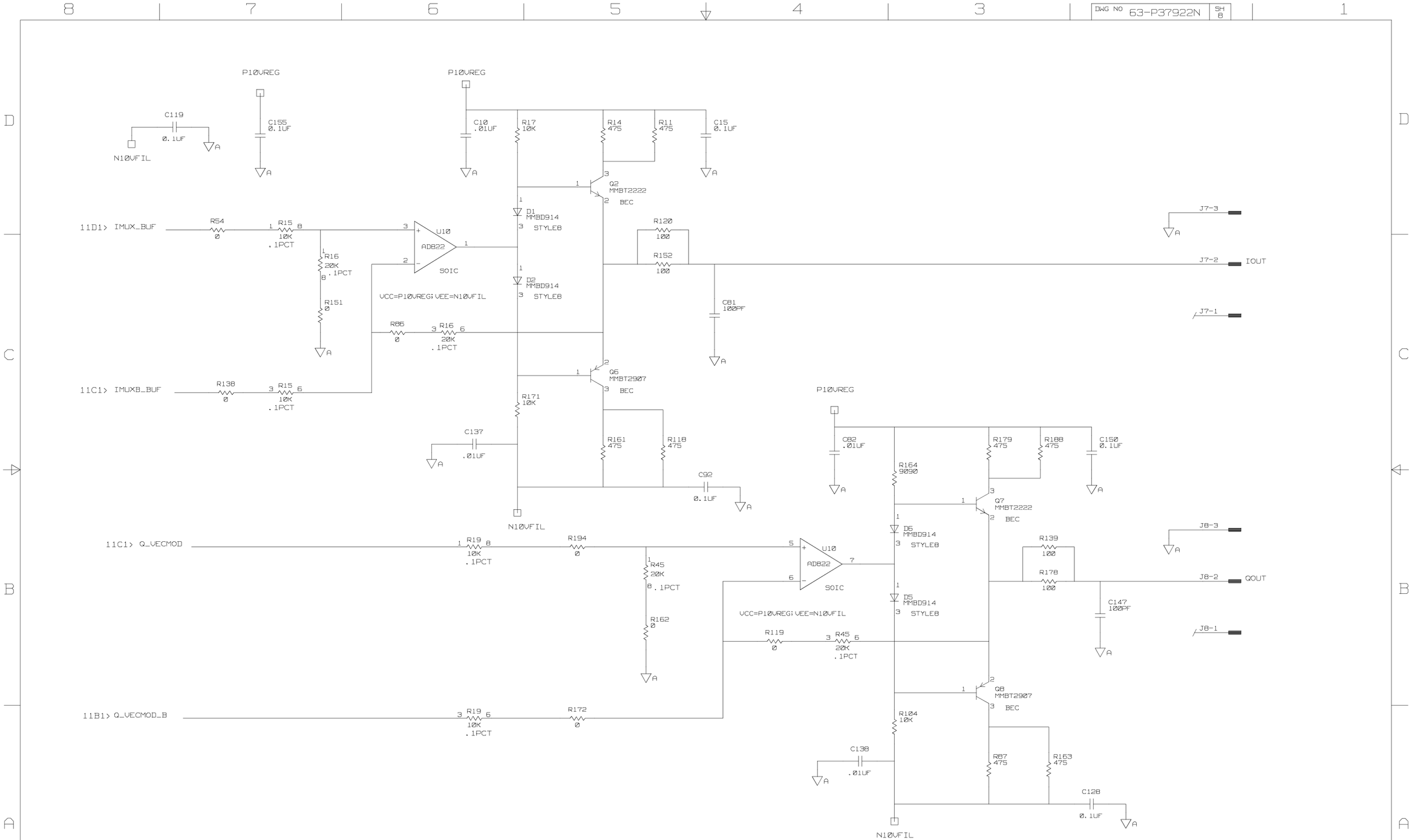

DWG NO 63-P37922N SH 5
P5VREG
R13 4.7
R48 4.7
R41 4.7
C133 0.1UF
C114 0.1UF
C125 1000PF
C77 .01UF
C48 .01UF
DGND2
R130 0
R114 0
C71 1000PF
C63 1000PF
R8 10K
SSI J6-45
SSIB J6-46
17B3> TRANLIN_RESET_N_BUF
CLKIB J6-50
CLKI J6-49
C509 56PF
C510 56PF
17D3> SPI_CLK_BUF
17D3> SPI_MOSI_BUF
SPI_MISO J6-40
R36 10
C41 100PF
17B3> TRANLIN_CS_N_BUF
C9 0.1UF
C31 0.1UF
C19 0.1UF
C16 0.1UF
R42 100K
R50 100K
R64 4.7
R177 4.7
R113 100K
C53 1000PF
C89 1000PF
C100 0.1UF
C112 1000PF
C115 .01UF
P10VREG
C102 0.1UF
C101 0.1UF
TRANLIN_80
U44
ABI
VAGB
VAGO
VAGSC
V25B
SSI
SSIB
MRSTB
CLKIB
CLKI
SPIC
SPII
SPIO
SPISB
VBLIN
VCNTO
VCTNF
VID
DGND
VDDA
AGND
FMOUT
GNDL
VCCL
CAPR
CAPRG
LP1I
LP1IB
LP2I
LP2IB
CAPQ
CAPI
CAPC
IFOUT
IFOUTB
LP1Q
VCCU
VCCD
VCC
LP1QB
QGENV
IFIN
LP2Q
IFINB
GNDU
GNDD
GND
LP2QB
LOINB
LOIN
BASE
EMIT
COL
VPP
LVCC
LGND
IOUT
PWRC0
PWRC1
PWRC2
PALS
PDW
IFI
SUB
VSSR
TLKA
R49 4.7
C124 0.1UF
R99 0
R80 0
E4
R14B 5110
C90 100PF
C7 39PF
C4 10PF
C2 10PF
C1 10PF
GT2
C113 1000PF
R129 0
R112 0
R98 0
R79 0
U9
ADB22
VCC=P10VREG; VEE=GNDA
Q10B7>
QB10A7>
U12
I10D7>
IB10C7>
R508 1210
C511 1000PF
R509 10K
L24 22NH
E16
C512 1000PF
Q29 MMBR920
BEC
C513 5.6PF
C516 2.5-10PF
C517 3.3PF
C518 2.7PF
C519 1000PF
R512 51.1
R510 15K
C514 1000PF
R511 1000
C515 22PF
C98 1000PF
R128 47.5
C76 0.1UF
R97 47.5
C62 .01UF
R63 100K
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D
CAGE CODE 94990
DWG NO 63-P37922N
REV C
SCALE NONE
SHEET 5



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37922N	REV C
	SCALE NONE		SHEET 6	

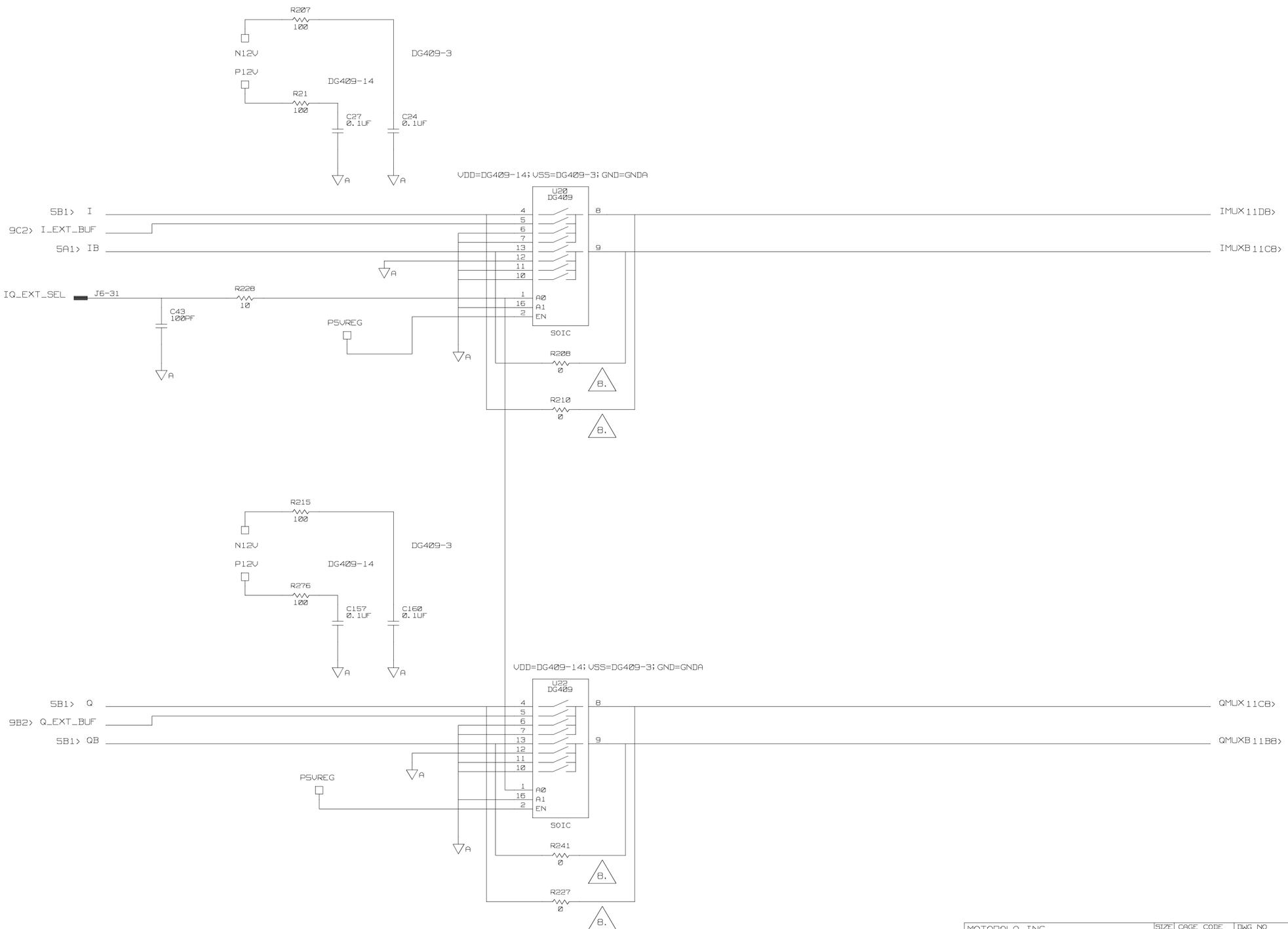


MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37922N	REV C
	SCALE NONE			SHEET 7

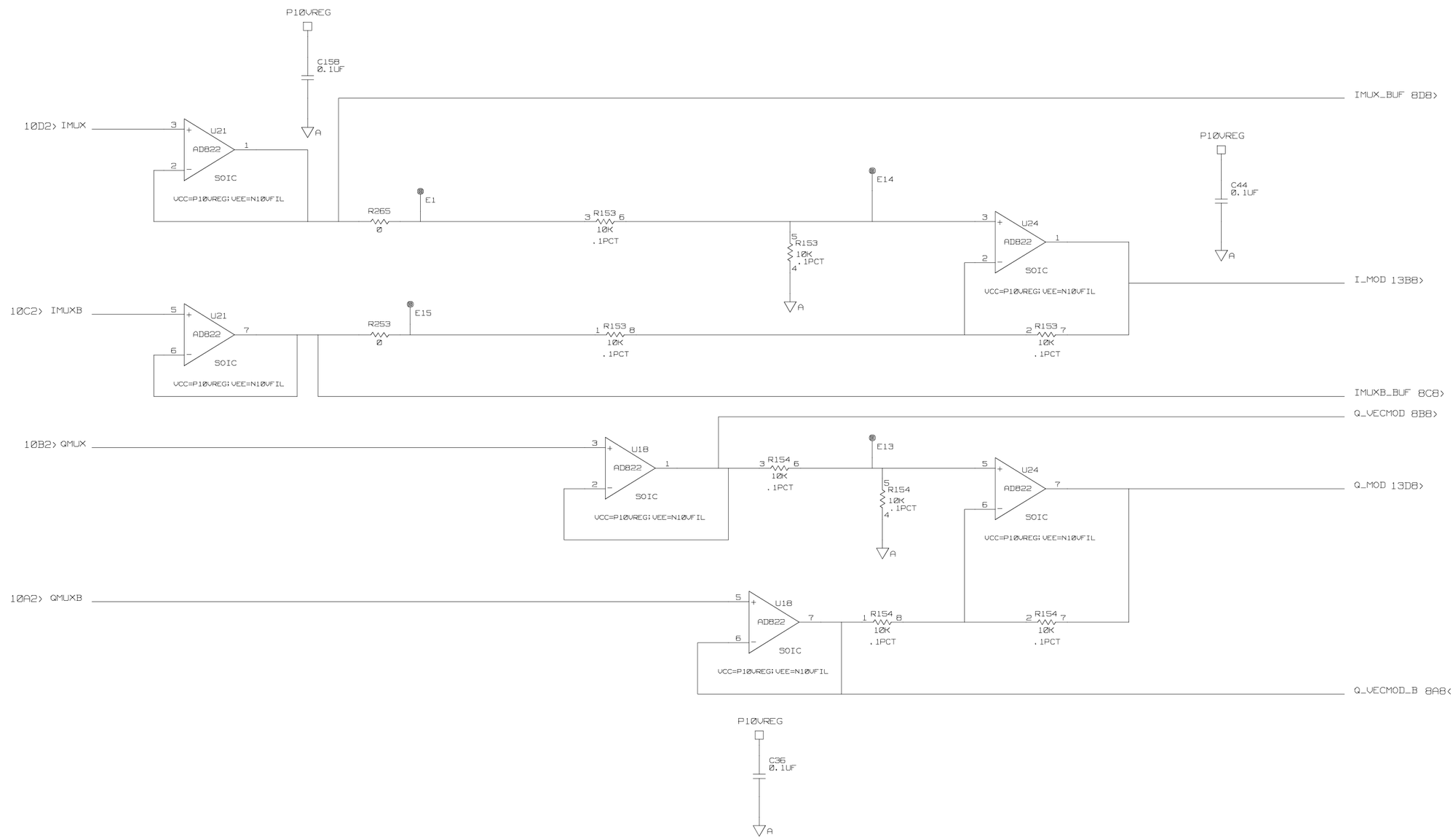


MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37922N	REV C
	SCALE NONE			SHEET 8

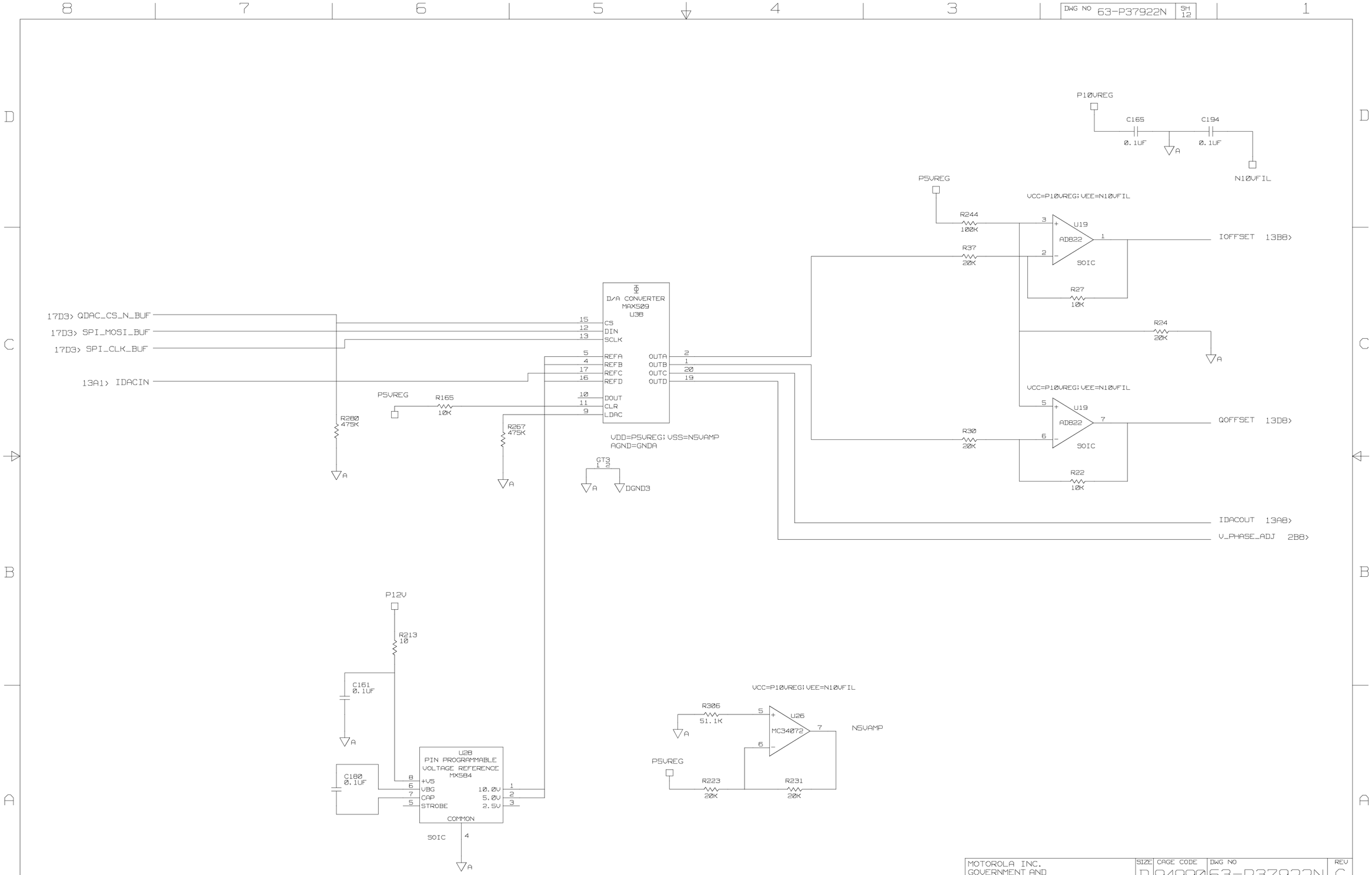
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE	CAGE CODE	DWG NO	REV
	D	94990	63-P37922N	C
	SCALE NONE		SHEET 9	



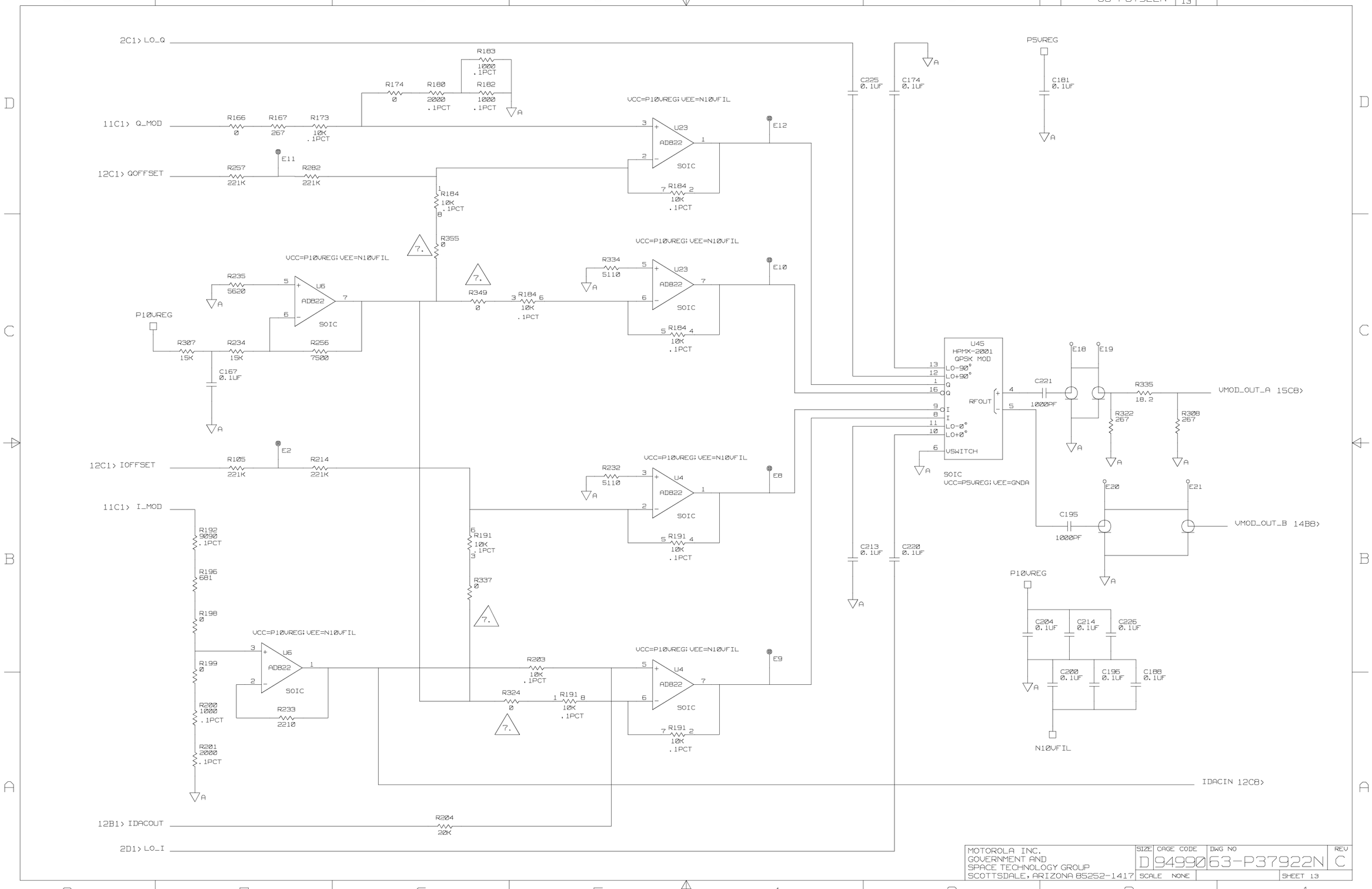
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37922N	REV C
	SCALE NONE			SHEET 10



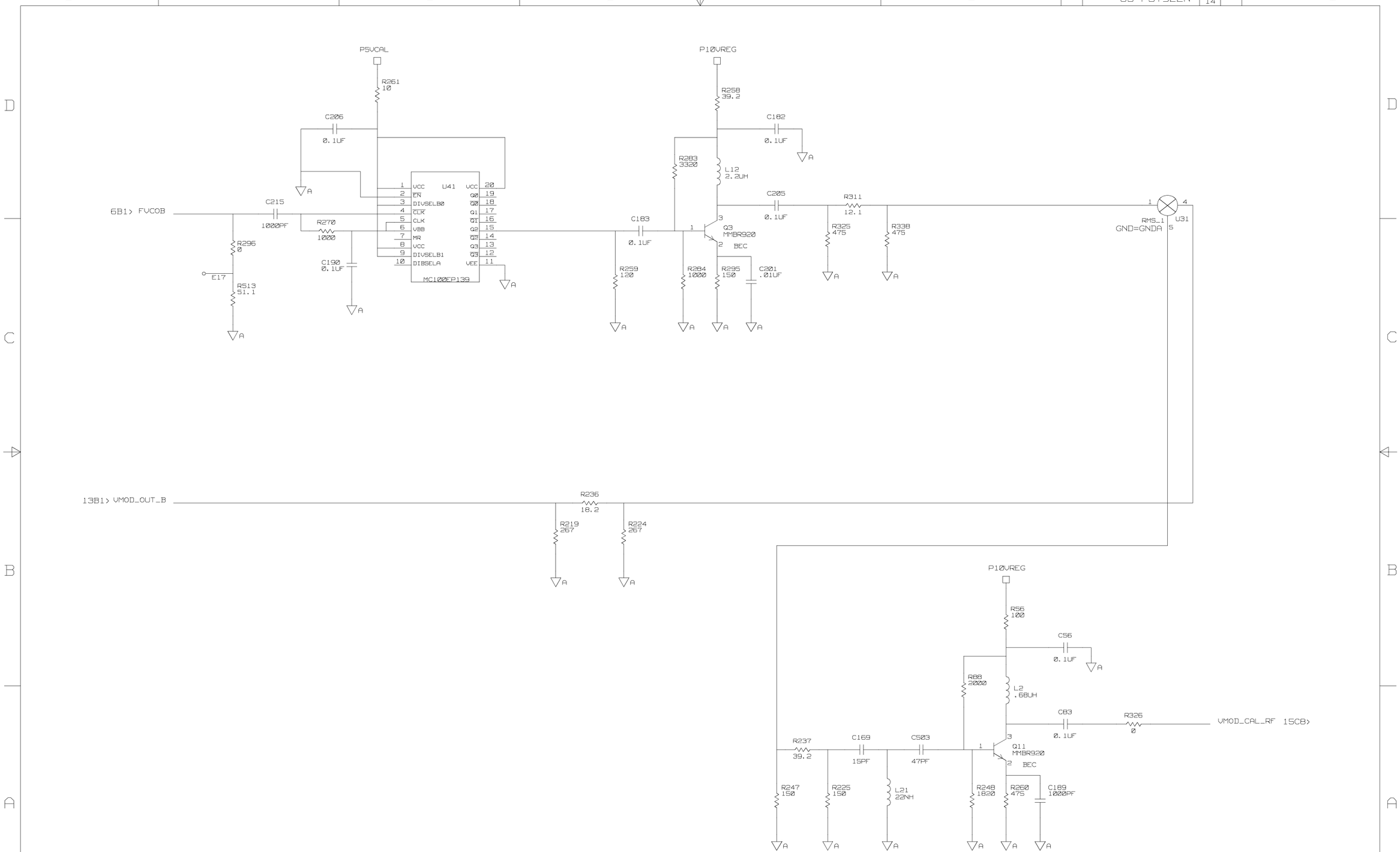
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37922N	REV C
	SCALE NONE			SHEET 11



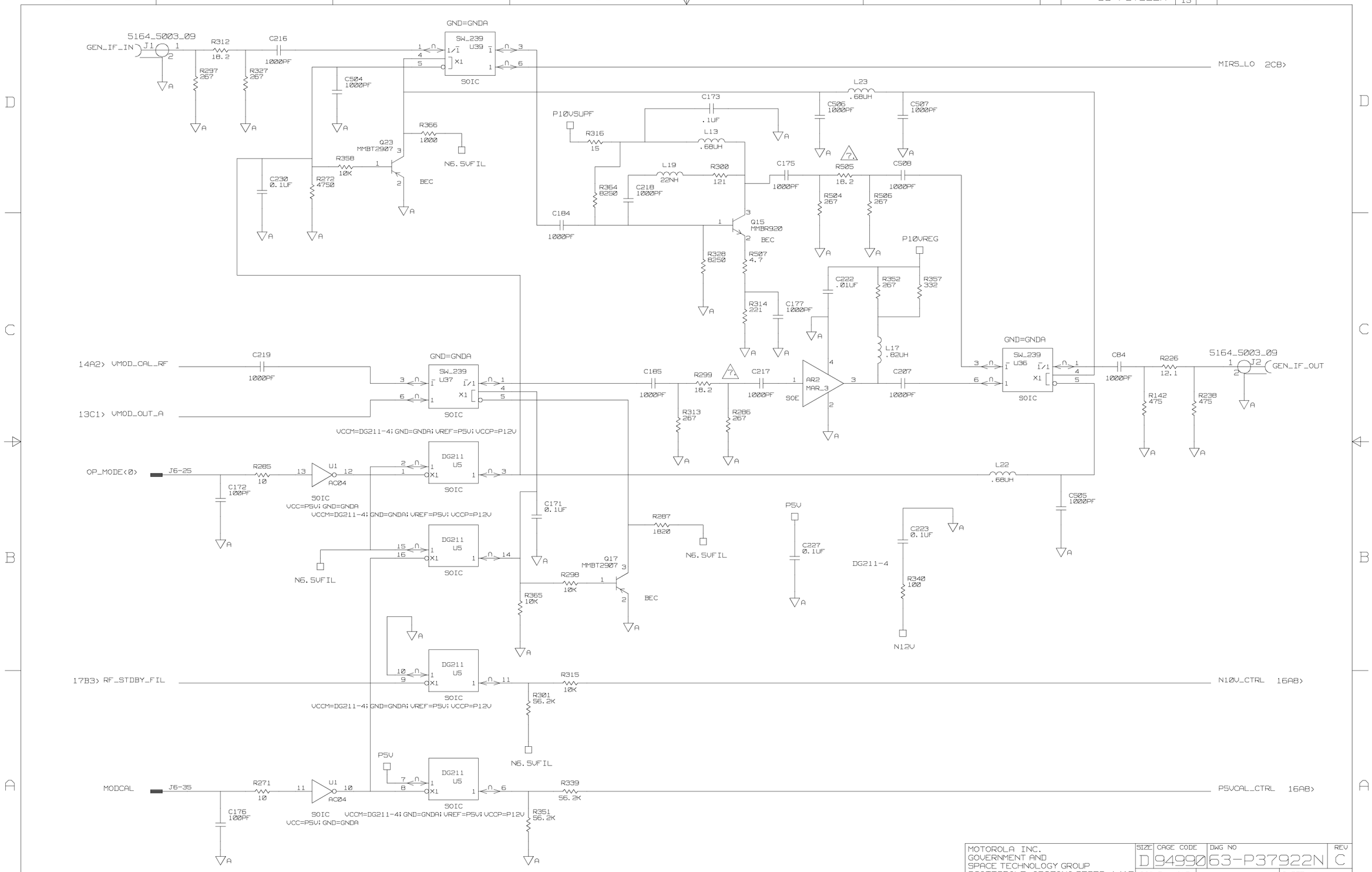
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE	CAGE CODE	DWG NO	REV
	D	94990	63-P37922N	C
	SCALE NONE		SHEET 12	



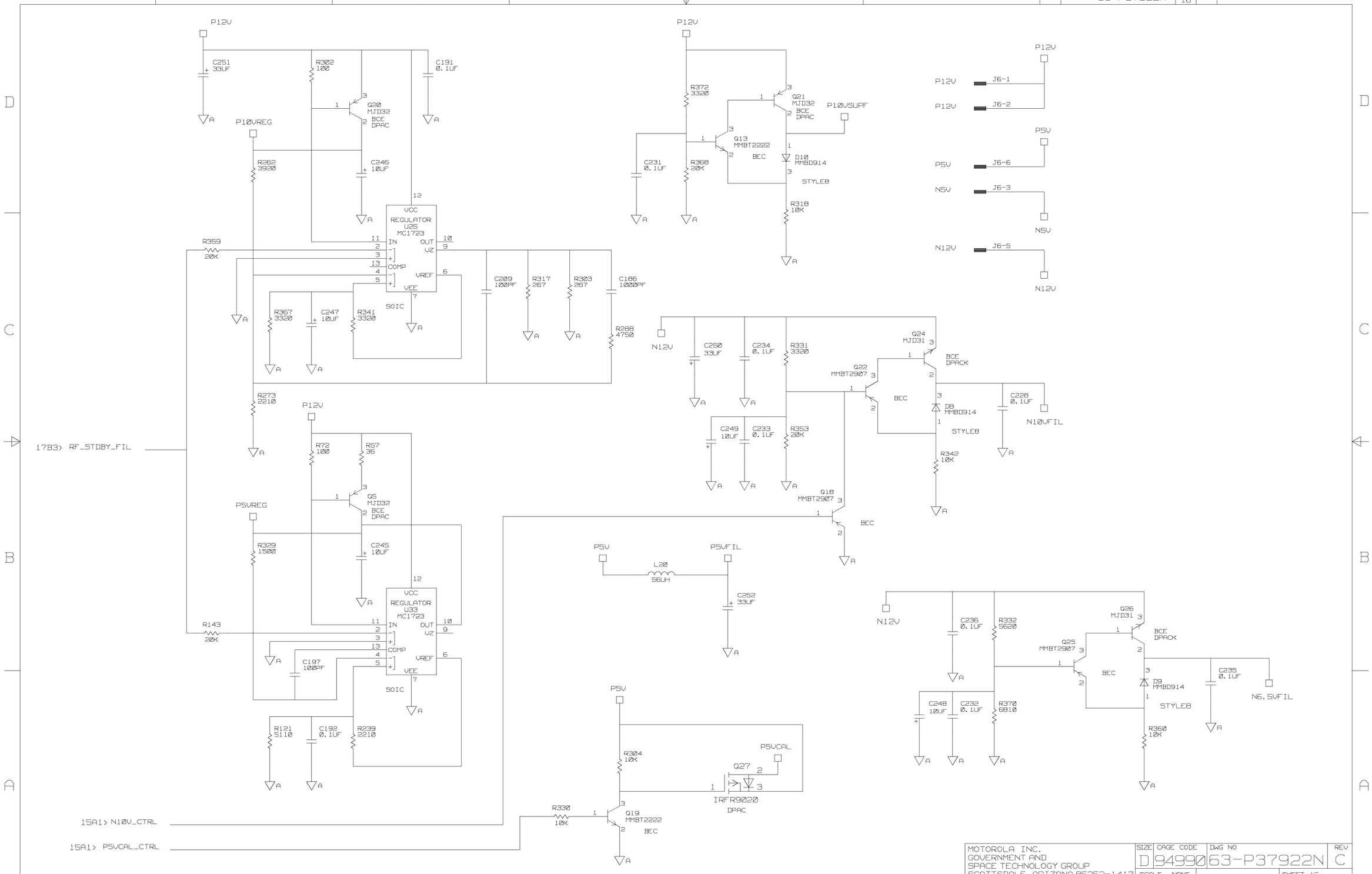
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37922N	REV C
	SCALE NONE			SHEET 13



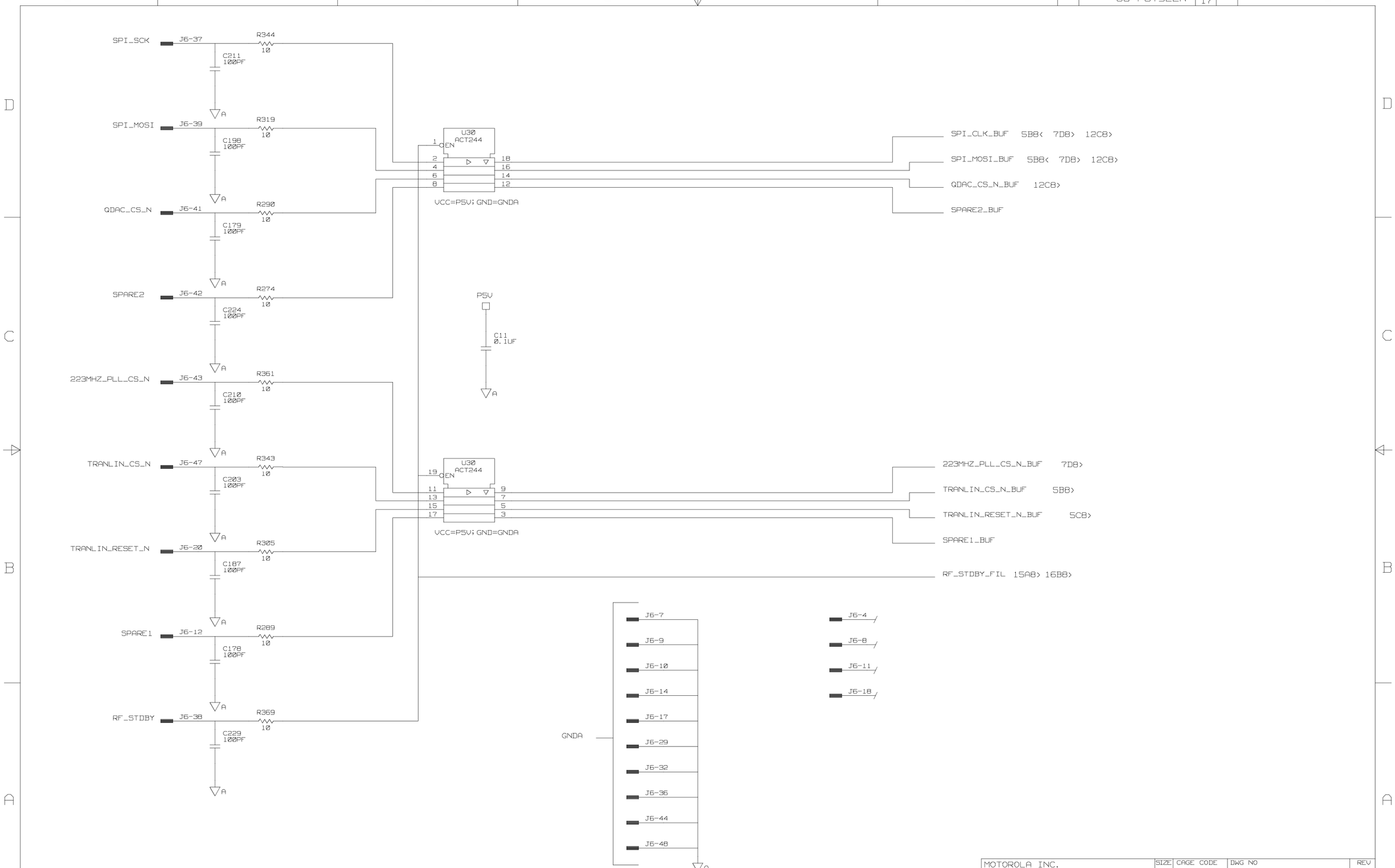
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37922N	REV C
	SCALE NONE			SHEET 14



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37922N	REV C
	SCALE NONE			SHEET 15



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37922N	REV C
	SCALE NONE		SHEET 16	



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37922N	REV C
	SCALE NONE			SHEET 17

TABLE 1 (5)

REF DES	DEVICE TYPE (6)	VCC CONNECTION		GND CONNECTION	NO CONNECTION	LOCATION (SHEET/ZONE)
		CONN	VOLTS			
U1	AC04	14	P5V	7		3A4, 3A7, 3C6, 15A7, 15B7
U2	AC08	14	P5VFILA	7		4C2, 4C3
U4	AD822	8 4	P10VREG N10VFIL			13A5, 13B5
U5	DG211	4 12 13	DG211-4 P5V P12V	5		15A6, 15B6
U6	AD822	8 4	P10VREG N10VFIL			13A7, 13C7
U8	AD822	8 4	P10VREG N10VFIL			9B7, 9D7
U9	AD822	8	P10VREG	4		5B2
U10	AD822	8 4	P10VREG N10VFIL			8B4, 8C6
U12	AD822	8	P10VREG	4		5A2, 5B2
U14	NE602	8	P5VFILB	3	7	4A6
U15	504PF	2	504PF-2	5		7A6
U16	TL072	4 8	N10VFIL P10VREG			7C3
U17	DG211	4 12 13	N12V P5V P12V	5		3C7, 3D7
U18	AD822	8 4	P10VREG N10VFIL			11C3, 11C5
U19	AD822	8 4	P10VREG N10VFIL			12C2
U20	DG409	3 14	DG409-3 DG409-14	15		10C5
U21	AD822	8 4	P10VREG N10VFIL			11C7, 11D7
U22	DG409	3 14	DG409-3 DG409-14	15		10A5
U23	AD822	8 4	P10VREG N10VFIL			13C5, 13D5
U24	AD822	8 4	P10VREG N10VFIL			11B3, 11C3
U25	MC1723				1, 8, 14	16C6
U26	MC34072	8 4	P10VREG N10VFIL			2B6, 12A4
U27	MC34072	8 4	P10VREG N10VFIL			2A4, 2B4

TABLE 1 (5)

REF DES	DEVICE TYPE (6)	VCC CONNECTION		GND CONNECTION	NO CONNECTION	LOCATION (SHEET/ZONE)
		CONN	VOLTS			
U28	MX584					12A6
U30	ACT244	20	P5V	10		17B6, 17D6
U31	RMS				2, 3, 6	14D2
U32	ABACUS				E5, E7, E9, E11, E13, G5, G7, G9, G11, G13, J7, J9, J11, L5, L7, L9, L11, L13, N5, N7, N9, N11, N13	4D6
U33	MC1723				1, 8, 14	16A6
U35	MC12019	7	MC12019-7	4	2, 8	6B4
U36	SW239			2, 7, 8		15C3
U37	SW239			2, 7, 8		15C6
U38	MAX509	3 8 18	N5VAMP DGND P5VREG	6	3, 14	12C5
U39	SW239			2, 7, 8		15D6
U40	10260				5, 6, 7, 8	2C4
U41	MC12009	1 16	MC12009-1 MC12009-16	8	6	14C6
U43	MC145158	5	MC145158-5	8	1, 6, 11, 16	7D6
U44	TRANLIN					5C5
U45	HPMX-2001	2, 3	P5VREG	14, 15	7	13C3

CAD MAINTAINED. CHANGES SHALL BE INCORPORATED BY THE DESIGN ACTIVITY

REVISION HISTORY

REV	DESCRIPTION	DATE	APPROVED
-	INITIAL RELEASE	94-05-09	
A	SEE CO E36187-3 VAH 95-10-17	95-10-19	JIM K.
B	SEE CO L48715-3 LLB 00-07-19	00-07-19	A. GATTO

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A19A2.

2. FOR REFERENCE DRAWINGS REFER TO:
   01-P37930N ASSEMBLY
   12-P37933N TEST PROCEDURE

3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS.
   ALL CAPACITORS ARE IN UF.
   ALL INDUCTORS ARE IN UH.
   ALL VOLTAGES ARE DC.

4. TERMINATIONS CODED WITH THE SAME LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.

5. DEVICE TYPE NUMBERS AND CONNECTIONS NOT SHOWN ON SYMBOL ARE LISTED IN TABLE 1.

6. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH MANUFACTURER. SEE ASSEMBLY PARTS LIST FOR PROPER PART NUMBER.

REFERENCE DESIGNATIONS

HIGHEST NUMBER USED	NOT USED
C260	C203, C225, C246, C247
D5	
E6	
J6	
L4	
P300	P2-P99, P101-P199,
	P201-P299
Q7	
R331	R162, R164, R177, R226,
	R265, R284, R310, E315,
	R318, R320
S1	
U109	U49, U78, U88, U104,
	U106
Y3	

ALL SHEETS ARE THE SAME REVISION STATUS

		CONTR
		ISS B35550-286(-)94-06-27
		APPROVALS
		DWN S. GRAHAM 93-11-17
		CHKR D. MILLER 94-06-27
		QA
		MATL K. NELSON 94-06-27
01-P37900N	COCHISE	MFG S. CASH 94-06-27
NEXT ASSY	USED ON	ENG A. KOESTNER 94-06-27
APPLICATION		CUST

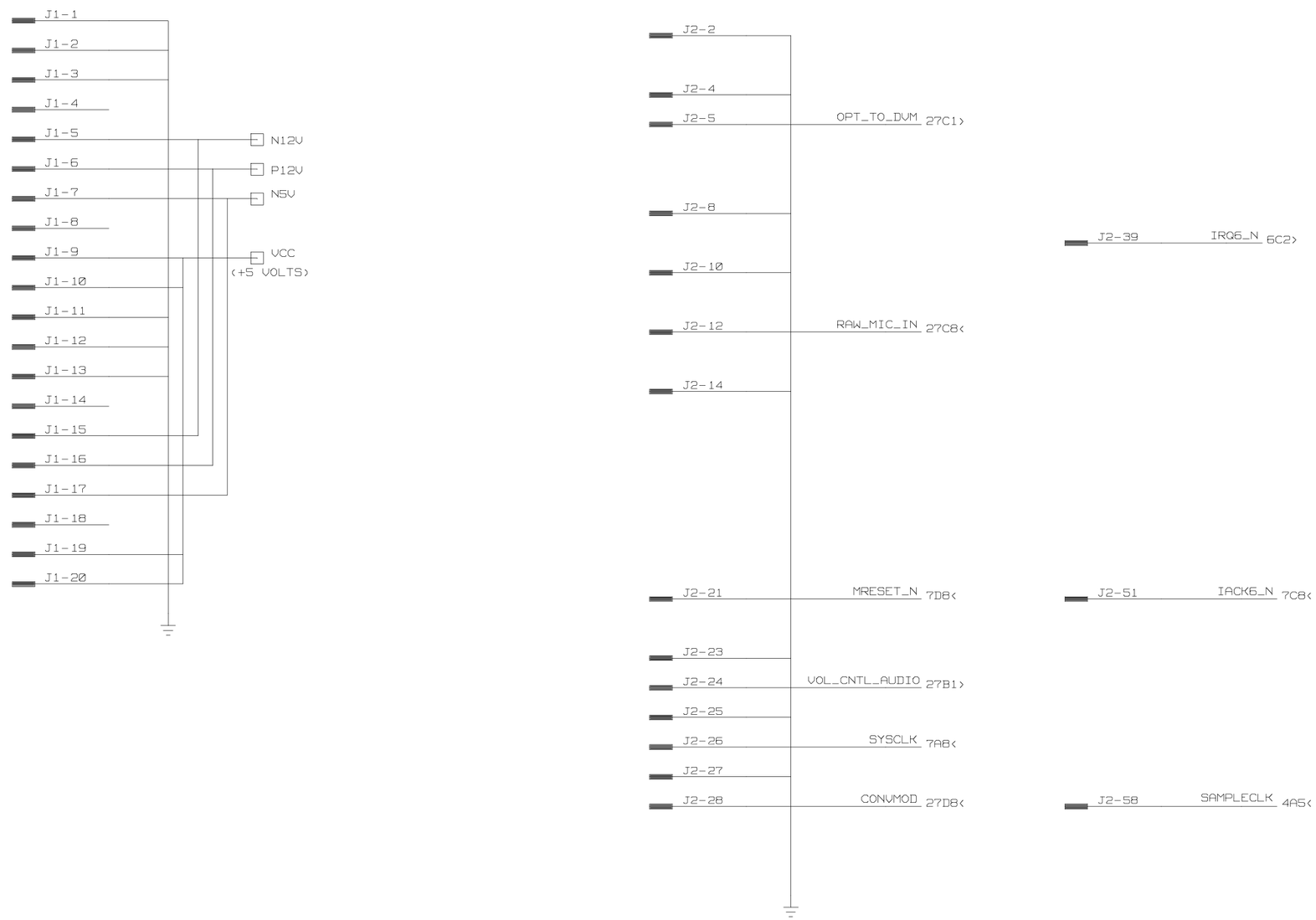
MOTOROLA INC.
GOVERNMENT AND SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417

TITLE

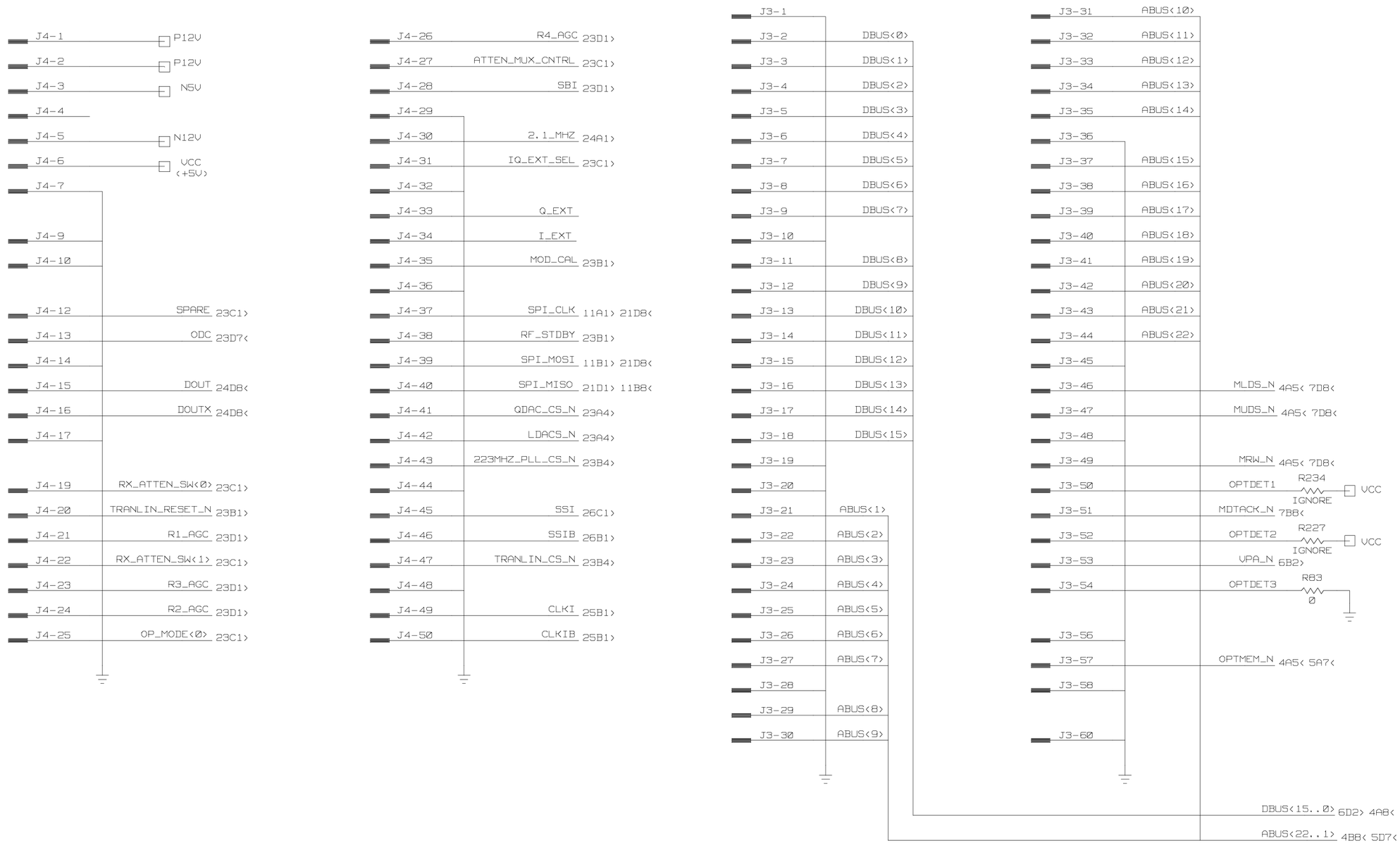
SCHEMATIC DIAGRAM
COCHISE iDEN

SIZE	CAGE CODE	DWG NO
D	94990	63-P37932N

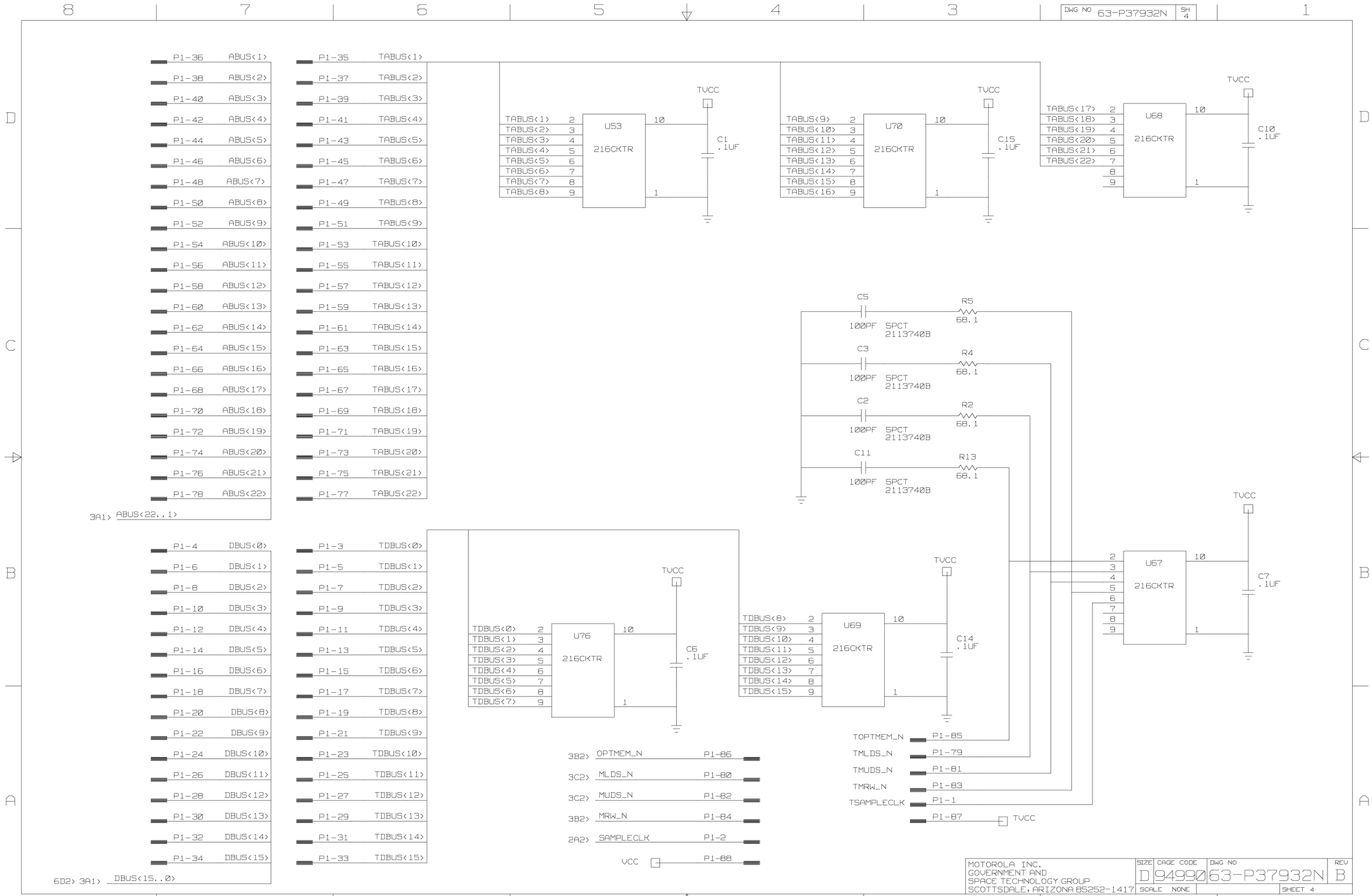
SCALE NONE



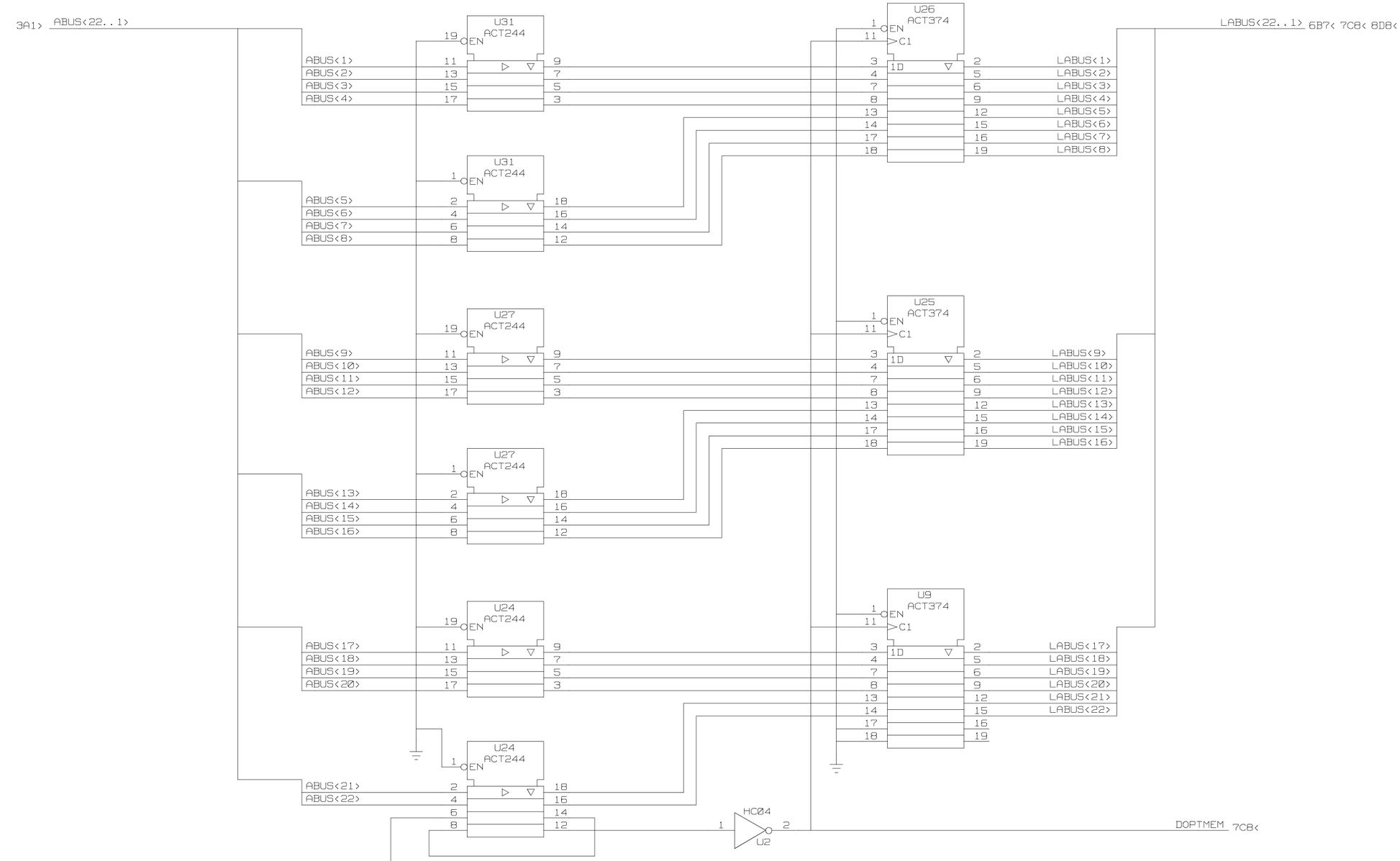
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 2	



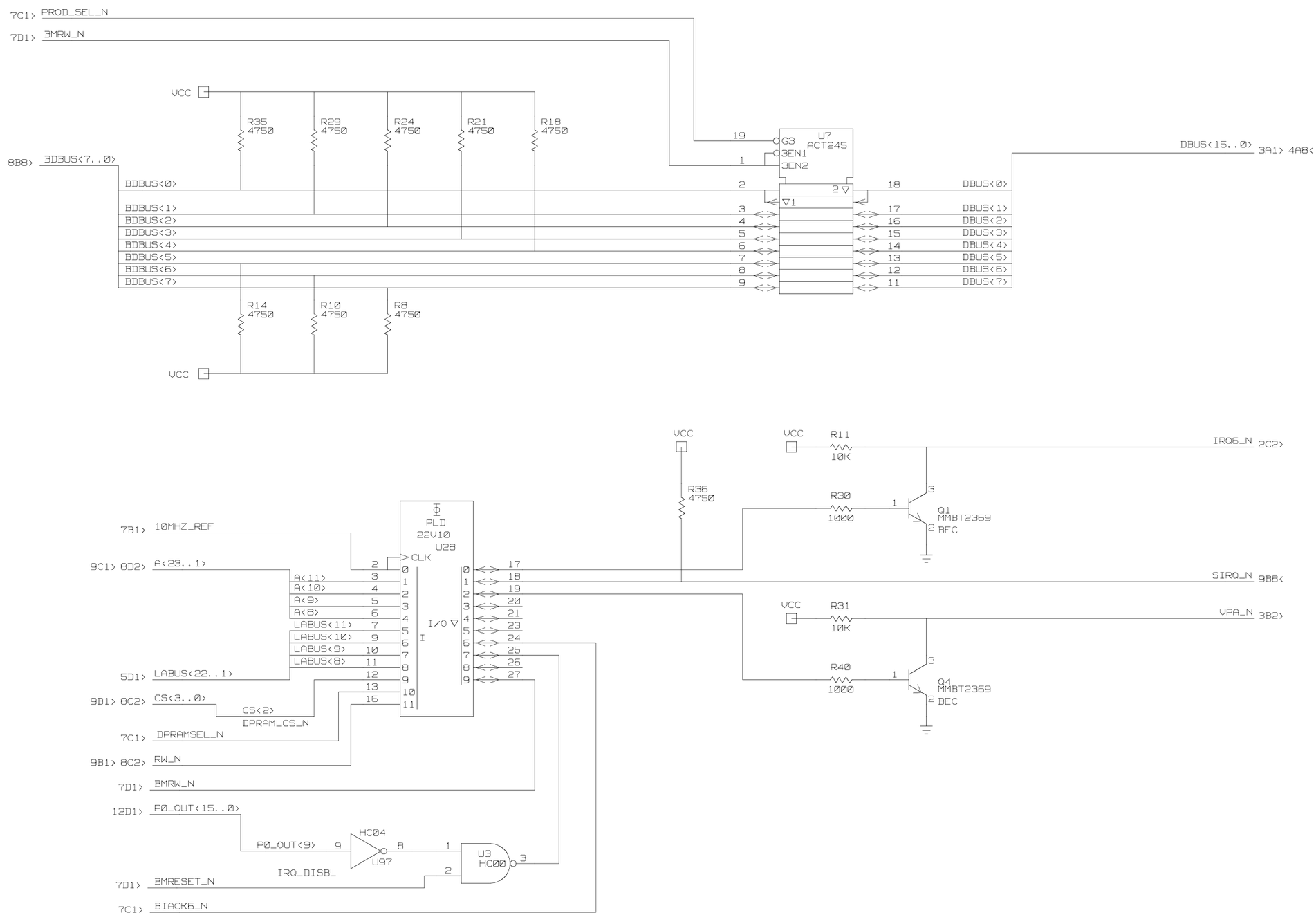
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 3	



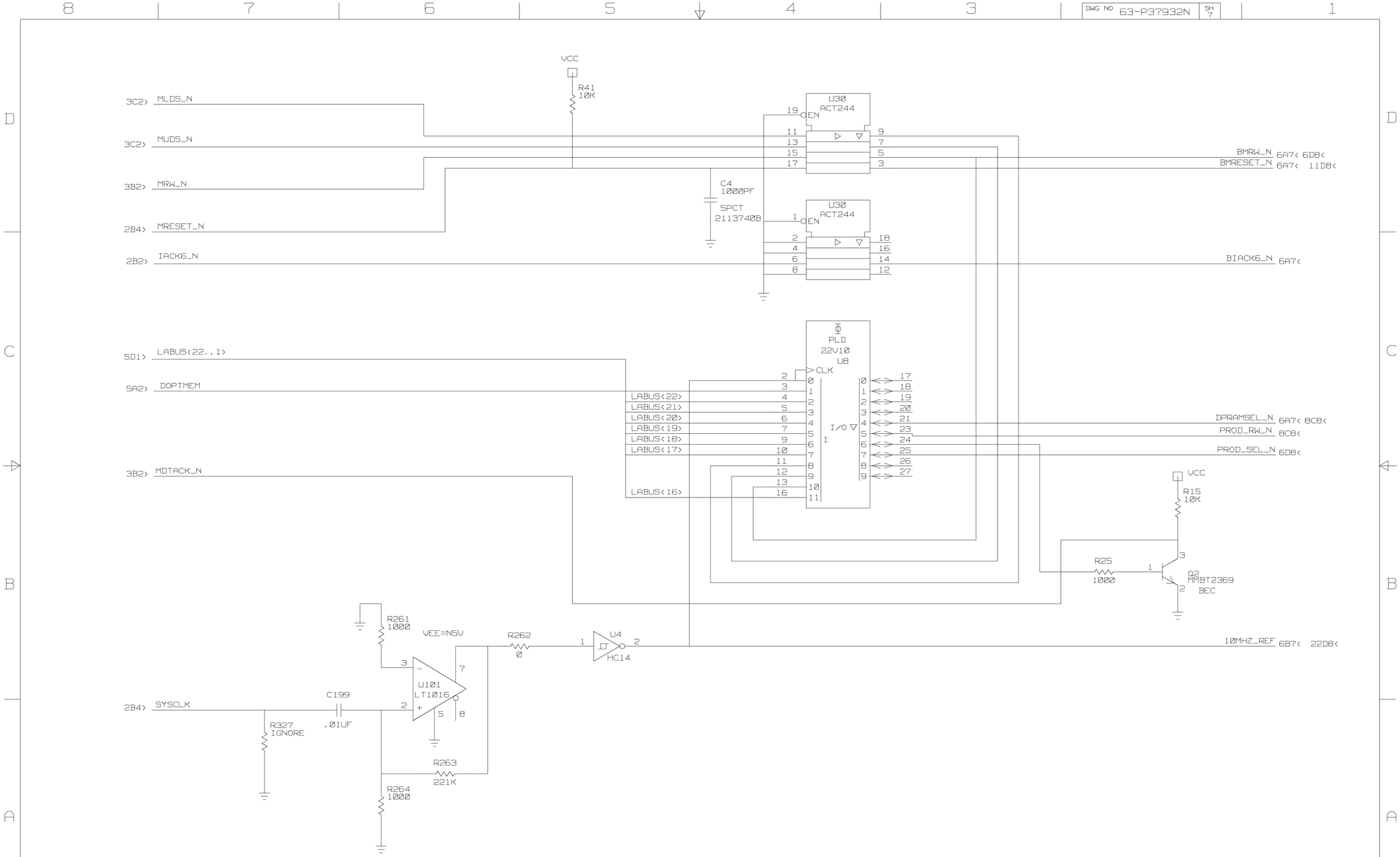
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE			SHEET 4



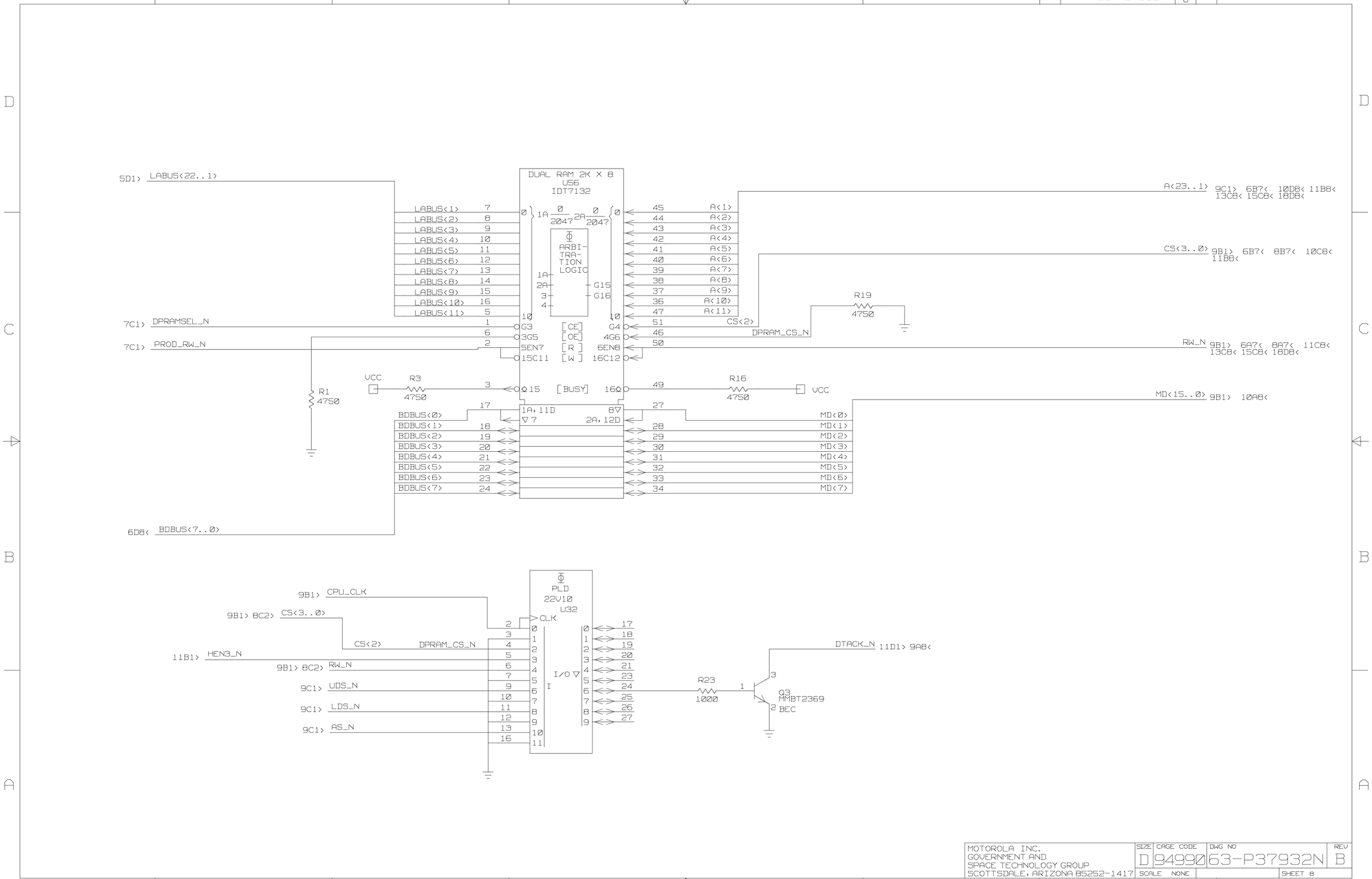
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 5	



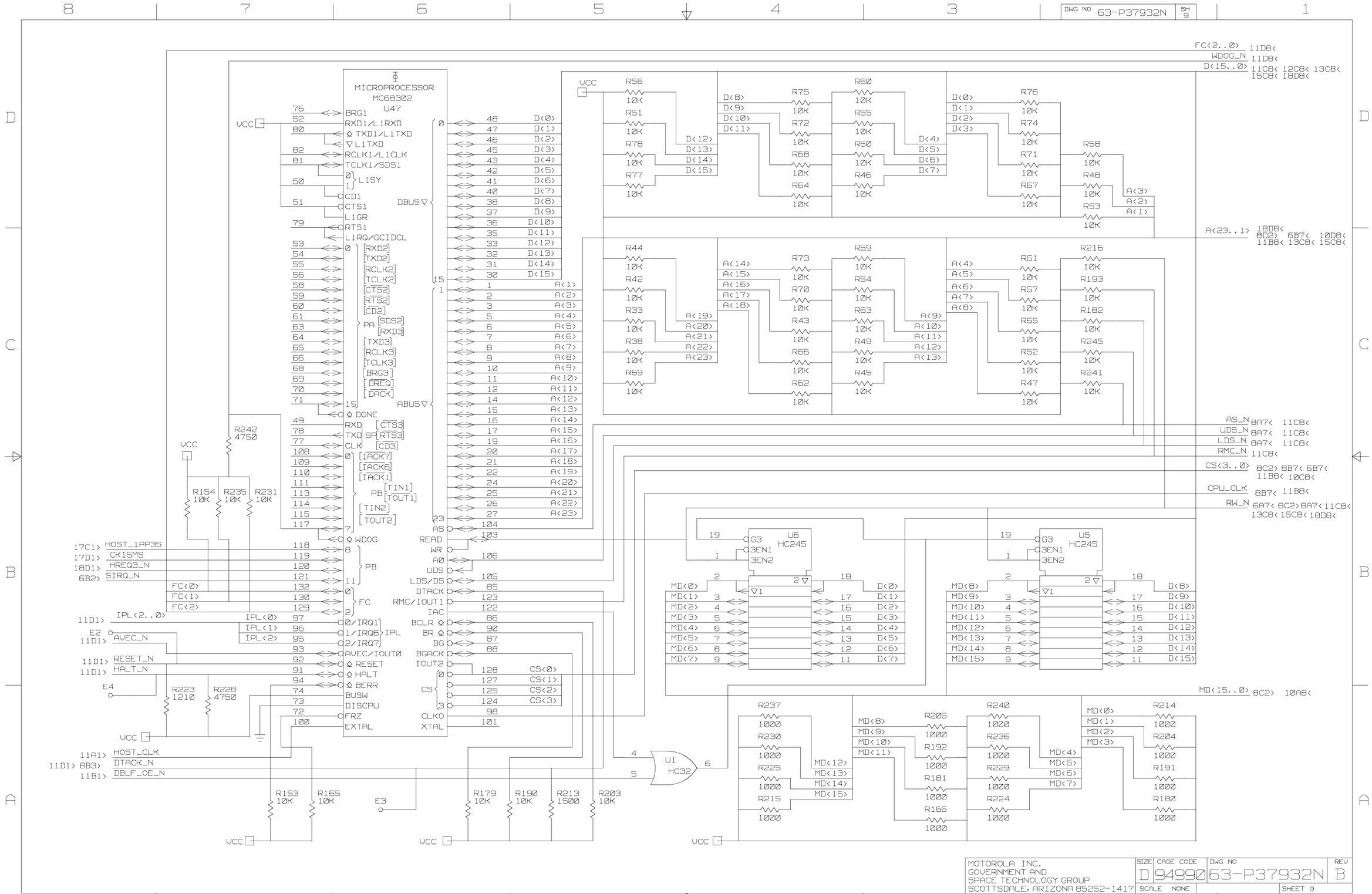
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE			SHEET 6



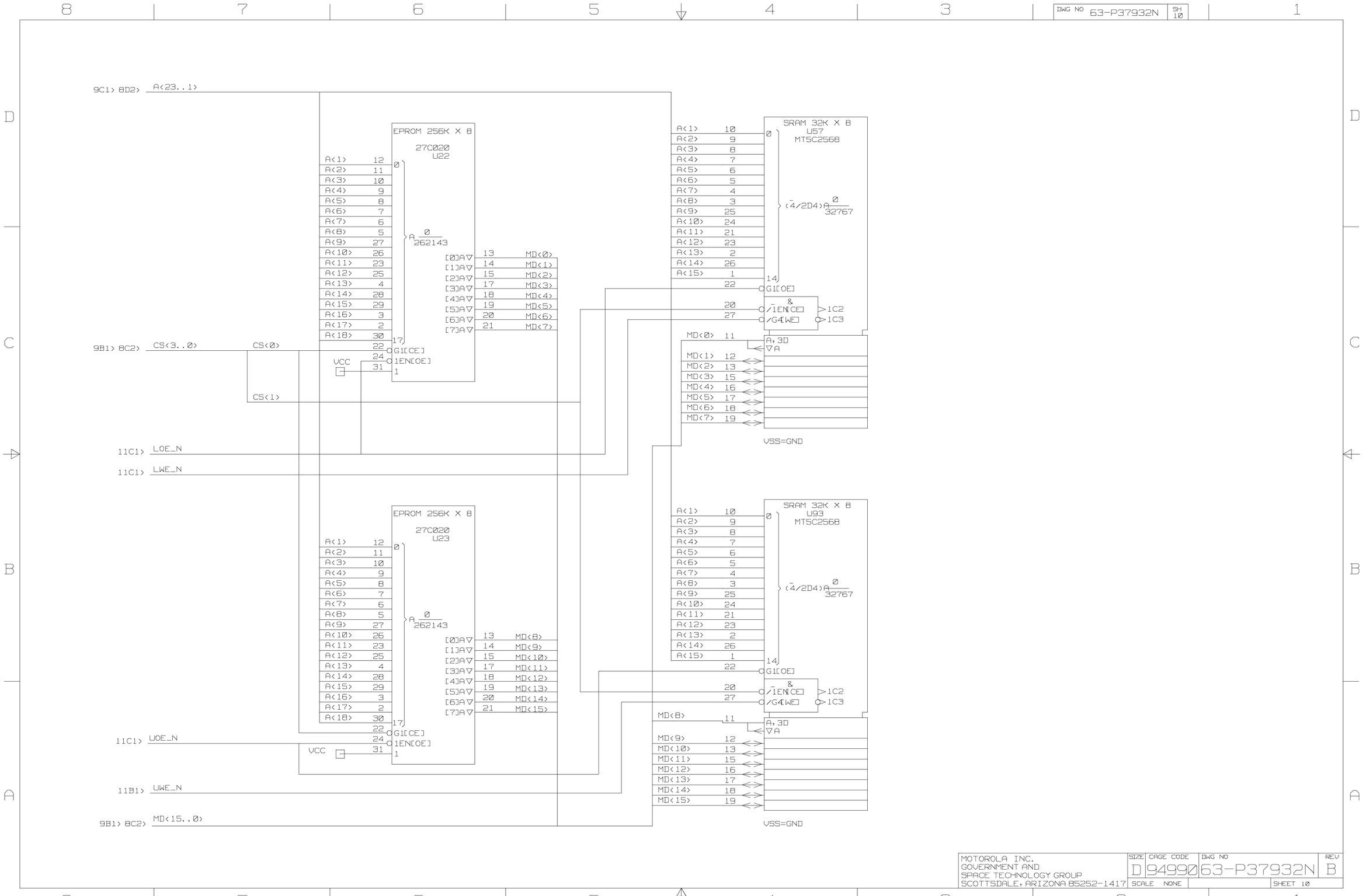
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 7	



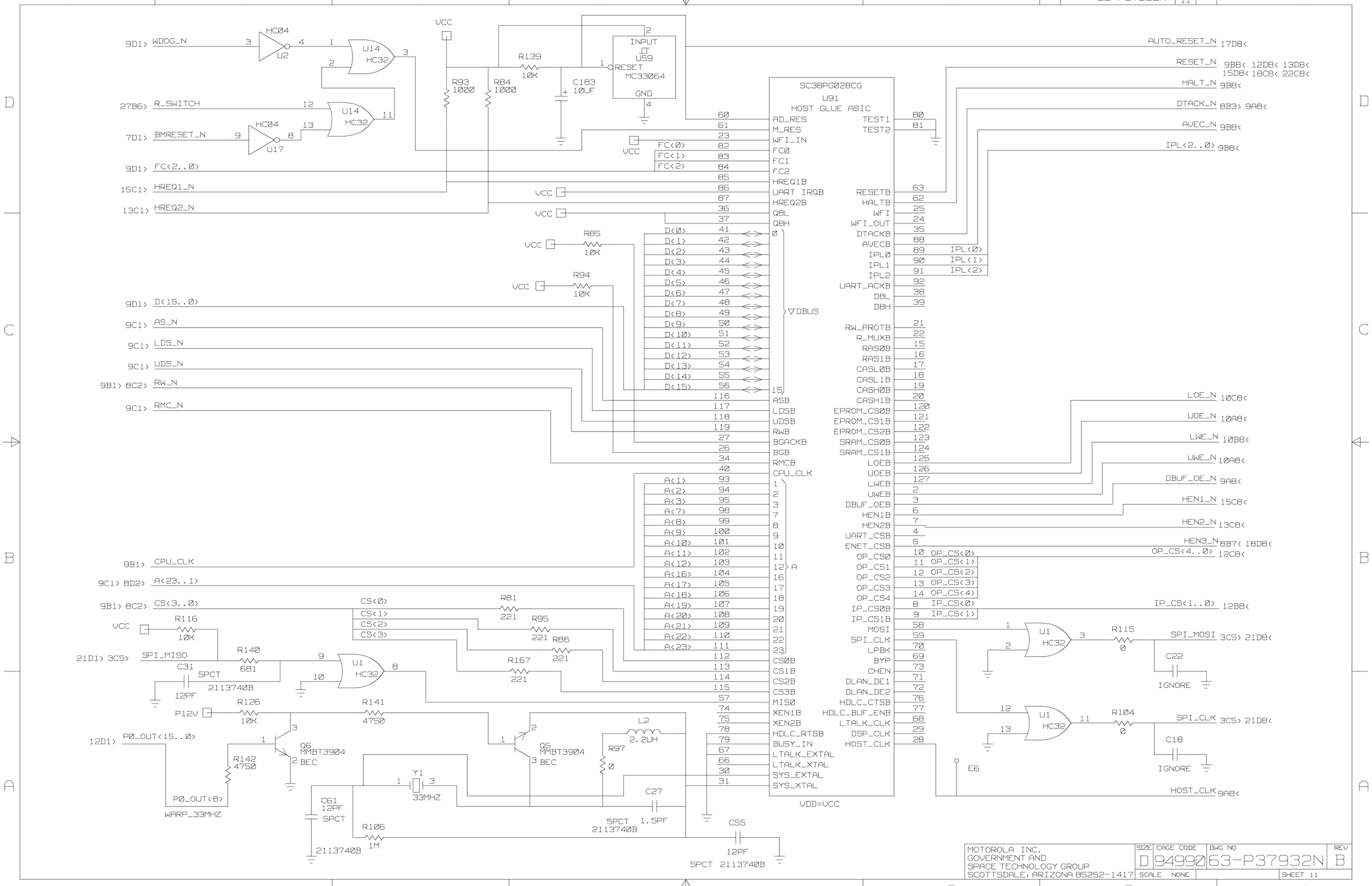
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 8	

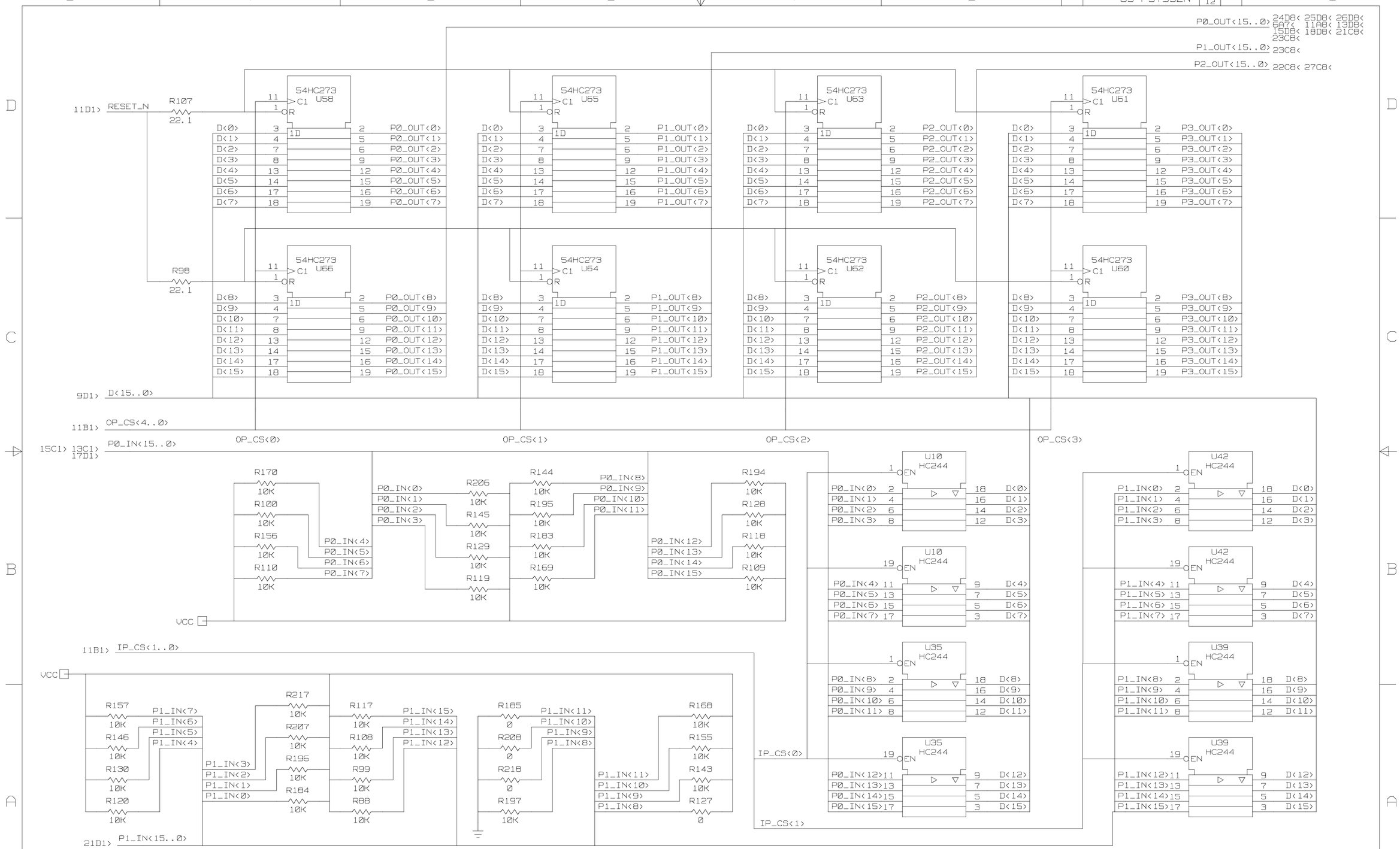


MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 9	

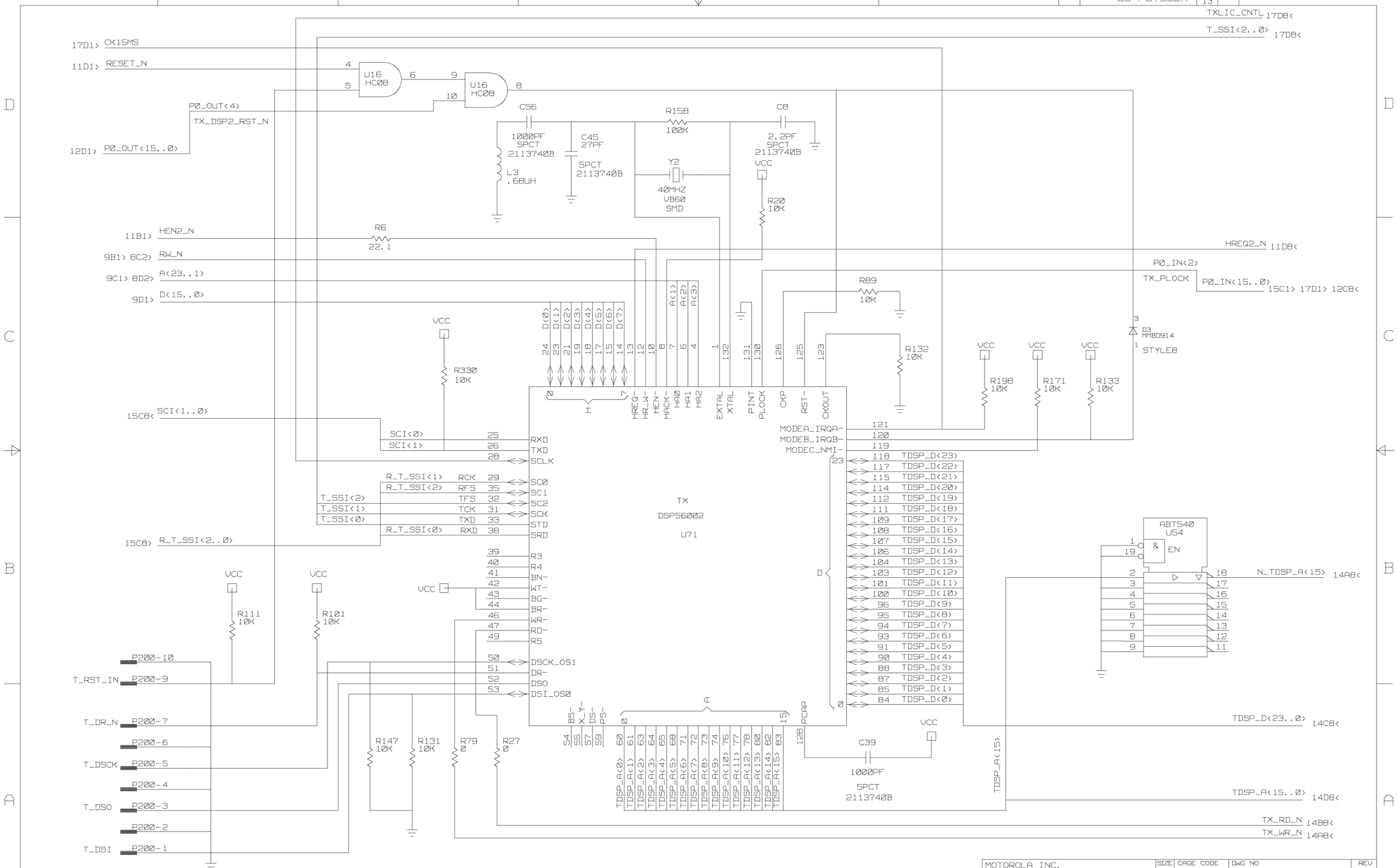


MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE			SHEET 10

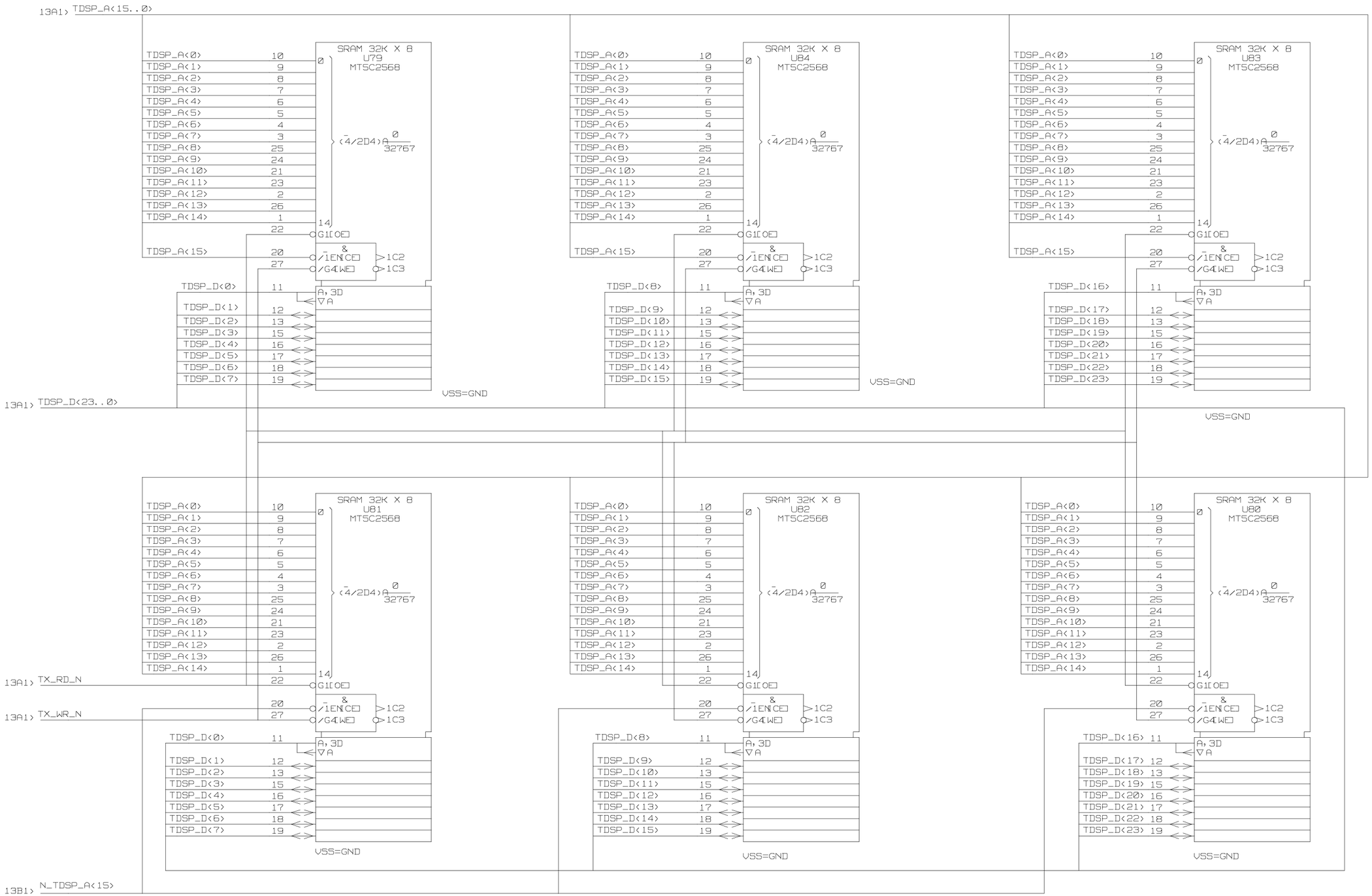

DWG NO 63-P37932N SH 11
SC38PG028CG
U91
HOST GLUE ASIC
VDD=VCC
U14 HC32
HC04 U2
HC04 U17
INPUT U59 RESET MC33064 GND
R139 10K
R93 1000
R84 1000
C183 10UF
R85 10K
R94 10K
R116 10K
R140 681
C31 12PF 5PCT 2113740B
R126 10K
R141 4750
R142 4750
Q6 MMBT3904 BEC
Q5 MMBT3904 BEC
L2 2.2UH
R97 0
Y1 33MHZ
WARP_33MHZ
C61 12PF 5PCT 2113740B
R106 1M
C27 1.5PF 5PCT 2113740B
C55 12PF 5PCT 2113740B
R81 221
R95 221
R86 221
R167 221
U1 HC32
R115 0
C22 IGNORE
R104 0
C18 IGNORE
E6
9D1> WDOG_N
27B6> R_SWITCH
7D1> BMRESET_N
9D1> FC<2..0>
15C1> HREQ1_N
13C1> HREQ2_N
9D1> D<15..0>
9C1> AS_N
9C1> LDS_N
9C1> UDS_N
9B1> 8C2> RW_N
9C1> RMC_N
9B1> CPU_CLK
9C1> 8D2> A<23..1>
9B1> 8C2> CS<3..0>
21D1> 3C5> SPI_MISO
12D1> P0_OUT<15..0>
P0_OUT<8>
AUTO_RESET_N 17D8<
RESET_N 9B8< 12D8< 13D8< 15D8< 18C8< 22C8<
HALT_N 9B8<
DTACK_N 8B3> 9A8<
AVEC_N 9B8<
IPL<2..0> 9B8<
LOE_N 10C8<
UOE_N 10A8<
LWE_N 10B8<
UWE_N 10A8<
DBUF_OE_N 9A8<
HEN1_N 15C8<
HEN2_N 13C8<
HEN3_N 8B7< 18D8<
OP_CS<4..0> 12C8<
IP_CS<1..0> 12B8<
SPI_MOSI 3C5> 21D8<
SPI_CLK 3C5> 21D8<
HOST_CLK 9A8<
MOTOROLA INC.
GOVERNMENT AND
SPACE TECHNOLOGY GROUP
SCOTTSDALE, ARIZONA 85252-1417
SIZE D CAGE CODE 94990 DWG NO 63-P37932N REV B
SCALE NONE SHEET 11



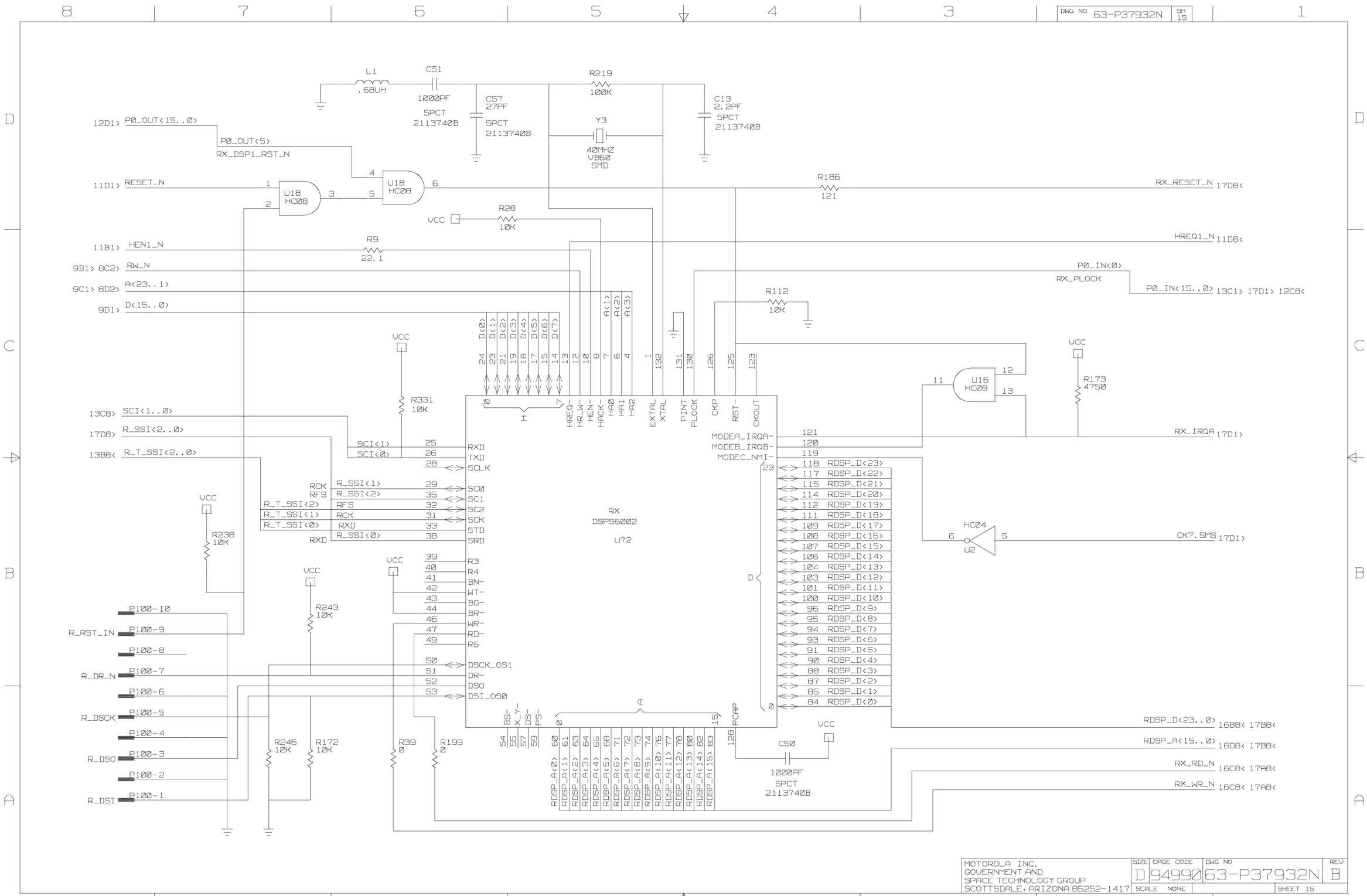
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 12	



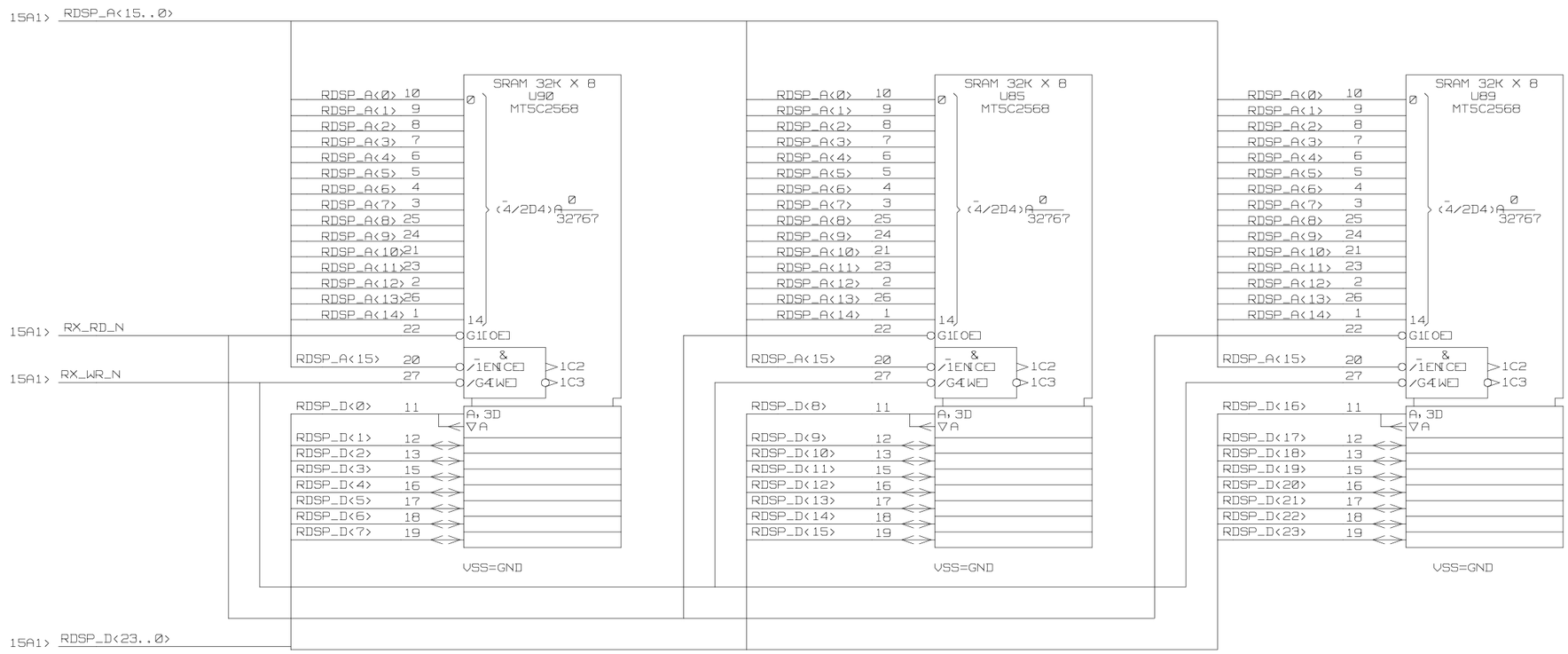
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 13	



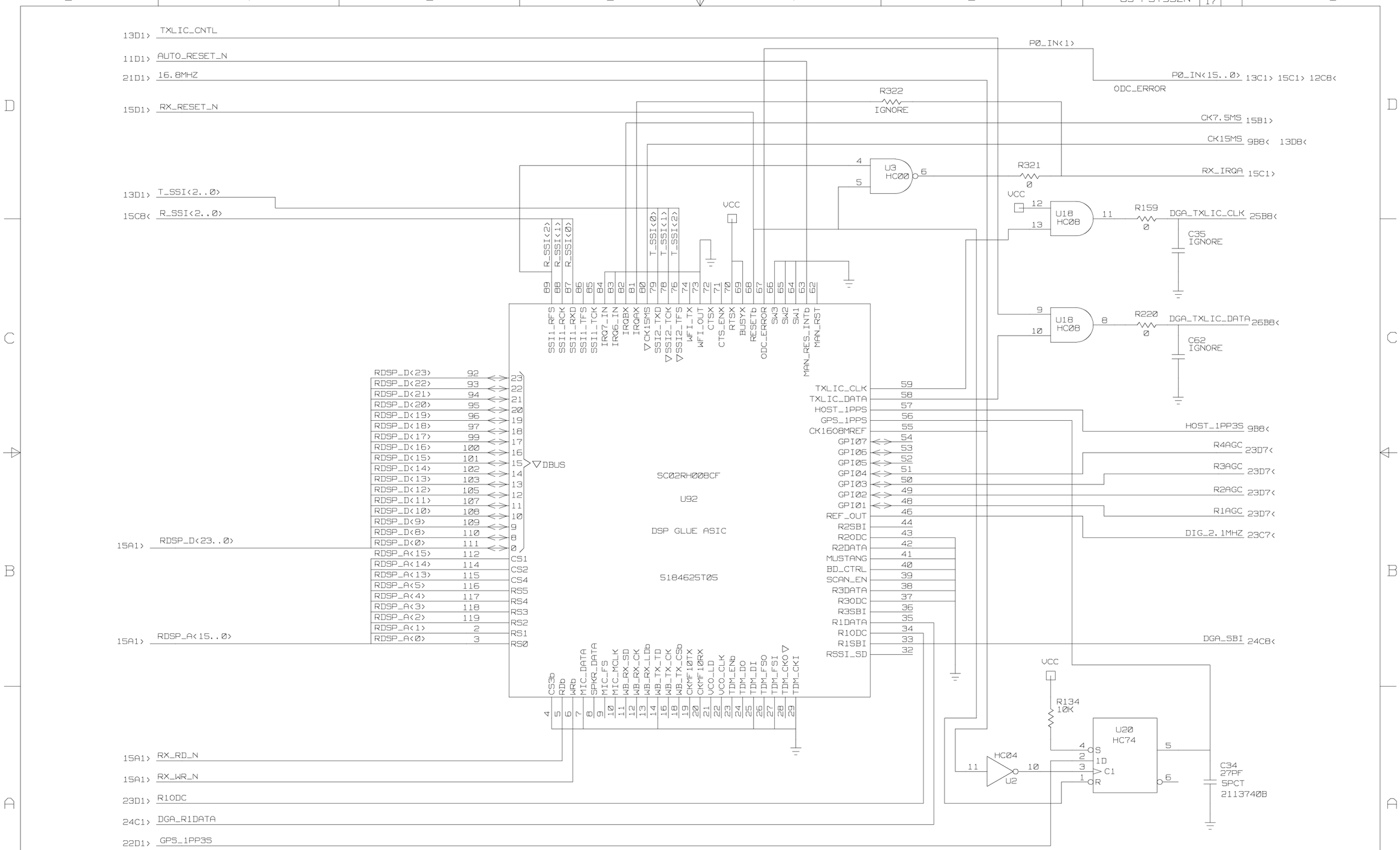
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 14	



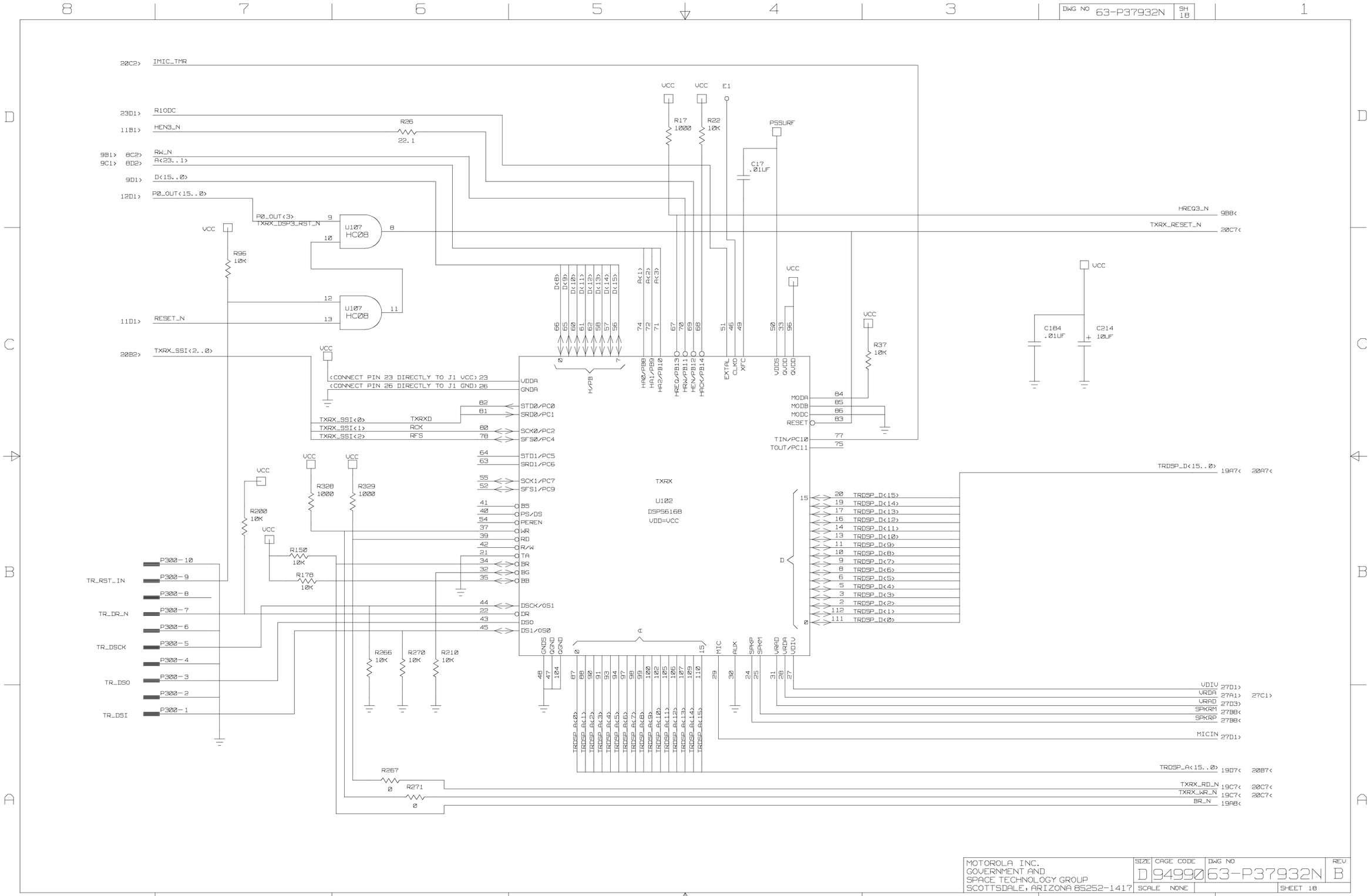
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 15	



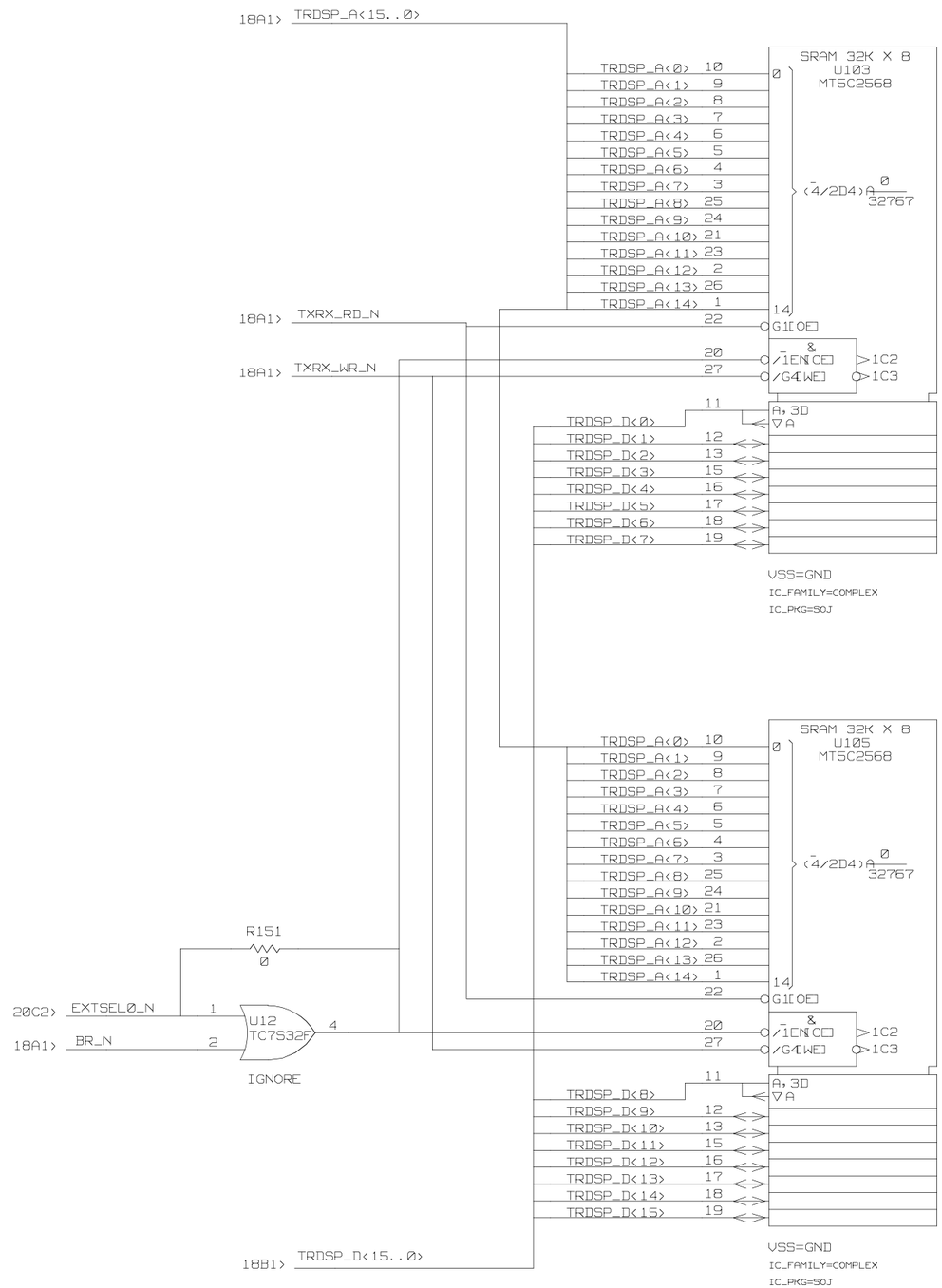
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE			SHEET 16



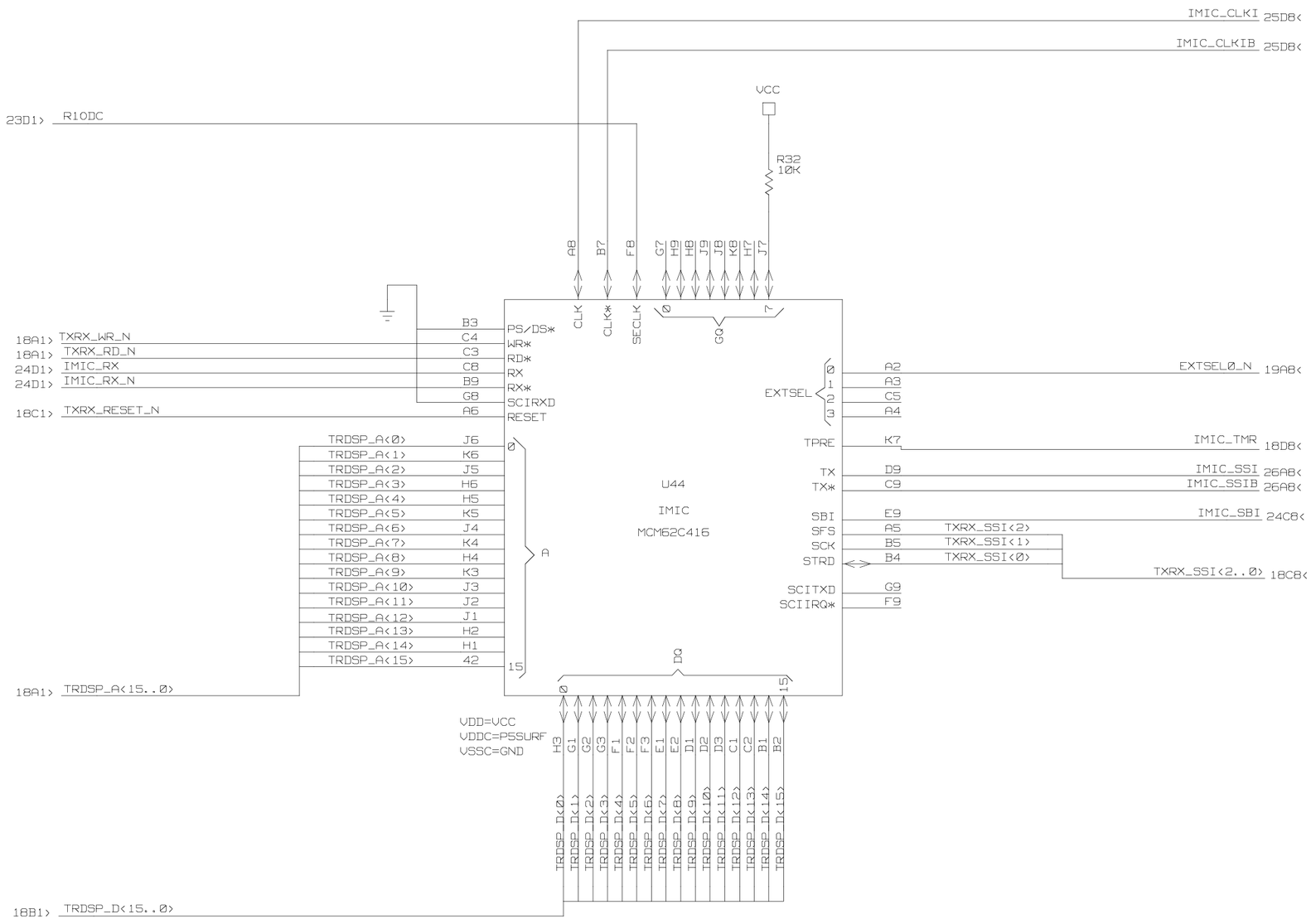
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 17	



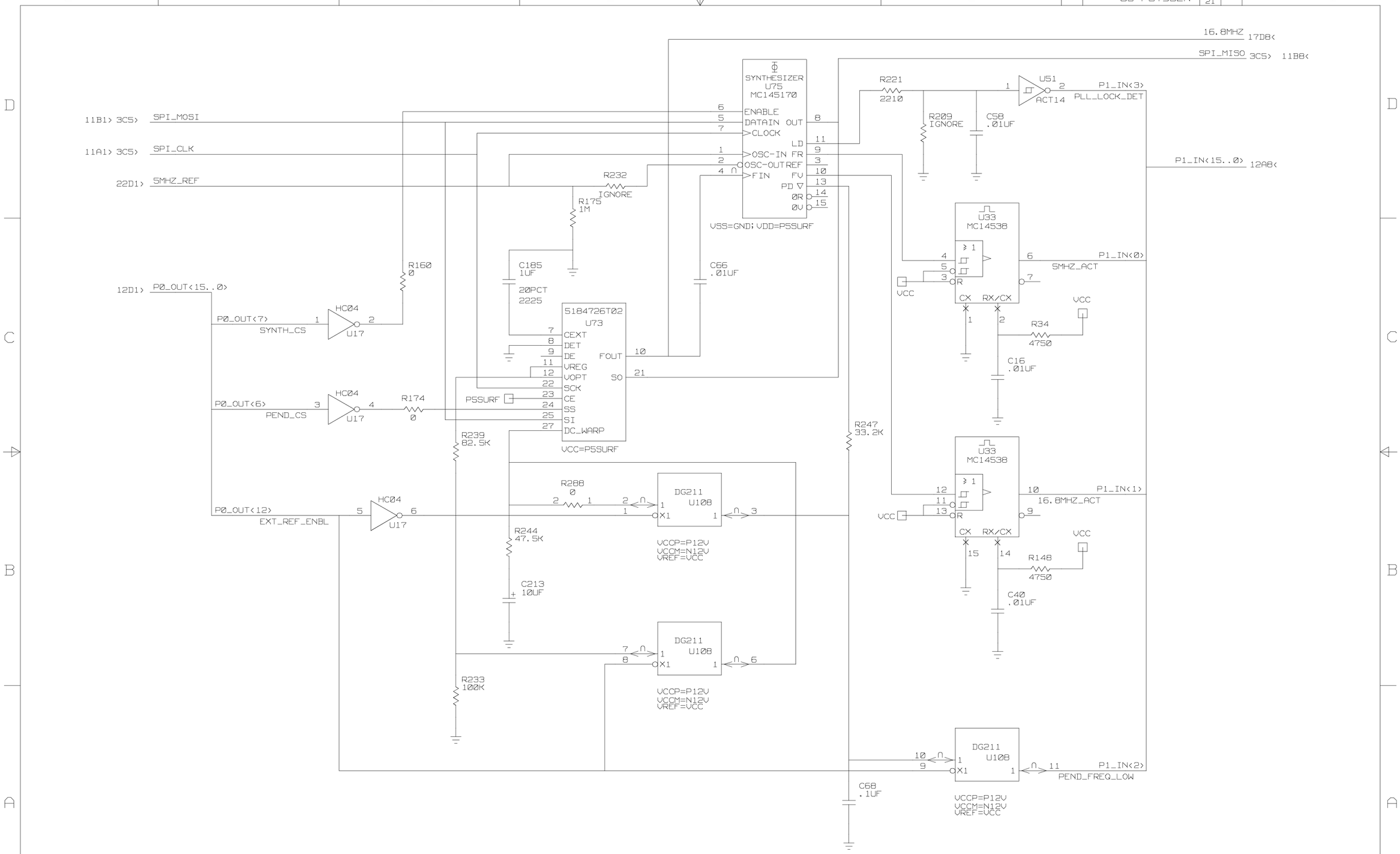
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 18	



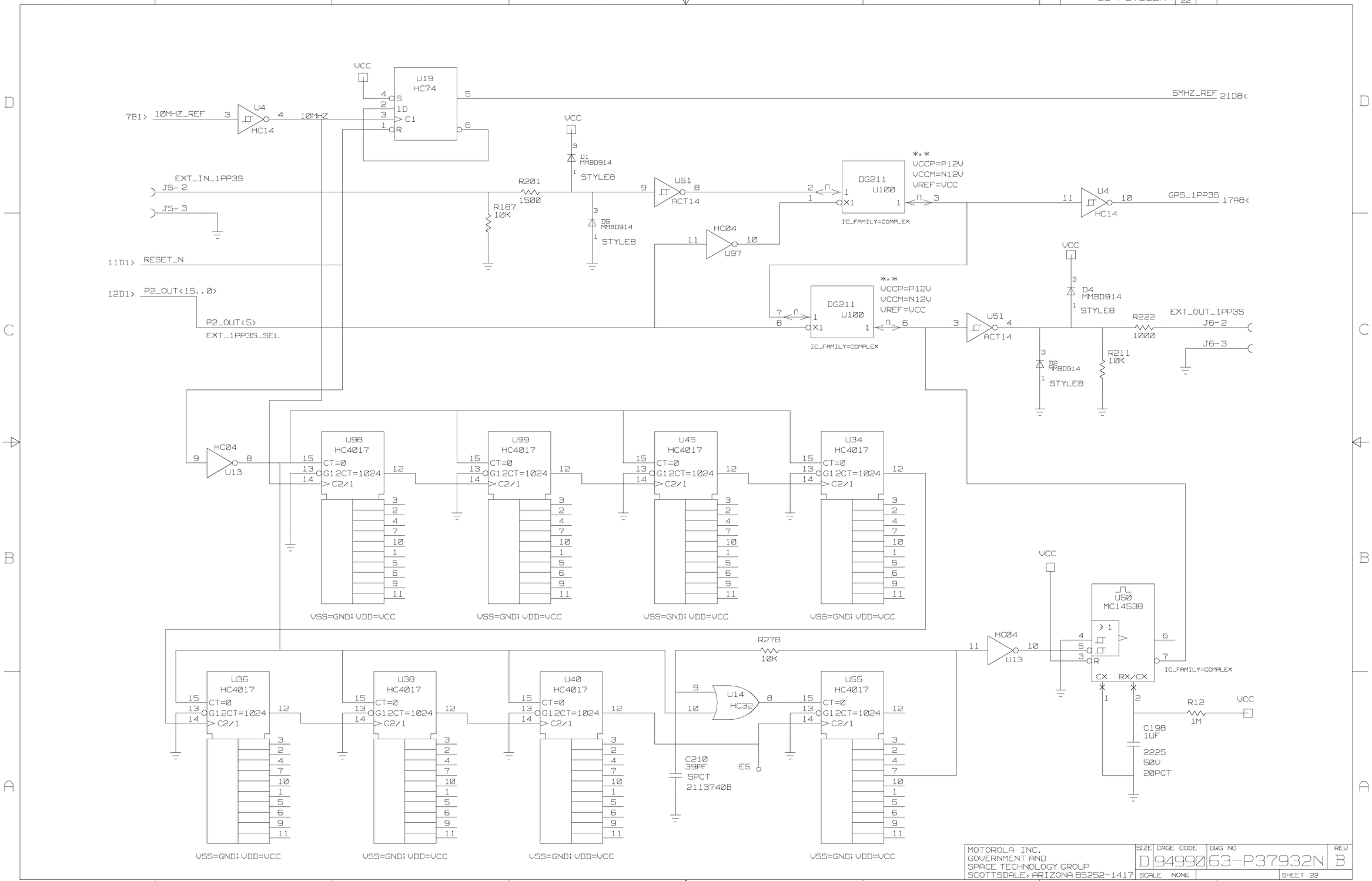
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 19	



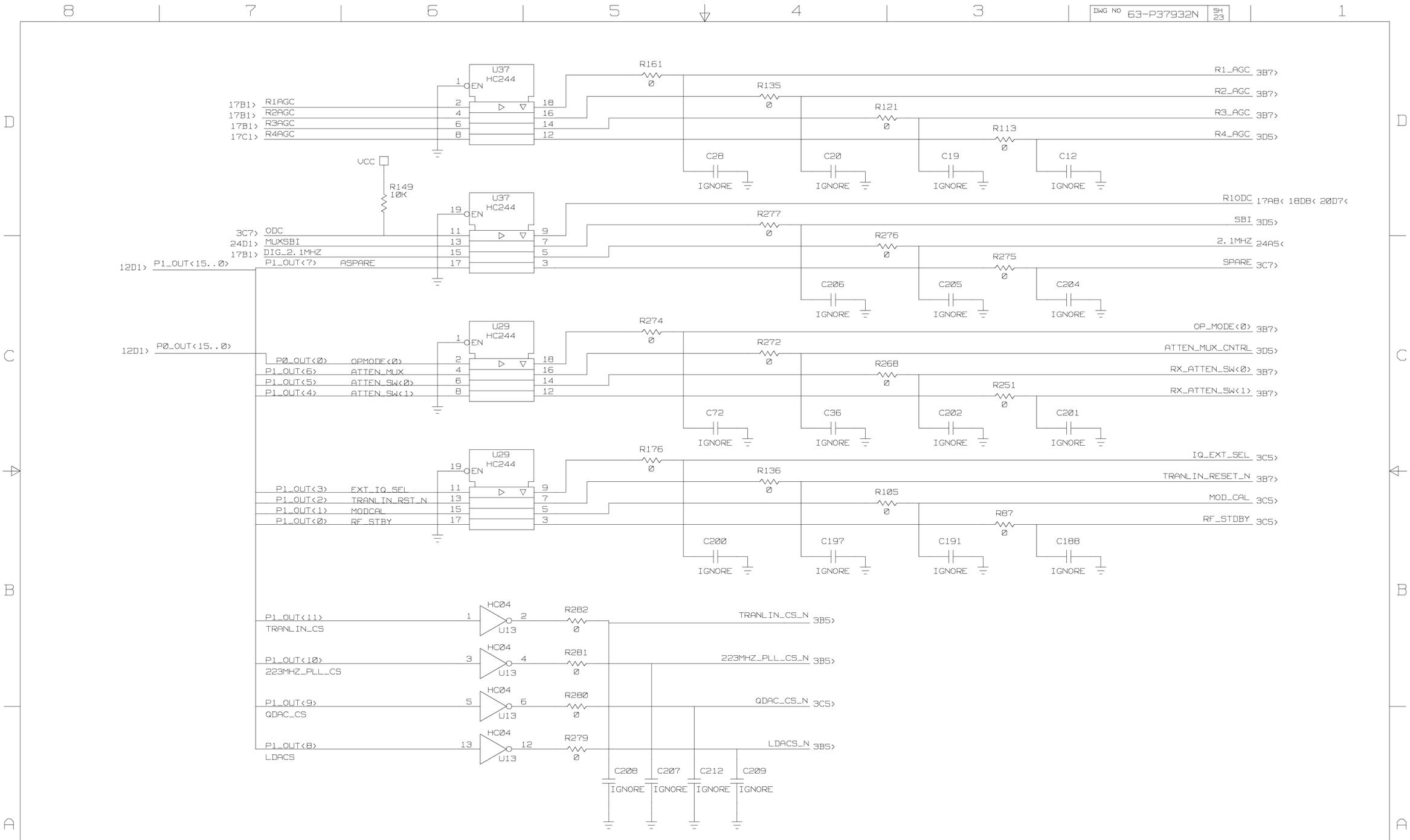
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE			SHEET 20



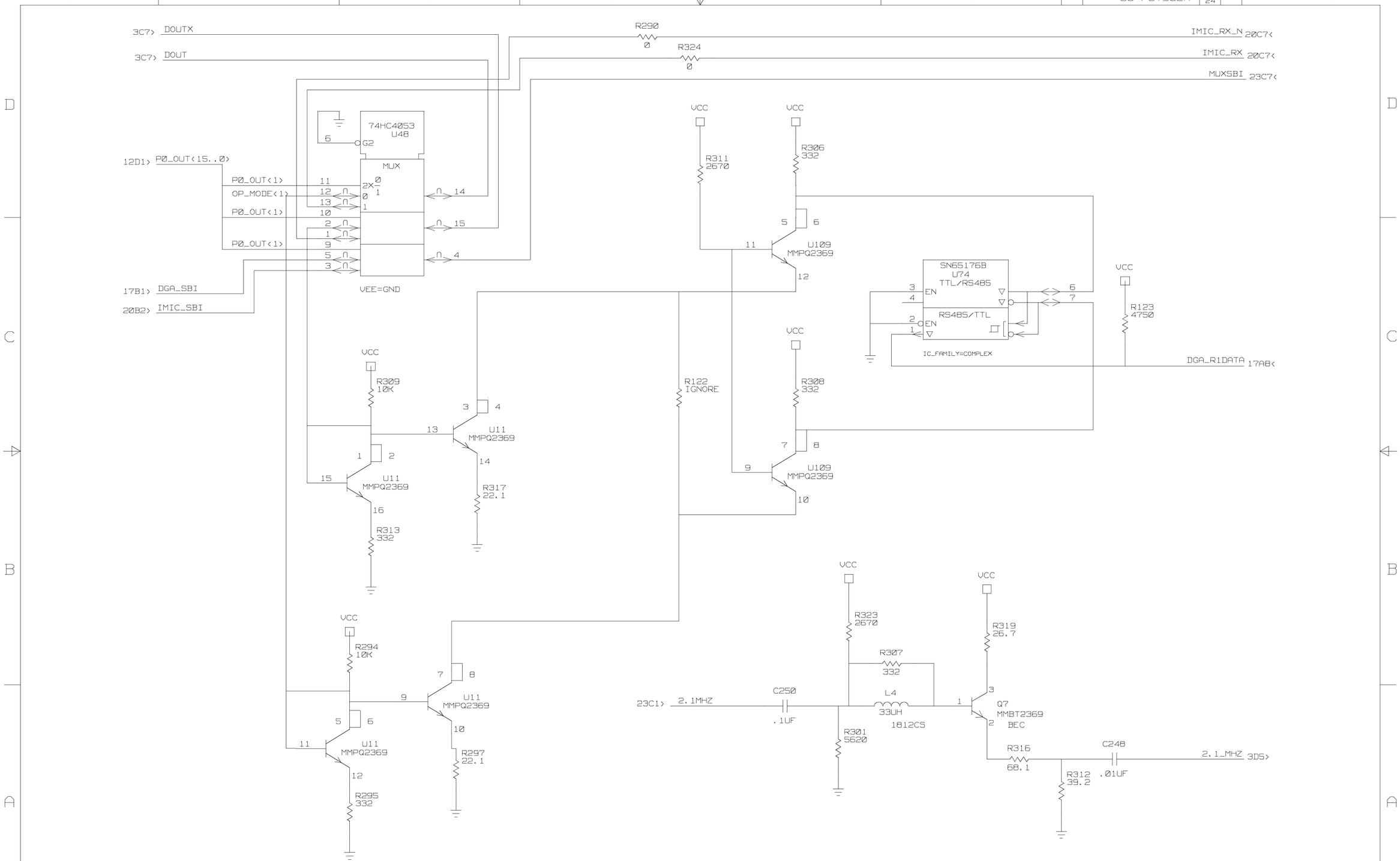
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE	CAGE CODE	DWG NO	REV
	D	94990	63-P37932N	B
	SCALE NONE		SHEET 21	



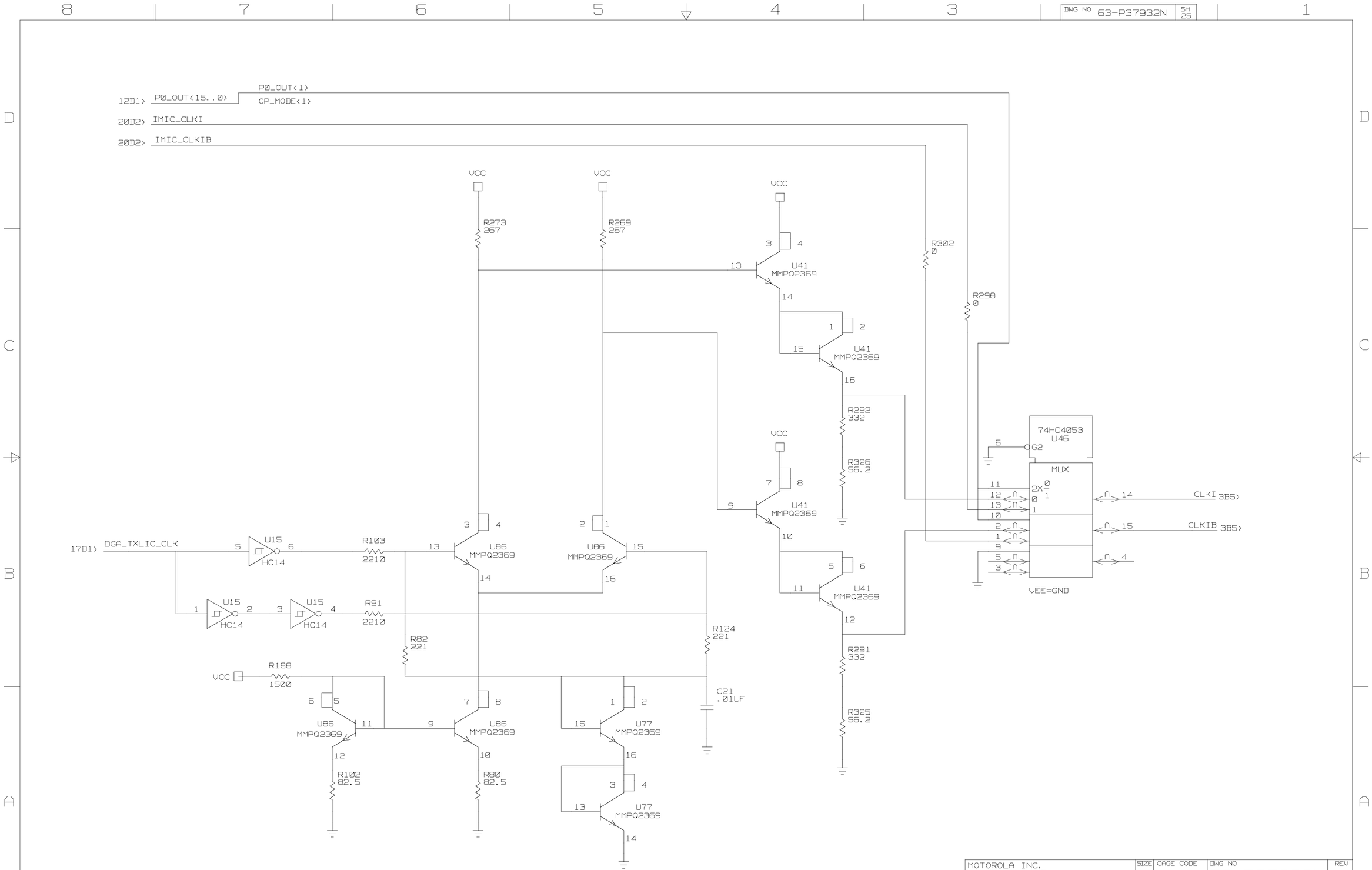
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 22	



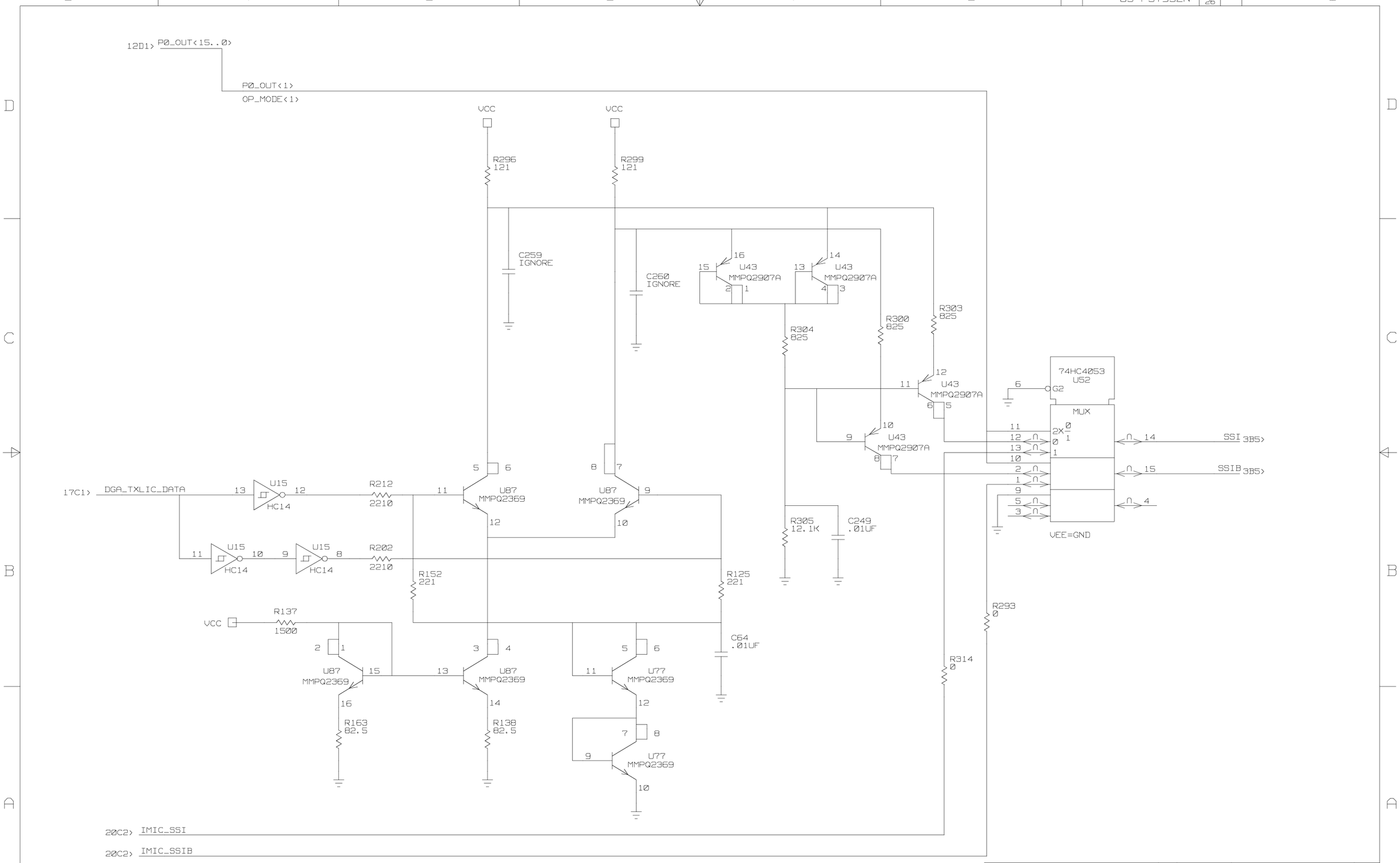
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 23	



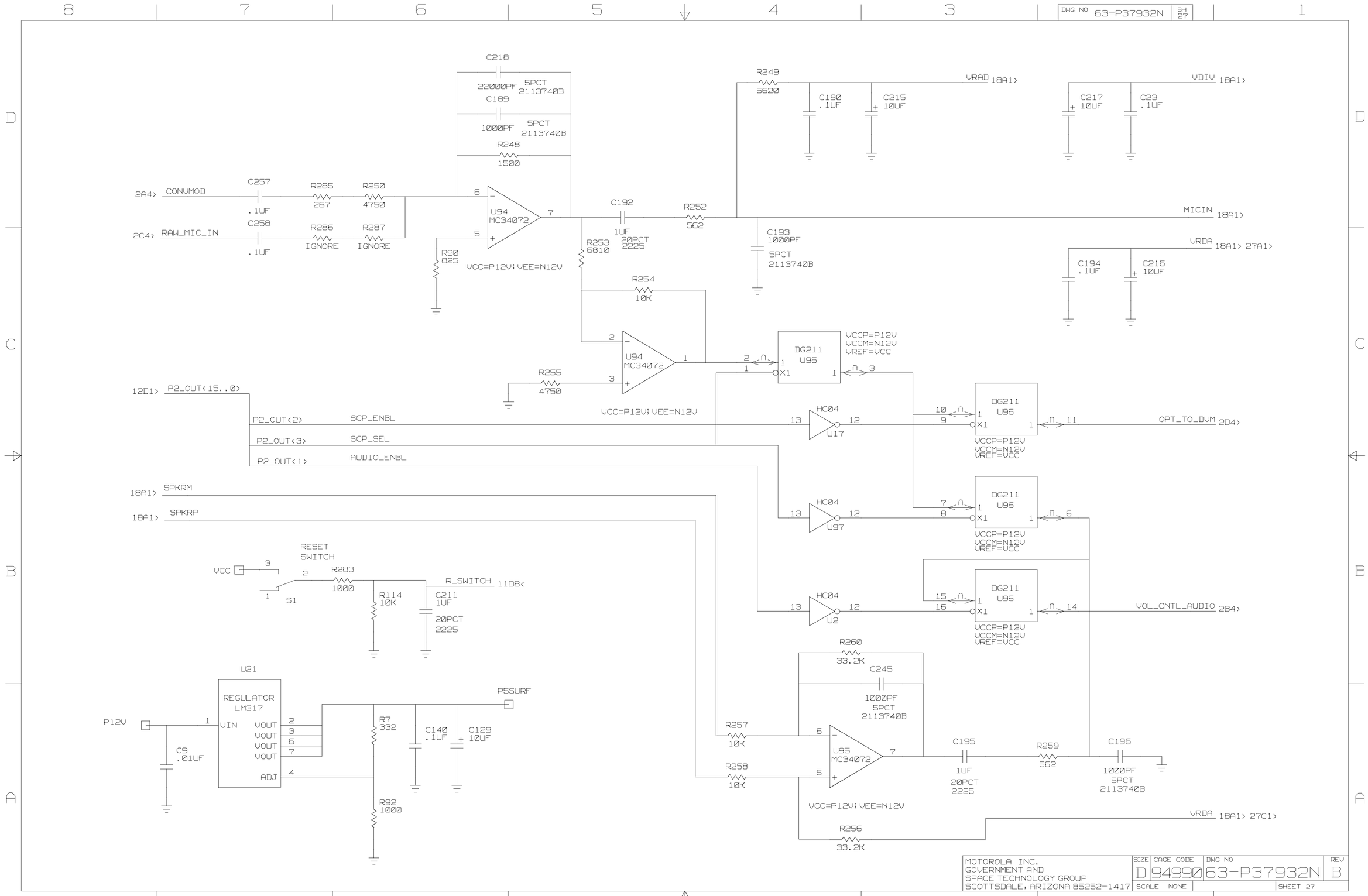
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE	CAGE CODE	DWG NO	REV
	D	94990	63-P37932N	B
	SCALE NONE		SHEET 24	



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 25	



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 26	



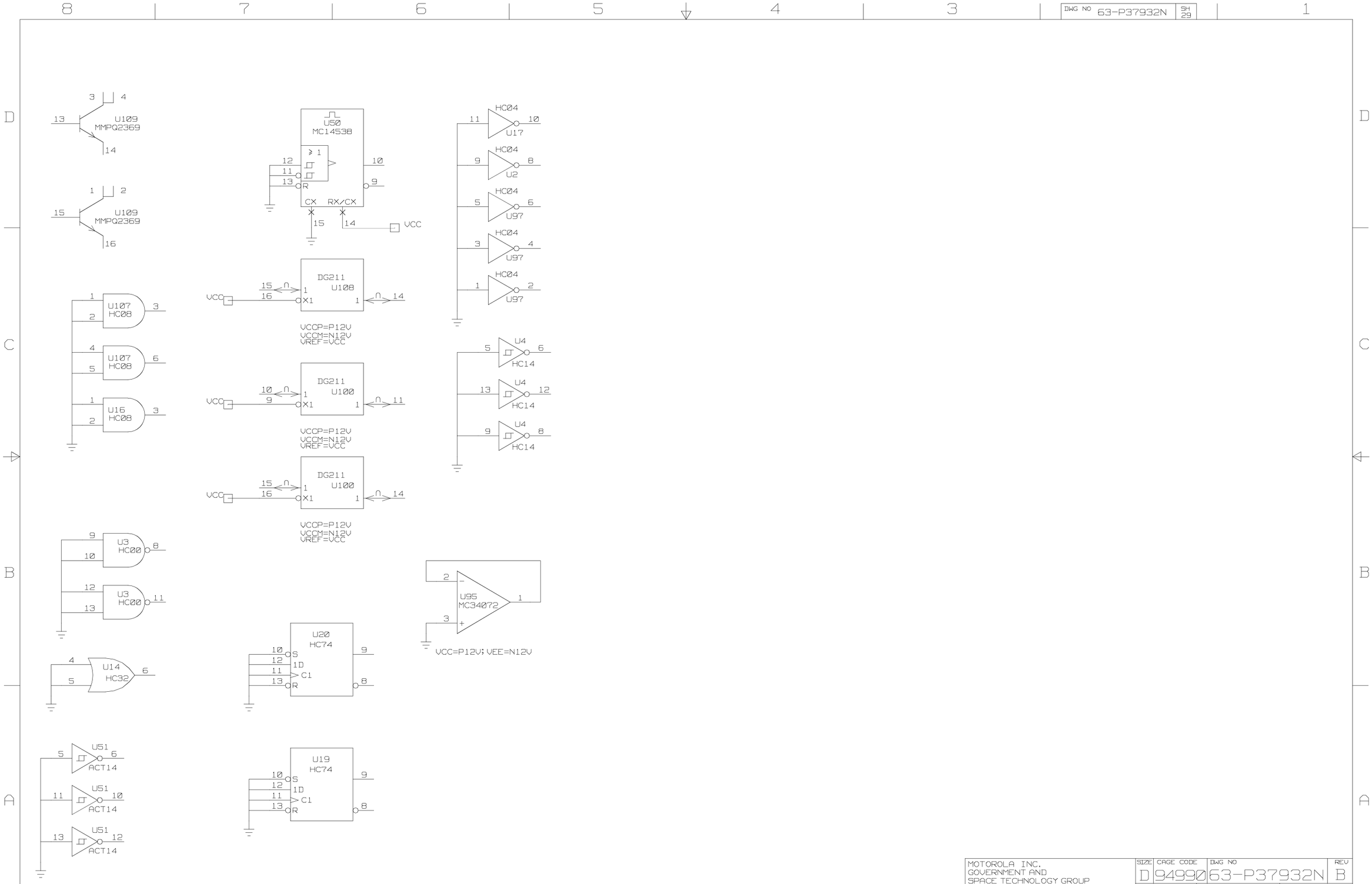
MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE			SHEET 27

N5V	(VDDA) VCC	P5SURF						P12V								N12V							
C228 .1UF	C229 .1UF	C230 .1UF	C231 .1UF	C232 .1UF	C233 .1UF	C251 .1UF		C234 .1UF	C235 .1UF	C236 .1UF	C237 .1UF	C238 .1UF	C239 .1UF			C240 .1UF	C241 .1UF	C242 .1UF	C243 .1UF	C244 .1UF			
U101-4	U102-D8	U73-13	U73-14	U75-16	U102-H11	U44-A7		U21-1	U94-8	U95-8	U96-13	U100-13	U108-13			U94-4	U95-4	U96-4	U100-4	U108-4			

VCC

C187 10UF	C186 10UF	C117 1UF	C167 1UF	C158 1UF	C149 1UF	C138 1UF	C128 .1UF	C130 .1UF	C119 .1UF	C109 .1UF	C102 .1UF	C95 .1UF	C88 .1UF	C177 .1UF	C173 .1UF	C169 .1UF	C162 .1UF	C152 .1UF	C141 .1UF	C161 .1UF	C151 .1UF	C176 .1UF	
J2	J2	20PCT 68302 2225	20PCT DSP2 2225	20PCT DSP2 2225	20PCT DSP1 2225	20PCT DSP3 2225	U1-14	U2-14	U3-14	U4-14	U5-20	U6-20	U7-20	U8-28	U9-20	U10-20	U13-14	U14-14	U15-14	U16-14	U17-14	U18-14	
C163 .1UF	C153 .1UF	C142 .1UF	C131 .1UF	C120 .1UF	C110 .1UF	C103 .1UF	C96 .1UF	C89 .1UF	C84 .1UF	C80 .1UF	C77 .1UF	C83 .1UF	C79 .1UF	C76 .1UF	C74 .1UF	C73 .1UF	C71 .1UF	C54 .1UF	C49 .1UF	C44 .1UF	C70 .1UF	C118 .1UF	
U19-14	U20-14	U22-32	U23-32	U24-20	U25-20	U26-20	U27-20	U28-28	U29-20	U30-20	U31-20	U32-28	U33-16	U34-16	U35-16	U36-16	U37-20	U38-16	U39-20	U40-16	U42-20	U45-16	
C65 .1UF	C48 .1UF	C43 .1UF	C38 .1UF	C33 .1UF	C30 .1UF	C37 .1UF	C32 .1UF	C29 .1UF	C26 .1UF	C63 .1UF	C60 .1UF	C25 .1UF	C24 .1UF	C59 .1UF	C53 .1UF	C47 .1UF	C42 .1UF	C52 .1UF	C46 .1UF	C41 .1UF	C69 .1UF	C139 .1UF	
U47-18	U47-28	U47-39	U47-62	U47-83	U47-99	U47-112	U47-131	U48-16	U46-16	U50-16	U51-14	U54-20	U55-16	U56-52	U57-28	U58-20	U60-20	U61-20	U62-20	U63-20	U64-20	U65-20	
C108 .1UF	C101 .1UF	C94 .1UF	C166 .1UF	C157 .1UF	C148 .1UF	C87 .1UF	C156 .1UF	C147 .1UF	C137 .1UF	C126 .1UF	C116 .1UF	C136 .1UF	C125 .1UF	C115 .1UF	C107 .1UF	C100 .1UF	C93 .1UF	C106 .1UF	C99 .1UF	C92 .1UF	C67 .1UF	C159 .1UF	
U66-20	U71-2	U71-9	U71-20	U71-30	U71-37	U71-45	U71-58	U71-66	U71-69	U71-79	U71-89	U71-97	U71-102	U71-113	U71-124	U71-127	U72-2	U72-9	U72-20	U72-30	U72-37	U72-45	
C75 .1UF	C182 .1UF	C181 .1UF	C179 .1UF	C175 .1UF	C171 .1UF	C178 .1UF	C174 .1UF	C170 .1UF	C165 .1UF	C155 .1UF	C146 .1UF	C164 .1UF	C154 .1UF	C145 .1UF	C135 .1UF	C124 .1UF	C114 .1UF	C134 .1UF	C123 .1UF	C113 .1UF	C127 .1UF	C172 .1UF	
U72-58	U72-66	U72-69	U72-79	U72-89	U72-97	U72-102	U72-113	U72-124	U72-127	U74-8	U79-28	U80-28	U81-28	U82-28	U83-28	U84-28	U85-28	U89-28	U90-28	U91-33	U91-64	U91-97	
C144 .1UF	C133 .1UF	C122 .1UF	C112 .1UF	C132 .1UF	C121 .1UF	C111 .1UF	C105 .1UF	C98 .1UF	C91 .1UF	C104 .1UF	C97 .1UF	C90 .1UF	C86 .1UF	C82 .1UF	C143 .1UF	C85 .1UF	C81 .1UF	C78 .1UF	C168 .1UF	C221 .1UF	C150 .1UF	C180 .1UF	
U91-128	U92-17	U92-30	U92-45	U92-60	U92-75	U92-90	U92-104	U92-120	U93-33	U96-12	U97-14	U98-16	U99-16	U100-12	U101-1	U102-E8	U102-D9	U102-A3	U102-J9	U102-E2	U102-F4	U102-K4	
C219 .1UF	C220 .1UF		C222 .1UF	C223 .1UF	C224 .1UF		1 C226 .1UF	1 C227 .1UF	C252 .1UF	C253 .1UF	C254 .1UF	C255 .1UF	C256 .1UF	C160 .1UF									
U102-G2	U102-A6		U103-28	U52-16	U105-28		2 U107-14	2 U108-12	U44-G5	U44-E4	U44-D6	U44-D7	U44-F7	U44-G4									

MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE D	CAGE CODE 94990	DWG NO 63-P37932N	REV B
	SCALE NONE		SHEET 28	



MOTOROLA INC. GOVERNMENT AND SPACE TECHNOLOGY GROUP SCOTTSDALE, ARIZONA 85252-1417	SIZE	CAGE CODE	DWG NO	REV
	D	94990	63-P37932N	B
	SCALE NONE		SHEET 29	

TABLE 1 (5)

REF DES	DEVICE TYPE (6)	VCC CONNECTION		GND CONNECTION	NO CONNECTION	DEVICE LOCATION
		CONN	VOLTS			
U1	HC32	14	+5V	7		9A5 11A2 11B2 11B6
U2	HC04	14	+5V	7		5A4 11D7 15B3 17A3 27B4 29D1
U3	HC00	14	+5V	7		6A6 17D3 29B3
U4	HC14	14	+5V	7		7B5 22D2 22D7 29C1
U5	HC245	20	+5V	10		9B2
U6	HC245	20	+5V	10		9B4
U7	ACT245	20	+5V	10		6D4
U8	22V10	28	+5V	14	1,8,15,22	7C4
U9	ACT374	20	+5V	10		5B3
U10	HC244	20	+5V	10		12B3
U11	MMPQ2369	-	-	-		24A6 24B6 24C6
U12	TC7S32F	5	+5V	3		19A7
U13	HC04	14	+5V	7		22B3 22B7 23A6 23A6 23B6 23B6
U14	HC32	14	+5V	7		11D6 22A4 29B3
U15	HC14	14	+5V	7		25B7 26B7
U16	HC08	14	+5V	7		13D6 15C3 29C3
U17	HC04	14	+5V	7		11D7 21B6 21C6 27C4 29D1
U18	HC08	14	+5V	7		15D6 15D7 17C3 17D3
U19	HC74	14	+5V	7		22D6 29A2
U20	HC74	14	+5V	7		17A2 29B2
U21	LM317	-	-	-	5,8	27B7
U22	27C020	1,32	+5V	16		10D6
U23	27C020	1,32	+5V	16		10B6
U24	ACT244	20	+5V	10		5B5
U25	ACT374	20	+5V	10		5C3
U26	ACT374	20	+5V	10		5D3
U27	ACT244	20	+5V	10		5C5
U28	22V10	28	+5V	14	1,8,15,22	6B6
U29	HC244	20	+5V	10		23C6
U30	ACT244	20	+5V	10		7D4
U31	ACT244	20	+5V	10		5D5
U32	22V10	28	+5V	14	1,8,15,22	8B5
U33	MC14538	16	+5V	8		21B3 21D3
U34	HC4017	16	+5V	8		22C4
U35	HC244	20	+5V	10		12A3 12B3
U36	HC4017	16	+5V	8		22A7
U37	HC244	20	+5V	10		23D6
U38	HC4017	16	+5V	8		22A6
U39	HC244	20	+5V	10		12A2 12B2
U40	HC4017	16	+5V	8		22A5
U41	MMPQ2369	-	-	-		25C4
U42	HC244	20	+5V	10		12B2
U43	MPQ2907A	-	-	-		26C3 26C4
U44	MCM62C416	D6,D7,E4,E5,E6,E7,F5,F6,F7,G4,G5,G6	+5V	B6,B8,C6,C7,D4,D5,D8,E3,E8,F4		20C4
		A7	+5SURF			
U45	HC4017	16	+5V	8		22C4
U46	HC4053	16	+5V	7,8		25C2
U47	MC68302	18,28,39,62,83,99,112,131	+5V	4,13,23,29,34,44,57,67,84,102,107,116,126	75,89	9D6
U48	HC4053	16	+5V	7,8		24D6
U50	MC14538	16	+5V	8		22B2 29D2

TABLE 1 (5)

REF DES	DEVICE TYPE (6)	VCC CONNECTION		GND CONNECTION	NO CONNECTION	LOCATION DEVICE
		CONN	VOLTS			
U51	ACT14	14	+5V	7		21D3 22C3 22D5 29A3
U52	HC4053	16	+5V	7,8		26C2
U53	216CKTR	-	-	-		4D5
U54	ABT540	20	+5V	10		13B2
U55	HC4017	16	+5V	8		22A4
U56	IDT7132	52	+5V	26	4,25,35,48	8D5
U57	MT5C2568	28	+5V	14		10D4
U58	HC273	20	+5V	10		12D7
U59	MC33064	-	-	-	3,5,6,7,8	11D5
U60	HC273	20	+5V	10		12C2
U61	HC273	20	+5V	10		12D2
U62	HC273	20	+5V	10		12C4
U63	HC273	20	+5V	10		12D4
U64	HC273	20	+5V	10		12C5
U65	HC273	20	+5V	10		12D5
U66	HC273	20	+5V	10		12C7
U67	216CKTR	-	-	-		4B2
U68	216CKTR	-	-	-		4D2
U69	216CKTR	-	-	-		4B4
U70	216CKTR	-	-	-		4D3
U71	DSP56002	2,9,20,30,37,45,58,66,69,79,89,97,102,113,124,127	+5V	3,5,11,16,22,27,34,36,48,56,62,67,70,75,81,86,92,98,99,105,110,116,122,129		13B5
U72	DSP56002	2,9,20,30,37,45,58,66,69,79,89,97,102,113,124,127	+5V	3,5,11,16,22,27,34,36,48,56,62,67,70,75,81,86,92,98,99,105,110,116,122,129		15B5
U73	5184726T02	13,14	+5SURF	26	1-6,15-20,28-32	21C5
U74	SN65176B	8	+5V	5		24C3
U75	MC145170	16	+5SURF	12		21D4
U76	216CKTR	-	-	-		4B5
U77	MMPQ2369	-	-	-		25A5 26A5 26B5
U79	MT5C2568	28	+5V	14		14D6
U80	MT5C2568	28	+5V	14		14B2
U81	MT5C2568	28	+5V	14		14B6
U82	MT5C2568	28	+5V	14		14B4
U83	MT5C2568	28	+5V	14		14D2
U84	MT5C2568	28	+5V	14		14D4
U85	MT5C2568	28	+5V	14		16D4
U86	MMPQ2369	-	-	-		25A6 25A7 25B5 25B6
U87	MMPQ2369	-	-	-		26B5 26B6 26B6 26B7
U89	MT5C2568	28	+5V	14		16D2
U90	MM5C2568	28	+5V	14		16D6
U91	SC38PG028CG	33,64,97,128	+5V	1,32,65,96		11D4
U92	SC02RH008CF	17,30,45,60,75,90,104,120	+5V	1,15,31,47,61,77,91,98,106,113		17B5
U93	MT5C2568	28	+5V	14		10B4
U94	MC34072	8	+12V	-		27C5 27D6
		4	-12V			
U95	MC34072	8	+12V	-		27A4 29B1
		4	-12V			
U96	DG211	4	-12V	5		27B3 27B3 27C3 27C4
		12	+5V			
		13	+12V			

TABLE 1 (5)

REF DES	DEVICE TYPE (6)	VCC CONNECTION		GND CONNECTION	NO CONNECTION	DEVICE LOCATION
		CONN	VOLTS			
U97	HC04	14	+5V	7		6A6 22C4 27B4 29C1 29D1 29D1
U98	HC4017	16	+5V	8		22C6
U99	HC4017	16	+5V	8		22C5
U100	DG211	4	-12V	5		22C4 22D3 29C2
		12	+5V			
		13	+12V			
U101	LT1016	1	+5V	6		7B6
		4	-5V			
U102	DSP56166	A3, A6, D8, D9, E2, E8, F4, G2, J9, K4	+5V	B9, D4, D5, D7, E1, E5, E6, E7, F5, F6, F7, G5, G6, G7, G10, G11, H4, H5, H6, H7		18B5
		H11	+5SURF			
U103	MT5C2568	28	+5V	14		19D5
U105	MT5C2568	28	+5V	14		19B5
U107	HC08	14	+5V	7		18C6 18D6 29C3
U108	DG211	4	-12V	5		21A3 21B5 29C2
		12	+5V			
		13	+12V			
U109	MMPQ2369	-	-	-		24B4 24C4 29D3