FT-227-R MEMORIZER
2 METER FM TRANSCEIVER

GENERAL

The model FT-227R is a new synthesized 2 meter FM transceiver specifically designed to provide high performance for amateur VHF/FM communications.

The transceiver utilizes the famed Yaesu computer theory, and is completely solid state. The unit has provision for the operation of 800 digital Phase Lock Loop channels* in 5 kHz steps between 144 to 148 MHz. An "optical coupling" system eliminates rotary switches which always used to get oxidized and noisy. The digital LED's display the selected channel in MHz, 100 kHz, and 1 kHz. The bright display lets you easily read the frequency in the bright sunlight without difficulty.

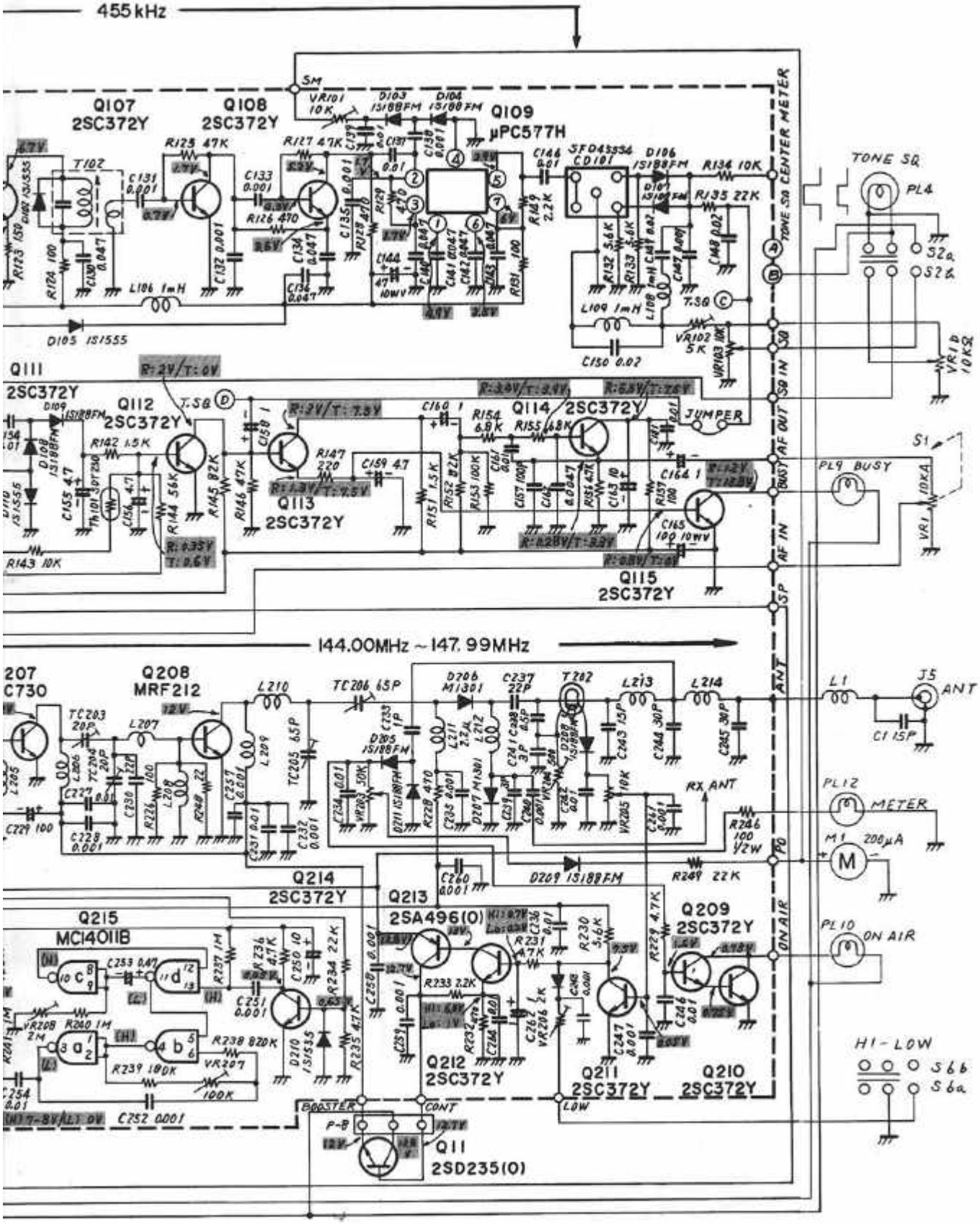
A memory circuit memorizes any channel out of 800 channels. A touch of a switch brings you back to the memorized channel instantly.

In addition to a conventional $\pm$600 kHz repeater split, any transmitter offset frequency is memorized with a touch of a push-button for operation on any ODD split frequency repeater.

The tone burst generator is built in for tone burst accessed repeater operation, and is fully adjustable for pitch, duration and level.

An optional tone guarded squelch (TGS) is provided for a silent monitoring. Placed in the TGS mode, a tone guarded signal automatically opens the receiver squelch circuit. The tone frequency can be selected within 160 Hz to 250 Hz.

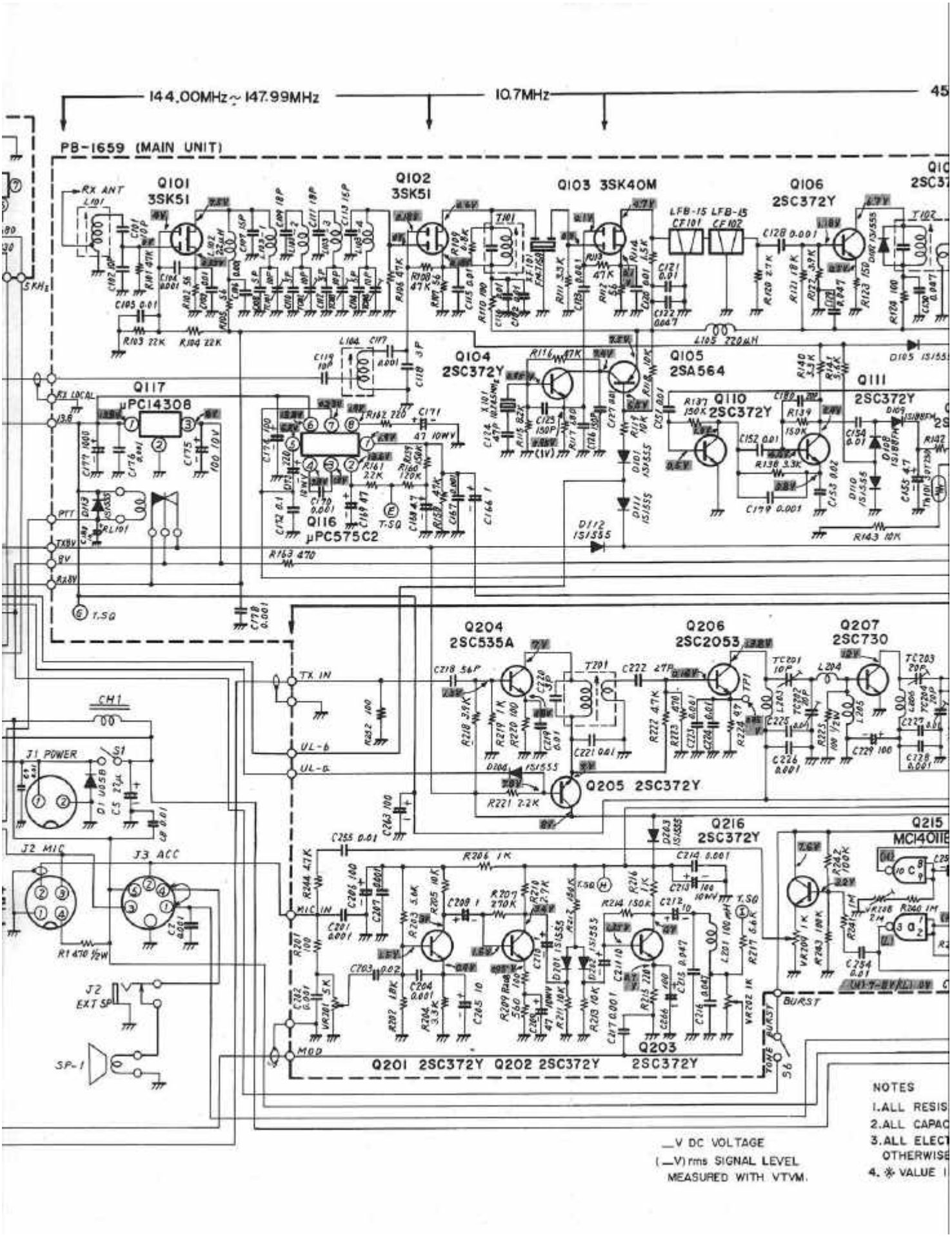
The BUSY lamp lights up if the channel is occupied by another station when the tone guarded squelch is in use. This also works as an alarm when the receiver volume is accidentally set too low.

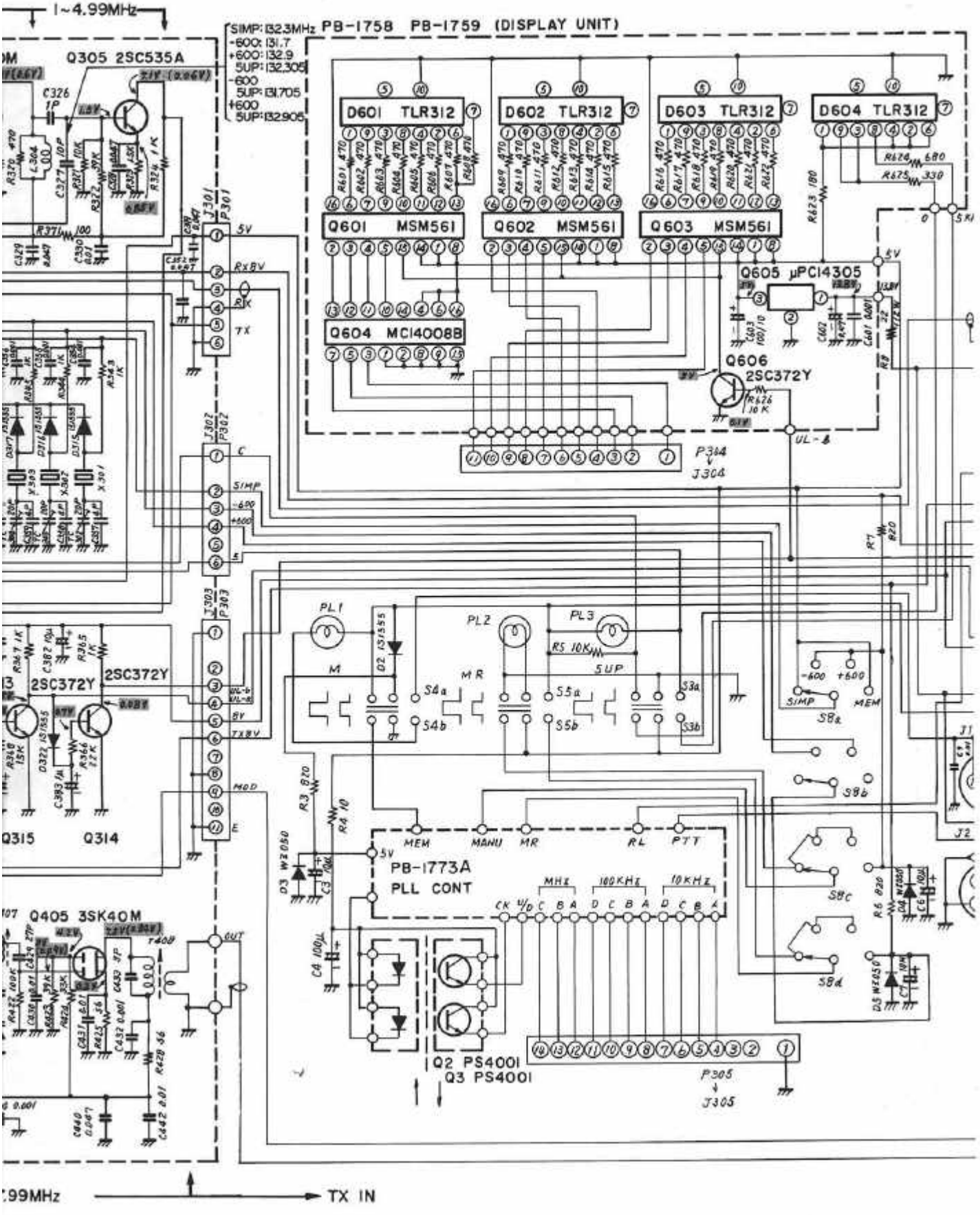


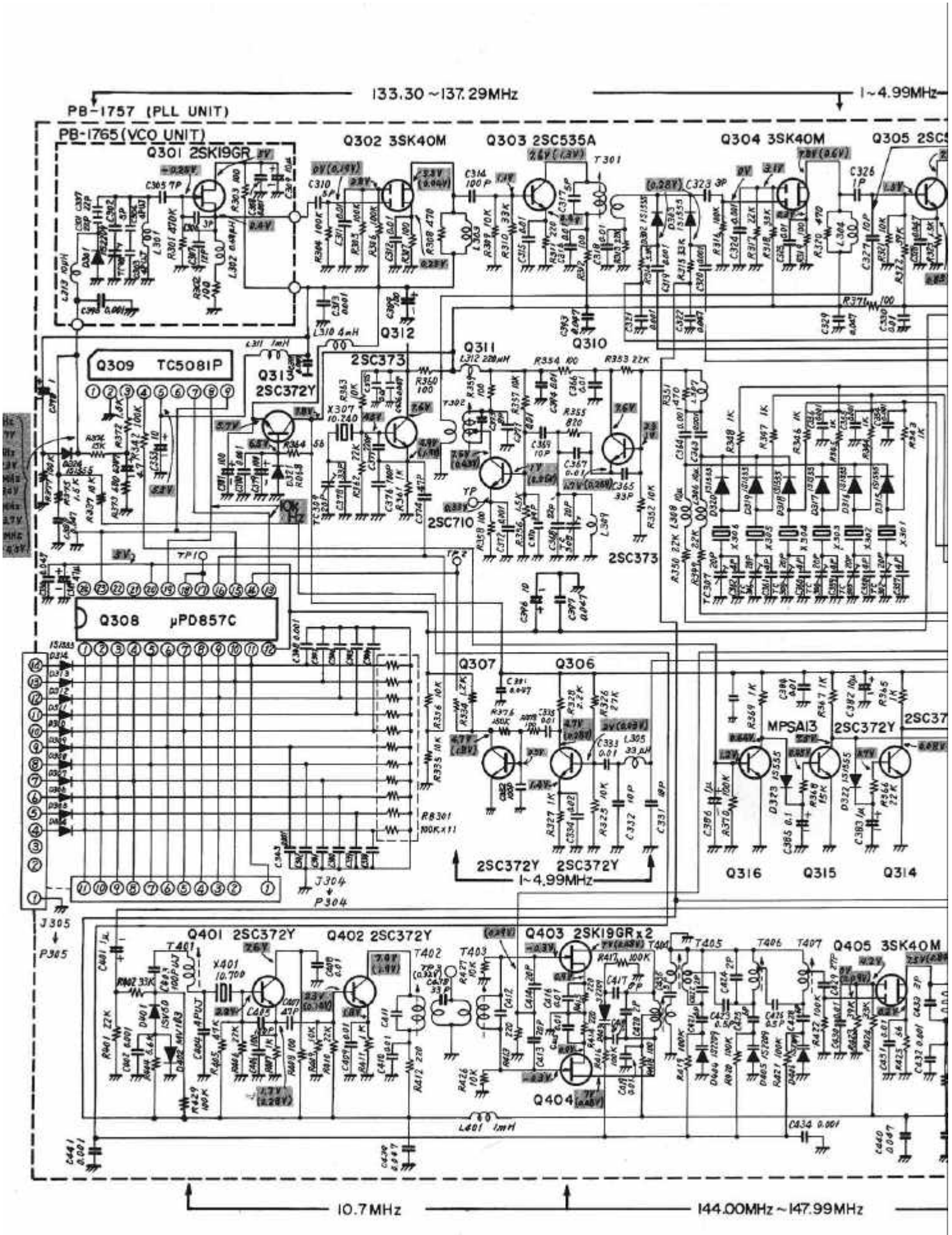
NOTES

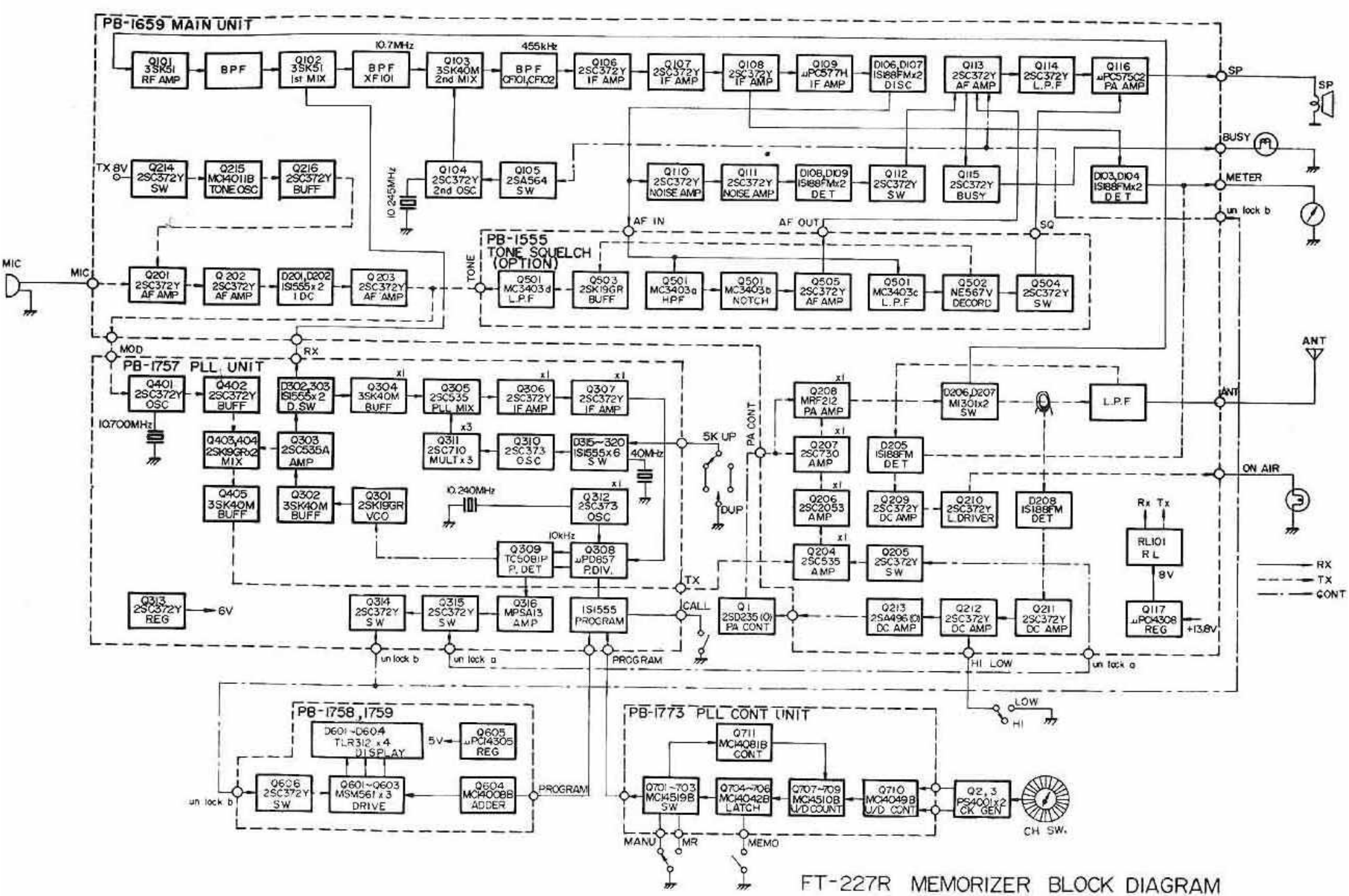
1. ALL RESISTORS ARE IN 1/4W UNLESS OTHERWISE NOTED.
2. ALL CAPACITORS ARE IN μF UNLESS OTHERWISE NOTED.
3. ALL ELECTROLYTIC CAPACITORS ARE 16WV UNLESS OTHERWISE NOTED
4. ※ VALUE IS NOMINAL.

FT-227R
CIRCUIT DIAGRAM

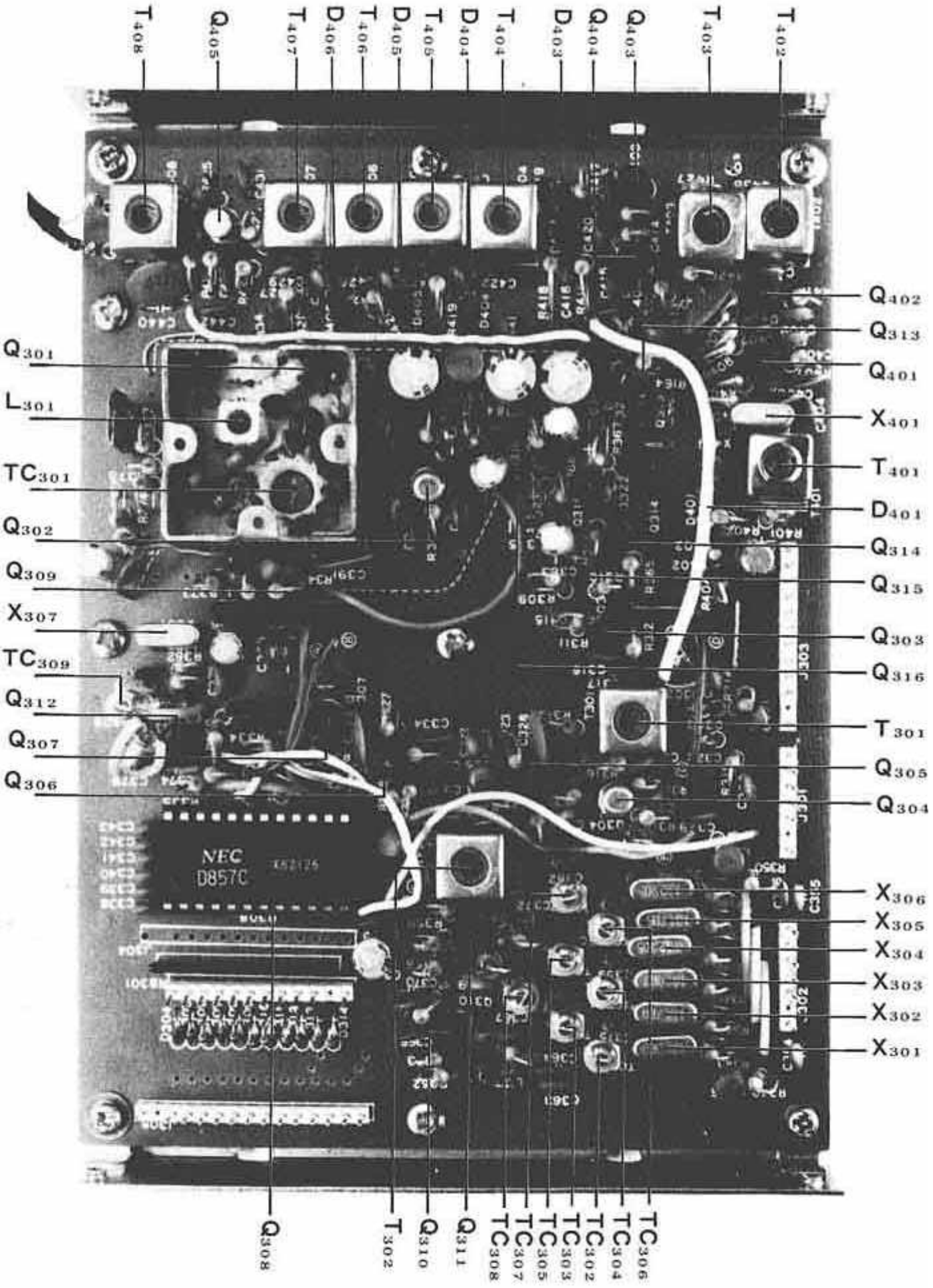

144.00MHz~147.99MHz
10.7MHz
PB-1659 (MAIN UNIT)
Q101 3SK51
Q102 3SK51
Q103 3SK40M
Q106 2SC372Y
LFB-15 LFB-15
CF101 CF102
Q104 2SC372Y
Q105 2SA564
Q111 2SC372Y
Q110 2SC372Y
Q117 μPC14308
Q116 μPC575C2
RX ANT
RX LOCAL
PTT
TX8V
8V
RX8V
T.SQ
TX IN
UL-6
UL-5
MIC IN
MOD
CH1
J1 POWER
J2 MIC
J3 ACC
J2 EXT SP
SP-1
S1
S6
Q204 2SC535A
Q206 2SC2053
Q207 2SC730
Q205 2SC372Y
Q216 2SC372Y
Q215 MC14011B
Q203
Q201 2SC372Y Q202 2SC372Y
BURST
TONE BURST
NOTES
1.ALL RESIS
2.ALL CAPAC
3.ALL ELECT
OTHERWISE
4. * VALUE
_V DC VOLTAGE
(_V) rms SIGNAL LEVEL
MEASURED WITH VTVM.

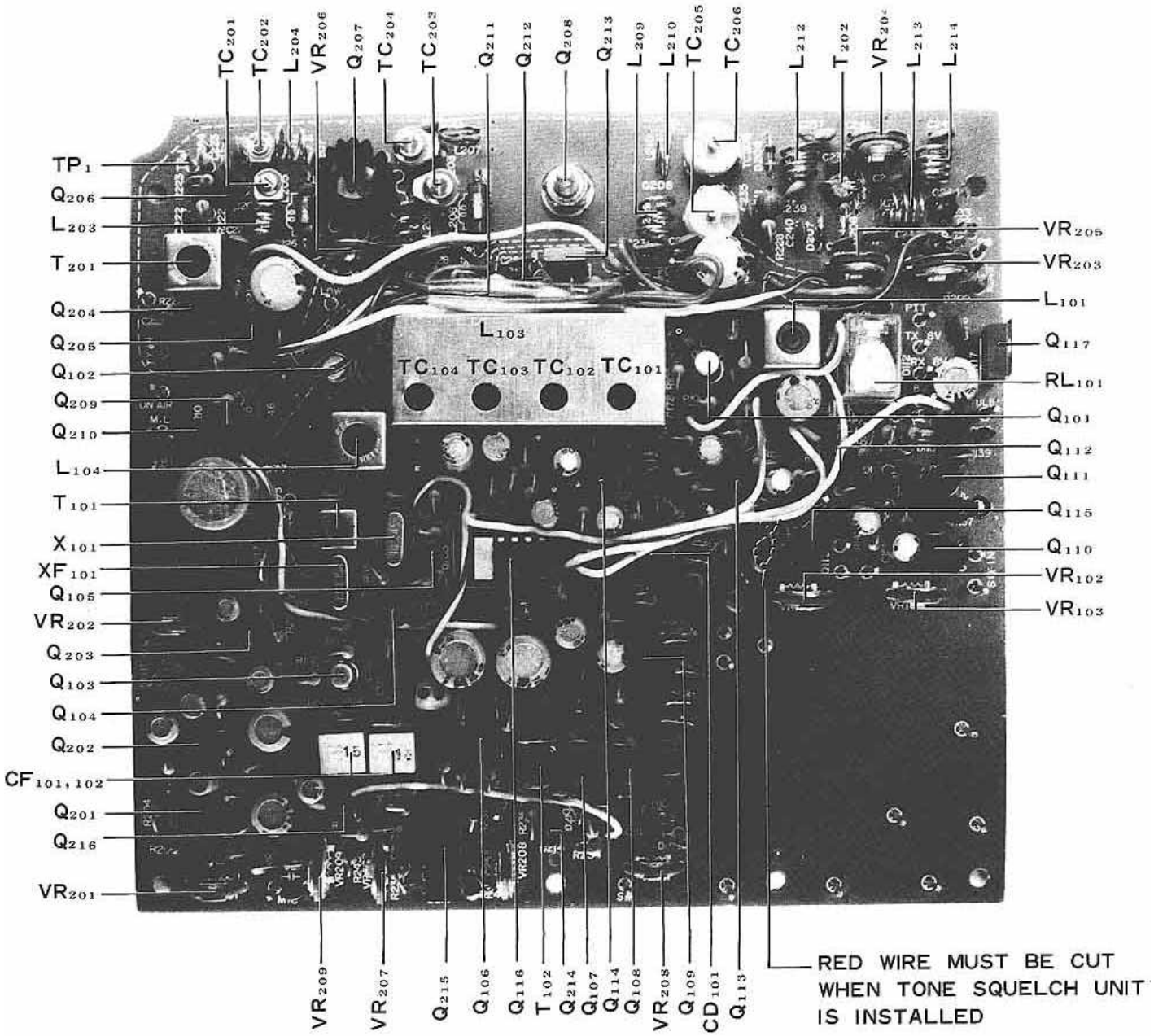

1~4.99MHz
SIMP: 132.3MHz PB-1758 PB-1759 (DISPLAY UNIT)
-600: 131.7
+600: 132.9
SUP: 132.305
-600
SUP: 131.705
+600
SUP: 132.905
Q305 2SC535A
D601 TLR312
D602 TLR312
D603 TLR312
D604 TLR312
Q601 MSM561
Q602 MSM561
Q603 MSM561
Q604 MC14008B
Q605 μPC14305
Q606 2SC372Y
P304
J304
P301
J301
P302
J302
P303
J303
PL1
PL2
PL3
M
MR
SUP
SIMP
MEM
-600
+600
2SC372Y
Q315
Q314
Q405 3SK40M
PB-1773A
PLL CONT
MEM
MANU
MR
RL
PTT
MHz
100KHz
10KHz
Q2 PS4001
Q3 PS4001
P305
J305
TX IN

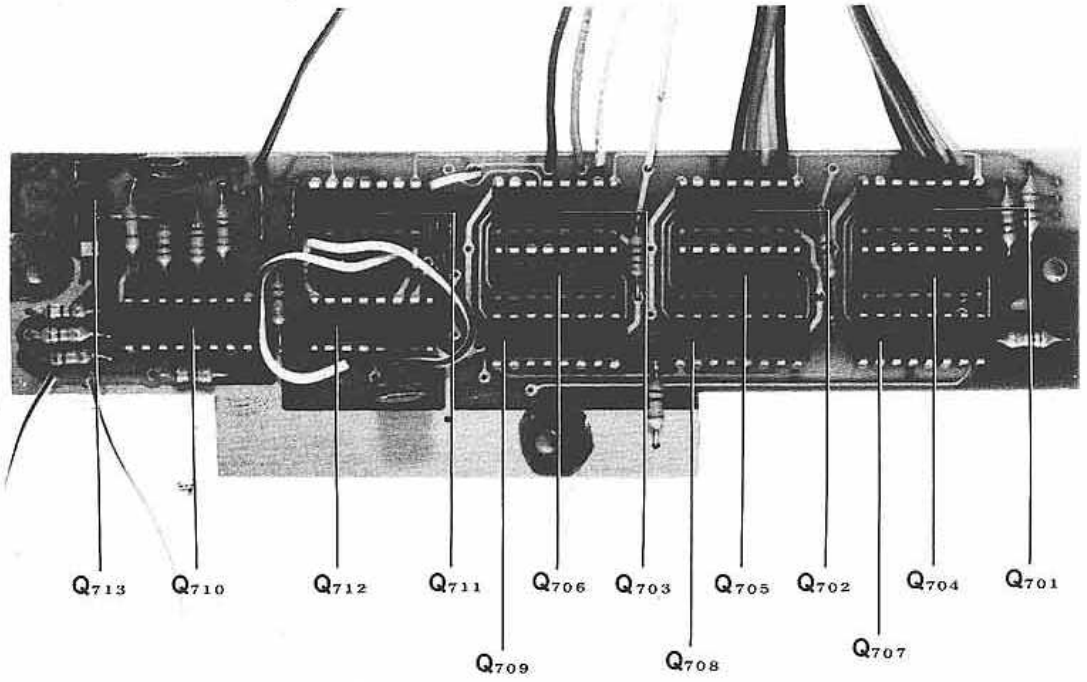

133.30~137.29MHz
1~4.99MHz
PB-1757 (PLL UNIT)
PB-1765(VCO UNIT)
Q301 2SK19GR
Q302 3SK40M
Q303 2SC535A
Q304 3SK40M
Q305 2SC5
Q309 TC5081P
Q313 2SC372Y
Q312
Q311 2SC373
Q310
Q308 μPD857C
2SC710
2SC373
Q307
Q306
MPSA13
2SC372Y
Q316
Q315
Q314
2SC372Y 2SC372Y
1~4.99MHz
J304
P304
J305
P305
Q401 2SC372Y
Q402 2SC372Y
Q403 2SK19GR x2
Q404
Q405 3SK40M
10.7MHz
144.00MHz~147.99MHz



FT-227R MEMORIZER BLOCK DIAGRAM


PLL UNIT
T408
Q405
T407
D406
T406
D405
T405
D404
T404
D403
Q404
Q403
T403
T402
Q402
Q313
Q401
X401
T401
D401
Q314
Q315
Q303
Q316
T301
Q305
Q304
X306
X305
X304
X303
X302
X301
Q301
L301
TC301
Q302
Q309
X307
TC309
Q312
Q307
Q306
Q308
T302
Q310
Q311
TC308
TC307
TC305
TC303
TC302
TC304
TC306
NEC
D857C





PLL CONTROL UNIT

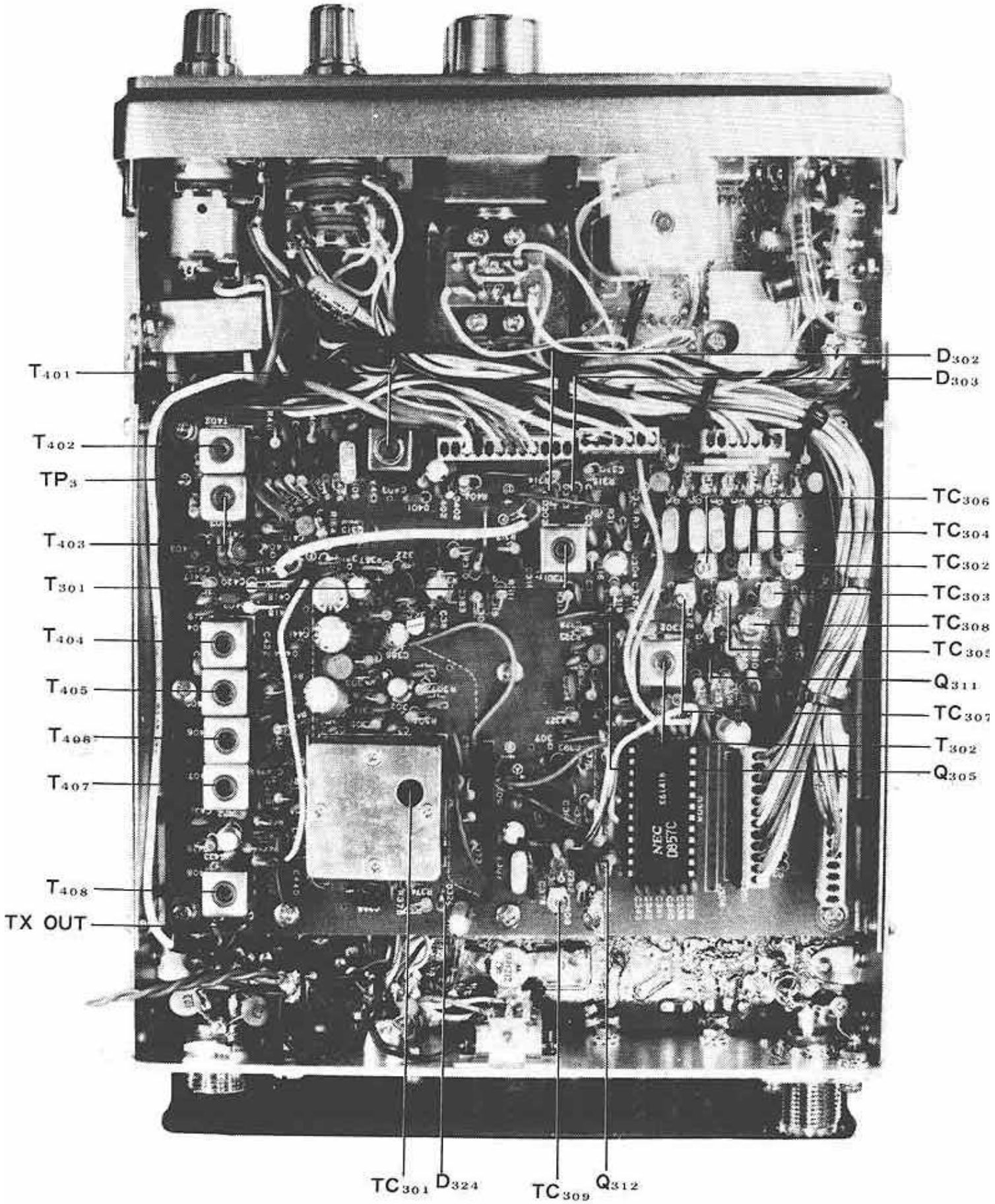


Figure 16 ALIGNMENT POINT

THEORY OF OPERATION

The block diagram and the circuit description that follows will provic you with a better understanding of this transceiver. Refer to the sch ematic diagram for circuit details.

The transceiver consists of a transmitter, and a double conversion super heterodyne receiver utilizing a digital phase lock loop synthesizer, capable of operating on any of the 800 channels within the frequency range of 144 to 148 MHz. Solid state circuitry is employed throughout and computer theory is utilized for frequency selection. The transceiver is designed to operate from a 13.8 Volts ±10% negative ground power source.

TRANSMITTER

The transmitter produces a Frequency Modulated (FM) signal. The audio signal from the microphone is set to a proper level by VR201 and amplified by Q201, Q202 and Q203, (2SC372Y). The audio output from Q202 is coupled to the IDC (Instantaneous Deviation Control) circuit where both positive and negative peaks are clipped by diodes D201 and D202, (1S1555). The output from the last amplifier Q203 is fed through a low-pass filter which attenuates frequencies above the speech range caused by the clipping at the level set by the deviation control potentiometer VR202. This control is nominally set for a deviation of ±5 kHz. The speech signal is then applied to a phase modulator varactor diode, D401, (ISV50) which varies the frequency of the 10.7 MHz crystal controlled oscillator, Q401 (2SC372Y). The frequency modulated 10.7 MHz signal is then amplified by a buffer amplifier Q402, (2SC372Y) and then fed to a balanced mixer consisting of Q403 and Q404, (2SK19GR) where the signal is converted up to 144-148 MHz signal by mixing with the 133.3-137.3 MHz signal delivered from the VCO (voltage controlled oscillator). The output frcm the balanced mixer is fed through the tuned circuits consisting of T404-T407 to an amplifier Q405, (35K40M). T404-T407 is tuned to the transmitting frequency by varactor diodes D403-D406 of whose capacitance changes in accordance with the DC output Voltage from the PLL circuit. The 144-148 MHz signal is then amplified by the amplifier stages consisting of Q204, (25C535A), Q206,(2SC2053), Q207, (2SC730) and Q208, (MRF212) which delivers 10 Watts of RF energy through a diode switch and low pass filter into a 50 ohm load.

Diodes D205, and D211 (1S188FM) rectify a small portion of the RF output and applies the resultant DC voltage to the meter which indicates relative power output from the transmitter.

The DC output from D205 also is delivered to the lamp driver Q209 and Q210, (2SC372Y) which turns the ON AIR lamp on during the transmission.

If the transmitter is keyed without an antenna being connected, or, if a high VSWR exists in the antenna system, the reflected power is detected through T202 and a diode, D208, (1S188FM) which produces DC voltage. Q211, (2SC372Y) conducts with DC voltage applied through VR205 causing a decrease in Q212, (2SC372Y)'s collector current.

Thus, the collector voltage of Q213, (2SA496) drops, causing Q11, (2SD235) to decrease current and supply voltage to the PA amplifier which is lowered to prevent damage to the transistor. The threshold level is set by VR205. This circuit is also used to switch the output power down to 1 Watt when the HI-LOW switch is set to LOW. The amount of power reduction may be adjusted with VR206.

The antenna change-over circuit consists of switching of diodes D206 and D207, (MI301).

The tone burst circuit consists of a timing generator and a gated multivibrator. With the BURST switch at the "ON" position, a DC voltage is applied to the tone burst circuit. When the transmitter is keyed, Q214, (2SC372Y) conducts and triggers the one-shot multivibrator Q215, (MC14011B). The other half of Q215 generates a tone signal which is amplified by a buffer Q216, (2SC372Y) and applied to the microphone circuit of the transmitter.

The tone frequency is adjustable by VR207, while the output level (deviation) is adjustable by VR209 and the burst duration by VR208.

RECEIVER SECTION

The input signal from the antenna is fed through the low-pass filter consisting of L1, L214, L213, C1 and C243-C245 and the diode change-over switch consisting of D206, D207 and L212 to the FET amplifier Q101, (3SK51). The amplified signal is then applied through four stage high Q coax resonators to the first mixer Q102, (3SK51). The use of a dual gate FET RF amplifier together with high Q coax resonators, minimizes effects of cross modulation and other spurious responses while providing a low noise figure for the receiver front end.

The 144 to 148 MHz signal is heterodyned with the first local oscillator and produces a 10.7 MHz first IF signal. The first local oscillator is delivered from the PLL (Phase Lock Loop) VCO circuit.

The first IF signal is fed through a crystal filter XF101 which has a pass band of $\pm$7.5 kHz, to the second mixer Q103, (3SK40M) which produces a 455 kHz second IF signal by heterodyning with the 10.245 MHz output signal of the second local oscillator Q104, (2SC372Y). Q105, (2SA564) works as a switch which disconnects the supply voltage to Q104 when the PLL circuit is unlocked.

The second IF circuit consists of Q106, Q107, Q108, (2SC372Y) and Q109, (μPC577H). The cascade connected ceramic filters CF101 and CF102 provide narrow band selectivity for the receiver and the limiting action of Q109 removes any amplitude variation to the ceramic discriminator consisting of CD101, D106, and D107, (1S188FM).

The discriminator produces an audio output in response to a corresponding frequency shift in the IF signal. The output audio signal is amplified by Q113, Q114, (2SC372Y) and is applied across the VOLUME control VR1 to the input of the audio amplifier Q116, (μPC575C2). The output from Q116 is applied in series through the ACC socket to the internal speaker. The low-pass filter between Q113 and Q114 attenuates the audio frequency spectrum above 3 kHz to increase readability of the received signal.

A portion of the 455 kHz IF signal is rectified by D103, D104, (1S188FM) for S-meter indication. VR101 is used to adjust the meter sensitivity.

When no carrier is present in 455 kHz IF, the high frequency noise at the discriminator output is amplified by Q110 and Q111, (2SC372Y) then detected by D108 and D109, (1S188FM) to produce a DC voltage. This voltage is then applied to turn Q112, (2SC372Y) on. With the conduction of Q112, the base of Q113 is grounded to squelch the audio amplifiet. When a carrier is present in the 455 kHz IF, the noise is removed from the discriminator output and the audio amplifier then recovers normal operation.

The squelch circuit opening causes Q113 to conduct, causing lamp driver Q115, (2SC372Y) to draw current to light up the BUSY LAMP. The SQUELCH controls, VR2 and VR102, set the threshold level.

HETERODYNE OSCILLATOR

The heterodyne signal is generated by the PLL (phase lock loop) circuit consisting of VCO (voltage controlled oscillator), reference crystal oscillator, programmable divider and phase comparator.

The VCO oscillator, Q301 (2SK19GR) generates 133.3-137.3 MHz signals. The oscillator frequency is controlled by a varactor diode D301, (1S2209) which varies the capacitance of a tuned circuit consisting of L301, TC301, C302 and C304 in accordance with a DC voltage supplied from a phase comparator Q309, (TC5081P).

The output signal from Q301 is amplified by a buffer amplifier Q302, (3SK40M) and Q303, (2SC535A) and fed through a diode switch, D302 and D303, (1S1555) to the receiver or transmitter mixers.

A portion of the output from Q303 is fed through a buffer amplifier Q304, 3SK40M to a PLL mixer, Q305, (2SC535A) which produces 1-5 MHz PLL IF signaled by mixing with the PLL heterodyne signal.

The PLL heterodyne signal is generated by a overtone crystal controlled oscillator Q310, (2SC373). The crystal frequency is shown in Table 1.

X-Tal	Frequency	PLL Het. Freq.	Remarks
X301	44.10000 MHz	132.300	Simplex
X302	43.90000	131.700	TX-600 kHz shift
X303	44.30000	132.900	TX+600 kHz shift
X304	44.10166	132.305	Simplex 5 kHz up
X305	43.90166	131.705	TX-600 kHz 5kHz up
X306	44.30166	132.905	TX+600 kHz 5kHz up

Table 1.

The diode switch D315-D320, 1S1555 selects the appropriate crystal in accordance with the FUNCTION switch and 5kHz up switch. The output from Q310 is fed to a tripler Q311, (2SC710) which produces the PLL heterodyne signal.

The PLL IF signal is fed through a low pass filter consisting of L305, C331 and C332 to the amplifiers Q306 and Q307, (2SC372Y). The amplified signal is then fed to a programmable divider, Q308, (uPD857C).

The crystal oscillator, Q312, (2SC373) generates 10.24 MHz signal, and its output is fed to the scaler/divider Q308 (uPD857C), where the 10.24 MHz signal generates a 10 kHz reference signal.

The digital phase comparator Q309, TC5081P compares the phase of the PLL IF signal with that of the reference signal, and any phase difference is converted into an error correcting voltage. This error correcting voltage is fed to the varactor diode D301 which changes the output signal phase to lock with that of the reference signal.

When the VCO is locked, the constant voltage at pin 4 of Q309 is applied to Q316, (MPSA13) to conduct, and in turn Q315, (2SC372Y) cuts off. The "H" voltage at the collector of Q315 turns Q205, (2SC372Y) to conduct and it supplies DC voltage to the exciter younger stages Q204 and Q206. When the VCO is unlocked, the DC voltage at the emitter of Q205 drops to prevent a normal operation of Q204 and Q206.

The output voltage from Q315 is reversed in polarity by Q314, (2SC372Y) and applied to the Q606, (2SC372Y) keeping the collector of Q606 in "H" level in order to drive Q601 through Q603 for the display of the channel frequency. The voltage is also applied to Q105, (2SA564) which supplies DC voltage to a second heterodyne oscillator Q104, (2SC372Y).

When the VCO is unlocked, the collector DC voltage drops causing the LED's to turn off and simultaneously the second heterodyne oscillator ceases to oscillate. Thus the receiver is muted until VCO lock occurs.

PLL CONTROL SECTION

The optical coupling system utilizes two photo-interrupters Q2 and Q3, (PS-4001) to generate two signal outputs which are applied to a PLL counter unit. The signal applied to CK terminal is fed through a waveshaper Q710, (MC14049B) to BCD up down counter, Q707 (10 kHz), Q708 (100 kHz) and Q709 (1 MHz), using MC14510B as a clock signal.

The signal applied to U/D terminal is inverted by a unit of Q710 and controls the up-down counter. The output from Q707-Q709 is fed to a 4 bit data selector, Q701-Q703 (MC1451B) and Quad latch, Q704-Q706, (MC14042B), which are used for memory when the MEMORY switch is pressed.

The output from Q701-Q703 is fed to a programmable divider, Q308, (μPD857C).

Q711, (MC14081B) (for high end) and Q712, (MC14028B) (for low end) cut off Q713, (2SC735Y) to prevent any transmission outside the amateur bands.

The BCD signals at the input of the programmable divider are also fed to the LED driver, Q601-Q603, (MSM561) to drive LED, D601-D603, TLR 312.

4-BIT full adder, Q604, (MC14008B) is used as a binary adder to produce 4-8 display on MHz range.

LED, D604, (TLR312) displays 0 or 5 by the 5 UP switch.

The display LED will be turned off by Q605, (2SC372Y) when an unlocked signal is received.

POWER SUPPLY

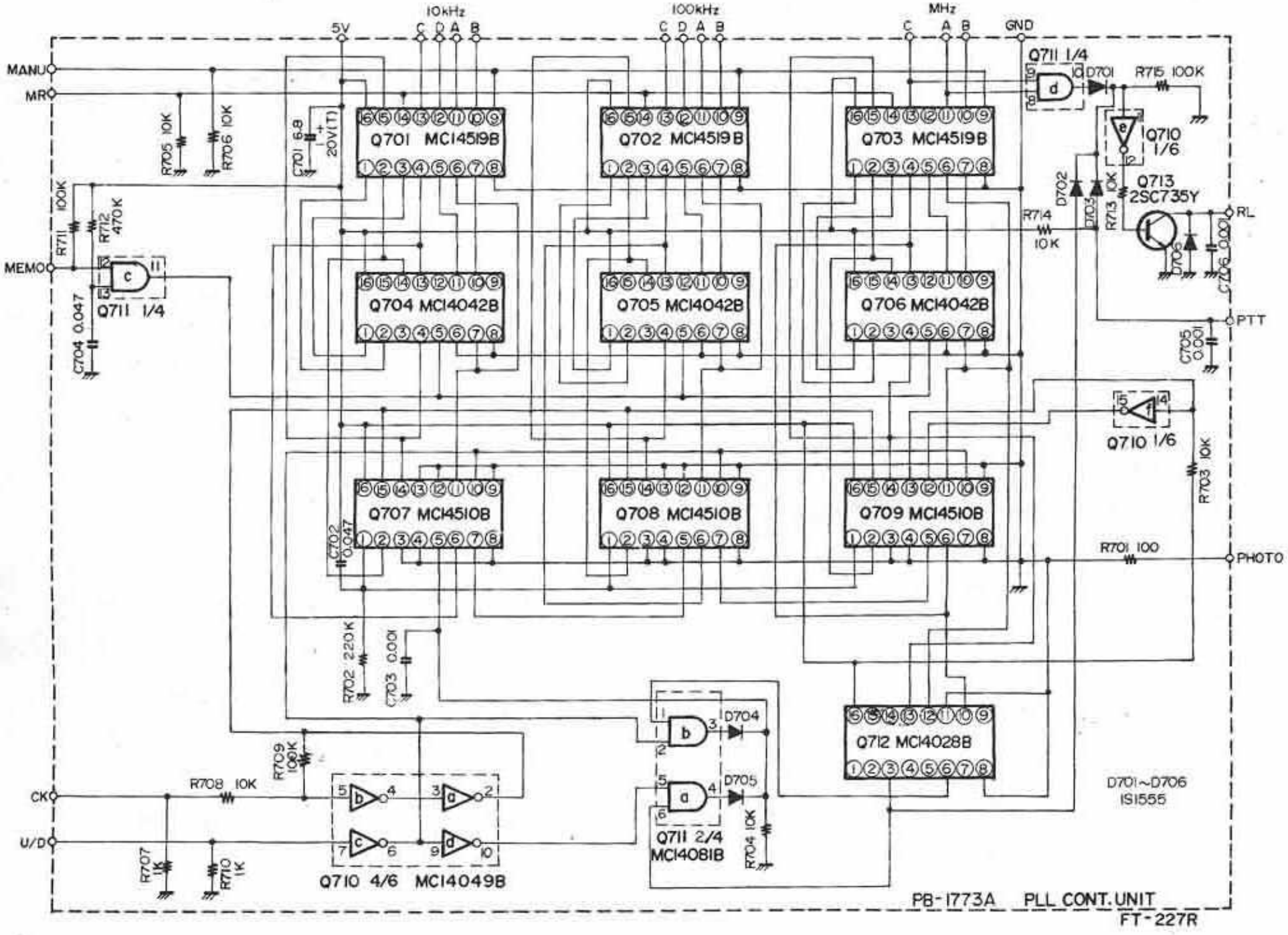
DC 13.8 Volt supply is used for the audio power amplifier Q116, relay and lamps. The supply voltage to the driver and final power amplifier is

fed through the voltage regulator, Q11 (2SD235D) which is controlled by the HI/LOW switch and the automatic final protection circuit.

Voltage regulator, Q605 (μPC14305) regulates the supply voltage at 5 Volts to supply Q308 and the display unit, Q313, (2SC372Y) and D301, (RD6.8EB) regulates the supply voltage at 6 Volts for the VCO and phase comparator. The 5 Volts supply for the PLL control unit is regulated by a zener diode, D3, (WZ050) and is connected directly to keep memory when the power switch is turned off with M switch pressed.

A regulated 8 Volt supply using Q117, (μPC14308) is used for all other circuits.

When the function switch is at MEM position, D4 (WZ050) supplies 5 Volts to the receiver, and D5, (WZ050) supplies 5 Volts to the transmitter.


10kHz
100kHz
MHz
5V
GND
C D A B
MANU
MR
MEMO
CK
U/D
PTT
RL
PHOTO
Q701 MC14519B
Q702 MC14519B
Q703 MC14519B
Q704 MC14042B
Q705 MC14042B
Q706 MC14042B
Q707 MC14510B
Q708 MC14510B
Q709 MC14510B
Q712 MC14028B
Q711 1/4
Q710 1/6
Q713 2SC735Y
Q710 4/6 MC14049B
Q711 2/4 MC14081B
D701~D706 1S1555
R705 10K
R706 10K
R711 100K
R712 470K
R715 100K
R714 10K
R713 10K
R703 10K
R701 100
R702 220K
R708 10K
R709 100K
R707 1K
R710 1K
R704 10K
C701 6.8 20V(T)
C704 0.047
C702 0.047
C703 0.001
C705 0.001
C706 0.001
PB-1773A PLL CONT. UNIT
FT-227R

OPTIONAL TONE SQUELCH CIRCUIT

The Tone Squelch operation permits private communications on crowded channels. The tone squelch circuit disables the audio circuit of receiver until a preset tone signal is received.

The transmitted signal is modulated by the tone signal within 70 Hz to 250 Hz which is below the 300 Hz to 3000 Hz voice frequency range used in radio communications.

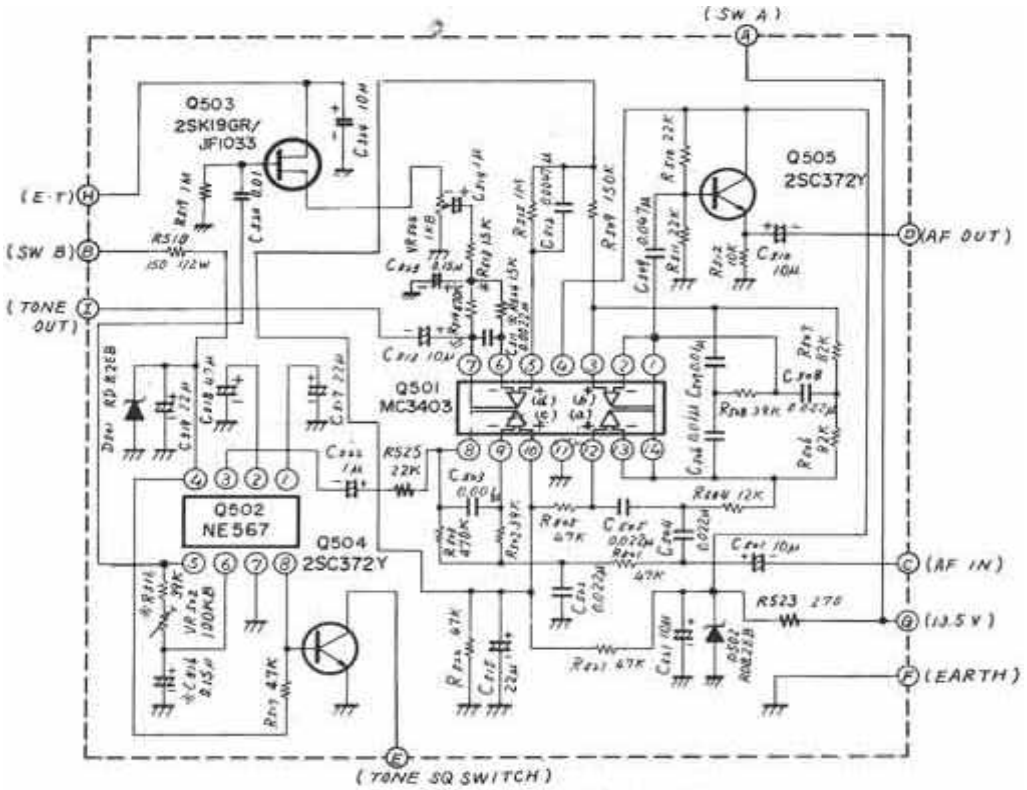
The tone signal is generated by Q502, NE567 and its frequency is set by R516, VR502 and C516. The level of the tone signal is set by VR504 and it is fed through a buffer amplifier Q503, 2SK19GR to the low-pass filter consisting of unit "d" of an operational amplifier Q501, MC3403. The tone signal is then superimposed to the speech signal by Q202. The constants for preset frequency are obtained from the chart.

The audio output signal from the receiver discriminator is fed to the unit "a" of Q501, MC3403. The unit "a" of Q501 forms a high-pass filter and the unit "b" of Q501 forms a T-notch filter. Both filters remove the tone signal from the audio signal which is then fed through an audio amplifier Q505, 2SC372Y to the receiver audio amplifier Q111.

The tone signal passes through a low pass filter by unit "c" of Q501 and is fed to Q502, NE567. When the tone signal has the same frequency as preset for transmitting, the voltage of pin 8 of Q502 becomes low causing Q504, 2SC372Y to "OFF". In turn, proper bias voltage is applied to Q116 for normal operation.

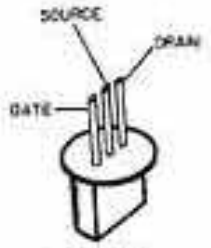
Without proper tone signal, Q504 conducts, removing the proper bias from Q116 to disable the audio circuit.

As the conventional carrier squelch circuit is operative when the tone squelch is switched in, the busy lamp lights up when any carrier is received.

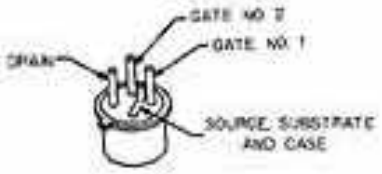


TONE SQUELCH (PB-1555A) OPTION

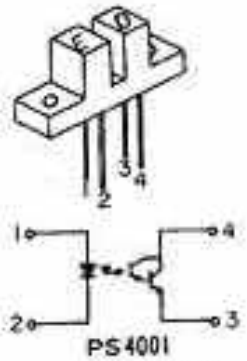
TRANSISTOR & IC CONNECTIONS



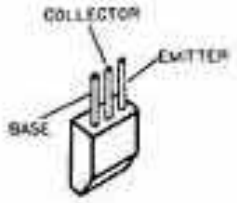
2SK19Y
2SK19GR



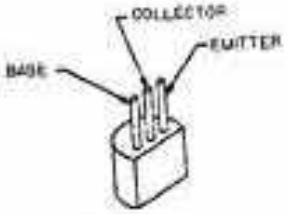
3SK40M
3SK51



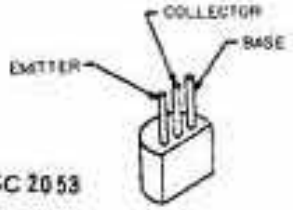
PS4001



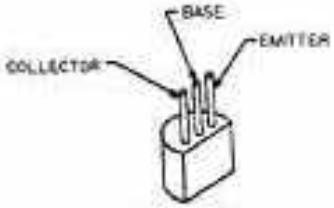
2SC535A



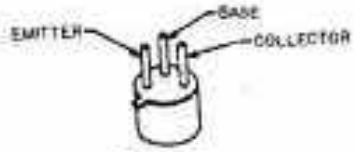
2SA564A
2SA733



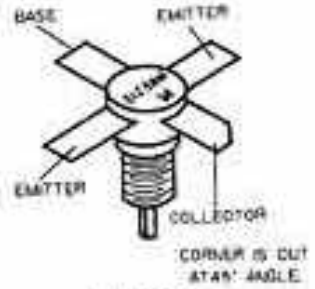
2SC2053
2SC710D



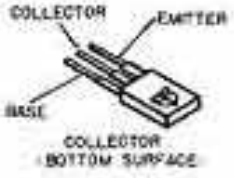
MPSA13



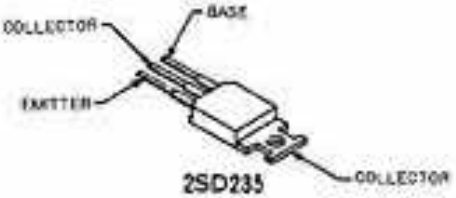
2SC730



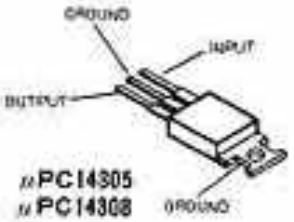
MRF212



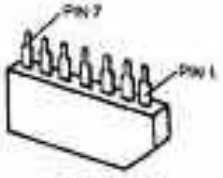
2SA496O



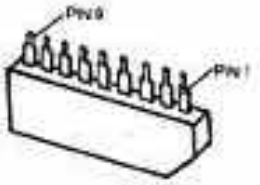
2SD235



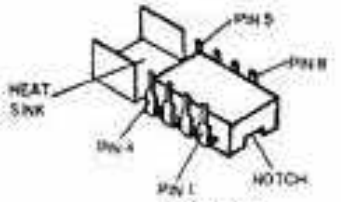
μPC1430S
μPC1430B



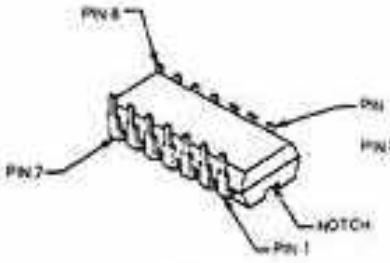
μPC577H



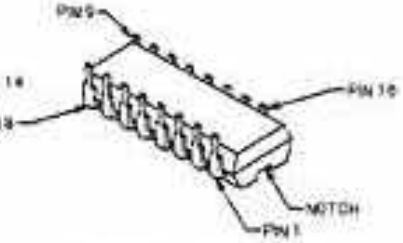
TC5081



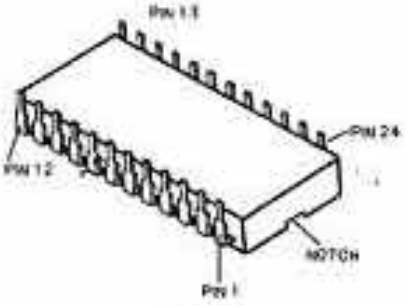
μPC575C2



MC14011B
MC14081B



MSM561 MC14049B
MC14008B MC14510B
MC14028B MC14511B
MC14042B MC14519B



μPD857C

Q308 (μPD857C) PROGRAMMABLE DIVIDER CODE

Q308 PROGRAMMABLE INPUT PIN →			1	2	3	4	5	6	7	8	9	10	11
P/J305 →			4	5	6	7	8	9	10	11	12	13	14
P/J304 →			11	10	9	8	7	6	5	4	3	2	1
FREQUENCY ↓	DIAL DISPLAY ↓	PROGRAMMABLE DIVIDER RATIO ↓	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	P_9	P_{10}	P_{11}
144.00	4.000	1/100	0	0	0	0	0	0	0	0	1	0	0
4.01	4.010	1/101	1	0	0	0	0	0	0	0	1	0	0
4.02	4.020	1/102	0	1	0	0	0	0	0	0	1	0	0
4.03	4.030	1/103	1	1	0	0	0	0	0	0	1	0	0
4.04	4.040	1/104	0	0	1	0	0	0	0	0	1	0	0
4.05	4.050	1/105	1	0	1	0	0	0	0	0	1	0	0
4.06	4.060	1/106	0	1	1	0	0	0	0	0	1	0	0
4.07	4.070	1/107	1	1	1	0	0	0	0	0	1	0	0
4.08	4.080	1/108	0	0	0	1	0	0	0	0	1	0	0
4.09	4.090	1/109	1	0	0	1	0	0	0	0	1	0	0
144.10	4.100	1/110	0	0	0	0	1	0	0	0	1	0	0
4.11	4.110	1/111	1	0	0	0	1	0	0	0	1	0	0
4.12	4.120	1/112	0	1	0	0	1	0	0	0	1	0	0
4.13	4.130	1/113	1	1	0	0	1	0	0	0	1	0	0
4.14	4.140	1/114	0	0	1	0	1	0	0	0	1	0	0
4.15	4.150	1/115	1	0	1	0	1	0	0	0	1	0	0
4.16	4.160	1/116	0	1	1	0	1	0	0	0	1	0	0
4.17	4.170	1/117	1	1	1	0	1	0	0	0	1	0	0
4.18	4.180	1/118	0	0	0	1	1	0	0	0	1	0	0
4.19	4.190	1/119	1	0	0	1	1	0	0	0	1	0	0
144.20	4.200	1/120	0	0	0	0	0	1	0	0	1	0	0
4.30	4.300	1/130	0	0	0	0	1	1	0	0	1	0	0
4.40	4.400	1/140	0	0	0	0	0	0	1	0	1	0	0
4.50	4.500	1/150	0	0	0	0	1	0	1	0	1	0	0
4.60	4.600	1/160	0	0	0	0	0	1	1	0	1	0	0
4.70	4.700	1/170	0	0	0	0	1	1	1	0	1	0	0
4.80	4.800	1/180	0	0	0	0	0	0	0	1	1	0	0
4.90	4.900	1/190	0	0	0	0	1	0	0	1	1	0	0
145.00	5.000	1/200	0	0	0	0	0	0	0	0	0	1	0
145.01	5.010	1/201	1	0	0	0	0	0	0	0	0	1	0
145.02	5.020	1/202	0	1	0	0	0	0	0	0	0	1	0
145.03	5.030	1/203	1	1	0	0	0	0	0	0	0	1	0
145.04	5.040	1/204	0	0	1	0	0	0	0	0	0	1	0
145.05	5.050	1/205	1	0	1	0	0	0	0	0	0	1	0
145.06	5.060	1/206	0	1	1	0	0	0	0	0	0	1	0
145.07	5.070	1/207	1	1	1	0	0	0	0	0	0	1	0
145.08	5.080	1/208	0	0	0	1	0	0	0	0	0	1	0
145.09	5.090	1/209	1	0	0	1	0	0	0	0	0	1	0
145.10	5.100	1/210	0	0	0	0	1	0	0	0	0	1	0
145.20	5.200	1/220	0	0	0	0	0	1	0	0	0	1	0
145.30	5.300	1/230	0	0	0	0	1	1	0	0	0	1	0
145.40	5.400	1/240	0	0	0	0	0	0	1	0	0	1	0
145.50	5.500	1/250	0	0	0	0	1	0	1	0	0	1	0
145.60	5.600	1/260	0	0	0	0	0	1	1	0	0	1	0
145.70	5.700	1/270	0	0	0	0	1	1	1	0	0	1	0
145.80	5.800	1/280	0	0	0	0	0	0	0	1	0	1	0
145.90	5.900	1/290	0	0	0	0	1	0	0	1	0	1	0
146.00	6.000	1/300	0	0	0	0	0	0	0	0	1	1	0
147.00	7.000	1/400	0	0	0	0	0	0	0	0	0	0	1
147.99	7.990	1/499	1	0	0	1	1	0	0	1	0	0	1

※1 HIGH LEVEL (5V)
※0 LOW LEVEL (0V)