MAINTENANCE MANUAL

GPS SIMULCAST
GETC INTERFACE MODULE
ROA 117 2269

TABLE OF CONTENTS

ERICSSON

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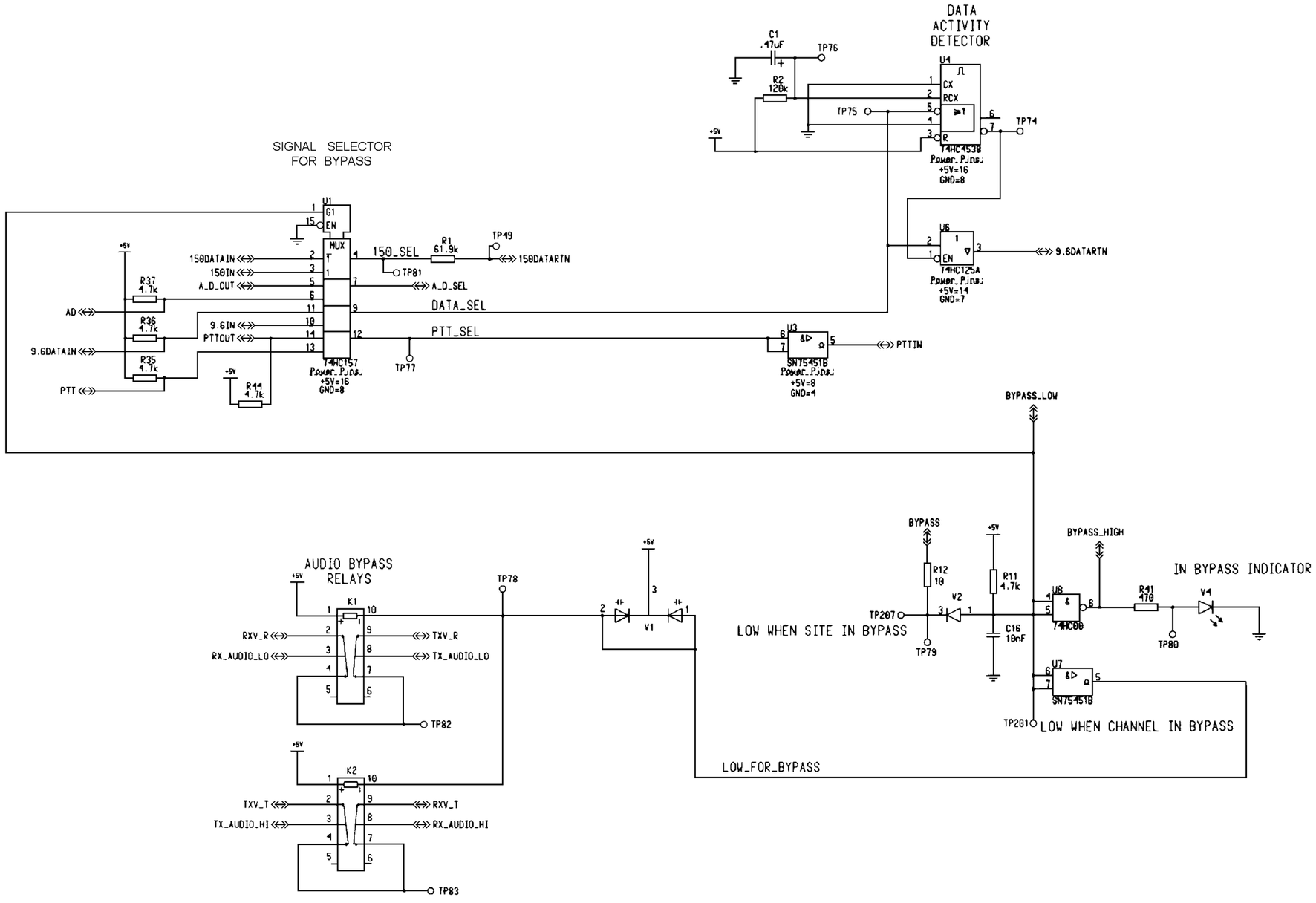
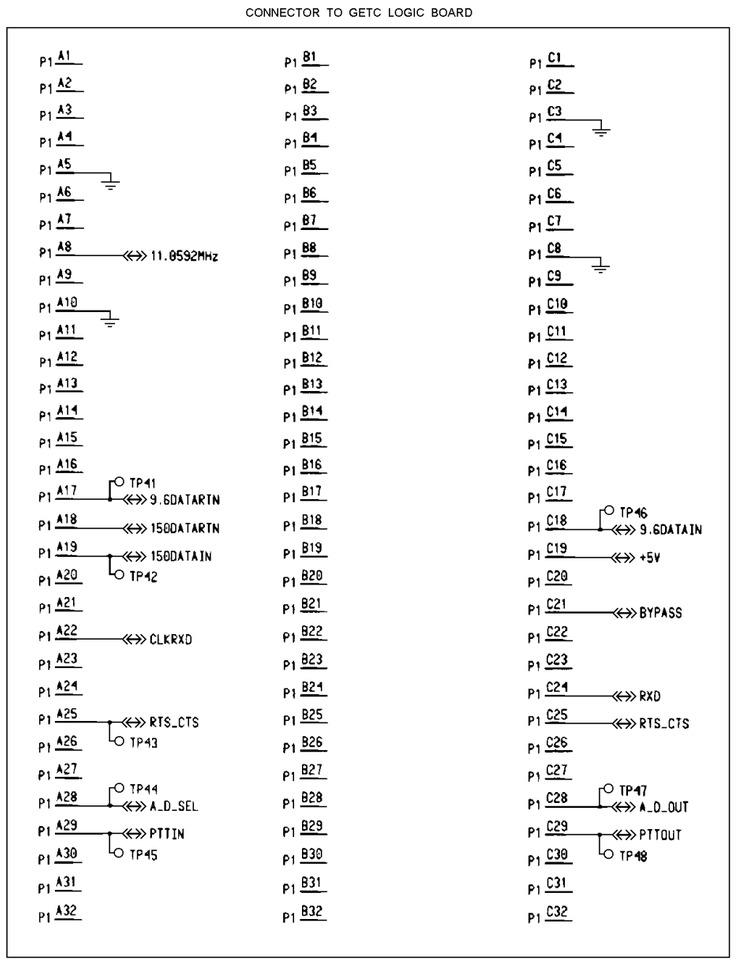
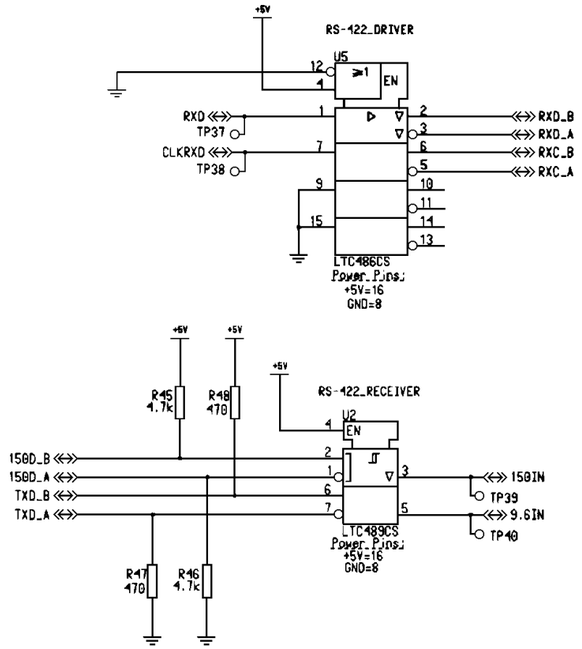
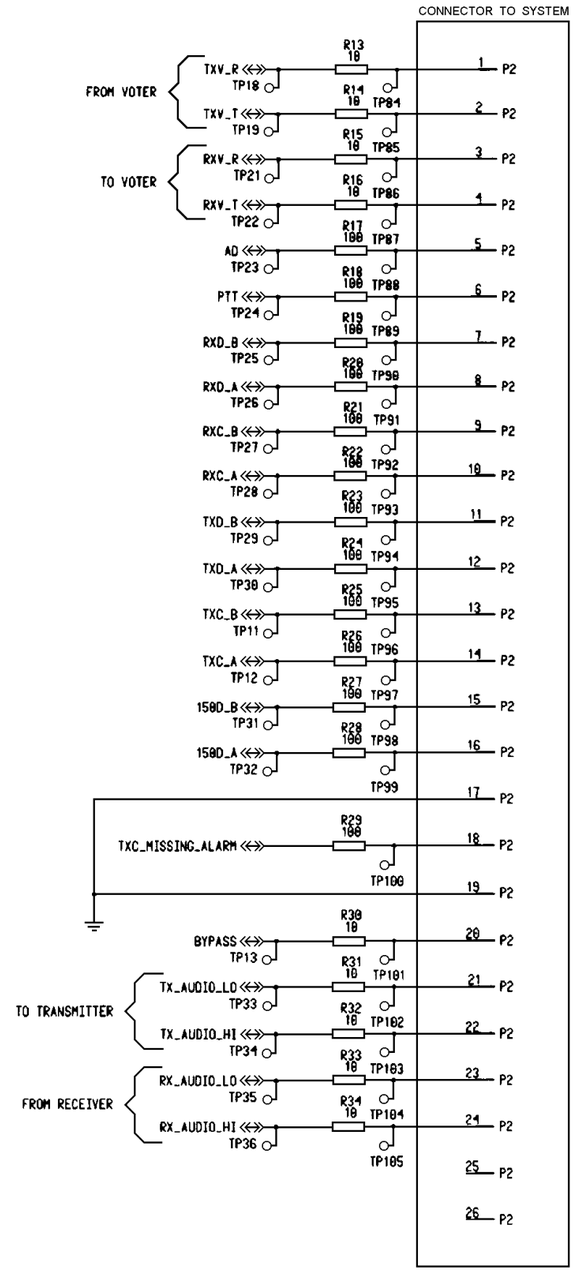


NOTE: IN BYPASS RX_AUDIO_LO CONNECTS TO TX_AUDIO_LO
AND
TX_AUDIO_HI CONNECTS TO RX_AUDIO_HI

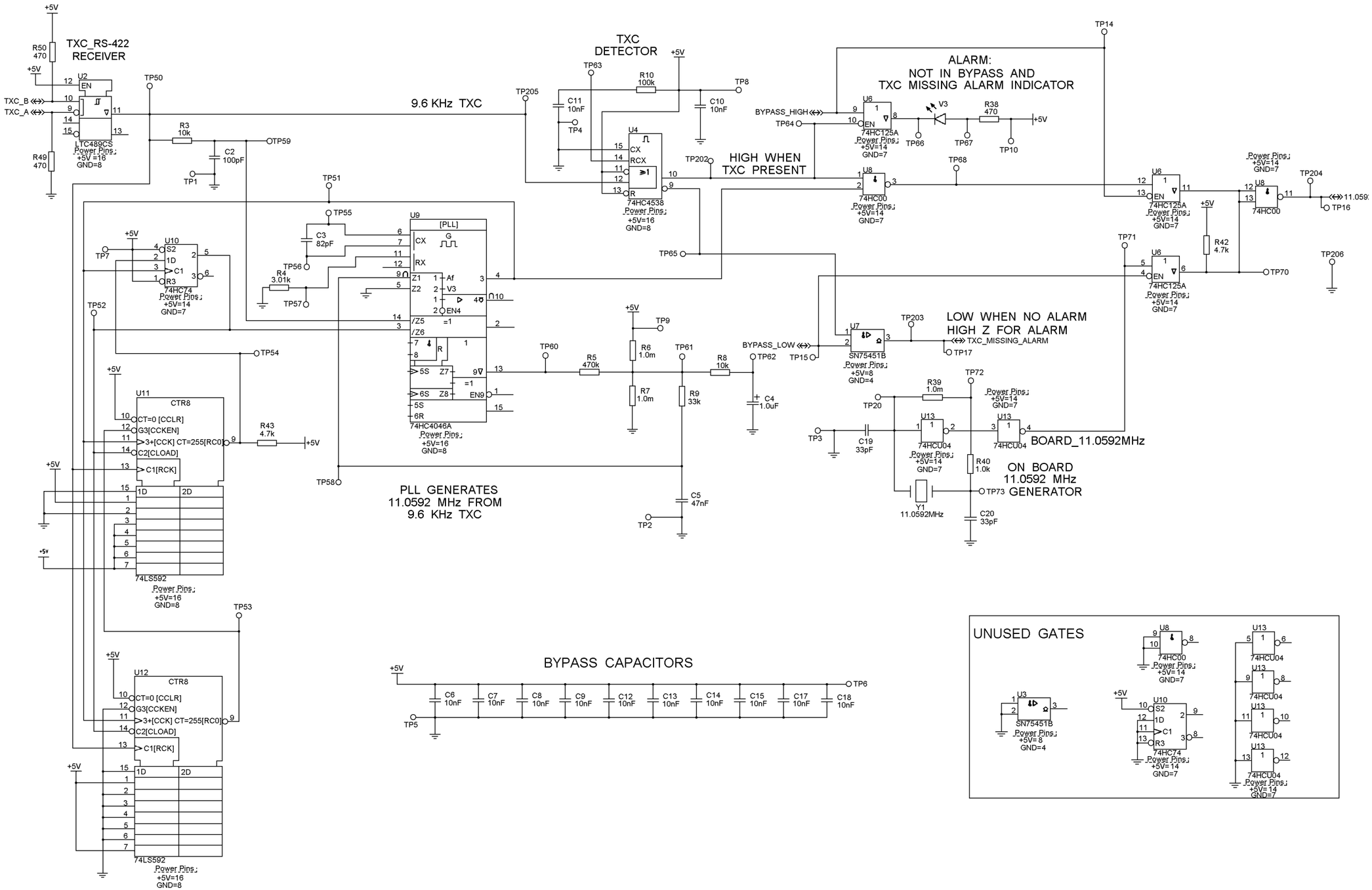
(1911 ROA 117 2269, Sh. 3, Rev. B)





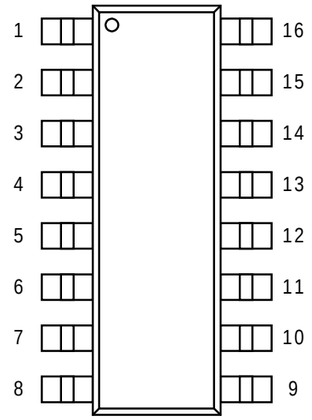


(1911 ROA 117 2269, Sh. 2, Rev.B)



(1911 ROA 117 2269, Sh. 1, Rev. B)

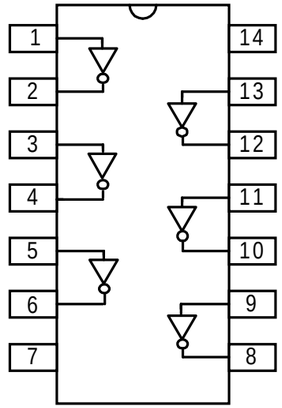
8-BIT BINARY COUNTER U11, U12
RYT2226014/C *(74LS592)*



CONNECTIONS

Terminal	Symbol	Function
1	B	Input B
2	C	Input C
3	D	Input D
4	E	Input E
5	F	Input F
6	G	Input G
7	H	Input H
8	GND	Ground
9	$\overline{\text{RCO}}$	Output
10	$\overline{\text{CCLR}}$	Output
11	CCK	Counter clear input
12	$\overline{\text{CCKEN}}$	Clock enable input
13	RCK	Registerclock input
14	$\overline{\text{CLOAD}}$	Counter load input
15	A	Input A
16	Vcc	Supply Voltage

HEX INVERTER (Unbuffered U13
RYT3066045/C *(74HCU04)*



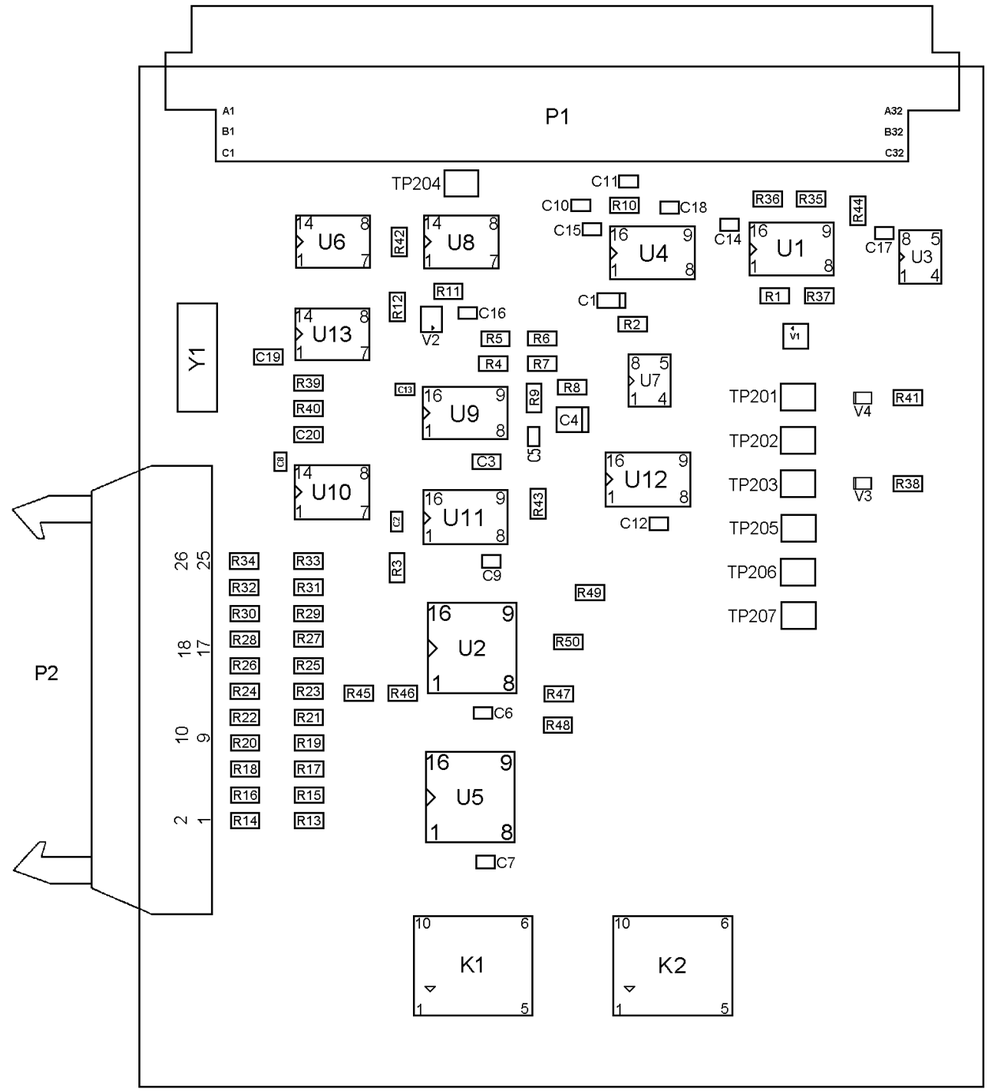
FUNCTION TABLE

Input	Output
H	L
L	H

H = High level (Steady state)
L = Low level (Steady state)

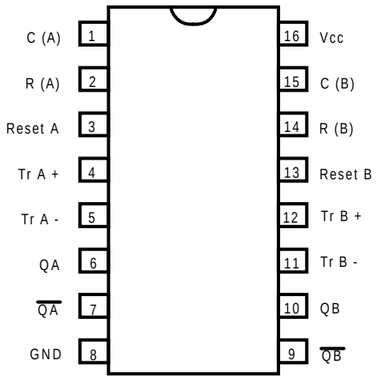
CONNECTIONS

Terminal	Symbol	Function
1	1A	Input
2	1Y	Output
3	2A	Input
4	2Y	Output
5	3A	Input
6	3Y	Output
7	GND	Ground
8	4Y	Output
9	4A	Input
10	5Y	Output
11	5A	Input
12	6Y	Output
13	6A	Input
14	Vcc	Supply Voltage



(1078 ROA 117 2269, Rev. B)

DUAL TRIGGERABLE MONSABLE MULTIVIBRATOR U4
RYT3062024/C *(74H4538)*



Inputs			Outputs	
Reset	**+ Trigg**	**- Trigg**	**Q**	**/Q**
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↑	H	⎍	⎎

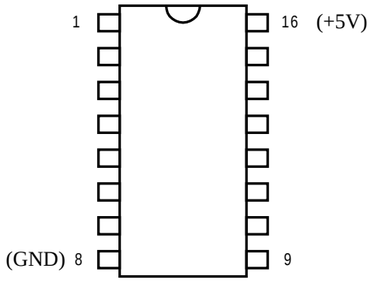
↓

X = H or L

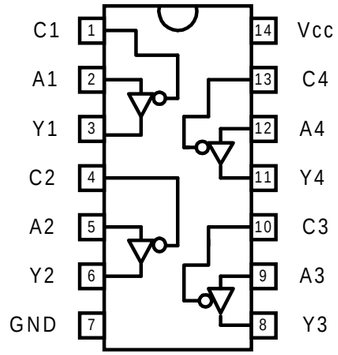
↑ = from L to H

↓ = from H to L

QUAD RS-485 LINE DRIVER U5
RYT 1096078/1C *(LTC486)*

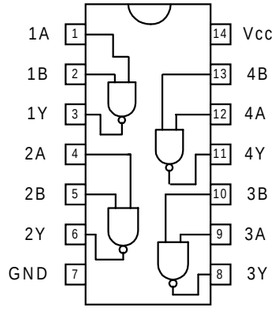


QUAD TRI-STATE BUFFER U6
RYT3066029/C *(74HC125)*



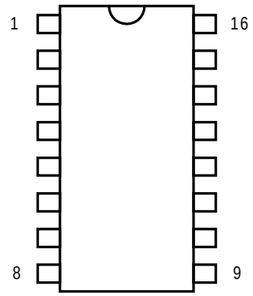
Inputs		Outputs
A	**C**	**Y**
H	L	H
L	L	L
X	H	Z

QUAD NAND GATE U8
RYT3062001/C (74HC00)



Positive Logic: $Y = \overline{A \bullet B}$

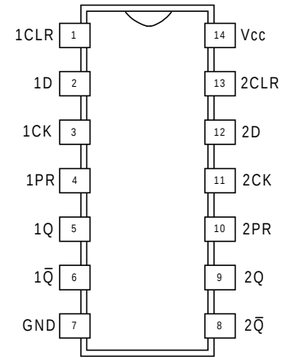
PHASE-LOCKED-LOOP U9
RYT3066057/C *(74HC4046)*



CONNECTIONS

Terminal	Symbol	Function
1	PCPout	Phase comparator pulse output
2	PC1out	Phase comparator 1 output
3	COMPin	Comparator input
4	VCOout	VCO output
5	INH	Inhibit input
6	C1A	Capacitor C1 connection A
7	C1B	Capacitor C1 connectioin B
8	GND	Ground
9	VCOin	VCO input
10	DEMout	Demodulator output
11	R1	Resistor R1 connection
12	R2	Resistor R2 connection
13	PC2out	Phase comparator 2 output
14	SIGin	Signal input
15	PC3out	Phase comparator 3 output
16	Vcc	Supply Voltage

D FLIP-FLOP U10
RYT3062003/C *(74HC74)*



Inputs			Outputs		
Preset	**Clear**	**Clock**	**D**	**Q**	**/Q**
l	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	/Q0

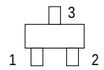
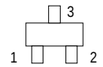
↑ = Transition from low to high level

Q0 = The level of Q after the previous clock pulse

* = Nonstable, don't preset when PR and CLR are set high

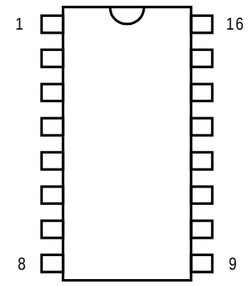
X = Any input, including transition

GETC INTERFACE BOARD
ROA 117 2269

SYMBOL	PART NUMBER	DESCRIPTION
		- - - -CAPACITORS- - - -
C1	RJE5843256/47	Tantalum: 0.47 µF ±4%, 25 VDCW.
C2	RJC4634043/1	Ceramic: 100 pF ±5%, 50 VDCW.
C3	RJC4634063/82	Ceramic: 82 pF ±5%, 50 VDCW.
C4	RJE5843357/1	Tantalum: 1 µF ±4%, 35 VDCW.
C5	RJC4643045/47	Ceramic: 0.047 µF ±10%, 50 VDCW.
C6 thru C18	RJC4643045/1	Ceramic: 0.01 µF ±10%, 50 VDCW.
C19 thru C20	RJC4634062/33	Ceramic: 33 pF ±5%, 50 VDCW.
		- - - -RELAYS- - - -
K1 and K2	RAV95405/S	Surface Mount, 5 V, 178 Ohms ±10%.
		- - - -CONNECTORS- - - -
P1	RPV403804/02	96 Pin Male Angled.
P2	RPV403143/226	26 Pin Header Angled.
		- - - -RESISTORS- - - -
R1	REP615625/619	61.9 k Ohms ±1%, ±100 PPM/°C.
R2	REP645626/12	120 k Ohms ±1%, ±100 PPM/°C.
R3	REP625425/1	10 k Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
R4	REP615624/301	3.01 k Ohms ±1%, ±100 PPM/°C.
R5	REP645626/47	470 k Ohms ±1%, ±100 PPM/°C.
R6 and R7	REP625427/1	1 M Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
R8	REP625425/1	10 k Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
R9	REP625425/33	33 k Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
R10	REP625426/1	100 k Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
R11	REP625424/47	4.7 k Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
R12 thru R16	REP625422/1	10 Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
R17 thru R29	REP625423/1	100 Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
R30 thru R34	REP625422/1	10 Ohms ±5%, ±200 PPM/°C, 1/8 Watt
R35 thru R37	REP625424/47	4.7 k Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
R38	REP625423/47	470 Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
R39	REP625427/1	1 M Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
R40	REP625424/1	1 k Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
R41	REP625423/47	470 Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
R42 thru R46	REP625424/47	4.7 k Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
R47 thru R50	REP625423/47	470 Ohms ±5%, ±200 PPM/°C, 1/8 Watt.
		- - - -TEST POINTS- - - -
TP201 thru TP207	RPV403813/01	Test points for board level trouble shooting.
		- -INTEGRATED CIRCUITS- -
U1	RYT3066052/C	Quad 2-Line To 1-LINE Data Selector, Sim to: 74HC157.
U2	RYT1096079/2C	Quad Low Power RS-485 Receiver, Sim to: LTC489.
U3 and U7	RYT1096064/C	Dual Peripheral driver, Sim to: SN75451B
U4	RYT3062024/C	Dual Retriggerable Monstable multivibrator, Sim to: 74HC4538.
U5	RYT1096078/C	Quad RS-485 Line Driver, Sim to: LTC486.
U6	RYT3066029/C	Quad Tri-State Buffer, Sim to: 74HC125.
U8	RYT3062001/C	Quad NAND, Sim to: 74HC00.
U9	RYT3066057/C	Phase-Locked-Loop, Sim to:74HC4046A.
U10	RYT3062003/C	D Flip-Flop, Sim to: 74HC74.
U11 and U12	RYT2226014/C	8-Bit Binary Counter, Sim to: 74LS592.
U13	RYT3066045/C	Hex Inverter (Buffered), Sim to: 74HC04.
		- - - -DIODES- - - -
V1	RKZUA32301/1	Dual variable capacitance diode:  1 - Anode 1 2 - Anode 2 3 - Common Cathode
V2	RKZ123601	Schottky Barrier Diode:  1 - Anode 2 - N.C. 3 - Cathode
V3 and V4	RKZ433634/10	Light Emitting Diode, plastic surface mount.
		- - - -CRYSTAL- - - -
Y1	RTM501659/02	11.0592 MHz XTAL

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

QUAD 2-LINE TO 1-LINE DATA SELECTOR U1
RYT306052/C *(74HC157)*



CONNECTIONS

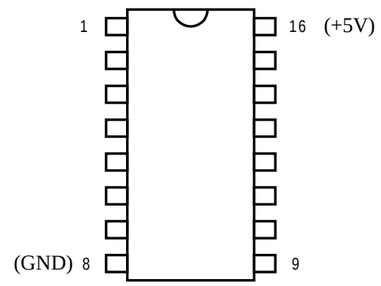
Terminal	Symbol	Function
1	S	Select input
2	A_0	Input 1
3	B_0	Input
4	Y_0	Output
5	A_1	Output1
6	B_1	Input2
7	Y_1	Input 2
8	GND	Ground
9	Y_2	Output 3
10	B_2	Input 3
11	A_2	Input 3
12	Y_3	Output 4
13	B_3	Input 4
14	A_3	Input 4
15	$\overline{OE}$	Output enable
16	Vcc	Supply Voltage

FUNCTION TABLE

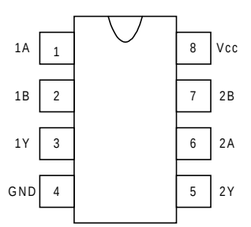
Inputs				Outputs
S	$\overline{OE}$	A	B	Yn
X	H	X	X	L
L	L	L	X	L
L	L	H	X	H
H	L	X	L	L
H	L	X	H	H

H=High level (Steady state)
L=Low level (Steady state)
X=Immaterial

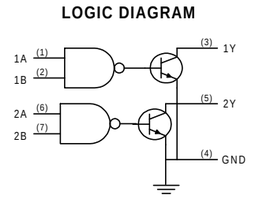
QUAD LOW POWER RS-485 RECEIVER U2
RYT1096079/2C *(LTC489)*



DUAL PERIPHERAL DRIVER U3, U7
RYT1096064/C *(SN75451B)*



LOGIC DIAGRAM



FUNCTION TABLE:

Inputs		Outputs
A	B	Y
L	L	L (on state)
L	HX	L (on state)
H	L	L (on state)
H	H	H (off state)

Positive Logic: Y = AB

ACTIVE TESTS

These tests are performed while applying clocks to the module. Make the following connections, which apply to all tests in this section:

1. Ground as indicated in table 2.
2. +5 power as indicated in table 2.
3. Set P1-A19 150DATAIN to HCTTL-H.
4. Tie P2-18 TXC_MISSING_ALARM to HCTTL-H through a 4.7k Ohm pull-up resistor.

Clocks Present In Non-Bypass Mode

This section tests the situation that clocks are input to the module and the module is not in bypass mode. The board is expected to have the following performance:

Table 8 - Tests for Clocks and Not In Bypass

Test	Performance	Verify
• Apply a 9600 Hz ± 10 Hz square wave with **+5v to -5v** swing to P2-13 (TXC_B) and ground to P2-14 (TXC_A).		
1.	Indicators show that the TXC clock is present and the board is not in bypass mode.	1. V3 (NOT IN BYPASS AND RXC MISSING INDICATOR) is not on (“ALARM”). 2. V4 (IN BYPASS INDICATOR) is not on (“BYPASS”). 3. TP201 (LOW WHEN IN BYPASS) is HCTTL-H. 4. TP202 (HIGH WHEN RXC PRESENT) is HCTTL-H. 5. TP203 (LOW WHEN NO ALARM HIGH Z WHEN ALARM) is HCTTL-L. 6. P2-18 TXC_MISSING_ALARM is HCTTL-L
2.	11.0592 MHz from the PLL is routed for output whenever RXC clocks are present	1. The frequency of the signal at P1-A8 11.0592 MHz is 1152 (to the nearest integer) times the frequency of P2-14 TXC_A & P2-13 TXC_B. 2. TP 204 (“11.0592 MHz”) is 1152 (to the nearest integer) times the frequency of P2-14 TXC_A & P2-13 TXC_B.
• Move the 9600 Hz ± 10Hz square wave with **+5v to -5v** swing to P2-16 (150D_A) and ground to P2-15(150D_B).		
3.	The Signal Selector for Bypass (*U1*) is set for non-bypass operation, so input signals (set to 9600 Hz clocks) are selected,and RS-422 rcvrs work.	1. P1-A18 (150DATARTN) is a 9600 Hz square wave at HCTTL levels.
• Move the 9600 Hz ± 10 Hz square wave with **+5v to -5v** swing to P2-12 (TXD_A) and ground to P2-11 (TXD_B).		
4.	The Signal Selector for Bypass (*U1*) is set for non-bypass operation, so input signals (set to 9600 Hz clocks) are selected and RS-422 recievers work.	1. P1-A17 (9.6DATARTN) is a 9600 Hz square wave at HCTTL levels.
• Move the 9600 Hz (±10 Hz) square wave with **+5v to -5v** swing to P2-13 TXC_B and ground to P2-14 TXC_B. • Connect 9600 Hz (±10 Hz) square wave with **+5v to 0** swing, present at TP205, to P1-C24 TXD.		
5.	*U5* RS-485 Driver is functional	1. Differential, 0-5v, 9600 Hz square waves are present at P2-7 (TXD_B) and P2-8 (TXD_A).
• Move the 9600 Hz ±10 Hz square wave with **+5v to 0** swing to P1-A22 (CLKTXD).		
6.	U5 RS-485 Driver is functional	1. Differential, 0-5v, 9600 Hz square waves are present at P2-9 (TXC_B) and P2-10 (TXC_A).

Clocks Present Bypass Mode

This test applies to the situation that clocks are input to the module and the module is in the bypass mode.

Make this connection in addition to those already made as follows:

1. Set P1-C21 or P2-20 (BYPASS) to HCTTL-L.
2. Apply a 9600 Hz ±10 Hz square wave with **+5v to -5v** swing to P2-13 (TXC_B).
3. Connect Ground to P2-14 (TXC_A).

The board is expected to have the following performance:

Table 9 - Tests for Clocks and In Bypass

Test	Performance	Verify
1.	Indicators show the board is in bypass mode.	1. V3 (NOT IN BYPASS AND RXC MISSING INDICATOR) is not illuminated (“ALARM”). 2. V4 (IN BYPASS INDICATOR) is illuminated (“BYPASS”). 3. TP201 (LOW WHEN IN BYPASS) is HCTTL-L. 4. TP202 (HIGH WHEN TXC PRESENT) is HCTTL-H. 5. TP203 (LOW WHEN NO ALARM HIGH Z WHEN ALARM) is HCTTL-L. 6. P2-18 TXC_MISSING_ALARM) is HCTTL-L
2.	11.0592 MHz from the on-board clock oscillator (Y1) is routed for output whenever in bypass.	1. P1-A8 11.0592MHz is present (11.0592 MHz ±1000 Hz). 2. TP204 (11.0592MHZ) is 11.0592 MHz ±1000 Hz .
3.	The Signal Selector for Bypass (*U1*) is set for bypass operation, so input signals (set to HCTTL-H) are selected.	1. P1-A18 (150DATARTN) is HCTTL-H.
4.	*U4* Data Activity Detector is working and 9.6DATARTN is selected by *U1*.	1. Connect and remove P1-C18 (9.6DATAIN) to ground and inspect a resulting HCTTL-H pulse on P1-A17 (9.6DATARTN) which is 35-45 mSec in length.

TEST AND TROUBLESHOOTING

TEST POINTS AND INDICATORS

The assembly has test points for testing by manufacturing and service technician personnel. The manufacturing test points are small pads on the secondary (non-component) side of the board, and are numbered TPXXX, where XXX is less than 200. The technician test points are on the primary (component) side of the board, are small wire loops allowing easy connection of test equipment, and are numbered TP201-TP207. Both forms of test points appear on the schematic, but the technician test points are in a larger print to make locating them more easy.

There are two LED's on the board to indicate the important conditions of bypass mode (V4) and loss of TXC while not in bypass (V3). The words "BYPASS" and "ALARM" are silk-screened near these components for reference.

Table 6 below summarizes the test points and their associated LED indicators.

Table 5 - Test Points and Associated LED Indicators

Test Point Number	Associated LED	Description
TP201	V4	TP is logic low and the LED is lit when bypass is active. Otherwise, TP is logic high and the LED is off. "BYPASS" is printed on the board near theLED. This TP pulls this station only into bypass.
TP202	none	TP is logic high when TXC is present (as detected by *U4*) and logic low otherwise.
TP203	V3	TP is high impedance and the LED lights when TXC is not present when the board is in normal (non-bypass) mode. If TXC is present or the board is in bypass, the LED is off and the TP is logic low. The signal at the TP is equivalent to the TXC_MISSING_ALARM output by the GETC Interface assembly. "ALARM" is printed on the board near the LED.
TP204	none	11.0592 MHz HCTTL clock. This clock may be generated by the PLL (normal operation) or on board oscillator circuit (bypass operation).
TP205	none	9.6 KHz TXC: HCTTL square wave, prior to input to the U4 TXC detector and the PLL.
TP206	none	ground
TP207	none	TP is logic low when in site bypass and logic high otherwise. This TP can be used to pull an entire site into bypass.

TEST EQUIPMENT

The following test equipment is necessary for board test.

- Oscilloscope: Tektronix 2230 or equivalent
- Digital function generator: HP 8116A or equivalent
- +5v power supply: Power Design Inc TP325 or equivalent
- Ohm meter
- Frequency Counter: HP 5385A or equivalent

TEST PROCEDURES

The following test procedures should be performed in the order indicated to ensure proper operation of the board.

Continuity Test

To verifiy that +5 Volts and ground are not shorted, refer to Table 2 and verify that +5 Volts power is not shorted to ground.

Stationary Tests

These tests are performed without applying clocks to the module. Make the following connections, which apply to all tests presented in this manual.

1. Ground as indicated in Table2.

2. +5v power as indicated in Table 2.

3. Set A_D_OUT to HCTTL-L (P1-C28).

4. Set PTTOUT to HCTTL-L (P1-C29).

No Clocks Present In Non-Bypass Mode

This test is applicable when no clocks are input to the module and the module is not in bypass mode. The board is expected to have the following performance:

Table 6 - Tests for No Clocks and Not In Bypass

Test	Performance	Verify
1.	Indicators show that the TXC clock is not present and the board is not in bypass mode.	1. V3 (NOT IN BYPASS AND TXC MISSING INDICATOR) is lighted ("ALARM"). 2. V4 (IN BYPASS INDICATOR) is not lighted ("BYPASS"). 3. TP201 (LOW WHEN IN BYPASS) is HCTTL-H. 4. TP202 (HIGH WHEN TXC PRESENT) is HCTTL-L. 5. TP203 (LOW WHEN NO ALARM HIGH Z WHEN ALARM) is HCTTL-H. 6. P2-18 TXC_MISSING_ALARM is HCTTL-H.
2.	No 11.0592 MHz clock is output if TXC is not present and module is not in bypass.	1. P1-A8 (11.0592 MHz) 11.0592 MHz ±1000 Hz is not present 2. TP204 (11.0592MHz) 11.0592 MHz ±1000 Hz is not present..
3.	The audio bypass relays (K1, K2) are set for non-bypass operation	1. P2-23 (RX_AUDIO_LO) to P2-3 (RXV_R) is 20 Ohms ± 1 Ohm. 2. P2-24 (RX_AUDIO_HI) to P2-4 (RXV_T) is 20 Ohms ± 1 Ohm. 3. P2-21 (TX_AUDIO_LO) to P2-1 (TXV_R) is 20 Ohms ± 1 Ohm. 4. P2-22 (TX_AUDIO-HI) to P2-2 (TXV_T) is 20 Ohms ± 1 Ohm.
4.	The Signal Selector for Bypass (U1) is set for non-bypass operation, so input signals A_D_OUT and PTTOUT (set to HCTTL-L) are not selected	1. P1-A29 (PTTIN) is HCTTL-H. 2. P1-A28 (A_D_SEL) is HCTTL-H.

No Clocks Present Bypass Mode

This test is applicable when no clocks are input to the module and the module is in bypass mode.

In addition to those connections already made, set P1-C21 or P2-20 (BYPASS) to HCTTL-L (relays K1 and K2 will click).

The board is expected to have the following performance:

Table 7 - Tests for No Clocks and In Bypass

Test	Performance	Verify
1.	Indicators show that the TXC clock is not present and the board is in bypass mode.	1. V3 (NOT IN BYPASS AND RXC MISSING INDICATOR) is not lighted ("ALARM"). 2. V4 (IN BYPASS INDICATOR) is lighted ("BYPASS"). 3. TP201 (LOW WHEN IN BYPASS) is HCTTL-L. 4. TP202 (HIGH WHEN RXC PRESENT) is HCTTL-L. 5. TP203 (LOW WHEN NO ALARM HIGH Z WHEN ALARM) is HCTTL-L. 6. P2-18 TXC_MISSING_ALARM is HCTTL-L.
2.	11.0592 MHz from the on-board clock oscillator (Y1) is routed for output whenever no TXC clocks are present	1. P1-A8 (11.0592MHz) is present (11.0592 MHz ±1000 Hz). 2. TP204 (11.0592MHz) is 11.0592 MHz ±1000 Hz.
3.	The audio bypass relays (K1, K2) are set for bypass operation	1. P2-23 (RX_AUDIO_LO) to P2-21 (TX_AUDIO_LO) is 20 Ohms ± 1 Ohm. 2. P2-24 (RX_AUDIO_HI) to P2-22 (TX_AUDIO_HI) is 20 Ohms ± 1 Ohm.
4.	The Signal Selector for Bypass (*U1*) is set for bypass operation, so input signals A_D_OUT and PTTOUT (set to HCTTL-L) are selected.	1. P1-A29 PTTIN is HCTTL-L. 2. P1-A28 A_D_SEL is HCTTL-L.

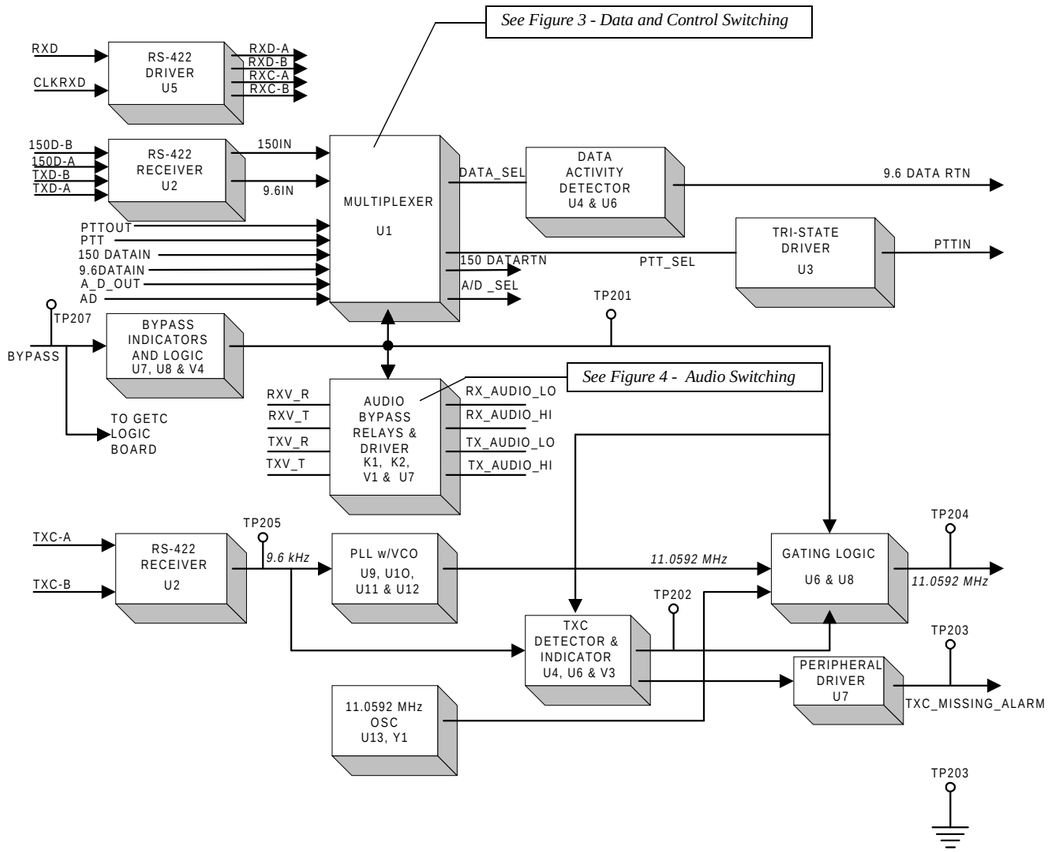


FIGURE 2 - GETC INTERFACE BLOCK DIAGRAM

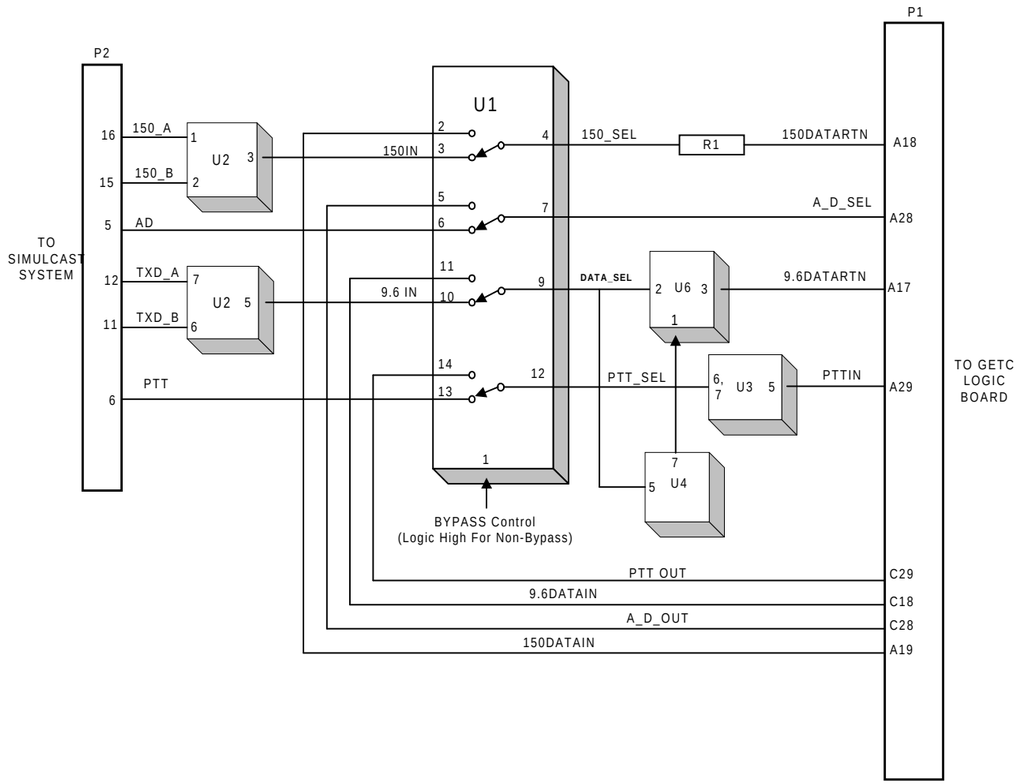


FIGURE 3 - DATA AND CONTROL SWITCHING
(Shown in the Non-Bypass Mode)

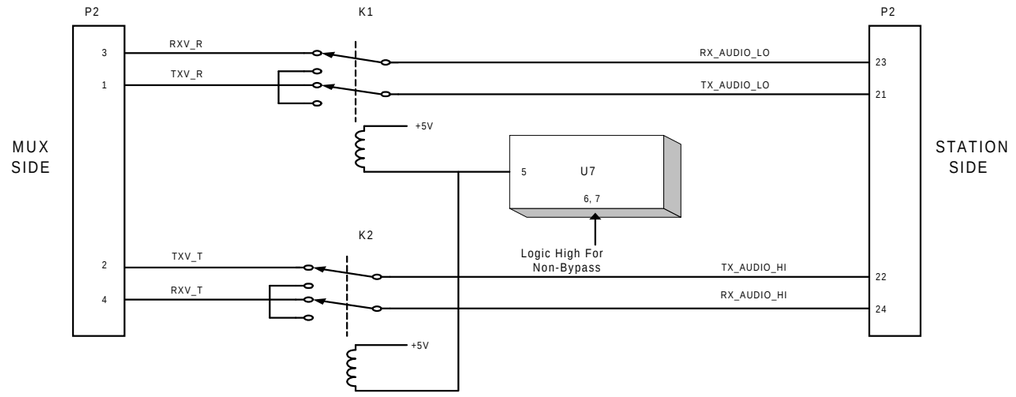


FIGURE 4 - AUDIO SWITCHING
(Shown in Normally Closed Non-Bypass Position)

RTS_CTS P1-A25, P1-C25:

RTS_CTS loops back the GETC logic board **R**equest **T**o **S**end (**RTS**) on P1-A25 to the GETC logic board **C**lear **T**o **S**end (**CTS**) on P1-C25:

150 BPS Data

150D_B, 150D_A (P2-15,16):

150D is a 150 BPS data stream from the simulcast system, originating from the control point. The data is converted from RS-422 (A and B) to TTL.

150DATAIN (P1-A19):

The 150 DATAIN is a 150 BPS data stream output from the GETC. This data is derived from a WALSH BIT generator on the GETC.

150DATARTN (P1-A18):

150 DATARTN is a 150 BPS data stream for “on-air” transmission by this station. The data comes from 150D in normal operation or 150DATAIN in bypass operation.

Push to Talk (PTT)

PTT (P2-6):

PTT is a push-to-talk control signal from the simulcast system, originating from the control point.

PTTOUT P1-C29:

PTTOUT is a push to talk control signal from the GETC logic board.

PTTIN - P1-A29:

PTTIN is the push to talk control signal into the GETC logic board. It is derived from PTT in normal operation and PTTOUT in bypass operation. It is converted into an open collector signal by U3.

Audio/Digital (A/D) signals

AD - P2-5:

AD is the A/D control line from the simulcast system.

A_D_OUT - P1-C28

A_D_OUT is the A/D control line from the GETC logic board signal A/DOUT.

A_D_SEL - P1-A28:

A_D_SEL is the A/D control line into the GETC logic board. It is used by the GETC for modulation path control, enabling either the audio and low speed data paths, or the high speed data path. A_D_SEL is derived from AD in normal operation and A_D_OUT in bypass operation.

Bypass

BYPASS - P2-20, P1-C21:

The active low bypass control line, BYPASS, is used to re-route certain paths on the GETC interface module. It serves to re-route the 9600 BPS data, the 150 BPS data, the A/D control line, and the PTT control line, all of which are directed back to the GETC logic board. There is also a voice bypass circuit which allows the audio to be interrupted and receive voice to be sent back to the station via relay K1, when in bypass mode. Figures 3 & 4 show the bypass modes of operation.

POWER DISTRIBUTION AND FILTERING

Power used by the GETC interface module is derived from the GETC logic board +5 Vdc and GND (0 volts). There are power bypass capacitors on the GETC interface module to filter any power noise transients or spikes from affecting circuit operation and module performance.

PHASE LOCKED 11.0592 MHz CLOCK

The GETC interface module generates an 11.0592 MHz clock from a reference 9600 Hz clock. This is accomplished by the digital Phase-Lock-Loop (PLL) and voltage controlled oscillator, U9. A divide by N prescaler consisting of 8-bit counters, U11 and U12, along with the synchronizing register, U10, perform the proper divide down of the 11.0592 MHz generated clock to compare against the reference 9600 Hz clock from the Simulcast System.

The reference clock, TXC_A and TXC_B, is converted from RS-422 to TTL via the level translator U2. Resistor R3 and capacitor C2 provide filtering and delay on the reference TTL clock for input to the PLL and VCO, U9. The other comparison input to the PLL and VCO is the output of the synchronizing register, U10.

The PLL and VCO, U9, is a self contained digital phase-lock-loop and voltage controlled oscillator. Resistor R4 and capacitor C3 set up the center running frequency of the voltage controlled oscillator. Resistors R5, R6, R7, R8, R9 and capacitors C4 and C5 comprise the loop filter of the PLL which sets up the capture range (frequency lock range).

The generated 11.0592 MHz clock is input to 8-bit counters, U11 and U12, along with the synchronizing register, U10. The counters are asynchronously reloaded with FA82 Hex via the active low output of register U10.

In a free running mode of operation (with the inputted 9600 reference clock), components U10, U11, and U12 count from FA82 Hex to FF01 Hex.

The total number of counts per cycle needed to produce the compare pulse (output of register U10) for input to the PLL is calculated below in Hex:

Final Count Before Repeat	FF01
Inital Count (Pre-loaded)	-FA82
Count Difference	47F
One Clock For Load	+1
Total	480

The quantity 480 (HEX) is equal to 1152 (DEC). This value compares with the desired divide by number (where 11.0592 MHz divided by 1152 equals 9600 Hz).

CLOCK SELECTION

The 11.0592 MHz clock output by this assembly may originate from the PLL circuit (U9, U10, U11, U12), may be generated by the on-board oscillator circuit (Y1, U13), or may be disabled. Logic within U8 and U6 determine the output state, depending on the state of bypass and the TXC detector (U4). The PLL source is selected if the assembly is not in bypass, and the TXC detector indicates that TXC is present. The oscillator is selected if the assembly is in bypass. If the assembly is not in bypass, and the TXC is not present (as determined by U4), then an error condition is present, and logic low is output in place of the 11.0592 MHz.

DESCRIPTION

This version of the **G**eneral **E**lectric **T**runking **C**ard (**GETC**) interface module is used in the EDACS® GPS Simulcast System at transmit sites. It provides signal level conversion, clock synchronization, bypass, and remote control functions for those signals whose source or destination is the GETC. Note that other, different GETC interface modules are used at GPS Simulcast control points, and throughout RS-232 version Simulcast systems.

The GETC interface module physically mounts in the station GETC shelf assembly of the EDACS trunked radio system. The GETC interface module plugs into the GETC logic board at GETC connector J3. This is the location where the 9600 baud modem option of the GETC shelf assembly normally mounts (Refer to Figure 1).

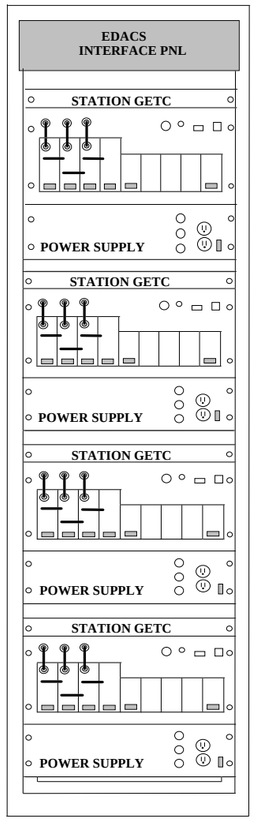


Figure 1 - GPS Simulcast MASTR III Station

The GETC Interface module buffers signals between the GETC logic board and the rest of the simulcast modules. The buffered signals include the 9600 Hz data clock (in and out), 9600 baud data (in and out) 150 baud data (in and out), modem handshaking lines (RTS/CTS), audio/digital (A/D) path select line (in and out), and push-to-talk line (in and out).

The GETC interface module uses the 9600 Hz transmit clock reference from the simulcast system to generate the 11.0592 MHz clock that is used to drive the GETC logic board. An on-board 11.0592 MHz oscillator is also available to drive the GETC logic board if the 9600 Hz clock is not present, or the transmit site is in bypass.

CIRCUIT ANALYSIS AND FUNCTIONAL DESCRIPTION

The GETC interface module provides signal, data, and clock level conversion (TTL to RS-422 and RS-422 to TTL), an alternate path for local control, data and clock lines (via the **BYPASS** line), and a GETC clock that is generated from the transmit reference clock.

The GETC interface module converts RS-422 level signals from the simulcast system to TTL signals for the GETC logic board. It also converts TTL signals from the GETC logic board to RS-422 for the simulcast system. The TTL and RS-422 levels are as follows:

TTL-High	3 to 5 Volts
TTL-Low	0 to 0.8 Volts
RS-422	±7 Volts

The industry standard RS-422 level is a differential voltage, the maximum (high) being +7 volts and the minimum (low) being -7 volts. In the GETC Interface Module application, the RS-422 voltage levels measured will be more like 0 to 5 volts.

RS-422 is a voltage differential specification. A logical “1” is represented by the “A” conductor being more negative than the “B” conductor. A logical “0” is represented by the “A” conductor being more positive than the “B” conductor.

The GETC interface module generates a 11.0592 MHz clock from a reference 9600 Hz transmit clock. This is accomplished using a Phase-Locked Loop (PLL) and a voltage controlled oscillator with a divide-by N prescaler. An on board 11.0592 MHz oscillator is used when the transmit clock is not present, or the transmit site is in bypass.

A pair of relays performs switching of tip and ring audio lines for normal and bypass operation.

There are no jumpers or adjustments on the GETC interface module. The hardware on the GETC interface module is comprised of the following:

- One quad RS-422 driver *(U5)* to buffer signals from the GETC logic board to the cross connect panel
- One quad RS-422 receiver *(U2)* to buffer signals from the cross connect panel to the GETC logic board
- Two peripheral drivers *(U3 & U7)* to drive the relays, buffer push-to-talk to the GETC logic board and output an alarm to the system
- Two relays *(K1 & K2)* to provide bypass switching for audio lines
- One quad two to one mux *(U1)* to select alternate paths for bypass control
- Two eight bit counters *(U11 & U12)* used for the PLL prescaler
- One D type flip flop *(U10)* used in the PLL
- One digital PLL/VCO *(U9)* used in the PLL
- One dual multivibrator *(U4)* for the 9600 baud tristate control and detection of RX clock absence
- One tri-state buffer driver *(U6)* and one quad NAND *(U8)* used for signal gating and logic signaling
- One hex unbuffered inverter *(U13)* used with the 11.0592 crystal to create an oscillator

General block diagrams of the GETC interface module are shown in Figures 2, 3 & 4.

There are two connectors used to connect the GETC interface module to components of the Simulcast System, P1 and P2. Connector P1 provides the interface with the logic board. A description of the various signals, data and clocks used between the two modules is summarized in Table 3. Connector P2 provides the interface with the Simulcast System. A description of the various signals, data, and clocks used between the GETC interface module and the cross connect panel is summarized in Table 4.

A series of 100 ohm and 10 ohm resistors (R13 through R34) are connected in series with the GETC interface board I/O lines to provide protection against surge currents that may occur.

Pull-up resistors R45 and R48 and Pull-down resistors R46 and R47 are used on RS-422 receiver (U2) inputs to force known logic level inputs when inputs are open, and for proper line termination.

SIGNAL FLOW

Clocks

Transmit Clock (TXC_B, TXC_A) P2-13,14:

A transmit clock is distributed to the GETC interface board from the simulcast system. This RS-422 (A and B) reference clock operates at 9600 Hz and is used by the GETC interface module to generate the 11.0592 MHz clock which is sent to the GETC to provide the clock used for synchronization.

11.0592 MHz Clock (P1-A8):

The 11.0592 MHz clock is generated on the GETC interface board by a phase-locked-loop oscillator or an on-board crystal oscillator circuit. The phase-locked-loop oscillator is referenced to the TXC clock for system stability. The 11.0592 MHz clock is then input to the GETC logic board. The corresponding clock on the GETC logic board is called MCLK.

9600 BPS Data

TXD_B, TXD_A (P2-11,12):

TXD is 9600 BPS data from the simulcast system (originates from the control point). The data is converted from RS-422 levels (A and B) to TTL.

9.6DATAIN (P1-C18):

The 9.6DATAIN is a 9600 BPS data stream output from the GETC. This data is derived from the RF modem, U4, on the GETC Logic Board.

9.6DATARTN (P1-A17):

9.6DATARTN is a 9600 BPS data stream for on-air transmission by this station. The data comes from TXD in normal operation or 9.6DATAIN in bypass mode.

RXD - P1-C24, RXD_A - P2-8, RXD_B - P2-7:

RXD data is a 9600 BPS data stream output from the GETC. This data is derived from the phone modem U19 on the GETC. RXD is converted from TTL to RS-422 (RXD_A, RXD_B) and sent to the simulcast system.

CLKRXD - P1-A22, RXC_A - P2-10, RXC_B - P2-9:

The CLKRXD clock is a 9600 Hz square wave output from the GETC. This clock is generated on the GETC phone modem U19 and converted from TTL to RS-422 (RXC_A, RXC_B) and sent to the simulcast system.

SPECIFICATIONS

GENERAL

Table 1 - General Specifications

Item	Specification
Input Voltages	+5 Volts +/- 10%
Temperature	-30°C to +60°C
Dimensions	3.93 X 4.725 inches
Digital/Data Type	HCTTL (0 to 5 volts) RS-422A (-7 to +7 volts)
Analog/Audio Type	None

POWER AND GROUND

Table 2 - Power and Ground Specifications

Voltage	Connector Point	Tolerance +/- %	Current Drain Typical mA
+5	P1-C19	10	225 mA BYPASS 150 mA NON-BYPASS
Ground	P1-A5 P1-A10 P1-C3 P1-C8	N/A	N/A

CONNECTOR P1 DEFINITION

P1 is a 96 pin connector (three rows, A, B, C of 32) which is used to interface to the GETC Logic Board. Any pin that is not listed below is a no connect.

Table 3 - Connector P1 Definitions

Connector Pin	Signal Name	Input/Output	Analog/Digital	Level
P1-A5	GROUND	I/O	D	0 Volts
P1-A8	11.059MHz	O	D	HCTTL
P1-A10	GROUND	I/O	D	0 Volts
P1-A17	9.6DATARTN	O	D	HCTTL
P1-A18	150DATARTN	O	D	HCTTL
P1-A19	150DATAIN	I	D	HCTTL
P1-A22	CLKRXD	I	D	HCTTL
P1-A25	RTS_CTS	I/O	D	HCTTL
P1-A28	A_D_SEL	O	D	HCTTL
P1-A29	PTTIN	O	D	HCTTL-L or High Z

Continued

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Continued

Connector Pin	Signal Name	Input/Output	Analog/Digital	Level
P1-C3	GROUND	I/O	D	0 Volts
P1-C8	GROUND	I/O	D	0 Volts
P1-C18	9.6DATAIN	I	D	HCTTL-L & High-Z
P1-C19	+5V	I	D	+5Volts
P1-C21	BYPASS	O	D	HCTTL
P1-C24	RXD	I	D	HCTTL
P1-C25	RTS_CTS	I/O	D	HCTTL
P1-C28	A_D_OUT	I	D	HCTTL
P1-C29	PTTOUT	I	D	HCTTL

CONNECTOR P2 DEFINITIONS

P2 is a 26 pin connector to the outside simulcast system.

Table 4 - Connector P2 Definition

Connector Pin	Signal Name	Input/Output	Analog/Digital	Level
P2-1	TXV_R	I	A	-10 dBm
P2-2	TXV_T	I	A	-10 dBm
P2-3	RXV_R	O	A	-10 dBm
P2-4	RXV_T	O	A	-10 dBm
P2-5	AD	I	D	HCTTL-L & High-Z
P2-6	PTT	I	D	HCTTL
P2-7	RXD_B	O	D	RS-422
P2-8	RXD_A	O	D	RS-422
P2-9	RXC_B	O	D	RS-422
P2-10	RXC_A	O	D	RS-422
P2-11	TXD_B	I	D	RS-422
P2-12	TXD_A	I	D	RS-422
P2-13	TXC_B	I	D	RS-422
P2-14	TXC_A	I	D	RS-422
P2-15	150D_B	I	D	RS-422
P2-16	150D_A	I	D	RS-422
P2-17	GROUND			0 V
P2-18	TXC_MISSING_ALARM	O	D	HCTTL-L or High-Z
P2-19	GROUND			0 V
P2-20	BYPASS	I	D	HC TTL
P2-21	TX_AUDIO_LO	O	A	-10 dBm
P2-22	TX_AUDIO_HI	O	A	-10 dBm
P2-23	RX_AUDIO_LO	I	A	-10 dBm
P2-24	RX_AUDIO_HI	I	A	-10 dBm
P2-25	N/C			
P2-26	N/C			

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