MAINTENANCE MANUAL

GPS TIMING MODULE
ROA 117 2260/1, 2

TABLE OF CONTENTS

SPECIFICATIONS

Input Voltage	+5 Vdc 10%
Current Drain	67 Milliamps (Typical)
Operating Temperature	-30ºC to +60ºC
Dimensions	8.0 inches long x 4.0 inches wide
Connector P1	
+5 Vdc	A30, A31, B30, B31
Ground	A1, B1, C1, C12, A32, B32, C32

ERICSSON

Ericsson Inc.
Private Radio Systems
Mountain View Road
Lynchburg, Virginia 24502
1-800-528-7711 (Outside USA, 804-528-7711)

AE/LZB 119 1875 R1A
Printed in U.S.A.

Connector P1 Definition

Terminal	A	B	C
1	GND	GND	GND
2	REF 9600 OUT 1A	REF 9600 OUT 1B	
3	REF 9600 OUT 2A	REF 9600 OUT 2B	
4	REF 9600 OUT 3A	REF 9600 OUT 3B	
5	REF 9600 OUT 4A	REF 9600 OUT 4B	
6	REF 9600 OUT 5A	REF 9600 OUT 5B	
7	REF 9600 OUT 6A	REF 9600 OUT 6B	
8	COMP REF1 OUT 1A	COMP REF1 OUT 1B	RC_IN
9	COMP REF1 OUT 2A	COMP REF1 OUT 2B	RC_OUT
10	COMP REF1 OUT 3A	COMP REF1 OUT 3B	
11	COMP REF1 OUT 4A	COMP REF1 OUT 4B	
12	COMP REF1 OUT 5A	COMP REF1 OUT 5B	GND
13	COMP REF1 OUT 6A	COMP REF1 OUT 6B	COMP REF 1 IN A
14	COMP REF 2 OUT 1A	COMP REF 2 OUT 1B	COMP REF 1 IN B
15	COMP REF 2 OUT 2A	COMP REF 2 OUT 2B	COMP REF 2 IN A
16	COMP REF 2 OUT 3A	COMP REF 2 OUT 3B	COMP REF 2 IN B
17	COMP REF 2 OUT 4A	COMP REF 2 OUT 4B	GND
18	COMP REF 2 OUT 5A	COMP REF 2 OUT 5B	SEL 9600 OUT 1
19	COMP REF 2 OUT 6A	COMP REF 2 OUT 6B	SEL 9600 OUT 2
20	GPSA 9600 IN A	GPSA 9600 IN B	SEL 9600 OUT 3
21	GPSA 9600 IN A	GPSB 9600 IN B	SEL 9600 OUT 4
22	GPSA 300 IN A	GPSA 300 IN B	LAND LINE BACKUP
23	GPSB 300 IN A	GPSB 300 IN B	SEL 300 OUT 1
24	GPSA IPPS IN A	GPSA IPPS IN A	SEL 300 OUT 2
25	GPSB IPPS IN A	GPSB IPPS IN B	SEL 300 OUT 3
26	GPSA FREQ ALM IN	GPSA FREQ LOCK IN	SEL 300 OUT 4
27	GPSB FREQ ALM IN	GPSB FREQ LOCK IN	FSL IN
28	1544 CLK IN A	1544 CLK IN B	MAJOR ALM1 OUT
29	MINOR ALM1 OUT	MINOR ALM2 OUT	MAJOR ALM2 OUT
30	+5Vdc	+5Vdc	
31	+5Vdc	+5Vdc	
32	GND	GND	GND

NOTE

Repairs to this equipment should be made only by an authorized service technician or facility designated the supplier. Any repairs, alterations or substitution of recommended parts made by the user to this equipment not approved by the manufacturer could void the user's authority to operate the equipment in addition to the manufacturer's warranty.

NOTICE!

DESCRIPTION

Global **P**ositioning **S**atellite (**GPS**) Timing Module *ROA 117 2260* is used in the GPS Simulcast Synch Shelf. There are multiple Synch Shelves in the GPS Simulcast System, one at the Control Point and one at each Transmit Site. Each Synch Shelf has two GPS Timing modules, A and B. Each of these are fully redundant.

The Timing Module plugs into slots 9 & 10 of the Synch Shelf located at both the Control Point and the Transmit Site.

At the Control Point, the Timing Module is an ROA 117 2260/1 and the module at the Transmit Site is an ROA 117 2260/2. One difference is that there is a different PROM in socket XU1 with different programming used between the two locations. Also, front panel LED's and labels differ: **CPTM** for **C**ontrol **P**oint **T**iming **M**odule *(Figure 1)* and **TXTM** for **T**ransmit**(X) T**iming **M**odule *(Figure 2).*

The Timing Module has three functions. Each function, though related, is performed differently at each location, control point or transmit site. At the Control Point, these functions:

- Generate 300 Hz FSL (Frame Sync Line)
- Generate Composite References
- Select 9600 Hz Clocks

At the Transmit site, these functions:

- Select 9600 Hz clocks
- Recover references from composites
- Control T1 delay

Refer to Figures 1 and 2. The following is a description of the LED indicators found on the front panel of the modules.

- **PWR** - Green LED indicates when power is applied to the module.
- **ACTV** - Green LED indicates when this is the active module.
- **MAJ** - Red LED indicates when a major alarm condition exists.
- **MIN** - Yellow LED indicates when a minor alarm condition exist.
- **GPS** - Yellow LED indicates that there is no signal coming from the GPS receivers. This is at the Control Point.
- **LL** - Yellow LED, at the transmit site, indicates that there is no signal coming from the GPS receivers and the Land Line signals are being used.
- **FSL** - Yellow LED indicates there is a loss of the Frame Synch Line at the Control Point.
- **REF 2** - Yellow LED indicates when there is a loss of composite reference 2 at the Transmit Site.
- **PROG** - Switch resets PROM U1 and the Xilinx (FPGA) module U4 to the initial state.
- **TEST** - Connector is an RJ12, 8-Pin connector used for test purposes (Refer to **TEST AND TROUBLESHOOTING)**.

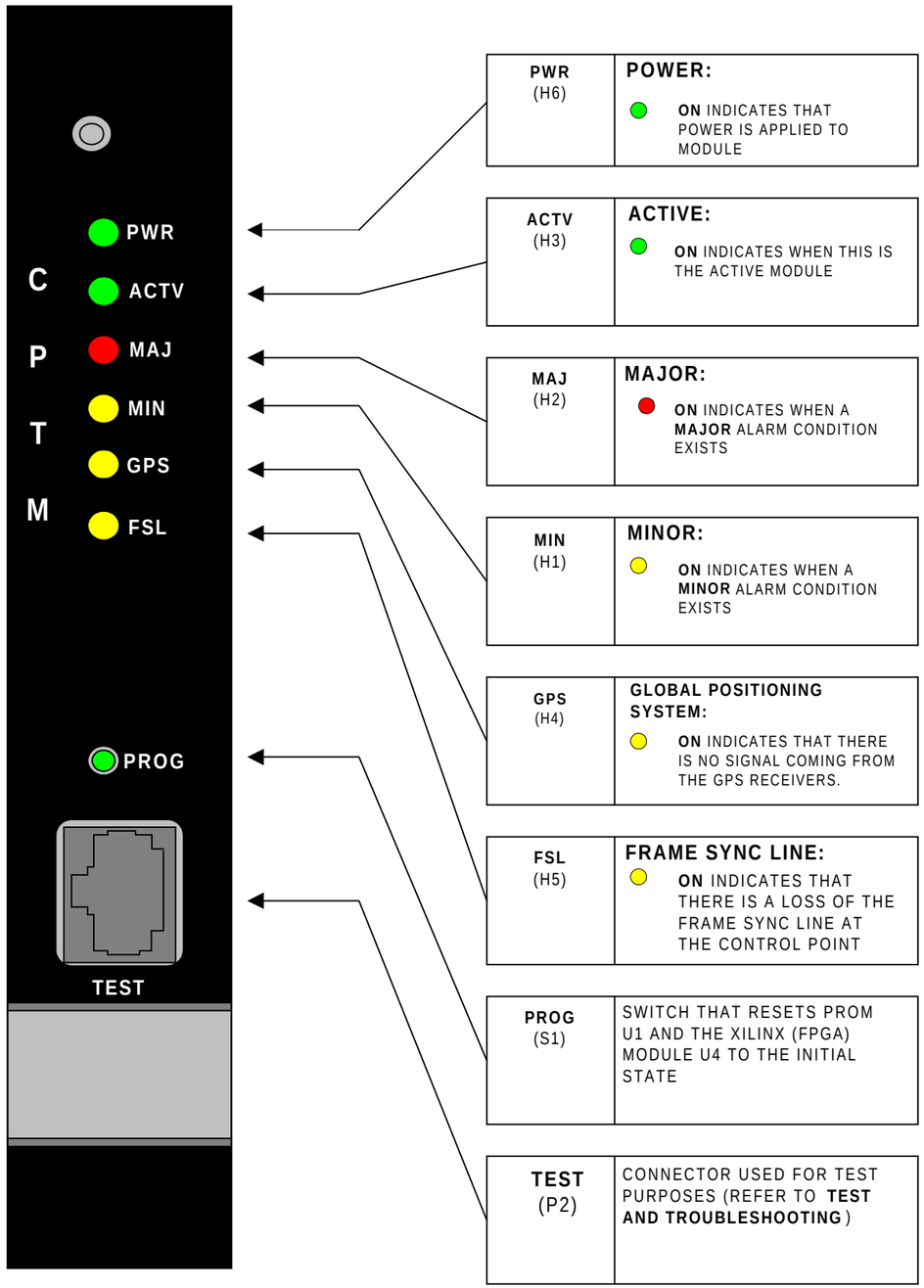


Figure 1 - Control Point Timing Module Front Panel

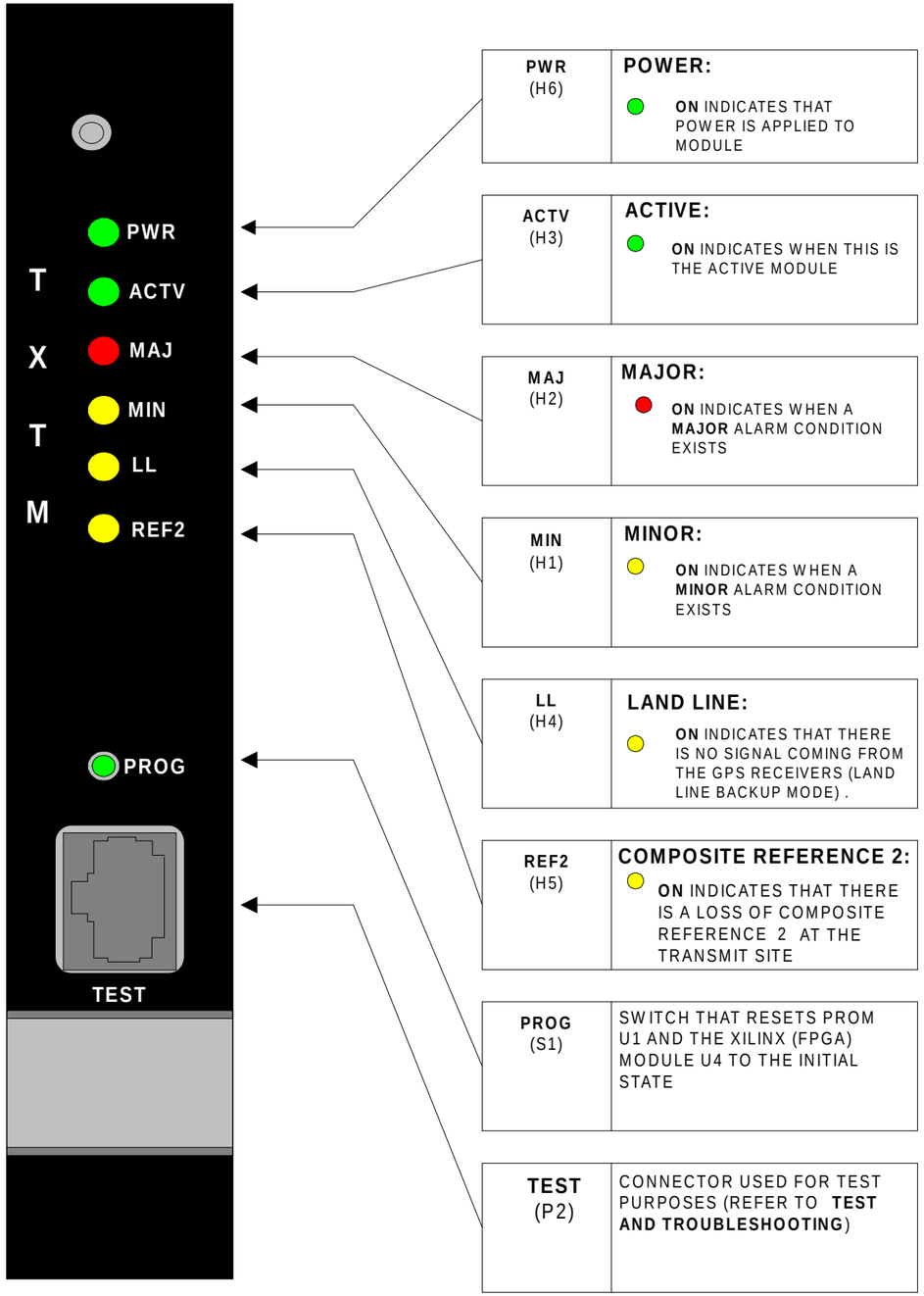


Figure 2 - Transmit Site Timing Module

CIRCUIT ANALYSIS

Functional circuitry is primarily contained in a Xilinx 3190A **FPGA** (**F**ield **P**rogrammable **G**ate **A**rray) integrated circuit (U4). This circuitry is programmed differently for control and transmit applications.

The GPS Timing module has hot standby capability. Circuitry outside the FPGA provides this capability as well as I/O interfaces and a **P**hase-**L**ock-**L**oop (**PLL**). The PLL is used at the transmit site.

Xilinx 3190A FPGA U4 is wired in master serial mode, which determines how programming is accomplished *(Figures 4 & 5)*. These figures are included for those familiar with Xilinx technology and are not described within this document.

At power up, following the release of the Reset/reprogram push-button switch S1, or following automatic detection of a Xilinx fault, data PROM U1 is read serially into U4. A watchdog function is performed by 555 timer, U5 in the Activity Detector circuit. This timer causes a reprogramming if the 9600 Hz selected clock is not provided by U4 (automatic Xilinx fault detection).

Crystal B1 provides a 4.9152 MHz clock used internally by the Xilinx logic.

This board operates from a single +5 volt supply. An onboard thermister fuse (F1) prevents module failure from causing this shelf supply to collapse.

Input signals arrive as RS-422 levels and are converted to TTL logic levels by RS-485 receivers U9, U11, and U14. Input fault lines connect directly to U4, as they arrive at TTL logic levels. The outputs driving the GPS ReSync modules (located in the same shelf) are buffered with tri-state line drivers U7, U13 and U15. The RS-422 level outputs are generated using RS-485 drivers U16-U20. The tri-state controls on all these drivers are used by the hot standby circuitry to turn the output to high impedance when the module is in hot standby. The circuitry attached to RC_IN and RC_OUT provides operational/hot-standby selection; these leads tie through the backplane to the companion module.

PLL U3 provides a de-jitter filter with zero phase shift on the recovered landline 9600 clock. This PLL is used only at the transmit site.

CONTROL POINT

The major functions performed at the Control Point are shown in Figure 3. The GPS signal selection block selects a 9600 clock and 1 pps signal from either of the redundant GPS locked clock sources. The Clock Generator block generates a 19200 Hz clock for use by the other blocks. The 300 Hz Generator generates the 300 Hz required by the ReSync by dividing the selected 9600 Hz by 32. It also ensures that the phase of this 300 Hz is proper relative to the **F**rame **S**ync **L**ine **(FSL)** input. The Composite Reference Generator takes the selected 9600 Hz clock and inserts tags at the proper times to create reference signals that contain:

- Composite Reference 1 contains 9600 Hz clock plus tags for 300 Hz and pseudo FSL.
- Composite Reference 2 contains 9600 Hz clock plus tags for 1 pps.

These Composite References are extracted at the transmit site. The 300 Hz generator and the Composite Reference Generator are implemented as state machines.

TRANSMIT SITE

The major functions performed at the transmit site are shown in Figure 4. There are similarities to the Control Point. The clock generator generates a 19,200 Hz clock for internal use; the GPS signal selection block selects the 1 pps and 9600 Hz clock from the two redundant GPS locked clock sources. In addition it also provides for selection of the landline 9600 Hz in the unlikely event that both GPS sources are failed. The Signal Recovery block is the corresponding function of the Composite Reference Generator at the Control Point. It extracts the 9600, 300 1 pps and pseudo FSL from the reference signals. The 9600 Hz landline is routed off the Xilinx IC (U4) to be filtered by the PLL and returned for use by the T1 delay module. The T1 delay module examines the selected GPS signals (1 pps and 9600) and compares their phase to the corresponding landline signals. If certain “hysterisis hurdles” are exceeded the number of T1 cycles of delay desired are serially sent to the Intraplex MUX where the actual delay is accomplished. This Delay Control block and Signal Recovery block are implemented with state machines.

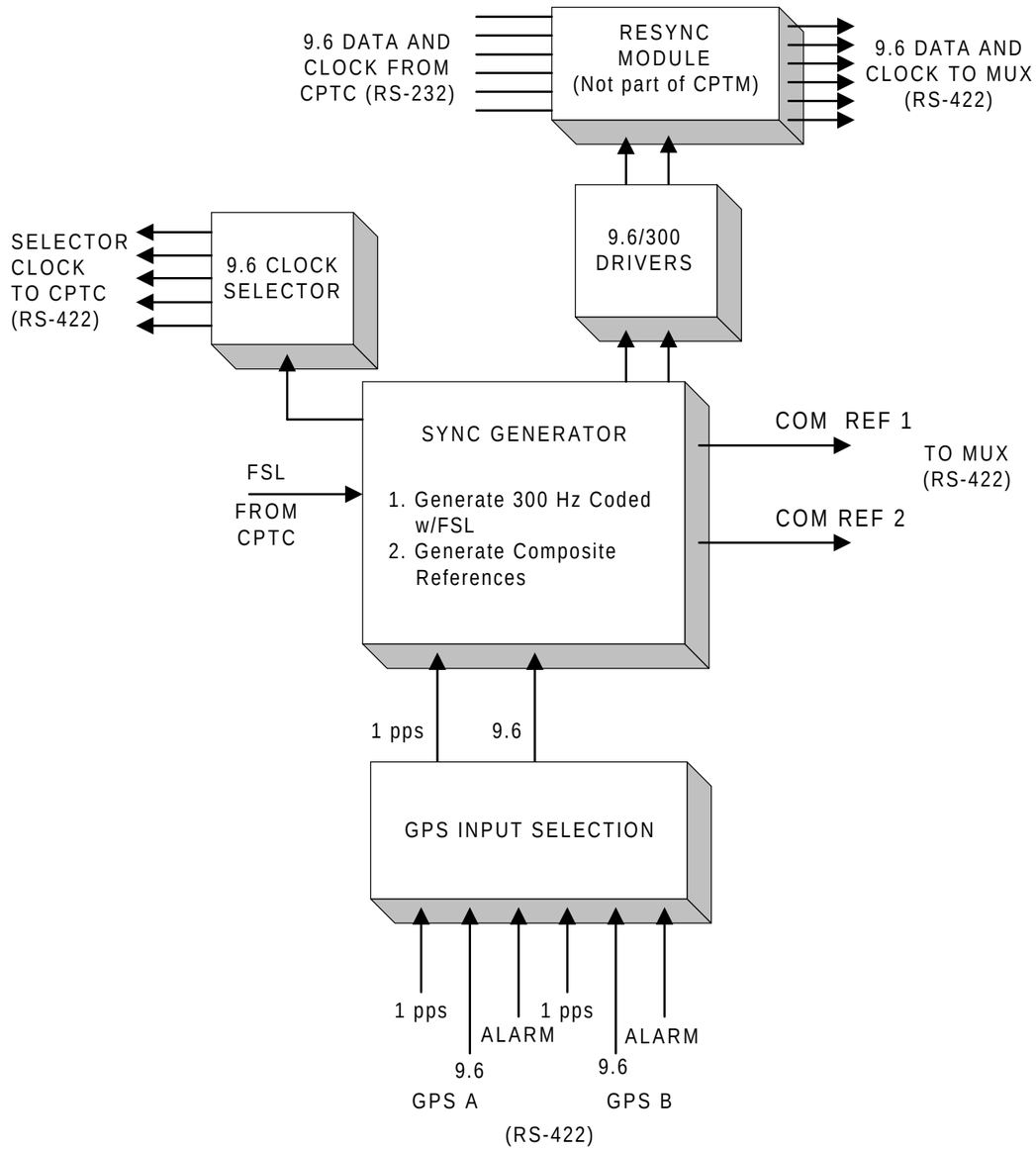


Figure 3 - Functions at the Control Point (CPTM)

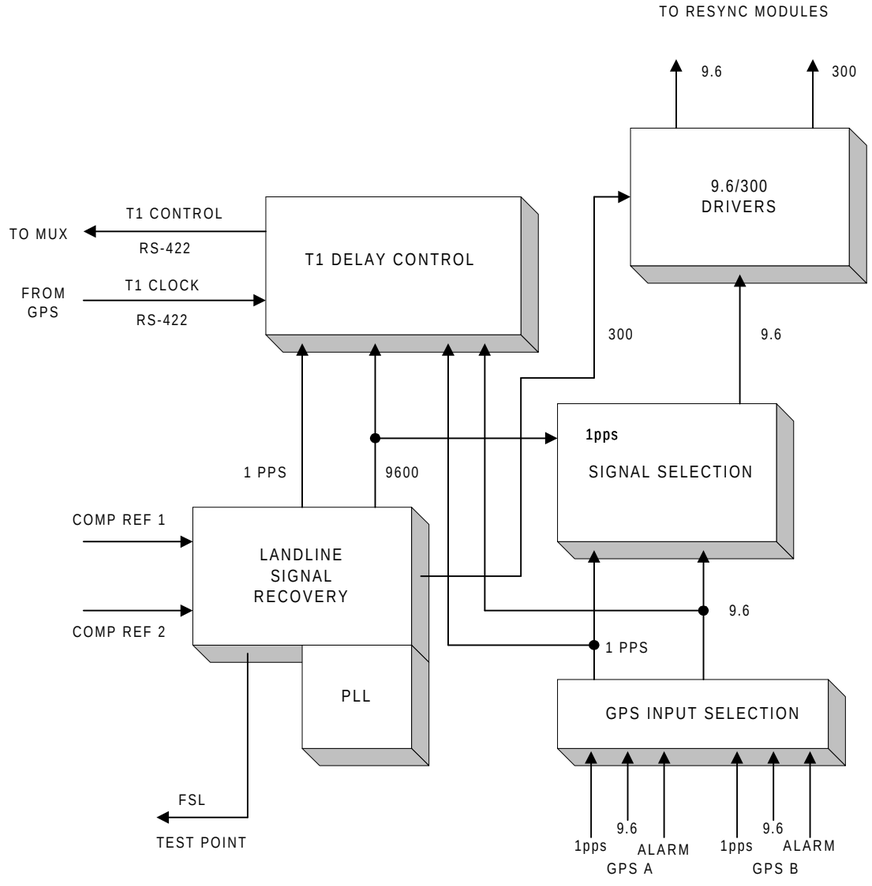


Figure 4 - Functions at the Transmit Site (TXTM)

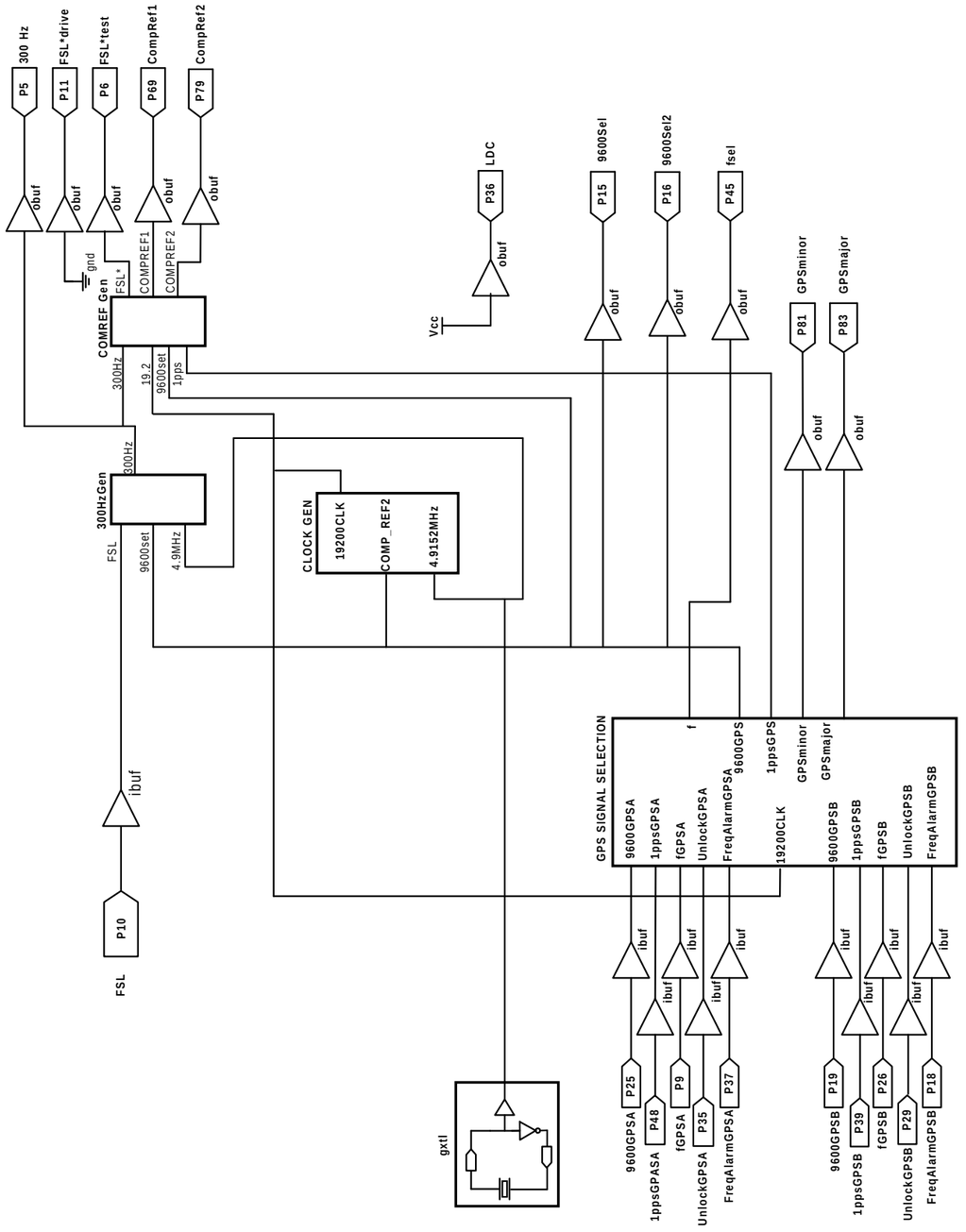


Figure 5 - Xilinx 3190A FPGA at the Control Point

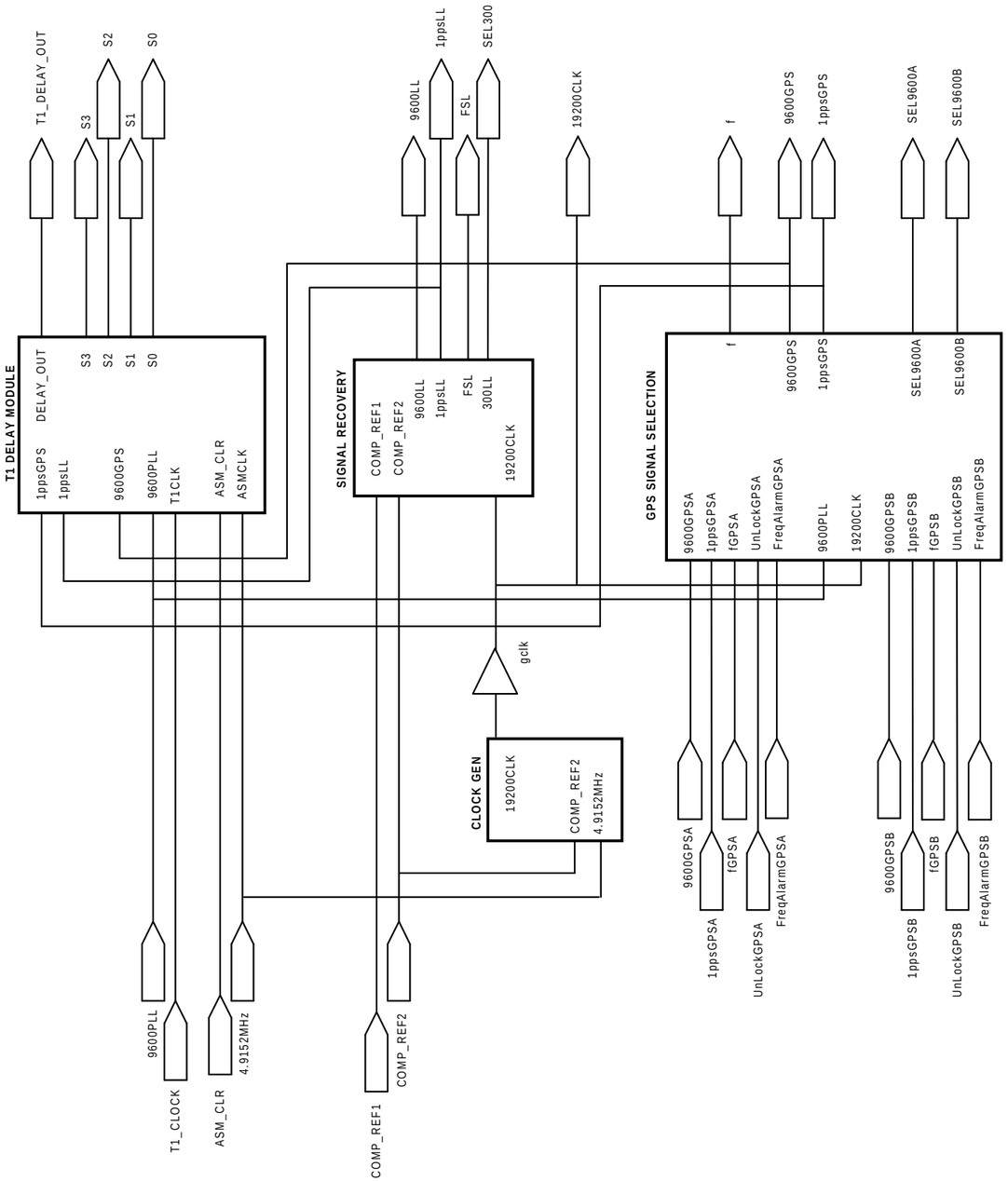


Figure 6 - Xilinx 3190A FPGA at the Transmit Site

TEST AND TROUBLESHOOTING

The GPS Timing operates in two functionally different applications. Some of the functionally is the same for both applications and some is complementary to the other application. The module contains a PROM which holds the configuration information for the application.

The functions to be tested are described previously for the control point and transmit site application.

Signal on test connector P2:

Control Point

Pin 1 - Composite Ref. 1
Pin 2 - 1pps GPS
Pin 3 - nc
Pin 4 - FSL*
Pin 5 - Selected 9600 (ReSync)
Pin 6 - 300 out
Pin 7 - Composite Ref. 2
Pin 8 - nc

Transmit Site

Pin 1 - T1 Delay Data
Pin 2 - 1pps GPS
Pin 3 - 1pps landline
Pin 4 - FSL*
Pin 5 - Selected 9600 (ReSync)
Pin 6 - 300 out
Pin 7 - nc
Pin 8 - 9600 PLL
* Pseudo FSL.

To test as a Control Point module:

The module must be powered up and supplied with GPS signals (9600 Hz, 1pps and an FSL). The presence of the "selected" signals at all the proper outputs and of the generated signals (300, Comp Ref. 1 and Comp Ref. 2) must be verified. This is done for GPS **"A"** and **"B".** The generated Comp Ref. 1 and Comp Ref. 2 need to be checked to verify the "tag" is placed consistently following the corresponding event.

With no signals present, the **MINOR** alarm goes active; the green activity (**ACTV**) LED goes out and the red **MAJOR** alarm LED comes on.

To test the Transmit Site:

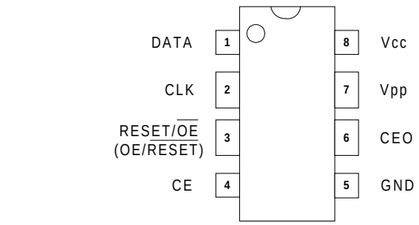
It is desirable to have an operational module in the Control Point mode to provide the Comp Ref. 1 and Comp Ref. 2 signals. Signal selection is checked similar to that done at the Control Point with the additional fault mode of reverting to landline 9600 if neither GPS source is present. A second GPS source allows a precise time difference between the landline 1pps and the "direct" 1pps to test the T1 delay portion of the module. A known time difference is programmed onto the local GPS and the T1 delay output is examined to verify that a new delay value is sent. As there is no MUX (& T1 delay module) the correction will successively add to itself.

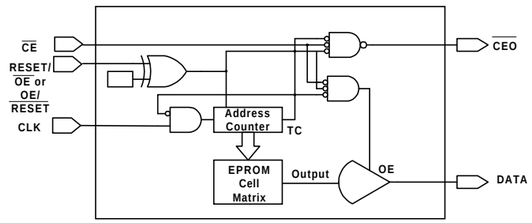
SYMBOL	PART NO.	DESCRIPTION
		- - - - CRYSTAL- - - -
B1	RTM 501 627/07	4.9152 MHz
		- - - -CAPACITORS- - - -
C1	RJE 599 1167/1	Tantalum: 1 µF, ±20%, 16 WVDC.
C2	RJC 464 3045/1	Ceramic: 0.01 µF ±10%, 50 WVDC.
C3	RJE 599 2168 /22	Tantalum: 22 µF 10%, 16 WVDC.
C4	RJC 463 4044/22	Ceramic: 2.2 nF 5%%, 50 WVDC.
C5	RJE 599 2167/47	Tantalum: 4.7 µF 10%,,16 WVDC.
C6	RJC 464 3045/1	Ceramic: 0.01 µF 10%, 50 WVDC.
C7	RJC 463 4043/47	Ceramic: 470 pF 5%, 50 WVDC @ 125C.
C8	RJC 464 3045/1	Ceramic: 0.01 µF 10%, 50 WVDC.
C9 and C10	RJC 463 4042/27	Ceramic: 27 pF 5%, 50 WVDC @ 125C.
C11 thru C13	RJC 464 3045/1	Ceramic: 0.01 µF 10%, 50 WVDC.
C14	RJA 532 4056/1	0.1 µF 5%, 16 WVDC.
C15 thru C20	RJC 464 3045/1	Ceramic: 0.01 µF 10%, 50 WVDC.
C21	RJE 599 1258/1	Ceramic: 10 µF 20 %, 25 WVDC.
C22 thru C33	RJC 464 3045/1	Ceramic: 0.01 µF 10%, 50 WVDC.
C34	RJE 584 3638/47	Tantalum: 47 µF 20%, 6.3 WVDC.
C35	RJC 464 3045/1	Ceramic: 0.01 µF 10%, 50 WVDC.
		- - - -FUSE- - - -
F1	REZ 701 28/1	0.5A 15V PTC/Thermistor
		- - - - DIODES- - - -
H1	RKZ 433 637/2	LED: yellow
H2	RKZ 433 637/1	LED: red
H3	RKZ 433 637/3	LED: green
H4	RKZ 433 637/2	LED: yellow
H5	RKZ 433 637/2	LED: yellow
H6	RKZ 433 637/3	LED: green
		- - - -CONNECTORS- - - -
P1	RPV 403 804/03	Right Angle, 96 Pin, Male.
P2	RNV 403 12/08	RJ12 Right Angle, 8 Pin connector.
		- - - -RESISTORS- - - -
R1 thru R4	REP 625 423/47	Chip: 470 Ohms 5%,,1/8 W
R5	REP 625 426/1	Chip: 100k Ohms 5%, 1/8 W
R7	REP 625 424/12	Chip: 1.2k Ohms 5%, 1/8 W
R8	REP 625 425/68	Chip: 68k Ohms 5%, 1/8 W
R9	REP 625 426/1	Chip: 100k Ohm 5%, 1/8 W
R10	REP 625 425/47	Chip: 47k Ohms 5% 1/8 W
R11	REP 625 427/1	Chip: 1 MEG Ohms 5%, 1/8 W.
R12 thru R14	REP 625 425/47	Chip: 47k Ohms 5% 1/8 W
R15 and R16	REP 625 426/1	Chip: 100k Ohms 5%, 1/8 W
R17	REP 625 425/47	Chip:47k Ohms 5%, 1/8 W
R18	REP 625 424/47	Chip: 4.7k Ohms 5%, 1/8 W.
R20	REP 625 424/47	Chip: 4.7k Ohms 5%, 1/8 W.
R21 and R22	REP 625 423/47	Chip: 470 Ohms 5%,,1/8 W
R23 and R24	REP 625 426/1	Chip: 100k Ohms 5%, 1/8 W
R25 and R26	REP 625 425/47	Chip: 47k Ohms 5%, 1/8 W
R27 thru R44	REP 625 423/47	Chip: 470 Ohms 5%,,1/8 W
		- - - -SWITCH- - - -
S1	RMD 955 006/01	Right Angle, Momentary.
		- -INTEGRATED CIRCUITS- -
U1	RON 107 786	PROM w/Socket (Used with ROA 117 2260/1 Control Point).
U1	RON 107 787	PROM w/Socket (Used with ROA 117 2260/2 Transmit Site).
U2	RYT 306 2003/C	Dual D Flip/Flop: Sim to 74HC74.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

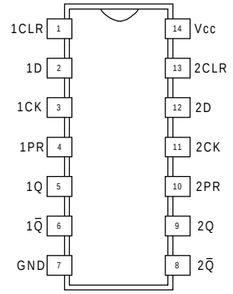
SYMBOL	PART NO.	DESCRIPTION
U3	RYT 304 1046/3C	Phase-Lock-Loop: Sim to 74HCT4046.
U4	RYT 139 009/3C	Xilinx: Sim to 3190A
U5	RYT108 6003/C	555 Timer
U6	RYT 306 2001/C	Quad NAND; Sim to 74HC00.
U7	RYT 306 6029/C	Tri-state Buffer; Sim to 74C125.
U8	RYT 306 2006/C	Quad NOR; Sim to 74HC02.
U9	RYT 109 6079/2C	RS-485 Quad Receiver: Sim to LTC489.
U10	RYT 306 6021/C	Inverter, Open Drain; Sim to 74HC05.
U11	RYT 109 6079/2C	RS-485 Quad Receiver: Sim to LTC489
U12	RYT 306 2007/C	Inverter; Sim to 74HC04.
U13	RYT 306 6029/C	Tri-state Buffer; Sim to 74C125.
U14	RYT 109 6079/2C	RS-485 Quad Receiver: Sim to LTC489
U15	RYT 306 6029/C	Tri-state Buffer; Sim to 74C125.
U16 thru U20	RYT 109 6078/1C	RS-485 Quad Driver; Sim to LTC486.
U21	RYT 306 2007/C	Invertor 74HC04
U22	RYT 306 2002/C	And Gate, 2-input, 74HC08
U23	RYT 306 6029/C	Tri-state Buffer; Sim to 74C125.
U24	RYT 113 6065/1	Power- on reset chip; Sim to MAX705.
		- - - -TRANSISTORS- - - -
V1 thru V3, V5	RYN 123 621/1	FET, n channel.
		- - - -SCHOTTKY DIODE- - - -
V4	RKZ 123 601	Signal Diode
		- - - -SOCKET- - - -
XU1	RNK 860 12/020	20 Pin, PLCC socket for U2.
		- - - -MISCELLANEOUS- - - -
	SXA 120 4174/12	Panel: Front (Control Point)
	SXA 120 4174/16	Panel: Front (Transmit Site)

U1
PROM
RON 107 786 CPTM *(XC1765D)*
RON 107 787 TXTM *(XC1765D)*





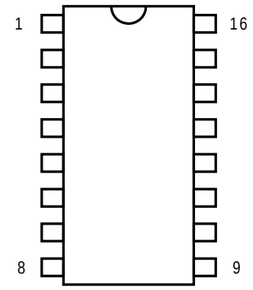
U2
DUAL D FLIP/FLOP
RYT 306 2003/C *(74HC74)*



Inputs			Outputs		
Preset	**Clear**	**Clock**	**D**	**Q**	**/Q**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	/Q0

↑ = Transition from low to high level
Q0 = The level of Q after the previous clock pulse
* = Nonstable, don't preset when PR and CLR are set high
X = Any input, including transition

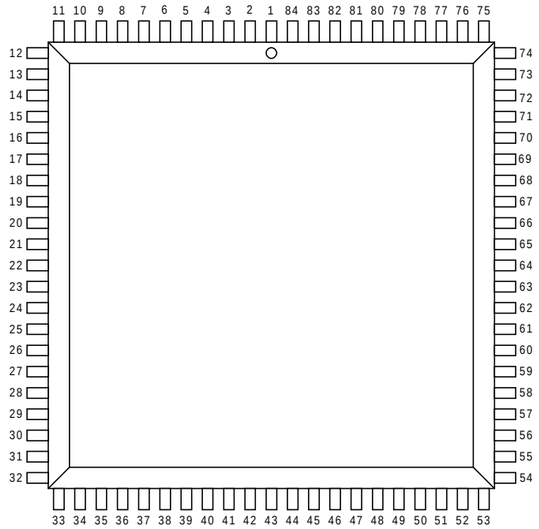
U3
PHASE-LOCK-LOOP
RYT 306 6075/C *(74HCT4046)*



CONNECTIONS

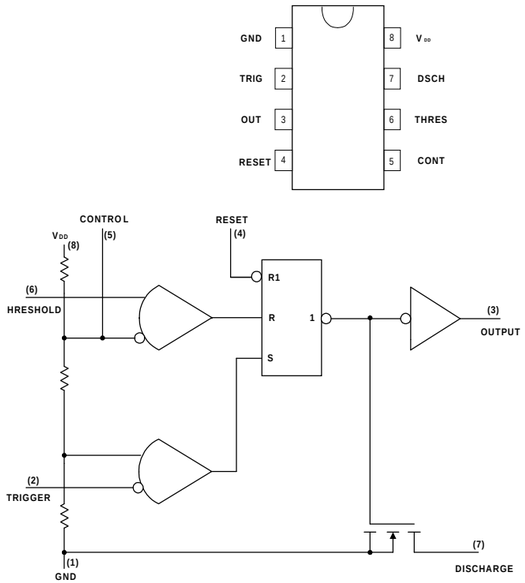
Terminal	Symbol	Function
1	PCPout	Phase comparator pulse output
2	PC1out	Phase comparator 1 output
3	COMPin	Comparator input
4	VCOout	VCO output
5	INH	Inhibit input
6	C1A	Capacitor C1 connection A
7	C1B	Capacitor C1 connection B
8	GND	Ground
9	VCOin	VCO input
10	DEMout	Demodulator output
11	R1	Resistor R1 connection
12	R2	Resistor R2 connection
13	PC2out	Phase comparator 2 output
14	SIGin	Signal input
15	PC3out	Phase comparator 3 output
16	Vcc	Supply Voltage

U4
XILINX
RYT 139 003/5C *(3190A)*

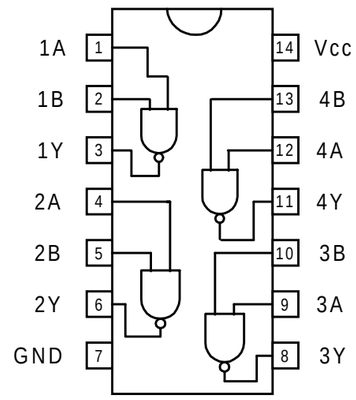


Terminal	Symbol	Function
1	VSS	Ground
2	VCC	Supply Voltage
3	A13-I/O	
4	A6-I/O	
5	A12-I/O	
6	A7-I/O	
7	I/O	
8	A11-I/O	
9	A8-I/O	
10	A10-I/O	
11	A9-I/O	
12	PWRDWN	PWRDWN (active low)
13	TCLKIN-I/O	
14	I/O	
15	I/O	
16	I/O	
17	I/O	
18	I/O	
19	I/O	
20	I/O	
21	VSS	Ground
22	VCC	Supply Voltage
23	I/O	
24	I/O	
25	I/O	
26	I/O	
27	I/O	
28	I/O	
29	I/O	
30	I/O	
31	M1-RDATA	RDATA (active low)
32	MO-RTRIG	
33	M2-I/O	
34	HDC-I/O	
35	I/O	
36	LDC-I/O	LDC (active low)
37	I/O	
38	I/O	
39	I/O	
40	I/O	
41	INIT-I/O	INIT (active low)
42	VCC	Supply Voltage
43	VSS	Ground
44	I/O	
45	I/O	
46	I/O	
47	I/O	
48	I/O	
49	I/O	
50	I/O	
51	I/O	
52	I/O	
53	XTAL2(IN)-I/O	
54	RESET	Active Low
55	DONE/PG	PG (active low)
56	D7-I/O	
57	XTAL1 (OUT)-BCLKIN-I/O	
58	D6-I/O	
59	I/O	
60	D5-I/O	
61	CSO-I/O	CSO (active low)
62	D4-I/O	
63	I/O	
64	VCC	Supply Voltage
65	VSS	Ground
66	D3-I/O	
67	CS1-I/O	CS1 (active low)
68	D2-I/O	
69	I/O	
70	D1-I/O	
71	RDY/BUSY-RCLK-I/O	BUSY-RCLK (active low)
72	DO-DIN-I/O	
73	DOUT-I/O	
74	CCLK	
75	A0-WS-I/O	WS (active low)
76	A1-CS2-I/O	
77	A2-I/O	
78	A3-I/O	
79	I/O	
80	I/O	
81	A15-I/O	
82	A4-I/O	
83	A14-I/O	
84	A5-I/O	

U5
555 TIMER
RYT 108 6003/C

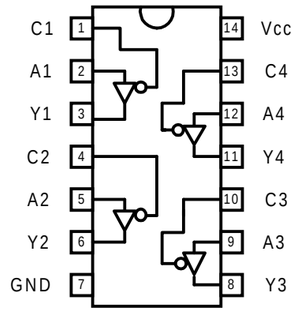


U6
QUAD NAND GATE
RYT 306 2001/C *(74HC00)*



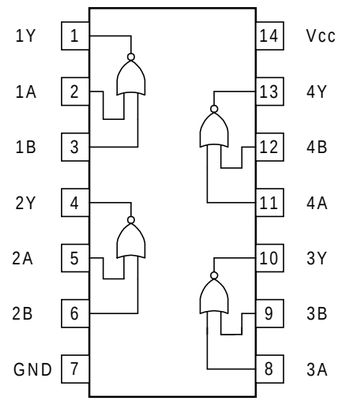
Positive Logic: Y=A • B

U7, U13, U15
TRI-STATE BUFFER
RYT 3066029/C *(74HC125)*



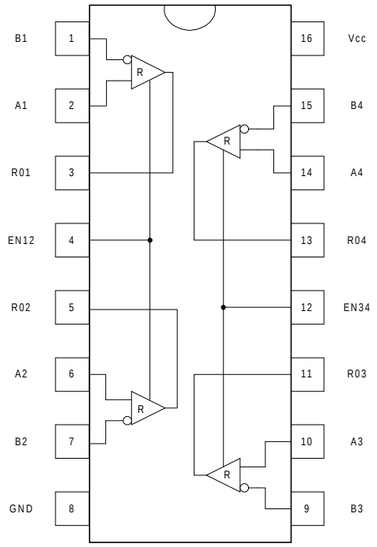
Inputs		Outputs
A	C	Y
H	L	H
L	L	L
X	H	Z

U8
QUAD NORGATE
RYT 306 2006/C *(74HC020)*

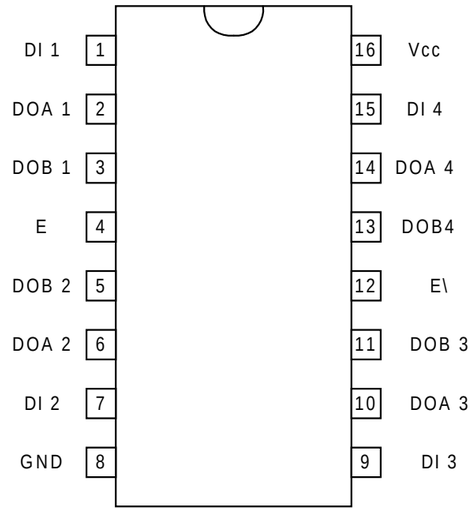


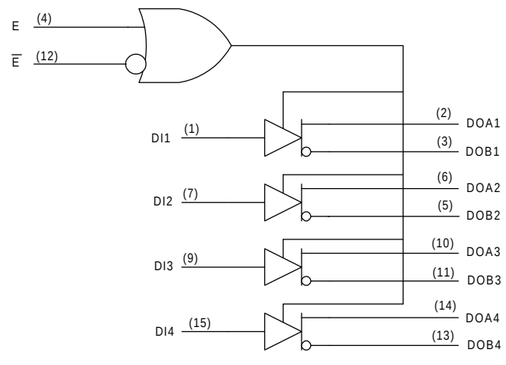
Positive Logic: Y=A+B

U9, U11, U14
RS-485 QUAD RECEIVER
RYT 109 6079/2C *(LTC489)*



U16 - U20
RS-485 QUAD DRIVER
RYT 109 6078/1C *(LTC486)*





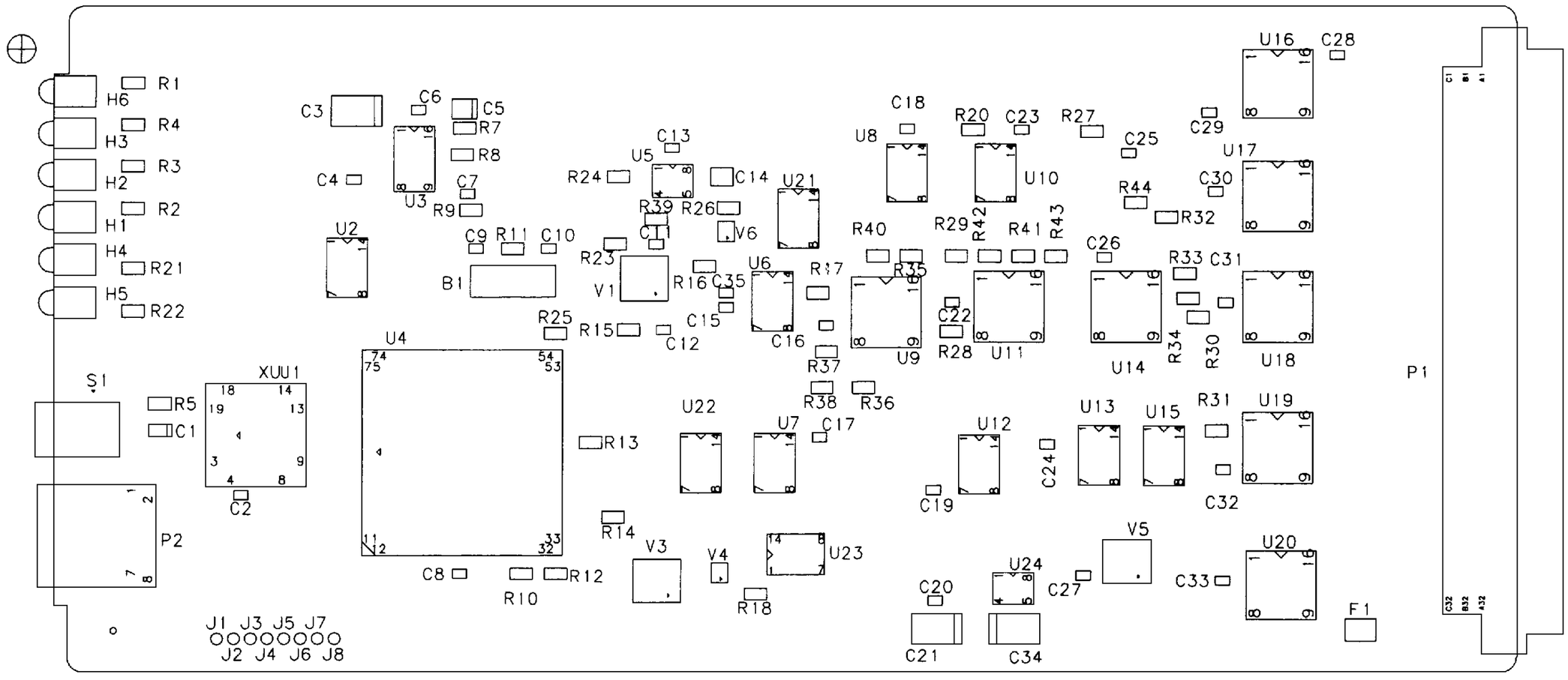
CONNECTIONS

Terminal	Symbol	Function
1	DI 1	Driver Input 1
2	DOA 1	Driver Output A 1
3	DOB 1	Driver Output B 1
4	E	Enable
5	DOB 2	Driver Input B 2
6	DOA 2	Driver Output A 2
7	DI 2	Driver Input 2
8	GND	Ground
9	DI 3	Driver Input 3
10	DOA 3	Driver Output A 3
11	DOB 3	Driver Output B 3
12	E\	Enable\
13	DOB 4	Driver Output B 4
14	DOA 4	Driver Output A 4
15	DI 4	Driver Input 4
16	Vcc	Supply Voltage

FUNCTION TABLE

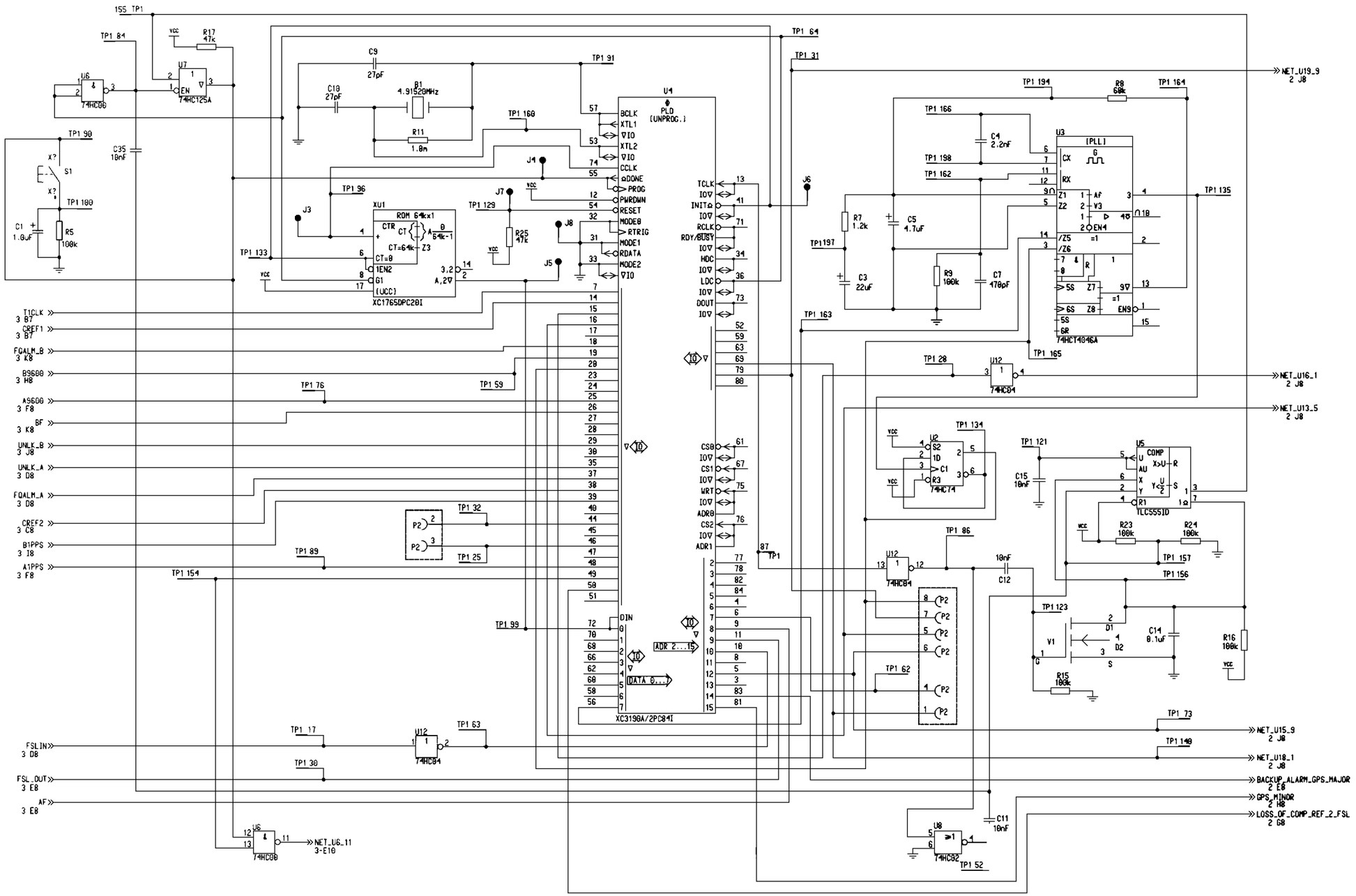
Input	Enables		Outputs	
DI	E	E	DOA	DOB
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H: High Level
L: Low Level
X: Irrelevant
Z: High Impedance (Off)



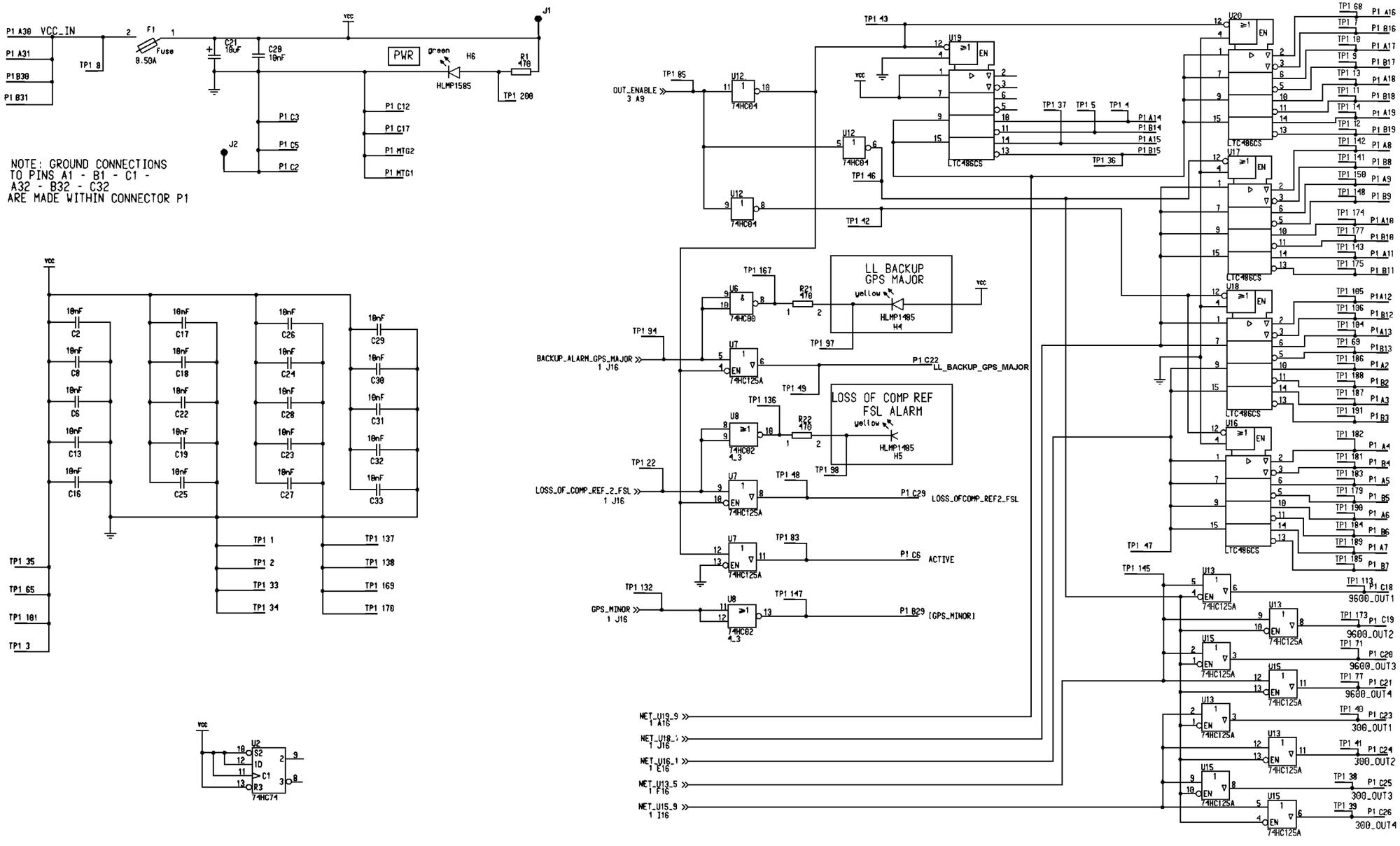
OUTLINE DIAGRAM

(1078 ROA 117 2260, Rev. B)



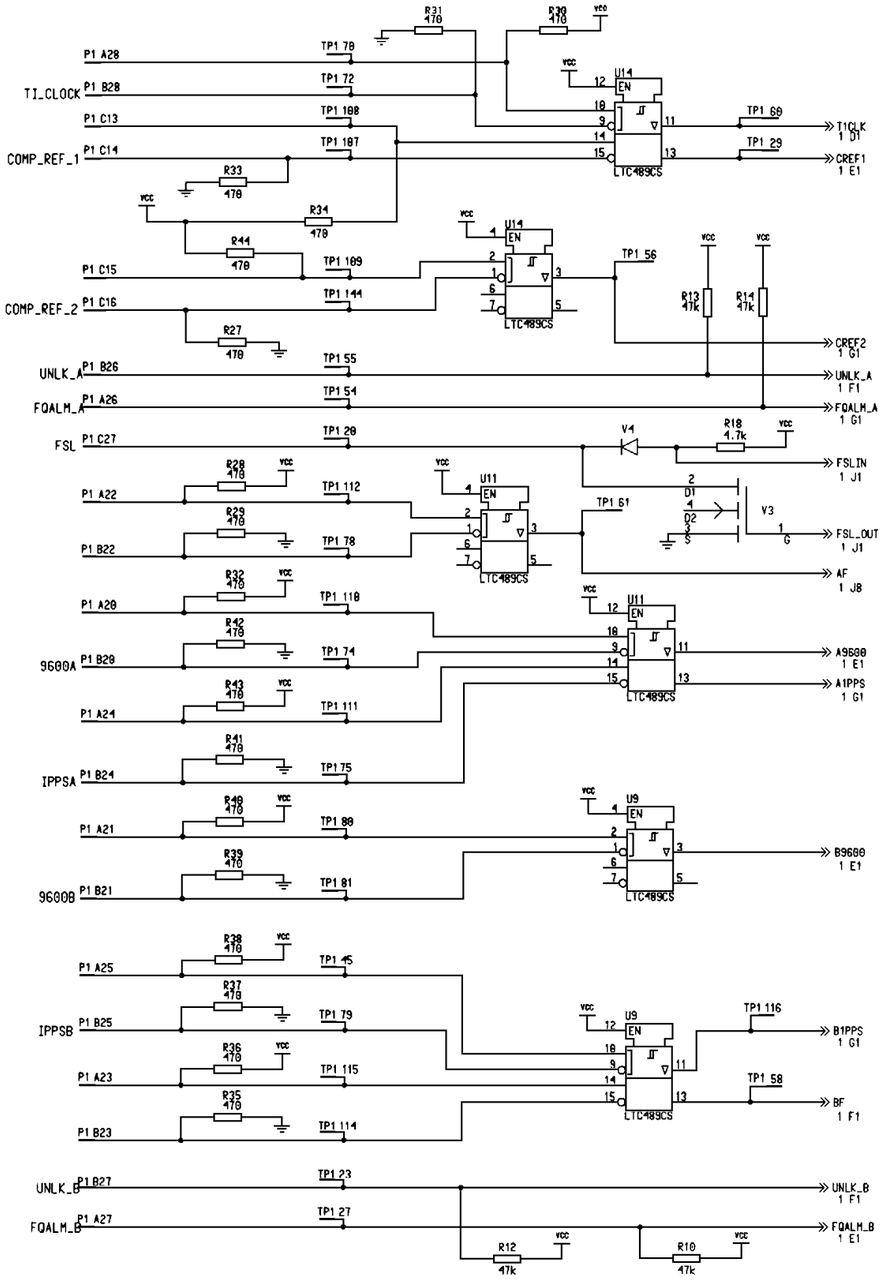
SCHEMATIC DIAGRAM

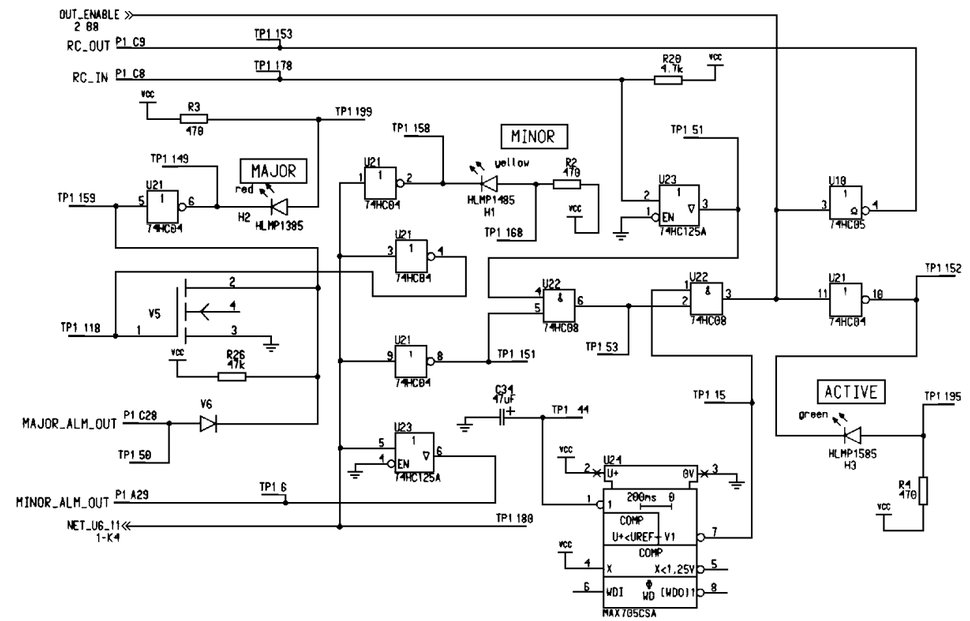
(1911 ROA 117 2260, Sh. 1, Rev. B)



SCHEMATIC DIAGRAM

(1911 ROA 117 2260, Sh. 2, Rev. B)





UNUSED RESERVED TEST POINTS

V2 (+12) ------ TP1 102
V2 (+12) ------ TP1 66
V3 (VARIABLE) ------ TP1 103
V3 (VARIABLE) ------ TP1 67
V4 (-12) ------ TP1 171
V4 (-12) ------ TP1 139

SCHEMATIC DIAGRAM

(1911 ROA 117 2260, Sh. 3, Rev. B)

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