Maintenance Manual

GPS SIMULCAST RESYNC MODULE
ROA 117 2263

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SPECIFICATIONS

Input Voltage	+5 Vdc ± 10%
Current Drain	65 Milliamps (Typical)
Operating Temperature	-30°C to +60°C
Dimensions	8 inches long x 4.0 inches wide
Connector	
+5 Vdc	A30, A31, B30, B31
Ground	A1, B1, C1, A5, B5, C5, A9, B9, C9, A14, B14, A19, B19, C19, A32, B32, C32

ERICSSON

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AE/LZB 119 1876 R1A
Printed in U.S.A.

Table 1 - Connector P1 Definition

Terminal	ROW A	ROW B	ROW C
1	GND	GND	GND
2	CLK IN1 (RS232)		DATA IN1 (RS232)
3	CLK IN2 (RS232)		DATA IN2 (RS232)
4	CLK IN3 (RS232)		DATA IN3 (RS232)
5	GND	GND	GND
6	CLK IN4 (RS232)		DATA IN4 (RS232)
7	CLK IN5 (RS232)		DATA IN5 (RS232)
8	CLK IN6 (RS232)		DATA IN6 (RS232)
9	GND	GND	GND
10	CLK OUT 1A (RS422)		CLK OUT 1B (RS422)
11	DATA OUT 1A (RS422)		DATA OUT 1B (RS422)
12	CLK OUT 2A (RS422)		CLK OUT 2B (RS422)
13	DATA OUT 2A (RS422)		DATA OUT 2B (RS422)
14	GND	GND	GND
15	CLK OUT 3A (RS422)		CLK OUT 3B (RS422)
16	DATA OUT 3A (RS422)		DATA OUT 3B (RS422)
17	CLK OUT 4A (RS422)		CLK OUT 4B (RS422)
18	DATA OUT 4A (RS422)		DATA OUT 4B (RS422)
19	GND	GND	GND
20	CLK OUT 5A (RS422)		CLK OUT 5B (RS422)
21	DATA OUT 5A (RS422)		DATA OUT 5B (RS422)
22	CLK OUT 6A (RS422)		CLK OUT 6B (RS422)
23	DATA OUT 6A (RS422)		DATA OUT 6B (RS422)
24			
25	SEL 300 IN (TTL)		SEL 9600 IN (TTL)
26			
27			
28			
29			
30	+5V	+5V	
31	+5V	+5V	
32	GND	GND	GND

Continued

NOTICE!

Repairs to this equipment should be made only by an authorized service technician or facility designated by the supplier. Any repairs, alterations or substitution of recommended parts made by the user to this equipment not approved by the manufacturer could void the user's authority to operate the equipment in addition to the manufacturer's warranty.

NOTICE!

Continued

Table 2 - Connector P2 Definition

Terminal	Signal (TTL Levels)
1	DATAOUT6
2	OUTCLK
3	300
4	DATAOUT 5
5	DATAOUT4
6	DATAOUT3
7	DATAOUT2
8	DATAOUT1

DESCRIPTION

ReSync Module ROA 117 2263 performs the function of Simulcast re-synchronization for 9600 bps data in the **EDACS®** GPS Simulcast System. Each module is capable of performing this function on six data paths (channels) independently. Data and clock input for each channel (at RS-232 levels) flow through the module (at logic levels) and are output at RS-422. Also, input to this module is the 300 gating clock and the 9600 bit clock, both at logic levels. Xilinx, **F**ield **P**rogrammable **G**ate **A**rray (**FPGA**) U1 contains the ReSync and **F**irst-**I**n-**F**irst-**O**ut (**FIFO**) control logic for all six channels.

CIRCUIT ANALYSIS

XILINX, FPGA

This device contains the logic for each channel replicated six times within the FPGA. The circuitry arms for resync when a sufficient string of consecutive zeros occur and controls the reset of the FIFO (1/2 of a U3, U9, or U11). The circuitry also executes the resync when the first "one" appears in the data stream. The Xilinx (U1) is wired in master serial mode, which refers to the manner in which the part programming is accomplished. At power up or following release of the reset/reprogram push-button, the data in PROM U10 is serially read into U1. The 555 timer (U12) performs a watch dog function, causing a reprogram if out-clock is not properly getting through U1 (i.e. will cause alarm).

INTERFACE

The pinout of the backplane is shown in Table 1 and on the Schematic Diagram, Sheet 4. The RS-232 inputs are converted to logic levels by quad line receivers U2, U8 & U18. The logic level inputs are received through a Schmitt inverter (U4) to provide hysterisis/noise immunity. The output data and clocks are converted to RS-422 by dual line drivers U15, U16 & U17.

POWER

The ReSync module operates from a single 5 Vdc (std. TTL tolerance) power supply. Thermistor fuse F1, on the module, prevents a module failure from collapsing a shelf power supply.

FIFO

Integrated circuits U3, U9 & U11 are dual 256 x 1 clocked, **FIFO** memories. Each integrated circuit package supports two channels. To properly reset this FIFO, a sequence four (4) clock cycles long is required. The Xilinx logic provides this. The two input OR gate following the Q output of the FIFO allows the data output to be forced to the proper state during a ReSync, preventing erroneous data that may have otherwise occurred as the FIFO is reset.

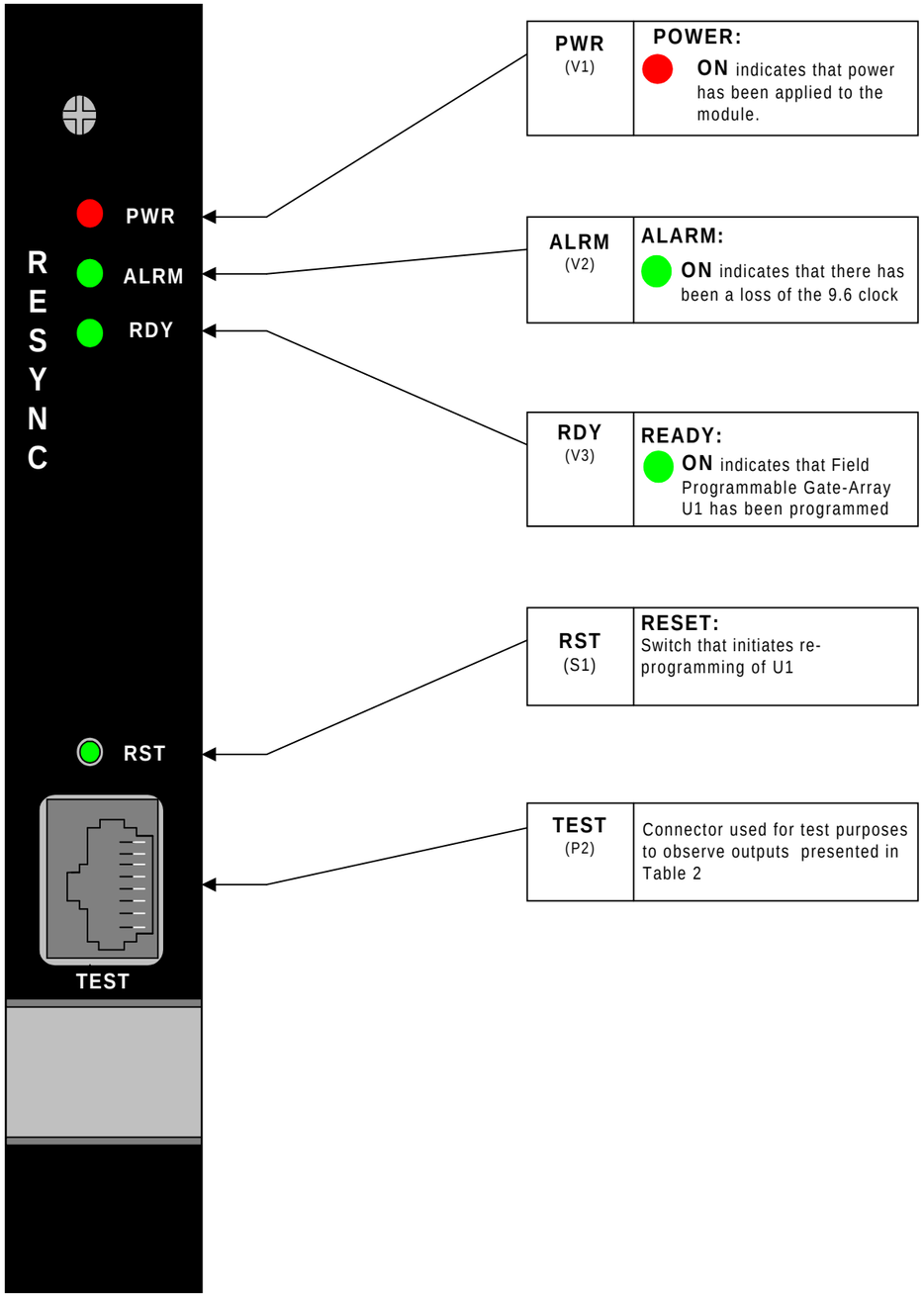


Figure 1 - Front Panel

TEST AND TROUBLESHOOTING

Equipment Required:

- +5 Vdc Power Supply
- Multimeter
- Two Function Generators
- Oscilloscope
- Provider of a Recognizable Data Stream

Continuity Test:

Using the multimeter, check for no short circuit between +5 Vdc and ground.

Initial Test Setup:

+5 Vdc Pins	Ground Pins
A30	A1
A31	B1
B30	C1
B31	A32
	B32
	C32

1. Apply +5 Vdc to the power pins and ground listed above.
2. Place a 300 Hz TTL level clock at pin A25.
3. Place a 9600 Hz TTL level clock at pin C25.
4. For each of the tests outlined in steps 1 through 7 under **Test Procedures** check for the appropriate results as indicated.

Test Procedures

1. Check all ground and Power pin connections as follows:

Power	Ground
A30	A1
A31	B1
B30	C1
B31	A5
	B5
	C5
	A9
	B9
	A14
	B14
	C14
	A19
	B19
	C19
	A32
	B32
	C32

Perform Steps 2 - 7 for each of the six (6) data paths.

2. Place RS232 level data and clock signals on the six inputs and check for the same data as input on the corresponding output pins but not on the other output pins as follows:

Data Input	Clock Input	RS-422 A, B Data Out
C2	A2	A11, C11
C3	A3	A13, C13
C4	A4	A16, C16
C6	A6	A18, C18
C7	A7	A21, C21
C8	A8	A23, C23

3. Remove the 9600 Hz clock from pin C25 while data and clock are applied to the input pins. The corresponding output pin should not have data out.
4. Remove the 300 Hz clock from pin A25 while data and clock are applied to the input pins. The corresponding output pin should have data on the output.
5. Place a level high on the data input. The data output stream should stop.
6. Place the data back on the input pin. The data out should not resume.
7. Place the 300 Hz clock on pin A25. The data out should resume.

DefinitionTable 3 - Board Test Points

Test Point	Signal (TTL Levels)
TP501	CLKIN1
TP502	DATAIN1
TP503	DATAIN2
TP504	CLKIN2
TP505	CLKIN3
TP506	DATAIN3
TP507	CLKIN4
TP508	DATAIN4
TP509	GND
TP510	CLKIN5
TP511	DATAIN5
TP512	CLKIN6
TP513	DATAIN6

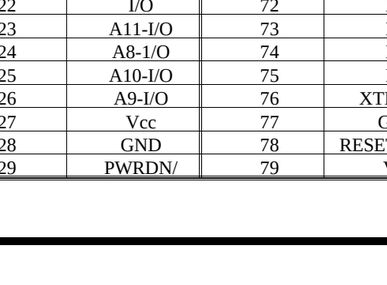
PARTS LIST
RESYNC MODULE
ROA 117 2263

SYMBOL	PART NO.	DESCRIPTION
		- - - - - - - - - CAPACITORS - - - - - - - - -
C1 thru C12	RJC 463 4043/47	Ceramic: 470 pF ±5%, 50 VDCW.
C13 thru C16	RJC 464 3045/1	Ceramic: 0.01 µF ±10%, 50 VDCW.
C17	RJE 584 3167/1	Tantalum: 1 µF ±20%, 50 VDCW.
C18 and C19	RJE 584 3638/47	Tantalum: 47 µF ±20%, 16 VDCW.
C20 thru C38	RJC 464 3045/1	Ceramic: 0.01 µF ±10%, 50 VDCW.
C39 and C40	RJC 463 4042/27	Ceramic: 27 pF ±5%, 50 VDCW.
		- - - - - - - - - FUSE - - - - - - - - -
F1	REZ 701 28/1	Thermistor 0.5A 15V PTC.
		- - - - - - - - - CONNECTOR - - - - - - - - -
J1	Part of U10	20-Pin PLCC Socket: Sim to Newark 50F227.
P1	RPV 403 804/03	Right Angle, 96-Pin Male.
P2	RNV 403 12/08	Modular Jack/Connector.
		- - - - - - - - - RESISTORS - - - - - - - - -
R1 and R2	REP 625 424/51	Chip: 5.1k Ohms ±5%, 0.125 Watt.
R3	REP 625 426/1	Chip: 100k Ohms ±5%, 0.125 Watt.
R4 thru R6	REP 625 423/47	Chip: 470 Ohms ±5%, 0.125 Watt.
R7 thru R9	REP 625 426/1	Chip: 100k Ohms ±5%, 0.125 Watt.
R11	REP 625 427/1	Chip: 1 MEG Ohm ±5%, 0.125 Watt.
		- - - - - - - - - SWITCH - - - - - - - - -
S1	RMD 955 006/01	Right Angle, Momentary: Sim to GE 19A149923P2.
		- - - - - - - - - TEST POINTS - - - - - - - - -
TP1 thru TP13	RPV 380 902/01	Test Point: Sim to Newark MR5010.MP1.
		- - - - - - - - - INTEGRATED CIRCUITS - - - - - - - - -
U1		Field Programmable Gate Array: Sim to Xilink 3042 PQFP,100 Pin.
U2	RYT 109 003/2C	Quad Line Receiver: Sim to 1489.
U3	RYT 110 6021/C	Dual 256 x 1 Clocked FIFO Memories: Sim to TI 74ACT2228.
U4	RYT 306 2007/C	Hex Inverter: Sim to 74HC04.
U5	RYT 306 2006/C	Quad OR: Sim to 74HC02
U6	RYT 306 2020/C	Schmitt Inverter: Sim to 74HC14.
U7	RYT 306 6029/Cc	Tri-State Buffer; Sim to 74HC125H.
U8	RYT 306 003/2C	Quad Line Receiver: Sim to 1489.
U9	RYT 110 6021/C	Dual 256 x 1 Clocked FIFO Memories: Sim to T1 74ACT2228.
U10	RYT 118 6045/2C	PROM, 20-Pin PLCC with socket: Sim to XC1736D.
U11	RYT 110 6021/C	Dual 256 x 1 FIFO Memories: Sim to T1 74ACT2228.
U12	RYT 108 6003/C	555 Timer.
U13	RYT 306 2002/C	Quad AND: Sim to 74HC08.
U14	RYT 306 6021/C	Open Drain Inverter: Sim to 74HC05.
U15 thru U17	RYT 109 6078/C	Dual Line Driver: Sim to LTC486.
U18	RYT 109 003/2C	Quad Line Receiver: Sim to 1489.
U20	RYT 306 2006/C	Quad OR: Sim to 74HC02.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES.

SYMBOL	PART NO.	DESCRIPTION
		- - - - - - - - - INDICATORS - - - - - - - - -
V1 and V2/	RKZ 433 637/3	LED: Right Angle, Sub, Green.
V3	RKZ 433 637/1	LED: Right Angle, Sub, Red.
		- - - - - - - - - CRYSTAL - - - - - - - - -
Y1	RTM 501 627/07	4.9152 MHz.
		- - - - - - - - - MISCELLANEOUS - - - - - - - - -
	NTM 201 1079	Mounting Kit: Sim to RPV 380 902/01.
	SXA 120 4174/1	Face Plate.

U1
Field Programmable Gate-Array
RYT 139 003/6C (Xilink 3042PQFP)

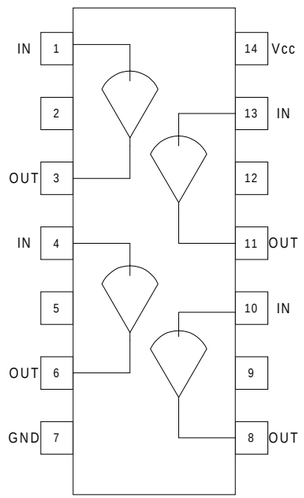


Pin No.	Designation	Pin No	Designation
1	DOUT-1/O	51	I/O
2	CCLK	52	M1-RD\
3	Vcc	53	GND
4	GND	54	M0-RT
5	A0-WS\-I/O	55	Vcc
6	A1-CS2-I/O	56	M2-I/O
7	I/O	57	HDC-I/O
8	A2-I/O	58	I/O
9	A3-I/O	59	LDC\-I/O
10	I/O	60	I/O
11	I/O	61	I/O
12	A15-1/O	62	I/O
13	A4-I/O	63	I/O
14	A14-I/O	64	I/O
15	A5-I/O	65	INIT\-I/O
16	GND	66	GND
17	A13-I/O	67	I/O
18	A6-I/O	68	I/O
19	A12-I/O	69	I/O
20	A7-I/O	70	I/O
21	I/O	71	I/O
22	I/O	72	I/O
23	A11-I/O	73	I/O
24	A8-1/O	74	I/O
25	A10-I/O	75	I/O
26	A9-I/O	76	XTL2-I/O
27	Vcc	77	GND
28	GND	78	RESET\D7-I/O
29	PWRDN/	79	Vcc

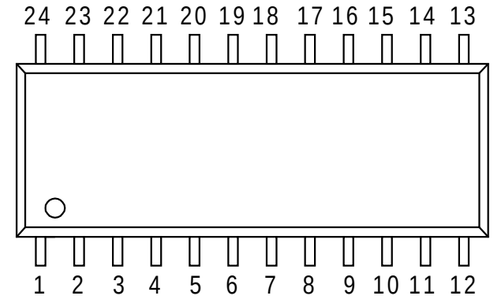
Continued

Pin No.	Designation	Pin No	Designation
30	TCLKIN-I/O	80	DONE-PG\
31	I/O	81	D7-1/O
32	I/O	82	BCLKIN-XTL 1-I/O
33	I/O	83	D6-I/O
34	I/O	84	I/O
35	I/O	85	I/O
36	I/O	86	I/O
37	I/O	87	D5-I/O
38	I/O	88	CSO\-I/O
39	I/O	89	D2-I/O
40	I/O	90	I/O
41	Vcc	91	Vcc
42	I/O	92	D3-I/O
43	I/O	93	CS1\-I/O
44	I/O	94	D2-I/O
45	I/O	95	I/O
46	I/O	96	I/O
47	I/O	97	I/O
48	I/O	98	D1-I/O
49	I/O	99	RDY/BUSY\-R CLK\-I/O
50	I/O	100	D0-DIN-I/O

U2, U8 & U18
QUAD LINE RECEIVER
RYT 109 003/2C (14C89)

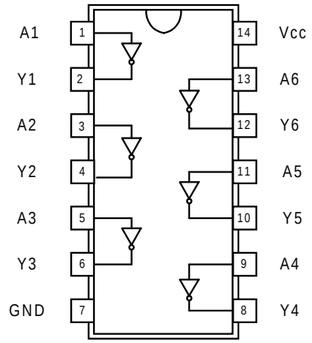


U3, U9 & U11
DUAL 256 X 1 Clocked FIFO MEMORIES
RYT 110 6021/C (TI74ACT2228)

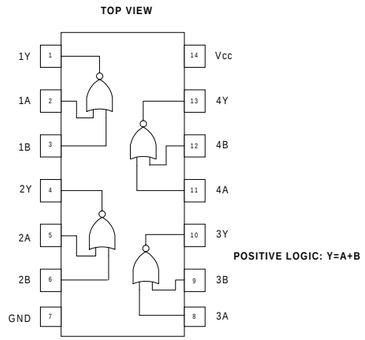


Terminal	Symbol	Function
1	1HF	Half-Full Flag
2	1AF/AE	Almost Full/Almost Empty Flag
3	1WRTCLK	Write Clock
4	1WRTEN	Write Enable
5	1IR	Input Ready Flag
6	1D	Data Input
7	GND	Ground
8	1RESET\	Reset
9	2Q	Data Output
10	2OR	Output Ready
11	2RDEN	Read Enable
12	2RDCLK	Read Clock
13	2HF	Half-Full Flag
14	2AF/AE	Almost Full/ Almost Empty Flag
15	2WRTCLK	Write Clock
16	2WRTEN	Write Enable
17	2IR	Input Ready Flag
18	2D	Data Input
19	Vcc	Supply Voltage
20	2RESET\	Reset
21	1Q	Data Output
22	1OR	Output Ready
23	1RDEN	Red Enable
24	1RDCLK	Read Clock

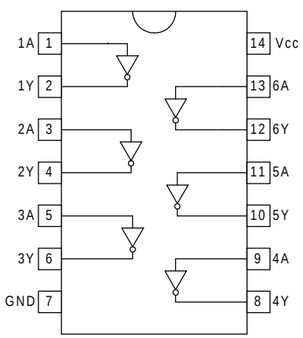
U4
HEX INVERTER
RYT 306 2007/C (74HC04)



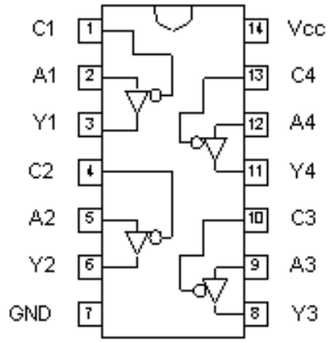
U5 & U20
QUAD OR GATE
RYT 306 2006/C (74HC02)



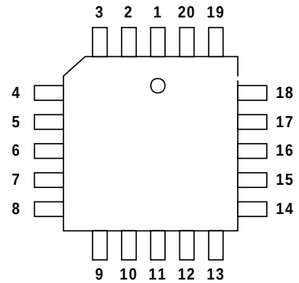
U6
SCHMITT INVERTER
RYT 306 2020/C (74HC14)



U7
TRI STATE BUFFER
RYT 306 6029/C (74HC125H)

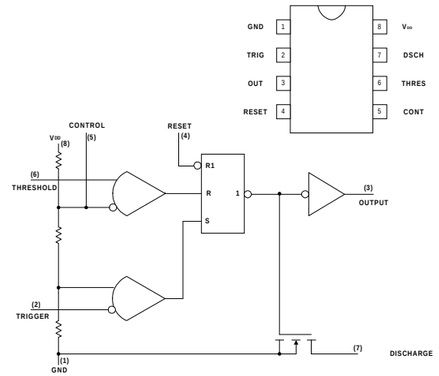


U10
PROM, 20-PIN
RYT 118 6045/2C (XC1736D)

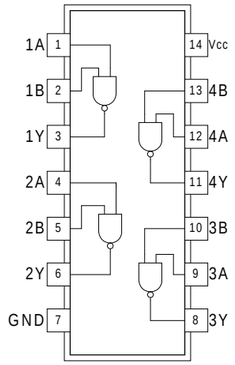


Terminal	Symbol	Function
1	nc	Not Connected
2	DATA	
3	nc	Not Connected
4	CLK	
5	nc	Not Connected
6	RESET/OE\	Reset/Output Enable Input, Programable as RESET\ /OE
7	nc	Not Connected
8	CE\	Chip Enable Input
9	nc	Not Connected
10	GND	Ground
11	nc	Not Connected
12	nc	Not Connected
13	nc	Not Connected
14	CEO\	Chip Enable Output
15	nc	Not Connected
16	nc	Not Connected
17	Vpp	Supply Voltage, Programming
18	nc	Not Connected
19	nc	Not Connected
20	Vcc	Supply Voltage

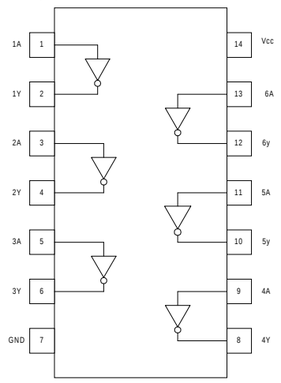
U12
555 TIMER
RYT 108 6003/C



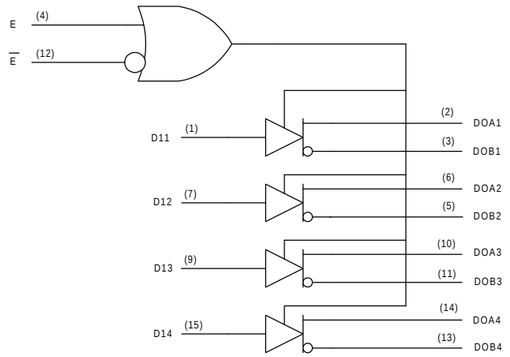
U13
QUAD NAND GATE
RYT 306 2002/C (74HC08)

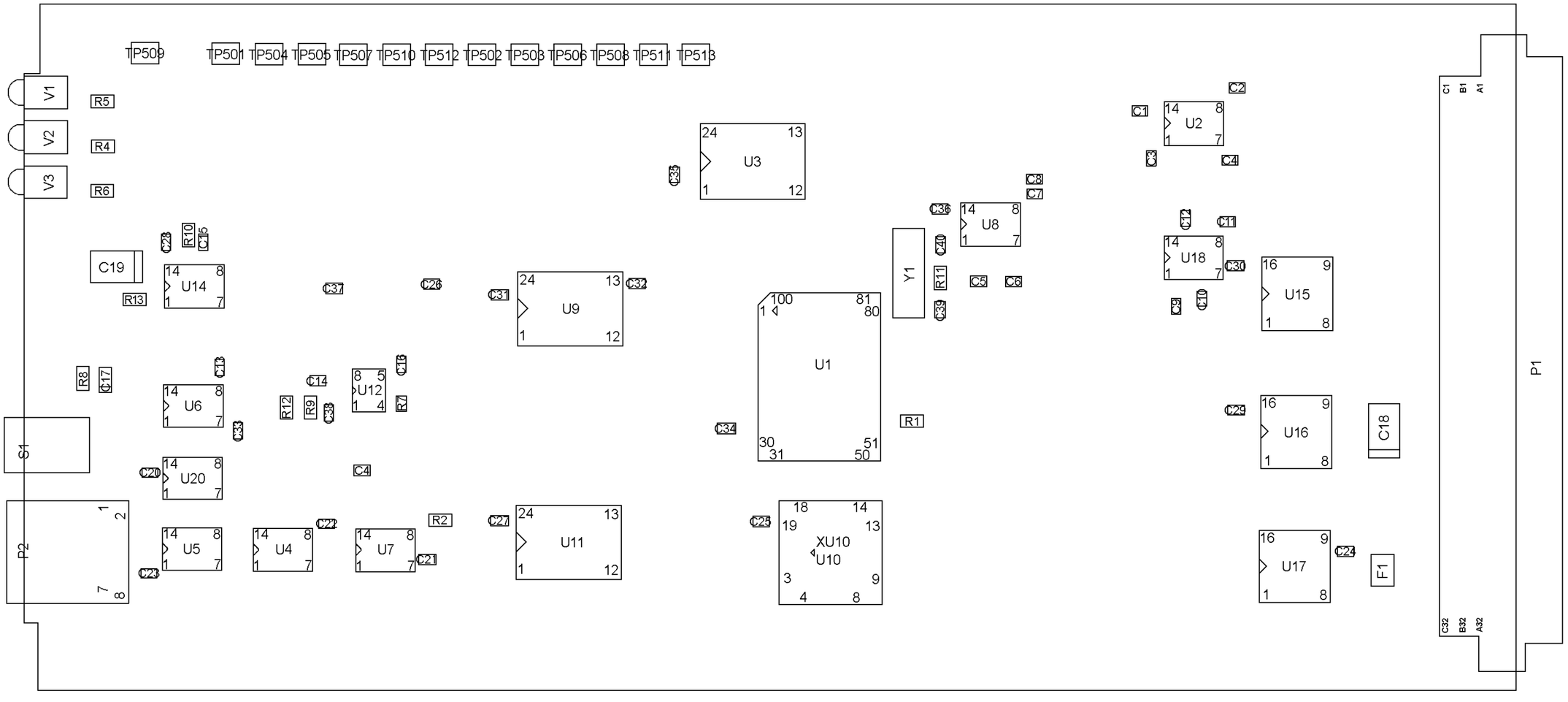


U14
OPEN DRAIN INVERTER
RYT 306 6021/C (74HC05)



U15, 16 & 17
DUAL LINE DRIVER
RYT 109 6078/C (LTC486)





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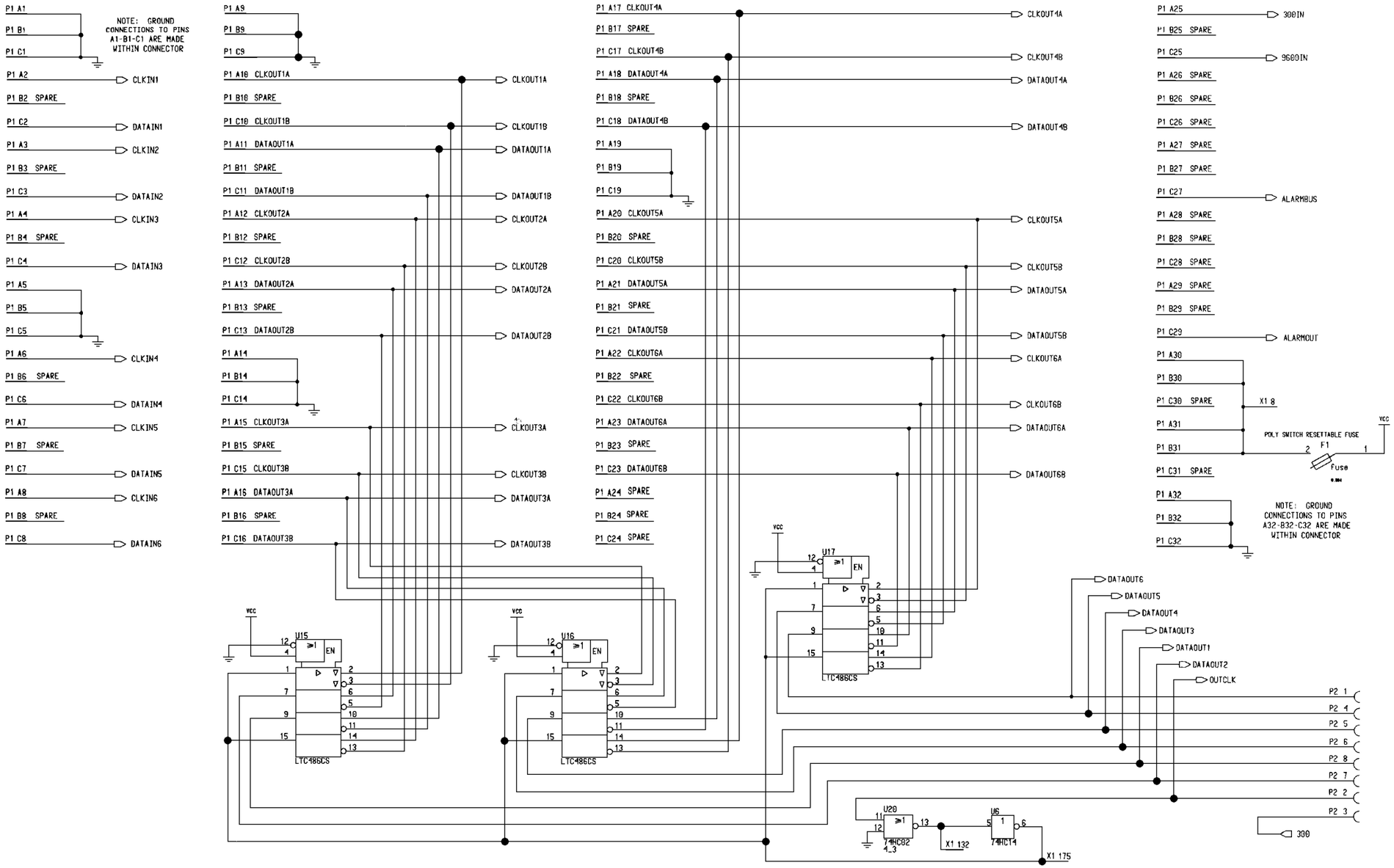

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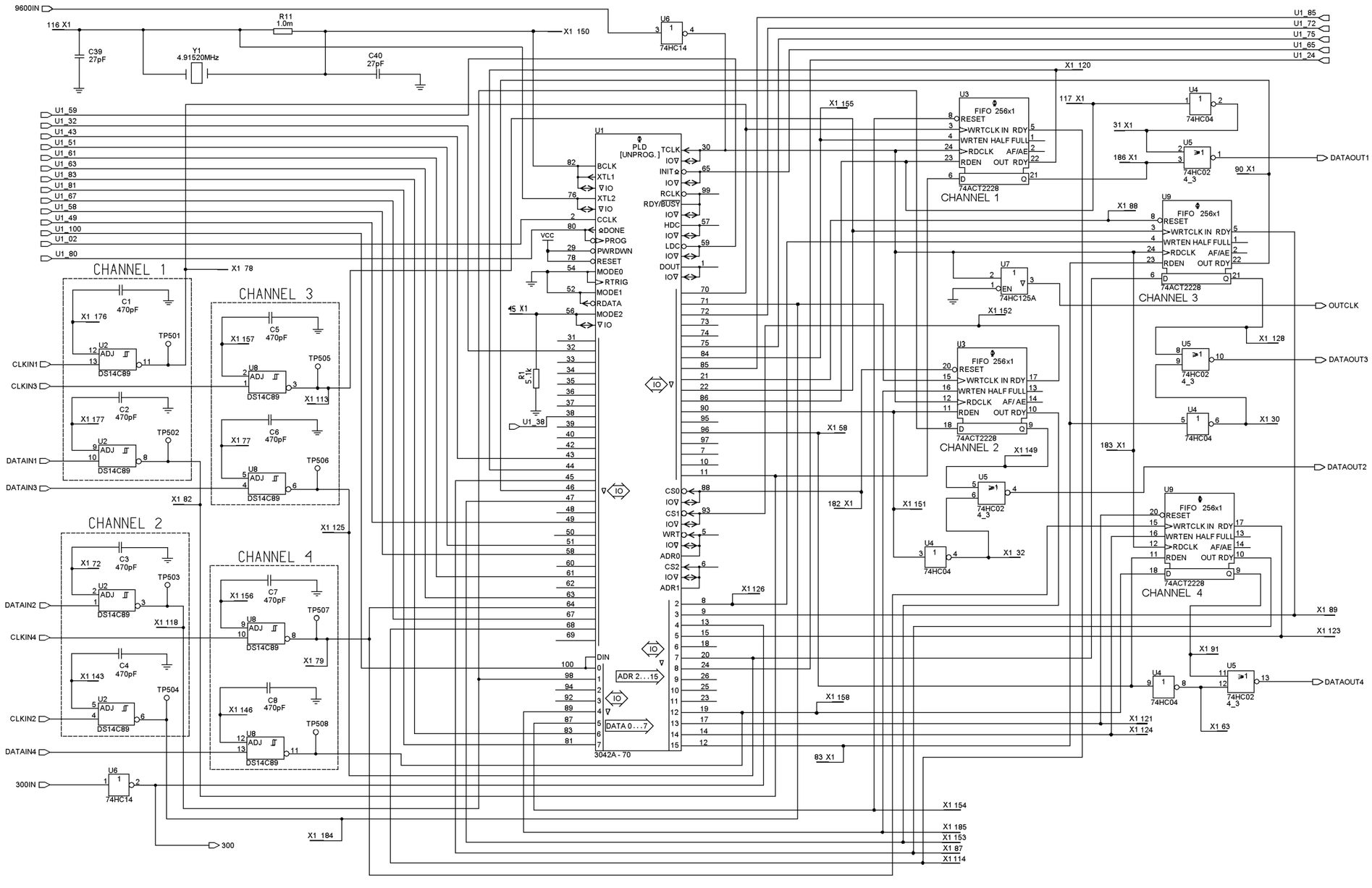

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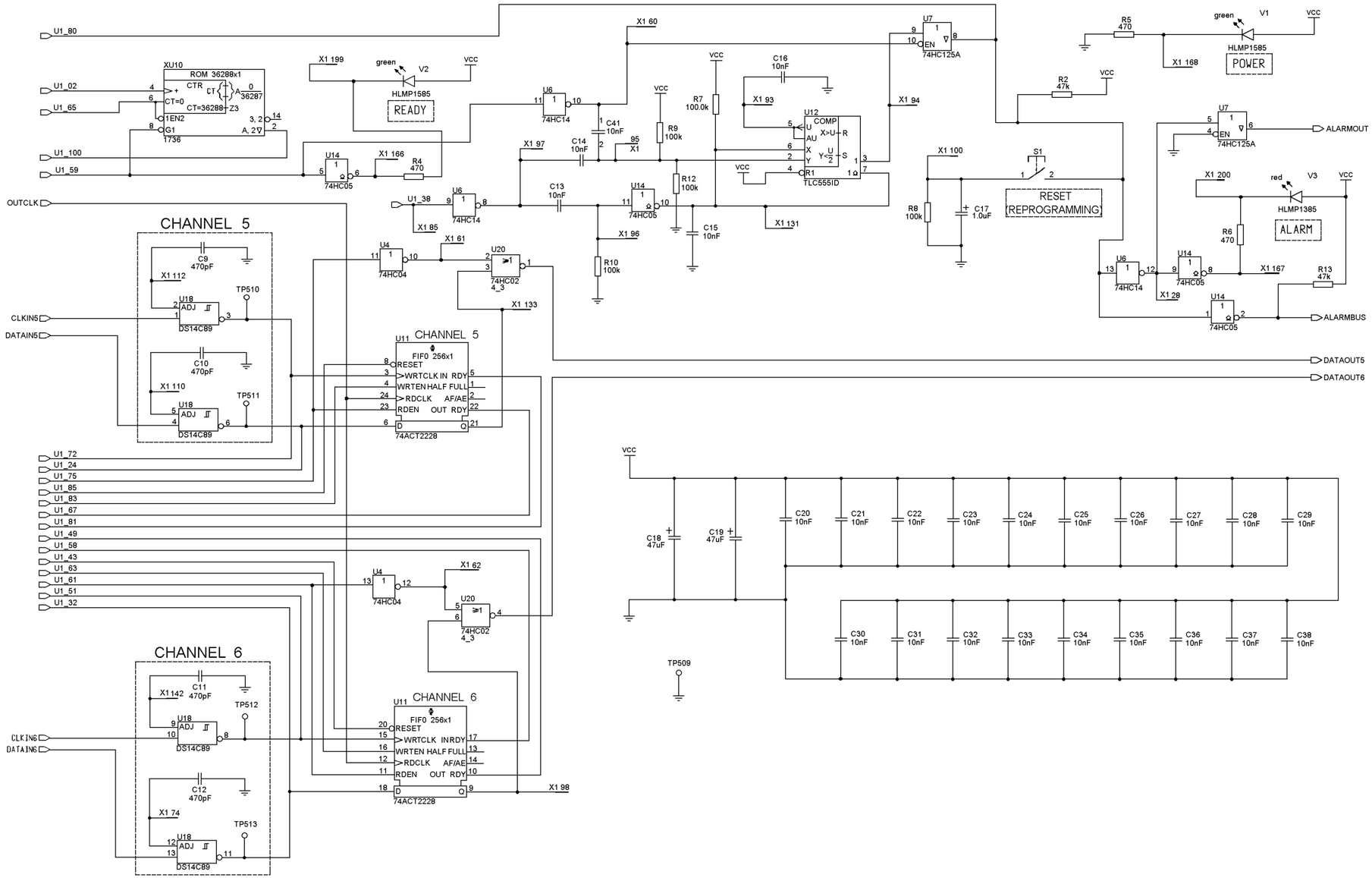

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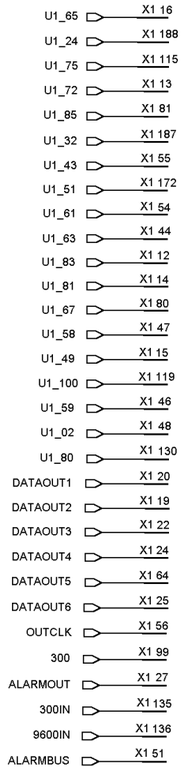
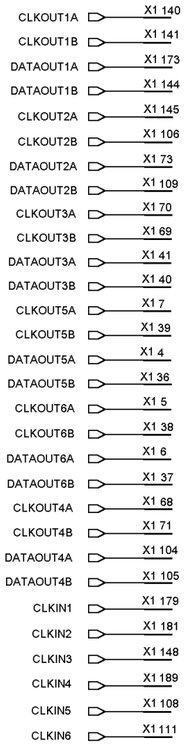
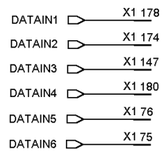
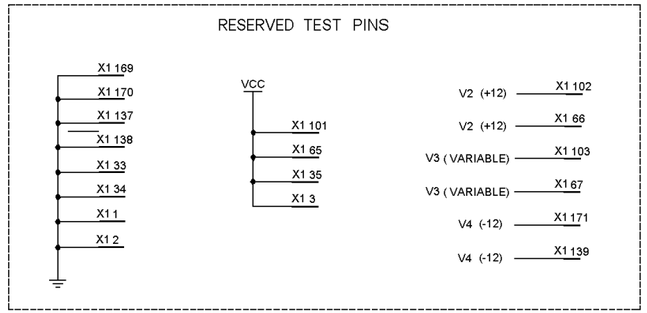


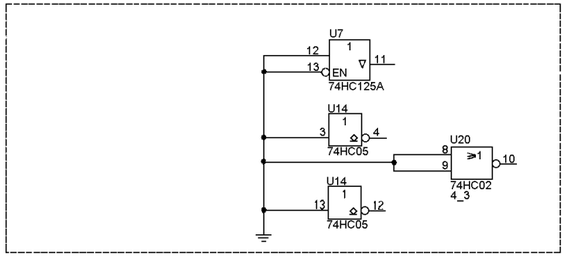






		GND	VCC
U1	3042A-70	04 16	03 27
U1	3042A-70	28 53	41 55
U1	3042A-70	66 77	79
U1	3042A-70		91
U2	DS14C89	7	14
U3	74ACT2228	7	19
U4	74HC04	7	14
U5	74HC02	7	14
U6	74HC14	7	14
U7	74HC125A	7	14
U8	DS14C89	7	14
U9	74ACT2228	7	19
U10	1736	10	17 20
U11	74ACT2228	7	19
U12	TLC555ID	1	08
U14	74HC05	7	14
U15	LTC486CS	8	16
U16	LTC486CS	8	16
U17	LTC486CS	8	16
U18	DS14C89	7	14
U20	74HC02	7	14

SPARES



LAST REF USED

P2	X1
R13	TP513
C41	S1
U20	F1
V3	Y1

(1911 ROA 117 2263, Sh. 4, Rev. B)