MAINTENANCE MANUAL

LOW SPEED DATA SELECTOR
ROA 117 2262

TABLE OF CONTENTS

SPECIFICATIONS

Input Voltage	+5 Vdc ± 10%
Connector	P1-A30, A31, B30, B31
Ground	J-A1, B1, C1, A32, B32, C32
Temperature	-30°C to +60°C
Dimensions	8 inches long x 4.0 inches wide
Digital/Data type:	
Tx	RS-422
Rx	RS-232
Analog/Audio Type	None

ERICSSON

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AE/LZB 119 1880 R1A
Printed in U.S.A.

Connector P1 Definition

Connector	Signal Name	Input/Output	Analog/Digital	Level
P1-A1	Ground	I		0 Vdc
P1-A2	IN1	I	D	RS-232
P1-A3	IN2	I	D	RS-232
P1-A4	IN3	I	D	RS-232
P1-A5	IN4	I	D	RS-232
P1-A6	IN5	I	D	RS-232
P1-A7	IN6	I	D	RS-232
P1-A8	IN7	I	D	RS-232
P1-A9	IN8	I	D	RS-232
P1-A10	IN9	I	D	RS-232
P1-A11	IN10	I	D	RS-232
P1-A12	IN11	I	D	RS-232
P1-A13	IN12	I	D	RS-232
P1-A14	IN13	I	D	RS-232
P1-A15	IN14	I	D	RS-232
P1-A16	IN15	I	D	RS-232
P1-A17	IN16	I	D	RS-232
P1-A18	IN17	I	D	RS-232
P1-A19	IN18	I	D	RS-232
P1-A20	IN19	I	D	RS-232
P1-A21	IN20	I	D	RS-232
P1-A22	IN21	I	D	RS-232
P1-A23	IN22	I	D	RS-232
P1-A24	IN23	I	D	RS-232
P1-A25	IN24	I	D	RS-232
P1-A30	Power	I		5 Vdc
P1-A31	Power	I		5 Vdc
P1-A32	Ground	I		0 Vdc

Continued

Connector	Signal Name	Input/Output	Analog/Digital	Level
P1-B1	Ground	I		0 Vdc
P1-B30	Power	I		5 Vdc
P1-B31	Power	I		5 Vdc
P1-B32	Ground	I		0 Vdc
P1-C1	Ground	I		0 Vdc
P1-C2	LSD1-	O	D	RS-422
P1-C3	LSD1+	O	D	RS-422
P1-C4	LSD2-	O	D	RS-422
P1-C5	LSD2+	O	D	RS-422
P1-C6	LSD3-	O	D	RS-422
P1-C7	LSD3+	O	D	RS-422
P1-C8	LSD4-	O	D	RS-422
P1-C9	LSD4+	O	D	RS-422
P1-C10	LSD5-	O	D	RS-422
P1-C11	LSD5+	O	D	RS-422
P1-C12	LSD6-	O	D	RS-422
P1-C13	LSD6+	O	D	RS-422
P1-C14	LSD7-	O	D	RS-422
P1-C15	LSD7+	O	D	RS-422
P1-C16	LSD8-	O	D	RS-422
P1-C17	LSD8+	O	D	RS-422
P1-C18	ACTIVE	O	D	TTL
P1-C19	RC-IN	I	D	TTL
P1-C20	RC-OUT	O	D	TTL
P1-C21	(SPARE)			
P1-C22	(SPARE)			
P1-C23	MINOR_ALARM	O	D	TTL
P1-C24	MAJOR_ALARM	O	D	TTL
P1-C25	(SPARE)			
P1-C26	(SPARE)			
P1-C27	(SPARE)			
P1-C28	(SPARE)			
P1-C29	(SPARE)			
P1-C30	-12 VDC	NC		-12 Vdc
P1-C31	+12 VDC	NC		+12 Vdc
P1-C32	Ground	I		0 Vdc
SW-1	Manual Advance			
SW-2	Test Mode			
SW-3	Channel Scan Set			

NOTICE!

Repairs to this equipment should be made only by an authorized service technician or facility designated by the supplier. Any repairs, alterations or substitution of recommended parts made by the user to this equipment not approved by the manufacturer could void the user's authority to operate the equipment in addition to the manufacturer's warranty.

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DESCRIPTION

Low Speed Data (LSD) Selector Module ROA 117 2262, used in the GPS Simulcast System, automatically selects a 150 Baud Data stream (Low Speed Data) from one of twenty-four Control Point Trunking Cards (CPTC). All CPTC's generate identical low speed data except for the active control channel CPTC (Figure 1). The channel number of the selected LSD source is displayed on the front of the LSD Selector Module, two digit LED display (Figure 2).

The function of the LSD Selector module is to receive low speed data from the CPTC's, pass this data through multiplexer circuits on the selector module and select a single 150 Baud Data Stream. This data stream is then buffered at RS-422 and routed through a jackfield to the Intraplex Multiplexer. There are eight (8) redundant outputs from the LSD Module. Six of them are input through a jackfield to the Intraplex Multiplexer. The other two (2) outputs are spares.

The interfaces are RS-422 differential. This requires that the multiplex outputs from the LSD Selector module be converted to RS-422.

The LSD Selector Module, used at the Control Point only, plugs into slots 3 (PS3) and 4 (PS4) of the Synch Shelf (refer to Sync Shelf Maintenance Manual AE/LZB 119 1903). Two LSD Selector Modules are used for redundancy.

Clock and Control circuitry on the LSD Selector Module provide the scanning mechanism to select a channel or source that contains a valid low speed data stream. The scan rule used is the presence of an active falling edge on the RS-232C input within ten clock cycles. The clock cycle corresponds to 75 Hz. Should the channel or source fail, the LSD Selector Module automatically advances to the next channel and scans for a valid data stream during a 10 clock cycle time. This continues until a valid stream is found.

Momentary switch SW1 (ADVAN) enables a manual advance function. This switch bypasses a portion of the scanning circuitry and allows a forced increment in the selected channel number. The low speed data selection will increment until a signal is found and a valid lock is established.

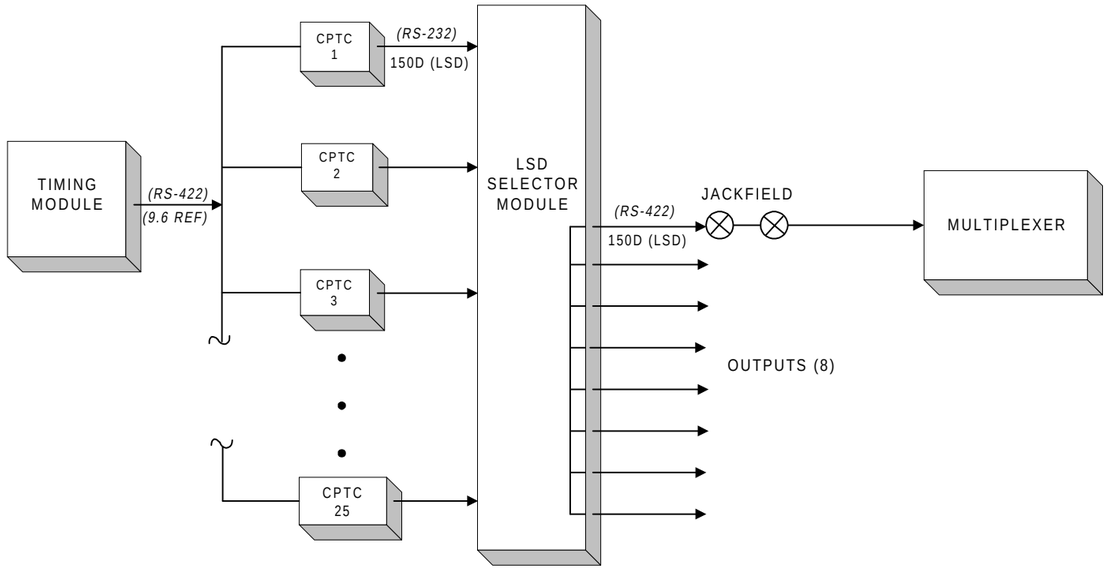


Figure 1 - Control Point Low Speed Data

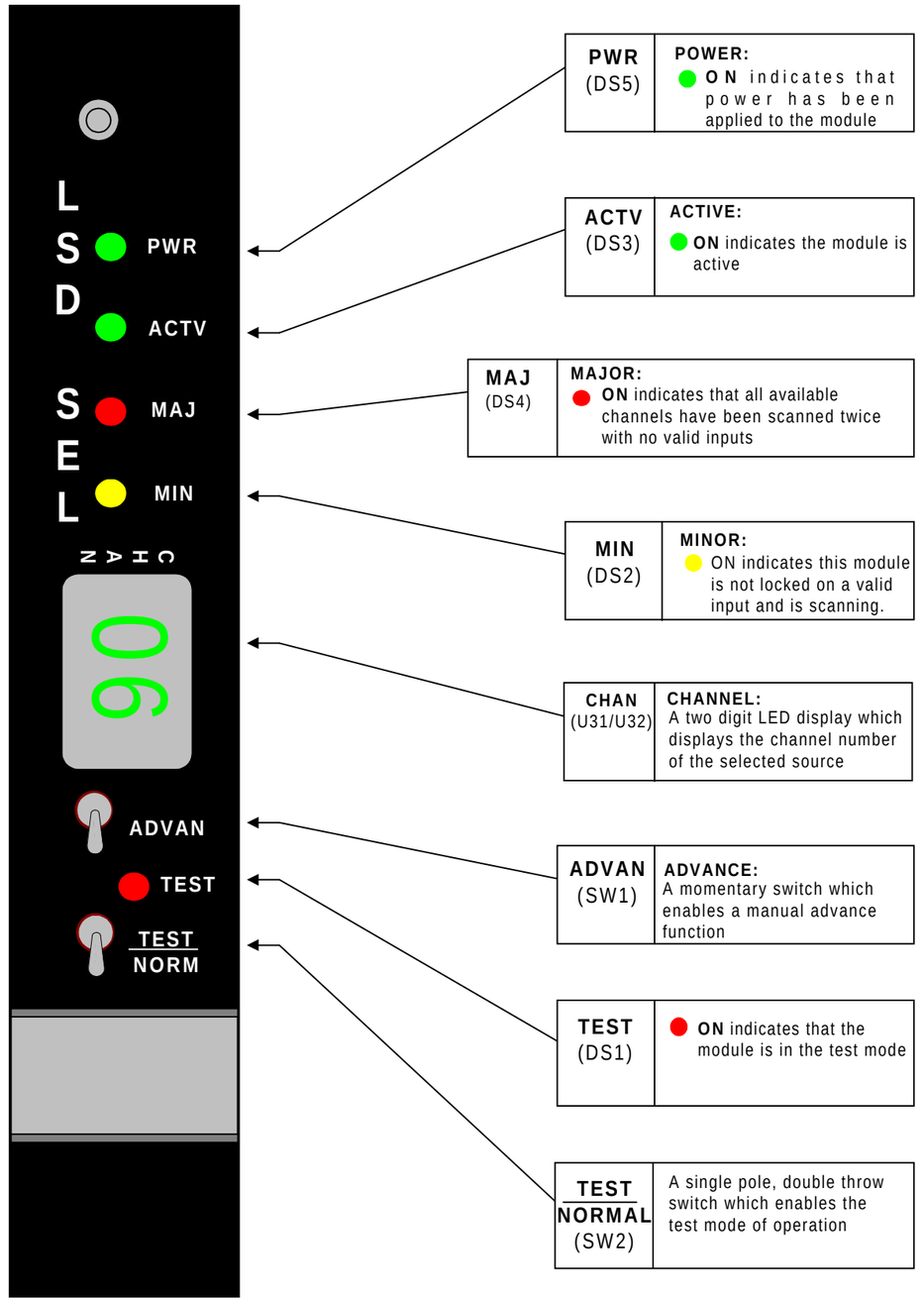


Figure 2 - LSD Selector Front Panel

Single pole, double throw switch SW2 (TEST/NORM) enables the test mode of operation. In the test mode a fixed 75 Hz is used as the data stream output. Red LED DS1 (TEST) illuminated indicates that the module is in the test mode.

Two numeric LED displays indicate the number of the valid (locked-on) signal. A PROM is used for the table look-up in generating the LED matrix display from the binary adddress of the locked on channel. The number displayed will be from 1 to the number of channels in the system.

The LSD Selector generates two alarms, minor and major. The minor alarm displayed by a yellow LED DS2 (MIN) on the front panel indicates when this module is not locked on a valid input and is scanning. The major alarm is displayed by red LED DS4 (MAJ) on the front panel. DS4 indicates when the LSD Selector Module has scanned through all available channels at least twice with no valid input.

Green LED DS5 (PWR) on the front panel indicates power to the module.

Green LED DS3 (ACTV) on the front panel indicates the module is active.

CIRCUIT ANALYSIS

INPUTS

CPTC inputs on connector P1, A2 - A25 (IN1 - IN24) to the LSD Module come from each of separate 24 CPTC channels. The number of channels selectable corresponds to the number set by the DIP switches on DIP switch package SW3. The maximum number of channels that can be selected is by SW3 is 32. However, the LSD module only provides for 24 inputs. These inputs are converted from RS-232 levels to TTL levels by Line Driver Receivers U3-U8. The input (i.e. channel 1) IN1 connects through line driver U8 and multiplexers U12 and U13 (Figure 3).

MULTIPLEXERS

After the input on IN1 is converted to the proper logic level through line driver U8, it is sent to 8:1 multiplexers U12 & U13 where it waits to be selected.

The multiplexers consist of U10-U13. These devices scan up to 24 sources. The low speed data is taken from inputs IN1-IN24 and buffered through RS-232C Line Receivers U3-U8.

NOTE

If there are no signals present on any of the channels, then all logic "highs" will be on the inputs to these multiplexers.

The LSD module is put in the test mode by switch SW2. Placing SW2 in the TEST position places a logic one (1) on multiplexer U13, Pin 9. The 75 Hz TEST_CLK is selected and LED indicator DS1 (TEST) lights.

The 8:1 multiplexers take the steering (address or select inputs) from the lowest three bits of channel address counters U28 and U29 (Figures 3&4). Multiplexer U13 selects one of the three 8:1 multiplexer (U10, U11 or U12) or a fixed 75 Hz from clock divider U23.

The select control for U13 is taken from the most significant two bits of the channel address and the test enable switch position. If the test is enabled LED DS1 is illuminated and a high is on U13, Pin 9. This steers the 75 Hz to the SELOUT line. If the test is disabled, the two channel address lines SEL16 and SEL8 select the three LSD multiplexer (U10-U12).

The three data multiplexers use the select lines SEL4, SEL2 and SEL1 from channel address counters U28 and U29 to select one of 8 inputs per device.

The SEL_OUT on U13, Pin 5 connects to the input of flip-flop U18, Pin 3 (Figure 4). The output on U18, Pin 5 connects through NOR gates U24 to the DATA input of U18, Pin 12. The Q\ output (U18TOU28) on U18, Pin 8 connects to the input of address counter U28, Pin 4.

MANUAL ADVANCE

Momentary switch SW1 (ADVAN) toggles flip-flops U17 to cause NOR gates U24 to trigger flip-flop U18, advancing the U18TOU28 data output (Figure 5). The output on U18, Pin 8 connects back to U17, Pin 3 to clear U17 and end the manual advance.

Synchronous 4-Bit Decade Counter U16 provides a clock for U18 and flip-flop U25. Flip-flop U25 toggles by the absence of data on U18, Pin 5. This produces a SEL_ALARM output on U25, Pin 5. The input to U16 is taken from digital select oscillator U23 and U15.

BINARY UP/DOWN COUNTERS

The U18TOU28 output of U18, Pin 8 connects to the input of Binary Up/Down counter U28, Pin 4. The output of U28, Pin 13 connects to the input of U29, Pin 4 (Figure 5) These two counters provide the scan function for scanning through all channels to find one that is valid. The number of channels scanned is determined by the settings of DIP switch package SW3. This switch package is set in binary to the number of channels in the Simulcast system. Counters U28 and U29 provide the select lines SEL1, SEL2, SEL4, SEL8 and SEL16 which connect to the multiplexers to select the valid channel. These same outputs connect to I/O's of PROM U20 (Figure 8).

ADDRESS SCAN COUNTING

The output of U28, Pin 13 connects to the input of two input NOR gate U30. Pin 3. The output of U29. Pin 13 connects to the other input of NOR gate 30, Pin 2 (Figure 5). The output of U30, Pin 4 connects to the input of address scan counters U14 and U25 (Figure 6). This circuit counts through two complete scan cycles. If an active channel is not found after two cycles, an alarm signal (S_L2ALARM) is applied to the input of AND gate U27, Pin 4 (Figure 9).

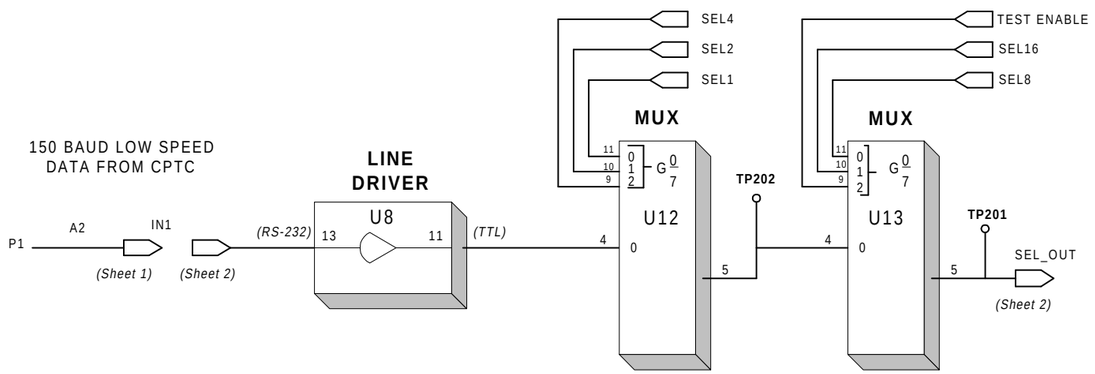


Figure 3 - Input for Channel 1 (IN1)

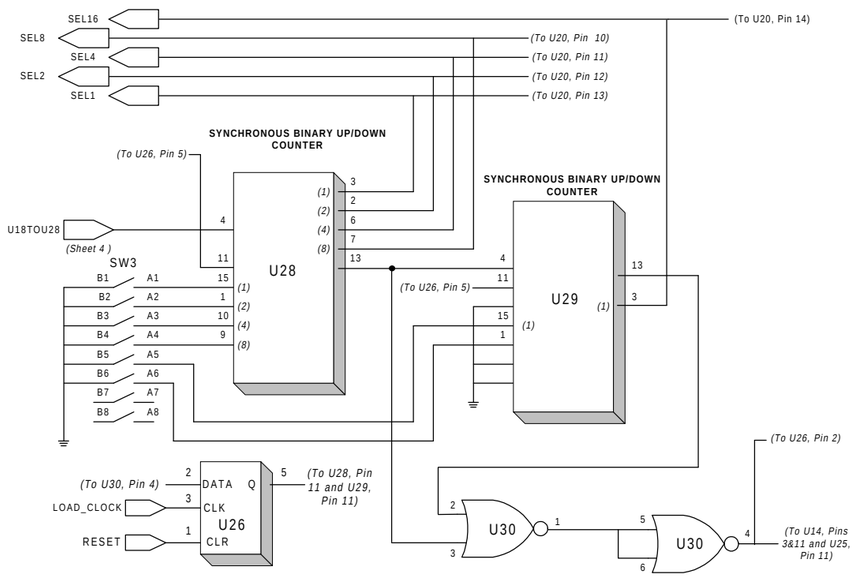


Figure 4 - Binary Up/Down Counters

DIGITAL SELECT OSCILLATOR

The digital select oscillator consist of a free running 1.23 KHz clock derived from 555 timer U23 (Figure 7). Resistor R1 and R2 and capacitors C1 and C2 determine the nominal free running frequency.

The 1.23 kHz output (U23, Pin 3) is input to binary counter U15 (U15, Pin 1). The outputs of U15 consist of a LOAD_CLOCK signal on Pin 3 and a 75 Hz clock on Pin 6.

The LOAD_CLOCK signal connects to Flip-Flop U26 which is part of the start up reset circuit.

The 75 Hz clock is used for test mode and edge detection of SEL_OUT on U18, Pin 3.

DIP SWITCH PACKAGE SW3

Switch Package SW3 DIP switches are set to the number of channels that the system has (up to 24). These DIP switches are the preset inputs to binary up/down counters U28 and U29. The counters are configured in such a way that they will count down from the highest number of channels selected to zero and then repeat. Seven segment display circuits U21 and U22, and U31 and U32 show the channel numbers (Figure 8). The up/down counters, as they are counting down, will select each input that is on the multiplexers. If a signal is present on the first channel that is selected, this is the channel that the low speed data is taken from and the channel is displayed on the front panel of the module. If a signal is not present on the selected channel, the counters continue to count down until a valid channel is found.

MAJOR AND MINOR ALARMS

Two LED's DS4 (MAJ) and DS2 (MIN) indicate alarms. When there is no signal found on any channel, while the card is searching for a channel with a signal, the MIN LED DS2 lights and ACTV LED DS3 goes out until another channel with a signal is found. Then, the ACTV LED, lights and the MIN LED goes out. If counters (U14 and U25) cycle through twice without finding a signal, then the MAJ LED lights along with the already lit MIN LED. This is an indication of a major alarm which means that the card could not find a channel with a signal.

When a SEL-ALARM signal is on U36, Pin 13 indicating that no active channel has been found, the MIN LED lights. When a S-L2ALARM signal is on U27, Pin 4 and the SEL_ALARM signal is on U27, Pin 5, the MAJ LED DS4 lights.

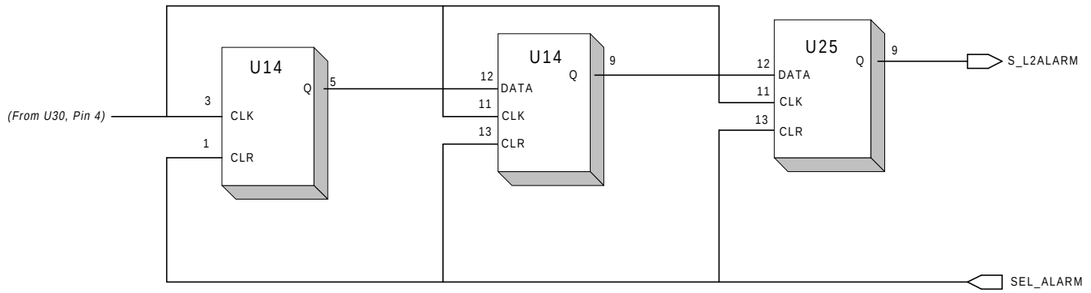


Figure 6 - Address Scan Counters

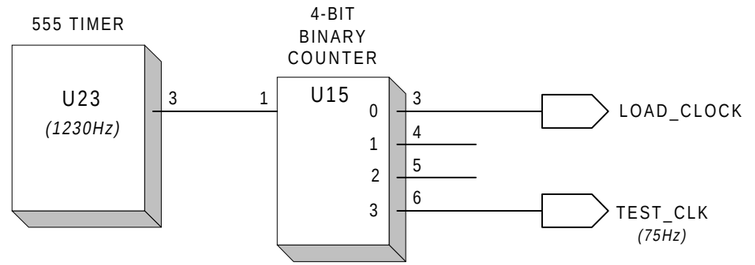


Figure 7- Digital Select Oscillator

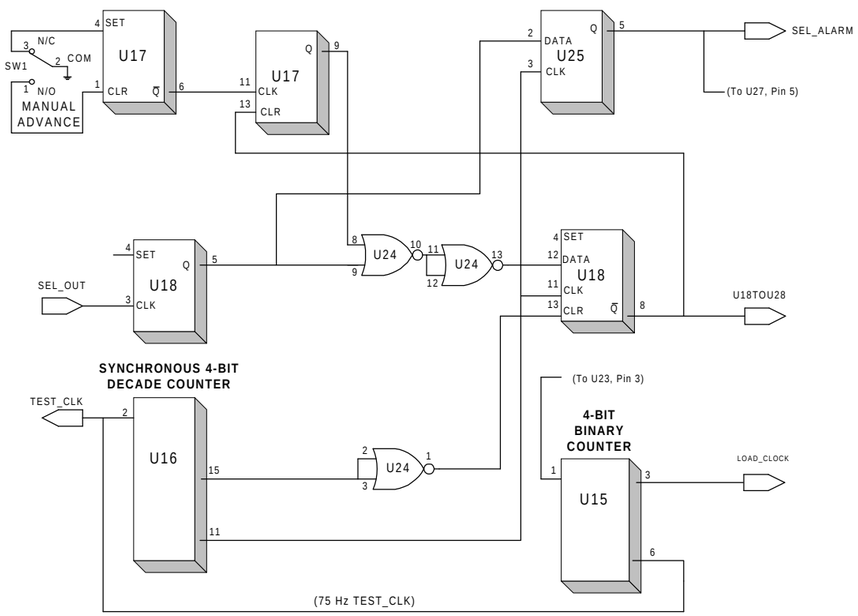


Figure 5 - Manual Advance

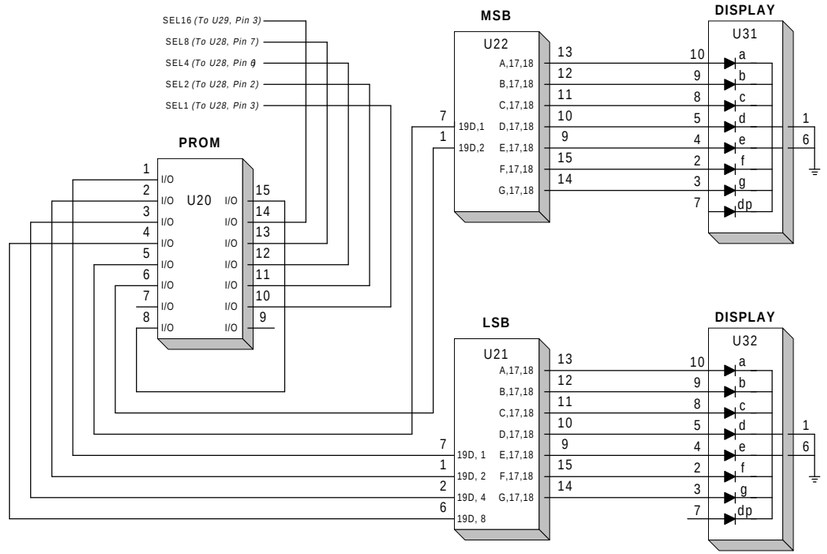


Figure 8 - Two Digit LED Display

ACTV LED

When the LSD selector finds a channel with a signal on it, the counters stops counting at that channel. There is no SEL_ALARM signal on inverter U19, Pin 6 or RC_IN (Redundant Control) signal from a redundant LSD on inverter U33, Pin 5, the ACTV LED DS3 lights.

OUTPUTS

The SEL_OUT signal (selected low speed data stream) from U13, Pin 5 connects to the inputs of RS-485 quad drivers U1 & U2 (Figure 11). An OUT_ENABLE signal for U1 & U2 is derived from the ACTIVE detect circuit and is applied to Pin 12 of each driver (Figure 11).

Outputs of U1 & U2 connect to connector P1, C2-C17 (LSD1-LSD8). When a channel with a signal is detected, these outputs will all have the same signal.

POWER-UP RESET

Microprocessor supervisory circuit U9 produces a power-up RESET signal (Figure 10). This is accomplished by holding the output on U9, Pin 7 at logic 0 for 200 milliseconds when power is initially applied to the LSD module. The output on U9, Pin 7 connects to NAND gate U27, Pin 9 in the activity detect circuit and to flip-flop U26, Pin 1 (CLR). This signal on U27, Pin 9 keeps the module inactive and ACTIVE LED DS3 from lighting until a scan has occurred and an active channel selected. The output on U26, Pin 5 provides a synchronized load for counter circuits U28 and U29. The RESET signal on flip-flop U26, Pin 1 resets and holds the load signal for 200 milliseconds. During this time switch SW3 settings for the preset channel limits are loaded into counters U28 and U29. At the end 200 milliseconds U28 and U29 start counting from the preset channel limit.

REDUNDANT CONTROL

Redundant control line RC_IN and RC_OUT control the operation of redundant LSD Modules. If one LSD Module is active the RC-IN line of the inactive one will be a logic low on buffer U33, Pins 5 & 6. This low will also be on NAND gate U27, Pin 1. Since the SEL_ALARM is a logic low on the active LSD, U19, Pin 5 will be low. U19, Pin 6 will high. The input to U27, Pin 2 will be high. The output of U27, Pin 8 will be high and the ACTIVE LED will be on. If the other LSD Module is active the input RC_IN will be low resulting in the ACTIVE LED of the inactive module being off.

Integrated circuits U19 and U36, provide the appropriate logic level for the RC_OUT signal to the other redundant LSD Module. RC_OUT connects to RC_IN of an other module. The output of buffer U33 provides an ACTIVE signal to the Integrated EDACS Alarm System (IEA) as an indication as to which LSD Module is active.

POWER DISTRIBUTION AND FILTERING

The +5 Vdc power used by the LSD Module is taken from the Simulcast power supply. The + 5Vdc power input (+5) is used to power all active components on the LSD Module. The active components include 8:1 multiplexers U10-U13, the RS-232C line drivers U3-U8, 1230 Hz oscillator U23, scanning circuitry U28 & U29, PROM U20 and LED matrix display circiuts U21, U22, U31 & U32.

The +5Vdc is applied to the LSD Module at connector P1 A30, A31, B30 and B31 (+5VDC). This 5 volt line is fused using 0.5 Amp thermister fuse F1. When power is applied to the module and the fuse is good, the green POWER LED DS5 is on.

Power bypass capacitors C3 through C28 filter power noise transients or spikes from the 5 volt supply to prevent them from affecting circuit operation and module performance.

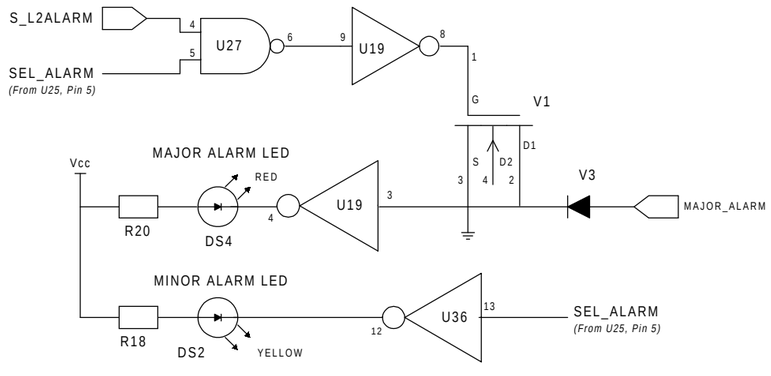


Figure 9- Alarm LED's

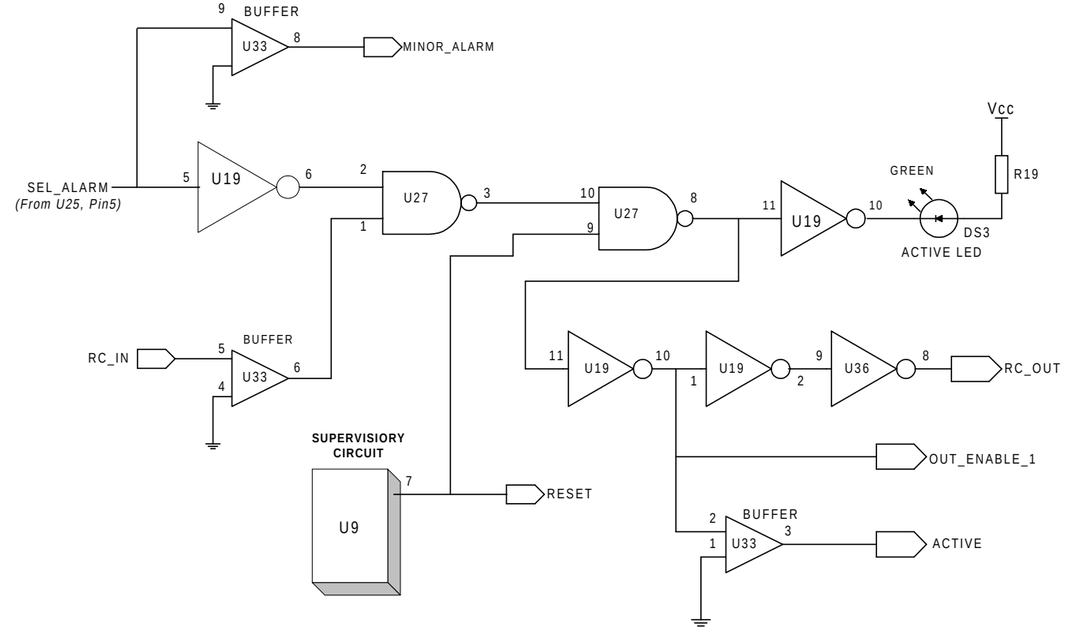


Figure 10 - Active LED

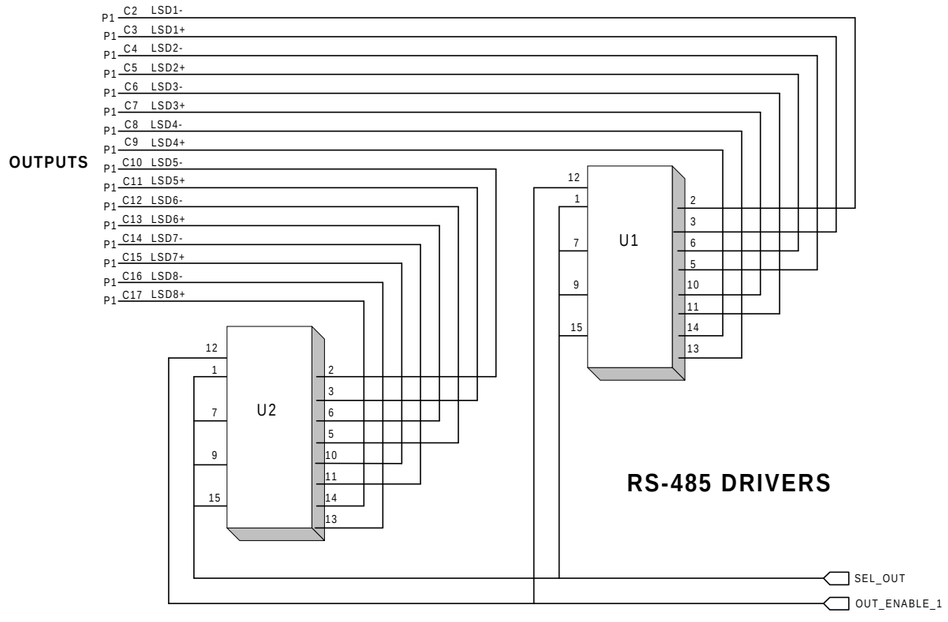


Figure 11 - Outputs

SWITCH SW3 SETTING PROCEDURE

The desired number of selectable channels is preset on the data inputs of high speed synchronous counters U28 & U29 using switch SW3 (Figure 4). The number to the left of the switch is the number of channel selected to be scanned.

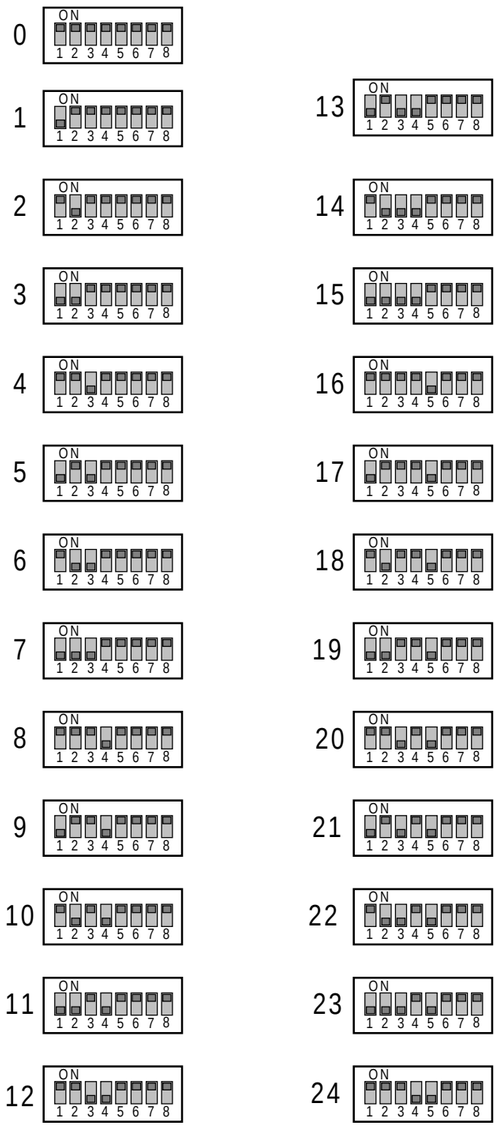


Figure 12 - Switching Settings

TEST PROCEDURE

Required Equipment:

- + 5 Vdc power supply
- Multimeter (voltage, continuity and frequency)
- Function Generator (Square wave)

Continuity Test:

Using the multimeter check for a short circuit between power and ground on the assembly.

Power Pins	Ground Pins
A30	A1
A31	B1
B30	C1
B31	A32 B32 C32

Test Procedure:

1. Apply +5 Vdc power to one of the power pins A30, A31, B30 or B31and ground to one of the ground pins A1, B1, C1, A32, B32 or C32.
2. Check all ground and power pin connections.
3. Place a 75 Hz square wave (RS-232 level) on Pin A2 and check and record distribution on output pins.

Output Pins	Results
C3	
C5	
C7	
C9	
C11	
C13	
C15	
C17	

4. Apply a 75 Hz square wave signal on channels 1 through 24 inputs (A2-A25) and look for an output signal. Check that the channel number is displayed on the 7-segment display.

Channel	Results
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	

5. Check Test Mode
   a. Switch 2 in up position.
   b. Disconnect all input signals (IN1-IN24, A2-A25).
   c. Check for 75 Hz output signal on U18TOU2, C3-C9 and C11-C17.
6. With switch 2 in the down position apply an input signal to IN1, A2. Press and release switch 1. The output signal should disappear then reappear.
7. Check LED's
   a. DS5 (Power).
   b. DS3 (Apply an input signal).
   c. DS1 (switch 2 is Up).
   d. DS2 (Remove the input signal Pin C20 (RC_OUT).
   e. DS4 & DS2 (Remove all input signals).

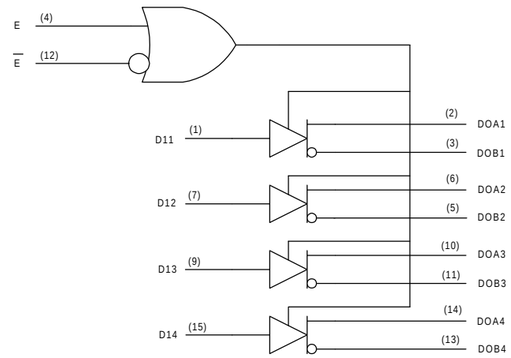
LSD SELECTOR MODULE
ROA 117 2262

SYMBOL	PART NO.	DESCRIPTION
		- - - -CAPACITORS- - - -
C1	RJC 464 3045/1	10 nF, ±10%, 50 V.
C2	RJA 532 4056/1	0.1µF, 16 V.
C3 thru C26	RJC 463 4043/1	100pF, ±5%, 50 V.
C27 and C28	RJE 599 1258/1	10 µF, ±20%, 25 V.
C29 thru C52	RJC 463 4043/47	470 pF, ±5%, 50 V.
C53	RJE 584 3638/47	Tantalum: 47 µF, 6.3 V.
		- - - -DIODES- - - -
DS1	RKZ 433 637/1	LED, Red, 90° Angled.
DS2	RKZ 433 637/2	LED, Yellowd, 90° Angled.
DS3	RKZ 433 637/3	LED, Green, 90° Angled.
DS4	RKZ 433 637/1	LED, Red, 90° Angled.
DS5	RKZ 433 637/3	LED, Green, 90° Angled.
		- - - -FUSE- - - -
F1	REZ 701 28/1	0.5 Amp, 15V, PTC/Thermistor.
		- - - -PLUGS- - - -
P1	RPV 403 804/03	96 position DIN/PIN Connector.
		- - - -RESISTORS- - - -
R1 and R2	REP 625 424/39	Metal Film: 3.9k Ohms ± 5%, 1/8 Watt.
R3 thru R6	REP 625 424/47	Metal Film: 4.7k Ohms ± 5%, 1/8 Watt.
R7	REP 625 423/47	Metal Film: 470 Ohms ± 5%, 1/8 Watt.
R8 thru R13	REP 625 424/27	Metal Film: 2.7k Ohms ± 5%, 1/8 Watt.
R14 thru R20	REP 625 423/47	Metal Film: 4.7k Ohms ± 5%, 1/8 Watt.
R15	REP 625 425/47	Metal Film: 47k Ohms ±5%, 1/8 Watt.
R16	REP 625 424/47	Metal Film: 4.7k Ohms ± 5%, 1/8 Watt.
R18 thru R20	REP 625 423/47	Metal Film: 4.7k Ohms ± 5%, 1/8 Watt.
R21 thru R34	REP 623 643/33	Metal Film: 330 Ohm, ±1%, 0.06 Watt.
		- - - -SWITCHES- - - -
SW1	RMF 356 101/03	1-Pole, 2-Positions, 2-3 ON, 1-2 Momentary.
SW2	RMF 356 101/02	1-Pole, 2-Position, 2-3 ON, 1-2 ON.
SW3	RMF 356 001/08	Dip Switch, 8-Positions.
		- - - -TEST POINTS- - - -
TP201 thru TP204	RPV403 813/01	Test Point for board level troubleshooting.

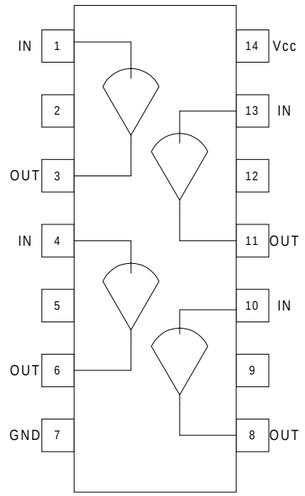
*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES.

SYMBOL	PART NO.	DESCRIPTION
		- - -INTEGRATED CIRCUITS- - -
U1 and U2	RYT 109 6078/1C	RS-485 Quad Driver: Sim to LCT486CS.
U3 thru U8	RYT 109 003/2C	Quad Line Receiver: Sim to DS14C89.
U9	RYT 113 6065/1	Microprocessor Supervisory Circuit: Sim to MAX705CSA.
U10 thru U13	RYT 304 0151/C	1 of 8 Input Multiplexer: Sim to 74HC151.
U14	RYT 306 2003/C	Dual D Flip-Flop: Sim to 74HC74.
U15	RYT 306 6028/C	Dual 4-Bit Binary Counter: Sim to 74HC393.
U16	RYT 306 6043/C	Synchronous 4-Bit Decade Counters: Sim to 74HC160.
U17 and U18	RYT 306 2003/C	Dual D Flip-Flop: Sim to 74HC74.
U19	RYT 304 0004/C	Hex Inverter: Sim to 74HC04.
U20	PROM	Factory programmed.
U21 and U22	RYT 304 1112/C	BCD-To- 7Seg Display Driver: Sim to 74HC4511.
U23	RYT 108 6003/C	555 Timer: Sim to TLC555ID.
U24	RYT 306 2006/C	Quad NOR Gate: Sim to 74HC02.
U25 and U26	RYT 306 2003/C	Dual D Flip-Flop: Sim to 74HC74.
U27	RYT 304 0008/C	4x2 AND Gates: Sim to 74HC08.
U28 and U29	RYT 306 2034/C	Synchronous Binary Up/Down Counters: Sim to 74HC193.
U30	RYT 306 2006/C	Quad NOR Gate: Sim to 74HC02.
U31 and U32	RNH 921 515	7-Segment Display: Sim to HDSP-A513.
U33	RYT 306 6029/C	Quad Buffers: Sim to 74HC125A.
U36	RYT 306 6021/C	Hex Inverters with Open-Drain Outputs: Sim to 74HC05.
		- - - -TRANSISTORS- - - -
V1	RYN 123 621/1	Medium Power N-Channel Enhancement Mode MOSFET.
		- - - -DIODE- - - -
V3	RKZ 123 601	BAR43.
		- - - -SOCKET- - - -
XU20	RNK 841 001/16	I/O, 16-Position/Holder.
XU31 and XU32	PNK 855 410	90 For Display, 10-Position, Vertical.

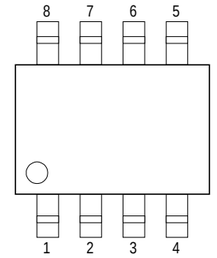
U1, U2
RS-485 QUAD DRIVER
RYT 109 6078/1C (TL486CS)



U3 thru U8
QUAD LINE RECEIVER
RYT 109 003/2C (DS14C89)

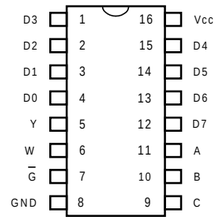


U9
MICROPROCESSOR SUPERVISORY CIRCUIT
RYT 113 6065/‘1 (MAX705CSA)



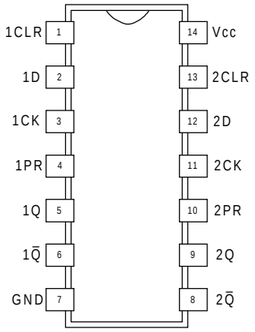
Terminal	Symbol	Function
1	MR\	Manual Reset Input
2	Vcc	Supply Voltage
3	GND	Ground
4	PFI	Power-Fail Voltage Monitor Input
5	PFO\	Power Fail Output
6	WDI	Watchdog Input
7	RESET\	Reset output pulse for 200 ms
8	WDO\	Watchdog Output

U10 thru U13
1 OF 8 INPUT MULTIPLEXER
RYT 304 0151/C (74HC151)



Terminal	Symbols	Function
1	D3	Data input 3
2	D2	Data input 2
3	D1	Data input 1
4	D0	Data input 0
5	Y	Non-Inverting Data Output
6	W	Inverting Data Output
7	G\	Enable Input (Active Low)
8	GND	Ground
9	C	Input Select Input C
10	B	Input Select Input B
11	A	Input Select Input A
12	D7	Data Input 7
13	D6	Data Input 6
14	D5	Data Input 5
15	D4	Data Input 4
16	Vcc	Supply Voltage

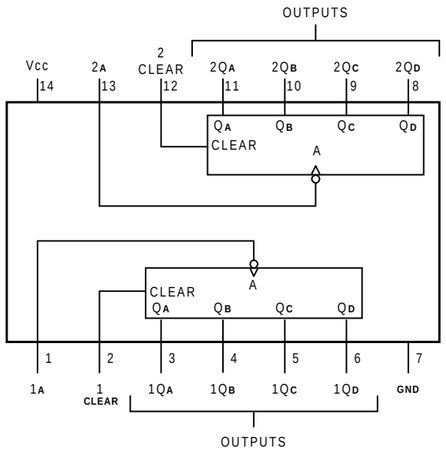
U14, U17 & U18,
DUAL D FLIP-FLOP-
RYT 306 2003/C (74HC74)



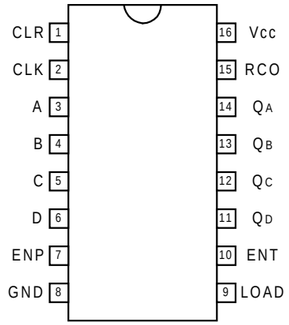
Inputs			Outputs		
Preset	Clear	Clock	D	Q	/Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	/Q0

↑ = Transition from low to high level
Q0 = The level of Q after the previous clock pulse
* = Non-stable, when PR and CLR are set low
X = Any input, including transition

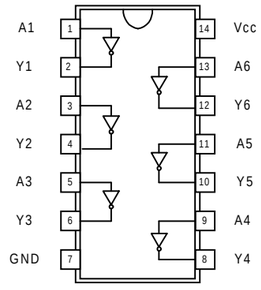
U15
DUAL 4-BIT BINARY COUNTER
RYT 306 6028/C (74HC393)



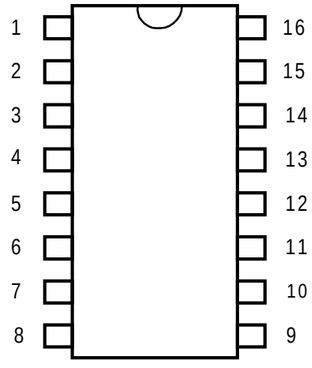
U16
SYNCHRONOUS 4-BIT DECADE COUNTER
RYT 306 6043/C (74HC160)



U19
HEX INVERTER
RYT 304 0004/C (74HC04)



U20
PROM
RYT 118 6102/1D (Blank PROM)
RON 107 788 (Factory Programmed PROM)

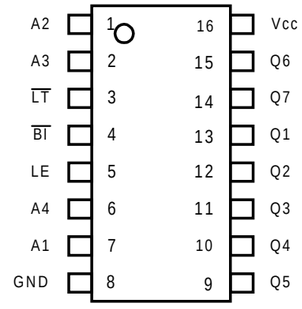


Continued

U20 Table

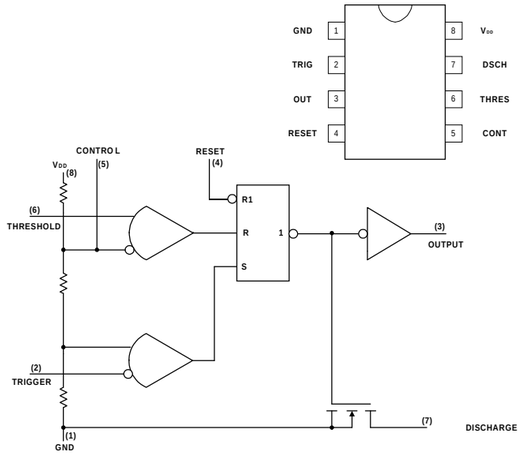
Terminal	Symbol	Function
1	01	Data Output
2	02	Data Output
3	03	Data Output
4	04	Data Output
5	05	Data Output
6	06	Data Output
7	07	Data Output
8	GND	Ground
9	08	Data Output
10	A0	Address Input
11	A1	Address Input
12	A2	Address Input
13	A3	Address Input
14	A4	Address Input
15	CE\	Chip Enable
16	Vcc	Supply Voltage

U21 & U22
BCD-TO-7-SEGMENT DISPLAY DRIVER
RYT 304 1112/C (74HC4511)

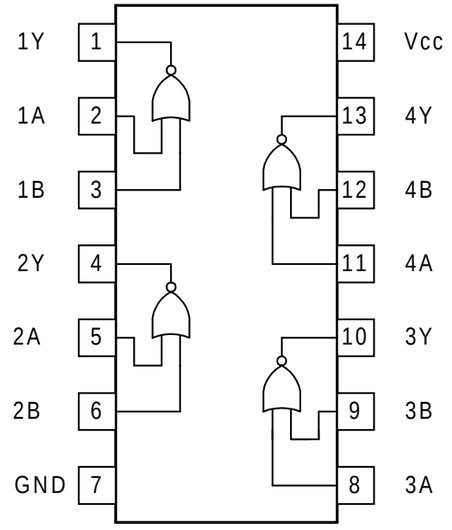


Terminal	Symbols	Function
16	Vcc	Supply Voltage
8	GND	Ground
3	LT\	Lampt Test Input (Active Low)
4	BI\	Blanking Input (Acitve Low)
5	LE	Latch Enable Inputs
7, 1, 2, 6	A1, A2, A3, A4	BCD Address Inputs
13, 12, 11, 10, 9, 15, 14	Q1, Q2, Q3, Q4, Q5, Q6, Q7	Segments Outputs

U23
555 TIMER
RYT 108 6003/C (TLC555ID)

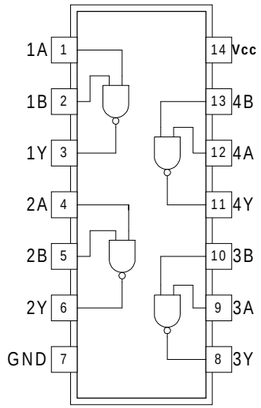


U24, U30
QUAD NOR
RYT 306 2006/C (74HC02)

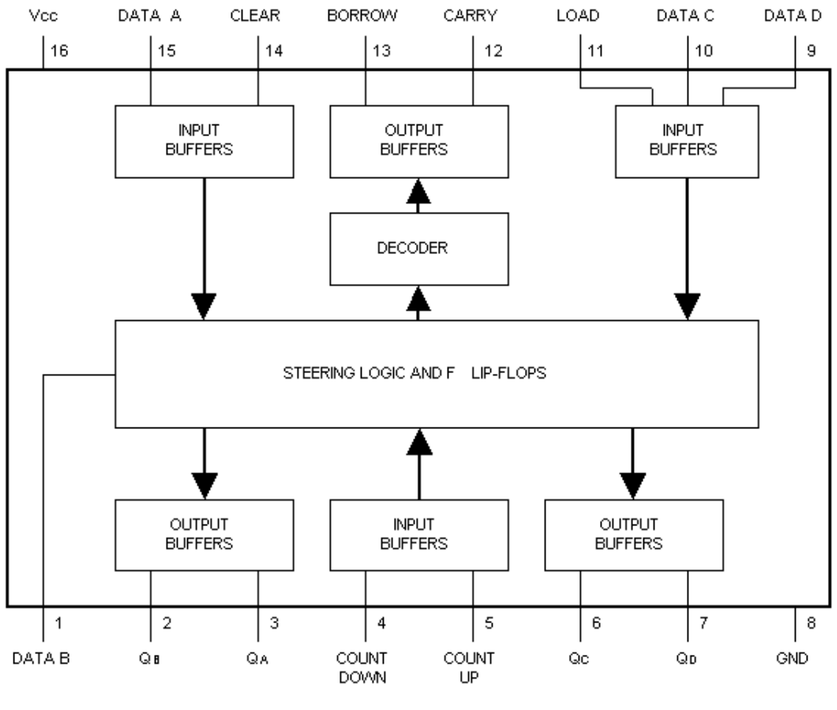


Positive Logic: Y=A+B

U27
QUAD AND GATES
RYT 304 0008/C (74HC08)



U28 & U29
SYNCHRONOUS BINARY UP/DOWN COUNTERS
RYT 306 2034/C (74HC193)

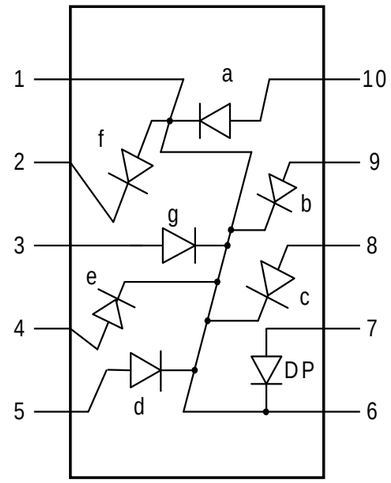


U28 & U29 - Truth Table

Count		Clear	Load	Function
Up	Down			
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Clear
X	X	L	L	Load

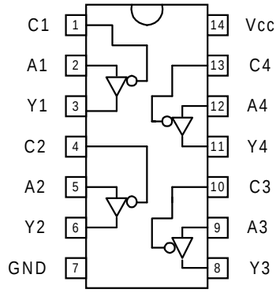
H = high level
L = low level
↑ = transition from low-to-high
X = don't care

U31 & U32
7-SEGMENT DISPLAY
RNH 921 515 (HDSP-A513)

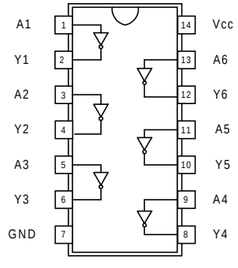


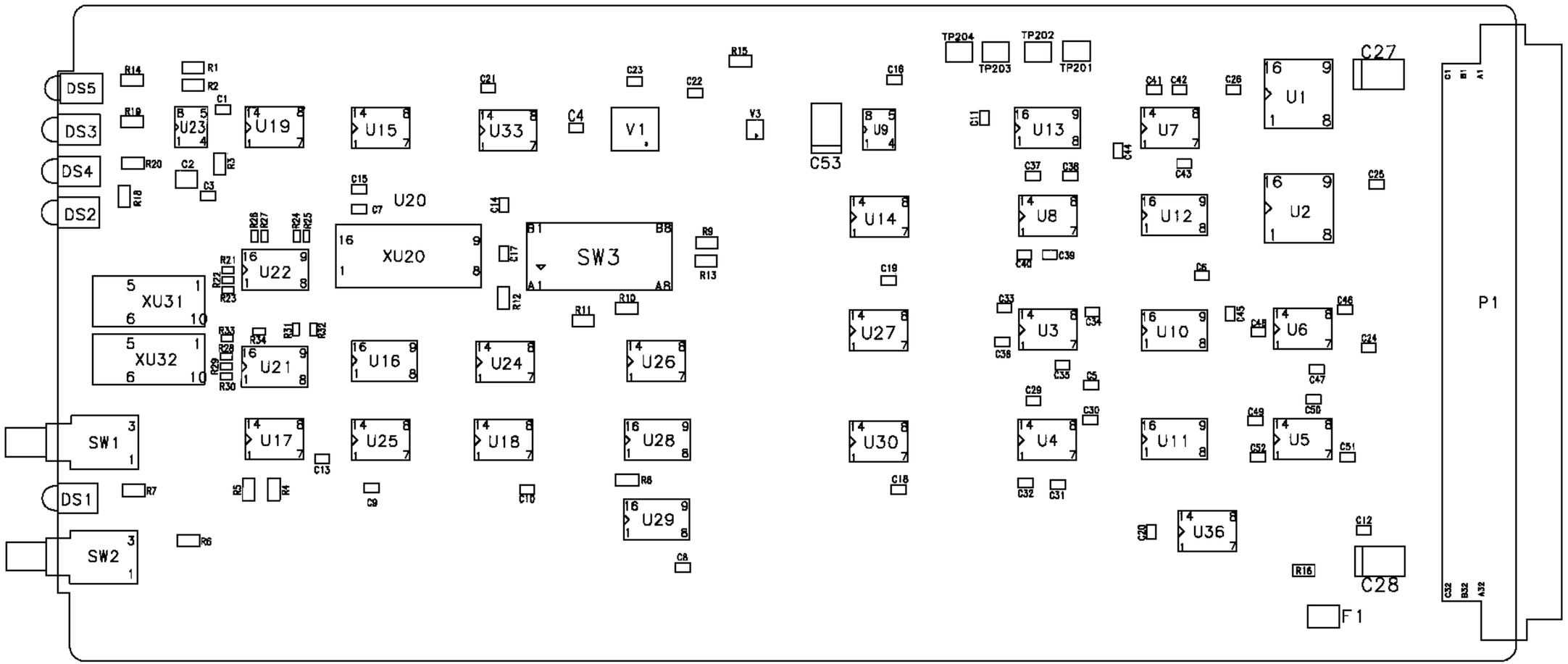
Terminal	Function
1	Cathode
2	Anode f
3	Anode g
4	Anode e
5	Anode d
6	Cathode
7	Anode DP
8	Anode c
9	Anode b
10	Anode a

U33
QUAD BUFFERS
RYT 306 6029/C (74HC125A)

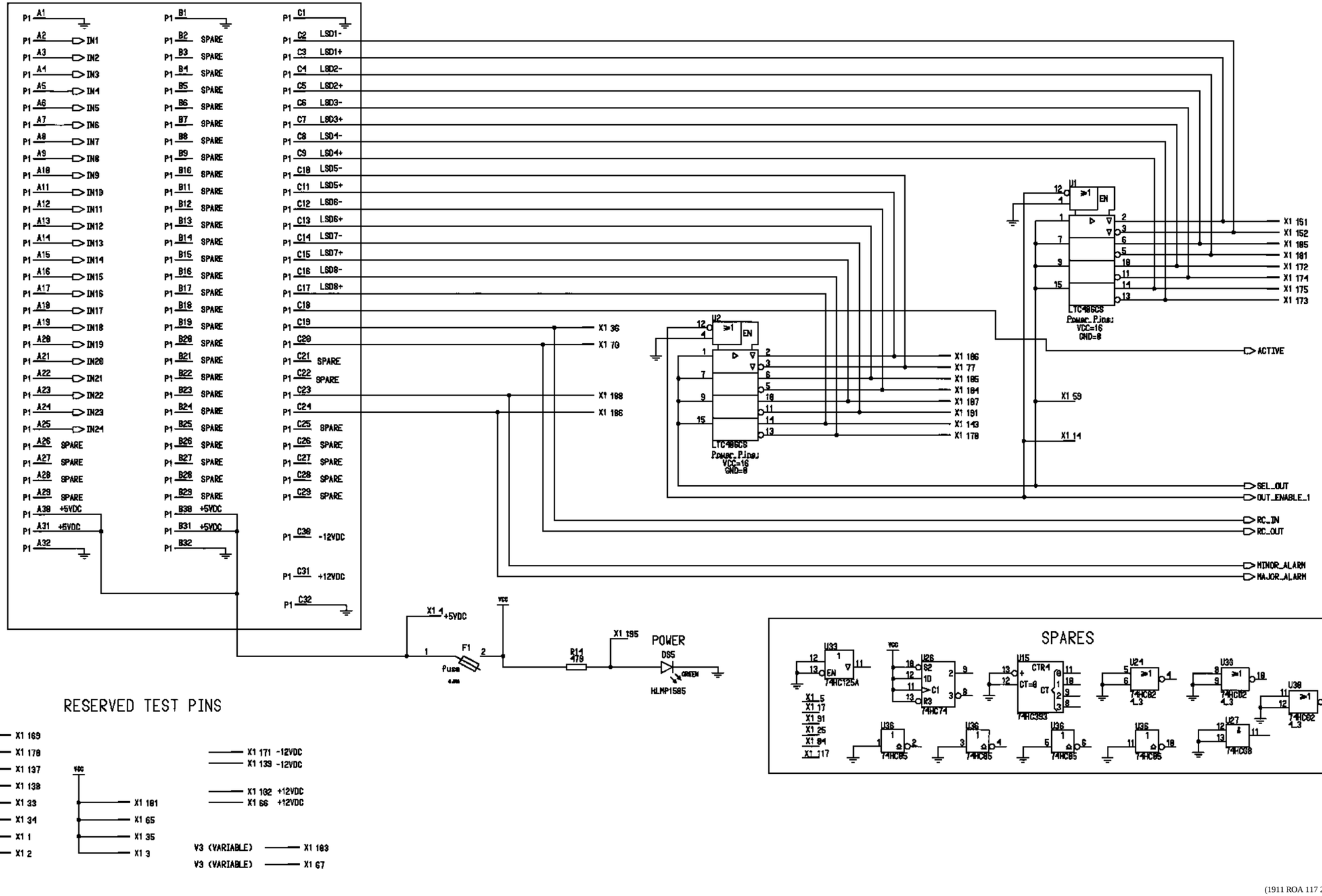


U36
HEX INVERTERS WITH OPEN-DRAIN OUTPUTS
RYT 306 6021/C (74HC05)

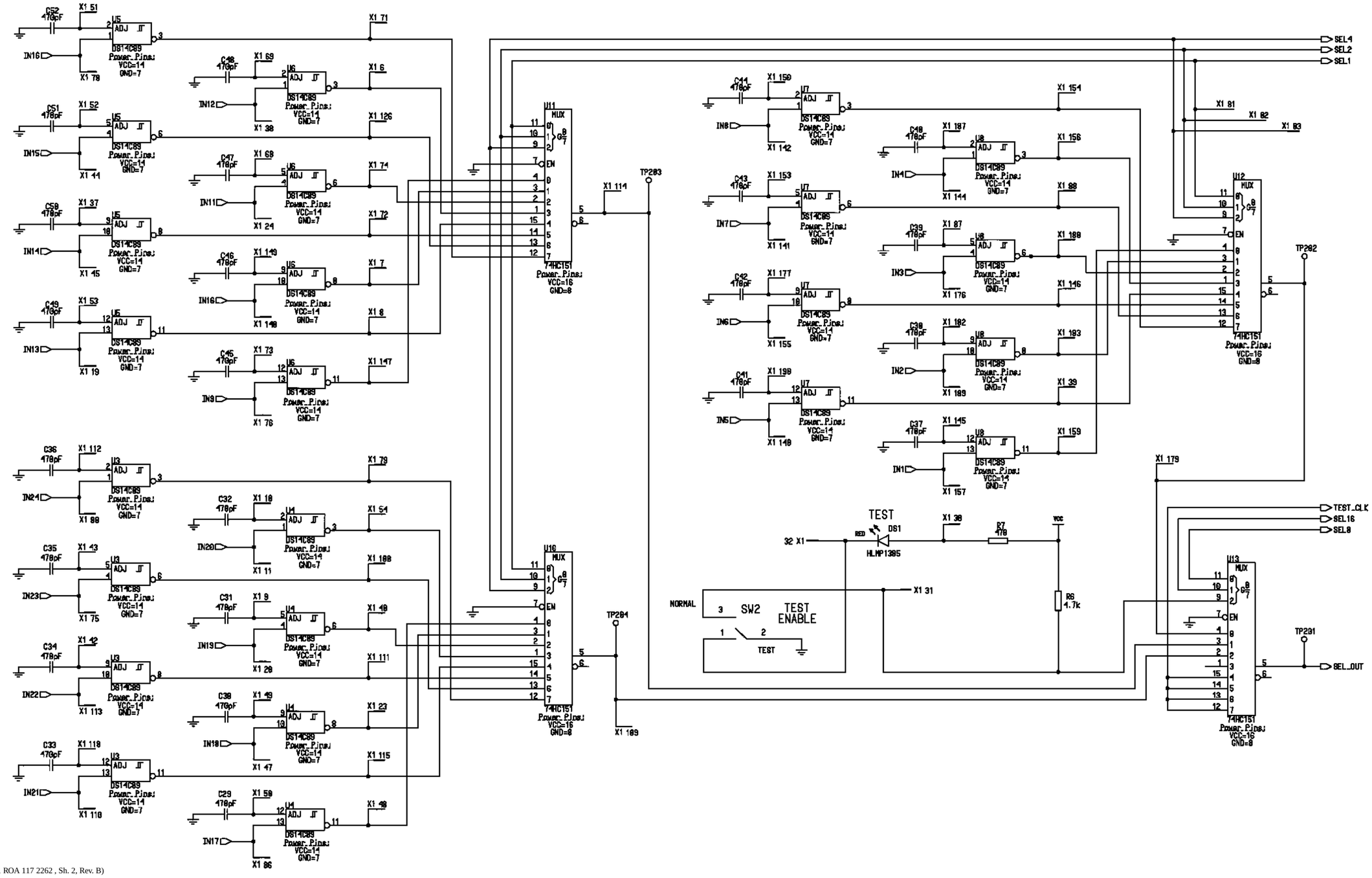




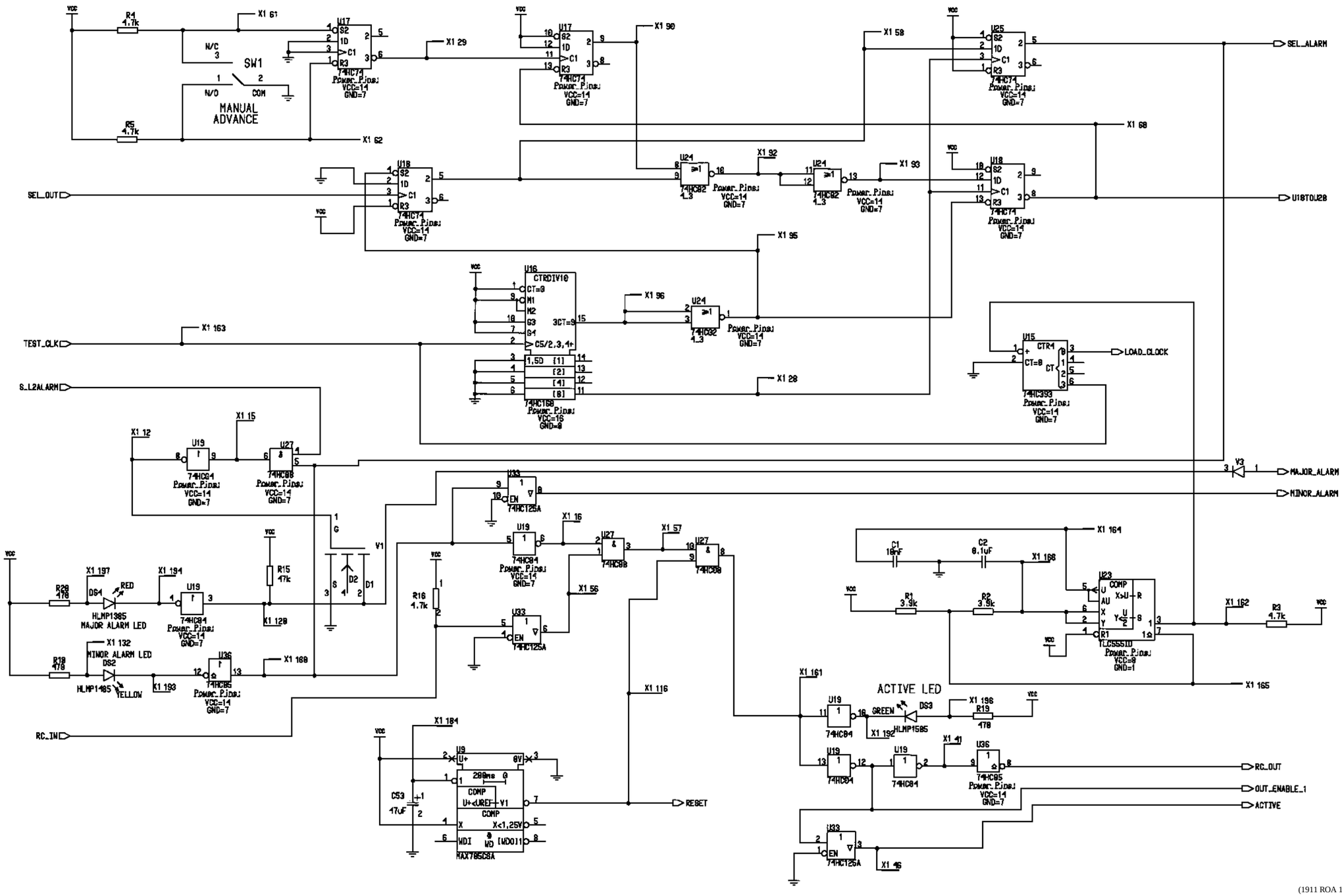
(1078A-ROA 117 2262, Rev.B)



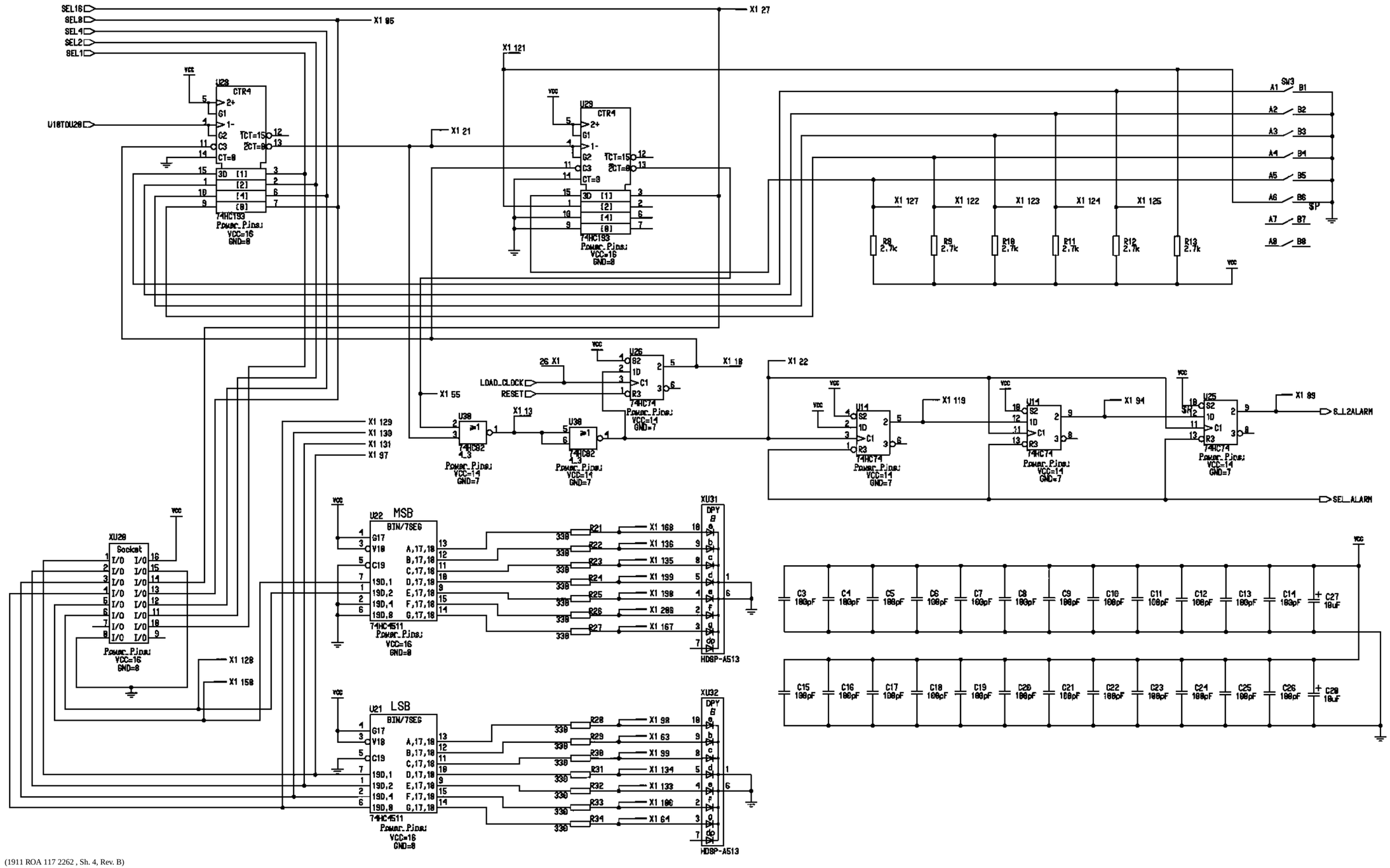
(1911 ROA 117 2262 , Sh. 1, Rev. B)



(1911 ROA 117 2262 , Sh. 2, Rev. B)



(1911 ROA 117 2262 , Sh. 3, Rev. B)



(1911 ROA 117 2262 , Sh. 4, Rev. B)

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