MAINTENANCE MANUAL

GPS SIMULCAST
BYPASS MODULE
ROA 117 2278

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ERICSSON

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SPECIFICATIONS

Tables 1 though 3 show the specifications of the Bypass Module used in the GPS Simulcast system as follows:

- Table 1 outlines the genreral specifications.
- Table 2 outlines the power drain and ground specifications
- Table 3 outlines the P1 connector interface to the Synchronizer Shelf.

GENERAL

Table 1 - General Specifications

ITEM	SPECIFICATION
Input Voltages	+5 Vdc ± 10%
Temperature	-30°C to +60°C
Dimensions	8.0 inches Long x 4.0 inches Wide
Digital/Data type	HCTTL
Analog/Audio Type	None

POWER AND GROUND

Table 2 - Power and Ground Specifications

VOLTAGE	CONNECTOR POINT	TOLERANCE ±%	CURRENT DRAIN TYPICAL mA
+ 5 Vdc	J1-A30, A31, B30, B31	10	75 mA (Non-Bypass) 30 mA (Bypass, with no split system)
Ground	J1-A1, B1, C1, A32, B32, C32	N/A	N/A

NOTICE!

Repairs to this equipment should be made only by an authorized service technician or facility designated by the supplier. Any repairs, alterations or substitution of recommended parts made by the user to this equipment not approved by the manufacturer could void the user's authority to operate the equipment in addition to the manufacturer's warranty.

NOTICE!

CONNECTOR J1 DEFINITION

Connector J1 is a 96-Pin connector (three rows, A, B, C of 32) which is used to interface to the synchronizer shelf back-plane. Any pin that is not listed below is a no connect.

Table 3 - Connector J1 Specification

CONNECTOR PIN	SIGNAL NAME	INPUT/ OUTPUT	ANALOG/ DIGITAL	LEVEL
J1-A1	Ground	O		0 Vdc
J1-A30	Power	I		5 Vdc
J1-A31	Power	I		5 Vdc
J1-A32	Ground	O		0 Vdc
J1-B1	Ground	O		0 Vdc
J1-B30	Power	I		5 Vdc
J1-B31	Power	I		5 Vdc
J1-B32	Ground	O		0 Vdc
J1-C-1	Ground	O		0 Vdc
J1-C11	Monitor_Split_ System	O	D	HCTTL
J1-C12	Alarm_B (Spare)			
J1-C13	Alarm_C (Spare)			
J1-C14	Alarm_D (Spare)			
J1-C16	Enable_Split_ System	O	D	HCTTL
J1-C17	Resync_ Alarm_ Buss	I	D	HCTTL
J1-C18	GPS Major Alarm	I	D	HCTTL
J1-C20	GPS_Distribution_ Major_ Alarm	I	D	HCTTL
J1-C22	System_Bypass_In	I	D	HCTTL
J1-C24	Normally_Open_1	O	D	HCTTL
J1-C25	Common_1 (Ground)	O		0 Vdc
J1-C26	Normally_Closed_1 (Bypass Out)	O	D	HCTTL
J1-C27	Normally_Open_2	I/O		Closure to Common 2
J1-C28	Common_2	I/O		Closure to Normally Open 2 or Normally Closed 2
J1-C29	Normally_Closed_2	I/O		Closure to Common 2
J1-C32	Ground	O		0 Vdc

DESCRIPTION

Bypass Module ROA 117 2278 is used in the GPS Simulcast Synchronizer shelf located in the equipment rack at the Transmit Site. This module is located in slot #19 of the Synchronizer shelf.

The Bypass module forces the transmit site into bypass and lights the appropriate front panel LED's for any of the following conditions:

- A Transmit Timing Module (TXTM) major alarm (logic high) is received from the TXTM module in the Synchronizer Shelf.
- A GPS distribution amplifier major alarm (open or high logic level) is present.
- A sync major alarm (logic high) is received from the Resync Modules
- A system bypass input (logic high) from the Integrated EDACS Alarm (IEA) system is present.
- The front panel Local Bypass switch is switched to "On".

The module is used to enable split system operation by a front panel switch. When enabled, a front panel LED is lit and a signal indicator (Monitor Split System) is fed to the IEA. Once the system goes into the Bypass mode, the Bypass module generates a logic low Split System enable output signal. This signal is used by the Bypass Mapping Module ROA 117 2277 to control GETC inhibit lines (i.e., select which stations will be operating while in the bypass mode).

The Bypass Mapping Module is located on the GPS Simulcast Transmit Rack Interface Panel. For information on Bypass Mapping Module ROA 117 2277 refer to Maintenance Manual LBI-39205.

Bypass Module ROA 117 2278 has spare board inputs (Alarm B, C, D), logic inputs (U3, Pins 4, 5, 12, 13), and outputs (K1 relay, side 2) for customization of bypass control.

CIRCUIT ANALYSIS

When no alarms or bypass inputs are present, the module is in the non-bypass mode, no red LED's are lit, the K1 relay is energized and Normally_Closed_1 (Bypass Out), (J1 C26) is logic high (Refer to Figure 1 and Schematic Diagram).

The four alarm/bypass inputs, listed below, are configured in a "wired AND" configuration. Each can initiate bypass operation by causing NAND gate U3, Pins 9&10 to go low. This results in a logic high input on driver U2, Pins 6 & 7. Driver U2 de-energizes the K1 relay, causing BYPASS INDICATOR DS2 (BYPS) to light and a closure to ground on J1 C26 Normally_Closed_1 (Bypass Out).

- A TXTM_major_Alarm (Transmit Site Timing Module) (J1 C18): In the non-bypass state, this line is logic low. When open or pulled high, TXTM ALARM INDICATOR DS5 (TXTM) lights. NAND gate U3, Pins 9&10 are pulled low by invertor U4, Pin 12.
- GPS_Distribution_Major_Alarm (J1 C20): In the non-bypass state, this line is logic low. When open or pulled high, GPS DISTRIBUTION MAJOR ALARM INDICATOR DS6 (10 MHz) lights. NAND gate U3, Pins 9&10 are pulled low by inverter U1, Pin 8.
- Resync_Alarm_Buss (J1 C17): The non-bypass state of this line is logic low. When pulled high by all RESYNC Modules (all in alarm), RESYNC ALARM indicator DS7 (SYNC) lights. A logic low reaches U3, Pins 9 & 10 through invertor U4, Pin 10.
- System_Bypass_In (J1 C22): The non-bypass state for this line is logic low. Pull down resistor R22 forces the logic low input even when the input is open (IEA is not present). When pulled high by the IEA, SYSTEM BYPASS INDICATOR DS4 (SYS) lights. A logic low reaches U3, Pins 9&10 through inverter U1, Pin 10.
- Local bypass S2 (LOCL BYPS): The non-bypass state requires switch S2 to be in the OFF position. When switched to ON, LOCAL BYPASS INDICATOR DS3 (LOCL BYPS) lights. NAND gate U3, Pins 9&10 are pulled low by U1, Pin 6.

Split system operation can be enabled by putting switch S1 (SPLIT SYS) in the ENBL position. This lights the yellow SPLIT SYSTEM ENABLED INDICATOR DS8. Though enabled, split system operation will not become active (i.e., J1 C16 Split System enable will not go low) until the module is in the bypass mode. When S1 SPLIT SYS is in the ENBL position, and bypass is active, U1, Pins 2&4 both are logic low.

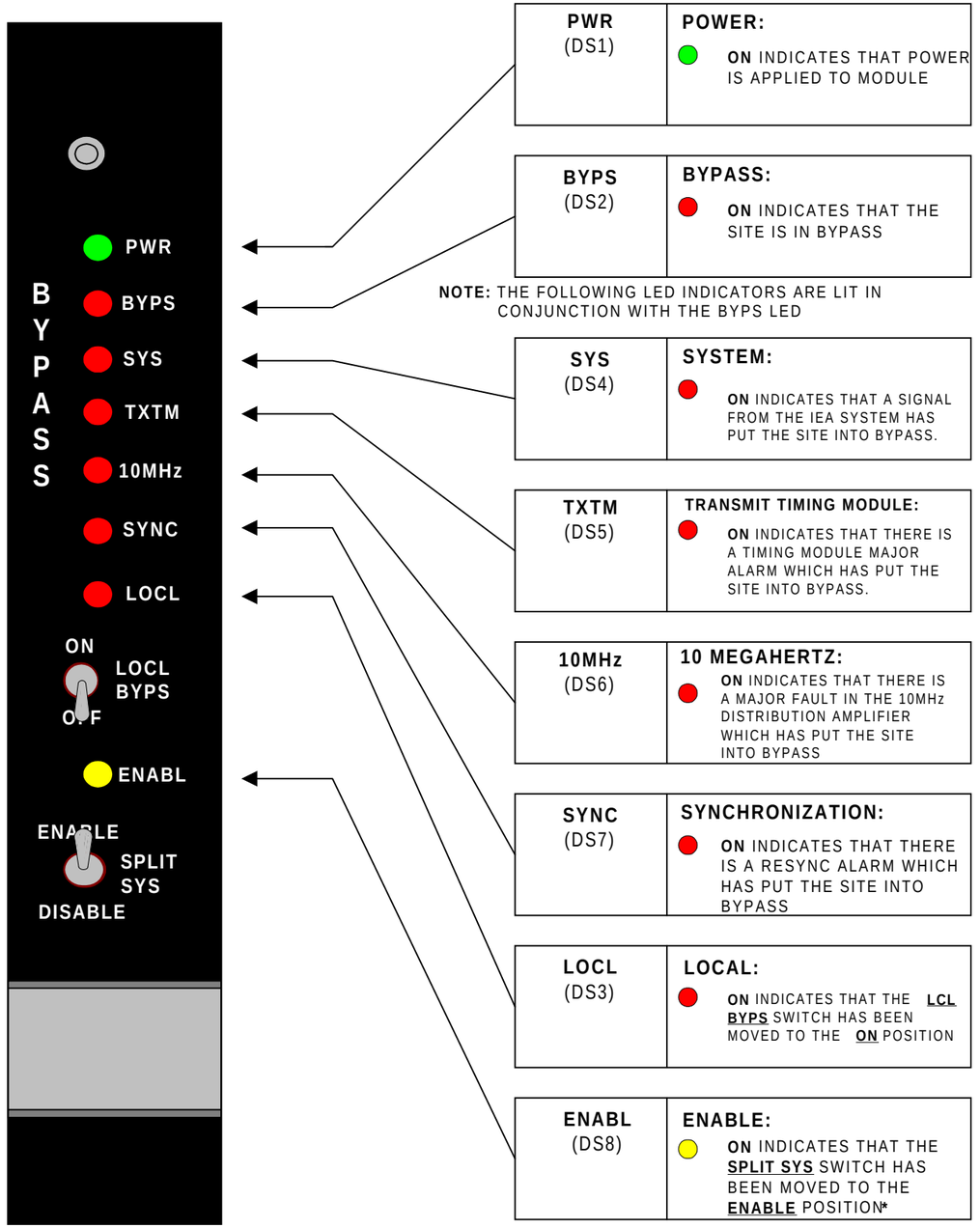


Figure 1 - Front Panel

TABLE 4 - Test Steps

	SIGNAL	Test 1	Test 2	Test 3	Test 4	Test 5	Test 6	Test 7	Test 8
I	SYSTEM BYPASS (J1 C22)	open*	**high**	open*	open*	open*	open*	open*	open*
N	GPS MAJOR ALARM (J1 C18)	low	low	**open***	low	low	low	low	low
P	GPS DIST. MAJOR ALARM (J1 C20)	low	low	low	**open***	low	low	low	low
U	RESYNC ALARM BUSS (J1 C17)	low	low	low	low	**open***	low	low	low
T	LOCL BYPASS (S2)	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	**ON**
S	SPLIT SYS (S1)	NOT	NOT	NOT	NOT	NOT	NOT	**ENBL**	**ENBL**
O	PWR LED DS1 (PWR)	**lit**	**lit**	**lit**	**lit**	**lit**	**lit**	**lit**	**lit**
U	BYPS LED DS2 (BYPS)	off	**lit**	**lit**	**lit**	**lit**	**lit**	off	**lit**
T	SYS LED DS4 (SYS)	off	**lit**	off	off	off	off	off	off
P	TIMING LED DS5 (TXTM)	off	off	**lit**	off	off	off	off	off
U	10 MHz LED DS6 (10 MHz)	off	off	off	**lit**	off	off	off	off
T	RESYNC LED DS7 (SYNC)	off	off	off	off	**lit**	off	off	off
S	LOCL BYPASS LED DS3 (LOCL)	off	off	off	off	off	**lit**	off	**lit**
	SPLIT SYS LED (ENABL)	off	off	off	off	off	off	**lit**	**lit**
	MONITOR SPLIT SYSTEM (J1 C11)	high** v ≃ 1.9v	high	high	high	high	high	**low** v≃ .006v	**low** v≃ .006v
	SPLIT SYSTEM ENABLE (J1 C16)	high v≃ 5v	high	high	high	high	high	high v≃ 5v	**low** v≃.05v
	BYPASS OUT (J1 C26)	high v≃ 5v	**low** v≃.05v	**low**	**low**	high	**low**	high	**low**
	NORMALLY OPEN 1 (J1 C24)	shorted to C25	not shorted to C25	not shorted to ground	not shorted to ground	shorted to ground	not shorted to ground	shorted to ground	not shorted to ground
	NORMALLY CLOSED 2 (J1 C29)	not shorted to J1 C28	shorted to J1 C28	shorted to J1 C28	shorted to J1 C28	not shorted to J1 C28	shorted to J1 C28	not shorted to J1 C28	shorted to J1 C28
	NORMALLY OPEN 2 (J1 C27)	shorted to J1 C28	not shorted to J1 C28	not shorted to J1 C28	not shorted to J1 C28	shorted to J1 C28	not shorted to J1 C28	shorted to J1 C28	not shorted to J1 C28

* open means leave the pin alone; do not connect any signal to it.

**Note: This will be pulled to logic high by the IEA input card.

TEST AND TROUBLESHOOTING

TEST EQUIPMENT

The following equipment is necessary for board test.

- +5 Vdc power supply: Power Design Inc TP325 or equivalent
- Ohmmeter
- Voltmeter

TEST PROCEDURES

Continuity Test

Using Table 2, verify that Power and Ground are not shorted on the assembly.

Stationery Tests

1. Ground as indicated in Table 2.
2. Apply + 5 Vdc power as indicated in Table 2.
3. For each of the test in Table 4, set inputs as shown and verify corresponding outputs. Bolded text indicates the primary focus of each test. Shaded areas of the output portion of the table are shown for completeness, and need not be performed.

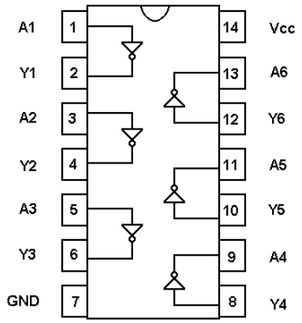
PARTS LIST

BYPASS MODULE ROA 117 2278

SYMBOL	PART NO.	DESCRIPTION
		- - -CAPACITORS- - -
C1 thru C3	RJC 464 3045/1	10 nF -10%, 50 VDCW.
C4	RJE 599 1258/1	10 µF ± 20%, 25 VDCW.
		- - - -DIODES- - - -
DS1	RKZ 433 637/3	LED: Green, 90° Angle.
DS2 thru DS7	RKZ 433 637/1	LED: Red, 90° Angle.
DS8	RKZ 433 637/2	LED: Yellow, 90° Angle.
		- - - -FUSE- - - -
F1	REQ 2103L 50A	Thermistor.
		- - -CONNECTOR- - -
J1	RVP 403 804/03	Pin Connector Unit, Rt angle, 96 position DIN.
		- - - -RELAY- - - -
K1	RAV 954 05/S	/2 Form C.
		- - - -RESISTORS- - - -
R1 thru R20	REP 625 424/47	Chip: 470 Ohms ± 5%, 1/8 Watt.
R22 thru R24	REP 625 426/1	Chip: 100 kOhms ± 5%, 1/8 Watt.
		- - - -SWITCH- - - -
S1 and S2	RMF 356 101/02	Toggle.
		- -INTEGRATED CIRCUIT- -
U1	RYT 306 6021/C	Inverter Circuits: Sim to 74HC05.
U2	RYT 109 6064/C	Dual Peripheral AND-Driver: Sim to SN75451B.
U3	RYT 306 2001/ C	Quad, 2-Inputs NAND Gates: Sim to 74HC00.
U4	RYT 306 6021/C	Inverter Circuits: Sim to 74HC05.
		-- -VARIABLE CAPACITOR- -
V1	RKZUA 323 01/1	Dual Variable Capacitance.
		- - - -DIODE- - - -
V2	RKZ 123 601	Schottky Barrier.
		- - - -HOLDER- - - -
XF1	NFN 102 04	Fuse.

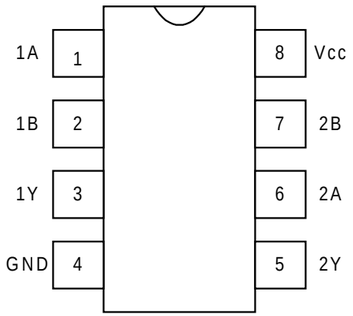
* COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES.

U1
INVERTER CIRCUITS
RYT 306 6021/C *(74HC05)*

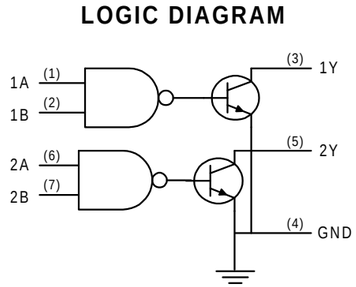


INPUT A	OUTPUT Y
H	L
L	H

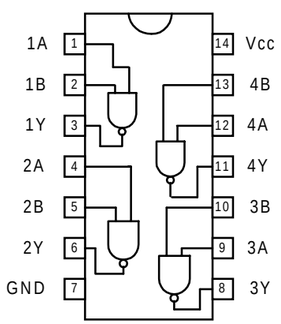
U2
DUAL PERIPHERAL AND-DRIVER
RYT 109 6064/C *(SN75451B)*



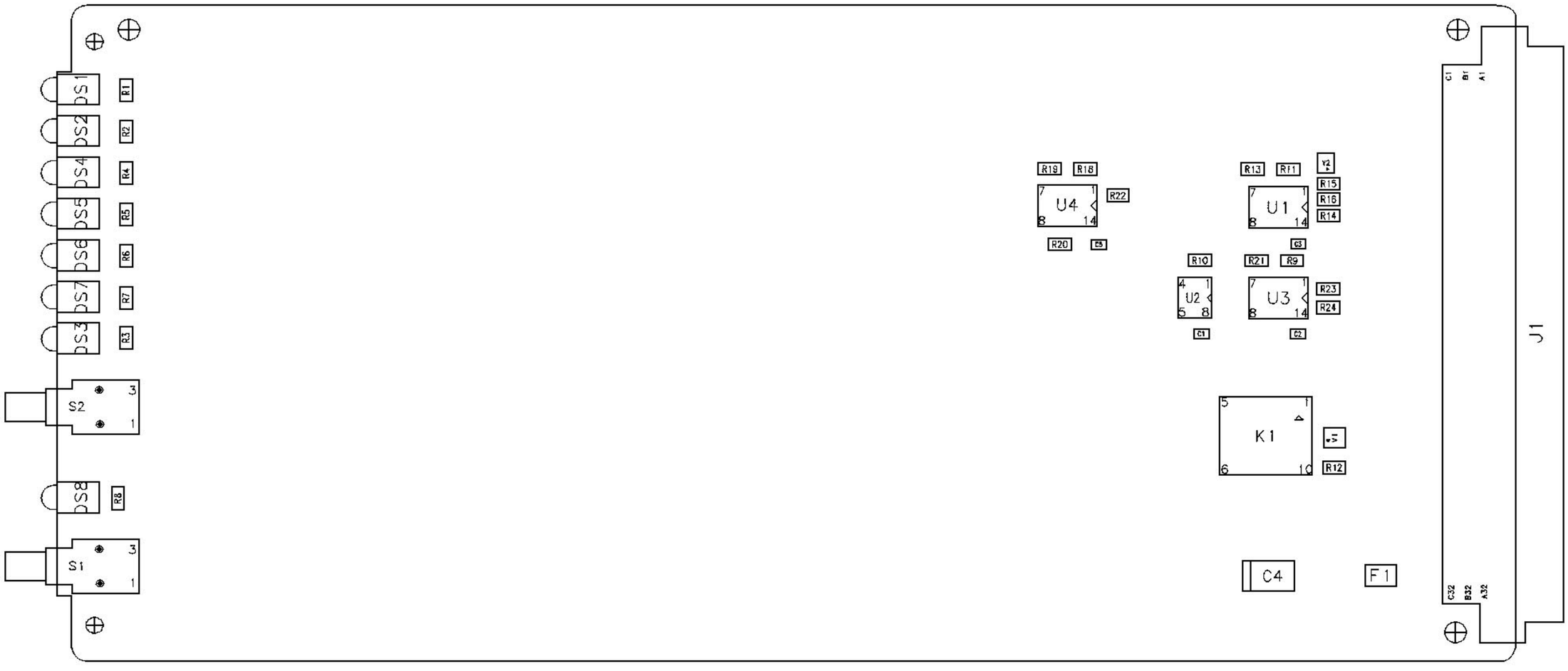
LOGIC DIAGRAM



U3
QUAD, 2-INPUT NAND GATES
RYT 306 2001/C *(74HC00)*



Positive Logic: $Y = \overline{A \bullet B}$



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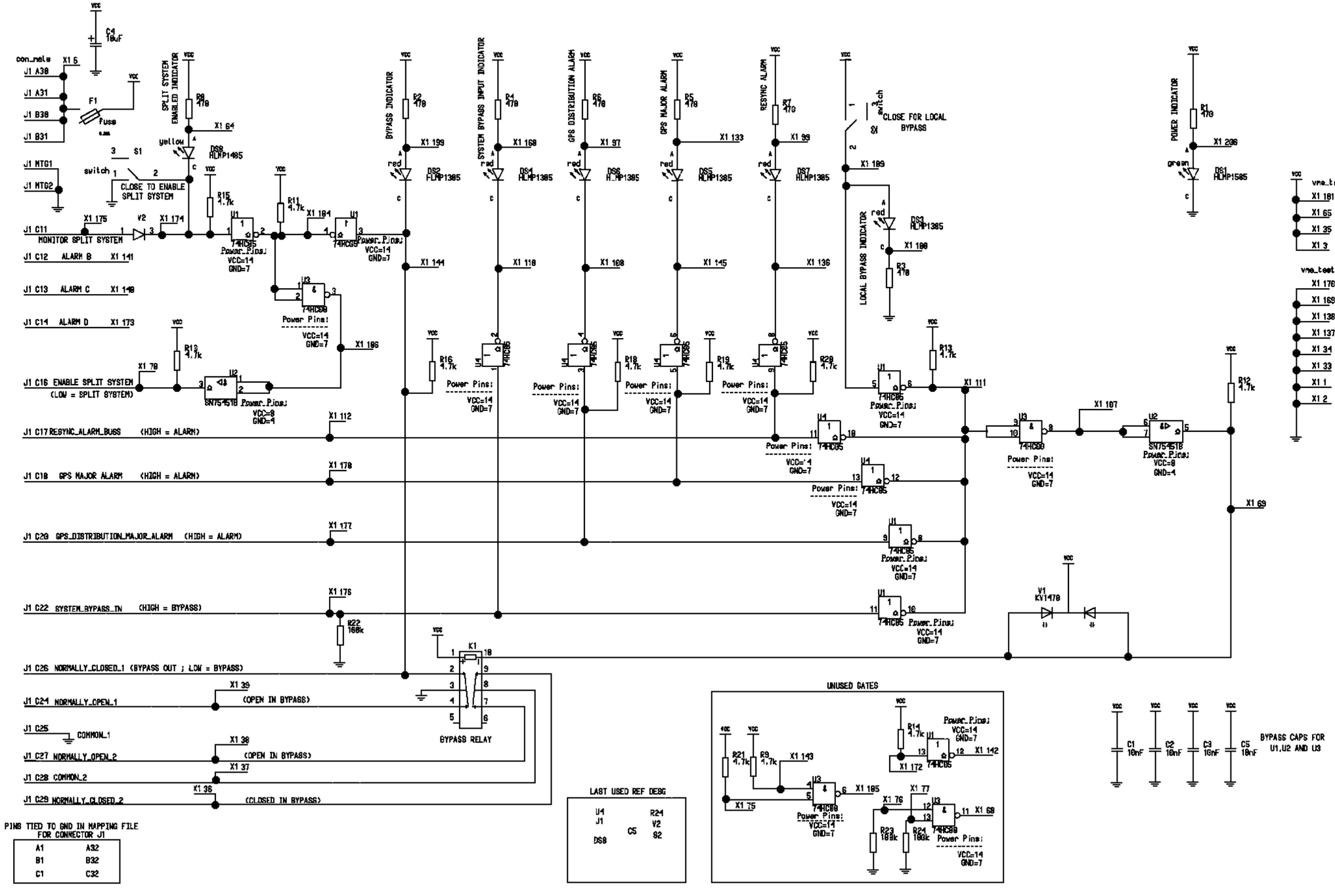

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