MAINTENANCE MANUAL

EDACS® SIMULCAST
CONTROL POINT TRUNKING CARD
ROA 117 2240/3

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FIGURES AND TABLES

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SPECIFICATIONS*

ITEM	SPECIFICATION
DIMENSIONS (H x L)	100 mm x 220 mm
POWER REQUIREMENTS	+5 Vdc ±5% 300 mA typical. +12 Vdc ±5% 30 mA typical. -12 Vdc ±5% 1 mA typical.
CONNECTIONS	96 Pin DIN connector (X1) mating to VME backplane interface. Six pin modular RJ-12 connector (X3).
COMM PORTS	2 synchronous 9600 baud 1 asynchronous - switched for the following purposes: • Backup Serial Link (BSL) • Flash • Site Controller 1 (SC1) • Site Controller 2 (SC2)

* These specifications are intended for use during servicing. Refer to appropriate Specification Sheet for the complete specification.

INTRODUCTION

This manual provides information on the operation, installation, and maintenance of the General Purpose Trunking Card (GPTC) when configured and used as the Simulcast Control Point Trunking Card (CPTC).

The GPTC refers to the basic ROA 117 2240 trunking card without the Front Panel or Configuration Plug.

The CPTC is refers to the ROA 117 2240/3, a trunking card configured for Control Point Trunking by adding a unique Simulcast Front Panel (SXA 120 4174/6) and Configuration Plug (ROA 117 2273). The CPTC is installed in the Simulcast Control Point Trunking Shelf (SXK 107 3847/2) along with its associated Vertical Turbo Card and Simulcast Interface Card. Electrical connections are made by plugging the CPTC into the proper card slot, which connects X1 into the shelf's backplane.

DESCRIPTION

The Simulcast CPTC is an integral part of the Simulcast Control Point and is co-located with the Voter and Control Point Simulcast and MUX equipment. The Control Point does not contain transmit-receive equipment, so all Transmit-Receive Sites are considered remote, even if one is co-located with the Simulcast Control Point. Data and Voice signals are brought to the Voter Digital and Analog Receivers via an inter-site communication system (usually microwave) and multiplex equipment at the Control Point and Transmit-Receive Sites.

Voted voice and data signals are cross connected to the Simulcast Analog and Digital equipment for distribution to the Transmit-Receive Sites. The voted voice is the Simulcast repeat audio source, the voted data is the voted digital voice source and path for trunking data messages to the CPTC.

The CPTC passes messages back to its Voter Selector which tell the Selector which mode it should be operating in. For example, Control Channel, Clear Voice Working Channel, and Digital Voice Working Channel.

The Console (switch) interface consists of transmit and receive audio/data pairs for each Trunked RF Channel and E & M keying signal from the switch for Switch Keying (PTT) to the Simulcast System.

SOFTWARE REQUIREMENTS

Over the life of the product, the software may undergo improvements or enhancements. As a result, you should always refer to the Trunking Card Software Release Notes to verify software and hardware compatibility.

NOTE

As a general rule, all trunking cards for a particular EDACS channel should run the same software version. This ensures software compatibility within the same EDACS channel. Since there is no software interaction between EDACS channels, different versions of software may exist on different channels, but it is not recommended.

The CPTC software is flashed into the Flash PROM U25 using the Flash Loading program stored in the trunking card's Flash Loader PROM U26 in conjunction with the PC Loader “leafoff”.

Properly installed trunking card Software is verified by observing the front panel LED display. The CPTC has four active front panel LED's. The **FS** LED, is used to indicate if the CPTC is communicating over the Backup Serial link (BSL). The **REM** LED indicates when a remote phone line is being routed to the transmitter. The **MODE** LED, indicates when the CPTC has enabled the low speed data (LSD) operation. The **D/A** LED indicates when the CPTC is transmitting High Speed Data (HSD). Refer to the *Front Panel Controlls and Indicators* section for additional information on the functions of the front panel indicators.

CONTROLS AND INDICATORS

The front panel LED's indicate the operational status of the CPTC in the Simulcasat system.

NOTE

The numbers shown in parentheses refer to the circuit diagram’s reference designator.

The CPTC front panel includes LED indicators, a reset switch, and the programming connector as shown in Figure 1.

FS

The **F**ail**S**oft Indicator (V14) is ON when communication is occuring on the BSL, such as in failsoft operation. When the indicator is OFF, the CPTC is communicating over the Site Controller serial link(s).

REM

The **Rem**ote Key indicator (V11) is ON when remote phone line audio is being routed to the transmitter

MODE

The Activity **Mode** indicator (V13) indicates when Low Speed Data is enabled. The indicator is ON whenever the CPTC is functioning as the Control Channel or as a Working Channel.

D/A

The **D**ata/**A**udio indicator (V16) is ON when the CPTC is transmitting High Speed Data in the Control Channel mode or sending Digital Voice or Data in the Working Channel mode.

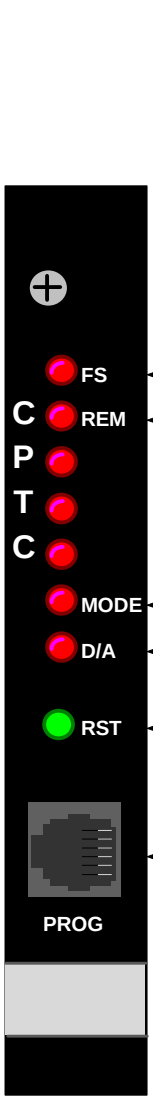
The indicator is OFF when the CPTC is repeating Clear Voice in the Working Channel mode.

RST

The Reset Switch (R4) is used to manually generate the reset pulse and initialize the CPTC software.

PROG

The programming connector (X3) is a six contact modular RJ-12 connector used to flash the CPTC software from a PC into the CPTC. When PC software "leafoff" runs, it asserts DTR which causes V35 to turn on +12 volts to the flash PROM. When 12 volts appears, a reset pulse is generated by comparator U2 which resets the CPTC and initializes the Flash Loader program. Refer to the *Programming* and *Circuit Analysis* sections for complete details.



FS (V14)	**F**ail**S**oft Operation. ✹ **ON** indicates the CPTC is communicating on the BSL. ❍ **OFF** indicates the CPTC is communicating on the Site Controller serial link(s).
REM (V11)	**Rem**ote Key. ✹ **ON** indicates call is in progress and Voted audio is being routed to the transmitter.
MODE (V13)	Activity **Mode**. ✹ **ON** in Control Channel Mode (D/A must also be ON). ✹ **ON** in Working Channel Mode when channel is assigned. (D/A is also ON when routing Digital Voice or Data.) ❍ **OFF** in Working Channel Mode when channel is not assigned.
D/A (V16)	High Speed **D**ata or **A**udio Path. ✹ **ON** when the CPTC is transmitting High Speed Data. ❍ **OFF** when repeating Clear Voice in the Working Channel Mode.
RST (S4)	Manual Reset button.
PROG (X3)	Connector used for flashing software into the CPTC.

Figure 1 - Simulcast Control Point Trunking Card Front Panel

CONFIGURATION

INSTALLATION

Installation or removal of the CPTC involves sliding the card into or out of the Simulcast Control Point Trunking Shelf. The actual slot position is determined by the system's number of channels and sites. However, one CPTC will always be in slot two (2) with the Turbo Card in slot one (1) and the Simulcast Interface Card in slot three (3).

The card may be inserted or removed from the shelf with power applied, however, always observe basic safety precautions to prevent injury or equipment damage.

DIP SWITCH SETTINGS

The following procedures provide instructions for setting the CPTC DIP switches under various operating environments with the software indicated. DIP Switch tables may also be found in the Software Release Notes for the particular software release. Table 1 shows the DIP switches. Table 2 shows the switch settings for channels 1 through 24.

Through improvements in software and hardware, fewer changes in DIP switch settings are required. As a result more switch positions are being ignored and their functionality is being programmed into the CPTC via the Personality Programming. The following is a summary of those changes:

Use the following procedure to set the DIP switches for Simulcast Control Point Working and Control Channel CPTC's:

1. **Set S1-1 thru S1-7 and S2-1 thru S2-4:**
   - Don't Care - Programmed in personality.
2. **Set S1-8:**
   - G5 (or later) software - Don't Care
   - G4 (or earlier) software - Set to OPEN.
3. **Set S2-5 to enable or disable Conventional Failsoft:**
   - G5 (or later) software - Don't Care, program in personality.
   - G4 software - CLOSED, program in personality.
   - G2 (or earlier) software - CLOSED to enable.
4. **Set S2-6 thru S2-8:**
   - Set to CLOSED.
5. **Set S3-1 thru S3-5 to Channel Address:**
   - Set DIP switches S3-1 thru S3-5 to the appropriate Channel Address according to the chart given in Table 2.
6. **Set S3-6:**
   - Set to CLOSED.
7. **Set S3-7 for Simulcast:**
   - G4 (or later) software - CLOSED, program in personality.
   - G2 (or earlier) software - OPEN for Simulcast Control Point Working and Control Channels.
8. **Set S3-6 for Site Controller connection:**
   - CLOSED when connected to Site Controller.
   - OPEN if **never** connected to Site Controller.

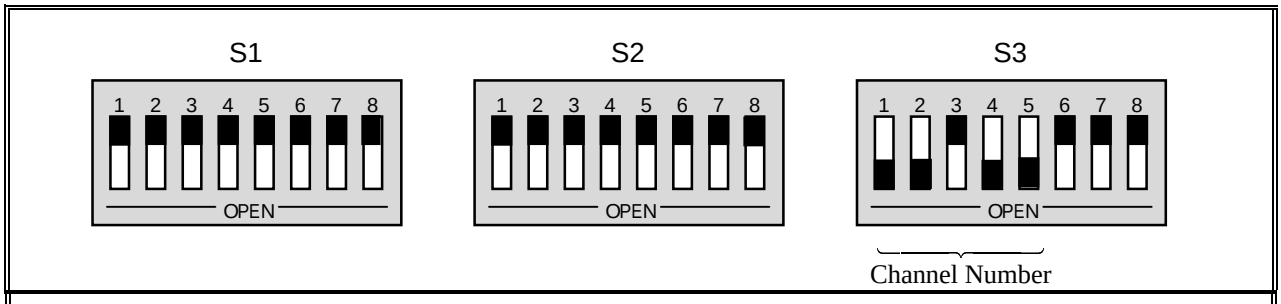
CONFIGURATION PLUG INSTALLATION

The configuration plug is used to physically alter data paths or circuit operation in the CPTC. For correct operation install the following configuration plug:

- Simulcast C.P. ROA 117 2273

The words "Simulcast C.P." are silk-screened on the top of the plug (See Configuration Plug Assembly Diagram).

Table 1 - DIP Switch Settings



O = Open, C = Closed, X = Don't Care (Recommend Closed)

When installing the plug, ensure the configuration plug is oriented correctly for with the key plug aligned with the cut pin on connector X2 (X2-50).

FLASH LOADER PROM INSTALLATION

Ensure the correct version of the Flash Loader PROM is installed in socket XU26. A label on the top of the Prom indicates that the Prom is programmed with Flash Loading software "FLASH BURN" and the software version (for example, RON 107 756/1 version R1, EDACS **01**).

NOTE

Refer to the Software Release Notes to verify software requirements and hardware compatibility.

Table 2 - Channel Number Switch Settings

	S3-1 thru S3-5 Channel Selection (LSB)				(MSB)
Ch. No.	**1**	**2**	**3**	**4**	**5**
1	O	C	C	C	C
2	C	O	C	C	C
3	O	O	C	C	C
4	C	C	O	C	C
5	O	C	O	C	C
6	C	O	O	C	C
7	O	O	O	C	C
8	C	C	C	O	C
9	O	C	C	O	C
10	C	O	C	O	C
11	O	O	C	O	C
12	C	C	O	O	C
13	O	C	O	O	C
14	C	O	O	O	C
15	O	O	O	O	C
16	C	C	C	C	O
17	O	C	C	C	O
18	C	O	C	C	O
19	O	O	C	C	O
20	C	C	O	C	O
21	O	C	O	C	O
22	C	O	O	C	O
23	O	O	O	C	O
24	C	C	C	O	O

O = Open switch position (1)

C = Closed switch position (0)

CPTC SOFTWARE INSTALLATION

This procedure provides instructions for downloading the CPTC software. The CPTC uses the Software contained in the AE/LZT 213 767/2 media kit. This kit contains the same code as the horizontal GETC except on a floppy disk. Also included in the kit is the flash and Turbo code as well as the loaders for both pieces of application code.. The installation process involves using an IBM compatible personal computer (PC), and interconnecting programming cable (19B804346P111) to download software into CPTC.

Equipment Required

- IBM PC/XT/AT or compatible with at least 640K memory, monitor and keyboard running MS-DOS version 3.0 or higher.
- Hard disk is recommended; but, not required.
- Serial Port configured as COM1.
- Programming Cable 19B804346P111.
- Software Media Kit AE/LZY 213 767/2.

CPTC Programming

The loadable CPTC software must reside on the PC as an Intel Hex file. The file "leafoff.exe" is the executable program which loads the CPTC hex file into the trunking card. Both files should be located in the same directory.

PC Setup

During first time use it may be necessary to setup the PC. Prepare the PC for programming the CPTC board by performing the following steps:

1. Using standard DOS commands or a software file manager, create a directory named "**CPTC**" on the PC's hard drive (directory name is user selectable). This step is only required for first time use. When upgrading, all existing files should be archived before copying the new files into the directory.
2. Make " **CPTC** " the current directory and copy the following files from the software distribution diskette into the "**CPTC**" directory:
    - leafoff.exe
    - *hexfile*.hex

Programming the CPTC

1. Connect the 19B804346P111 programming cable from the PC's Comm Port 1 to the RJ-12 phone jack "**PROG**" on the front of the CPTC.
2. Apply power to the Trunking Shelf.

NOTE

Power must be applied to the Trunking Shelf when programming the CPTC.

2. From the "**CPTC**" directory, run the **leafoff.exe** program by entering the command:

   "**leafoff *hexfile*.hex-1**".

   Replace "*hexfile"* with the CPTC software file name.

3. The program will reset the CPTC and run the Flash Loader program. The program erases the existing CPTC software residing in the Flash PROM U25 and writes the new CPTC software into the Flash PROM.

   When the program is finished, the PC will display the message "Radio Programmed. Closing down port COM1." Wait a couple of seconds to allow time for the PC to reset the CPTC and initialize the application program loaded, then disconnect the programming cable from the "**PROG**" connector.

4. Repeat Steps 2 and 3 to program additional trunking cards.

NOTE

To save time, it is possible to set up a batch file to run the Flash loading program. The following is an example batch file.

Name the batch, for example, TC.BAT. Names in italicsrefer to variables that you can name yourself. *"cptc"* is the name of the directory where the *hexfile* and *leafoff* reside. The file named *"hexfile"* is the file to be loaded and "*leafoff*" is the executable program. Enter the following batch program:

```
cd\cptc
leafoff hexfile.hex-1
```

The batch file performs the operations outlined in Step 2. To run the program, type "TC" <enter> to program the CPTC.

   If any difficulty is encountered when loading the program, refer to the *Troubleshooting* section.

5. Refer to the System Installation Manual LBI-39210 and check out the trunking card(s) operation. If any problems are encountered, refer to the troubleshooting procedures in the Installation Manual.

   If a problem is traced to an individual CPTC, refer to the troubleshooting procedures in this manual.

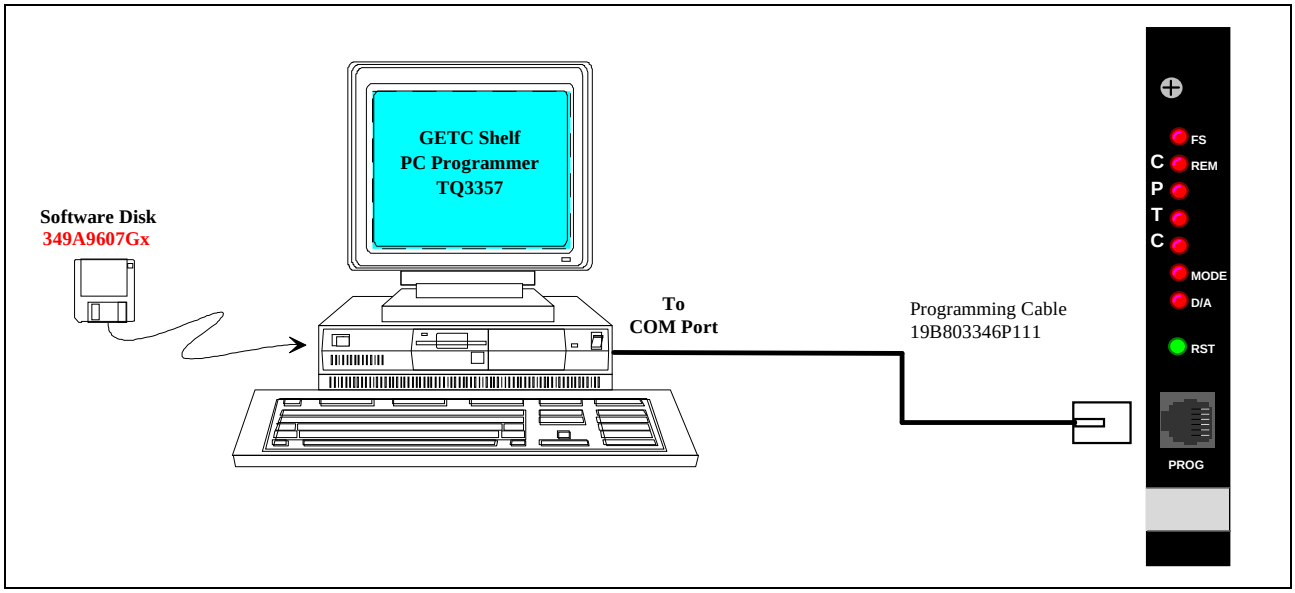


Figure 2 - Control Point Trunking Card Programming

OPERATION

The various operating states for the Control Point Trunking Card are listed in Figures 3 and 4. The pattern of illuminated indicators identifies the operating state. Operating states in Table 3 are for normal trunking operating.

The operating states for the CPTC when in the Failsoft operating mode are listed in Table 4.

Table 3 - CPTC Normal Trunking States

LED Indicators		Working Channel Idle	Working Channel Assigned Clear Voice	Working Channel Assigned Digital Voice/Data	Control Channel
FS	(V14)	❍	❍	❍	❍
REM	(V11)	❍	✹	✹	❍
	(V10)	❍	❍	❍	❍
	(V15)	❍	❍	❍	❍
	(V12)	❍	❍	❍	❍
MODE	(V13)	❍	✹	✹	✹
D/A	(V16)	✹	❍	✹	✹

Legend: ❍ = OFF ✹ = ON ✻ = FLASHING

Table 4 - CPTC Operating in Failsoft

LED Indicators		Working Channel Idle	Working Channel Assigned Clear Voice	Working Channel Assigned Digital Voice/Data	Control Channel
FS	(V14)	✹	✹	✹	✹
REM	(V11)	❍	✹	✹	❍
	(V10)	❍	❍	❍	❍
	(V15)	❍	❍	❍	❍
	(V12)	❍	❍	❍	❍
MODE	(V13)	❍	✹	✹	✹
D/A	(V16)	✹	❍	✹	✹

Legend: ❍ = OFF ✹ = ON ✻ = FLASHING

NOTE: If REM indicator fails to come on immediately after MODE, the Voice Signal failed to connect to the CPTC.

CIRCUIT ANALYSIS

This section describes the functionality of the various circuits on the CPTC.

NOTE

Navigation references shown as "≺sh. 1≻" refer to a specific sheet (1 thru 5) of Schematic Diagram 1911-ROA 117 2240 located at the end of this manual.

There are six main circuit groupings. These are the:

- Reset circuit
- Clock circuit
- Microprocessor Logic circuit
- Input and Output circuits
- Serial Ports
- Flash Loading circuits

INPUT POWER

Power for the GPTC is provided by external power supplies supplying +5 Vdc +12 Vdc and -12 Vdc. The +5 Vdc enters at X1 pins A30, A31, B30, and B31 ≺sh. 1≻ and is routed through fuse F1 to the Vcc plane on the 4-layer PCB. The +12 Vdc enters at X1 pin C31 and is routed through fuse F2 to the +12V line, and the -12 Vdc enters at X1 pin C30 and is routed through fuse F3 to the -12V line. Capacitors C1 and C2, C3, and C4 provide additional filtering for the +5 Vdc +12 Vdc and -12 Vdc lines, respectively. Ground connection is made on X1 pins A1, C1, A32, B32, and C32 and connect to a ground plane.

RESET CIRCUITRY

The GPTC contains a Power-on/Manual reset for initializing the programmed code and hardware devices on the board. The heart of the circuit is the microprocessor supervisory circuits contained in U14. These circuits reset the CPU and modems whenever one of the following events occur:

- Power is restored to the board.
- An external momentary active low is applied to X1 pin C23. A one-shot generates a reset pulse when X1-C23 goes low.
- An active low continuous reset is applied to X1 pin C22. Processor is held reset as long as X1-C22 is low.
- The **RESET** switch S4 is pushed and released.
- The Watchdog Timer in U31 times out.
- Flashing is initiated or terminated via the programming cable connected to the **PROG** connector X3.

When power is initially applied to the GPTC or if input power dips below the reset threshold, the microprocessor supervisor IC, U14 ≺sh. 4≻ will initiate a reset pulse. The reset output pulse, RESET, (U14 pin 7) goes low and remains low until the Vcc rises above the reset threshold and the internal timer releases RESET after a preset delay (≈200 ms). The active low reset pulse is applied to NAND gate U33A pin 1 resulting in an active high output at U33A pin 3. This is applied to modem U31 pin 25 (RESIN) . The modem RESOUT (U31 pin 3) is the logical-OR of the RESIN and the internal watchdog-timer pulse (if not serviced by the microcomputer U1). The high output reset pulse (RES) then resets the microcomputer at U1 pin 10 ≺sh. 3≻ and the Phone Modem at U32 pin 25. It is also applied to inverter U10-4 pin 9 ≺sh. 2≻. The low output signal (pin 8) is then applied to pin 1 on the Output Latches U5, U6, and U7, resetting them.

Reset is also accomplished by pulling NAND Gate U34D pin 13 low. This may be done either externally, by pulling the RESET IN CONT line (X1-C22) low or by pressing the RESET button S4, which grounds pin 13. The resultant output from U34D pin 11 is a high pulse which is inverted by U9-4 and applied to the manual reset (pin 1) input of U14. U14 then generates the reset pulse as described previously.

When the external reset is generated by a pulsed signal, to ensure a permanent reset will not inhibit the GPTC, the RESET IN PULSE line (X1-C23) is used. This momentary active low pulse is applied to the Retriggerable Monostable Multivibrator U8-0 on pin 5 ≺sh. 4≻. The multivibrator generates a negative going pulse with a pulse width of ≈ 50 ms. This pulse is applied to NAND Gate U34D at pin 12. The reset circuit then functions the same as pressing the manual reset.

A reset may occur automatically if the microcomputer fails to service the watchdog timer in modem U32 ≺sh. 4≻. This reset will occur if the microcomputer misses a service for a two-second period .

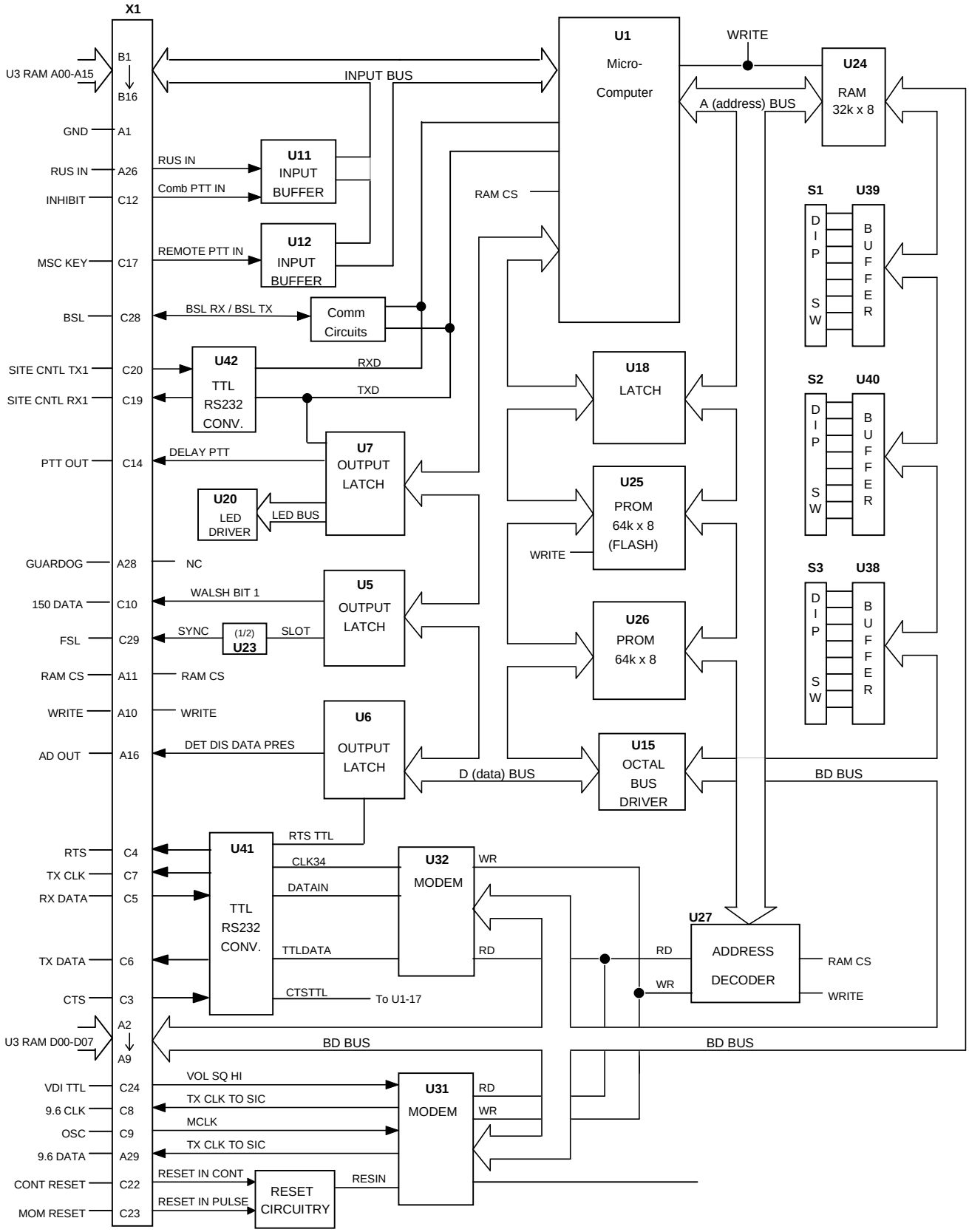


Figure 3 - GPTC Block Diagram

It is also necessary to generate a reset pulse any time the unit initiates the Flash programming or returns to normal operation. When the Flash programming is initiated by the PC though the programming cable plugged into the **PROG** connector X3, the flash circuit consisting of V36, V37, and V35 ⩤sh. 5⩥ causes the FLASH VPP line to go to +12 volts. This transistioning signal is applied the input of a comparator U14 pin 4 ⩤sh. 4⩥. The output of the comparator U14 pin 5 (FLASHING) goes to +5 volts during the flash loading process and returns to zero (0) volts when flashing is complete.

The time constant of R6 and C8 causes a slower rising or falling transition to occur at comparator U2 pins 5 and 6. U2-1 pin 7 is biased at approximately 3.3 volts and U2-2 pin 4 is biased at approximately 1.66 volts.

When the rising or falling FLASHING signal is below 3.3 volts, the output of Comparator U2-1 is high (open collector). When the rising or falling FLASHING signal is above 1.66 volts, the output of Comparator U2-2 is high (open collector). While the signal transitions from 1.66 volts to 3.33 volts or from 3.33 volts to 1.66 volts, the outputs of both comparators are high. Outside 1.66 to 3.33 volt range, one of the comparator outputs will be low keeping V6 cut off and U33A pin 2 high, holding off the reset.

While both comparator outputs are high, V6 turns on and applies a low to NAND Gate U33 pin 2 which outputs an active low signal to the modem U31 pin 25 (RESIN). The modem then resets the microcomputer, Phone Modem, and output latches as previously described.

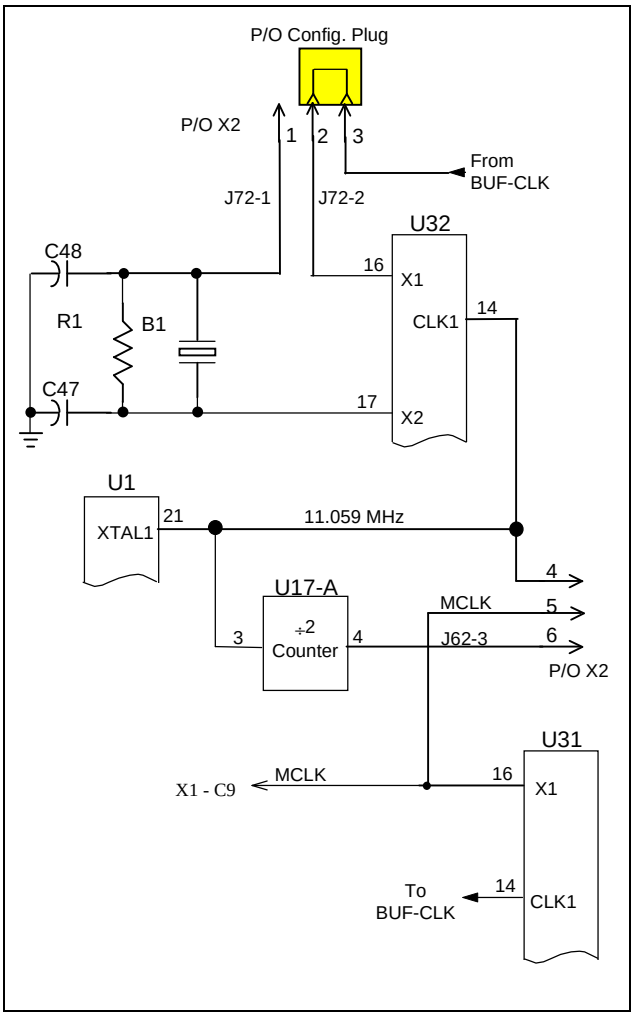


Figure 4 - Clock Circuit

CLOCK CIRCUITRY

Internal Clock (Not used with Simulcast)

The clock drive for the GPTC originates in modem U32 ⩤sh. 3⩥. The clock oscillator consists of crystal B1, the oscillator amplifier in modem U32, and associated circuitry (see simplified diagram in Figure 4).

The crystal oscillator B1 and associated circuitry is connected to the modem oscillator amplifier U32 pin 16 by installing the Configuration Plug on connector X2 connecting pins 1 and 2 together. The oscillator amplifier circuit runs at 11.059 MHz as determined by crystal B1. The oscillator amplifier output at U32 pin 14 (CLK 1) provides buffered clock signals (11.059 MHz) directly to the microcomputer (U1) and to the RF Data Modem U31 pin 16 (MCLK) via the Configuration Plug and X2 pins 4 and 5.

External Clock

In the Control Point Trunking Card configuration the GPTC uses an external reference oscillator signal which originates at the GPS Receiver. This 9600 Hz reference signal is routed to the Simulcast Interface Card, which generates the 11.0592 MHz clock signal (OSC).

The 11.0592 MHz clock is input to the GPTC at X1-C9 and routed to U31 pin 16 (MCLK). U31 amplifies and buffers the signal. The amplified clock output (U31 pin 14) is routed to U32 pin 16 via the BUF-CLK line and configuration plug connection J72-2. U32 also amplifies and buffers the signal. The output from U31 (U31 pin 14) is then applied directly to the microprocessor U1.

MICROPROCESSOR LOGIC CIRCUIT

The GPTC Logic circuitry ⩤sh. 3⩥ consists of the microcomputer U1, the Flash Prom U25, Flash Controller Prom U26, RAM U24, Address Decoder U27, Bus

Transceiver U15, ALE Latch U18, associated latches, DIP switches S1 thru S3 and Bus Drivers U38 thru U40. The microcomputer obtains its instructions from the code loaded into the Flash Prom U25. The upper eight address lines (bits 8 thru 15) of the microcomputer exit port 2, U1 pins 24 (bit 8) to 31 (bit 15) and connect to the Flash PROM U25. The lower address lines (bits 0 thru 7) exit port 0, U1 pins 36 (bit 7) to 43 (bit 0) and are latched into register U18 when ALE (Address Latch Enable) goes high. The output of U18 supplies the lower eight address lines to the Flash PROM. Thus the lower eight address bits are on the address bus during the entire microprocessor cycle. The microcomputer uses the PSEN (Program Store Enable) U1 pin 32 control line to access the data from the Flash PROM U25 pin 24. Address Decoder U27 generates chip enable (CE) signals when RAM U24 or either of the two modems, or any of the three DIP switches, or any of the three output latches are accessed by the software. The address lines to the RAM are identical to those going to the PROM U25.

Microcomputer U1 interfaces via the BD Bus to the Phone Modem (U32). The Phone Modem TTL input and output data is converted to or from RS-232 data via the TTL/RS-232 Converter U41 ⋖sh. 5⋗. This provides a 9600 baud synchronous remote data interface.

The configuration of the GPTC is partly determined by the settings of switches S1 thru S3. The microcomputer reads the switch settings via octal buffers U38 (S3), U39 (S1), and U40 (S2). Resistor pull-ups are provided for each of the switch lines.

The microcomputer accesses data to or from RAM U24, modem U31, modem U32, and octal buffers U38, U39, and U40 via octal bus transceiver U15. The transceiver, when directed by the microcomputer read command (RD at U1 pin 19) transfers the data from the switches and BD (buffered data) Bus to the D (Data) Bus. Data going to or from the PROMs U25 and U26, and Output Latches U5, U6, and U7 is handled by the D (data) bus.

Program memory is selected by the PSEN strobe (U1 pin 32). The ALE addresses the devices on the A (address) Bus by latching the lower eight bits of the address in U18. The upper eight bits of the address are sent directly to the devices. The two-to-four Address Decoder U27 is used to decode the upper address lines (A11 thru A13). When gated by RD (U1 pin 19) or WR (U1 pin 18), the decoder enables the desired device to transmit or receive data. The devices on the microcomputer bus are addressed according to Table 5.

Table 5 - Device Addresses

DEVICE	HEXADECIMAL ADDRESS
U24 - RAM	0000 - 1FFF
U31 - RF Modem	A170 - A172
U38 - S3 Latch	B800
U39 - S1 Latch	B000
U40 - S2 Latch	A800
U32 - Phone Modem	A0F0 - A0F2
U7 - Output Latch	A800
U6 - Output Latch	B000
U5 - Output Latch	B800

INPUT AND OUTPUT CIRCUITS

Input signals are sent to the microcomputer U1 via the Input Bus. The microcomputer evaluates the input data and depending on programming, outputs the necessary control signals to other elements of the system and turns on or off the front panel LEDs.

Input signals to the GPTC are buffered by U11 and U12 ⋖sh. 2⋗ which interface to the Input Bus. The microcomputer can read the data on the input bus, port 1, at any time.

The microcomputer provides output signals by writing specific logic values into output latches U5, U6, and U7.

The outputs of U7 turn on and off the various LEDs V10 thru V16. These LEDs provide visual front panel indications of the module's operation.

The U6 latch sends out the Data Present (DET DIS DATA PRESENT) signal to X1-A16. This signal identified as AD OUT is routed to the Interface Card.

Output latch U5 outputs the WALSH BIT 1 signal. 150 Hz Data signal is routed through X1-C29 ⋖sh. 1⋗ to the backplane for conversion to an RS-232 signal by the Interface Card.

SERIAL PORTS

The GPTC contains both synchronous and asynchronous serial communication ports.

Asynchronous

All of the asynchronous signals go in and out of the microcomputer via the RXD (U1 pin 11) and TXD (U1 pin 12) lines. The logic circuits consisting of U9, U13, U33, U35, U36, and U37 ⩤sh. 5⩥ route these communication signals to the Backup Serial Link (BSL RX and BSL TX), to the PC during flash programming (FLASH RX and FLASH TX), to the RS232/TTL converter U42 via the SITE CNTL RX1 (X1-C19) and SITE CNTL TX1 (X1-C20) lines, and to SITE CNTRL 2 under the control of various logic signals 11_73_1SEL, 11_73_2SEL, FLASHING, LED_BUS_2, LED_BUS_5, and J16_2.

The data routed the RXD and TXD lines only flows in one direction at time at the rate of 19.2K Baud.

Synchronous

The 9600 baud synchronous data is received by the GPTC at X1-C5 (RX DATA) ⩤sh. 1⩥. When RS-232 communication is used, data comes directly to X1-C5 and is converted from RS-232 to TTL by the RS232/TTL converter U41 pin 4 ⩤sh. 5⩥. The output of the converter at pin 20 (DATAIN) is sent to the Phone Modem U32 pin 19 ⩤sh. 3⩥. When ready, the microcomputer directs the modem (via the ALE and RE signals) to convert the serial data to parallel data and download the data onto the BD Bus (pins 4 thru 11).

NOTE

When the Control Point communicates with the Voter via RS-232 link an RS-232 Interface Module is used in place of the RMIC in slot 2.

RS-232 connections are used even when the Voter and site are not collocated if the link is over T1 Mux.

Data to be transmitted by the GPTC is latched from the BD Bus into the Phone Modem U32. The modem converts the data from parallel to serial format and outputs the data from U32 pin 21 (TXDAT) on the TTL DATA line to the RS232/TTL converter U41 pin 10 ⩤sh. 5⩥. U41 converts the data from TTL to RS-232 and routes the dat from U41 pin 7 to X1-C6 (TX DATA).

FLASH LOADING CIRCUITS

Flashing is controlled by the DTR line X3-5 from the PC. When the DTR is low (-12 V) at X3-5, power FET V35 is turned on connecting +12 volts to FLASH_VPP. Applying FLASH_VPP to the Reset Circuit U14 and U2 ⩤sh. 4⩥, generates a reset and starts the flashing process.

When going in or out of Flash mode, it is necessary to generate a reset pulse so the processor will begin executing the Flash Loader PROM program or the Voter program contained in the Flash PROM (normal operation). This is accomplished by circuitry around U2. When 12 volts is either applied to or removed from the flash, a reset is generated by the dual comparator circuit U2. (Refer to discussion on Reset.)

During flashing, the CPTC program data is down loaded from the PC at X3-1 and is converted by the RS232/TTL converter U42. The TTL data (FLASH_RX) is routed to the RXD input of the Microcomputer U1 via the U35 logic circuits. Handshaking from the microcomputer to the PC (FLASH_TX) is routed to the TTL/RS232 converter U42 through logic circuits U13 and U36. Signal lines between the PC and the GPTC **PROG** connector are shown in Figure 5.

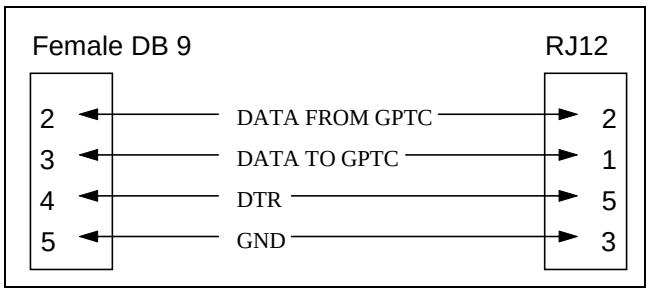


Figure 5 - Programming Cable (19B804346P111)

MAINTENANCE

RECOMMENDED TEST EQUIPMENT

The following equipment is required to test the GPTC:

- Oscilloscope
- Digital Voltmeter with fine tip probes
- Extender Board, ROA 117 2249 (Part of Test Module kit VPTS3X)
- Programming Cable, 19B804346P111 (Part of Test Module kit VPTS3X)

TESTING

An experienced technician can perform limited test and troubleshooting of the GPTC using the extender board to observe signals during operation. Individual resistors and capacitors may be replaced if care is used. The two soldering iron method is recommended. It is not recommended that ICs be replaced in the field.

NOTE

There are no adjustments on the GPTC.

TROUBLESHOOTING

When troubleshooting the GPTC, use the discussion in the Circuit Analysis section to help isolate problems. Use the extender board and the Test Point chart in Table 6 to check signals under operating conditions.

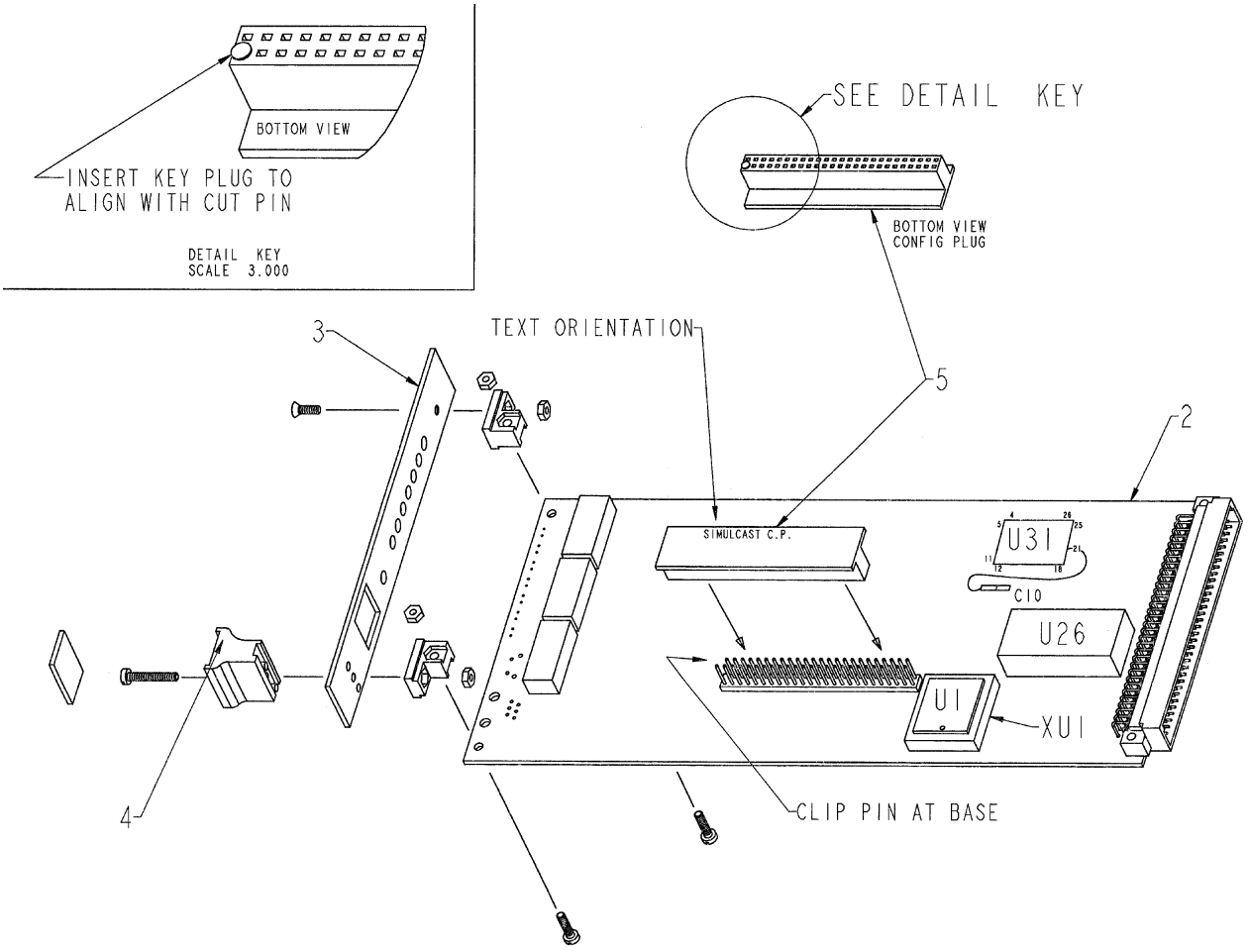
The Troubleshooting Chart provided in Table 7 lists some possible problems and recommended corrective action. Always check for correct configuration plug and proper installation of plug, DIP switch settings, socketted parts properly seated, blown fuses, and broken or missing parts.

Table 6 - Test Point Chart

TEST POINT	FUNCTION
TP30	OSC/2
TP31	GND
TP32	VCC
TP33	WALSH BIT 1
TP34	WALSH BIT 2
TP35	PH RECOVERED DATA
TP36	PH RX CLK
TP37	RF RCV DATA
TP38	RF RX CLK
TP39	PH TX CLK RS232
TP40	SYNC
TP41	BSL TX
TP101	RF TX DATA
TP102	INT0
TP103	VOL/SQ HI (RF DATA IN)
TP104	RF TX CLK
TP105	PH TX DATA
TP106	INT1
TP107	PH RX DATA

Table 7 - Troubleshooting Chart

SYMPTOM	AREA TO CHECK	POSSIBLE PROBLEM
RDY LED OFF after programming Flash PROM.	1. Programming may be corrupted, reprogram Flash PROM. 2. Ensure sufficient decay time is allowed before disconnecting the PC to GPTC programming cable. 3. Program will not load or loads incorrectly, DTR line to PC is not working.	1. The program "leafoff" controls the DTR out of the PC COMM port to turn on and off the +12 Vdc which must be applied to the Flash PROM on the GPTC in order to program it. 2. It is good practice to wait a few seconds after programming is over before unplugging the programming cable. This gives the +12 Vdc time to decay and avoids glitching the DTR while the +12 Vdc is still active. 3. When "leafoff" runs, DTR is at +12 Vdc (inactive state) initially, and FLASH_VPP on the GPTC is at 0V. When directed by the PC program, DTR goes to -12 Vdc causing FLASH_VPP to go to +12 Vdc. This prepares the Flash PROM for reprogramming. DTR is pin 20 on a DB25 connector and pin 4 on a DB-9 connector.
PC displays message "Radio not responding. Please cycle power on the radio."	1. Check voltage and fuses. 2. Check Programming cable. 3. Ensure Configuration plug and U26 are properly installed. 4. Initiate a reset.	1. Voltage at F1 should be +5 Vdc. Voltage at F2 should be +12 Vdc. Voltage at F3 should be -12 Vdc. 2. Disconnect and inspect Programming cable. 3. Observe proper orientation of Configuration plug and U26, refer to GPTC Assembly diagrams for installation information. 4. A reset may be initiated by turning power off, removing and reinserting the GPTC, or by pressing the S4 Reset button on the front panel.



NOTE:

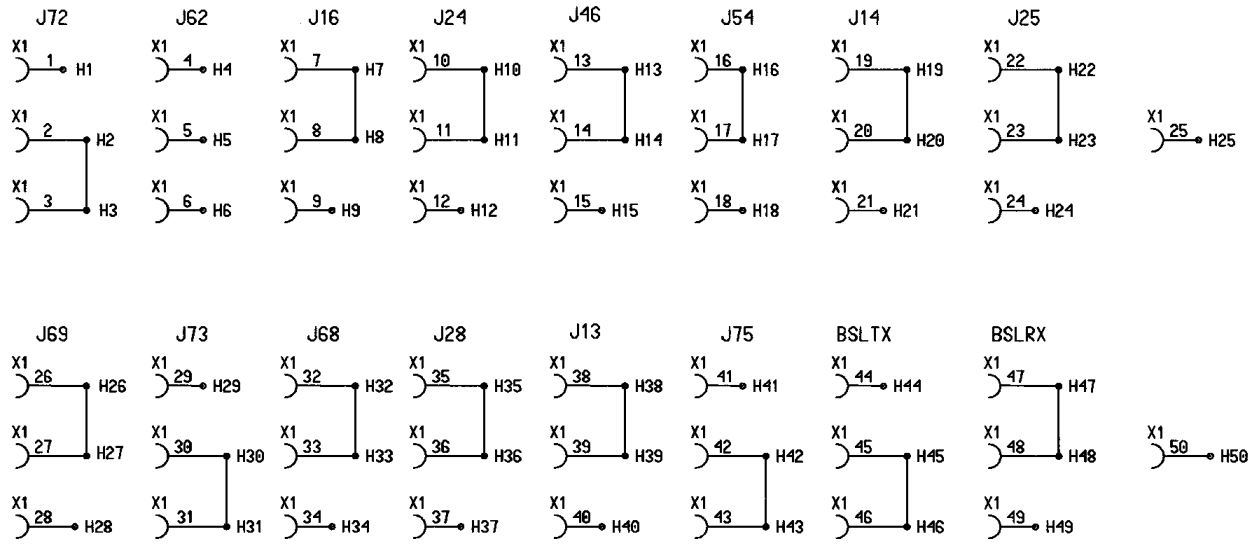
1. Tack solder one 47K ohm resistor (REP 625 425/47) to left side of C10 as shown. Tack solder a #26 solid insulated wire from other side of resistor to U31 pin 21.

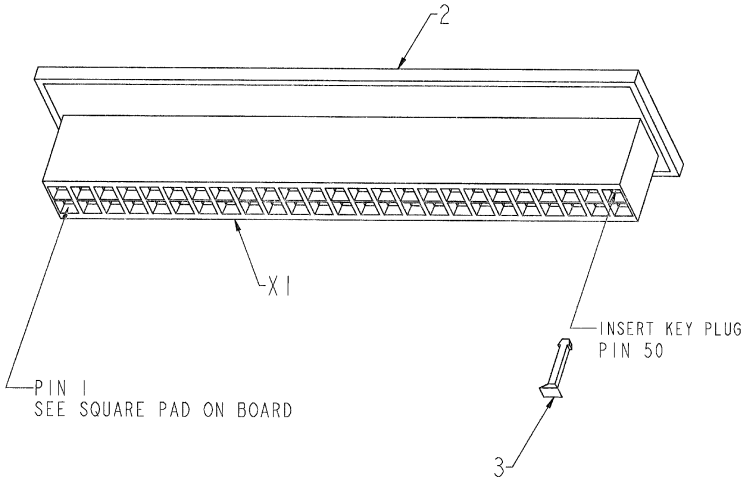
SIMULCAST CONTROL POINT TRUNKING CARD ASSEMBLY
131 32-ROA 117 2240/3
Revision: A

SYMBOL	PART NUMBER	DESCRIPTION
2	ROA 117 2240	General Purpose Trunking Card. (See separate parts list.)
3	SXA 120 4174/6	Simulcast Control Point Front Panel.
4	NTM 201 1079	Hardware Kit.
5	ROA 117 2273	Simulcast Control Point Configuration Plug. (See separate parts list.)
R131	REP 625 425/47	Chip: 47K Ohm 5% 1/8w
U1	RYT 121 6060/C	Digital: 8-Bit Microprocessor; sim to Dallas *Speedit µP* 80C320.

SIMULCAST CONTROL POINT TRUNKING CARD ASSEMBLY ROA 117 2240/3

(1/1078-ROA 117 2240/3, Sh. 1, Rev. A)



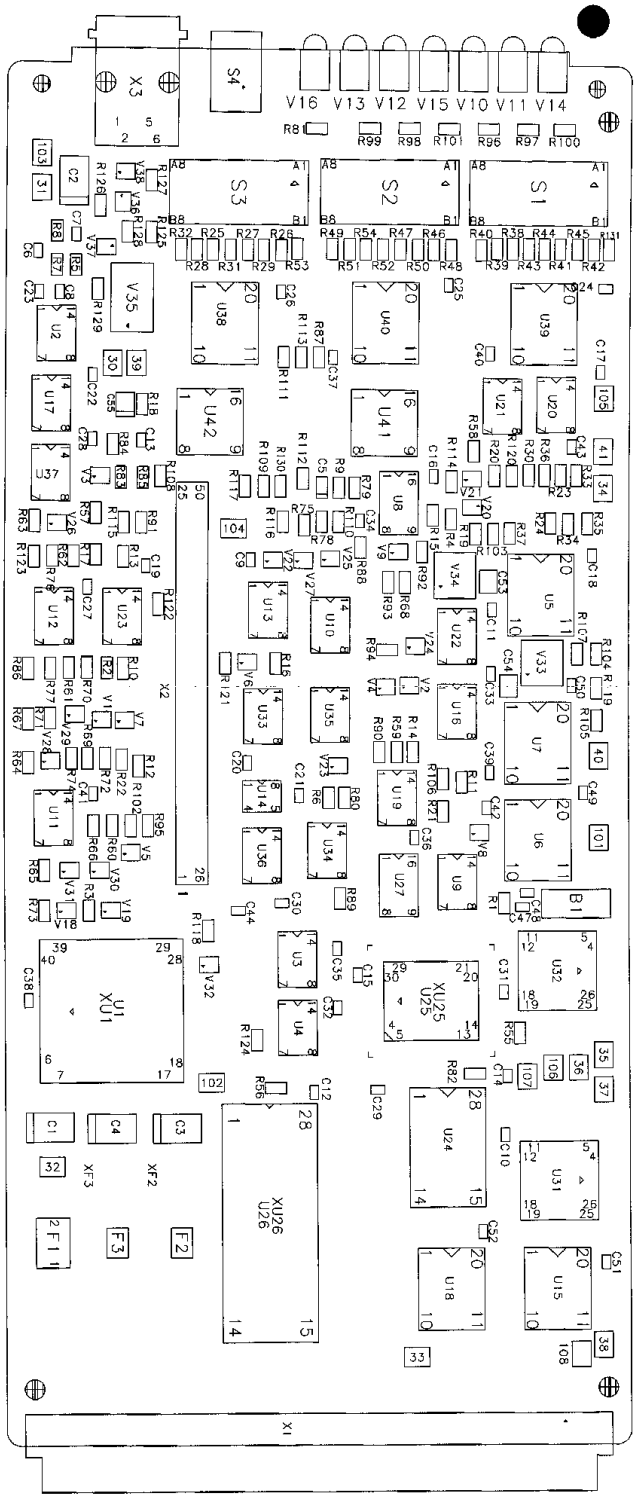


SIMULCAST CONTROL POINT CONFIGURATION PLUG
131 32 - ROA 117 2273
Revision: A

SYMBOL	PART NUMBER	DESCRIPTION
	TVA 117 2242 R1	Printed Wiring Board.
2		
3	RNY 101 01/4	Keying Plug.
		---------- CONNECTORS ---------
X1	RNV 403 105/225	Connector, Receptacle, PWB mounted.

SIMULCAST CPTC CONFIGURATION PLUG ROA 117 2273

(1911-ROA 117 2273 Sh. 1, Rev. A; 1078-ROA 117 2273, Sh. 1, Rev. A)



GPTC PRINTED WIRING BOARD ASSEMBLY
ROA 117 2240

(1078-ROA 117 2240, Sh. 1, Rev. B)

GENERAL PURPOSE TRUNKING CARD (GPTC)
PRINTED WIRING BOARD ASSEMBLY

131 32 - ROA 117 2240
Revision: F

SYMBOL	PART NUMBER	DESCRIPTION
2	TVK 117 2217 R3	Printed Wiring Board.
		---------- CRYSTALS ----------
B1	RTM 501 658/01	Quartz crystal unit; 11.0592 MHz.
		---------- CAPACITORS ----------
C1 thru C4	RJE 584 3168/47	Tantalum, electrolytic SMD: 47 µF, ±20%, 16 V.
C5	RJE 584 3107/22	Tantalum, electrolytic SMD: 2.2 µF, ±20%, 10V.
C6 thru C44	RJC 464 3045/1	Monolithic ceramic chip: 10 nF, ±10%, 50V.
C47 and C48	RJC 463 4042/27	Monolithic ceramic chip: 27 pF ±5%, 50V.
C49 thru C52	RJC 464 3045/1	Tantalum, electrolytic SMD: 2.2 µF, ±20%, 10V.
C53 and C54	RJC 463 4074/1	Monolithic ceramic chip: 1.0 nF ±5% 50V.
C55	RJE 584 3167/22	Tantalum, electrolytic SMD: 2.2 µF ±20% 16V.
		---------- FUSES ----------
F1	REZ 701 16/4	Thermistor Circuit Protector: 1.0A 30V PTC, 1.5w when tripped.
F2	REZ 701 28/1	Thermistor Circuit Protector: 0.5A 15V PTC, 0.8w when tripped.
F3	REZ 701 28/1	Thermistor Circuit Protector: 0.5A 15V PTC, 0.8w when tripped.
		---------- RESISTORS ----------
R1	REP 625 428/1	Ceramic chip: 10 Meg, 5%, 1/8w.
R2 thru R11	REP 625 426/1	Ceramic chip: 100K, 5%, 1/8w.
R12 and R13	REP 625 425/47	Ceramic chip: 47K, 5%, 1/8w.
R14 and R15	REP 625 425/27	Ceramic chip: 27K, 5%, 1/8w.
R16	REP 625 425/22	Ceramic chip: 22K, 5%, 1/8w.
R17	REP 625 425/12	Ceramic chip: 12K, 5%, 1/8w.
R18	REP 625 425/1	Ceramic chip: 10k, 5%, 1/8w.
R19	REP 625 423/1	Ceramic chip: 100 Ohm, 5%, 1/8w.
R20	REP 625 423/51	Ceramic chip: 510 Ohm, 5%, 1/8w.
R21 thru R87	REP 625 425/1	Ceramic chip: 10K, 5%, 1/8w.
R88 and R89	REP 625 424/47	Ceramic chip: 4.7K, 5%, 1/8w.
R90 and R91	REP 625 424/39	Ceramic chip: 3.9K, 5%, 1/8w.
R92 thru R95	REP 625 424/22	Ceramic chip: 2.2K, 5%, 1/8w.
R96 thru R102	REP 625 424/1	Ceramic chip: 1K, 5%, 1/8w.
R103 and R104	REP 625 424/39	Ceramic chip: 3.9K, 5%, 1/8w.
R105	REP 625 423/51	Ceramic chip: 510 Ohm, 5%, 1/8w.
R106	REP 625 423/47	Ceramic chip: 470 Ohm, 5%, 1/8w.
R107 thru R117	REP 625 423/1	Ceramic chip: 100 Ohm, 5%, 1/8w.
R118	REP 625 425/1	Ceramic chip: 10K, 5%, 1/8w.
R119 and R120	REP 625 423/51	Ceramic chip: 510 Ohm, 5%, 1/8w.
R121 thru R123	REP 625 425/1	Ceramic chip: 10K, 5%, 1/8w.
R124	REP 625 424/1	Ceramic chip: 1K, 5%, 1/8w.
R125 and R126	REP 625 426/1	Ceramic chip: 100K, 5%, 1/8w.
R127 thru R129	REP 625 425/1	Ceramic chip: 10K, 5%, 1/8w.
R130	REP 625 425/1	Ceramic chip: 10K, 5%, 1/8w.
R131	REP 625 425/47	Ceramic chip: 47K, 5%, 1/8w.
		----------SWITCHES ----------
S1 thru S3	RMF 356 001/08	Switch, DIP; 8 position.
S4	RMD 955 006/01	Switch, Push Button.
		----------TEST POINTS ----------
TP30 thru	RPV 403 813/01	Connector, test point 1 pole.

SYMBOL	PART NUMBER	DESCRIPTION
TP107		
		-------INTEGRATED CIRCUITS-------
U1		Refer to next highrer assembly.
U2	RYT 101 321/C	Linear: Quad Voltage Comparator; sim to LM339.
U3 and U4	RYT 318 0000/C	Digital: 4x2 In NAND Gate; sim to 74AC00.
U5 thru U7	RYT 306 2031/C	Digital: CMOS 8-Bit Flip-flop; sim to 74HC273.
U8	RYT 306 2024/C	Digital: CMOS 2 x Monostable Multivbrator; sim to 74HC4538.
U9 thru U13	RYT 306 2020/C	Digital: CMOS 6 x Inverter, Schmitt Trigger; sim to 74HC14.
U14	RYT 113 6065/1	Digital: Microprocessor Supervisory Reset Circuit; sim to MAX705CSA.
U15	RYT 306 2013/C	Digital: CMOS Octal Tri-state Transceiver; sim to 74HC245.
U16	RYT 306 2006/C	Digital: CMOS Quad 2-Input NOR Gate; sim to 74HC02.
U17	RYT 306 2003/C	Digital: CMOS Dual Data Flip-flop; sim to 74HC74.
U18	RYT 304 0373/C	Digital: Octal Data Latch; sim to 74HC373.
U19 thru U23	RYT 202 106/C	Digital: Hex Open Collector Inverter; sim to 7406.
U24	RYT 119 6005/4C	Digital: 32K x 8 Static RAM; sim to ECI55257AFL.
U25	RYT 118 6040/C	Digital: CMOS 64K x 8 Flash Memory; sim to 28F512S200.
U26	RON 107 756/1	Preprogrammed 512K byte UV EPROM; part of Media kit 3501521G1.
U27	RYT 116 006/C	Digital: Dual 2-to-1 Decoder/Demultiplexer; sim to 74LS155.
U31 and U32	ROP 101 688/4C	Integrated Circuit, Modem.
U33 thru U37	RYT 306 2001/C	Digital: CMOS QUAD 2-Input NAND Gate; sim to 74HC00.
U38 thru U40	RYT 306 2012/C	Digital: Octal Tri-state Buffer; sim to 74HC244.
U41 thru	RYT 109 6073/1	EIA232-D and CCITT V.28

SYMBOL	PART NUMBER	DESCRIPTION
U42		driver/receiver; sim to MC145406.
		---- DIODES and TRANSISTORS ----
V1 thru V8	RYN 121 675/1	Transistor, Silicon, NPN, low profile; sim to MMBT3904
V9	RYN 120 619/1	Transistor, Silicon, PNP, low profile; sim to MMBT3906
V10 thru V16	RKZ 433 637/1	Light Emitting Diode: 90 degree RED, T1 package.
V18 thru V32	RKZ 123 03/1	Diode, Dual - switching; sim to BAV99, SOT-23.
V33 and V34	RYN 123 621/1	FET, medium power N-channel enhancement mode; sim to BSP29, SOT-223.
V35	RYN 122 623/1	FET, Power P-channel enhancement mode; sim to MTD406.
V36 and V37	RYN 121 675/1	Transistor, Silicon, NPN, low profile; sim to MMBT3904
V38	RKZ 123 03/1	Diode, Dual - switching; sim to BAV99, SOT-23.
		----------CONNECTORS----------
X1	RPV 403 209/102	Connector, 96 contact.
X2	RPV 380 220/225	Connector, double row pin strip.
X3	RNV 403 19/06	Connector, socket.
		-------- SOCKETS & HOLDERS --------
XU1	RNK 860 12/044	Holder PLCC 44-pole.
XU25	RNK 860 11/1	Holder PLCC 32-pole; sim to AMP 822034-1.
XU26	RNK 841 001/28	Holder DIL 28-pole.

PRODUCTION CHANGES

Changes in the equipment to improve performance or simplify circuits are identified by a "Revision Letter," which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the parts list for the descriptions of the parts affected by these revisions.

Rev. R1B - ROA 117 2240

Change added Crystal B1 to parts list.

Rev. R2A - ROA 117 2240

Changes revision level of printed wiring board (item 2, TVK 117 2217) from R1 to R2. Rev. R1 and R2 PWBs are functionally equivalent.

Changes connector X3 from RNV 256 103 to RNV 403 19/06.

Rev. R2B - ROA 117 2240

Changed U31 and U32 to to new version of the Modem IC. Was: ROP 101 688/C Replaced by: ROA 101 688/4C. New version is functionally equivalent.

Rev. R2C - ROA 117 2240

Parts list restructured to move U1 from 131 23 - ROA 117 2240 to next higher assembly.

Rev. R3A - ROA 117 2240

To improve the functionality and producability of the assembly, the following components were removed, added, or replaced:

Removed:

ICs - U28,U28,U30	RYT 109 082/C
Fuse Holder - XF1, XF2, XF3	NFN 102 04

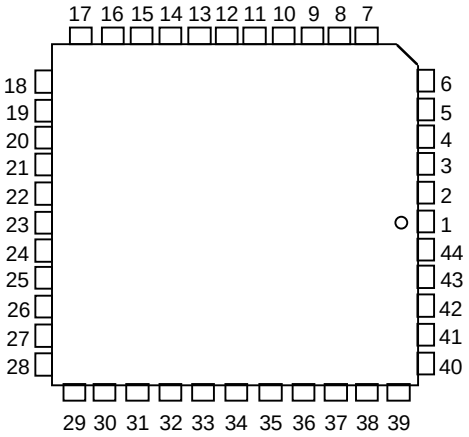
Added:

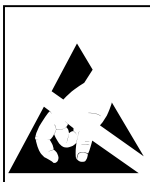
ICs - U41 and U42	RYT 109 6073/1
Resistor R130	REP 625 425/1
Resistor R131	REP 625 425/47

Replaced:

Swicth S1, S2, S3	was: RMF 356 004/08 Repl. by: RMF 356 001/08
Fuse F1	was: NGH 241 04/1 Repl. by: REZ 701 16/4
Fuse F2 and F3	was: NGH 241 03/25 Repl. by: REZ 701 28/1
TP30 thru TP107	was: RPV 380 902/01 Repl. by: RPV 403 813/01
Printed Wiring Board	was: TVK 117 2217 R2 Repl. by: TVK 117 2217 R3

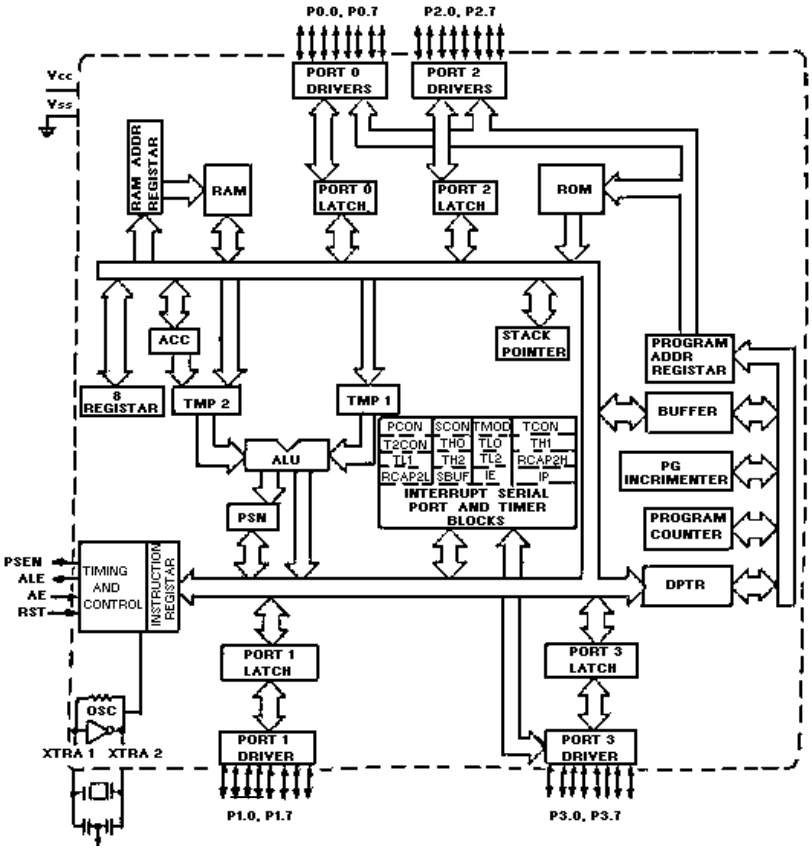
8-BIT MICROPROCESSOR - U1
RYT 121 6060/C (P80C32)





CAUTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

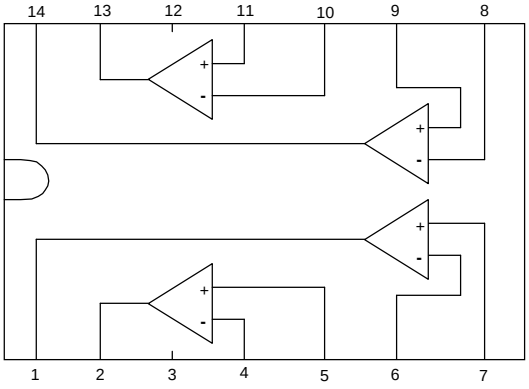
FUNCTION DIAGRAM



PIN	FUNCTION	PIN	FUNCTION
1	NC	23	NC
2	T2/P1.0	24	P2.0/A8
3	T2EX/P1.1	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6	30	P2.6/A14
9	P1.7	31	P2.7/A15
10	RST	32	$\overline{\text{PSEN}}$
11	RxD/P3.0	33	ALE/$\overline{\text{PROG}}$
12	NC	34	NC
13	TxD/P3.1	35	EA/Vpp
14	$\overline{\text{INT0}}$/P3.2	36	P0.7/AD7
15	$\overline{\text{INT1}}$/P3.3	37	P0.6/AD6
16	T0/P3.4	38	P0.5/AD5
17	$\overline{\text{T1}}$/P3.5	39	P0.4/AD4
18	$\overline{\text{WR}}$/P3.6	40	P0.3/AD3
19	RD/P3.7	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	Vss	44	Vcc

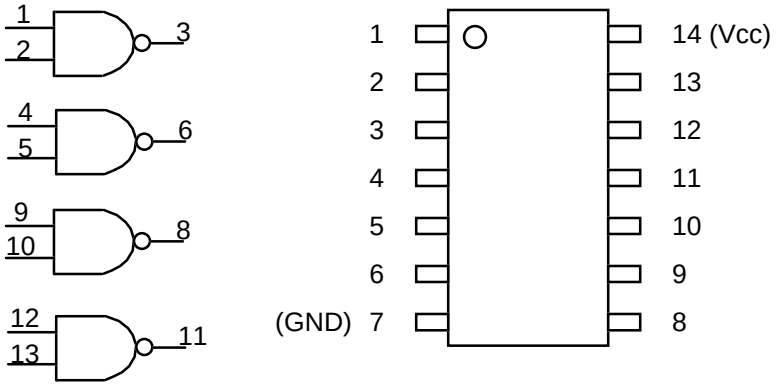
U2 - QUAD VOLTAGE COMPARATOR
RYT 101 321/C (LM339)

TERMINAL	FUNCTION
3	Positive voltage supply
12	Negative voltage supply
	Opamp 1
4	Inverting input (-IN)
5	Noninverting input (+IN)
2	Output
	Opamp 2
6	Inverting input (-IN)
7	Noninverting input (+IN)
1	Output
	Opamp 3
8	Inverting input (-IN)
9	Noninverting input (+IN)
14	Output



	Opamp 4
10	Inverting input (-IN)
11	Noninverting input (+IN)
13	Output

U3 AND U4- NAND GATE
RYT 318 0000/C (74AC00)

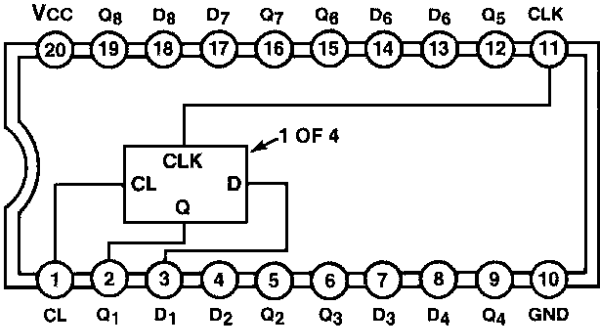


TRUTH TABLE

INPUTS		OUTPUTS
A1 (A2,A3,A4)	B1 (B2,B3,B4)	O1 (O2,O3,O4)
L	L	H
L	H	H
H	L	H
H	H	L

CMOS OCTAL DATA FLIP-FLOP - U5, U6 & U7
RYT 306 2031/C (74HC273)

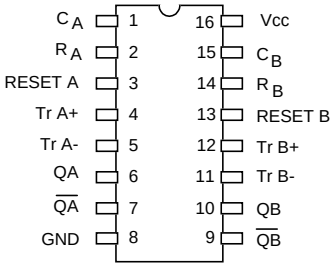
CAUTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES



INPUTS		OUTPUTS	
CLEAR	CLOCK	D	Q
Ø	X	X	Ø
1		1	1
1		Ø	Ø
1	Ø	X	Q_0

X = DON'T CARE Q_0 = Q BEFORE

CMOS 2 X MONOSTABLE MULTIVIBRATOR - U8
RYT 306 2024/C (74HC4538)



FUNCTION TABLE

INPUTS			OUTPUTS	
Reset	+Triggr	- Trigg	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎍
H	↑	H	⎍	⎍

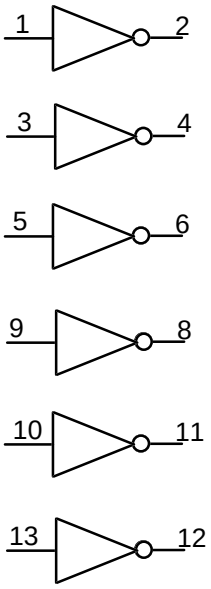
X = H or L

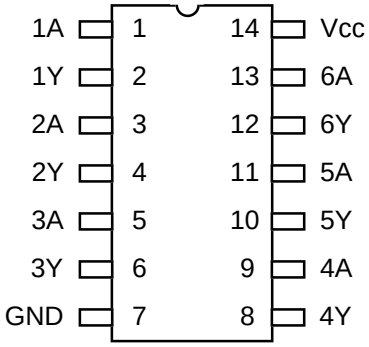
↑ = from L to H

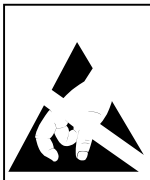
↓ = from H to L

CAUTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

U9 THRU U13 - 6 X INVERTER, SCHMITT TRIGGER
RYT 306 2020/C (74HC14)

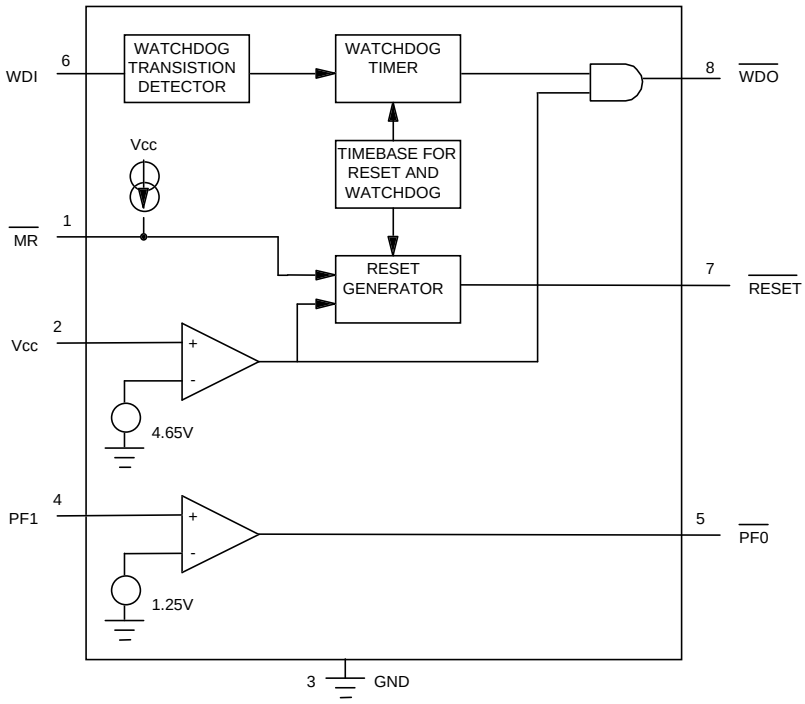


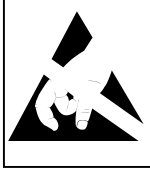




CAUTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

U14 - MICROPROCESSOR SUPERVISORY CIRCUIT
RYT 113 6065/1 (MAX705CSA)

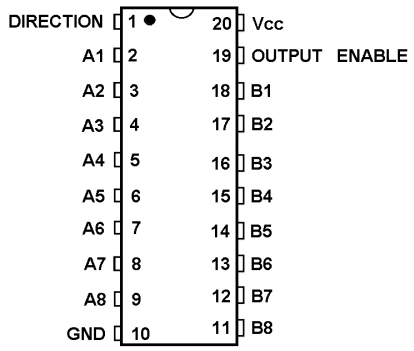




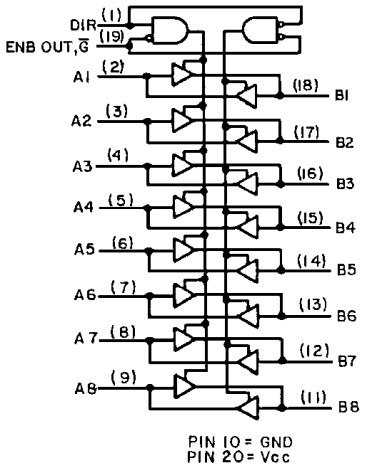
CAUTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

U15 - CMOS OCTAL TRI-STATE TRANSCEIVER
RYT 306 2013/C (74HC245)

PIN ASSIGNMENT



LOGIC DIAGRAM (POSITION LOGIC)



PIN 10 = GND
PIN 20 = Vcc

CAUTION
OBSERVE PRECAUTIONS FOR HANDLING **ELECTROSTATIC SENSITIVE DEVICES**

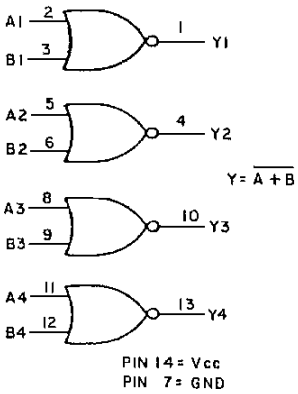
FUNCTION TABLE

CONTROL INPUTS		OPERATION
OUTPUT ENABLE	DIRECTION	
L	L	DATA TRANSMITTED FROM BUS B TO BUS A
L	H	DATA TRANSMITTED FROM BUS A TO BUS B
H	X	BUSES ISOLATOR (HIGH IMPEDANCE STATE)

X=DON'T CARE

U16
CMOS QUAD 2-INPUT NOR GATE
RYT 306 2006/C (74HC02)

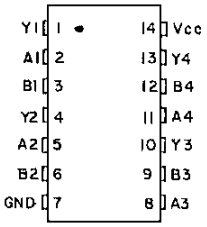
LOGIC DIAGRAM



$Y = \overline{A + B}$

PIN 14 = Vcc
PIN 7 = GND

PIN ASSIGNMENT

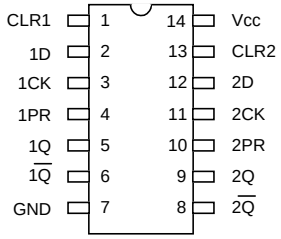


FUNCTION DIAGRAM

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

CAUTION
OBSERVE PRECAUTIONS FOR HANDLING **ELECTROSTATIC SENSITIVE DEVICES**

U17
CMOS DUAL DATA FLIP-FLOP
RYT 306 2003/C (74HC74)



FUNCTION TABLE

INPUTS				OUTPUTS	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	H	L	X	H*	H*
H	L	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

X = Any input, including transistion

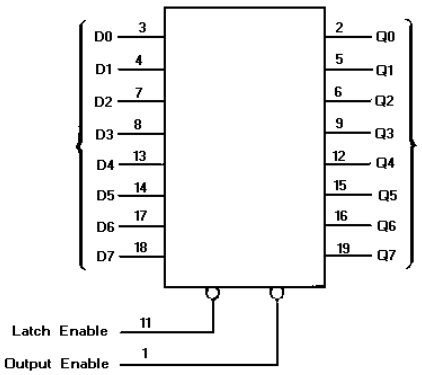
↑ = from L to H

Q_0 = The level of Q after the previous clock pulse

* = Nonstable; don't persist when PR and CLR are set high

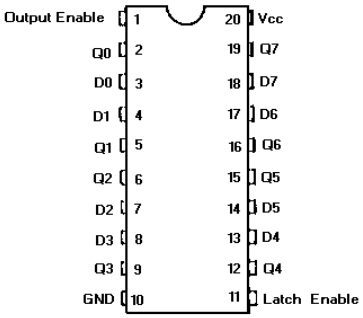
U18 - OCTAL DATA LATCH
RYT 304 0373/C (74HC373)

BLOCK DIAGRAM



Pin 20 = Vcc
Pin 10 = GND

PIN ASSIGNMENT

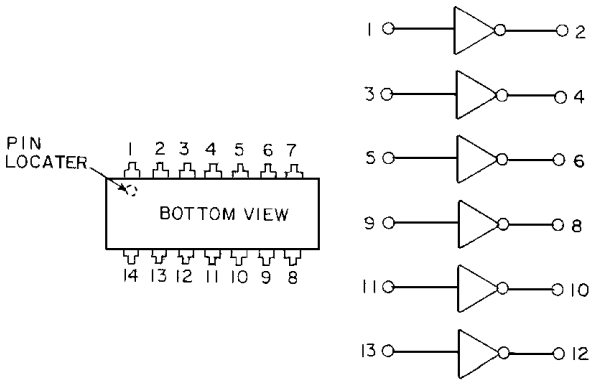


FUNCTION TABLE

Output Enable	Latch Enable	D	Output
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

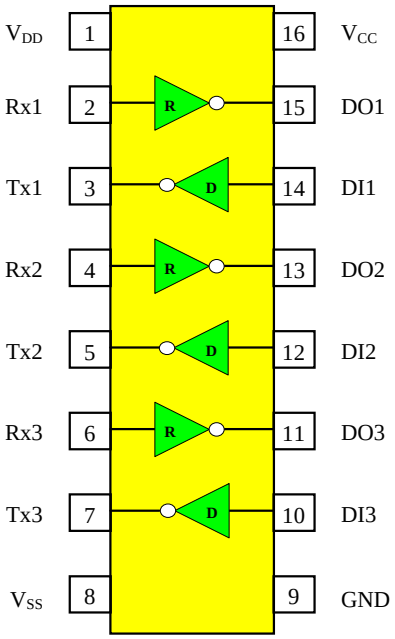
X = don't care
Z = high impedance

U19 THRU U23
HEX OPEN COLLECTOR INVERTER
RYT 202 106/C (7406)



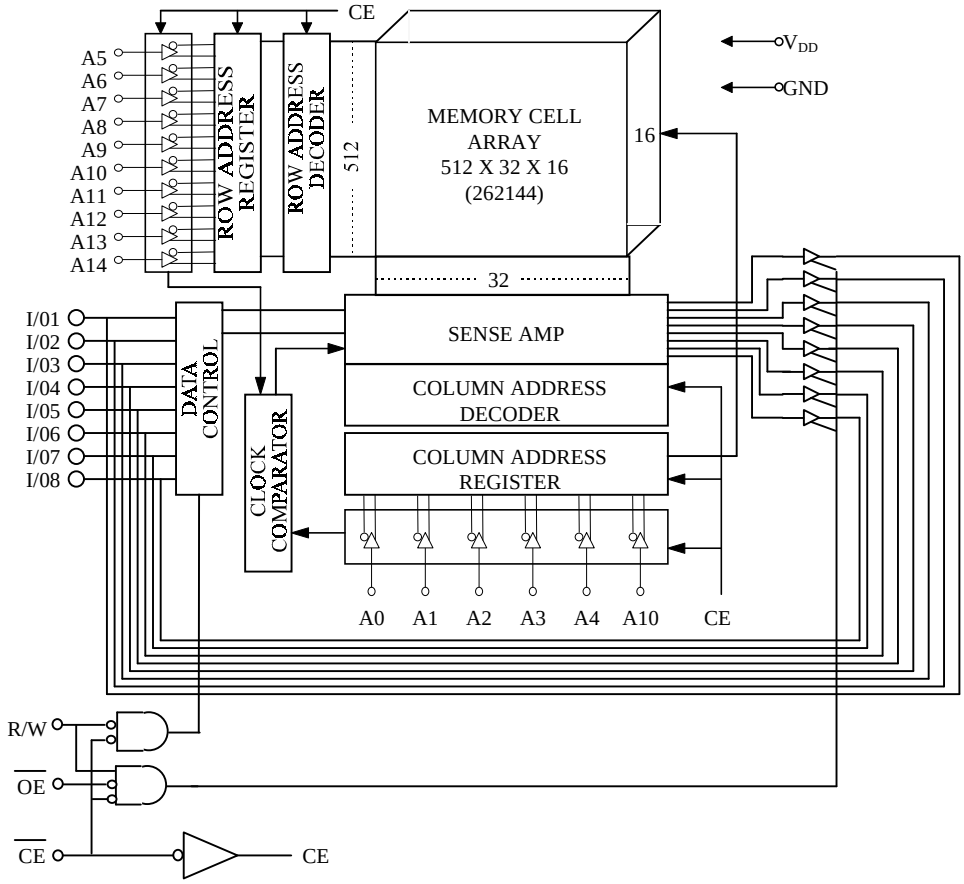
GND = 7
Vcc = 14

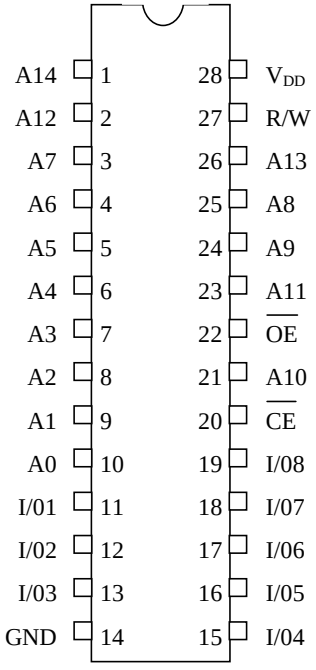
U41 AND U42 - RS232 - TTL CONVERTER
RYT 109 6073/1 (145406)



D = Driver
R = Receiver
DI = Data In
DO = Data Out

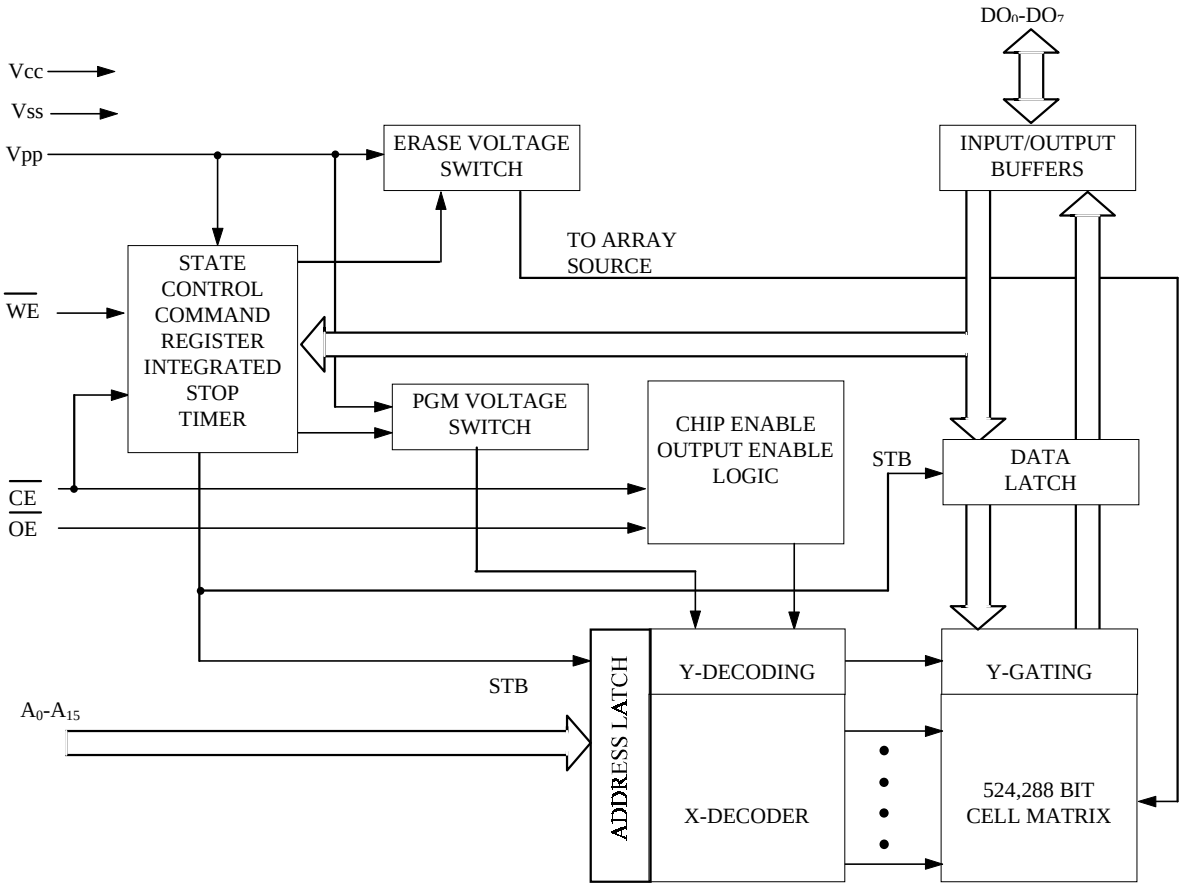
U24
32K X 8 STATIC RAM
RYT 119 6005/4C (EC155257AFL)

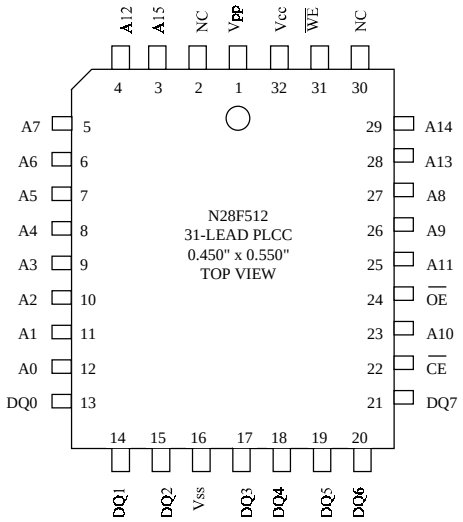




PIN NAMES	FUNCTION
A0 thru A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
I/01 thru I/08	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

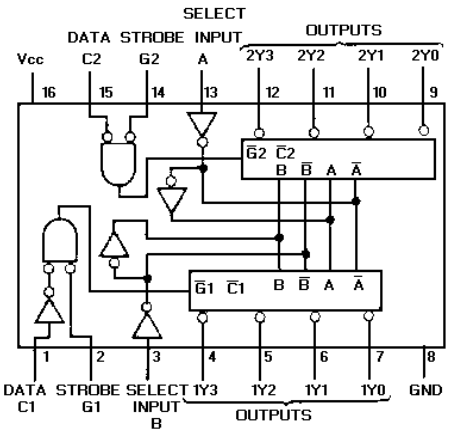
U25
CMOS 64K X 8 FLASH MEMORY
RYT 118 6040/C (28F512S200)





SYMBOL	TYPE	NAME AND FUNCTION
A_0-A_{15}	Input	ADDRESS INPUT for memory address. Addresses are internally latched during a write cycle.
DQ_0-DQ_7	Input/Output	DATA INPUT/OUTPUT: Inputs data during memory write cycles; outputs data during memory read cycles.
$\overline{CE}$	Input	CHIP ENABLE: Activates the device's control logic, input buffers, decoders, and sense amplifiers.
$\overline{OE}$	Input	OUTPUT ENABLE: Gates the devices output through the databuffers during a read cycle.
$\overline{WE}$	Input	WRITE ENABLE: Controls writes to the control register and the array.
Vpp		ERASE/PROGRAM SUPPLY for writing the command register, erasing the entire array, or programming bytes in the array.
Vcc		Device Power Supply. (5V ±10%)
Vss		Ground
NC		No connection to device.

U27 - DUAL 2-TO-1 DECODER/DEMULTIPLEXER
RYT 116 006/C (74LS155)

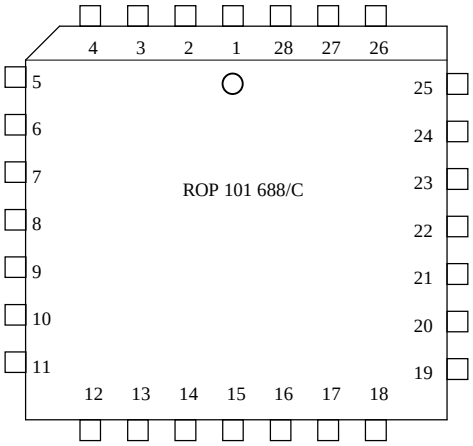


2-Line-to-4-Line Decoder
or 1-Line-to-4-Line Demultiplexer

Inputs			Outputs			
Select	Strobe	Data				
B A	G1	C1	1Y0	1Y1	1Y2	1Y3
X X	H	X	H	H	H	H
L L	L	H	L	H	H	H
L H	L	H	H	L	H	H
H L	L	H	H	H	L	H
H H	L	H	H	H	H	L
X X	X	L	H	H	H	H

Inputs			Outputs			
Select	Strobe	Data				
B A	G2	C2	2Y0	2Y1	2Y2	2Y3
X X	H	X	H	H	H	H
L L	L	L	L	H	H	H
L H	L	L	H	L	H	H
H L	L	L	H	H	L	H
H H	L	L	H	H	H	L
X X	X	H	H	H	H	H

U31 AND U32 - MODEM
ROP 101 688/4C

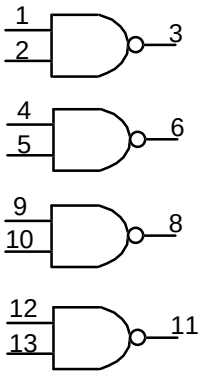


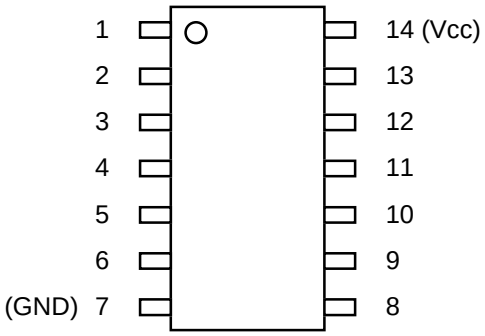
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	RE	Read Enable (active low).
2	EN	Chip Enable (active low).
3	RESOUT	Resout Output (active high).
4	AD0	Bi-directional Address/Data Bus.
5	AD1	Bi-directional Address/Data Bus.
6	AD2	Bi-directional Address/Data Bus.
7	AD3	Bi-directional Address/Data Bus.
8	AD4	Bi-directional Address/Data Bus.
9	AD5	Bi-directional Address/Data Bus.
10	AD6	Bi-directional Address/Data Bus.
11	AD7	Bi-directional Address/Data Bus.
12	ALE	Address Latch Enable (active high).
13	VSS	Ground.
14	CLK1	Buffered Oscillator Output.
15	VDD	Power Supply.
16	XTAL1	Oscillator Input.
17	XTAL2	Oscillator Output.
18	CLK2	640 kHz Output.
19	DATAIN	Received Data Input.
20	SAT/G1	Received SAT Input/G1 EN.HC138 (active high).
21	TXDAT	Transmit Data Output.
22	RCVCLK/ Q2	Recovered Clock Output/Q2 Output for HC138).
23	RCVCLK/ Q0	Recovered Clock Output/Q0 Output for HC138).
24	INT	Interrupt Request (active low O.D.).
25	RESIN	Reset Input (active high).
26	CS	Chip Select (active low).
27	CLK3/4	Transmit Clock Output/CLK1/6 Output.
28	WR	Write Enable (active low).

U33 THRU U37
CMOS QUAD TWO INPUT NAND GATE
RYT 306 2001/C (74HC00)

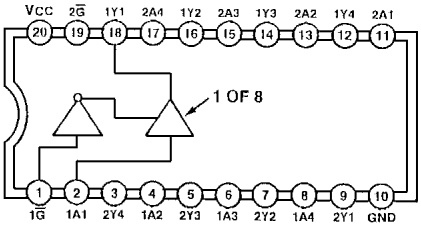
TRUTH TABLE

INPUTS		OUTPUTS
Pin 1 (4, 9, 12)	Pin 2 (5, 10, 13)	Pin 3 (6, 8, 11)
L	L	H
L	H	H
H	L	H
H	H	L



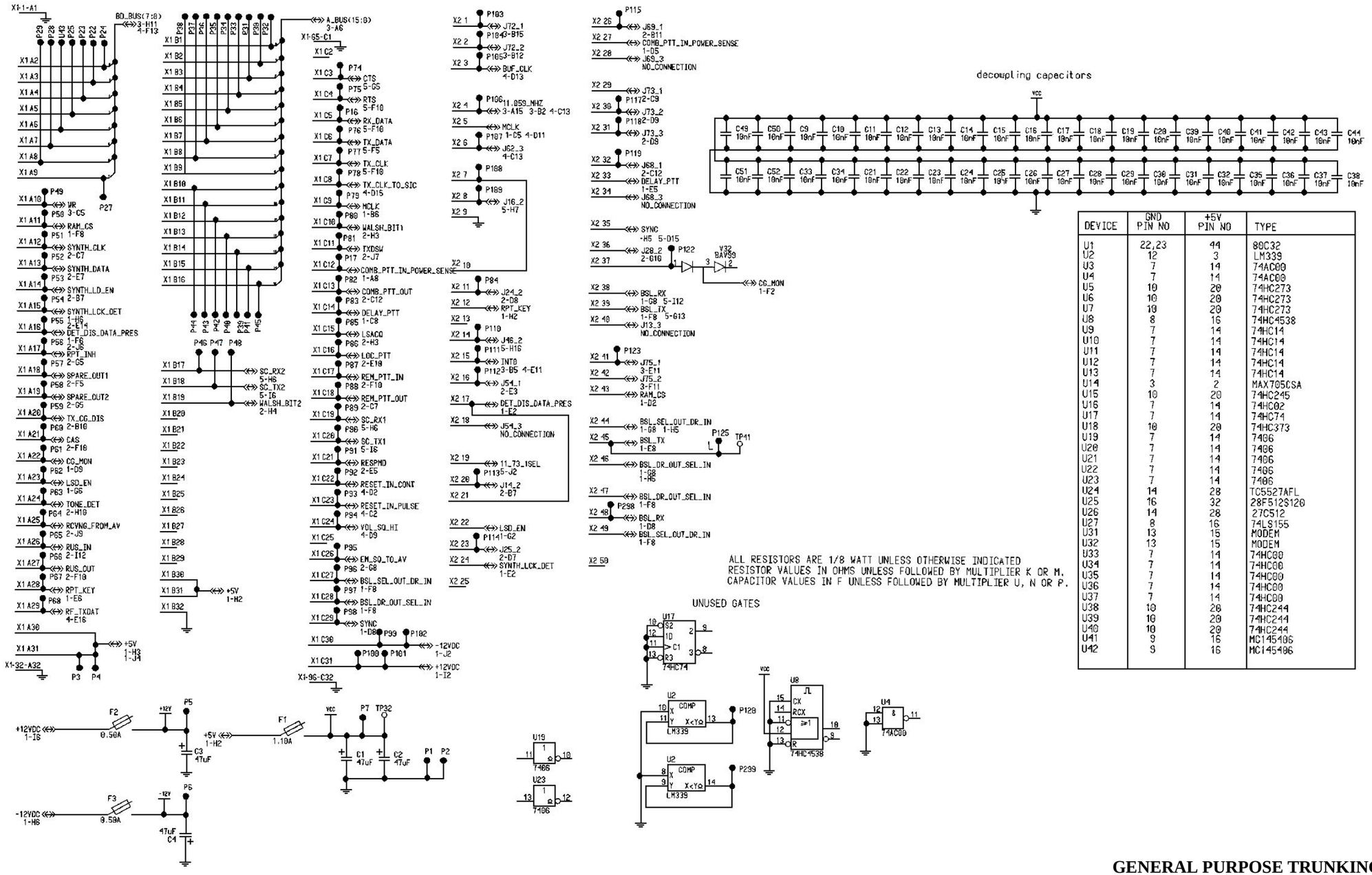


U38 THRU U40
OCTAL TRI-STATE BUFFER
RYT 306 2012/C (74HC244)



$\overline{1G}$	1A	1Y	$\overline{2G}$	2A	2Y
0	0	0	0	0	0
0	1	1	0	1	1
1	0	Z	1	0	Z
1	1	Z	1	1	Z

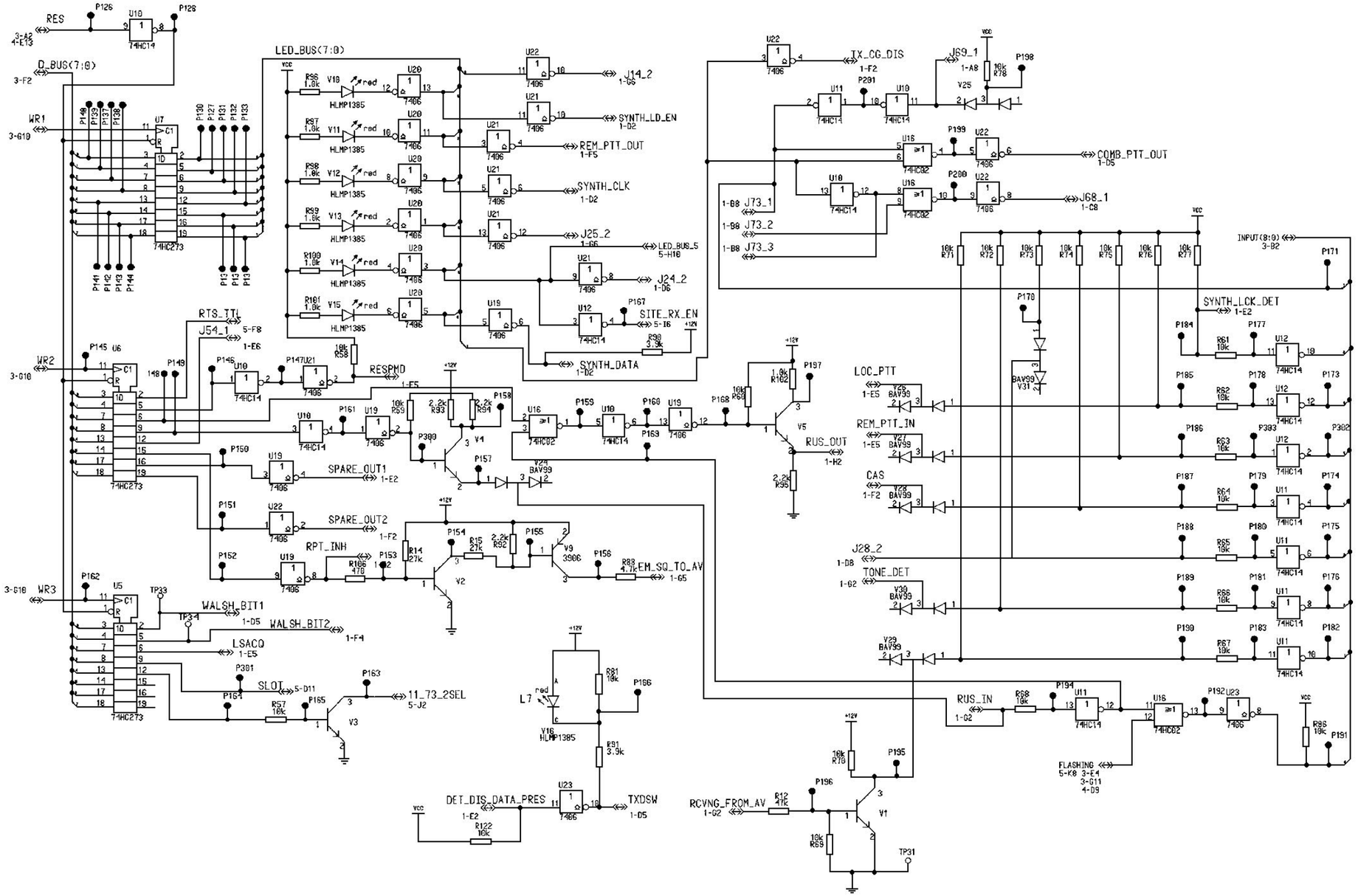
Z = HIGH IMPEDANCE



DEVICE	GND PIN NO	+5V PIN NO	TYPE
U1	22,23	44	80C32
U2	12	3	LM339
U3	7	14	74AC00
U4	7	14	74AC00
U5	10	20	74HC273
U6	10	20	74HC273
U7	10	20	74HC273
U8	8	16	74HC4538
U9	7	14	74HC14
U10	7	14	74HC14
U11	7	14	74HC14
U12	7	14	74HC14
U13	7	14	74HC14
U14	3	2	MAX705CSA
U15	10	20	74HC245
U16	7	14	74HC02
U17	7	14	74HC74
U18	10	20	74HC373
U19	7	14	7406
U20	7	14	7406
U21	7	14	7406
U22	7	14	7406
U23	7	14	7406
U24	14	28	TC5527AFL
U25	16	32	28F512$120
U26	14	28	27C512
U27	8	16	74LS155
U31	13	15	MODEM
U32	13	15	MODEM
U33	7	14	74HC00
U34	7	14	74HC00
U35	7	14	74HC00
U36	7	14	74HC00
U37	7	14	74HC00
U38	10	20	74HC244
U39	10	20	74HC244
U40	10	20	74HC244
U41	9	16	MC145406
U42	9	16	MC145406

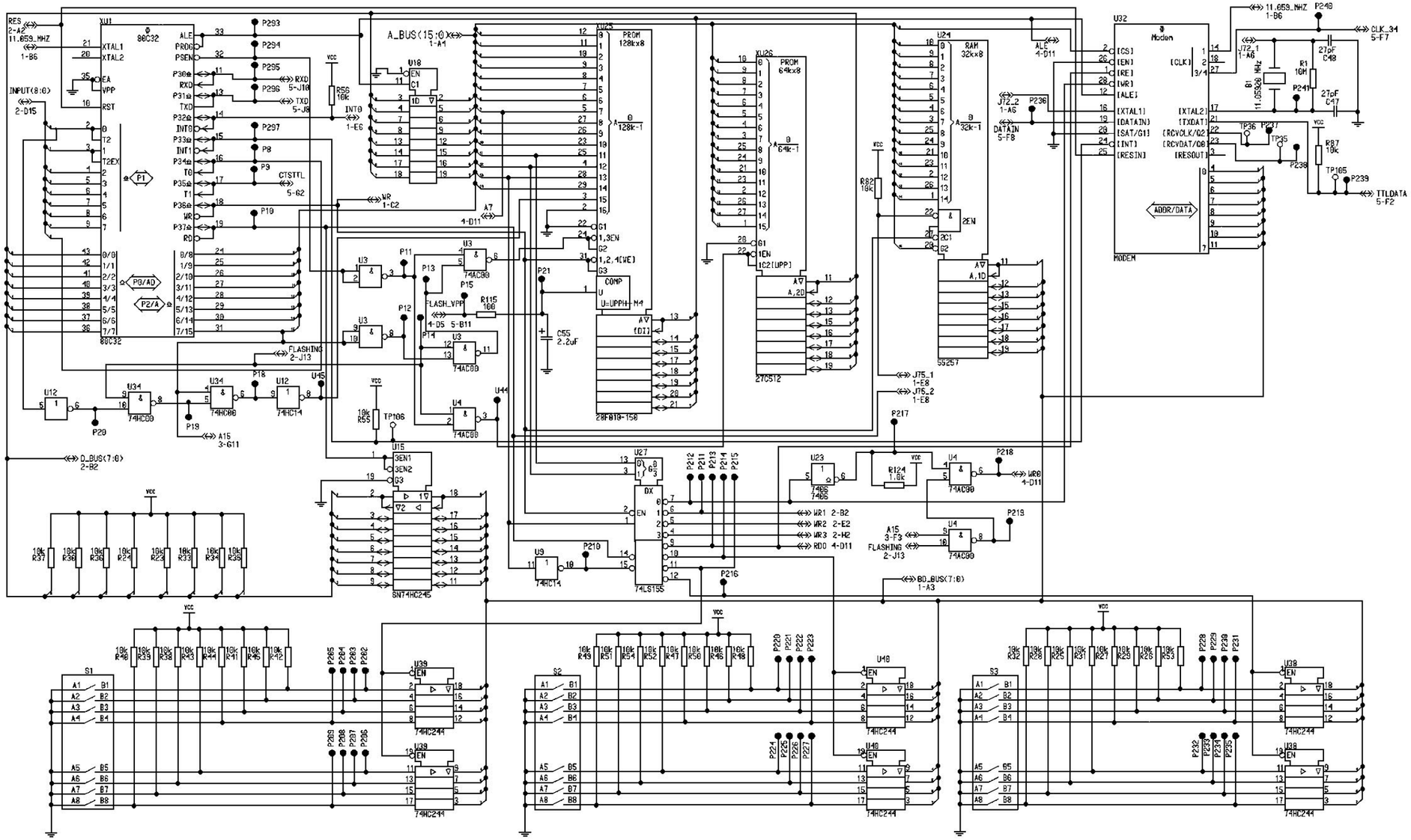
GENERAL PURPOSE TRUNKING CARD
ROA 117 2240

(1911-ROA 117 2240, Sh. 1, Rev. C)



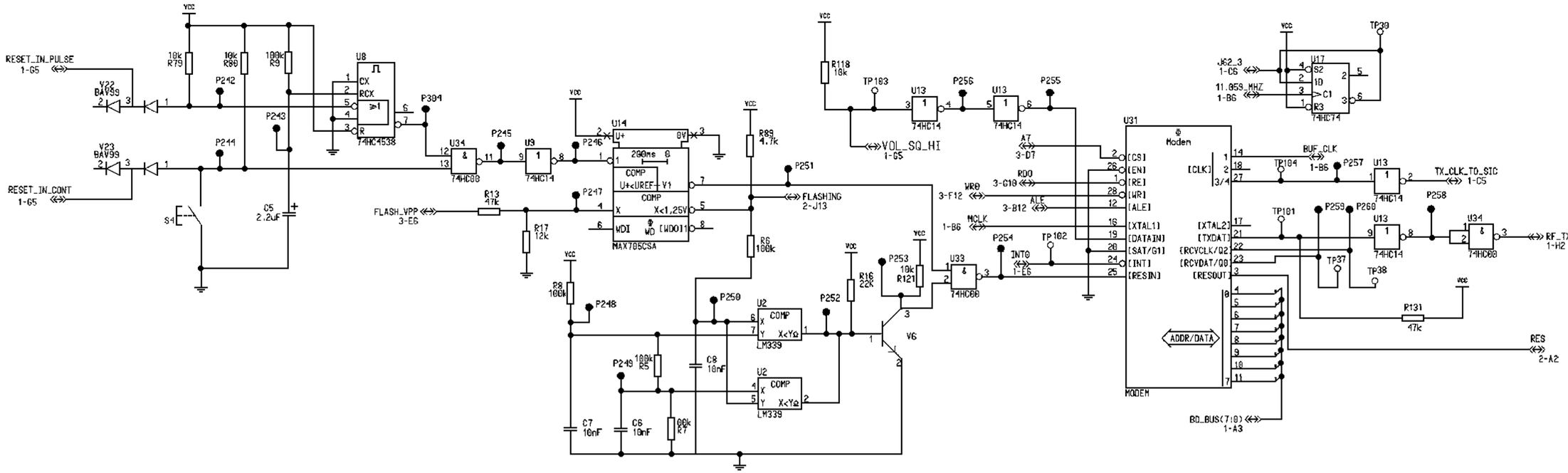
GENERAL PURPOSE TRUNKING CARD
ROA 117 2240

(1911-ROA 117 2240, Sh. 2, Rev. C)



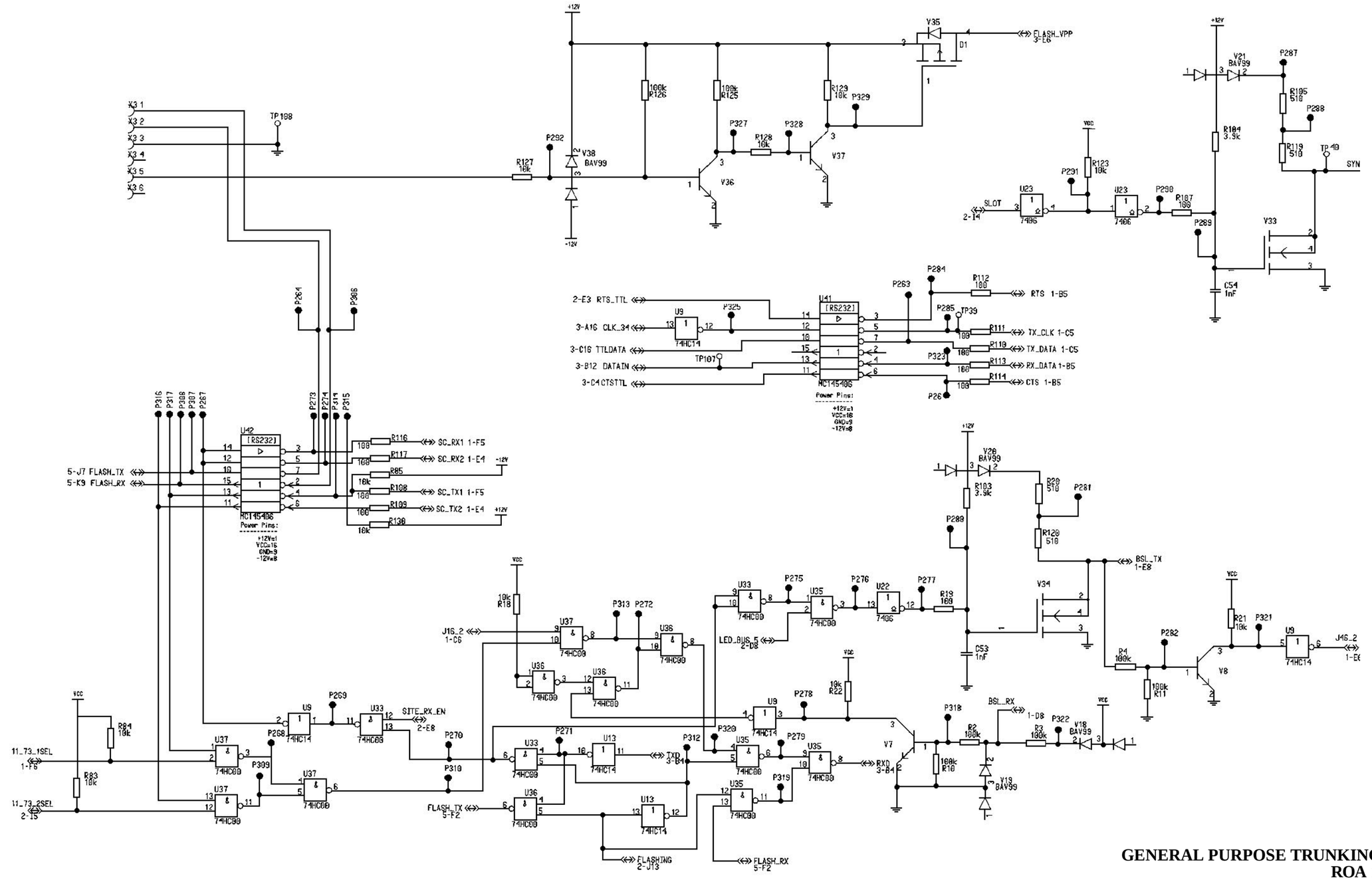
GENERAL PURPOSE TRUNKING CARD
ROA 117 2240

(1911-ROA 117 2240, Sh. 3, Rev. C)



GENERAL PURPOSE TRUNKING CARD
ROA 117 2240

(1911-ROA 117 2240, Sh. 4, Rev. C)



GENERAL PURPOSE TRUNKING CARD
ROA 117 2240

(1911-ROA 117 2240, Sh. 5, Rev. C)

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AE/LZB 119 1886 R1A
Printed in U.S.A.