MAINTENANCE MANUAL

EDACS® VERTICAL SIMULCAST INTERFACE CARD ROA 117 2235

TABLE OF CONTENTS

ERICSSON

SPECIFICATIONS*

ITEM	SPECIFICATION
POWER REQUIREMENTS	+5 Vdc ±5%, 150 mA (maximum). +12 Vdc ±5%, 80 mA (maximum). -12 Vdc ±5%, 20 mA (maximum).
CONNECTIONS	96 pin DIN connector (P1) mating to VME backplane interface.
DIGITAL DATA TYPE	TTL, RS-232 & RS422.
ANALOG/AUDIO TYPE	Voice Grade Audio Circuits (equal to 3002).
DIMENSIONS	100 mm (high) x 220 mm (long).

* These specifications are intended for use during servicing. Refer to appropriate Specification Sheet for the complete specification.

INTRODUCTION

The Vertical Simulcast Interface Card (ROA 117 2235) is used in the EDACS Simulcast System to provide signal level conversion and clock synchronization for those signals whose source or destination is the Control Point Trunking Card.

The Interface Card is manufactured using surface mount components. The card plugs into a Trunking Shelf along with the Control Point Trunking Card and the Vertical Turbo Card. Electrical connections are made by plugging the Interface Card into the proper card slot which connects P1 into the shelf's backplane.

The Simulcast Interface Card buffers signals between the Trunking Card and the rest of the simulcast modules. The buffered signals include the following:

- 9600 Hz data clock (in and out)
- 9600 baud data (in and out)
- 150 baud data (in and out)
- Modem handshaking lines
- Audio/digital path select line (in and out)
- Push-to-talk line (in and out)

- A/D lines (in and out).
- VDI data (in and out)

The Simulcast Interface Card uses the 9600 Hz reference clock generated by the Data Selector 2 Module to phase lock the 11.0592 MHz clock that is used to drive the Trunking Card. This provides the stable and synchronized clock source for the system at the Control Point.

CIRCUIT AND FUNCTIONAL DESCRIPTION

The Simulcast Interface Card provides signal, data, and clock level conversion (TTL to RS-232C and RS-232C to TTL), data and clock lines, and a Trunking Card clock that is phase locked to the reference clock.

The Simulcast Interface Card converts RS-232C level signals from the backplane of the simulcast system to TTL signals for the Trunking Card. It also converts TTL signals from the Trunking Card to RS-232C for the backplane for intersite use.

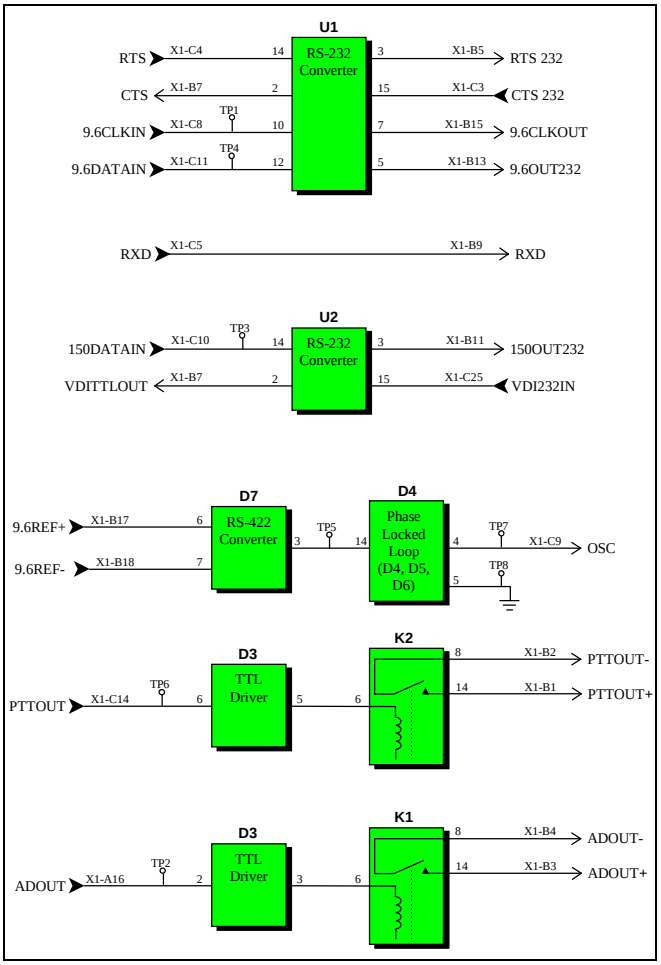


Figure 1 -Simulcast Interface Card Block Diagram

The Simulcast Interface Card generates a synchronized 11.0592 MHz clock from a reference 9600 Hz clock. This is accomplished using a Phase-Locked Loop (PLL) and a voltage controlled oscillator with a divide-by N prescaler.

Two relays are used on the Simulcast Interface Card. One relay provides a contact closure based on the Trunking Card PTT output. The other relay provides a contact closure based on the Trunking Card A/D (audio and low speed data/high speed) control line.

A block diagram of the Simulcast Interface Card is shown in Figure 1.

There is only one connector used to connect the Simulcast Interface Card to components of the Simulcast System, X1. Connector X1 provides the interface with the backplane which distributes the signals according the system interconnect plan. A description of the various signals, data and clocks used between the Trunking Card and the Interface Card is summarized in Table 2.

SIGNAL FLOW

9.6REF+ (X1-B17), 9.6REF- (X1-B18)

A 9600 Hz reference clock at RS-422 level is applied to the Interface Card at X1-B17 and X1-B18. This signal is converted to TTL by Differential bus transceiver D7. The TTL output (D7-1) can be monitored at TP5 (9.6REF) before it is applied to the PLL at D4-14.

11.0592MHz Clock (X1-C9)

The 11.0592MHz Clock is generated on the Interface Card by the Phase Locked Loop circuit. The circuit uses the 9600 Hz reference (9.6REF)for system stability. The 11.0592MHz Clock is then output to the backplane as OSC (X1-C9) for use by other system components.

9.6CLKIN (X1-C8), 9.6CLKOUT (X1-B15)

The 9.6CLKIN is a 9600 Hz square wave output from the Trunking Card. The clock is derived from the RF modem on the Trunking Card. The 9.6CLKIN (TP1, 9.6 CLK) is converted from TTL (U1-10) to RS-232C (U1-7) and sent to the backplane, as 9.6CLKOUT (X1-B15).

9.6DATAIN (X1-C11), 9.6OUT232 (X1-B13)

The 9.6DATAIN is a 9600 bps data stream output from the Trunking Card. This data is derived from the RF modem on the Trunking Card. The 9.6DATAIN (TP4, 9.6DAT) is

converted from TTL (U1-12) to RS-232C (U1-5) and sent to the backplane as 9.6OUT232 (X1-B13).

150DATAIN (X1-C10), 150OUTB232 (X1-B11)

The 150DATAIN is a 150 bps data stream output from the Trunking Card. This data is derived from a WALSH BIT generator on the Trunking Card. The 150DATAIN (TP3, 150DAT) is converted from TTL (U2-14) to RS-232C (U2-3) and sent to the backplane as 150OUT232 (X1-B11).

RXD (X1-C5), RXD (X1-B9)

RXD data is a 9600 bps data stream input to the Trunking Card. This data is derived from the backplane data line. The RXD is routed through the Interface Card without conditioning to the backplane as RXD (X1-B9).

PTTOUT (X1-C14), PTTOUT + (X1-B1), PTTOUT - (X1-B2)

PTTOUT comes from the Trunking Card. The microcomputer produces the delayed PTT output. The PTTOUT (TP6, PTT) is input to a peripheral relay driver (D3-6) which drives relay K2 (K2-6). K2 provides a contact closure and connects PTTOUT + (K2-14) to PTTOUT - (K2-8). These two signals are sent to the backplane as PTTOUT+ (X1-B1) and PTTOUT - (X1-B2).

A/DOUT (X1-A16), A/DOUT + (J2-13), A/DOUT- (J2-14)

A/DOUT is output from the Trunking Card to produce the modulation path control to select the audio and low speed data or the high speed data path. The A/DOUT is input to a peripheral relay driver (D3-1) which drives relay K3. Relay K3 provides a contact closure and connects A/DOUT + (K3-14) to A/DOUT- (K3-8). These two signals are sent to the backplane as A/DOUT + (X1-B3) and A/DOUT-(X1-B4).

RTS (X1-C4), RTS232 (X1-B5)

The request To Send (RTS) signal (X1-C4) is a handshake signal coming from the Trunking Card. This signal, RTS, is converted from TTL to RS-232C and sent to the backplane as RTS232 (X1-B5). RTS232 is also re-routed from backplane connector J14 to J15 to provide CTS232.

CTS (X1-C3), CTS232 (X1-B7)

The signal, Clear To Send (CTS), is a handshake signal input to the Trunking Card. This signal is derived from one of two external sources. The first is the line CTS232 from the transmit cross connect panel. The second source is the signal RTS232 which is routed back on the CTS232 line.

VDI232IN (X1-C25), VDITTLOUT (X1-C24)

The Voted Digital Interconnect (VDI) signal at RS-232 level is input from the backplane (X1-C25). This VDI signal, VDI232IN is converted from RS-232 (U2-4) to TTL (U2-13) and sent to the backplane, as VDITTLOUT (X1-C24).

POWER DISTRIBUTION AND FILTERING

The DC voltages used by the Simulcast Interface Card are received by the Backplane, ROA 117 2256 from the Power Distribution Panel. The fused power includes +5 Vdc, +12 Vdc, -12 Vdc and GND (0 volts or logic ground).

On the Interface Card each voltage line passes through a thermistor which will open if too much current is drawn by the circuitry.

The +12 Vdc and -12 Vdc supplies power the TTL to RS-232C level translators. The +5 Vdc is used to power the remaining circuits on the Simulcast Interface Card. All power lines have by-pass capacitors at each IC to filter out any power noise transients or spikes.

PHASE LOCKED 11.0592 MHZ CLOCK

The Interface Card generates an 11.0592 MHz clock from a reference 9600 Hz clock. This is accomplished by the digital Phase-Lock-Loop (PLL) and voltage controlled oscillator, D4. A divide by N prescaler consisting of 8 bit counters, D5 and D6, along with the synchronizing register, U4, perform the proper divide down (÷1152) of the 11.0592 MHz generated clock to compare against the 9600 Hz reference clock.

The reference clock, 9.6REF, is converted from RS-422 to TTL by the differential transceiver D7. Resistor R8 and capacitor C1 provide filtering and delay of the reference TTL clock for input to the PLL and VCO, D4. The other compare input to the PLL and VCO is the output of synchronizing register, U4. The PLL and VCO, D4, is a self contained digital phase-lock-loop and voltage controlled oscillator. Resistor R1 and capacitor C3 set up the free running frequency of the voltage controlled oscillator. Resistors R12, R17, R18, R19, R20 and capacitors C4 and C5 comprise the loop filter of the PLL which sets up the capture range (frequency lock range).

The generated 11.0592 MHz clock (TP7) is input to 8-bit counters, D5 and D6, along with the synchronizing register, U4. The counters are asynchronously reloaded via the active low output of register U4.

MAINTENANCE

CONNECTOR PIN DEFINITIONS

Only one connector (J1) is used to provide the interface connections for the Simulcast Interface Card. The following tables identify each pin used and provides such information as the signal name, whether or not it is an input or output signal, analog or digital signal, and the signal level (TTL, RS-232, or RS-422).

TEST AND SERVICE

The following equipment is necessary to test the GETC interface module:

1. Tektronix 2430A Digital Storage Scope or equivalent

2. HP 8116 Pulse/function Generator or equivalent

3. Triplett model 630-PL Type 5 or equivalent

4. Test Cables as required

The following steps are necessary to test the Simulcast Interface Card as part of the Simulcast System.

1. Install the Simulcast Interface Card in the Trunking Shelf assembly of the Simulcast System.

2. Verify that the +5, +12, and -12 Vdc source voltages are within the tolerances specified.

3. Verify correct operation of the PLL and VCO. Verify the 9.6 REF (TP5) channel bank clock and the 11.0592 MHz clock (TP7).

4. Verify the presence of 9.6CLKIN (TP1) and 9.6DATAIN (TP4) from the Trunking Card.

5. Verify the presence of 150DATAIN (TP3) from the Trunking Card.

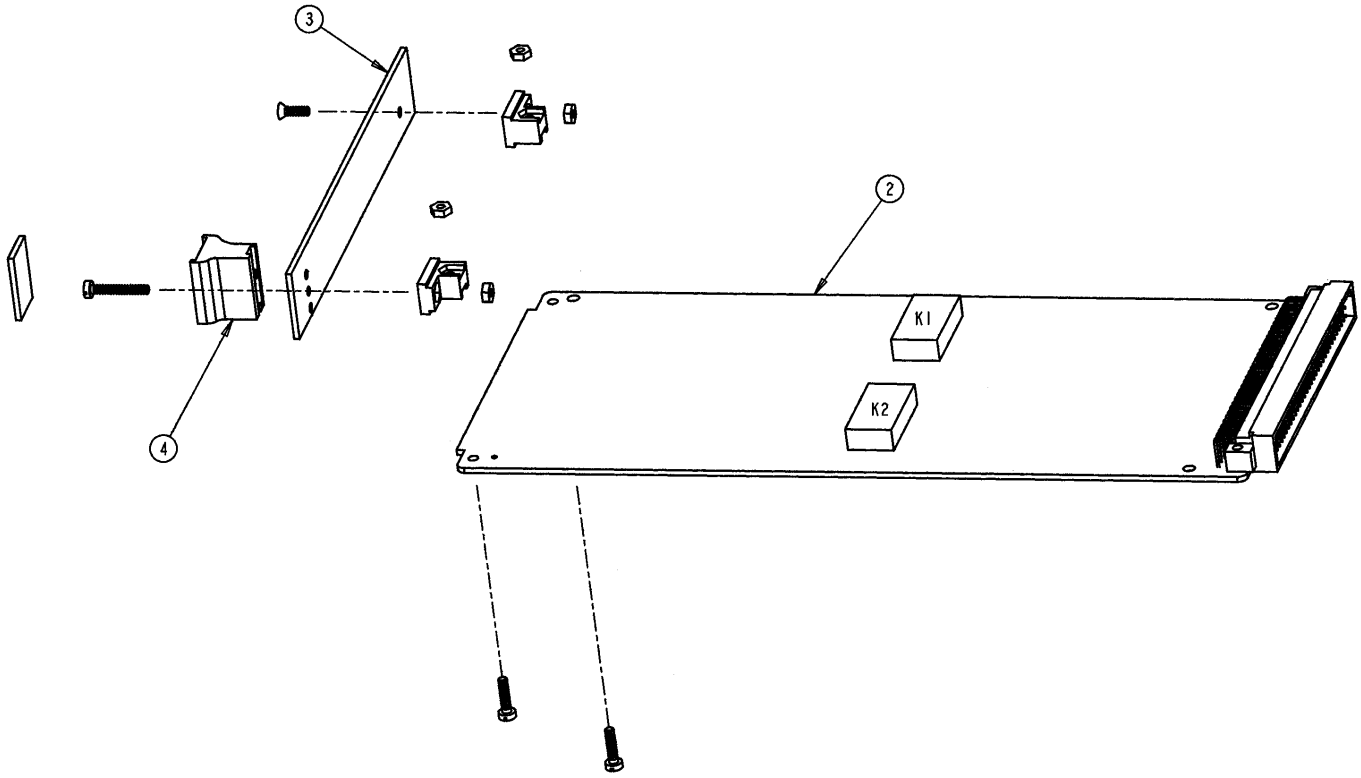
6. If the modem control lines, TXD, CTS, and RTS are used, verify the presence of activity on these lines.

7. To check low speed data and high speed data control lines, verify activity on A/DOUT (TP2) and contact closure to ground on A/DOUT +.

8. To check transmit control functions, verify activity on PTTOUT (TP6) and contact closure to ground on PTTOUT +.

Table 1 - P1 Connector Definition

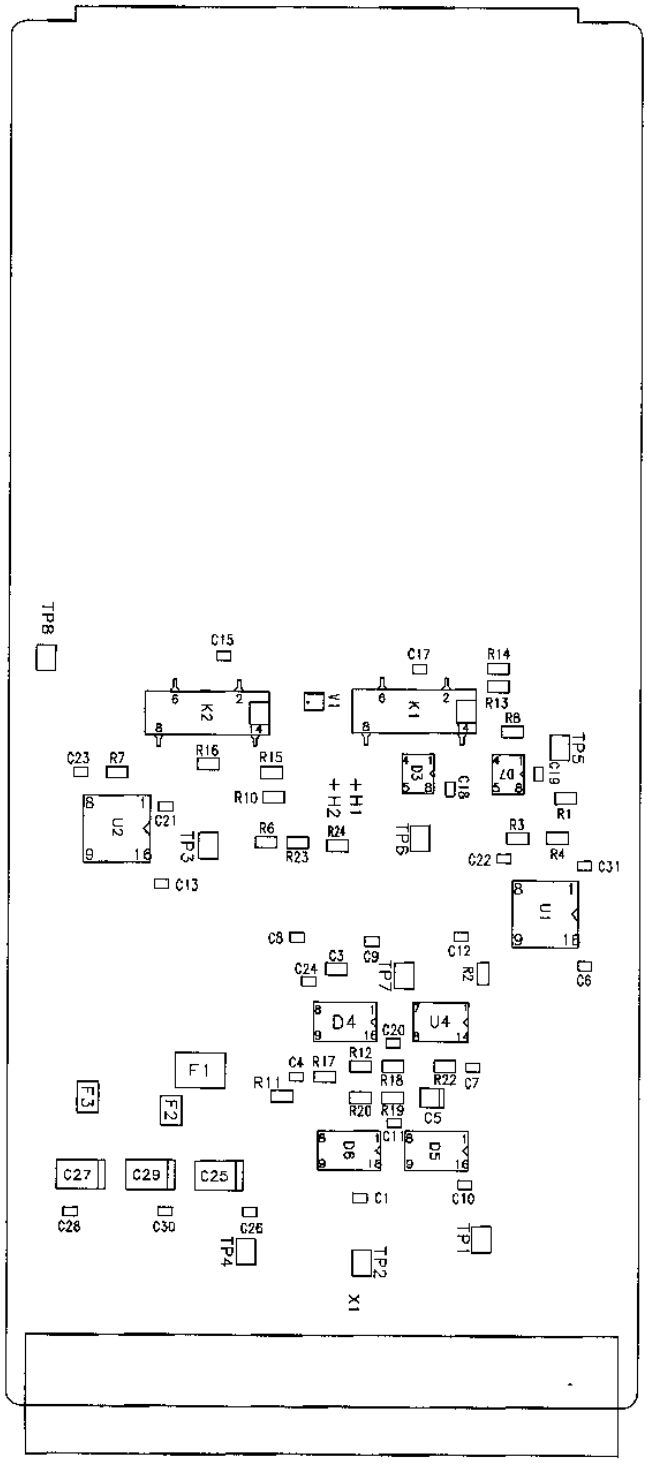
CONNECTOR PIN	SIGNAL NAME	INPUT/ OUTPUT	DIGITAL CLOCK (C) or DATA (D)	LEVEL
X1-A1	GND	I/O	D	0 V
X1-A16	A/DOUT	I	D	TTL
X1-A26	GND	I/O	D	0 V
X1-A30	+5	I		5 Vdc
X1-A31	+5	I		5 Vdc
X1-A32	GND	I		0 V
X1-B1	PTTOUT+	O	D	0,FLOAT
X1-B2	PTTOUT-	O	D	0 V
X1-B3	A/DOUT+	O	D	0 V,FLOAT
X1-B4	A/DOUT-	O	D	0 V
X1-B5	RTS232+	O		RS-232C
X1-B6	GND	I/O	D	0 V
X1-B7	CTS232+	I		RS-232C
X1-B8	GND	I/O	D	0 V
X1-B9	RXD	O	D	TTL
X1-B10	GND	I/O	D	0 V
X1-B11	150OUT232+	O	D (150 bps)	RS-232C
X1-B12	GND	I/O	D	0 V
X1-B13	9.6OUT232+	O	D (9600 bps)	RS-232C
X1-B14	GND	I/O	D	0 V
X1-B15	9.6CLKOUT+	O	D (9600 bps)	RS-232C
X1-B16	GND	I/O	D	0 V
X1-B17	9.6REF+	I	C (9600 Hz)	RS-422
X1-B18	9.6REF-	I	C (9600 Hz)	RS-422
X1-B30	+5	I		5 Vdc
X1-B30	+5	I		5 Vdc
X1-B32	GND	I		0 V
X1-C1	GND	I/O	D	0 V
X1-C3	CTS	O	D	TTL
X1-C4	RTS	I	D	TTL
X1-C5	RXD	I	D	TTL
X1-C8	9.6CLKIN		C (9600 Hz)	TTL
X1-C9	OSC	O	C (11.0592 Mhz)	TTL
X1-C10	150DATAIN	I	D (150 bps)	TTL
X1-C11	9.6DATAIN	I	D (9600 bps)	TTL
X1-C14	PTTOUT	I	D	TTL
X1-C24	VDITTLOUT	O	D	TTL
X1-C25	VDI232IN	I	D	RS-232C
X1-C30	-12V	I		-12 Vdc
X1-C31	+12V	I		+12 Vdc
X1-C32	GND			0 V



SIMULCAST INTERFACE CARD

ROA 117 2235

(1/1078 ROA 117 2235, Sh. 1, Rev. A)



SIMULCAST INTERFACE CARD

ROA 117 2235

(1078-ROA 117 2235, Sh. 1, Rev. B)

SIMULCAST INTERFACE CARD
131-32 ROA 117 2235
Revision: F

SYMBOL	PART NUMBER	DESCRIPTION
		---------- CAPACITOR ----------
C1	RJC 463 4043/1	100pF 0805 50V ±5%
C3	RJC 463 4062/82	82pF 1206 50V ±5%
C4	RJC 464 3045/47	47nF 0805 50V -10%
C5	RJE 584 3357/1	Tantalum, 1 µF 35 V, B-Case, SMD.
C6	RJC 464 3045/1	10nF 0805 50V -10%
C7	RJC 464 3045/1	10nF 0805 50V -10%
C8	RJC 464 3045/1	10nF 0805 50V -10%
C9	RJC 464 3045/1	10nF 0805 50V -10%
C10	RJC 464 3045/1	10nF 0805 50V -10%
C11	RJC 464 3045/1	10nF 0805 50V -10%
C12	RJC 464 3045/1	10nF 0805 50V -10%
C13	RJC 464 3045/1	10nF 0805 50V -10%
C15	RJC 464 3045/1	10nF 0805 50V -10%
C17	RJC 464 3045/1	10nF 0805 50V -10%
C18	RJC 464 3045/1	10nF 0805 50V -10%
C19	RJC 464 3045/1	10nF 0805 50V -10%
C20	RJC 464 3045/1	10nF 0805 50V -10%
C21	RJC 464 3045/1	10nF 0805 50V -10%
C22	RJC 464 3045/1	10nF 0805 50V -10%
C23	RJC 464 3045/1	10nF 0805 50V -10%
C24	RJC 464 3045/1	10nF 0805 50V -10%
C25	RJE 572 1638/47	Tantalum, electrolytic: 4.7 µF, ±20%, 10V.
C26	RJC 464 2046/1	100nF 0805 ±5%
C27	RJE 572 1638/47	Tantalum, electrolytic: 4.7 µF, ±20%, 10V.
C28	RJC 464 2046/1	100nF 0805 ±5%
C29	RJE 572 1638/47	Tantalum, electrolytic: 4.7 µF, ±20%, 10V.
C30	RJC 464 2046/1	100nF 0805 ±5%
C31	RJC 464 3045/1	10nF 0805 50V -10%
		------ INTEGRATED CIRCUITS --------
D3	RYT 109 6064/C	Digital: Dual Peripheral Driver; sim to 75451B.
D4	RYT 306 6057/C	Phase Lock Loop with VCO; sim to 74HC4046.
D5	RYT 222 6014/C	Digital: 8-Bit Binary Counter; sim to 74LS592.
D6	RYT 222 6014/C	Digital: 8-Bit Binary Counter; sim to 74LS592.
D7	RYT 109 6043/1C	Differential Bus Driver; sim to SN75176BD.
		---------- THERMISTORS ----------
F1	REZ 701 16/2	0.5A 60V PTC.
F2	REZ 701 28/1	0.5A 15V PTC.
F3	REZ 701 28/1	0.5A 15V PTC.
		---------- RELAYS ----------
K1	RAV 947 27/1	Reed Relay SMD 1-Pole.
K2	RAV 947 27/1	Reed Relay SMD 1-Pole.
		---------- RESISTORS ----------
R1	REP 625 423/1	100 Ohm, 1206 Chip, 5% 1/8w.
R2	REP 625 423/1	100 Ohm, 1206 Chip, 5% 1/8w.
R3	REP 625 423/1	100 Ohm, 1206 Chip, 5% 1/8w.
R4	REP 625 423/1	100 Ohm, 1206 Chip, 5% 1/8w.
R6	REP 645 62	0 Ohm 1206 0.15w.
R7	REP 625 423/1	100 Ohm, 1206 Chip, 5% 1/8w.
R8	REP 625 425/1	10K Ohm, 1206 Chip, 5% 1/8w.
R10	REP 625 425/1	10K Ohm, 1206 Chip, 5% 1/8w.
R11	REP 615 624/301	3.01K Ohm, ±1%, ±100PPM.
R12	REP 645 626/47	470K Ohm 1% 1206 0.15w.
R13	REP 645 622/47	47 Ohm 1% 1206 0.15w.
R14	REP 645 622/47	47 Ohm 1% 1206 0.15w.
R15	REP 645 622/47	47 Ohm 1% 1206 0.15w.
R16	REP 645 622/47	47 Ohm 1% 1206 0.15w.
R17	REP 625 425/33	33K Ohm, 1206 Chip, 5% 1/8w.
R18	REP 625 427/1	1 Meg Ohm,1206 CHIP, 5% 1/8w.
R19	REP 625 425/1	10K Ohm, 1206 Chip, 5% 1/8w.
R20	REP 625 427/1	1 Meg Ohm,1206 CHIP, 5% 1/8w.
R22	REP 645 624/33	3.3K Ohm 1% 1206 0.15w.
R23	REP 645 62	0 Ohm, 1206, 0.15w.
R24	REP 625 425/1	10K Ohm, 1206 Chip, 5% 1/8w.
		---------- TEST POINTS ----------
TP1	RPV 403 813/01	Connector, test.
TP2	RPV 403 813/01	Connector, test.
TP3	RPV 403 813/01	Connector, test.
TP4	RPV 403 813/01	Connector, test.
TP5	RPV 403 813/01	Connector, test.
TP6	RPV 403 813/01	Connector, test.
TP7	RPV 403 813/01	Connector, test.
TP8	RPV 403 813/01	Connector, test.
		------- INTEGRATED CIRCUITS --------
U1	RYT 109 6073/1	EIA232-D and CCITT V.28 Driver/Receiver; sim to MC145406.
U2	RYT 109 6073/1	EIA232-D and CCITT V.28 Driver/Receiver; sim to MC145406.
U4	RYT 306 2003/C	Digital: Dual Data Flip-Flop; sim to 74HC74.
		---------- DIODE ----------
V1	RKZ 123 03/3	Dual switching, common cathode; sim to BAV70.

		---------- CONNECTOR ----------
X1	RPV 403 209/102	96 Pole, 4 Ground pins.
		---------- MISCELLANEOUS ----------
2	TVA 117 2218 R2	Printed Wiring Board.
3	SXA 120 4174/8	Simulcast Interface Front Panel.
4	NTM 201 1079	Hardware Kit.

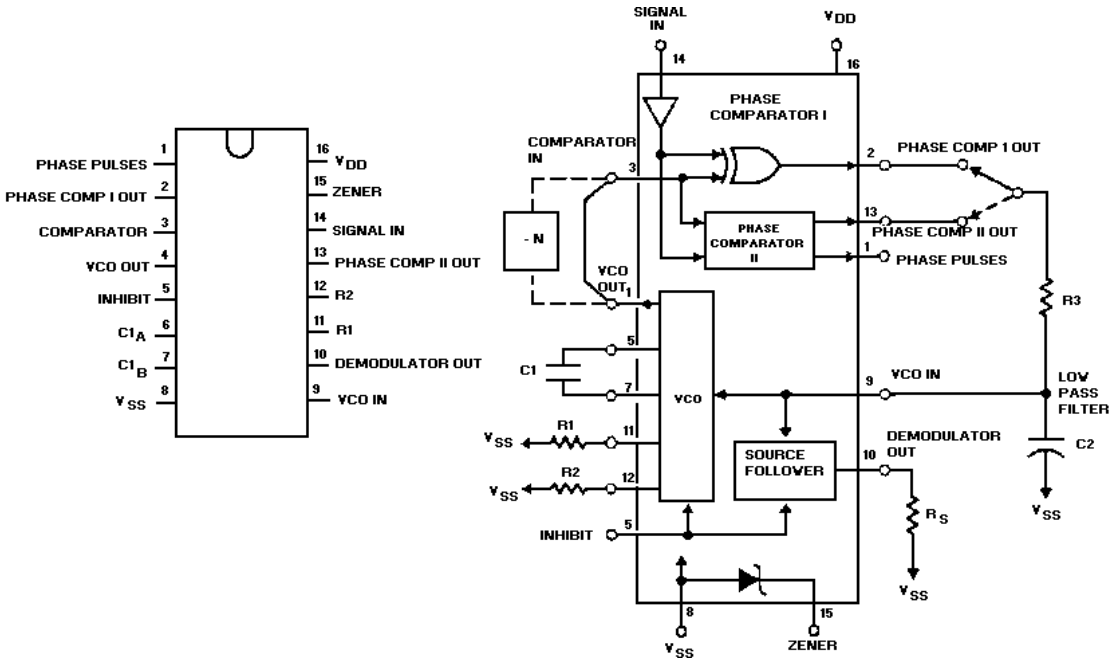
PRODUCTION CHANGES

Changes in the equipment to improve performance or simplify circuits are identified by a "Revision Letter," which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the parts list for the descriptions of the parts affected by these revisions.

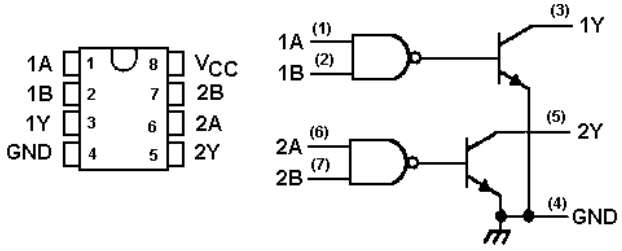
Rev. R2A - **SIMULCAST INTERFACE CARD ROA 117 2235**

Changes revision level of printed wiring board (item 2, TVK 117 2218) from R1 to R2. Rev. R1 and R2 PWBs are functionally equivalent. R2 adds silkscreening for D1, D2, D3, and U4, and adds U4 to parts list.

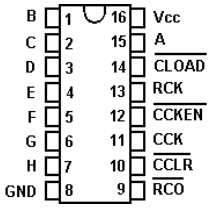
D3 - PHASE LOCKED LOOP
RYT 306 6057/C (74HC4046)



D3 - DUAL PERIPHERAL DRIVER
RYT 109 6064/C (75451B)



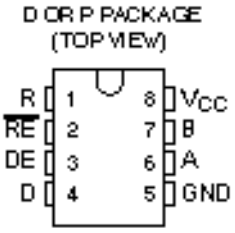
D5 & D6 - 8 BIT BINARY COUNTER
RYT 222 6014/C (74LS592)



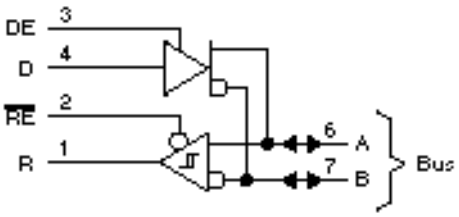
COUNTER CLOCK ENABLE CONTROL

CCKEN	$\overline{CCKEN}$	EFFECT ON CCK
L	L	ENABLE
L	H	DISABLE
H	L	ENABLE
H	H	ENABLE

D7 - DIFFERENTIAL BUS DRIVER
RYT 109 6043/1C (SN75176BD)

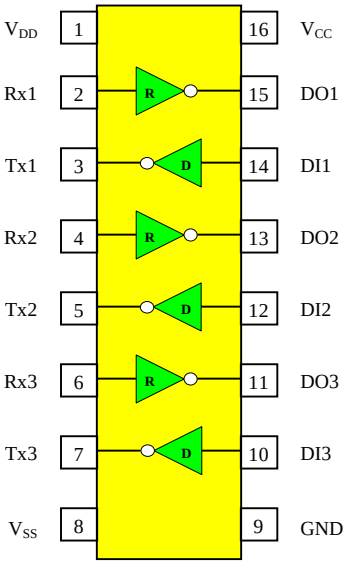


logic diagram (positive logic)

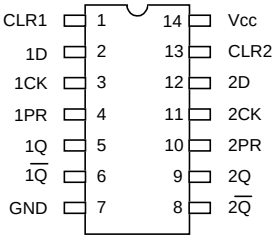


U1 & U2 - RECEIVER/DRIVER
RYT 109 6073/1 (MC 145406)

D = Driver
R = Receiver
DI = Data In
DO = Data Out



U4 - CMOS DUAL FLIP-FLOP
RYT 306 2003/C (74HC74)



FUNCTION TABLE

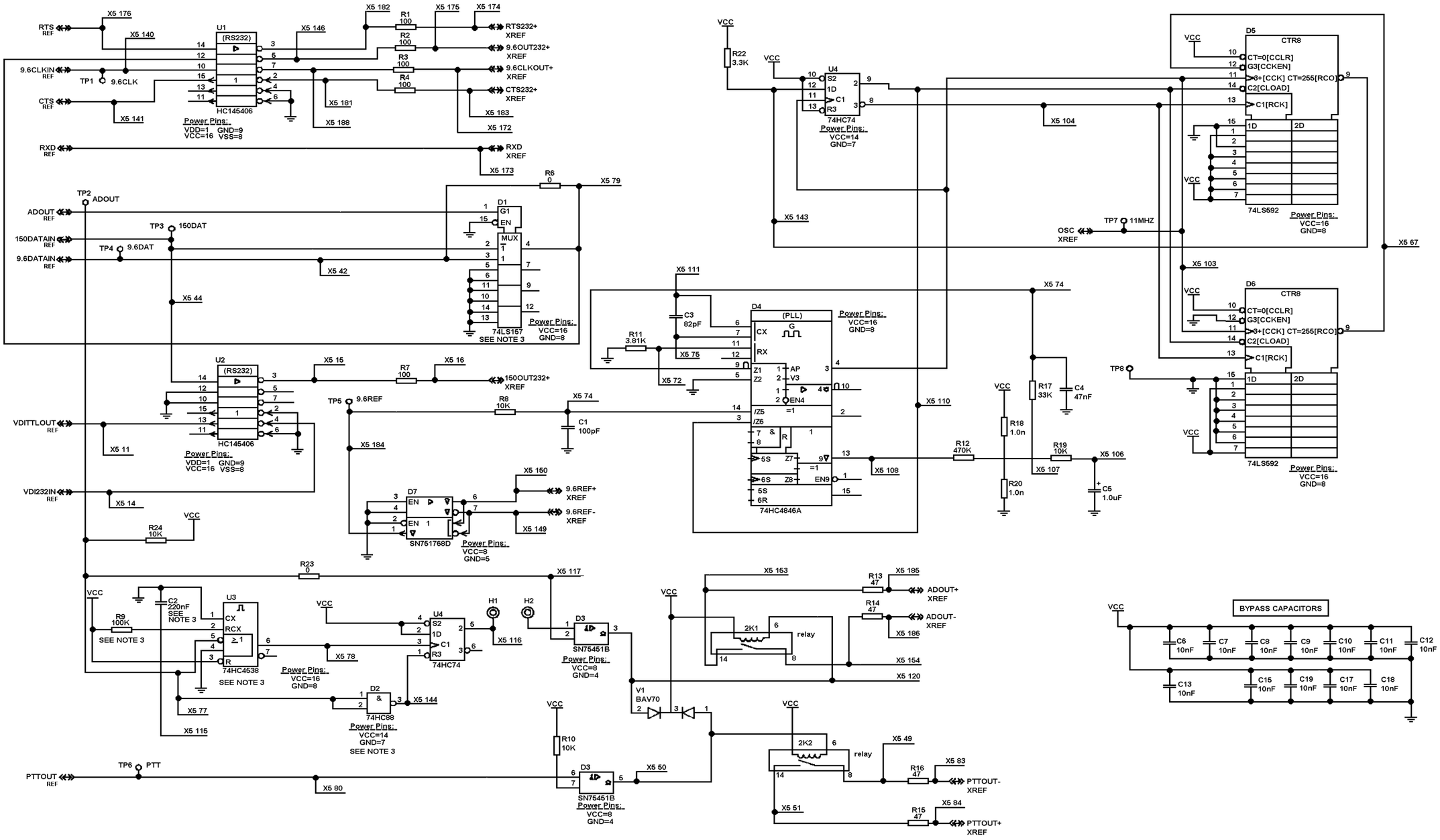
INPUTS				OUTPUTS	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	H	L	X	H*	H*
H	L	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

X = Any input, including transistion

↑ = from L to H

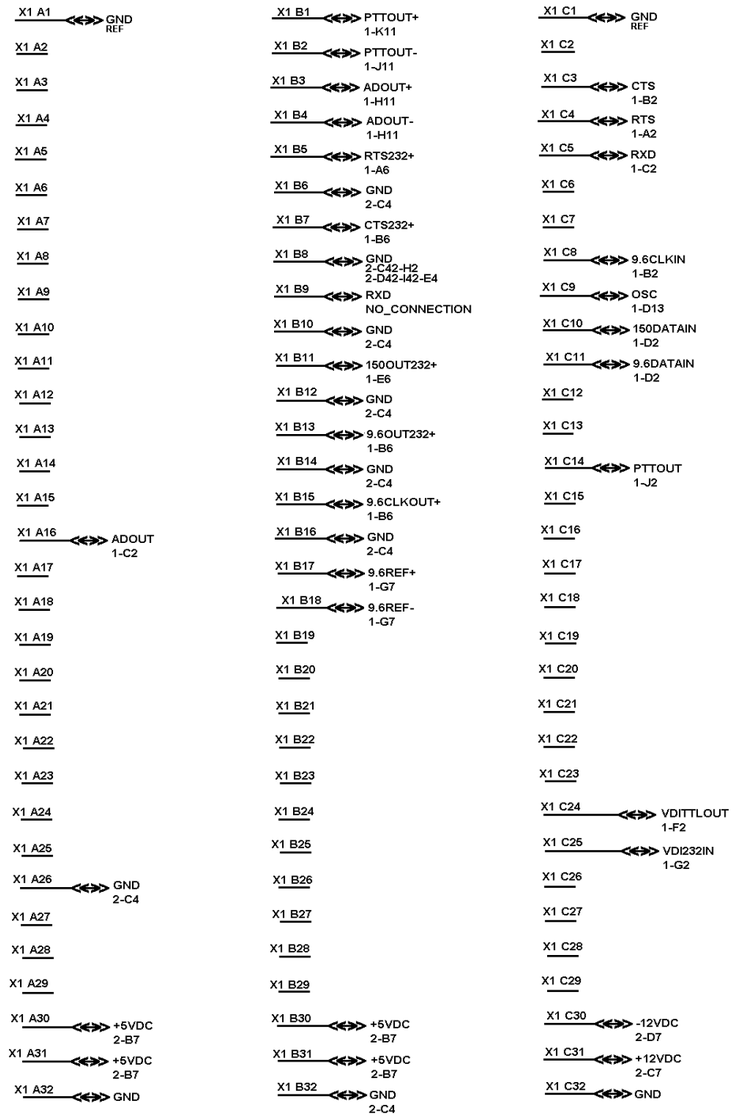
Q_0 = The level of Q after the previous clock pulse

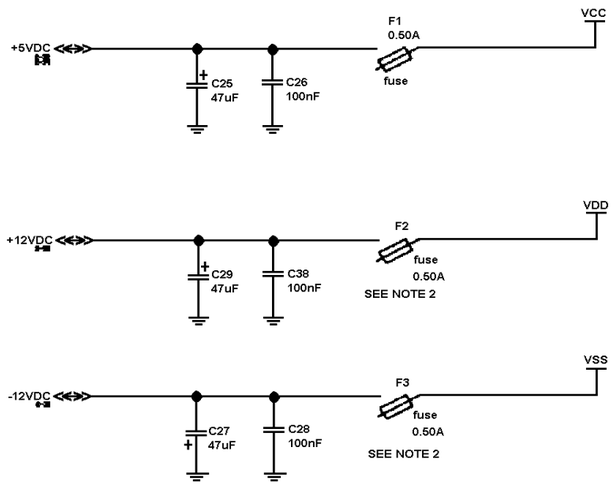
* = Nonstable; don't persist when PR and CLR are set high



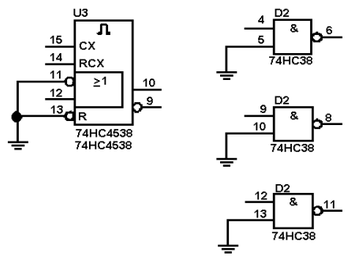
SIMULCAST INTERFACE CARD
ROA 117 2235

(1911-ROA 117 2235, Sh. 1, Rev. B)



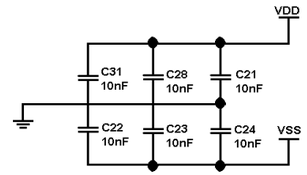


UNUSED GATES

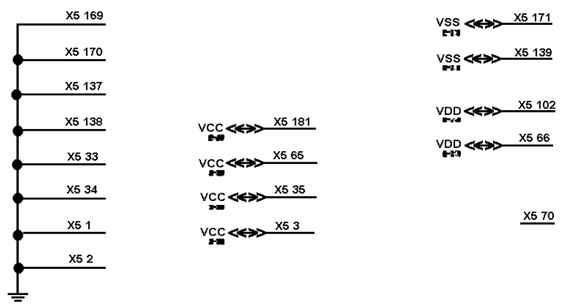


POWER AND GROUND CONNECTIONS				
DEVICE	GND PIN NO.	+5V PIN NO.	+12V PIN NO.	-12V PIN NO.
U1,U2	9	16	1	8
U3	8	16		
U4	7	14		
D2	7	14		
D1	8	16		
D4	8	16		
D3	4	8		
D6,D6	8	16		
D5	5	8		

BYPASS CAPACITORS



NOTES: 1 X5 DENOTES TEST PROBE POINTS ON REAR OF BOARD.
2 F2 AND F3 ARE MINI SMD.
3 THE FOLLOWING COMPONENTS ARE NOT PLACED:
D1, D2, C2, R9 AND U3.



SIMULCAST INTERFACE CARD
ROA 117 2235

(1911-ROA 117 2235, Sh. 2, Rev. B)

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