MOBILE RADIO

MASTR® Executive II MAINTENANCE MANUAL

PRIORITY SEARCH-LOCK MONITOR 19C321727G1 (OPTION 9922)

Maintenance Manual LBI30244C
DATAFILE FOLDER - DF8410

MASTR EXECUTIVE II STATION PSLM

SPECIFICATIONS *

Search Rate (Each Channel)	Four times per second
Sample Time (Each Channel)	125 milliseconds
Priority Channel Search Rate	Four times per second, 225-275 milliseconds apart
Priority Channel Sample Time	6-7 milliseconds
Priority Squelch Sensitivity	20-dB quieting
Input Power	6 milliamperes @ +10 volts DC 86 milliamperes @ +13.8
Silicon Transistors	21
Integrated Circuit Modules	6
Light Emitting Diode	1
Temperature Range	-30°C to +70°C

*These specifications are intended primarily for the use of the serviceman. Refer to the appropriate Specification Sheet for the complete specifications.

GENERAL ELECTRIC

TABLE OF CONTENTS

SPECIFICATIONS	Cover
DESCRIPTION	1
CIRCUIT ANALYSIS	1
Master Pulse Generator	1
Modes of Operation	1
Receiver Squelched	1
Receiving Priority	2
Receiving Non Priority	3
Priority Disable	4
Voltage Regulator	4
Transmit Revert Mode	4
MAINTENANCE	4
SYSTEM MODIFICATION	5
PRIORITY SQUELCH ADJUSTMENT	5
INSTALLATION INSTRUCTIONS	7
OUTLINE DIAGRAM	8
SCHEMATIC DIAGRAM	9
PARTS LIST	10

WARNING

Under no circumstances should any person be permitted to handle any portion of the equipment that is supplied with high voltage, or to connect any external apparatus to the units while the units are supplied with power. KEEP AWAY FROM LIVE CIRCUITS.

DESCRIPTION

The General Electric MASTR® Executive II Station Priority Search-Lock Monitor provides two out of eight channel monitoring by alternately searching a priority channel and a non-priority channel. The Priority Search-Lock Monitor (PSLM) assures reception of all signals received on the priority channel regardless of signal strength or which channel receives the first signal.

When a signal is received on the priority channel, the PSLM stops searching and locks on the priority channel for the duration of the message. When a signal is first received on the non-priority channel, the PSLM stops on that channel while monitoring the priority channel. If a signal is received on the priority channel while the PSLM is stopped on the non-priority channel, the PSLM reverts to the priority channel and locks on that channel for the duration of the message.

NOTE

The PSLM will operate only when the PSLM switch is on and the receiver is squelched.

The priority channel is locked on the channel by simply changing a connection on the PSLM board. Instructions for making this change are contained in Notes 1 & 2 on the Schematic Diagram (see Table of Contents.

In applications where a priority channel is not desired, the priority feature may be disabled by removing C3 and making connections as described in Note 3 on the schematic diagram. With this change the PSLM will alternately search both channels and will lock on the channel receiving the first signal.

NOTE

The PSLM is normally strapped for F1 priority. To change or disable the priority function, refer to notes 1, 2 and 3 on the Schematic Diagram for the PSLM.

CIRCUIT ANALYSIS

The Priority Search-Lock Monitor is fully transistorized, using both discrete components and Integrated circuit modules (IC's) to achieve maximum reliability.

References to symbol numbers mentioned in the following text may be found on the Outline Diagram, Schematic Diagram and Parts List (see Table of Contents).

Two input supply voltages are provided for the PSLM. The 10 Volts Regulated supplies voltage for Noise/Audio circuits. The 13.8V input supply voltage for the PSLM is provided through the Search ON/OFF switch (S-2401). This 13.8 Volts provides the input voltage for the 5-Volt Regulator (VR1) which supplies voltage for the other circuits on the PSLM board. The search switch also supplies the base bias voltage to turn on switch (Q16) which grounds the base of the Wiper Switch (Q15) keeping it off. Thus keeping the wiper lead of Frequency Switch S701/S702 above ground allowing the PSLM to search. Refer to the Block Diagram of the PSLM in Figure 4.

MASTR PULSE GENERATOR

The heart of the PSLM is the MASTR Pulse Generator U1. The pulse generator produces negative going pulses at a rate of 16 pulses per second or 67.5 milliseconds (Ms) apart. The 67.5 Ms pulse drives the "divide by two" Flip-Flop U2A which provides a 125 Ms square wave output to the other "divide by two" Flip-Flop U2B which produces a 250 Ms square wave. The 125 Ms square wave is used to drive clock gate U3B and the 250 Ms square wave is used to drive clock gate U3A which provides the timing pulses required for the different modes of operation. The PSLM sample rates and times discussed in the different modes of operation were selected to assure the reception of the first syllable of a message received on either channel and to assure full intelligibility of messages received on the non-priority channel.

MODES OF OPERATION

Operation of the PSLM can be divided into three different modes. The three modes are:

- Receiver Squelched
- Receiving priority channel
- Receiving non-priority channel

RECEIVER SQUELCHED

When the receiver is squelched (no signal applied), the PSLM alternately monitors each channel four times per second for a duration of 125 milliseconds. Associated timing wave forms for this mode of operation are shown in Figure 1.

NOTE

Logical "0" is less than +1.0 Volts. Logical "1" is greater than +2.5 Volts.

When the PSLM Search switch S2401 is turned on, 13.8 Volts is applied to the

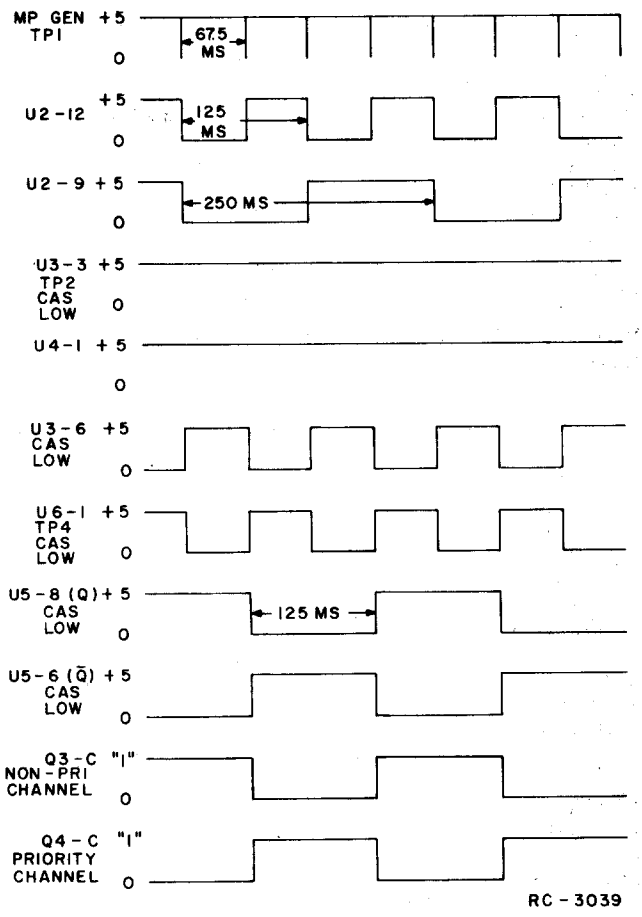


Figure 1 - Receiver Squelched Waveforms

5 Volt Regulator VR1 which starts the MASTR PULSE GENERATOR U1. The MASTR PULSE GENerator U1 applies sharp negative pulses at intervals of 67.5 milliseconds (Ms) to the "Divide by Two" Flip-Flop U2A Pin 1. The "Divide by Two" Flip-Flop U2A produces a 125 Ms square wave to U2B and to Pin 4 of GATE U3B. With the receiver squelched the CAS line is low (logical "0") which turns off Q2 providing a logical "1" at GATE U3B Pin 5. When both inputs of GATE U3B are at logical "1", the logical "0" output is inverted to a logical "1" by inverter U6A. This logical "1" is fed to clock (Pin 12) of Channel Flip-Flop U5. Thus the channel Flip-Flop is triggered or changes states every 125 milliseconds under the influence of "Divide by Two" Flip-Flop U2A. The two NOR GATES U6C and U6D are also alternately turned on by the channel FF as long as the Delayed Push-To-Talk (DPTT) lead is high (logical "1"). This keeps Q17 turned off, placing a low (logical "0") at the base of Q19 turning it off. With Q19 turned off, this places a high (logical "1") on the base of Q20 turning it on. With Q20 turned on, this places a low (logical "0") on Pins 9 & 12 of the NOR GATES U6C and U6D, enabling them. The two NOR GATES alternately turn on the Channel Drivers Q3 & Q4 which alternately put a ground (logical "0") on the receiver oscillators. The PSLM will continue switching until a signal unsquelches the receiver or until the transmitter is keyed.

The high (logical "1") at Pin 5 of GATE U3B is also applied to the base of Light Inhibit Q6 turning it on. With Q6 conducting this grounds the base of the Light Driver Q5 keeping it turned off. The Channel Busy Indicator CR2407 is biased off during this mode of operation.

RECEIVING PRIORITY CHANNEL

When a signal is received on the priority channel, the PSLM locks on that channel for the duration of the message. Timing waveforms for this mode of operation are shown in Figure 2.

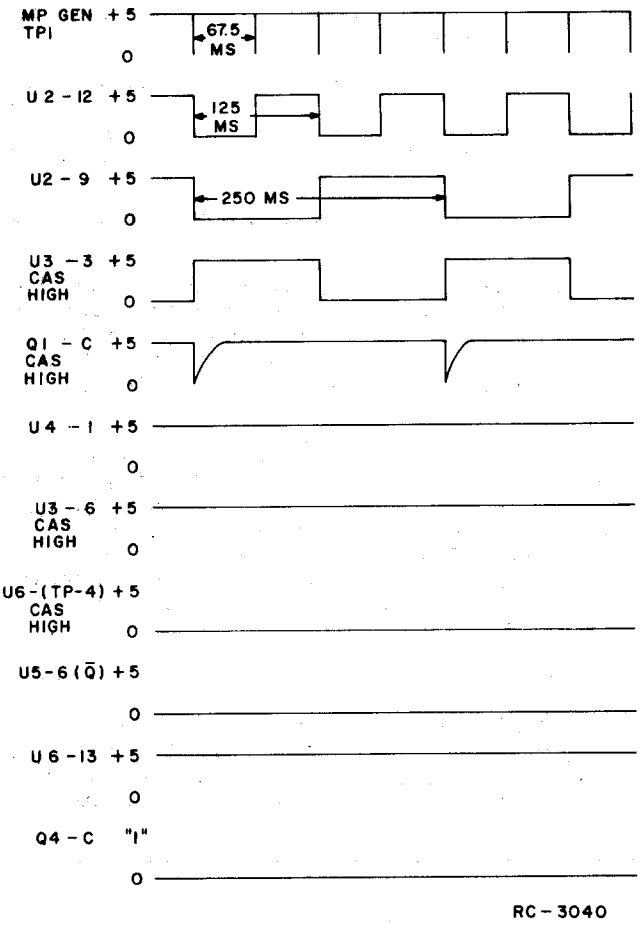


Figure 2 - Receiving Priority Channel Waveforms

Assume that F1 is the priority channel. Receiving a signal on the F1 channel unsquelches the receiver and puts a high (logical "1") on the CAS lead which allows the CAS switch Q2 to conduct applying a logical "0" to GATE U3B turning it off. With GATE U3B off the 125 millisecond square

wave from the "Divide by Two" Flip-Flop U2A cannot trigger the Channel Flip-Flop U5 so the Channel Flip-Flop is locked providing a logical "0" to Pin 11 of NOR GATE U6D. Pin 12 of NOR GATE U6D is at logical "0". This produces a logical "1" to the base of the Priority Channel Driver Q4 turning it on to put a ground on the receiver oscillator F1.

The logical "0" at Pin 6 of FF U5 provides an input to Pin 5 of PRIORITY SAMPLE ONE-SHOT U4 providing a logical "1" on the output of Pin 1 or provides a logical "1" to Pin 13 of Channel FF U5 to insure that it stays locked up. With the Channel FF inhibited the PSLM remains locked on the F1 channel until the message is completed (receiver squelches).

The logical "0" at the collector of CAS switch Q2 turns off Light Inhibit Q6 allowing the logical "1" at Pin 13 of NOR GATE U6D to turn on Light Driver Q5. The Channel Busy Indicator CR2407 is turned on during this mode of operation.

RECEIVING NON-PRIORITY CHANNEL

When a signal is received on the non-priority channel, the PSLM stops on that channel while monitoring the priority channel four times per second for a duration of six milliseconds. If a signal is received on the priority channel while receiving the non-priority channel, the PSLM will revert from the non-priority channel and lock on the priority channel for the duration of the message. Timing waveforms for this mode of operation are shown in Figure 3.

Assume that F2 is the non-priority channel. Receiving a signal on the F2 channel unsquelches the receiver and puts a logical "1" on the CAS lead which allows CAS switch Q2 to conduct applying a logical "0" to GATE U3B turning it off. With GATE U3B off the channel FF U5 is stopped on the NON-PRIORITY CHANNEL providing a logical "0" to Pin 8 of NOR GATE U6C. Pin 9 of NOR GATE U6C is also at logical "0". This produces a logical "1" to the base of the NON-PRIORITY Channel Driver Q3 turning it on to put a ground to the receiver oscillator F2.

The MASTR Pulse Generator U1 drives "Divide by Two" FF U2A which in turn drives the other "Divide by Two" FF U2B with a 125 millisecond square wave producing a 250 millisecond square wave output to Pin 2 of GATE U3A. Pin 1 of GATE U3A is at logical "1" provided by Inverter U3D since CAS switch Q2 is conducting. The output of GATE U3A is differentiated by C3 and R3 with these pulses applied to the base of Q1. Since Q1 is a NPN transistor, only the positive pulses (applied every 250 milliseconds) cause the transistor to conduct. When Q1 conducts, the negative-going output pulse at its collector is fed to Pin 3 of Priority Sample One-Shot U4.

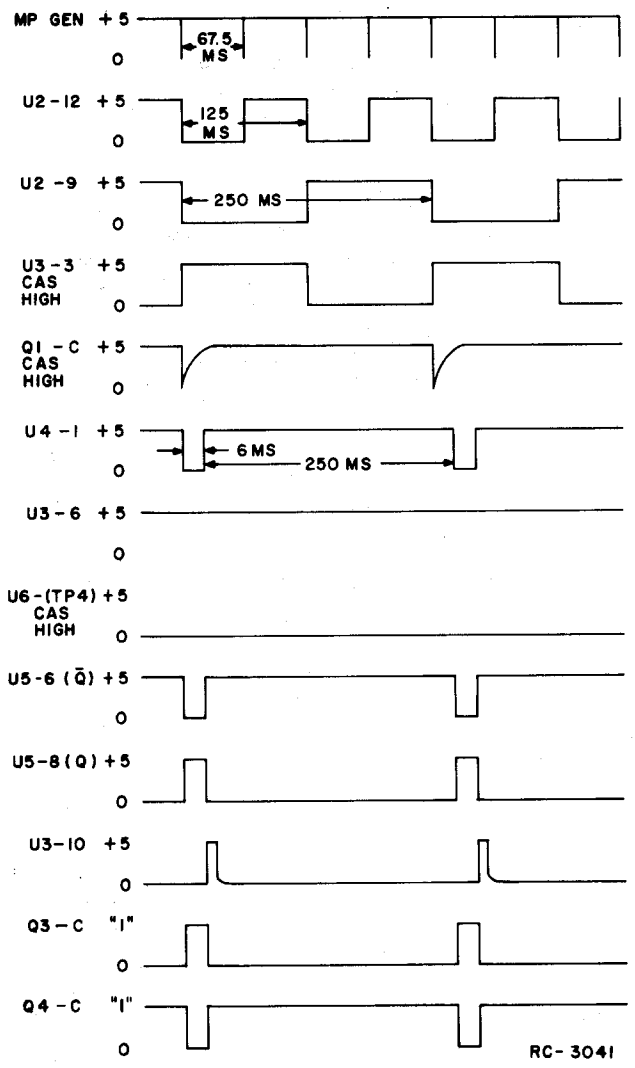


Figure 3 - Receiving Non-Priority Channel Waveforms

The Priority Sample One-Shot U4 provides a six millisecond positive output pulse from Pin 6 to the Audio Muting circuit and a six millisecond negative-going pulse to Pin 13 of Channel FF U5 and to Differentiator Q7.

In the audio muting circuit the audio circuit to the Volume control on the station system board is broken and brought in on P2413-2 coupled through C12, R27, C10 and emitter follower Q8, and then re-routed back out through P2413-1 back to the Volume control high on the system board.

The positive pulse from the Priority Sample One-Shot U4 Pin 6 turns on Q10 and Q9 for a total of eight milliseconds. When turned on, the collectors of Q10 and Q9 drop to ground potential, shunting the receiver audio path. This prevents an objectionable noise burst from being heard

at the speaker each time the priority channel is monitored (every 250 milliseconds).

At the same time the audio is muted, the negative-going output pulse of the One-Shot U4 Pin 1 is applied to the Squelch Muting transistor Q11 and to Differentiator Q7.

The fast squelch circuit consists of Q11 through Q14. When the priority channel is not being monitored, audio and noise applied to the fast squelch circuit is shunted to ground by the normally-on transistor Q11. When the Channel Flip-Flop is switched to the priority channel, the negative-going six millisecond One-Shot U4 Pin 1 output is applied to the base of Q11, turning the transistor off. While Q11 is turned off, the noise output of the active high-pass noise filter is applied to the base of Noise Amplifier Q13. The filter consists of C16, C14, C13, R30, R29, Squelch Adjust potentiometer R31, and Q12. Instructions for setting R31 are listed in the Table of Contents.

The output of Q13 is rectified by CR4 and CR5 and the resultant negative voltage turns off DC Switch Q14. Turning off Q14 removes the "0" at the input of GATE U3C Pin 9, unlocking the gate.

While Q14 is turned off, the output of One-Shot U4 Pin 1 is differentiated by C9 and R19, and the positive-going pulse turns off PNP transistor Q7. Turning off Q7 applies a "1" to Pin 10 of GATE U3C, switching the output to a "0" as long as Q14 is off. The "0" resets the Channel Flip-Flop U5, causing it to switch back to the non-priority channel. The entire cycle is repeated every 250 milliseconds until a signal is received on the priority channel.

If a signal is received on the priority channel during the six millisecond monitor period, the signal quiets the receiver. With the receiver quieted, there is insufficient noise to operate the fast squelch circuit so that Q14 remains on (its collector at ground potential). The "0" at the collector of Q14 blocks GATE U3C while the output of the CAS switch Q2 blocks GATE U3B. With both gates blocked, the Channel Flip-Flop remains locked on the priority channel for the duration of the signal.

The logical "0" at the collector of CAS switch Q2 is fed to the base of Light Inhibit Q6 keeping it off allowing the 6 millisecond turn on time of NOR GATE U6D to turn on Light Driver Q5. The Channel Busy Indicator CR2407 is biased on for 6 milliseconds every 250 milliseconds for this mode of operation.

PRIORITY DISABLE

The PSLM can also be modified to operate without priority for either channel. To disable the priority function of the PSLM and revert to Search Lock Monitor operation refer to Note 3 on the Schematic Diagram listed in the Table of Contents.

VOLTAGE REGULATOR

The Integrated Circuit Voltage Regulator VR1 provides +5.0 Volts to the PSLM circuits. Transistor Q16 is a DC switch that grounds the base of Q15 when the Search switch S2401 is turned on. This keeps Wiper switch Q15 turned off keeping the wiper lead for the frequency selector switch above ground potential.

TRANSMIT REVERT MODE

When operating in the Transmit Revert Mode (PTT switch depressed) the transmit revert circuits within the PSLM disable the two NOR GATES, the Channel Drivers and turn off the Channel Busy Indicator. Messages are transmitted on the channel selected by the Frequency Selector Switch.

Operating the PTT switch puts a logical "0" on the Delayed Push-To-Talk (DPTT) line. This logical "0" on the base of PTT switch Q17 causes it to turn on placing a logical "1" on the base of PTT switch Q18 turning it on. When Q18 conducts this places a logical "0" on the WIPER line for the Frequency Selector switch S701/S702 thus grounding the wiper and allowing the frequency select switch to determine the transmit frequency.

When the PTT switch Q17 is conducting this also places a logical "1" on the base of INVERTER Q19 turning it on which in turn puts a logical "0" on the base of Search Inhibit Q20, turning it off. With Q20 turned off this places a logical "1" on NOR GATES U6C Pin 9 and U6D Pin 12. This blocks both NOR GATES which also turns off the two Channel Drivers Q3 & Q4. With both Channel Drivers off the PSLM is disabled. The transmit frequency is now determined by the Frequency Selector switch S701/S702. With NOR GATE U6D blocked a logical "0" is put on the base of Light Driver Q5 turning it off. The Channel Busy Indicator CR2407 is turned off during this mode of operation.

MAINTENANCE

DISASSEMBLY

Loosen the knurled knobs located in the back, one on each side and remove the top cover. The PSLM board is mounted on the back side of the Front Control Housing.

TROUBLESHOOTING

To troubleshoot the PSLM board refer to the Schematic Diagram, Circuit Analysis and Timing waveforms in Figures 1, 2 and 3.

SYSTEM MODIFICATION

Modifications are required in the MASTR EXECUTIVE II Desk Top station combination when the Priority Search-Lock Monitor option 9922 is installed. Refer to the 19D423678 Installation Instructions.

PRIORITY SQUELCH ADJUSTMENT

Priority Squelch Adjust R31 was set at the factory for 20-dB quieting sensitivity on the priority channel, and will normally require no further adjustment. If it should become necessary to set R31, use one of the following procedures. Procedure A requires two signal generators (803A or equivalent) with a three way 6-dB pad. Procedure B requires a signal generator (803A or equivalent) with a 6-dB pad.

PROCEDURE A

Before starting Procedure A, make sure that the receiver is properly aligned with the PSLM disabled (Search switch in the off position). Then measure and record the F1 (or priority channel) 20-dB quieting sensitivity.

1. Turn on the PSLM Search switch on the Front Panel. Set Priority Squelch Adjust R31 fully clockwise.

2. Set the receiver squelch at critical squelch. Apply a 100 microvolt signal from generator #2, with standard modulation, to Channel 2. Also apply a 20-dB quieting level (previously measured and recorded). Modulate signal from generator #1 to Channel 1. Slowly turn the Priority Squelch adjust R31 counterclockwise until the PSLM locks on Channel 1 (priority channel). This will be shown by a steady glow of LED CR2407 on the Front Panel.

PROCEDURE B

1. Turn on the PSLM Search switch on the Front Panel.

2. With the receiver squelched, apply a 100 microvolt signal on Channel 2 (non-priority channel).

3. Turn R31 fully counterclockwise, causing the receiver to false (a repeated thumping noise is heard in the speaker).

4. Carefully turn R31 clockwise until the falsing stops. Then continue turning R31 clockwise for an additional 15 to 20 percent of rotation.

GENERAL ELECTRIC COMPANY • MOBILE COMMUNICATIONS DIVISION
WORLD HEADQUARTERS • LYNCHBURG, VIRGINIA 24502 U.S.A.

GENERAL ELECTRIC*
U.S.A.

Printed in U.S.A.

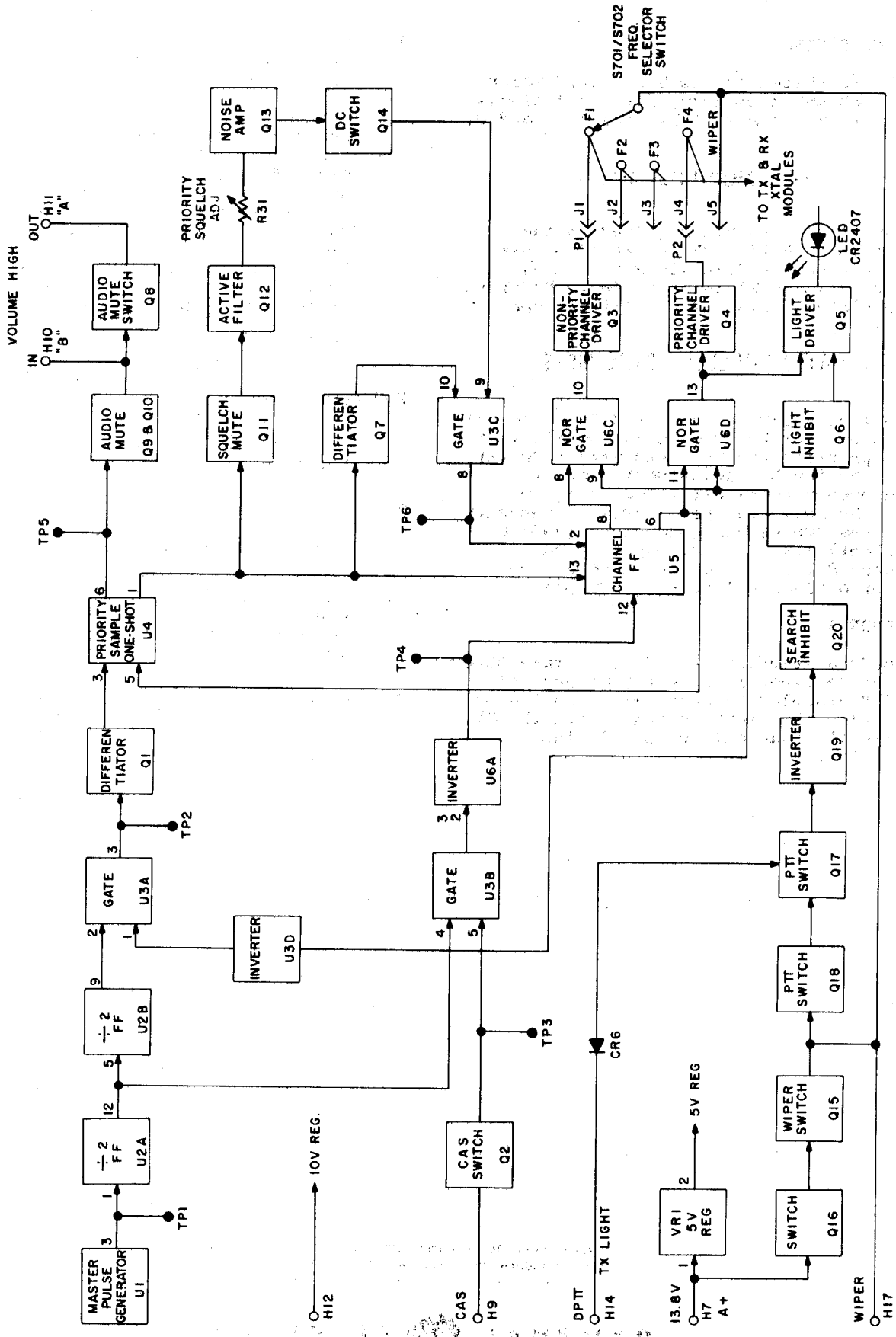
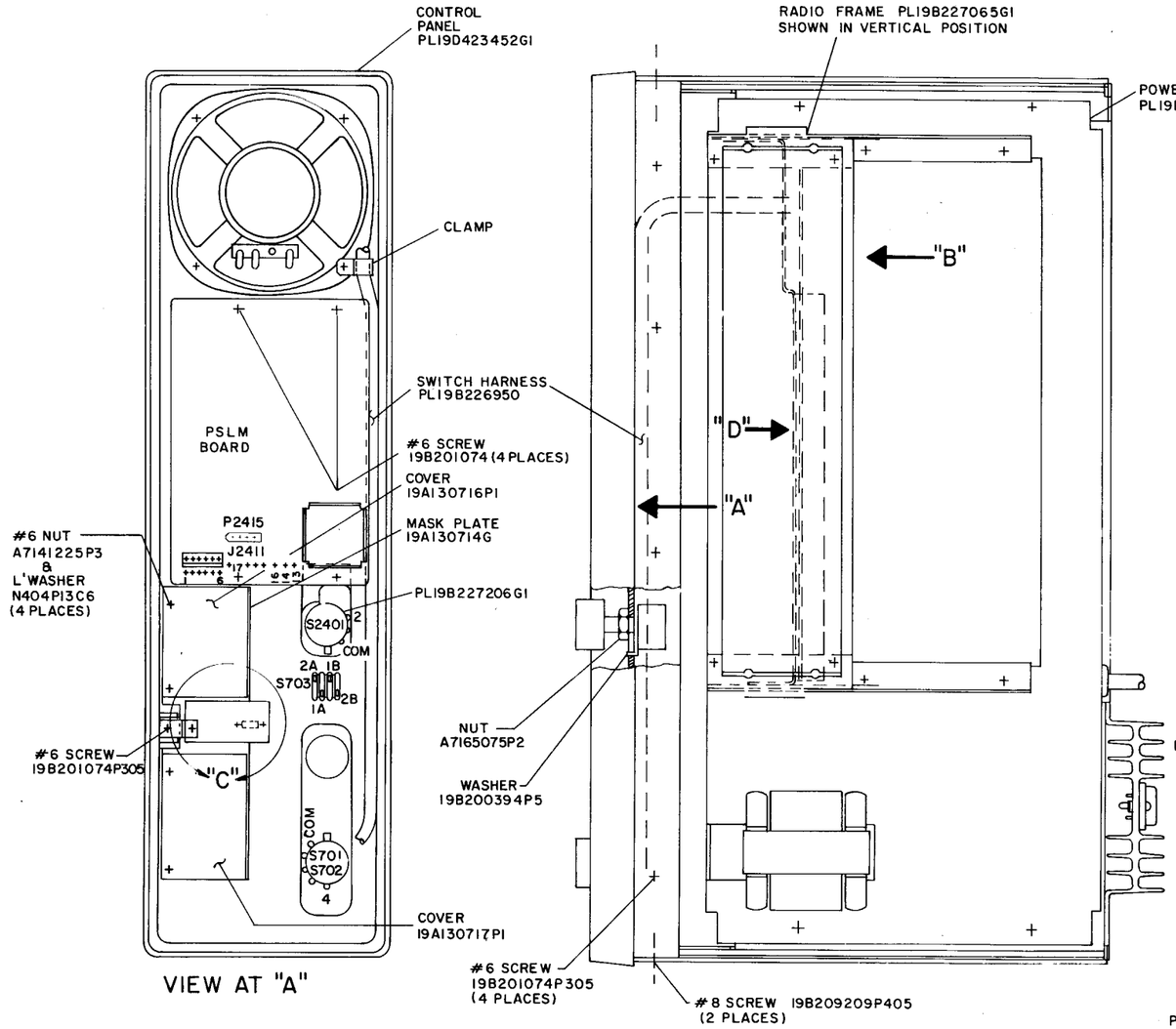
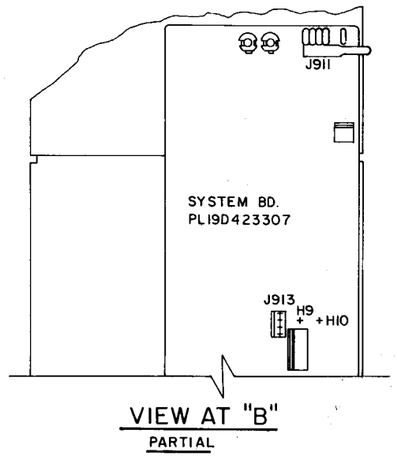
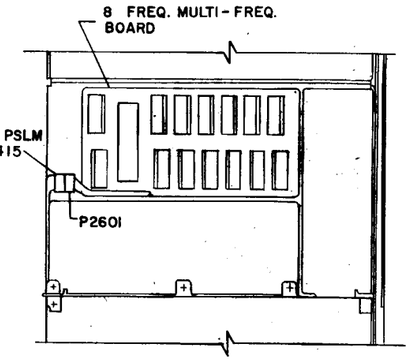


Figure 4 - Block Diagram MASTR Executive II Station PSLM

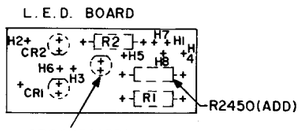




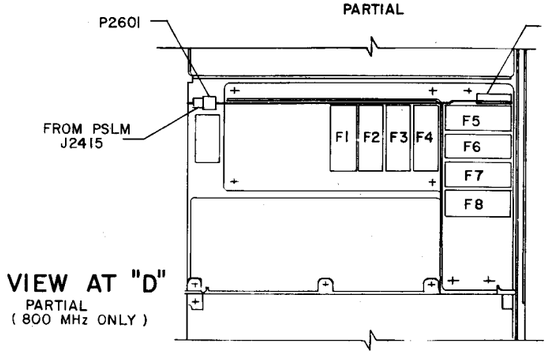
VIEW AT "B"
PARTIAL



VIEW AT "D"
PARTIAL



DETAIL "C"
ENLARGED



VIEW AT "D"
PARTIAL
(800 MHz ONLY)

THESE INSTRUCTIONS COVER INSTALLATION OF PSLM BD. PLI9C321727GI TO A MULTI-FREQUENCY MASTR EXECUTIVE II DESK TOP STATION.

INSTRUCTIONS:

1. REMOVE FRONT CASTING FROM BASE AND KEEP HARDWARE FOR REASSEMBLY.
2. REMOVE AND DISCARD DUMMY SHAFT AND REPLACE WITH S2401 AS SHOWN. SAVE KNOB AND ASSEMBLE TO SWITCH.
3. ASM. P.S.L.M. BOARD AS SHOWN AND DRESS CABLE UNDER EDGE OF BOARD ROUTING P2411 & P2413 CABLES THROUGH CABLE CLAMP.
4. REMOVE LED BOARD AND ASSEMBLE R2450 & CR2407 IN LOCATIONS SHOWN. SAVE SCREW 19B201074P305 FOR REASSEMBLY.
5. SOLDER SF22-BL WIRE FROM S2401-2 INTO H7 OF LED BOARD.
6. SOLDER SF22-W-O-R WIRE FROM H15 ON PSLM BOARD INTO H5 OF LED BOARD.
7. SOLDER SF22-BR WIRE FROM H14 ON PSLM BOARD INTO H6 OF LED BOARD.
8. REMOVE MASK PLATE 19AI30714GI BY REMOVING 2 #6 NUTS AND L'WASHERS, 1 FROM EITHER END OF PLATE. RETAIN 2 #6 NUTS AND L'WASHERS FOR REASSEMBLY. REMOVE COVER 19AI30716PI AND COVER 19AI30717PI FROM MASK PLATE 19AI30714GI BY REMOVING 2 #6 NUTS & L'WASHERS LEFT ON PLATE. RETAIN 2 #6 NUTS AND L'WASHERS FOR REASSEMBLY. DISCARD MASK PLATE 19AI30714GI AND REPLACE WITH MASK PLATE 19AI30714G2. REASSEMBLE COVERS TO MASK PLATE AND MASK PLATE TO FRONT CASTING BY REVERSING PROCEDURE.
9. REASSEMBLE LED BOARD USING EXISTING HARDWARE SAVED FROM INSTRUCTION 4.
10. SOLDER SF22-BL WIRE FROM PSLM BOARD H13 TO S2401-COMMON.
11. SOLDER SF22-W-G-O WIRE FROM PSLM BOARD H16 TO S703-1A.
12. REMOVE AND DISCARD BLACK WIRE FROM S701, S702 OR S704 COMMON TO S703-1B.
13. SOLDER SF22-W-G-O WIRE FROM S2401-1 TO S703-1B.
14. SOLDER SF22-BK WIRE FROM PSLM BOARD H17 TO S701 OR S702 COMMON.
15. UNPLUG P911, PART OF SWITCH HARNESS 19B226950, FROM J911 ON SYSTEM BOARD AND PLUG ONTO J2411 ON PSLM BOARD.
16. CUT JUMPER FROM H9 TO H10 ON SYSTEM BOARD.
17. PLUG P2411 FROM PSLM BOARD ONTO J911 ON SYSTEM BOARD.
18. PLUG P2413 FROM PSLM BOARD ONTO J913 ON SYSTEM BOARD.

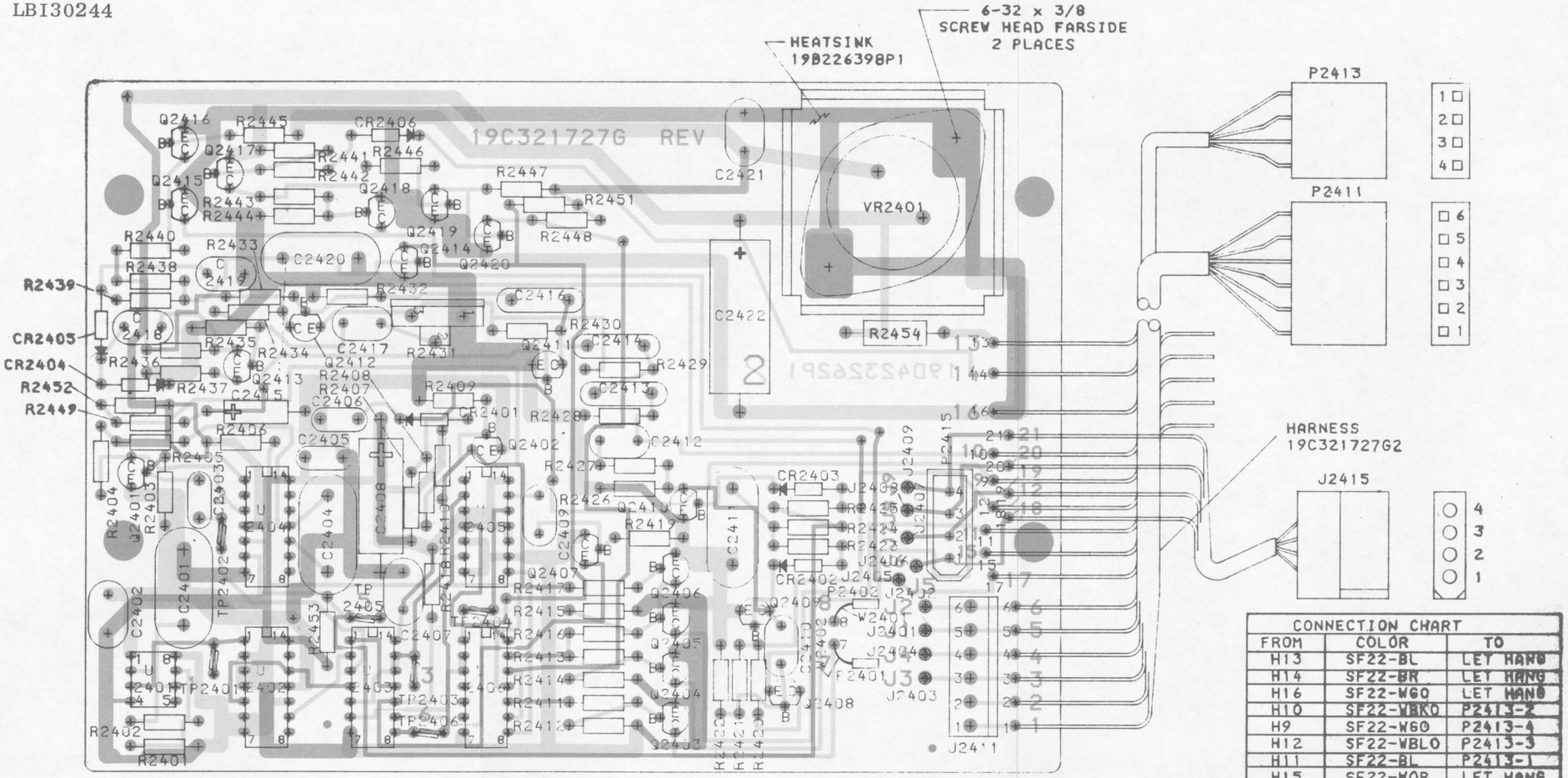
FOR 8 FREQ UNITS ONLY:

19. UNPLUG J2601 FROM P2601 AT THE 8 FREQ MULTI-FREQ BOARD AND PLUG INTO P2415 ON PSLM BOARD.
20. PLUG J2415 FROM PSLM BOARD INTO P2601 AT THE 8 FREQ MULTI-FREQ BOARD.
21. REASSEMBLE FRONT CASTING TO BASE USING HARDWARE RETAINED FROM INSTRUCTION 1.

FOR 800 MHz UNITS ONLY:

22. REMOVE R991 AND R992 FROM SYSTEM BOARD.

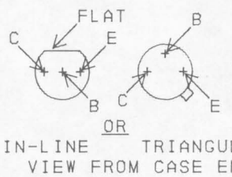
(19D423678, Rev. 6)



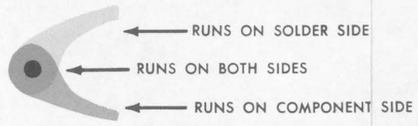
(19C327475, Rev. 2)
(19B226967, Sh. 1, Rev. 2)
(19B226967, Sh. 2, Rev. 2)

CONNECTION CHART		
FROM	COLOR	TO
H13	SF22-BL	LET HANG
H14	SF22-BR	LET HANG
H16	SF22-WGO	LET HANG
H10	SF22-WBKO	P2413-2
H9	SF22-WGO	P2413-4
H12	SF22-WBLO	P2413-3
H11	SF22-BL	P2413-1
H15	SF22-WOR	LET HANG
H17	SF22-BK	LET HANG
H6	SF22-W	P2411-6
H5	SF22-G	P2411-5
H4	SF22-O	P2411-4
H3	SF22-BK	P2411-3
H2	SF22-R	P2411-2
H1	SF22-BR	P2411-1
H18	SF22-BL	J2415-1
H19	SF22-WRBK	J2415-2
H20	SF22-W	J2415-3
H21	SF22-WGO	J2415-4

LEAD IDENTIFICATION
FOR Q2401-Q2420

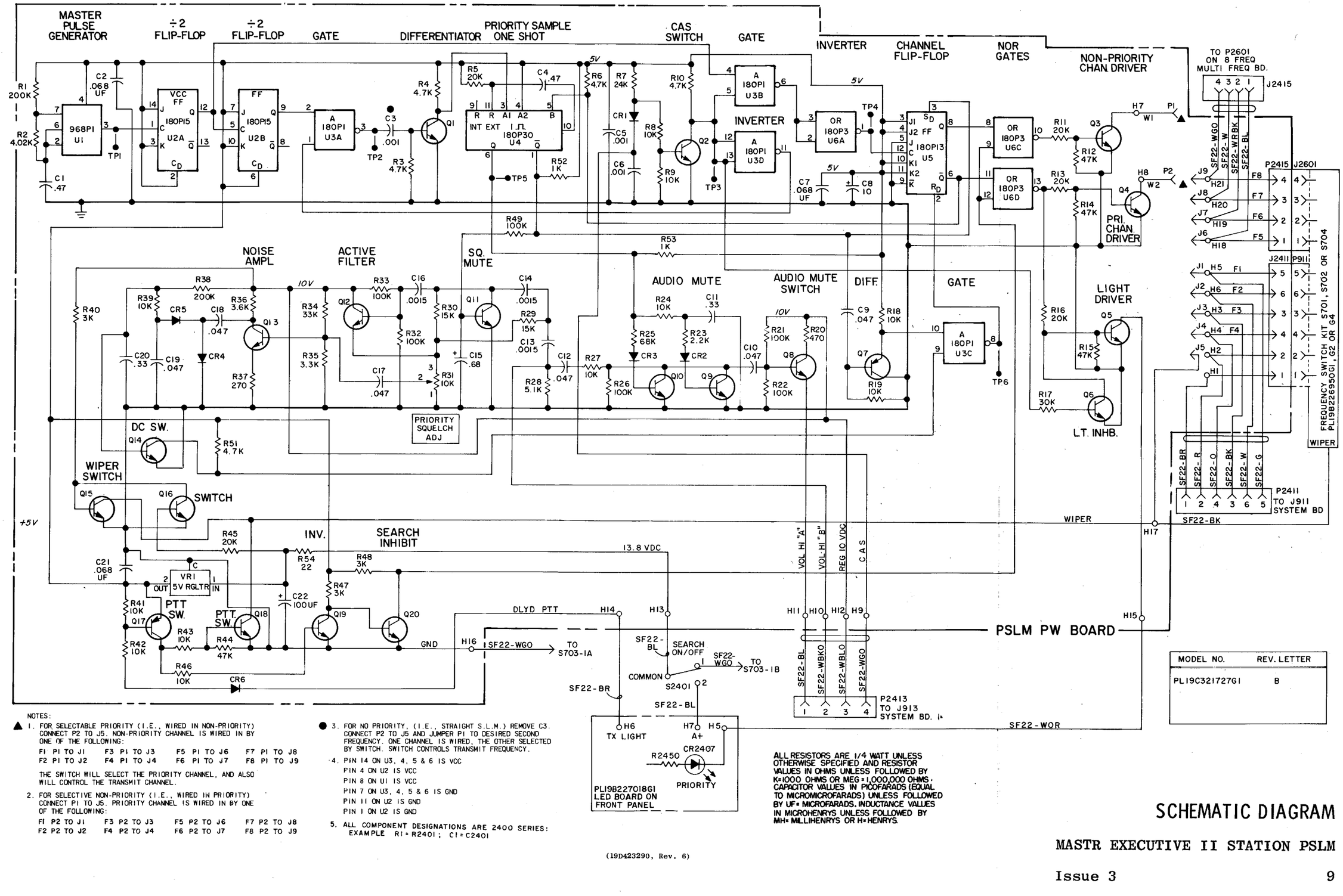


NOTE: LEAD ARRANGEMENT, AND NOT CASE SHAPE, IS DETERMINING FACTOR FOR LEAD IDENTIFICATION. TAB INDICATES EMITTER LEAD.



OUTLINE DIAGRAM

MASTR EXECUTIVE II STATION PSLM



NOTES:

▲ 1. FOR SELECTABLE PRIORITY (I.E., WIRED IN NON-PRIORITY) CONNECT P2 TO J5. NON-PRIORITY CHANNEL IS WIRED IN BY ONE OF THE FOLLOWING:

F1 P1 TO J1	F3 P1 TO J3	F5 P1 TO J6	F7 P1 TO J8
F2 P1 TO J2	F4 P1 TO J4	F6 P1 TO J7	F8 P1 TO J9

THE SWITCH WILL SELECT THE PRIORITY CHANNEL, AND ALSO WILL CONTROL THE TRANSMIT CHANNEL.

2. FOR SELECTIVE NON-PRIORITY (I.E., WIRED IN PRIORITY) CONNECT P1 TO J5. PRIORITY CHANNEL IS WIRED IN BY ONE OF THE FOLLOWING:

F1 P2 TO J1	F3 P2 TO J3	F5 P2 TO J6	F7 P2 TO J8
F2 P2 TO J2	F4 P2 TO J4	F6 P2 TO J7	F8 P2 TO J9

● 3. FOR NO PRIORITY, (I.E., STRAIGHT S.L.M.) REMOVE C3. CONNECT P2 TO J5 AND JUMPER P1 TO DESIRED SECOND FREQUENCY. ONE CHANNEL IS WIRED, THE OTHER SELECTED BY SWITCH. SWITCH CONTROLS TRANSMIT FREQUENCY.

4. PIN 14 ON U3, 4, 5 & 6 IS VCC
PIN 4 ON U2 IS VCC
PIN 8 ON U1 IS VCC
PIN 7 ON U3, 4, 5 & 6 IS GND
PIN 11 ON U2 IS GND
PIN 1 ON U2 IS GND

5. ALL COMPONENT DESIGNATIONS ARE 2400 SERIES: EXAMPLE R1 = R2401; C1 = C2401

ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY K=1000 OHMS OR MEG=1,000,000 OHMS. CAPACITOR VALUES IN PICOFARADS (EQUAL TO MICROMICROFARADS) UNLESS FOLLOWED BY UF= MICROFARADS. INDUCTANCE VALUES IN MICROHENRYS UNLESS FOLLOWED BY MH= MILLIHENRYS OR H= HENRYS.

MODEL NO.	REV. LETTER
PLI9C321727G1	B

(19D423290, Rev. 6)

SCHEMATIC DIAGRAM

MASTR EXECUTIVE II STATION PSLM

PARTS LIST

LBI30245B

MASTR EXECUTIVE II STATION
PRIORITY SEARCH LOCK MONITOR
19C321727G1

SYMBOL	GE PART NO.	DESCRIPTION
		- - - - - - - - - - - CAPACITORS - - - - - - - - -
C2401	19A116080P111	Polyester: 0.47 µf ±10%, 50 VDCW.
C2402	19A116080P106	Polyester: 0.068 µf ±10%, 50 VDCW.
C2403	5494481P111	Ceramic disc: 1000 pf ±20%, 1000 VDCW; sim to RMC Type JF Discap.
C2404	19A116080P211	Polyester: 0.47 µf ±5%, 50 VDCW.
C2405 and C2406	5494481P111	Ceramic disc: 1000 pf ±20%, 1000 VDCW; sim to RMC Type JF Discap.
C2407	19A116080P106	Polyester: 0.068 µF ±10%, 50 VDCW.
C2408	19A115680P8	Electrolytic: 10 µf +150% -10%, 25 VDCW; sim to Mallory Type TTX.
C2409 and C2410	19A116080P5	Polyester: 0.047 µf ±20%, 50 VDCW.
C2411	19A116080P110	Polyester: 0.33 µf ±10%, 50 VDCW.
C2412	19A116080P5	Polyester: 0.047 µf ±20%, 50 VDCW.
C2413 and C2414	5494481P124	Ceramic disc: 1500 pf ±10%, 1000 VDCW; sim to RMC Type JF Discap.
C2415	5496267P29	Tantalum: 0.68 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C2416	5494481P124	Ceramic disc: 1500 pf ±10%, 1000 VDCW; sim to RMC Type JF Discap.
C2417 thru C2419	19A116080P5	Polyester: 0.047 µf ±20%, 50 VDCW.
C2420	19A116080P110	Polyester: 0.33 µf ±10%, 50 VDCW.
C2421	19A116080P106	Polyester: 0.068 µf ±10%, 50 VDCW.
C2422	19A115680P7	Electrolytic: 100 µf +150% -10%, 15 VDCW; sim to Mallory Type TTX.
		- - - - - - - - DIODES AND RECTIFIERS - - - - - -
CR2401 thru CR2406	19A115250P1	Silicon, fast recovery, 225 mA, 50 PIV.
CR2407	19A134354P2	Diode, optoelectronic: yellow; sim to HEW. Packard 5082-4555.
		- - - - - - - - JACKS AND RECEPTACLES - - - - - -
J2401 thru J2405	4033513P15	Contact, electrical: sim to Bead Chain R40-1A.
J2406* thru J2409*	4033513P15	Contact, electrical: sim to Bead Chain R40-1A. Added by REV B.
J2411	19A116659P105	Connector, printed wiring: 6 contacts; sim to Molex 09-60-1061.
J2415*		Connector. Includes: Added by REV B.
	19B209505P204	Shell.
	19B209505P21	Contact, female. (Quantity 4).
		- - - - - - - - - - - PLUGS - - - - - - - - - - -
P2411		Connector. Includes:
	19A116659P80	Shell.
	19A116781P6	Contact, electrical: wire range No. 22-26 AWG; sim to Molex 08-50-0108. (Quantity 6).
P2413		Connector. Includes:
	19A116659P84	Shell.
	19A116781P6	Contact, electrical: wire range No. 22-26 AWG; sim to Molex 08-50-0108. (Quantity 4).
P2415*		Connector. Includes: Added by REV B.
	19B209505P104	Shell.
	19B209505P22	Contact, male. (Quantity 4).
		- - - - - - - - - TRANSISTORS - - - - - - - - -
Q2401 thru Q2406	19A115910P1	Silicon, NPN; sim to Type 2N3904.
Q2407	19A115852P1	Silicon, PNP; sim to Type 2N3906.
Q2408 thru Q2416	19A115910P1	Silicon, NPN; sim to Type 2N3904.
Q2417	19A115852P1	Silicon, PNP; sim to Type 2N3906.
Q2418 thru Q2420	19A115910P1	Silicon, NPN; sim to Type 2N3904.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R2401	19C314256P22003	Metal film: 200K ohms ±1%, 1/4 w.
R2402	19C314256P24021	Metal film: 4.02K ohms ±1%, 1/4 w.
R2403 and R2404	3R152P472J	Composition: 4.7K ohms ±5%, 1/4 w.
R2405	3R152P203J	Composition: 20K ohms ±5%, 1/4 w.
R2406	3R152P472J	Composition: 4.7K ohms ±5%, 1/4 w.
R2407	3R152P243J	Composition: 24K ohms ±5%, 1/4 w.
R2408 and R2409	3R152P103J	Composition: 10K ohms ±5%, 1/4 w.
R2410	3R152P472J	Composition: 4.7K ohms ±5%, 1/4 w.
R2411	3R152P203J	Composition: 20K ohms ±5%, 1/4 w.
R2412	3R152P473J	Composition: 47K ohms ±5%, 1/4 w.
R2413	3R152P203J	Composition: 20K ohms ±5%, 1/4 w.
R2414 and R2415	3R152P473J	Composition: 47K ohms ±5%, 1/4 w.
R2416	3R152P203J	Composition: 20K ohms ±5%, 1/4 w.
R2417	3R152P303J	Composition: 30K ohms ±5%, 1/4 w.
R2418 and R2419	3R152P103J	Composition: 10K ohms ±5%, 1/4 w.
R2420	3R152P471J	Composition: 470 ohms ±5%, 1/4 w.
R2421 and R2422	3R152P104J	Composition: 100K ohms ±5%, 1/4 w.
R2423	3R152P222J	Composition: 2.2K ohms ±5%, 1/4 w.
R2424	3R152P103J	Composition: 10K ohms ±5%, 1/4 w.
R2425	3R152P683J	Composition: 68K ohms ±5%, 1/4 w.
R2426	3R152P104J	Composition: 100K ohms ±5%, 1/4 w.
R2427	3R152P103J	Composition: 10K ohms ±5%, 1/4 w.
R2428	3R152P512J	Composition: 5.1K ohms ±5%, 1/4 w.
R2429 and R2430	3R152P153J	Composition: 15K ohms ±5%, 1/4 w.
R2431	19B209358P106	Variable, carbon film: approx 300 to 10,000 ohms ±10%, 0.25 w; sim to CTS Type X-201.
R2432 and R2433	3R152P104J	Composition: 100K ohms ±5%, 1/4 w.
R2434	3R152P333J	Composition: 33K ohms ±5%, 1/4 w.
R2435	3R152P332J	Composition: 3.3K ohms ±5%, 1/4 w.
R2436	3R152P362J	Composition: 3.6K ohms ±5%, 1/4 w.
R2437	3R152P271J	Composition: 270 ohms ±5%, 1/4 w.
R2438	3R152P204J	Composition: 200K ohms ±5%, 1/4 w.
R2439	3R152P103J	Composition: 10K ohms ±5%, 1/4 w.
R2440	3R152P302J	Composition: 3K ohms ±5%, 1/4 w.
R2441 thru R2443	3R152P103J	Composition: 10K ohms ±5%, 1/4 w.
R2444	3R152P473J	Composition: 47K ohms ±5%, 1/4 w.
R2445	3R152P203J	Composition: 20K ohms ±5%, 1/4 w.
R2446	3R152P103J	Composition: 10K ohms ±5%, 1/4 w.
R2447 and R2448	3R152P302J	Composition: 3K ohms ±5%, 1/4 w.
R2449	3R152P104J	Composition: 100K ohms ±5%, 1/4 w.
R2450	3R77P561J	Composition: 560 ohms ±5%, 1/2 w.
R2451	3R152P472J	Composition: 4.7K ohms ±5%, 1/4 w.
R2452 and R2453	3R152P102J	Composition: 1K ohms ±5%, 1/4 w.
R2454	3R77P220J	Composition: 22 ohms ±5%, 1/2 w.
		- - - - - - - - - - SWITCHES - - - - - - - - - -
S2401	19B227206G1	Rotary: 1 pole, 2 positions, non-shorting, 36° indexing contacts, 10 ma at 115 VDC or 1 amp at 28 VDC, molded melamine plastic base, without mounting hardware; sim to Grayhill Series 5000.
		- - - - - - - - - - TEST POINTS - - - - - - - - - -
TP2401 thru TP2406	19B211379P1	Spring (Test Point).
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - - -
U2401	19A116968P1	Linear, Dual In Line 8 Pin Mini Dip package; sim to Signetics SA555N.
U2402	19A116180P15	Digital, Dual J-K Master-Slave Flip-Flop: Identification No. 7473.
U2403	19A116180P1	Digital, Quad 2-Input Nand Gate: Identification No. 7400.
U2404	19A116180P30	Digital, Monostable Multivibrator: Identification No. 74121.
U2405	19A116180P13	Digital, J-K Flip-Flop: Identification No. 7470.
U2406	19A116180P3	Digital, Quad 2-Input Nor Gate: Identification No. 7402.
		- - - - - - - - VOLTAGE REGULATORS - - - - - - - -
VR2401	19A116834P1	Linear, regulator: 35 volt input, 20 watts; sim to MICROAMP 209K.
		- - - - - - - - - - CABLES - - - - - - - - - -
W2401 and W2402	19A129947G4	Cable: approx 2 inches long.
		HARNESS ASSEMBLY 19C321727G2 (Includes J2415, P2411, P2413)
		- - - - - - - - - MISCELLANEOUS - - - - - - - - -
	19B226398P1	Heat Sink. (Used with VR2401).
	19A130714G2	Plate.

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter," which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by these revisions.

REV. A - To improve the stability of the 5 Volt Regulator. Added C2422 and R2454.

REV. B - To allow use with 8 frequency station. Added J2406-J2409, J2415 and P2415.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES