MOBILE RADIO

MAINTENANCE MANUAL

FOUR/EIGHT FREQUENCY PRIORITY SEARCH LOCK MONITOR

(Used with C-800/C-900 Series Control Units)

Maintenance Manual LBI 30258F
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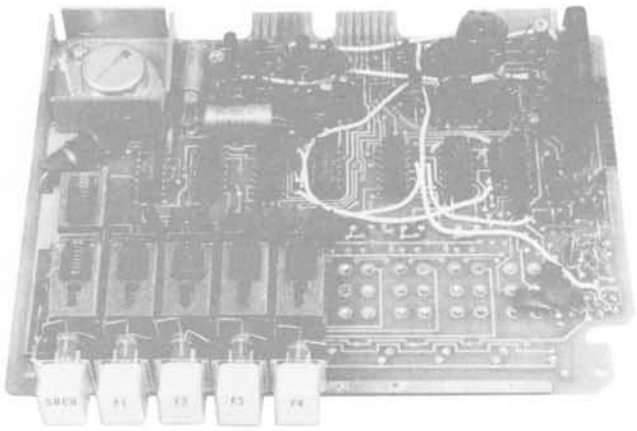

FOUR/EIGHT FREQUENCY PRIORITY SEARCH LOCK MONITOR 19D417678G1, 2

SPECIFICATIONS *

Controls	Priority Squelch Adjust Search (ON-OFF) Non-Priority Selector Switches (eight)
Channel Search Rate	5 Times Per Second (Four Frequency) 2.5 Times Per Second (Eight Frequency)
Priority Sample Time	6-7 Milliseconds
Priority Sample Rate	Four Times Per Second
Priority Signal Override	20 dB quieting
Temperature Range	-40°C to +70°C (-40°F to +158°F)
Current Drain	190 mA
Indicators	One Search Enable and Eight Multi-functional Channel Indicators
Voltage Input	13.8 VDC ±20%
Regulator Output	5 VDC ±0.25 VDC 9 VDC ±1 VDC

*These specifications are intended primarily for the use of the serviceman. Refer to the appropriate Specification Sheet for the complete specifications.

GENERAL ELECTRIC

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WARNING

Although the highest DC voltage in the radio is supplied by the vehicle battery, high current may be drawn under short circuit conditions. These currents can possibly heat metal objects such as tools, rings, watchbands, etc. enough to cause burns. Be careful when working near energized 12-volt circuits.

High-level RF energy in the transmitter Power Amplifier assembly can cause RF burns. KEEP AWAY FROM THESE CIRCUITS WHEN THE TRANSMITTER IS ENERGIZED!

DESCRIPTION

The General Electric four/eight frequency Priority Search Lock Monitor (PSLM) sequentially searches up to eight channels for an incoming message. The priority channel is selectable using the channel selector switch; the non-priority channels to be searched are selected by the non-priority pushbutton switches located on the PSLM module. This arrangement allows the user to select the priority and non-priority channels to be searched at any given time.

The priority channel may also be strapped for locked priority operation, thus eliminating the selectable priority option. This allows the user to transmit on any channel without automatically reassigning the priority channel.

The 19D417678 PSLM is used with the C-800 and C-900 series control units and plugs into the option deck (upper level in C-800 control series units and the center or upper level in the C-900 series control units). The 19D417678G1 searches a maximum of four channels while the 19D417678G2 searches a maximum of eight channels. If number of channels to be searched is less than the capability of the board, the unused channels are made inoperative by the use of lockout rivets installed behind the pushbuttons.

The component board is equipped with backlighted pushbutton switches (push-push) for search control and non-priority channel selection. Light Emitting Diodes (LED's) are used exclusively to illuminate the indicators. The SRCH (search) switch turns the PSLM "on" or "off" and the remaining switches (4 or 8) select the non-priority channels to be searched.

OPERATION

When only the SRCH button is pressed in all pushbutton switches are backlighted, indicating the PSLM is on, but not searching. The SRCH button will be at maximum brightness, the others somewhat less brilliant.

When the SRCH switch is in the "OFF" position, the PSLM circuitry is disabled and messages are received and transmitted on the channel selected by the channel selector switch(es). The SRCH pushbutton is backlighted at a low level.

To initiate channel searching, press in the SRCH pushbutton, select the desired priority channel using the channel selector switch(es), and select the non-priority channels by pressing in the corresponding non-priority pushbutton switches on the PSLM module (option deck). The PSLM sequentially monitors the priority and non-priority channels and selects the appropriate channel when a message is received.

The PSLM assures reception of all signals on the priority channel regardless of the signal strength of the first channel received. It searches the selected channels (4 or 8 maximum) for a period of 40 milliseconds at least twice each second (five times if 4-freq. PSLM); the priority channel is searched at least five times each second for a period of 40 milliseconds.

When a signal is received on the priority channel, the PSLM stops searching and locks on the priority channel for the duration of the message. The priority channel indicator will glow at maximum brightness and will not flash on and off. The audio will be louder than non-priority channels.

When a signal is received on the non-priority channel, the PSLM stops on that channel but continues to monitor the priority channel. The indicator for the receiving non-priority channel is on at maximum brightness and blinks off during the priority channel search time. The priority channel indicator will flash on indicating that it's being searched while receiving the non-priority message. If a signal is then received on the priority channel whose signal strength equals or exceeds 20 dB quieting, the PSLM reverts to the priority channel and locks for the duration of the priority message.

NOTE

The PSLM operates only when the receiver is squelched. When the receiver is unsquelched the PSLM will lock onto the active channel. If this should be the non-priority channel and a second signal is received on the priority channel the PSLM will revert to priority channel operation.

During short periods of signal fadeout or temporary loss of carrier, a CAS delay circuit will hold the receiver open for up to 1.3 seconds. This will prevent the PSLM from searching and perhaps selecting an alternate channel.

CIRCUIT ANALYSIS

SEARCH Switch (S2401)

Refer to Figure 1 (Block Diagram) and Schematic Diagram for details.

SRCH switch S2401 turns the search function "on" or "off". When selected (pushed in) the switch:

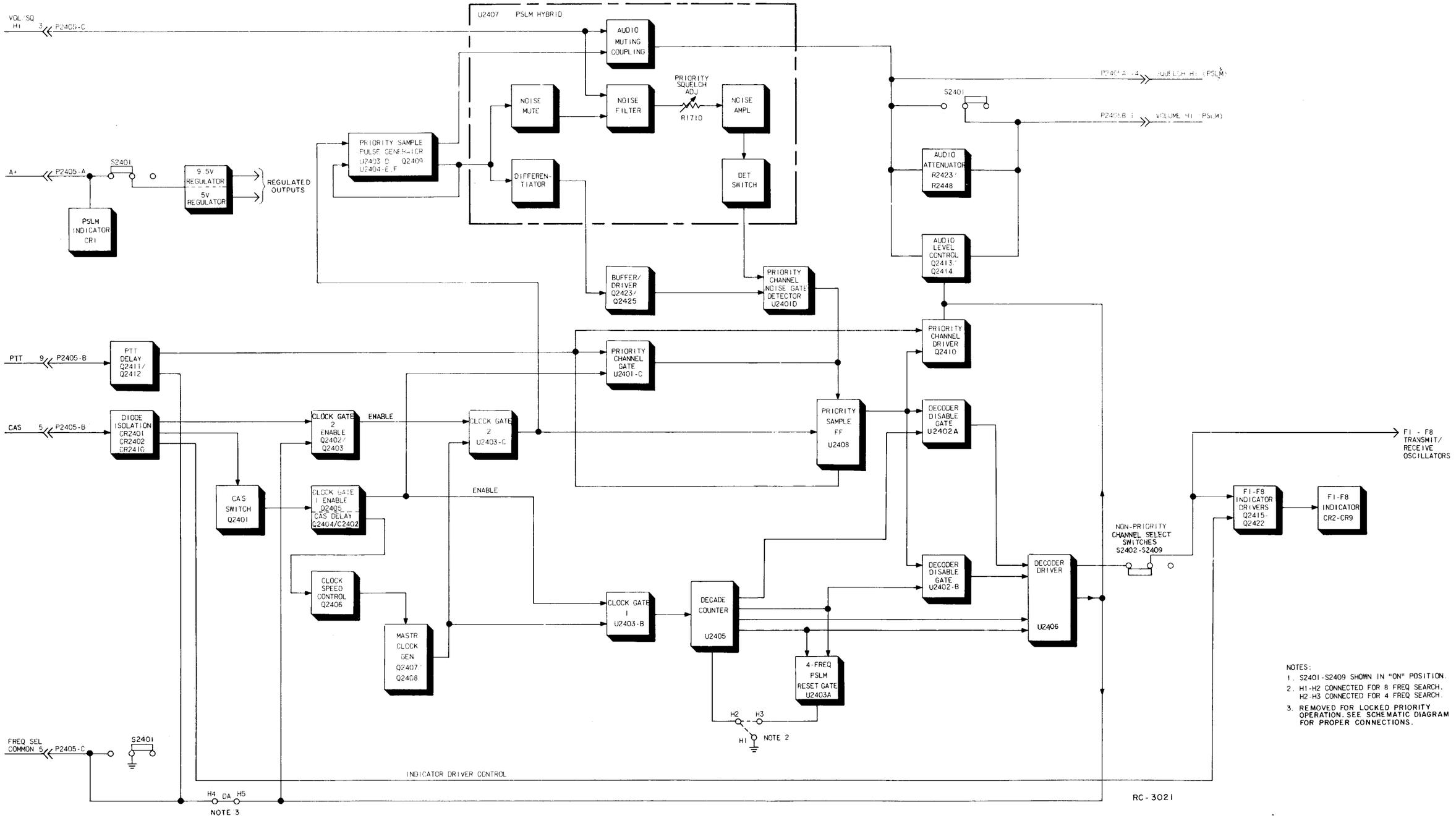

Figure 1 - Block Diagram

(1) enables the non-priority audio attenuator to provide a reduced audio level for all non-priority channels (audio is attenuated on non-priority channels due to open contacts 3 and 5, which insert the audio attenuator into the circuit).

(2) applies A+ to the +5 V regulator and SRCH indicator LED through closed contacts 4 and 6 to operate all IC's and transistors not supplied by the 9.5 V regulator. The SRCH indicator glows at maximum brightness.

(3) removes A- from the frequency select lead to allow channel search control by the PSLM circuitry.

(4) removes A- from pin 1 of the PSLM mute hybrid, to enable it.

When the search mode is not selected, (SRCH switch is "out") the SRCH switch:

(1) removes power from the +5 V regulator.

(2) bypasses the audio attenuator for non-priority channels thereby providing the same audio level for all channels.

(3) applies A- to the frequency select lead to assure that all transmissions occur over the channel indicated by the channel selector switch on the control modules.

(4) applies A- to pin 1 of the PSLM hybrid to disable it.

Operating the push-to-talk (PTT) switch disables the PSLM circuitry and permits message transmissions on the frequency selected by the channel selector switch. The Channel Busy indicator is off when transmitting.

A+ is applied to the SRCH indicator at all times through P2405A-7, R2455 and R2458, causing it to operate at a reduced light level; however, when operating in the search mode, R2424 is placed in parallel with R2458 causing the SRCH indicator to operate at maximum brightness.

MASTER CLOCK GENERATOR

The master clock generator generates the timing pulses required to search the selected channels and to monitor the priority channel while receiving on a non-priority channel. It consists of transistors Q2407 and Q2408, clock speed control transistor Q2406, diode CR2405, capacitor C2403 and resistors R2410 and R2411. The master clock generator operates at two different speeds, 4 and 25 Hz, and generates an output pulse at 250 or 40 millisecond intervals respectively.

Q2406 monitors the output of CAS switch Q2401. In the search mode (receiver squelched), CAS switch Q2401 is turned off and holds clock speed control transistor Q2406 off. Switching diode CR2405 is forward biased, paralleling R2410 and R2411 and causing the master clock generator to operate at 25 Hz. The fast clock speed is determined by R2410, R2411 and C2403. The output pulse is a negative going 3-Volt pulse with a width of approximately one millisecond.

When a message is received on any channel, the CAS line goes to +10 V and CAS switch Q2401 turns on. Clock speed control transistor Q2406 then turns on, back biasing diode CR2405 to remove R2410 from the emitter circuit of Q2407. This causes the master clock generator to operate at 4 Hz, providing a negative output pulse every 250 milliseconds. The slow clock speed is determined by R2411 and C2403.

CAS DELAY

The CAS delay circuit holds the receiver open for up to 1.3 seconds during periods of signal fade out or loss of carrier. This prevents the PSLM from searching during the CAS delay time and perhaps selecting an alternate channel.

The CAS delay circuit consists of C2402, R2407, R2409 and Q2404. When a carrier is received, CAS switch Q2401 turns on and charges C2402. During a short signal fadeout or loss of carrier, CAS switch Q2401 will turn off, thus attempting to remove the positive voltage from the base of clock gate 1 enable transistor Q2405, clock speed control transistor Q2406 and CAS delay capacitor C2402. Instead, capacitor C2402 now begins discharging through R2407, R2409 and the base/emitter junctions of Q2405 and Q2406 respectively. Q2405 and Q2406 remain on, thereby preventing the PSLM from reverting to the search mode during the CAS delay time.

Should the carrier fail to return within 1.3 seconds, C2402 will have discharged to a level sufficient to turn off clock speed control transistor Q2406 and start to turn off clock gate 1 enable transistor Q2405.

When Q2405 starts to turn off, CAS delay Q2404 instantaneously turns on, turning Q2405 off fast. This locks the PSLM into the search mode again causing all channels to be searched sequentially.

NOTE

The CAS delay feature is not compatable with Channel Guard or in radios that utilize PSLM with locked priority. If either of these two conditions exist, CAS delay capacitor C2402 must be removed.

MODES OF OPERATION

To facilitate circuit analysis, a description is provided for each of the three operational modes:

- Receiver Squelched
- Receiving Non-Priority - Searching Priority Channel
- Receiving Priority Channel

RECEIVER SQUELCHED

When the receiver is squelched (no signal applied) the PSLM sequentially searches each selected channel as follows:

- Searches non-priority channel an average of 2.5 times per second
- Searches priority channel at <u>least</u> 5 times per second (more if the priority channel is selected by the non-priority select switch)

When the receiver is squelched (no messages being received), the CAS line is near A-. This low is applied to a diode isolation matrix consisting of CR2401, CR2402 and CR2410 and controls the CAS switch, channel indicator drivers and clock gate 2 enable transistors Q2403 and Q2402. The channel indicator drivers are held off. CAS switch Q2401 is turned off, producing a low state on its emitter. This low is applied to the base of Q2406, turning it off and causing the master clock generator to operate at the fast speed (a pulse every 40 milliseconds). At the same time, CR2403 is reverse biased turning Q2402 off. When Q2402 turns off, Q2403 turns on placing a low on one input of clock gate 2 (U2403C). This turns clock gate 2 off, inhibiting the clock input pulse to the priority sample (one-shot) pulse generator.

The negative output pulse from the master clock generator is applied through inverter U2404C to one input of clock gate 2. The second input to clock gate 2 is also high since clock gate 1 enable transistor Q2405 is held off by CAS switch Q2401. The collector of Q2405 goes high enabling clock gate 2 and allowing the inverted clock pulses to be applied to the trigger input of decade counter U2405. Refer to Figure 2, Receiver Squelched Timing Diagram.

BCD (Binary Coded Decimal) outputs are applied from decade counter U2405 to Decoder/Driver, U2406. Pins 8 and 11 of U2405 are fed through inverter U2402C and U2402D to one input of decoder/driver disable gates U2402A and U2402B, respectively. The second input of each gate is driven to a high state by the Q output (pin 8) of FF U2408.

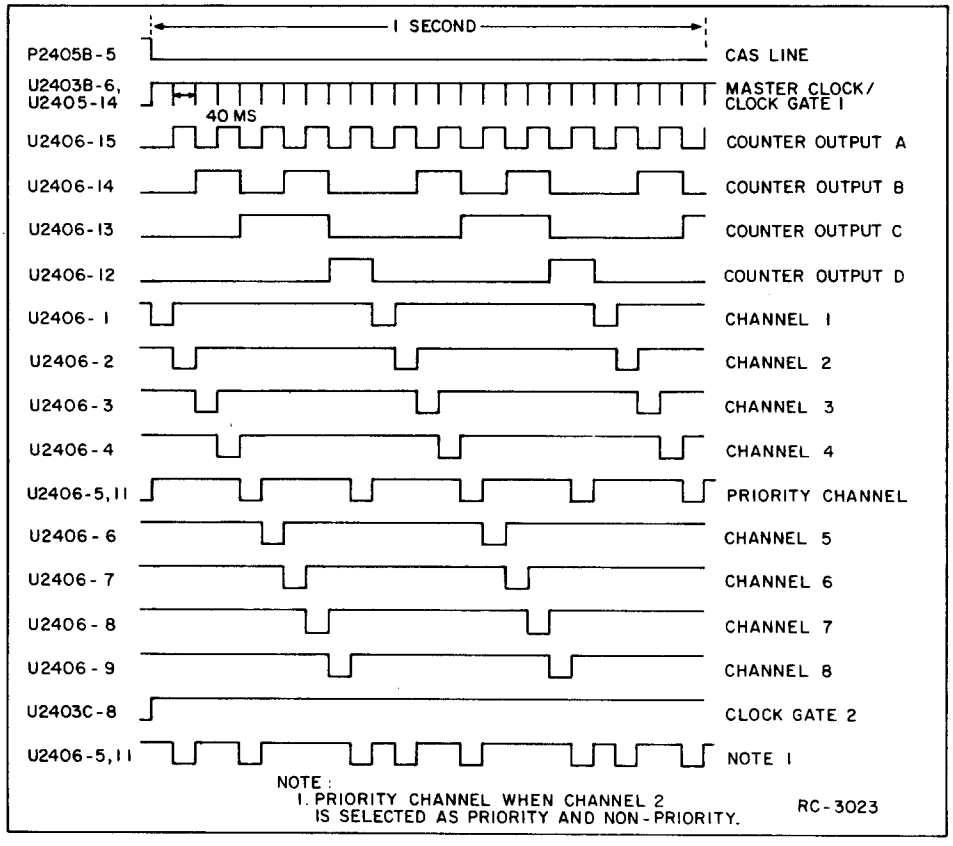

Figure 2 - Receiver Squelched, Eight Frequency Search Timing Diagram

(In this mode U2402A and B function as inverters). The Q output of the FF is forced to a high state by gate U2401C. This is achieved by the highs on pins 8 and 9 of U2401C to provide a low output on pin 10. Pin 10 of U2401C is connected to the SD (set direct) input of FF U2408 which causes the Q output of the FF to switch to the high state. This enables BCD outputs (on pins 9 and 11) from the decade counter to be applied in the proper time sequence to the decoder/driver. The decoder/driver sequentially grounds (applies a low) the frequency select lead of each selected non-priority channel.

The priority channel is searched on the fifth and tenth count for a duration of 40 milliseconds, (or 5 times per second). If the priority channel is also selected by a non-priority switch, the priority channel will be searched the number of times equal to the sum of the priority and non-priority channel search rates. This can be seen by superimposing the non-priority channel search time over the priority channel search time. For example, if channel 2 were selected as a non-priority channel and also as the priority channel it would be searched 8 times each second.

Four Frequency Search

To operate in the four or eight frequency search mode, the DA jumper interconnecting H2-H1 or H2-H3 must be connected properly. To operate in the four frequency mode the DA jumper is connected from H2-H3. A timing diagram for the four frequency search mode is shown in Figure 3.

NOTE

A four frequency 19D417678G1 PSLM board is not equipped to search 8 channels.

The four frequency PSLM reset gate, U2403A, is used to decode the fifth count (sixth state) of the counter. This provides time to search four channels plus the priority channel. A "1 0 1" state on the counter output pins 12, 9, and 8 respectively represent count 5. Count 5 is detected by ANDing the output of U2403A pins 12 and 8. The low output of reset gate U2403A is inverted by U2404A and applied to pins 2 and 3 of counter U2405, instantaneously resetting the counter to zero (channel 1 search). The reset pulse is present only long enough to reset the counter (approximately 50 nanoseconds) since the counter resets on the leading edge of the transition.

RECEIVING NON-PRIORITY

When a non-priority channel becomes active (signal received), the CAS line will go to +10 VDC. The PSLM will stop on that channel while monitoring the priority channel. The priority channel is monitored for 6-7 milliseconds at approximately 250 millisecond intervals (four times per second). If a signal is received on the priority channel while receiving the non-priority channel, the PSLM will transfer operation from the non-priority channel to the priority channel for the duration of the message. Refer to Figure 4 for the timing diagram for receiving non-priority channels.

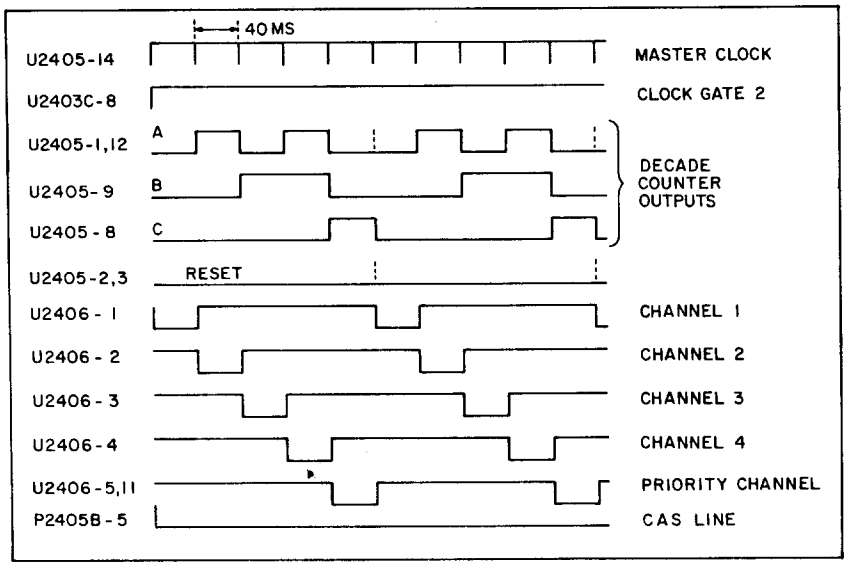

Figure 3 - Receiver Squelched, Four Frequency Search Timing Diagram

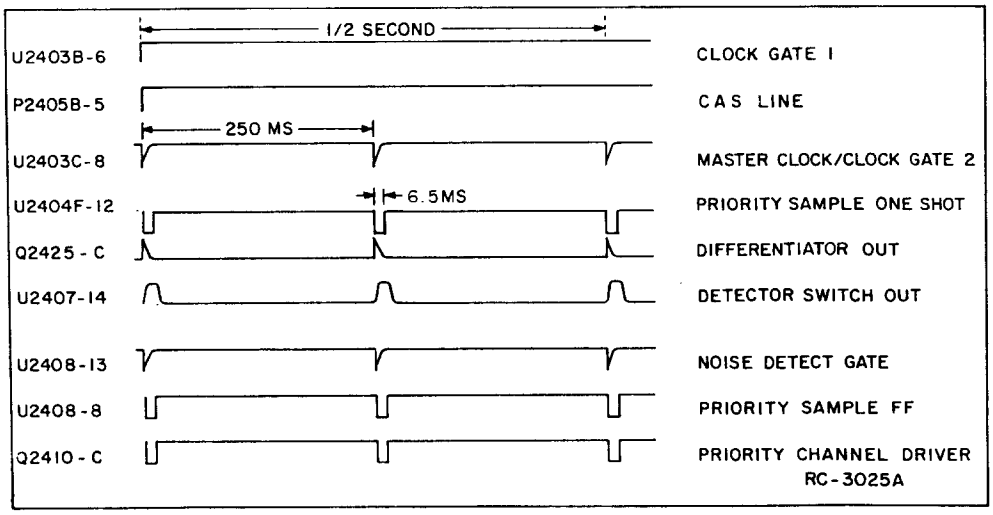

Figure 4 - Receiving Non-Priority Timing Diagram

When the CAS line goes high diodes CR2401, CR2402 and CR2410 in the diode isolation matrix are reverse biased. CAS switch Q2401 turns on, applying A+ to the base of clock gate 1 enable transistor Q2405. Q2405 turns on and applies A- to one input of clock gate 2, turning it off to stop the counter and decoder/driver on the active non-priority channel. It also applies A- to one input of priority control gate U2401C, causing its output (which is connected to the SD input of priority sample FF) to go high, thereby removing the set input to the priority sample FF. The priority sample FF, U2408, now operates under control of the trigger and SD inputs to monitor the priority channel at the proper time.

When receiving on a non-priority channel the positive voltage applied from CAS switch Q2401 turns on clock speed control transistor Q2406. When Q2406 conducts, diode switch CR2405 is reverse biased removing R2410 from its parallel connection across R2411, producing the slower clock speed. The master clock generator generates one negative going clock pulse every 250 milliseconds.

Clock gate 2 enable transistors Q2403 and Q2402 now switch states. With CR2402 reverse biased Q2402 turns on causing Q2403 to turn off, thereby removing A- from the enable input (pin 9) of clock gate 2. With the enable input now at +5V, the clock pulses are passed through to inverter U2404D and to the input of priority sample one-shot generator. The output of the inverter is used to trigger priority sample FF U2408.

Priority Sample FF

In the search mode, the Q output of priority sample FF U2408 was held high (+5V) by priority control gate U2401C and clock pulses were not applied to the trigger input. When receiving on a non-priority channel however, the priority control gate U2401C releases the SD input. Slow speed clock pulses (4 Hz) are applied to the trigger input of priority FF U2408.

FF U2408 changes state on the negative transition of the clock pulse and the Q output switches from +5V to near A-.

It remains in this state for approximately 6 milliseconds and goes positive coincident with the trailing edge of the priority sample pulse generated by the priority sample one-shot pulse generator. The positive transition is achieved by differentiating the priority sample pulse and ANDing it with the trailing edge of the noise detector output to assure the absence of a signal on the priority channel. The resulting negative pulse is applied to the SD (set direct) input of priority sample FF U2408. The Q output immediately goes high creating the 6 millisecond negative pulse. The Q output (pin 8) of U2408 goes low for a duration of 6 milliseconds once every 250 milliseconds. The pulse is inverted and applied to the MSB (most significant bit) inputs, pins 12 and 13, of decoder/driver U2406. This drives all decoder outputs high (no channels selected) each pulse period.

During each pulse period, the output of U2401A (high state) turns Q2410 on, which in turn places a ground on the priority channel frequency select lead. This allows the selected priority channel to be sampled 4 times per second while receiving a non-priority channel. If at the end of the 6 millisecond pulse period no signal is detected (noise pulse present), the priority channel noise detect gate (U2401D) is enabled by applying a negative output pulse to the SD input of the priority sample FF. This forces the Q output of the FF to a high state which enables the decoder/driver to reselect the active non-priority channel.

Priority Sample One-Shot and PSLM Hybrid

The 6 millisecond priority sample pulse is generated by OR gate U2403D, inverters U2404E, F and Q2409. When a signal is received on a non-priority channel, slow speed clock pulses from clock gate 2 are applied to one input of OR gate U2403D. The second input is high at this time. The negative transition of the input clock pulse is inverted by the OR gate and applied to inverter U2404E. The negative going output turns Q2409 off allowing the input of inverter U2404F to go high and its output low. (This is the negative going transition of the priority sample pulse). The low output of inverter U2404F is applied back to the input of OR gate U2403D holding its output high. Approximately 6 milliseconds later capacitor C2410 is charged up and allows Q2409 to turn on causing the output of inverter U2404F to go high (positive transition of priority sample pulse) and open the OR gate to the next clock pulse. At the same time the output of the OR gate is driven low (due to high's on both inputs) to complete the creation of a 6 millisecond pulse on the OR gate output.

At the same time, the positive going pulse is applied from the output of OR gate U2403D to pin 2 of U2407 (PSLM Hybrid). In the audio muting circuit, audio and noise from the receiver are coupled from pin 3 of U2407, through the audio muting coupling circuit to pin 4 of U2407. The positive pulse at pin 2 causes the priority channel audio to be muted during the priority channel search period. This prevents objectionable noise bursts from being heard at the speaker each time the priority channel is monitored. Refer to Figure 5 for a typical diagram of the PSLM Hybrid.

When the audio is muted, a negative going priority sample pulse is applied to the noise muting circuit and to the differentiator circuit (U2407-pin 9). The noise muting circuit applies audio and noise to the fast squelch circuit. The fast squelch circuit is comprised of the noise mute circuit, noise filter, noise amplifier, and detector switch. When the priority channel is not being monitored, audio and noise is shunted to ground by the noise mute circuit, thus the detector switch output is at ground potential. This inhibits the priority channel noise detect gate, U2401D.

The differentiator applies a positive spike at the end of the 6 millisecond period to the base of Q2423, turning it on. Q2423 turns Q2425 off. When Q2425 turns off, it applies a positive going pulse to one input of priority channel noise detect gate U2401D.

When the priority channel one-shot pulse occurs (searching priority channel begins), the negative going pulse turns the noise mute circuit off. While the noise mute circuit is turned off, the noise output of the noise filter is applied to the noise amplifier. The output of the noise amplifier is rectified and fed to the detector switch, turning it off. Turning the detector switch off, generates a positive going 10-12 millisecond pulse which is applied from U2407-pin 14 to one input of the priority channel noise detect gate (U2401D). Thus, with positive inputs on noise detect gate U2401D, a negative going pulse appears at its output. This negative pulse occurs coincident with the trailing edge of the priority pulse and is applied to the SD input of the priority sample FF. This sets the Q output of FF U2408 back to the high state and allows the decoder/driver to reselect the active non-priority channel. This cycle is repeated once every 250 milliseconds or until a priority channel becomes active.

When receiving a non-priority channel, the audio is attenuated approximately 4 dB by Q2414, 2413, and R2423. Normally, Q2413 is turned on, Q2414 is off and R2423 is in series with the Volume Hi (audio) lead from the PSLM, thus attenuating the non-priority audio.

Channel Indicators

CR2411 is reverse biased allowing a positive voltage to be applied to the base of all channel indicator drivers, Q2415–Q2422. This turns on the transistor corresponding to the active channel since only the transistor associated with the active channel will have its emitter returned to ground through the associated non-priority switch and decoder/driver U2406.

The LED indicator correspoding to the active non-priority channel will be on and blink off. The indicator for the priority channel is off and will flash on four times per second during the priority channel search time.

Priority Channel Transfer

If a priority signal is received during the 6 milliseconds search period, the priority signal quiets the receiver, inhibiting the operation of the fast squelch circuit in the PSLM hybrid so that the noise filter remains on. As a result, the detector switch remains on providing a ground at its output (pin 14). This inhibits the priority channel noise detect gate from generating a negative pulse to reset the priority sample FF.

The Q output then will remain near A-. This low is inverted by U2402A and B and applied to the decoder/driver, driving all channel driver outputs high (none selected). The CAS line remains high indicating receipt of the priority message. Therefore, clock gate 1 is still turned off and no

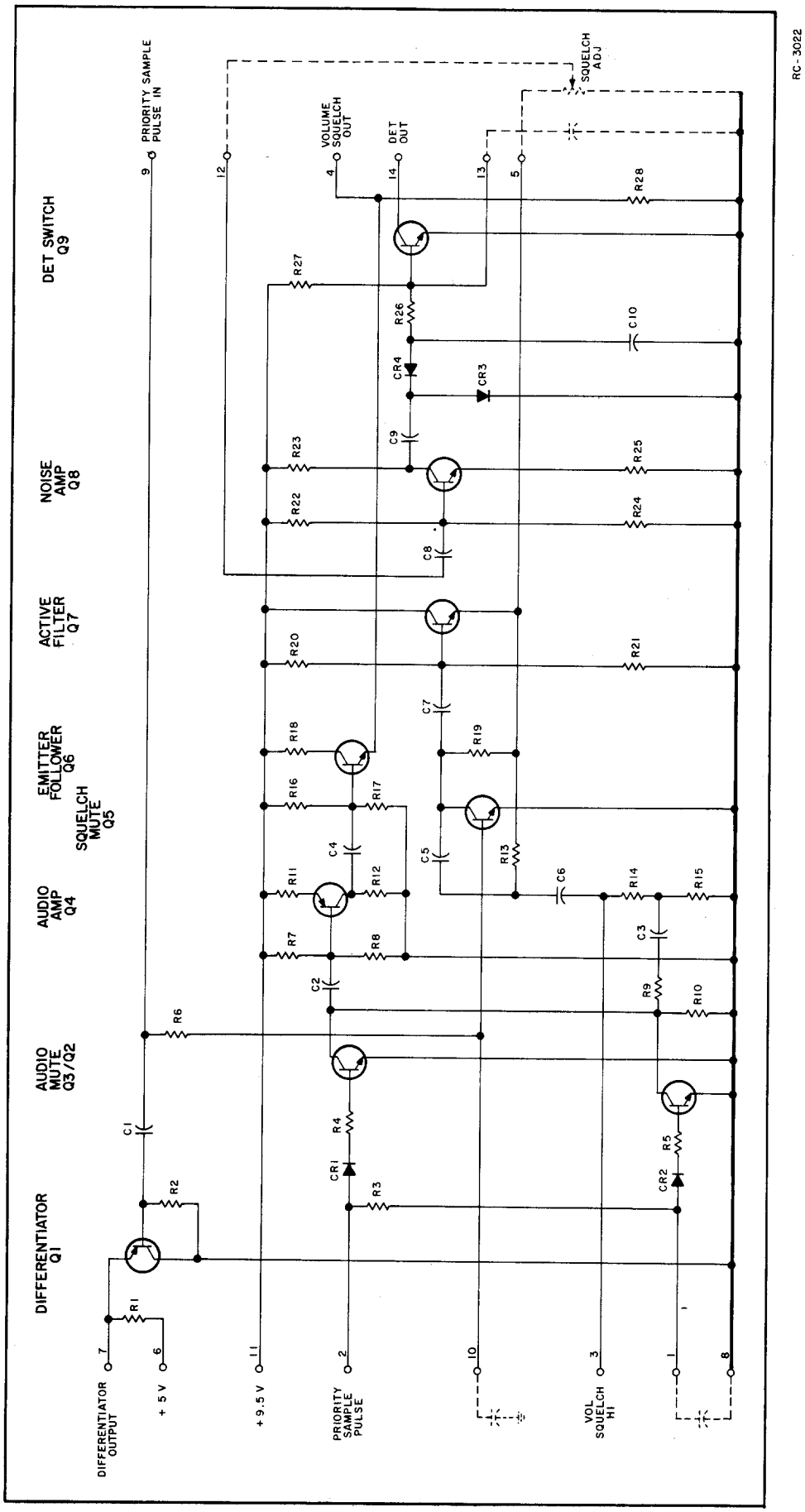

Figure 5 - Simplified Diagram PSLM Hybrid

clock pulses are applied to the decade counter. The counter then retains storage of the previously selected non-priority channel. At the same time the Q output of the priority sample FF is also applied through inverter U2401A to the base of priority channel driver Q2410. Q2410 turns on and drives the frequency select lead and the base of clock gate 2 enable transistor Q2402 low for the duration of the priority message.

Clock gate 2 enable switch Q2402 turns on inverter Q2403. Q2403 drives one input of clock gate 2 low inhibiting the slow speed clock pulses. This removes the trigger input from the priority sample FF locking it on the priority channel.

RECEIVING PRIORITY

In the search mode when a priority channel becomes active (receives signal), the decade counter (U2405) will latch onto the active channel. Refer to Figure 6, Receiving Priority. When the CAS lead goes high CAS switch Q2401 turns on and as a result turns on Q2405 which applies A- to the inhibit input of clock gate 1 (U2403B). This inhibits the gate, removing clock pulses to the decade counter. Clock pulses to the priority sample one-shot also are inhibited simultaneously when the frequency select lead is grounded by the decoder/driver. A low is applied through diode CR2404 to the base of Q2402, turning it off and as a result, turns Q2403 on. This inhibits clock gate 2, preventing clock pulses from triggering the priority sample FF and the priority sample one-shot generator.

The LED indicator will turn on and remain on. CR2411 is reverse biased, applying a positive voltage to the base of all indicator drivers. Only the emitter of the priority channel is returned to A- through decoder/driver U2406. Since both clock gates are turned off there is no priority sample pulse, therefore, the LED will not flash off but instead remain on at maximum brightness.

Audio Level Control

Priority channel driver Q2410 also applies A- to the base of audio level control transistor Q2413 turning it off. Q2413 turns Q2414 on to short out audio attenuator resistor R2423. This increases the audio output level of the priority channel by 4 dB with respect to the audio level of non-priority channels.

LOCKED PRIORITY OPERATION

Locked priority operation prevents the operator from selecting the priority channel. The priority channel is designated by the user and physically strapped to that channel; however, the strapping arrangement permits the priority channel to be reassigned as desired.

Circuit operation is the same as in the other modes of operation. Messages are transmitted over the channel indicated by the channel selector switch. The CAS delay circuit is disabled when the priority channel is locked on one channel (not selectable).

PUSH-TO-TALK OPERATION

When the push-to-talk line goes low (PTT switch pressed), A- is applied to the PTT delay circuit, master clock generator, CAS delay circuit, CAS switch, indicator drivers, clock gate 2 enable. This shuts down the master clock, shorts out CAS delay capacitor C2402, inhibits clock gate 2 and turns off all LED drivers.

NOTE

The PTT delay circuit is active only in systems equipped with Channel Guard. If Channel Guard is not used PTT delay capacitor C2408 is removed.

A- is applied to PTT delay switch Q2411 through diodes CR2408 and CR2409 reverse biasing CR2409. This causes Q2411 to turn off. When Q2411 stops conducting, its collector rises toward +5V. The base

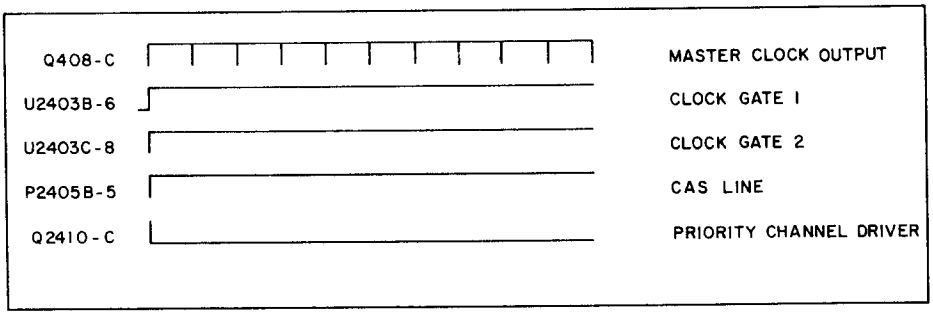

Figure 6 - Receiving Priority, Timing Diagram

of transmit channel driver transistor Q2412, which is connected through R2419 to the collector of Q2411, follows this rise in voltage and, when the rise in voltage exceeds the threshold, turns Q2412 on. Q2412 grounds the frequency select common lead and selects the frequency of the transmitter to be keyed through the channel selector switch. PTT delay control transistor Q2426 is turned off by the positive voltage applied to its base through R2456.

The positive voltage (high) on the collector of Q2411 is applied to inverters U2404B and U2401B. The low output of U2404B is applied to the CD (clear direct) input of priority sample FF U2408. This forces the Q output (pin 8) to a low state, which produces a high at the output of gates U2402A and U2402B. With highs on pins 12 and 13 of decoder/driver U2406, the decoder/driver outputs all are forced to the ones state. At the same time, the output of inverter U2401B is low keeping Q2410 off.

When the PTT switch is released, A- is removed from the junction of CR2408 and CR2409. The PTT dropout delay is controlled by R2417 and C2408. Approximately 250 milliseconds is required to charge C2408 to the point where PTT delay switch Q2411 will turn on (Q2411 is held off by the charging current of C2408). After this delay Q2411 starts to turn on, turning Q2426 on through C2418 which in turn drives Q2411 into saturation. At the same time transmit channel driver Q2412 is turned off, releasing the ground on the frequency select common lead.

The fast on/slow off action of the PTT delay circuit is required to maintain a ground on the frequency select common lead (holds transmitter oscillator module on) for the duration of the Channel Guard transmit phase reversal (for squelch tail elimination). If Channel Guard is not present, C2408 is removed and there is no delay from the time the PTT switch is released and PSLM resumes searching.

VOLTAGE REGULATOR

The 9.5V regulator consists of Q2424 and associated circuitry. It provides +9.5V to the PSLM Hybrid (U2407). Transistor Q2424 is a series regulator whose base-emitter voltage is held constant by zener diode VR2401 (10V zener). Q2424 can be considered as a voltage controlled variable resistor whose resistance varies with a change in collector voltage.

With the base-emitter voltage constant a drop in collector voltage will cause Q2424 to conduct harder, thereby reducing the voltage drop across the collector to emitter and maintaining a constant +9.5V at the emitter, conversely, an increase in collector voltage will decrease conduction of Q2424 which effectively increases the series resistance and prevents the emitter voltage from rising.

A 5-Volt regulator, VR2402, provides +5V to operate the remaining PSLM circuitry.

CHANNEL INDICATORS

The channel indicators (CR2 thru CR9) are backlighted at a low level when the SRCH switch is pressed in. Switched A+ is applied to the anode of each LED through contacts 4 and 6 of S2401. The cathodes are returned to A- through two series connected current limiting resistors. An LED driver transistor is connected across the 1K series resistor. In order for the transistor to turn on its emitter must be returned to A- (channel being searched) and its base positive (message being received). When this condition occurs the driver transistor turns on and shorts out the 1K current limiting resistor and allows the LED to glow at maximum brilliance.

When a non-priority channel is receiving a message the non-priority LED indicator will be on and blink off for 6 milliseconds 4 times a second while the opposite is true for the priority channel indicator. It will be off and flash on. This is caused by the emitters being removed and connected to A- during priority channel search time.

When a priority channel is receiving a message the associated LED will remain on at maximum brilliance.

INSTALLATION

CONTROL MODULE

- Remove the front panel of control unit.
- Remove control module as directed in control unit manual and cut or remove lettered DA wires (F, G & K) connected between H6-H60, H58-H59 and H72-H73 respectively. Re-install control module.

PSLM MODULE (in radios equipped with Channel Guard)

- Remove CAS delay capacitor C2402.

PSLM MODULE (in radios not equipped with Channel Guard)

- Remove PTT delay capacitor C2408.

After completing above circuit modifications, plug PSLM component board into appropriate option deck and replace front panel.

FIELD MODIFICATION

EIGHT CHANNEL PSLM 19D417678G2

The eight frequency PSLM may be modified to search only four channels, or if origin-

ally strapped for four channel operation, may be expanded to search eight channels. Lockout rivets behind the pushbuttons may be installed or removed to provide the desired number of searched channels. Connect a DA wire as indicated below to provide desired operation.

4-Channel Search	8-Channel Search
H2-H3	H1-H2

LOCKED PRIORITY

The priority channel is normally selectable from 1 through 8 channels but may be locked to a specific channel. For selectable priority operation a DA wire is connected between H4 and H5. For locked priority operation the DA wire connected between H4 and H5 is removed. A DA wire is then connected between H6 and H7-H14 as indicated on the Schematic Diagram.

CAS DELAY

The CAS delay capacitor (C2402) is present only in radios not equipped with Channel Guard. When Channel Guard is provided in radios equipped with PSLM, capacitor C2402 is removed.

PTT DELAY

The PTT delay function is used only in radios equipped with Channel Guard and is provided by C2408. If the radio is not equipped with Channel Guard C2408 is removed. If Channel Guard is field installed in a radio equipped with PSLM, C2408 must also be installed on the PSLM module. Refer to Schematic Diagram.

AUDIO ATTENUATOR

The audio attenuator operates on non-priority channels only. To disable the audio attenuator so that the audio level is the same for all channels connect a DA wire between H61 and H62.

PRIORITY DISABLE

The PSLM can be modified to operate without the PRIORITY function (Search Lock only). To disable the priority function on the PSLM board and revert to Search Lock Monitor operation, remove Q2402.

PSLM MODIFICATION
(DELTA-S, SX Application)

When using the Four/Eight Frequency PSLM with DELTA-S, SX radios, R2410 is removed and replace with R1 (Part No. 19A701250P369). R1 is:

Refer to Installation Instruction 19D800900.

MAINTENANCE & TROUBLESHOOTING

An optional extender board, 19D417773 is available for servicing the C-800 and C-900 series control units.

A troubleshooting procedure, including waveforms, is provided to aid the technician to isolate a malfunction.

A single adjustment control, R2415 (Priority Squelch) is contained on the PSLM module. Refer to the Troubleshooting Procedure to determine when adjustment of R2415 is necessary.

PRIORITY SQUELCH ADJUSTMENT

Priority Squelch Adjust R2415 is preset at the factory for 20-dB quieting sensitivity on the priority channel, and will normally require no further adjustment. If it should become necessary to readjust R2415 use the following procedure. Two signal generators (M560 or equivalent) with a three way 6-dB pad are required. Insert the PSLM board in the Option Module Extender board and plug into option deck.

1. Using frequency select switch, select F1 as the priority channel.
2. Select all of the non-priority channel pushbutton switches on the PSLM, except F1.
3. Apply a 1000 microvolt signal with standard modulation on F2 channel. Also apply a 20 dB quieting level (unmodulated) to F1 channel using the second generator.
4. Slowly turn priority squelch adjust control R2415 counterclockwise until the priority channel pre-empts the non-priority channel.
5. Respective channel select indicators should indicate priority take-over.

NOTE

The audio quality of the non-priority channel can best be checked with an unmodulated carrier or voice modulation. When the PSLM is on a non-priority channel, applying a constant tone to the receiver will result in a pulsed sound.

SYMPTOM	PROCEDURE
No receiver audio	1. Check the receiver in a different system (with or without PSLM). 2. Check waveforms at Test Points (N) and (M).
Fails to lock onto a non-priority channel	1. Check the setting of Priority Squelch Adjust R2415. 2. Check waveforms at Test Points (A), (D), (B), (T). Check waveform (J) for all selected channels. 3. Check system interconnections (refer to Interconnection Diagram in the Maintenance Manual for the control unit).
Does not transfer to priority channel	1. Check setting of Priority Squelch Adjust R2415. 2. Check voltage readings and waveforms at Test Points (A) (C) (E) (L) (K) (J) (P) (W) (R) (S) (T) and (U).
Incorrect channel assignment for locked priority or non-priority operation	1. Verify correct strapping for assigned channel. Refer to Schematic Diagram. 2. Check voltage readings and waveforms at Test Point (J) for all selected channels.
Missed syllables on the first part of transmissions	1. Check waveform at Test Point (A) for incorrect sample rate. Resistors R2416 and R2411 control the sample rate.
PSLM continues searching when PTT switch depressed	1. Check for 0.6V or less at junction of CR2405 and CR2422 and the anode side of CR2421. 2. Check test points (S), (T) and (U). 3. Verify proper operation of Q2407 and Q2408. 4. Check microphone.
Intermittent audio muting while receiving on a priority channel	1. Check waveforms and voltage levels at Test Points (C) and (E).

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WAVEFORMS

All waveforms are taken at Test Points (A) thru (W) as shown on the outline and schematic diagrams. When applicable, the waveforms are shown for three different modes of operation as follows:

1. Receiver Squelched (PSLM Searching)
2. Receiver Unsquelched (Receiving Non-Priority Channel)
3. Receiver Unsquelched (Receiving Priority Channel)

NOTE

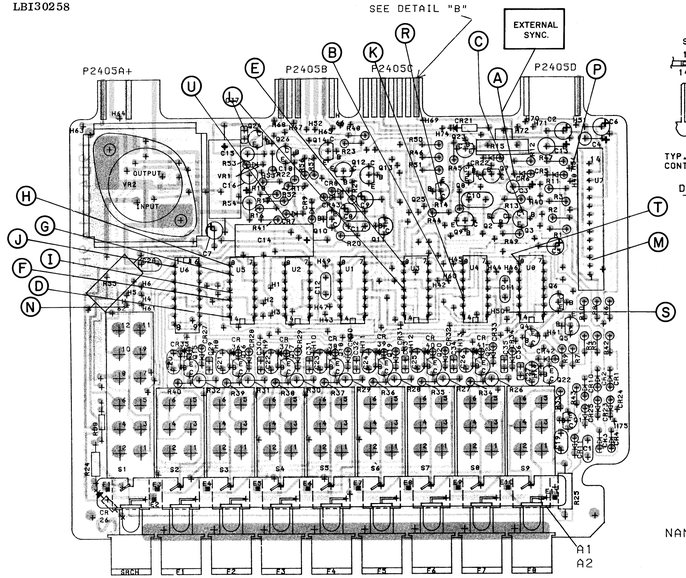
All waveforms are taken using Test Point A as the SYNC SOURCE (Trigger Pulse) except where NOTED.

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL	RECEIVING PRIORITY CHANNEL
A	 10ms/Div. 2V/Div.	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div.
B	 10ms/Div. 2V/Div.	 10ms/Div. 2V/Div.	 10ms/Div. 2V/Div.
C	 10ms/Div. 2V/Div. NOTE: INTERNAL SYNC	 50ms/Div. 2V/Div.	 10ms/Div. 2V/Div.
D	 10ms/Div. 2V/Div.	 10ms/Div. 2V/Div.	 10ms/Div. 2V/Div.
E	 10ms/Div. 2V/Div.	 50ms/Div. 2V/Div.	 10ms/Div. 2V/Div.

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL	RECEIVING PRIORITY CHANNEL
F	 50ms/Div. 2V/Div. NOTE: SYNC TEST POINT J	"0" OR 4 VOLTS (DEPENDS ON STATE OF COUNTER WHEN CAS LINE GOES HIGH)	"0" OR 4 VOLTS (DEPENDS ON STATE OF COUNTER WHEN CAS LINE GOES HIGH)
G	 50ms/Div. 2V/Div.	"0" OR 4 VOLTS (DEPENDS ON STATE OF COUNTER WHEN CAS LINE GOES HIGH)	"0" OR 4 VOLTS (DEPENDS ON STATE OF COUNTER WHEN CAS LINE GOES HIGH)
H	 50ms/Div. 2V/Div.	"0" OR 4 VOLTS (DEPENDS ON STATE OF COUNTER WHEN CAS LINE GOES HIGH)	"0" OR 4 VOLTS (DEPENDS ON STATE OF COUNTER WHEN CAS LINE GOES HIGH)
I	 50ms/Div. 2V/Div.	"0" OR 4 VOLTS (DEPENDS ON STATE OF COUNTER WHEN CAS LINE GOES HIGH)	"0" OR 4 VOLTS (DEPENDS ON STATE OF COUNTER WHEN CAS LINE GOES HIGH)
J	 50ms/Div. 2V/Div. NOTE: INTERNAL SYNC	 50ms/Div. 2V/Div. NOTE: +4.5 V WHEN NOT RECEIVING	"0" V WHEN RECEIVING PRIORITY +4.5 V WHEN RECEIVING NON-PRIORITY
K	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div.
L	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div.

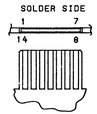
TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL	RECEIVING PRIORITY CHANNEL
M	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.
N	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.
P	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.
R	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.	
S	 2ms/Div. 2V/Div.	2ms/Div. 2V/Div.	2ms/Div. 2V/Div.

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL	RECEIVING PRIORITY CHANNEL
T	50ms/Div. 2V/Div.	50ms/Div. 2V/Div.	50ms/Div. 2V/Div.
U	50ms/Div. 2V/Div.	50ms/Div. 2V/Div.	50ms/Div. 2V/Div. NOTE: WHEN RECEIVING OR SEARCHING PRIORITY CHANNEL
U			50ms/Div. 2V/Div. NOTE: WHEN PRESSING PTT SWITCH
V	2ms/Div. 2V/Div.	2ms/Div. 2V/Div.	2ms/Div. 2V/Div.
W	2ms/Div. 2V/Div.	2ms/Div. 2V/Div.	



(19A144139, Sh. 1, Rev. 0)
(19A144139, Sh. 2, Rev. 1)
(BC-3029A)

SOLDER SIDE



TYP. NUMBERING OF CONTACT FINGERS.

DETAIL "B"

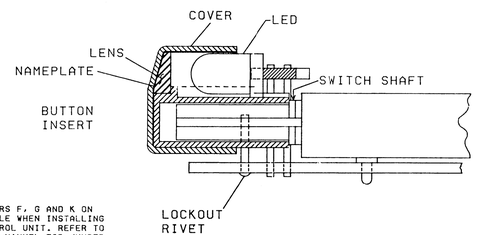
LEAD IDENTIFICATION FOR Q2401 THRU Q2426

IN-LINE
TOP VIEW

NOTE: CASE SHAPE, IS DETERMINING FACTOR FOR LEAD IDENTIFICATION.

CONNECTION CHART			
FROM	TO	WIRE	
H53	H48	ST22-W	
H41	H60	ST22-W	
H43	H42	ST22-W	
H40	H44	DA	
H47	H54	ST22-W	
H45	H46	DA	
H50	H49	ST22-W	
H52	H51	ST22-W	
H4	H5	DA	
H1	H2	DA	GROUP 2 ONLY
H2	H3	DA	GROUP 1 ONLY
H74	H75	ST22-W	

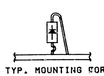
RUNS ON SOLDER SIDE
RUNS ON BOTH SIDES
RUNS ON COMPONENT SIDE



(19D424430, Rev. 7)

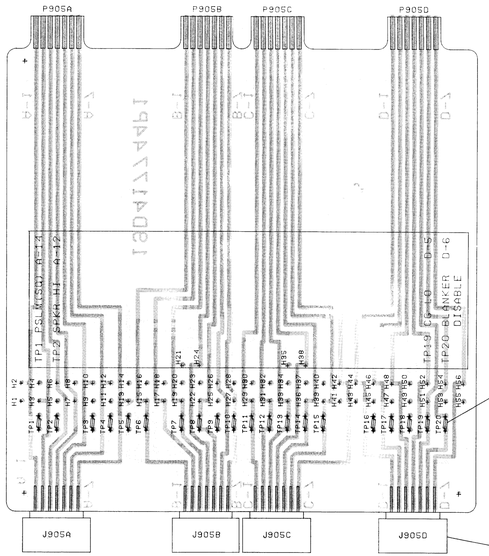
OUTLINE DIAGRAMS

FOUR-EIGHT FREQUENCY
PRIORITY SEARCH LOCK MONITOR
AND EXTENDER BOARD



TYP. MOUNTING FOR CR2401 THRU CR2443

NOTE:
1. REMOVE JUMPERS F, G AND K ON CONTROL MODULE WHEN INSTALLING PSLM IN CONTROL UNIT. REFER TO CONTROL UNIT MANUEL FOR JUMPER INDENTIFICATION.

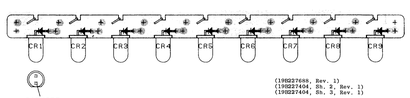


(19D424431, Rev. 0)
(19B226451, Sh. 2, Rev. 0)
(19B226451, Sh. 3, Rev. 0)

TYP. MOUNTING FOR CR2427 THRU CR2434

SOLDER SIDE
TYP. NUMBERING OF CONTACT FINGERS.
DETAIL "A"

SPRING 19B211379P1



(19B227608, Rev. 1)
(19B227404, Sh. 2, Rev. 1)
(19B227404, Sh. 3, Rev. 1)

VOLTAGE READINGS

All voltage readings are DC readings measured with a 20,000 ohm-per-volt VOM with reference to system negative. The readings are taken with F1 assigned as the priority channel.

NOTE

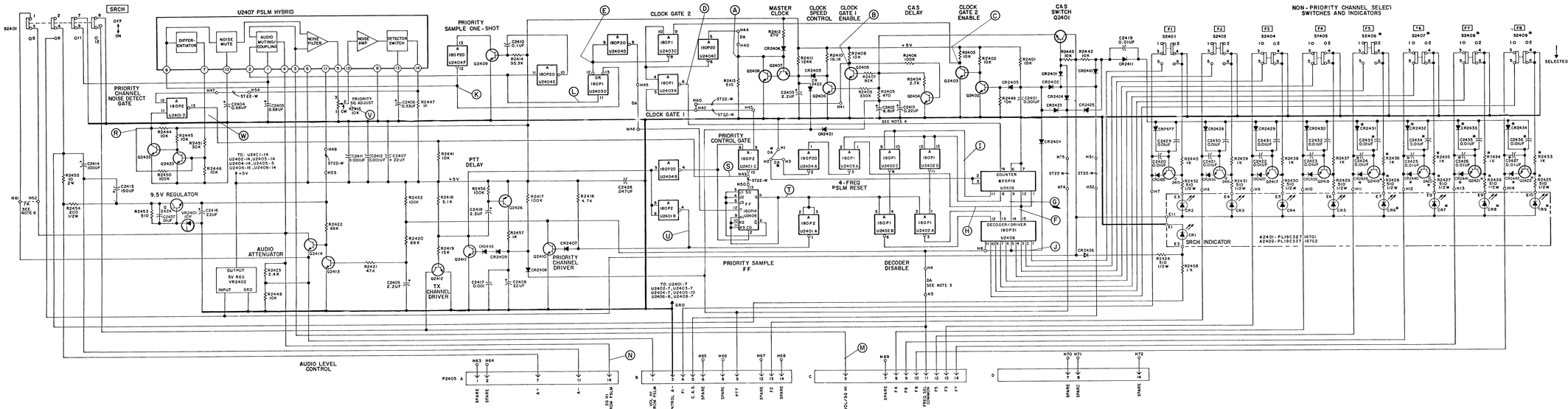
Readings followed by a (P) are averages of pulsating meter deflections. These readings may vary widely due to the differences in meter ballistics, but may be used to determine that the circuit is operative (or switching) and not at a DC or ground potential.

Preliminary Checks

NOTE - Voltages are nominal

1. Check for +9.5 volts at C2416 (+).
2. Check for +5 volts at C2407 (+).
3. Check for +5 volts at pin 14 of all IC's except U2407-6, U2405 and U2406. Check pins U2405-5 and U2406-16 for 5.0 volts.
4. Check for ground (A-) at pin 7 of all IC's except U2407-8, U2405 and U2406. Check pins U2405-10 and U2406-8 for A-.

Test Point	Reading with Receiver Squelched	Reading with Receiver Unsquelched (on Non-Priority Channel)	Reading with Receiver Unsquelched (on Priority Channel)
A	2.8V	2.8V	2.8V
B	4.4V	0.2V	0.2V
C	0.2V	4.8V	0.2V
D	4.0V	4.0V	4.0V
E	4.0V	3.8V	4.0V
F	1.5V (P)	4.0V or 0.2V	4.0V or 0.2V
G	1.5V (P)	4.0V or 0.2V	4.0V or 0.2V
H	1.5V (P)	4.0V or 0.2V	4.0V or 0.2V
I	0.7V (P)	4.0V or 0.2V	
J	5.0 (P) Lower	0.6 (P) Higher	0.2V
K	4.0V	3.2V (P)	4.0V
L	0.2V	0.3V (P)	0.2V
M	4.5V	4.5V	4.5V
N	4.5V	4.0V	4.0V
P	0.2V	0.5V (P)	0.2V
R	0.2V	0.3V (P)	0.2V
S	0.2V	3.2V (P)	0.2V
T	4.0V	3.6V (P)	4.0V
U	0.2V	0.0 (P)	0.2V
V	0.8V	0.8V	0.8V
W	0.6V	0.7V (P)	0.6V



(1S852D89, Rev. 21)
(RC-3029A)

THIS ELEM DIAG APPLIES TO		
MODEL NO.	REV LETTER	NO. FREQ
19C327B7502	K	4
19D417B7502	M	8
19C327B7701		4
19C327B7702		8

IN ORDER TO RETAIN RATED EQUIPMENT PERFORMANCE, REPLACEMENT OF ANY SERVICE PART SHOULD BE MADE ONLY WITH A COMPONENT HAVING THE SPECIFICATIONS SHOWN ON THE PARTS LIST FOR THAT PART.

NOTES:
1. ■ PRESENT IN GROUP 1 (4 FREQ) ONLY
2. ▪ PRESENT IN GROUP 2 (8 FREQ) ONLY
3. FOR LOCKED PRIORITY OPERATION REMOVE JUMPER FROM W4 TO W5 AND CONNECT W4 PCB TABLE 1.
4. TO DISABLE C.A.S. DELAY, REMOVE CR2402. THE C.A.S. DELAY IS NOT USED WHEN CHANNEL GUARD IS PRESENT.
5. *WHEN CHANNEL GUARD IS NOT USED, REMOVE C2401 TO DISABLE PTT DELAY.
6. TO DISABLE NON-PRIORITY AUDIO ATTENUATOR, REMOVE JUMPER FROM W10 AND W12.
7. ALL RESISTORS ARE 1/8 WATT UNLESS OTHERWISE SPECIFIED. ALL RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY K=KILOHMS OR M=MEGOHMS. ALL CAPACITOR VALUES IN MICROFARADS (MFD) UNLESS FOLLOWED BY UF=MICROFARADS, INDUCTANCE VALUES IN MICROHENRYS UNLESS FOLLOWED BY MH=MILLIHENRYS OR HENRYS.

TABLE I (SEE NOTE 3)

LOCKED CHANNEL	SOLDER LEAD FROM	TO
1	H7	H1
2	H8	H2
3	H9	H3
4	H10	H4
5	H11	H5
6	H12	H6
7	H13	H7
8	H14	H8

SCHEMATIC DIAGRAM

FOUR-EIGHT FREQUENCY
PRIORITY SEARCH LOCK MONITOR

PARTS LIST

LBI30259F

8 FREQUENCY PRIORITY SEARCH LOCK MONITOR
19D417678G1 4 FREQUENCY
19D417678G2 8 FREQUENCY

SYMBOL	GE PART NO.	DESCRIPTION
A2401 and A2402		CHANNEL INDICATOR BOARD 19C327167G1 4 FREQUENCY 19C327167G2 8 FREQUENCY
		- - - - - - - DIODES AND RECTIFIERS - - - - - - -
CR1 thru CR9	19A134354P7	Diode, optoelectronic: yellow: sim to Hew. Packard 5082-4555.
		- - - - - - - - - - CAPACITORS - - - - - - - - -
C2401	19A700233P7	Ceramic: 1000 pF ±20%, 50 VDCW.
C2402	5496267P218	Tantalum: 6.8 uF ±10%, 35 VDCW, sim to Sprague Type 150D.
C2403	5496267P413	Tantalum: 2.2 uF ±5%, 20 VDCW; sim to Sprague Type 150D.
C2404 and C2405	5496267P229	Tantalum: 0.68 uF ±10%, 35 VDCW; sim to Sprague Type 150D.
C2406	5496267P227	Tantalum: 0.33 uF ±10%, 35 VDCW; sim to Sprague Type 150D.
C2407	5496267P10	Tantalum: 22 uF ±10%, 15 VDCW, sim to Sprague Type 150D.
C2408	5496267P210	Tantalum: 22 uF ±10%, 15 VDCW, sim to Sprague Type 150D.
C2409	5496267P213	Tantalum: 2.2 uF ±20%, 15 VDCW, sim to Sprague Type 150D.
C2410	19A702059P13	Polyester: 0.1 uF ±5%, 50 VDCW.
C2411 and C2412	19A700233P7	Ceramic: 1000 pF ±20%, 50 VDCW.
C2413	5496267P26	Tantalum: 0.22 uF ±20%, 35 VDCW; sim to Sprague Type 150D.
C2414	5496267P16	Tantalum: 100 uF ±20%, 20 VDCW; sim to Sprague Type 150D.
C2415	5496267P12	Tantalum: 150 uF ±20%, 15 VDCW; sim to Sprague Type 150D.
C2416	5496267P10	Tantalum: 22 uF ±20%, 15 VDCW; sim to Sprague Type 150D.
C2417	19A700233P7	Ceramic: 1000 pF ±20%, 50 VDCW.
C2418	5491674P44	Tantalum: 2.2 uF ±20%, 15 VDCW; sim to Sprague Type 162D.
C2419 thru C2427	19A700234P7	Polyester: 0.01 uF ±10%, 50 VDCW.
C2428*	19A700234P11	Polyester: 0.047 uF ±10%, 50 VDCW.
		In REV G & earlier:
	19A116080P1	Polyester: 0.01 uF ±20%, 50 VDCW.
C2429 thru C2436	19A116192P1	Ceramic: 0.01 uF ±20%, 50 VDCW; sim to Erie 8121 Special.
C2437*	19A116192P1	Ceramic: 0.01 uF ±20%, 50 VDCW; sim to Erie 8121 Special. Added by REV G.
C2438*	19A116192P1	Ceramic: 0.01 uF ±20%, 50 VDCW; sim to Erie 8121 Special. Added by REV J. Deleted by REV K.
		- - - - - - - DIODES AND RECTIFIERS - - - - - - -
CR2401 thru CR2411	19A115250P1	Silicon, fast recovery, 225 mA, 50 PIV.
CR2421 thru CR2434	19A115250P1	Silicon, fast recovery, 225 mA, 50 PIV.
CR2435* thru CR2442*	19A115250P1	Silicon, fast recovery, 225 mA, 50 PIV. Added by REV F.
CR2443*	19A115250P1	Silicon, fast recovery, 225 mA, 50 PIV. Added by REV L.
		- - - - - - - - - - TERMINALS - - - - - - - - - -
E1 thru E11	19A116779P4	Contact, electrical: sim to Molex 08-50-0401.
		- - - - - - - - - - TRANSISTORS - - - - - - - - -
Q2401 thru Q2406	19A115910P1	Silicon, NPN; sim to Type 2N3904.
Q2407	19A115852P1	Silicon, PNP; sim to Type 2N3906.
Q2408 thru Q2425	19A115910P1	Silicon, NPN; sim to Type 2N3904.
Q2426	19A115852P1	Silicon, PNP; sim to Type 2N3906.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R2401 thru R2403	19A700106P87	Composition: 10K ohms ±5%, 1/4 w.
R2404	19A700106P73	Composition: 2.7K ohms ±5%, 1/4 w.
R2405	19A700106P55	Composition: 470 ohms ±5%, 1/4 w.
R2406	19A700106P111	Composition: 100K ohms ±5%, 1/4 w.
R2407	19A700106P109	Composition: 82K ohms ±5%, 1/4 w.
R2408	19A700106P87	Composition: 10K ohms ±5%, 1/4 w.
R2409	3R152P334J	Composition: 0.33 megohms ±5%, 1/4 w.
R2410	19A701250P328	Metal film: 19.1K ohms ±1%, 1/4 w.
R2411	19A701250P410	Metal film: 124K ohms ±1%, 1/4 w.
R2412	19A700106P49	Composition: 270 ohms ±5%, 1/4 w
R2413	3R152P511J	Composition: 510 ohms ±5%, 1/4 w.
R2414	19A701250P395	Metal film: 95.3K ohms ±1%, 1/4 w.
R2415	19B209358P106	Variable, carbon film: approx 300 to 10K ohms ±10%, 1/4 w; sim to CTS Type X-201.
R2416*	19A700106P79	Composition: 4.7K ohms ±5%, 1/4 w.
		In REV D & earlier:
	3R152P103J	Composition: 10K ohms ±5%, 1/4 w.
R2417	19A700106P111	Composition: 100K ohms ±5%, 1/4 w.
R2418	3R152P512J	Composition: 5.1K ohms ±5%, 1/4 w.
R2419	19A700106P91	Composition: 15K ohms ±5%, 1/4 w.
R2420	19A700106P107	Composition: 68K ohms ±5%, 1/4 w.
R2421	19A700106P103	Composition: 47K ohms ±5%, 1/4 w.
R2422	19A700106P107	Composition: 68K ohms ±5%, 1/4 w.
R2423	3R152P242J	Composition: 2.4K ohms ±5%, 1/4 w.
R2424 thru R2432	3R77P511J	Composition: 510 ohms ±5%, 1/2 w.
R2433 thru R2440	19A700106P63	Composition: 1K ohms ±5%, 1/4 w.
R2441 thru R2446	19A700106P87	Composition: 10K ohms ±5%, 1/4 w.
R2447*	19A700106P63	Composition: 1K ohms ±5%, 1/4 w.
		In REV L & earlier:
	19A700106P87	Composition: 10K ohms ±5%, 1/4 w.
R2448	19A700106P87	Composition: 10K ohms ±5%, 1/4 w.
R2449*	19A700106P87	Composition: 10K ohms ±5%, 1/4 w.
		In REV J & earlier:
	3R152P104J	Composition: 100K ohms ±5%, 1/4 w.
R2450	19A700106P111	Composition: 100K ohms ±5%, 1/4 w.
R2451	3R152P303J	Composition: 30K ohms ±5%, 1/4 w.
R2452*	19A700106P111	Composition: 100K ohms ±5%, 1/4 w.
		In REV J & earlier:
R2453*	3R152P303J	Composition: 30K ohms ±5%, 1/4 w.
		In REV C & earlier:
	3R152P511J	Composition: 510 ohms ±5%, 1/4 w.
R2454	19A700113P46	Composition: 200 ohms ±5%, 1/2 w.
R2455	19A700111P15	Composition: 10 ohms ±5%, 2 w.
R2456	19A700106P111	Composition: 100K ohms ±5%, 1/4 w.
R2457 and R2458	19A700106P63	Composition: 1K ohms ±5%, 1/4 w.
		- - - - - - - - - - SWITCHES - - - - - - - - - -
S2401	19B233625G1	Push button, 4 PDT contacts rated 1.1 amps at 14 VDC; sim to Switchcraft 14F-5323C.
S2402 thru S2409	19B233625G2	Push: 4PDT; a station, contacts rated 1.1 amp at 14 VDC; sim to Switchcraft 14S-5321C.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - -
U2401	19A116180P2	Digital: QUAD 2-INPUT NAND GATE. (OPEN COLLECTOR).
U2402 and U2403	19A116180P1	Digital: QUAD 2-INPUT NAND GATE
U2404	19A116180P20	Digital: HEX INVERTER.
U2405	19A116820P19	Digital: DECADE COUNTER.
U2406	19A116180P31	Digital: BDC-TO-DECIMAL DECODER/DRIVER.
U2407	19D424078G1	Hybrid: Mute PSLM.
U2408	19A116180P14	Digital: J-K MASTER-SLAVE FLIP-FLOP.
		- - - - - - - - VOLTAGE REGULATORS - - - - - - -
VR2401	4036887P11	Silicon, zener.
VR2402	19A116834P1	Linear: 5 volt regulator; sim to Microamp 209K.
		- - - - - - - - - MISCELLANEOUS - - - - - - - - -
	19B226398P2	Heat sink. (Used with VR2402).
	19A130148P1	Insulator. (Used with VR24020.
	19C321004P1	Lens. (Used with S2401-S2409).
	19B226331P1	Insert. (Used with S2401-S2409).
	19B226334P1	Cover. (Used with S2401-S2409).
	N276459P10	Nameplate. (SRCH).
	N276459P11	Nameplate. (F1).
	N276459P12	Nameplate. (F2).
	N276459P13	Nameplate. (F3).
	N276459P14	Nameplate. (F4).
	N276459P15	Nameplate. (F5).
	N276459P16	Nameplate. (F6).
	N276459P17	Nameplate. (F7).
	N276459P18	Nameplate. (F8).
		ASSOCIATED ASSEMBLIES
		DIODE KIT 19A144974G1
	19A115250P1	Diode, silicon, fast recovery, 225 mA, 50 PIV.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter," which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by these revisions.

REV. A, B, C - PSLM Board 19D417678G1, G2
Incorporated in initial shipment.

REV. D - To reduce audio distortion. Changed R2453.

REV. E - To ensure PSLM lock on priority channel. Changed R2416.

REV. F - To improve operation. Added CR2435 thru CR2438 on group 1 boards and CR2435 throu CR2442 on group 2 boards.

REV. G - To improve operation. Added C2437.

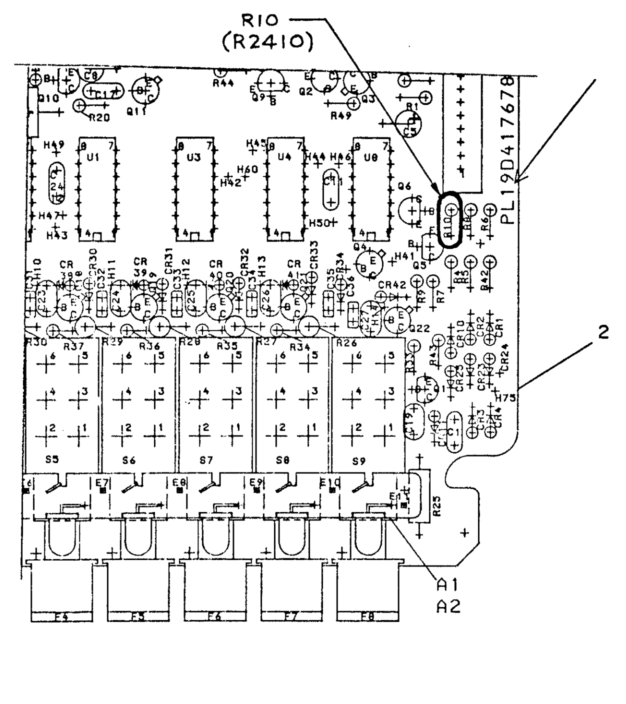
REV. H - To prevent oscillation on 5 Volt Buss. Changed C2428.

REV. J - Eliminate noise burst in search mode. Added C2438.

REV. K - Eliminate noise burst in search mode. Changed R2449 and R2452. Deleted C2438.

REV. L - To make compabile with DTMF encoder. Added CR2443.

REV. M - To assure priority channel seizes the receiver. Changed R2447.



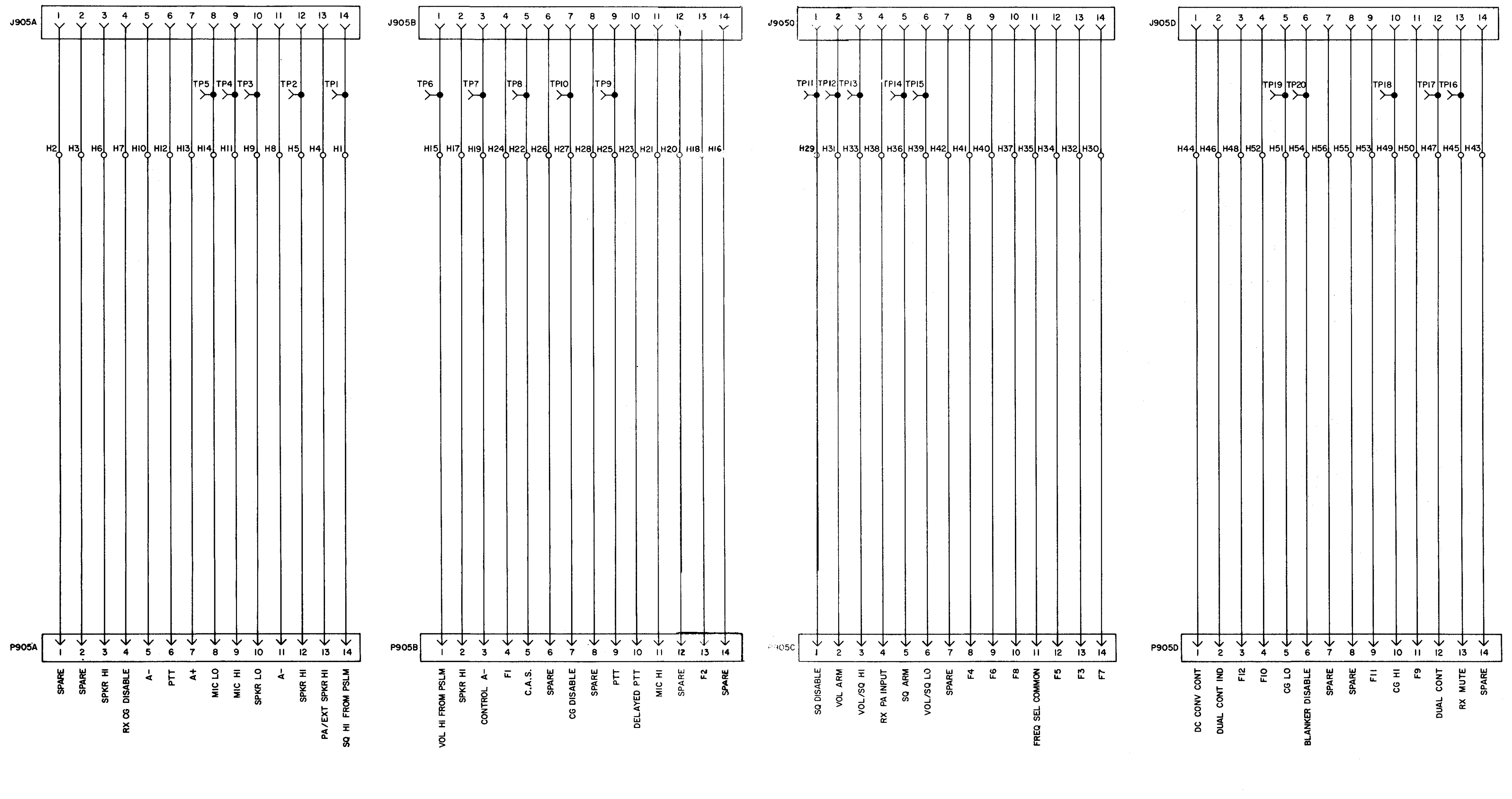
(19B800900, Rev. 1)

①

1. REMOVE R2410 FROM 19D417678G1 4 FREQUENCY PSLM BOARD.
2. REPLACE R2410 WITH R1 (19A701250P369) FROM PL19A702612.

PSLM MODIFICATION INSTRUCTIONS
(DELTA, DELTA - S APPLICATION)

SCHEMATIC DIAGRAM



(19R622088, Rev. 1)

THIS ELEM DIAG APPLIES TO	
MODEL NO	REV LETTER
PL19D417773	

SCHEMATIC DIAGRAM

EXTENDER BOARD

Issue 1