



MAINTENANCE MANUAL
138-174 MHz PHASE LOCK LOOP EXCITER 19D423249G1 & G2

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DESCRIPTION

The Phase Locked Loop (PLL) Exciter is a crystal controlled, frequency modulated, wideband exciter designed for multi-frequency operation (1 through 8) with wide channel spacing in 138-174 MHz frequency band. The wideband exciter utilizes a phase locked loop to provide a maximum transmitter frequency spacing of up to 17 MHz in the 138-155 MHz range or up to 24 MHz in the 148-174 MHz range. The frequency range is determined by the response of the plug-in bandpass filter and the core in L101. The solid state exciter uses integrated circuits (IC's) and discrete components to provide 250 milliwatts of RF power to the PA assembly. The exciter is used in standard and Voice Guard applications.

The operating frequency is selected by the channel selector switch on the control unit and is determined by the FM ICOM associated with the selected channel. The crystal frequencies range from approximately 11.5 to 14.5 MHz and are one-twelfth the RF carrier frequency. Oscillator stability is maintained within $\pm 0.0005\%$ or $\pm 0.0002\%$.

Except for individual frequency trimmer adjustments on the FM ICOMS and the modulation controls, only one tuning control, L101, in the voltage controlled oscillator (VCO) circuit, is used to center tune the exciter for all operating frequencies. For this reason, a centralized metering jack to monitor exciter operation is not applicable. The exciter RF output power is metered by the PA metering jack.

The PLL exciter utilizes the divided VCO frequency (Countdown train), phase detector, and a feedback path to lock the

output frequency of the VCO to the 12th multiple of the FM ICOM frequency.

CIRCUIT ANALYSIS

The phase detector compares the 3rd harmonic of the FM-ICOM with the output frequency of the VCO (divided by 4) to derive an error voltage proportional to the frequency and phase difference of the two inputs. The error voltage is amplified, passed through a lead/lag filter and applied to a varactor which instantaneously corrects the output frequency and phase of the VCO to the 12th multiple of the FM ICOM frequency.

After the VCO frequency is locked, (a maximum of 20 milliseconds), the RF amplifiers are turned on and the RF carrier output is presented to the PA.

Temperature compensation is provided in the audio and voltage regulator circuits to assure frequency stability and distortion free communications over the specified operating temperature range.

References to symbol numbers mentioned in the text are found on the block diagram, schematic diagram, outline diagram and parts list. Figure 1 is a block diagram of the PLL exciter.

Audio, supply voltages and control functions are connected from the system board to the exciter board through P902.

The PLL exciter contains up to eight FM ICOMs, an Audio processor and amplifier, bandpass filter, harmonic amplifier, phase lock loop, RF amplifiers, frequency lock detector, voltage regulators and temperature compensation circuits.

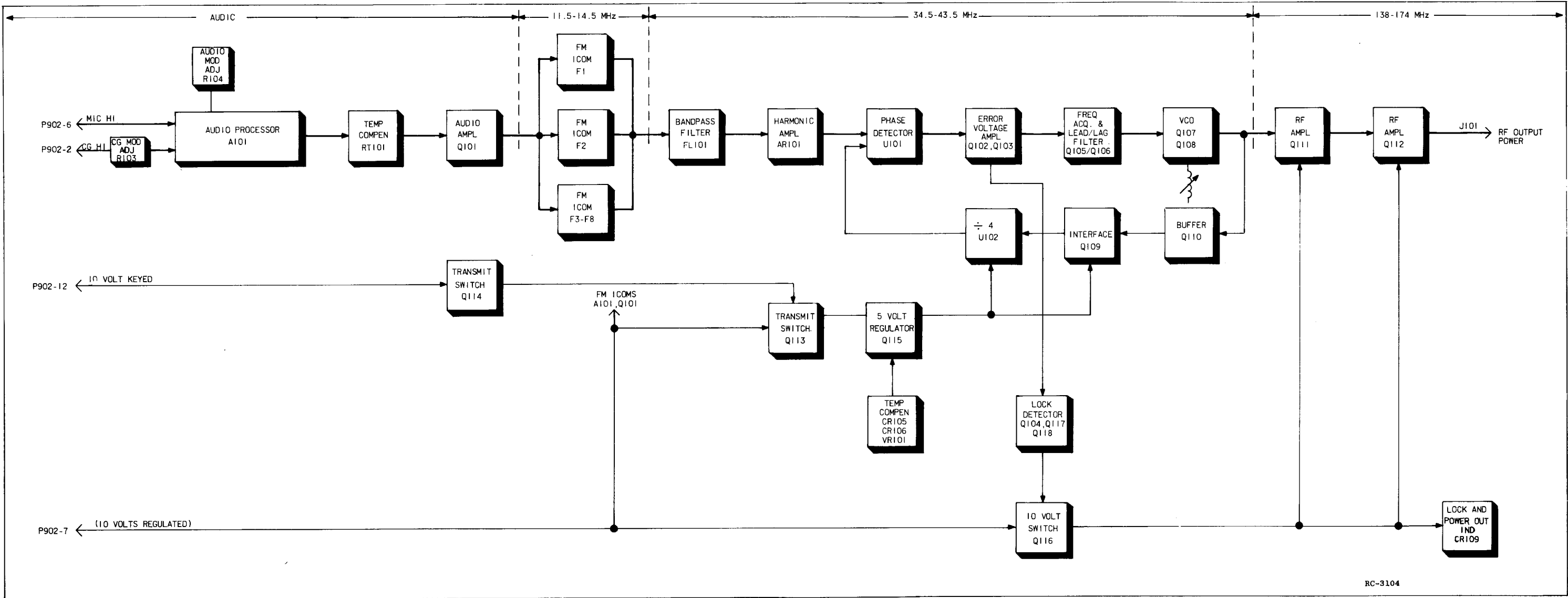


Figure 1 - Block Diagram

FM ICOMS (Frequency Modulated)

Three different types of FM ICOMs are available for use in the exciter. Each ICOM contains a crystal-controlled Colpitts oscillator, and two of the ICOMs contain compensator ICs. The different FM ICOMs are:

- 5C-FM ICOM - contains an oscillator and a 5 part-per-million ($\pm 0.0005\%$) compensator IC. Provides compensation for EC-ICOMs.
- EC-FM ICOM - contains an oscillator only. Requires external compensation from a 5C-ICOM.
- 2C-FM ICOM - contains an oscillator and a 2 PPM ($\pm 0.002\%$) compensator IC. Will not provide compensation for an EC-FM ICOM.

The ICOMs are enclosed in an RF shielded can with the type ICOM (5C-FM ICOM, EC-FM ICOM or 2C-FM ICOM) printed on the top of the can. Access to the oscillator trimmer is obtained through a hole in the top of the can.

Frequency selection is accomplished by switching the ICOM keying lead (terminal 9) to A- by means of the frequency selector switch on the control unit. In single-frequency radios, a jumper from H9 to H10 in the control unit connects terminal 9 of the FM ICOM to A-. The oscillator is turned on by applying a keyed +10 Volts to the external oscillator collector load resistor, R153, which forward biases an internal diode switch.

The FM ICOMs have an audio input which receives audio from the audio processor circuit. Therefore, with Modulation present, the output frequency of the "FM" ICOM varies at an audio rate.

CAUTION

All ICOMs are individually compensated at the factory and cannot be repaired in the field. Any attempt to repair or change the ICOM frequency will void the warranty.

In standard 5 PPM radios using EC-FM ICOMs, at least one 5C-FM ICOM or 5C ICOM must be used. The 5C ICOM is normally used in the receiver F1 position, but can be used in any receive position. A 5C-FM ICOM can be used in any transmit position.

NOTE

The EC and 5C type ICOMs are not interchangeable with EC-FM or 5C FM type ICOMs. The EC and 5C type ICOMs are used only in the receivers. While the EC-FM and 5C-FM type ICOMs are always used in the transmitter.

One 5C ICOM or 5C-FM ICOM can provide compensation for up to 15 EC ICOMs or EC-FM ICOMs in the transmitter and receiver. Should the 5C ICOM or the 5C-FM ICOM compensator fail in the open mode, the EC-FM ICOMs will still maintain 2 PPM frequency stability from 0°C to 55°C ($+32^{\circ}\text{F}$ to 131°F) due to the regulated compensation voltage (5 Volts) from the 10 Volt regulator IC. If desired, up to 8 5C-FM ICOMs may be used in the radio.

The 2C-FM ICOMs are self-compensated at 2 PPM and will not provide compensation for EC-FM ICOMs.

Oscillator Circuit

Quartz crystals used in ICOMs exhibit the traditional "S" curve characteristics of output frequency versus operating temperature.

At both the coldest and hottest temperatures, the frequency increases with increasing temperature. In the middle temperature range (approximately 0°C to 55°C), frequency decreases with increasing temperature.

Since the rate of change is nearly linear over the mid-temperature range, the output frequency change can be compensated by choosing a parallel compensation capacitor with a temperature coefficient approximately equal to and opposite that of the crystal.

Figure 2 shows the typical performance of an uncompensated crystal as well as the typical performance of a crystal which has been matched with a properly chosen compensation capacitor.

At temperatures above and below the mid-range, additional compensation must be introduced. An externally generated compensation voltage is applied to a varactor (voltage-variable capacitor) connected in parallel with the crystal. Refer to Figure 3 for a simplified diagram of the FM ICOM.

A constant bias of 5 Volts (provided from Regulator IC U901 connected in parallel with the compensator) maintains varactor capacity at a constant value over the entire mid-temperature range. This compensation voltage achieves the ± 2 PPM stability.

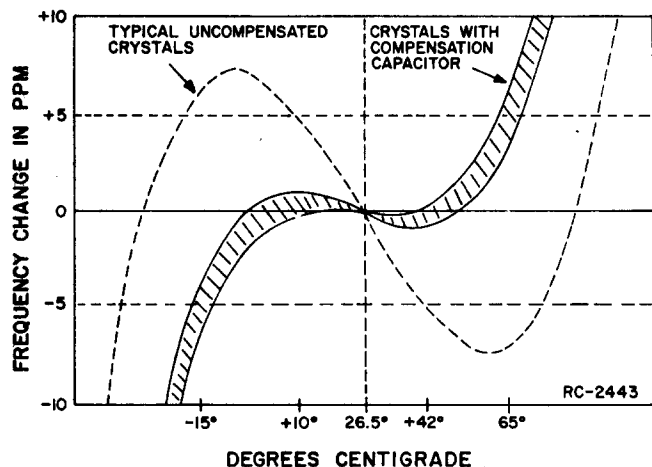


Figure 2 - Typical Crystal Characteristics

Modulation is accomplished with a hyperabrupt varicap connected in series with the crystal feedback capacitors. The varicap impedance is the dominant impedance in the loop. This allows large swings of load capacity with modulation, therefore, large frequency shifts are achieved for the modulated input. Biasing for the modulation varicap is provided by a voltage divider, R152 and R163, connected across the 10 volt regulator input at P902-7. A bias voltage of 6.2 volts is applied to pin 6 of all ICOMs.

Compensator Circuits

Both the 5C-ICOMs and 2C-FM ICOMs are temperature compensated at both ends of the temperature range to provide instant frequency compensation.

The cold end compensation circuit does not operate at temperatures above 0°C. When the temperature drops below 0°C, the circuit is activated. As the temperature decreases, the equivalent resistance decreases and the compensation voltage increases.

An increase in compensation voltage decreases the capacitance of the varactor in the oscillator, thereby increasing the output frequency of the ICOM.

The hot end compensation circuit does not operate at temperatures below +55°C. When the temperature rises above +55°C, the circuit is activated. As the temperature increases, the equivalent resistance decreases and the compensation voltage decreases. The decrease in compensation voltage increases the capacity of the varactor, decreasing the output frequency of the ICOM.

SERVICE NOTE

Proper ICOM operation is dependent on the closely-controlled input voltages for the 10-Volt regulator. Should all of the ICOMs shift off frequency, check the 10-Volt regulator module.

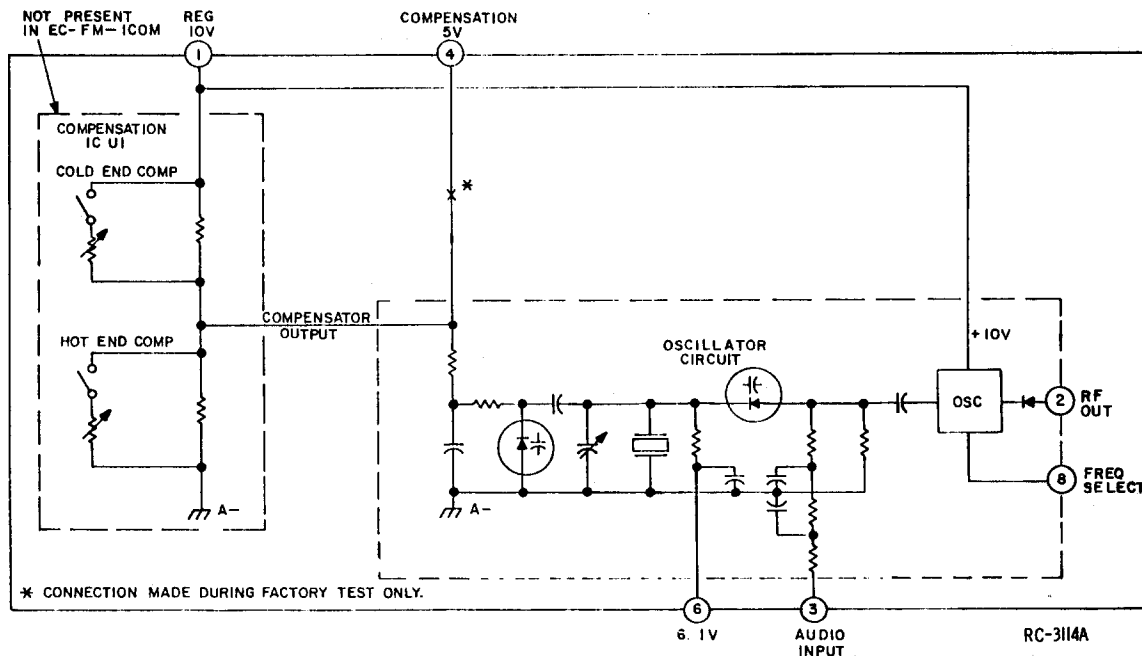


Figure 3 - Equivalent FM-ICOM Circuit

AUDIO PROCESSOR A101

The transmitter audio processor contains audio circuitry consisting of two operational amplifiers, AR101-A and -B, a pre-emphasis circuit with amplitude limiting and a post limiter filter. A total gain of approximately 24 dB is realized through the audio processor. Twenty dB is provided by AR101-B and 4 dB by AR101-A.

The 10 Volt regulator powers the audio processor and applies regulated +10 V thru P902-6 to a voltage divider consisting of R108 and R110. The +5 V output from the voltage divider establishes the operating reference point for both operational amplifiers. C107 filters out any noise that may be on the 10 Volt line to assure a stable voltage supply to the operational amplifiers.

Resistors R105, R106, and R107 and diodes CR101 and CR102 provide limiting for AR101-B. Diodes CR101 and CR102 are reverse biased by +5 VDC on AR101B-6 and voltage divider network R105, R106 and R107. The voltage divider network provides +7 VDC at the cathode of CR101 and +3 VDC at the anode of CR102. C102 and C103 permit a DC level change between AR101B-7 and the voltage divider network for diode biasing.

When the input signal at AR101B-6 is of a magnitude such that the amplifier output at AR101B-7 does not exceed 4 volts P-P, the amplifier provides a nominal 20 dB gain. When the audio signal level at AR101B-7 exceeds 4 volts PP, diodes CR101 and CR102 conduct on the positive and negative half cycles providing 100% negative feedback to reduce the amplifier gain to 1. This limits the audio amplitude at AR101B-7 to 5 volts PP.

Resistors R102, R103, and R104 and C104 comprise the audio pre-emphasis network that enhances the signal to noise ratio. R104 and C104 control the pre-emphasis curve below limiting. R103 and C104 control the cut-off point for high frequency pre-emphasis. As high frequencies are attenuated, the gain of AR101 is increased.

Audio from the microphone is applied to the audio processor at P102-1 and coupled to the input of operational amplifier AR101-B through R101 and C101.

The amplified output of AR101-B is coupled through P102-4 audio MOD ADJ control R104, R102-3, C106, R112 and R113 to a second operational amplifier AR101-A. Audio MOD ADJ control is set for a deviation of 4.5 kHz.

The Channel Guard tone input is applied to the audio processor through

P902-2, CG MOD ADJ R103 to P102-5. The CG tone is then coupled through C105 and R111 to AR101A-2 where it is combined with the microphone audio. AR101-A provides a signal gain of approximately 4 dB.

A post limiter filter consisting of AR101A, R112-R114, C108, and C109 provide 12 dB per octave roll off. R109 and C111 provide an additional 6 dB per octave roll off for a total of 18 dB.

SERVICE NOTE

R112-R114 are 1% resistors. This tolerance must be maintained to assure proper operation of the post limiter filter. Use exact replacements.

The output of the post limiter filter is coupled through C110 and P102-9 to the temperature compensated audio amplifier Q101.

AUDIO AMPLIFIER, BANDPASS FILTER, AND HARMONIC AMPLIFIER

The output of the audio processor is presented to audio amplifier Q101 through temperature compensator and biasing network consisting of RT101, R108 and R109. RT101, with a nominal resistance of 50 ohms from 25°C to 70°C, maintains a constant modulation index over the normal operating temperature range. The resistance of RT101 increases with a decrease in temperature below 25°C, thereby decreasing the signal drive to audio amplifier Q101. Audio amplifier Q101 has a nominal gain of 2. The temperature compensated audio is applied to pin 3 of the FM ICOM. A varactor within the FM ICOM is used to modulate the carrier frequency at the audio rate. The output of the FM ICOM is taken from pin 2 and applied to the bandpass filter.

The bandpass filter is a passive device with sharp frequency cutoff characteristics that pass only the 3rd harmonic. The fundamental frequency and all other harmonics are suppressed by at least 30 dB. The 3rd harmonic is amplified by high frequency harmonic amplifier AR101. The harmonic amplifier circuit has a high input impedance and provides a nominal power gain of 10. The output of AR101 is presented to pin 4 of phase detector U101 in the phase lock loop. Bandpass filter 19B226748G1 is used for frequencies between 138-155 MHz while bandpass filter 19B226748G2 is used for frequencies between 148-174 MHz.

PHASE LOCK LOOP

Phase detector U101, error voltage amplifier Q102 and Q103, frequency

acquisition and lead/lag filter circuit Q105 and Q106, voltage controlled oscillator circuit (VCO) Q107 and Q108, buffers Q109 and Q110, and frequency divider U102 form a phase locked loop. The PLL locks the VCO frequency to the 12th multiple of the FM ICOM frequency to provide the RF carrier output frequency. The phase locked loop locks the output of the VCO in frequency and in phase.

Phase detector U101 is a doubly-balanced modulator used to detect the difference (frequency and phase) between the divided frequency from the VCO and the 3rd harmonic of the FM ICOM and to provide a resultant error voltage output. The error voltage is directly proportional to the frequency/phase error.

When the frequency input from VCO (+4) is exactly the same as the frequency received from the harmonic amplifier, the output of the phase detector will be 8.0 VDC. If the two input signals are not at the same frequency, the output of the phase detector will be a DC voltage with an AC component equal to the difference frequency. This error voltage is amplified and applied to the VCO to correct and lock the VCO to the operating frequency. Biasing of the phase detector is arranged so that both inputs must be present for normal operation. Lack of either input will cause the voltage at U101-6 to rise to its maximum value (approximately 8.2 VDC).

DIFFERENTIAL ERROR VOLTAGE AMPLIFIER

Q102 and Q103 comprise a differential amplifier pair. Q103 is the reference amplifier that establishes the operating point against which error voltage amplifier Q102 operates. The operating point is established by a biasing network consisting of R127, R128, and C128. The differential amplifier pair translates the error signal and amplifies it to a level large enough to control the VCO. The error voltage detected by the phase detector is amplified by Q102 and applied to the emitter of reference amplifier Q103. The collector voltage of Q103 varies in proportion to the error voltage. When there is no frequency or phase error, there will be no varying error voltage. The collector voltage of Q103 is determined by its biasing network and the frequency assignments and spacing of the assigned transmitting frequencies. This voltage may be stable over a range of 3.4 to 6.4 Volts. A second output from the error voltage amplifier (taken from Q102-C) is applied to the lock detector (Q104, Q117, and Q118) to control the RF Amplifiers.

Lock detector/DC threshold control R171 controls the threshold level differential amplifier Q102, providing compensation for different output characteristics of U101. It is set for 1.8 \pm 0.1 VDC as measured at Q102-C (top of R129) with the transmitter keyed and an unused channel selected.

NOTE

R171 is preset at the factory and normally does not require field adjustment. However, if Q102, Q103, or U101 is replaced, readjustment may be necessary.

ACQUISITION CIRCUIT AND LEAD/LAG FILTER

The acquisition circuit consists of Q105 and Q106. The lead/lag filter circuit consists of R133, R135, R168, C129, and C130.

The lead/lag network controls the loop phase to provide frequency and phase stability and sets the bandwidth to about 20 kHz. The output of the differential error voltage amplifier is applied to the lead/lag filter. The lead/lag filter corrects the phase of the error signal applied to varactor CR102 to maintain loop stability. The varactor alters the frequency and phase of the VCO to stabilize the VCO at the RF output frequency.

During initial acquisition (when the transmitter is first keyed), the error signal from the differential error voltage amplifier will contain useful information far outside the normal bandwidth of the phase locked loop. For this reason, the acquisition circuit consisting of Q105 and Q106 is used to greatly increase the bandwidth. When an error signal with high frequency components is present and that has sufficient amplitude, either Q105 or Q106 will turn on. Q105 has the capability of increasing the voltage applied to varicap CR102 to a nominal 8.5 V while Q106 has the capability of lowering the varicap voltage to less than 1 Volt. This wide range of voltage being applied to varicap CR102 permits large and instantaneous frequency range. As the free running frequency of the VCO approaches the operating frequency, Q105 or Q106 turns off to permit final acquisition and phase lock. Frequency acquisition, and RF power output occurs in less than 20 milliseconds after the Tx lead is keyed.

Test point TP101 monitors the voltage applied to the varicap and is used to optimize the VCO frequency over the operating range.

NOTE

When adjusting the VCO voltage, always be sure to use a high impedance meter (10 megohm input impedance minimum).

The voltage at TP101 varies directly with frequency, (as the voltage increases, the frequency increases) and may range from +3.4 V to 6.4 V; however, the normal operating voltage is optimized around +5.0 V.

VCO (VOLTAGE CONTROLLED OSCILLATOR)

The VCO consists of two FET's, Q107 and Q108, connected in a cascade configuration with total feedback through C137 to provide instantaneous starts. The VCO operates over the output frequency range of 138-174 MHz. The free running frequency of the VCO is adjusted by L101 and is optimized by center tuning the free running frequency (TP101 at +5 V) between the highest and lowest operating frequencies. One of two cores are used in L101 to adjust the frequency (voltage) measured at TP101. One core is used for the 138-155 MHz range (ferrite) and a second core (aluminum) is used for the 148-174 MHz range.

BUFFER, INTERFACE AND FREQUENCY DIVIDER

RF output power from the VCO is taken from Q107 through a 4:1 step down transformer T101 and applied to the RF Amplifier and the feedback leg of the phase lock loop. The feedback leg of the phase lock loop consists of buffer Q110, interface Q109, and frequency divider U102.

The input to buffer Q110 is coupled through isolating resistor R139 and capacitor C148. Biasing for Q110 is provided by R149 and R150. The output of Q110 is taken from the collector and coupled through C149 to the base of emitter follower interface transistor Q109. Biasing for Q109 is provided by a voltage divider network consisting of CR104, R145, and R146. The output of interface transistor Q109 is taken from the emitter and applied directly to the input of frequency divider U102. The frequency divider divides the VCO frequency (assigned operating) by 4 and supplies it as the second input to the phase detector. The output of the frequency divider is compared in frequency and phase with the 3rd harmonic of the selected FM-ICOM frequency to maintain the VCO output frequency at the 12th multiple of the FM ICOM frequency. Operating voltage for interface transistor Q109 and frequency divider Q102 is provided by a temperature compensated +5 Volt regulator, Q115.

RF AMPLIFIERS

The wideband RF Amplifiers, Q111 and Q112, supply a minimum of 250 milliwatts of RF power at the carrier frequency to the power amplifiers. Q111 receives its input from the 4:1 step down transformer through coupling capacitor C138. It is biased for Class A operation by a biasing network consisting of R140 and R141.

The output of Q111 is taken from the collector and coupled to class C amplifier Q112 through L104 and C130. The RF Amplifier provide 250 milliwatts of RF power to J101 through L105 and C142.

DC power for the RF Amplifiers is controlled by 10 Volt switch Q116 and is not applied until the VCO output frequency is stable and locked on frequency.

LOCK DETECTOR AND 10 VOLT SWITCH

The lock detector monitors the operation of the differential error voltage amplifier and turns the RF Amplifiers on when the VCO is locked on frequency or turns them off if the VCO begins to vary or if one of the inputs to the phase detector is missing.

The lock detector consists of voltage doubler CR107, CR108, and C127, DC switch Q104, and Schmitt trigger Q117 and Q118.

When the VCO frequency is not locked with the FM ICOM frequency, the phase detector output at U101-6, instead of being a stable DC level (≈ 8.0 Volts), will be a DC level with an AC component varying at the beat (difference) frequency of the two inputs. The AC component is rectified by the voltage doubler, filtered by C169 and R162. The resultant DC voltage turns on DC switch Q104, lowering the base voltage of Schmitt trigger Q117. Q117 then turns off, allowing the base voltage of 10 volt switch Q116 to increase and turn it off. With Q116 turned off, +10 V is removed from the RF amplifiers, thereby removing the RF input to the PA. The collector of Q117 is also tied back to the base of Q118, the second stage of the Schmitt trigger. The increase in base voltage at Q118 causes it to turn on and raise the emitter voltage of Q117. With an increase in emitter voltage, Q117 is held off. The lock detect and control circuits and the RF amplifiers will remain in this state until the VCO achieves stability and is locked on frequency. The two inputs to the phase detector must be synchronous for normal operation.

When either of the two inputs to the phase detector is absent, the phase detector output will increase to approximately +8.2 Volts due to pull up

resistor R121. The increase in base voltage turns differential error voltage amplifier Q102 off causing the collector of Q102 to decrease to A- through R125. A- from the collector of Q102 is applied through R129 to the base of Schmitt trigger Q117, causing Q117 to turn off. With Q117 turned off, the base voltage of Q116 increases to near +10 V causing Q116 to turn off and remove voltage from RF Amplifiers Q111 and Q112.

Normally, Q117 is in the on condition, which allows 10 Volt switch Q116 to conduct and apply voltage to the RF amplifiers. RT102 in the base circuit of Q117 provides a temperature compensated reference for Q117 over the normal operating temperature range. The value of RT102 is approximately 2200 ohms.

LOCK DETECT INDICATOR

Lock detect indicator LED CR109 monitors the state of 10 Volt switch Q116. When Q116 is on and power is applied to the RF Amplifiers indicator CR109 is on. When the VCO voltage at TP101 is varying, or when one of the two inputs to the phase detector is lost, Q116 is switched off and indicator CR109 is out.

TRANSMIT SWITCH

The transmit switch applies +10 Volts to the exciter when the PTT switch

is operated. It consists of control transistor Q114 and 10 Volt switch Q113.

When the PTT switch is operated, +10 V (keyed) is applied to the base of Q114, turning it on. The collector of Q114 goes low turning 10 Volt switch Q113 on. Q113 controls the 10 Volt regulated input to the +5 Volt temperature compensated regulator Q115, pin 2 of the FM ICOMs, AR101, U101, Q102 and Q103, Q105 and Q106, and Q107 and Q108. 10 Volt regulated input power is applied directly to 10 Volt switch Q116, controlling the RF Amplifiers, pin 10 of all FM ICOMs, A101 and Q101.

+5 VOLT REGULATOR

The +5 Volt regulator receives a regulated 10 Volt input from Q113 and supplies a temperature compensated +5 Volt output to buffer interface transistor Q109 and frequency divider U102. A 4.4 Volt zener diode VR101 and two series connected diodes (CR105 and CR106) having a positive temperature coefficient comprise the temperature compensating network.

NOTE

Due to the temperature compensation characteristics of CR105 and CR106, only exact replacement diodes should be used. See parts list.

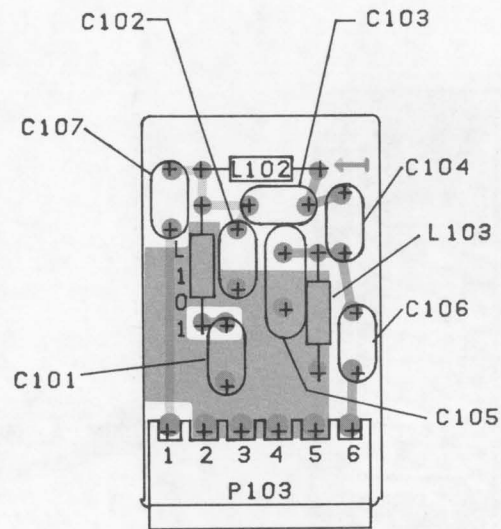


GE Mobile Communications

General Electric Company
Lynchburg, Virginia 24502

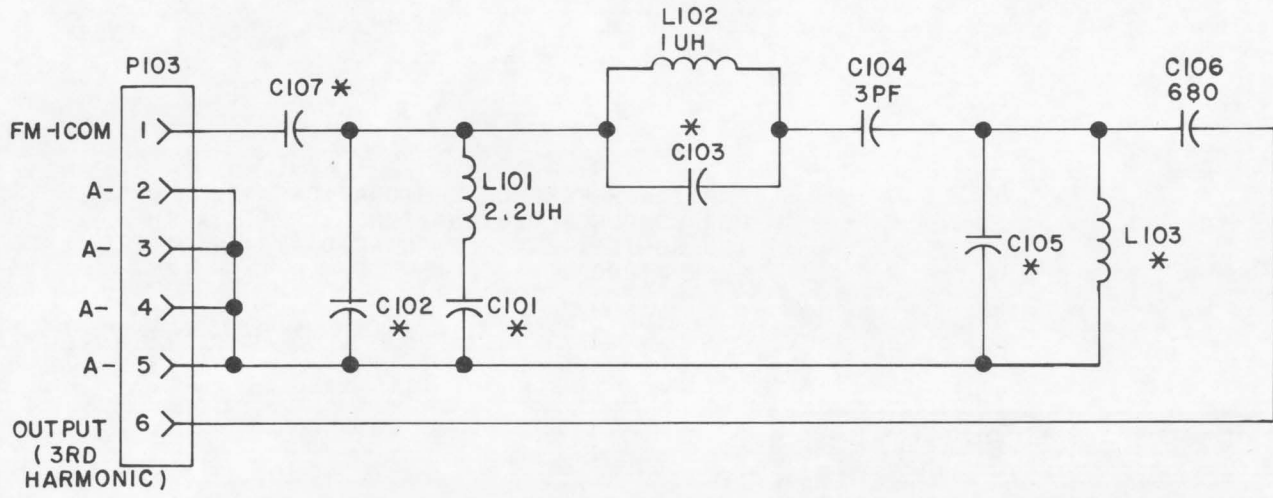
Printed in U.S.A.

OUTLINE DIAGRAM



(19B227783, Rev. 1)
(19B226746, Sh. 1, Rev. 1)
(19B226746, Sh. 2, Rev. 1)

SCHEMATIC DIAGRAM

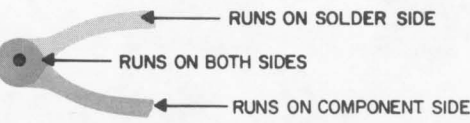


* COMPONENT VALUE CHART		
	138-155 MHZ(L)▲	148-174MHZ(H)▲
C101	15 PF	12 PF
C102	18 PF	15 PF
C103	15 PF	12 PF
C105	56 PF	51 PF
C107	10 PF	9 PF
L103	0.33UH	.27 UH

BANDPASS FILTER	REV LETTER	FREQUENCY RANGE
19B226748G1		138-155MHZ▲
19B226748G2		148-174MHZ▲

▲ TRANSMITTER OUTPUT FREQUENCIES

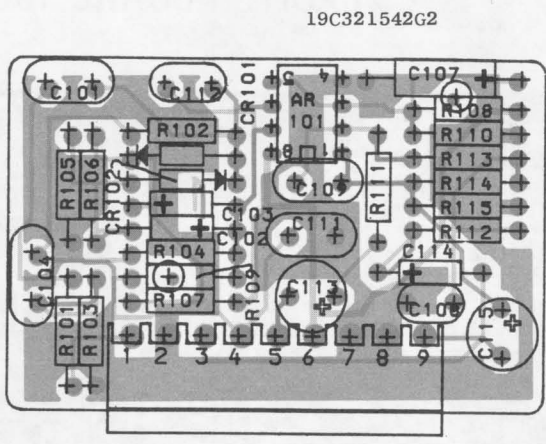
(19B227106, Rev. 3)



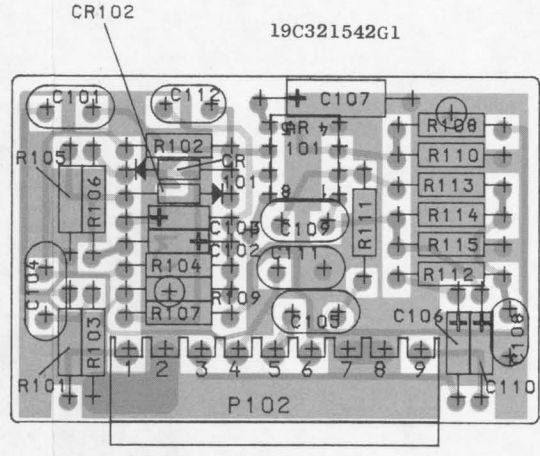
OUTLINE & SCHEMATIC DIAGRAM

138-174 MHz BAND PASS FILTER

OUTLINE DIAGRAM

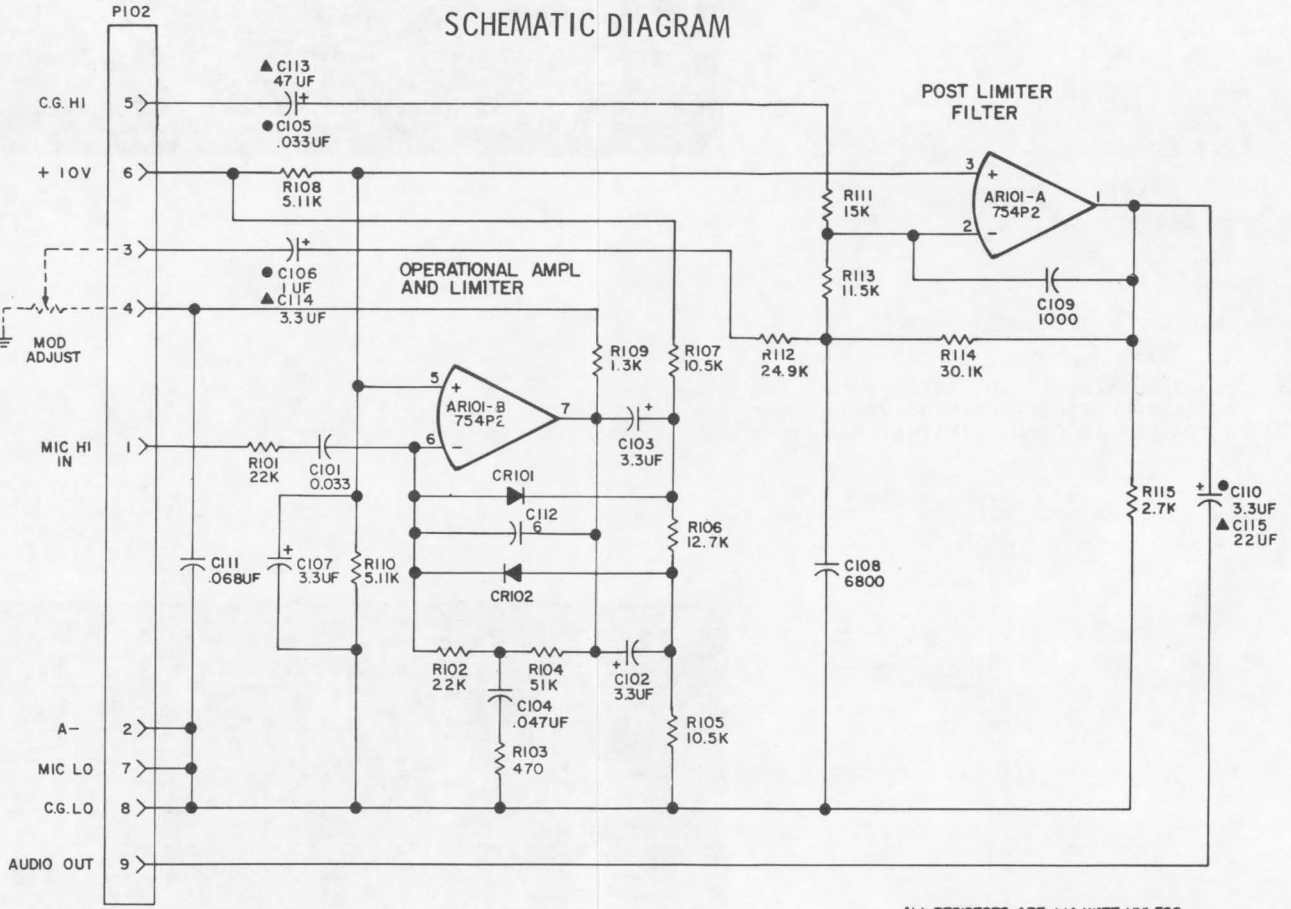


(19C331136, Rev. 3)
(19A143587, Sh. 1, Rev. 1)
(19A143587, Sh. 2, Rev. 2)



(19C327048, Rev. 4)
(19A130538, Sh. 1, Rev. 3)
(19A130538, Sh. 2, Rev. 3)

SCHEMATIC DIAGRAM



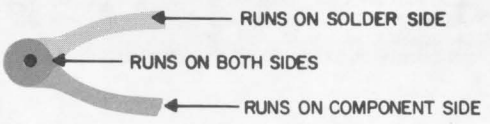
MODEL NO	REV LETTER
PL19C321542G1	C
PL19C321542G2	A

NOTES:
1. CONNECT GRD TO PIN 4 ON AR101,
CONNECT VCC (+10V) TO PIN 8 ON AR101.

(19C321854, Rev. 8)

ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY K=1000 OHMS OR MEG=1,000,000 OHMS. CAPACITOR VALUES IN PICOFARADS (EQUAL TO MICROMICROFARADS) UNLESS FOLLOWED BY UF= MICROFARADS. INDUCTANCE VALUES IN MICROHENRYS UNLESS FOLLOWED BY MH= MILLIHENRYS OR H=HENRYS.

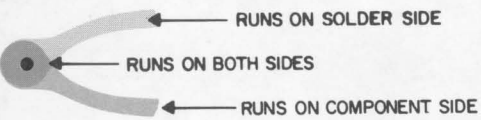
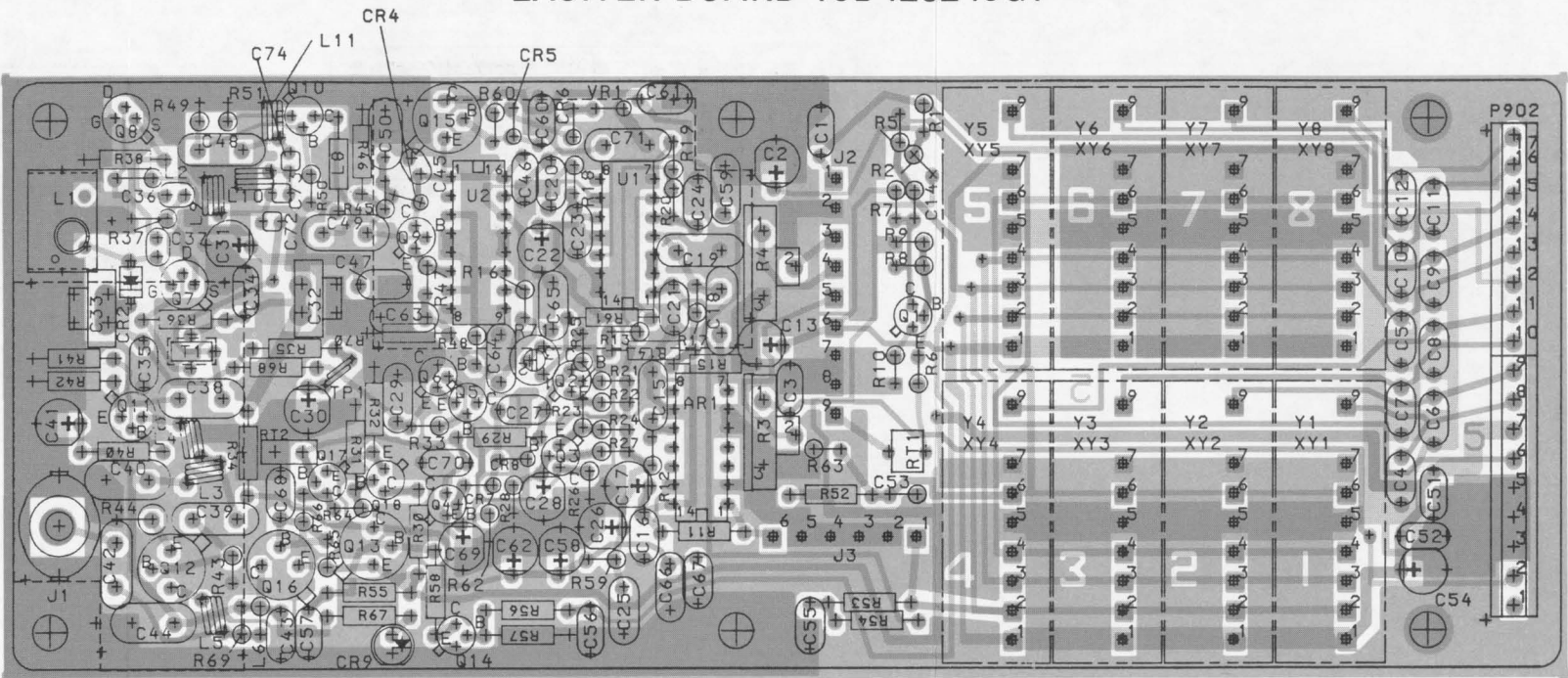
● G1
▲ G2



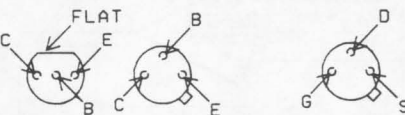
OUTLINE & SCHEMATIC DIAGRAM

AUDIO PROCESSOR

EXCITER BOARD 19D423249G1



LEAD IDENTIFICATION
FOR Q1 THRU Q6,
Q9 THRU Q18 Q7 AND Q8



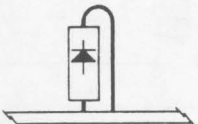
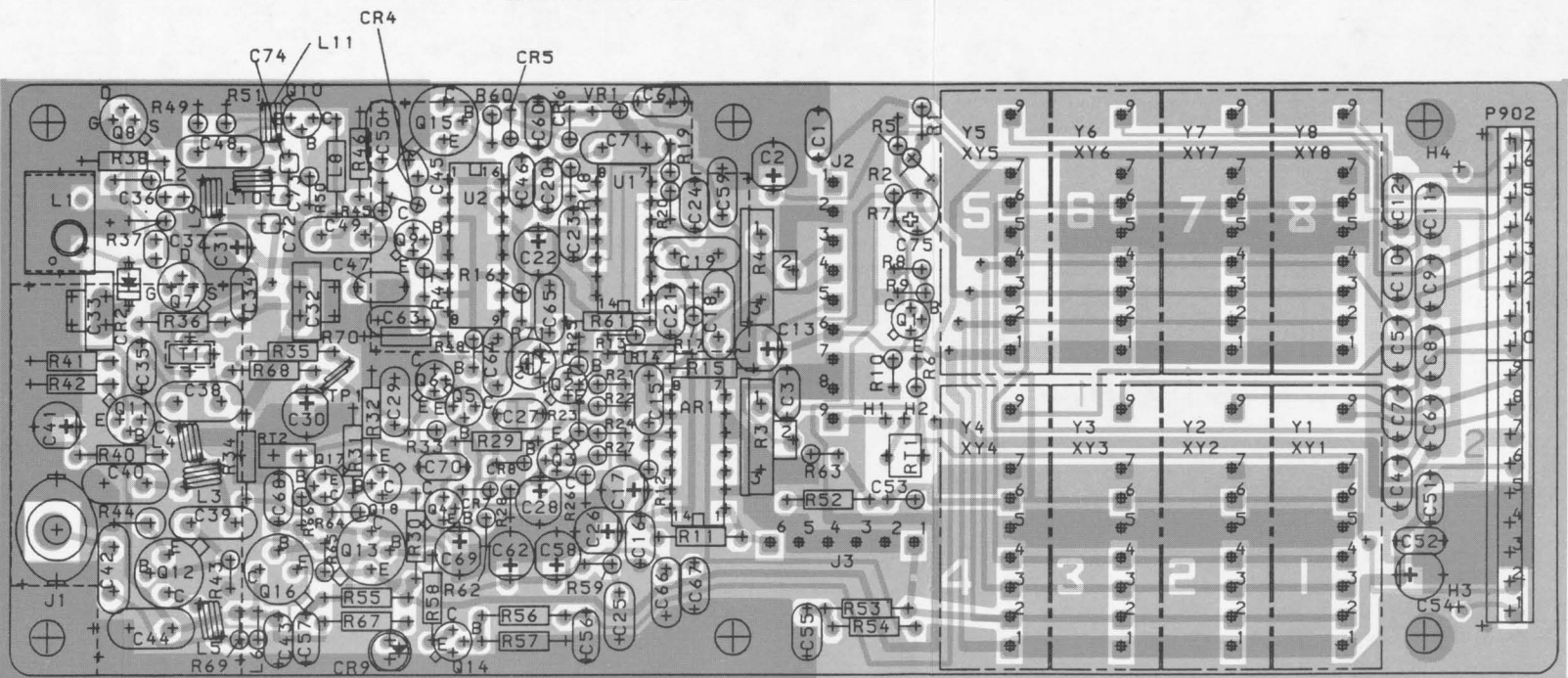
IN-LINE TRIANGULAR
QR TOP VIEW

NOTE: LEAD ARRANGEMENT, AND NOT
CASE SHAPE, IS DETERMINING
FACTOR FOR LEAD IDENTIFICATION.

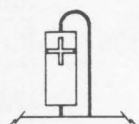
(19D424601, Rev. 7)
(19C321568, Sh. 1, Rev. 5)
(19C321568, Sh. 2, Rev. 5)

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
FOR COMPLETE DESIGNATIONS, PREFIX WITH
100 SERIES. EXAMPLE: C1-C101, R1-R101 ETC.
EXCEPT P902.

EXCITER BOARD 19D423249G2



TYPICAL ASSEMBLY FOR
CR4 THRU CR8
AND VR1



ASSEMBLY FOR C53

OUTLINE DIAGRAM

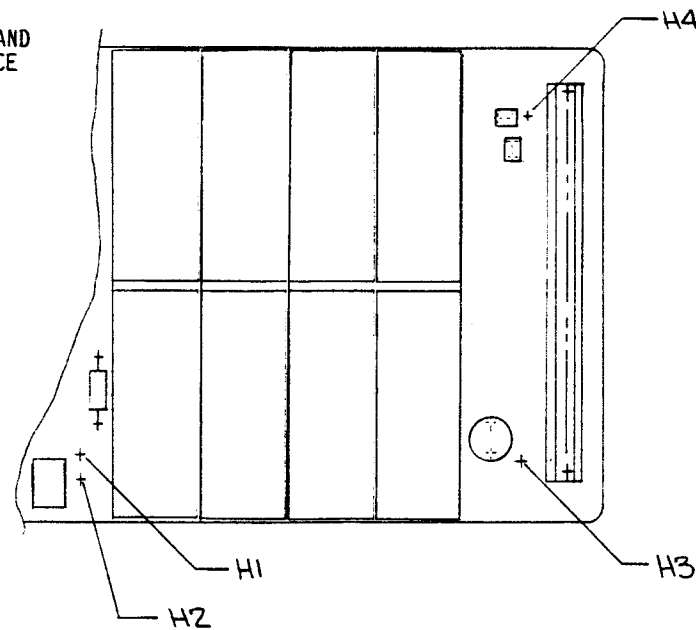
138—174 MHz
PHASE LOCK LOOP EXCITER

(19D432754, Rev. 1)
(19A143781, Sh. 1, Rev. 2)
(19A143781, Sh. 2, Rev. 1)

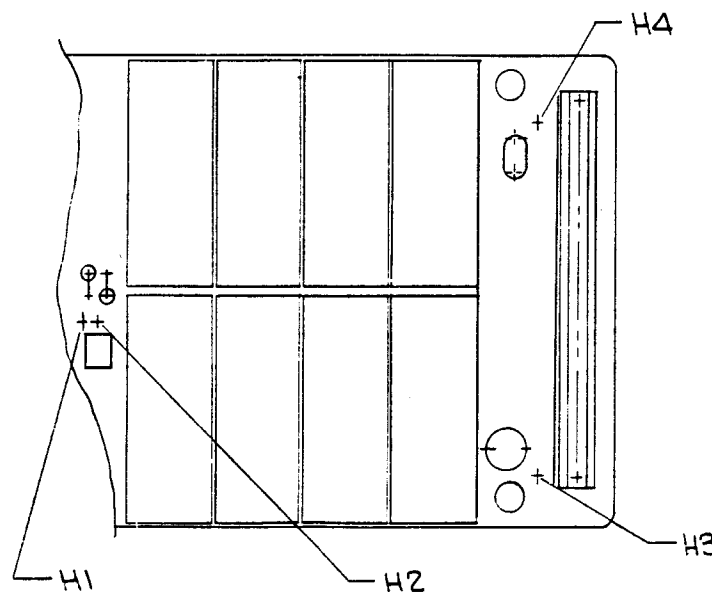
①

THIS INSTRUCTION MODIFIES A HIGH BAND OR UHF MASTR II FM EXCITER FOR VOICE GUARD OPERATION.

1. REMOVE JUMPER BETWEEN H1 & H2.
2. SOLDER SF24-R FROM H1 TO H3. (PL19B234774G1).
3. SOLDER SF24-R FROM H2 TO H4. (PL19B234774G1)



EXCITER BOARD (UHF)
PL19D432679



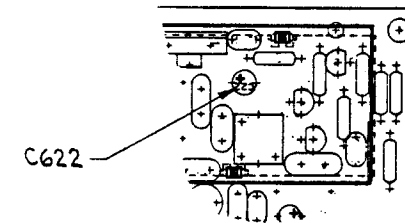
EXCITER BOARD HB
PL19D423249

③

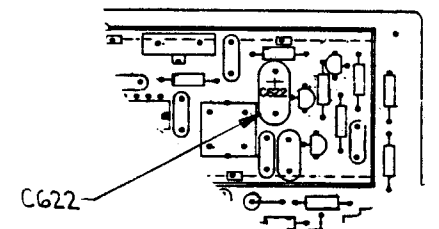
THIS INSTRUCTION MODIFIES A HIGH BAND OR UHF MASTR II RECEIVER IFAS BOARD FOR VOICE GUARD OPERATION.

1. REMOVE COVER FROM FM DETECTOR AREA.
2. REPLACE C622(0.47 UFD) WITH A 10 UFD CAPACITOR PART NUMBER 315A6047P106N (OBSERVE CORRECT POLARITY).
3. REPLACE COVER.

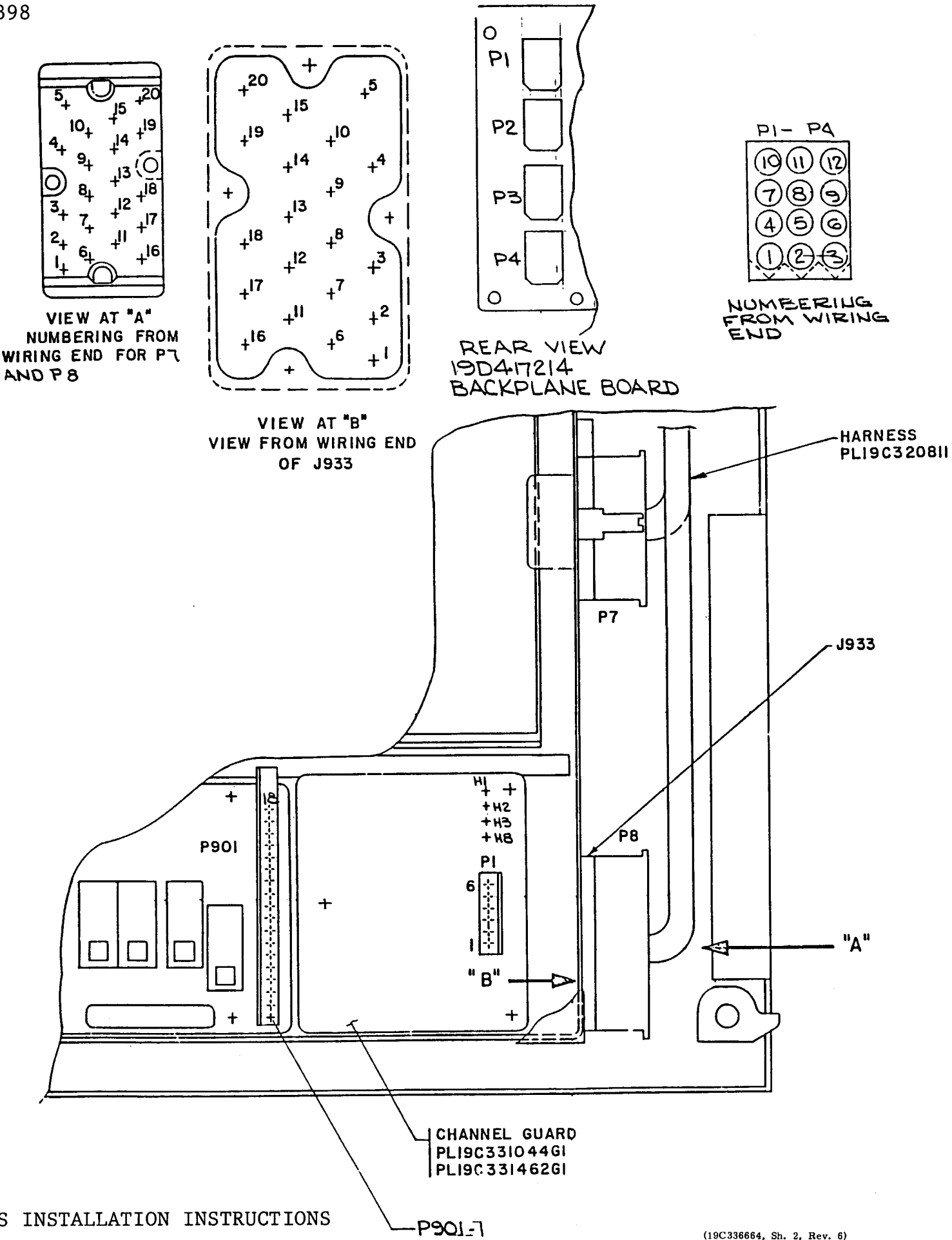
IF/AUDIO/SQUELCH BOARD
19D432667G1



IF/AUDIO/SQUELCH BOARD
19D417707G1



(19C336664, Sh. 1, Rev. 1)



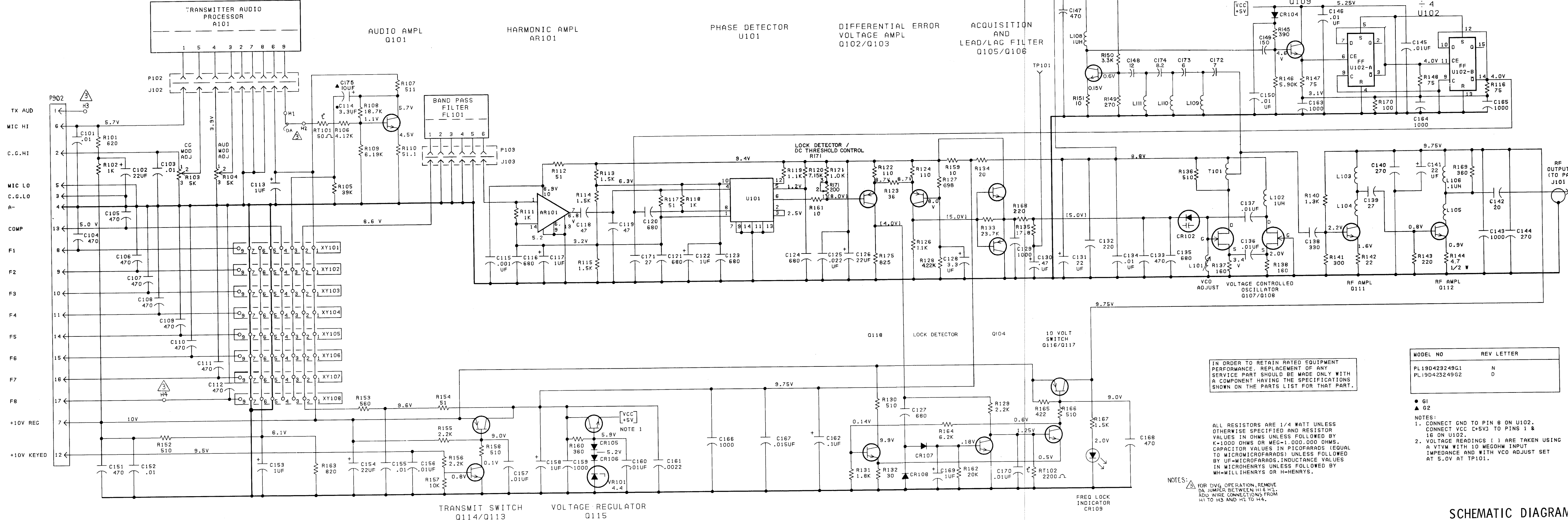
- ② THESE INSTRUCTIONS COVER THE INSTALLATION OF CABLE HARNESS PL19C851484 G2 & G3
1. INSTALL DA JUMPER BETWEEN H3 & H8 ON CG ENCODER. IF H8 NOT PRESENT CUT TERMINAL FROM WRBL WIRE (PL19234774G3) AND SOLDER TO H3. CONNECT OTHER END TO J933-18 AND SPOT TIE TO EXISTING CHANNEL GUARD HARNESS. SKIP TO STEP 3 IF H8 IS NOT PRESENT.
 2. IF H8 IS PRESENT, INSTALL WRBL WIRE (PL19B234774G3) IN P1-2 & SOLDER OTHER END TO J933-18 & SPOT TIE TO EXISTING CHANNEL GUARD HARNESS.
 3. INSTALL YELLOW WIRE (PL19B234774G4) IN P901-2 & SOLDER OTHER END TO J933-19 & SPOT TIE TO EXISTING EXCITER HARNESS.
 4. INSTALL ORANGE WIRE (PL19B234774G2) IN P901-18 & SOLDER OTHER END TO J933-20 & SPOT TIE TO EXISTING EXCITER HARNESS.
 5. INSTALL ORANGE WIRE PART OF PL19C851484G2 HARNESS IN P3-9 SOLDER OTHER END TO P8-20. INSTALL YELLOW WIRE PART OF PL19C851484G2 HARNESS IN P4-2 & SOLDER OTHER END TO P8-19. INSTALL WRBL WIRE PART OF PL19C851484G2 HARNESS IN P4-9 & SOLDER THE OTHER END TO P8-18. SPOT TIE THE PL19C851484G2 HARNESS TO EXISTING PL19C320811 HARNESS.

- ④ THESE INSTRUCTIONS COVER THE INSTALLATION OF CABLE HARNESS PL19C851484G3 AND PL19B23484161.
1. DO STEPS 1 THRU 4 OF PART 2 ABOVE.
 2. INSTALL YELLOW WIRE PART OF PL19B23484161 HARNESS IN P1-1 SOLDER OTHER END TO P7-5. INSTALL WHITE-RED WIRE PART OF PL19B23484161 HARNESS IN P4-9 SOLDER OTHER END TO P8-18. INSTALL WHITE-BLUE-BLACK WIRE PART OF PL19B23484161 HARNESS IN P4-2 SOLDER OTHER END TO P8-19. INSTALL WHITE-ORANGE WIRE PART OF PL19B23484161 HARNESS IN P3-9 SOLDER OTHER END TO P8-20.
 3. SPOT TIE PL19B23484161 TO EXISTING PL19C320811 HARNESS WITH CABLE CLAMPS SUPPLIED WITH PL19B23484161 HARNESS.

- ⑤ 800 MHZ PST - 19B234774G8
1. INSTALL YELLOW WIRE IN P901-2 & SOLDER OTHER END TO J933-19.
 2. INSTALL W-O WIRE IN P901-15 AND SOLDER OTHER END TO J933-20. SPOT TIE YELLOW AND ORANGE WIRES TO EXISTING EXCITER HARNESS.
 3. REMOVE DA WIRE BETWEEN J933-4 AND J933-8.

PARTS LIST		
LBI30401K		
138-174 MHz		
19D423249C1 HB, PHASE LOCK LOOP		
19D423249C2 HB, DIGITAL CHANNEL GUARD		
SYMBOL	GE PART NO.	DESCRIPTION
AR101	19A134441P1	Harmonic Amplifier.
----- CAPACITORS -----		
C101	19A700005P7	Polyester: 0.01 uF ±10%, 50 VDCW.
C102	19A134202P6	Tantalum: 22 uF ±20%, 15 VDCW.
C103	19A700005P7	Polyester: 0.01 uF ±10%, 50 VDCW.
C104 thru C112	19A116655P14	Ceramic disc: 470 pF ±10%, 1000 VDCW; sim. to RMC Type JF Discap.
C113	19A134202P14	Tantalum: 1 uF ±20%, 35 VDCW.
C114	5491674P36	Tantalum: 3.3 uF ±20%, 10 VDCW; sim to Sprague Type 162D.
C115	19A116655P19	Ceramic disc: 1000 pF ±20%, 1000 VDCW; sim to RMC Type JF Discap.
C116	19A116655P18	Ceramic disc: 680 pF ±10%, 1000 VDCW; sim to RMC Type JF Discap.
C117	19A134202P14	Tantalum: 1 uF ±20%, 35 VDCW.
C118 and C119	19A700105P26	Mica: 47 pF ±5%, 500 VDCW.
C120 and C121	19A116655P18	Ceramic disc: 680 pF ±10%, 1000 VDCW; sim to RMC Type JF Discap.
C122	19A134202P14	Tantalum: 1 uF ±20%, 35 VDCW.
C123 and C124	19A116655P18	Ceramic disc: 680 pF ±10%, 1000 VDCW; sim to RMC Type JF Discap.
C125	19A7000005P9	Polyester: 0.022 uF ±10%, 50 VDCW.
C126	19A134202P6	Tantalum: 22 uF ±20%, 15 VDCW.
C127	19A116655P18	Ceramic disc: 680 pF ±10%, 1000 VDCW; sim to RMC Type JF Discap.
C128	19A134202P5	Tantalum: 3.3 uF ±20%, 15 VDCW.
C129	19A116655P20	Ceramic disc: 1000 pF ±10%, 1000 VDCW; sim to RMC Type JF Discap.
C130*	19B209723P1	Tantalum: 0.47 uF ±10%, 35 VDCW.
In REV B & earlier:		
C131	19A134202P112	Tantalum: 0.47 uF ±10%, 35 VDCW.
C132	19A134202P6	Tantalum: 22 uF ±20%, 15 VDCW.
C133	19A700015P37	Teflon/Mica: 220 pF ±5%, 250 VDCW.
C134	19A700015P45	Silver mica: 470 pF ±5%, 250 VDCW.
C135	19A7000005P7	Polyester: 0.01 uF ±10%, 50 VDCW.
C136 and C137	19A116192P1	Ceramic: 0.01 uF ±20%, 50 VDCW; sim to Erie 8121 Special.
C138	7489162P39	Silver mica: 330 pF ±5%, 500 VDCW; sim to Sprague Type 118.
C139	7489162P113	Silver mica: 27 pF ±10%, 500 VDCW; sim to Sprague Type 118.
C140	19A700105P46	Mica: 270 pF ±5%, 500 VDCW.
C141	19A134202P6	Tantalum: 22 uF ±20%, 15 VDCW.
C142	19A700105P16	Mica: 20 pF ±5%, 500 VDCW.
C143	19A116655P19	Ceramic disc: 1000 pF ±20%, 1000 VDCW; sim to RMC Type JF Discap.
C144	19A700105P46	Mica: 270 pF ±5%, 500 VDCW.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES



SCHEMATIC DIAGRAM

138-174 MHz
PHASE LOCK LOOP EXCITER

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by these revisions.

REV. A - Audio Processor 19C321542G1
To standardize components. Changed R112.

REV. B - To improve audio response. Changed AR101 and R103. Added C112.

REV. C - To improve performance. Changed AR101 and R103.

REV. A - Exciter Board 19D423249G1
To increase exciter output power. Changed R144.

REV. B - To increase exciter output power. Changed R144.

REV. C - No units built. Superseded by Revision D.

REV. D - To improve operation. Changed R126 and Q103.

REV. E - To improve operation of lock detector indicator. Change R165.

REV. F - To improve operation of lock detector circuit. Changed R121.

REV. G - To shift voltage output range of differential error voltage amplifier to improve VCO lock on extremes of frequency split. Changed R127.

REV. H - To reduce level of conducted spurs. Added C172, C173, C174, L109, L110 and L111. Changed C148 and C145. Deleted R139.

OLD SCHEMATIC WAS:

REV. J - To improve detect sensitivity in cold environment. Changed Q117 and Q118. Added R171.

REV. K - To improve lock detector range and performance in a cold environment. Changed R125, R127 and R128.
R125 was: 19A700106P9 - Composition: 680 ohms $\pm 5\%$, 1/4 W.
R127 was: 19C314256P21821 - Metal film: 1.8K ohms $\pm 1\%$, 1/4 W.
in REV. F & earlier: 19C314256P22001 - Metal film: 2K ohms $\pm 1\%$, 1/4 W.
R128 was: 19C314256P21102 - Metal film: 11K ohms $\pm 1\%$, 1/4 W.

REV. A - Exciter Board 19D423249G2
Incorporated into initial shipment.

REV. B - 138-174 MHZ PLL EXCITER BOARD 19D423249G2

REV. L - 138-174 MHZ PLL EXCITER BOARD 19D423249G1

To reduce conducted spurious and improve operation. Changed C174 to 8.2pF. Old part number for C174 was: 19A116114P20 - Ceramic: 6 pF $\pm 5\%$, 100 VDCW; temp coef 0 PPM. Added by REV H.

REV C - EXCITER BOARD 19D423249G1
REV M - EXCITER BOARD 19D423249G2
To improve PA operation, changed R168.

REV D - EXCITER BOARD 19D423249G1
REV N - EXCITER BOARD 19D423249G2
To allow Lock Detector LED to extinguish when exciter is unkeyed, changed R165.

REV A - AUDIO PROCESSOR BOARD 19C321542G2
To improve low frequency response on Channel Guard Input, changed C113.
C113 was: 19A701534P7 Tantalum: 10 uF $\pm 20\%$, 16 VDCW.