LBI-30443A
(DF4104)

MOBILE RADIO

MAINTENANCE MANUAL
FOR
CONTROL MODULE 19D417750G2 WITH 2-FREQUENCY PSLM
(USED WITH C-800 AND C-900 SERIES CONTROL UNITS)
OPTIONS 9401, 9402 AND 9403

TABLE OF CONTENTS

SPECIFICATIONS*

Number of Frequencies	1 thru 12
Frequencies Searched	2
Supply Voltage	±13.8 VDC ±20%
Current Drain	170 Milliamperes (Maximum)
Controls	Power-On Volume Squelch Channel Selector Switch Search Switch
Indicators	Power On Light Transmit Light Channel Busy Light Search On Indicator

DESCRIPTION

Control Module 19D417750G2 provides all the normal control functions necessary to operate the radio and, in addition, circuitry is provided for the two frequency priority search-lock monitor function (PSLM). The PSLM alternately searches two of up to 12 channels for an incoming message.

Control functions and indicators contained on the control module include the power switch (PWR), volume and squelch controls, the channel selector switch, and the transmit and channel busy indicators.

A strapping arrangement allows the PSLM to be field modified to permit operation in one of three modes - identified by option numbers:

- Option 9401. Provides Two Frequency Search-Selectable Priority.
- Option 9402. Provides Multi-Frequency Search-Selectable Priority.
- Option 9403. Provides Multi-Frequency Search-Selectable Non-Priority.

The power on (PWR) and channel selector indicators are turned on to maximum brightness when power is applied to the radio (PWR switch on). The search (SRCH) switch is backlighted at a low level and attains maximum brightness when the search function is selected. The channel busy and transmit indicators come on when receiving or transmitting a message respectively.

All circuitry is fully transistorized using both discrete components and integrated

circuits to achieve maximum reliability. All pushbutton switches are back-lighted with light-emitting diodes (LEDs) for reliability, long life and low power consumption.

Supply voltage is provided from the vehicle ignition switch through P701-11 and the power switch S703. A 9.5-Volt regulator and 5-Volt regulator provide the required operating voltages.

The control module slides into the lower deck of the C-800 and C-900 Series Control Units. Refer to the Control Unit Maintenance Manual for installation and removal procedures.

CIRCUIT ANALYSIS

CONTROL CIRCUITS

References to symbol numbers mentioned in the following text are found on the Schematic Diagram, Outline Diagram and Parts List (see Table of Contents). The typical circuit diagrams used in the text are representative of the circuits used in the integrated circuit modules. A block diagram of the control unit is shown in Figure 1.

In addition to the two frequency PSLM circuitry, the control module is equipped with a VOLUME control (R701), SQUELCH control (R702), PWR on-off pushbutton switch and indicator (S701 and CR704), a yellow channel busy indicator (CR706), a red Transmit Indicator (CR705) and a channel selector switch (S702).

When the PWR on-off switch is in the "off" position, power is removed from the radio except for the transmitter PA, which is connected to the vehicle battery at all times. Pushing the switch in to the "on" position applies power to the radio, the PSLM circuitry, the 9.5 Volt regulator, and lights the power-on LED behind the pushbutton switch. It also backlights the PSLM indicator and completes the circuit to the DC converter when used.

CR701 and CR708 are protective diodes and will cause the fuse in the yellow lead to blow if the polarity is reversed.

Transmit Indicator/PTT Switch

Pressing the PTT switch on the microphone energizes the antenna switch, disables the search function, keys the transmitter, mutes the receiver, and lights the transmit indicator LED.

Releasing the PTT switch turns off the transmitter and transmit indicator, de-energizes the antenna switch and, when receiving, unmutes the receiver.

Channel Busy Indicator

When no signal is applied to the receiver, the Carrier Activity Sensor (CAS) voltage from the receiver squelch IC is near A-. This forward biases diode CR702 in the control unit, keeping Q701 turned off. When a signal is applied to the receiver (with or without audio), the CAS voltage rises to approximately 10 Volts. This reverse biases CR702, allowing Q701 to conduct and turn on channel busy indicator CR706. The indicator will remain on as long as a signal is applied to the receiver, or until the transmitter is keyed.

Channel Selector Switch

The channel selector switch is a 12-position rotary switch with a mechanical stop that limits rotation from one through twelve positions as required.

The channel selector switch selects the desired channel for both transmitting and receiving. The switch connects A- to the selected transmitter and receiver oscillator module so that the radio operates on the selected channel.

PRIORITY SEARCH LOCK MONITOR

When the SRCH switch is in the "OFF" position, the PSLM circuitry is disabled and messages are received and transmitted on the channel selected by the channel selector switch. The SRCH pushbutton is backlighted at a low level.

To initiate channel searching, press the SRCH pushbutton in. The SRCH pushbutton will now glow at maximum brightness. In multi-frequency applications where selectable priority (Option 9402) or selectable non-priority (Option 9403) operation is provided the priority and non-priority channels may be assigned. The selected channel is indicated by the position of the channel selector switch. In two frequency applications with selectable priority (Option 9401), the priority channel is indicated by the channel selector switch.

Operating the push-to-talk (PTT) Switch disables the PSLM circuitry and permits message transmissions on the frequency indicated by the channel Selector Switch. The Channel Busy Indicator is out when transmitting.

The PSLM assures reception of all signals on the priority channel regardless of the signal strength of the first signal received.

When a signal is received on the priority channel, the PSLM stops searching and locks on the priority channel for the

duration of the message. When a signal is received on the non-priority channel, the PSLM stops on that channel but continues to monitor the priority channel. If a signal is then received on the priority channel whose signal strength equals or exceeds 20 dB quieting, the PSLM reverts to the priority channel and locks for the duration of the priority message.

NOTE

The PSLM operates only when the receiver is squelched.

SEARCH Switch

SRCH switch S703 turns the search function "on" or "off". When selected (pushed in) the switch:

(1) applies A- (ground return) to the emitter junctions of channel drivers Q714 and Q715 to enable the search function.

(2) places R731 in parallel with R748 to turn on fully PSLM SRCH indicator CR727.

(3) connects the output of F1 channel driver to clock gate 2 enable circuit Q702 and to indicator control switch Q712 when option 9403 is incorporated.

When the SRCH switch is in the "off" position, the above circuits are disabled and the frequency select common lead is returned to A- through contacts 2 and 4 of the SRCH switch. This allows normal noise squelch operation on the channel indicated by the channel selector switch.

The Q and $\overline{Q}$ outputs are applied to channel drivers Q715 and Q714 respectively. As each transistor is turned on, the frequency select lead assigned to that channel driver is returned to A-, turning on the associated receiver oscillator module to monitor that specific channel. The channels are monitored during the time the associated channel driver is turned on.

MASTER CLOCK GENERATOR

The master clock generator generates the timing pulses required to search the selected channels and to monitor the priority channel while receiving on a non-priority channel. It consists of transistors Q707 and Q708, clock speed control transistor Q706, diode CR721, capacitor C703 and resistors R721 and R722. The master clock generator operates at two different speeds, 4 and 8 Hz, and generates an output pulse at 250 or 125 millisecond intervals respectively.

Q706 monitors the output of CAS switch Q716. In the search mode (receiver squelched) CAS switch Q716 is turned off and holds clock speed control transistor Q706 off. Switching diode CR721 is forward biased, paralleling R721 and R722 and causing the master clock generator to operate at 8 Hz. The fast clock speed is determined by R721, R722, and C703. The output pulse is a negative going 3-Volt pulse with a width of approximately one millisecond.

When a message is received on any channel, the CAS line switches to +10V and CAS switch Q716 turns on. Clock speed control transistors Q706 then turns on, back biasing diode CR721 to remove R721 from the emitter circuit of Q707. This causes the master clock generator to operate at 4 Hz, providing a negative output pulse every 250 milliseconds. The slow clock speed is determined by R722 and C703 and is used to monitor the priority channel when a non-priority message is being received.

CAS DELAY

The CAS delay circuit holds the receiver open for up to 5 seconds during periods of signal fade out or loss of carrier. This prevents the PSLM from searching during the CAS delay time and perhaps selecting the second channel.

The CAS delay circuit consists of C702, R718, R720 and Q704. When a carrier is received, CAS switch Q716 turns on and charges C702. During a short signal fadeout or loss of carrier, CAS switch Q716 will turn off, thus attempting to remove the positive voltage from the base of clock gate 1 enable transistor Q705, clock speed control transistor Q706 and CAS delay capacitor C702. Instead, capacitor C702 now begins discharging through R718, R720 and the base/emitter junctions of Q705 and Q706 respectively. Q705 and Q706 remain on, thereby preventing the PSLM from reverting to the search mode during the CAS delay time.

Should the carrier fail to return within 1.5 seconds, C702 will have discharged to a level sufficient to turn off clock speed control transistor Q706 and start to turn off clock gate 1 enable transistor Q705.

When Q705 starts to turn off, CAS switch Q704 instantaneously turns on, immediately turning Q705 off. This locks the PSLM into the search mode again.

NOTE

The CAS delay feature is not compatable with Channel Guard or in radios that utilize PSLM with locked priority. If either of these two conditions exist, CAS delay capacitor C702 must be removed.

MODES OF OPERATION

To facilitate circuit analysis, a description is provided for each of the three operational modes:

- Receiver Squelched
- Receiving Non-Priority - Searching Priority Channel
- Receiving Priority Channel

RECEIVER SQUELCHED

When the receiver is squelched (no messages being received), the PSLM alternately searches the priority and non-priority channel. The CAS line is near A-. This low voltage is applied to a diode isolation matrix consisting of CR702, CR717, and CR718 and controls operation of the CAS switch, channel busy indicator and clock gate 2 enable transistors Q703 and Q702. The channel busy switch Q701 is held off. CAS switch Q716 is turned off, causing its emitter to approach A-. This low voltage is applied to the base of Q706, turning it off and causing the master clock generator to operate at the fast speed (a pulse every 125 milliseconds). At the same time, CR703 is reverse biased turning Q702 off. When Q702 turns off, Q703 turns on placing a low on one input of clock gate 2 (U701C). This turns clock gate 2 off, inhibiting the clock input pulse to the priority sample (one-shot) pulse generator.

The negative output pulse from the master clock generator is applied through inverter U702D to one input of clock gate 1. The second input to clock gate 1 is also high since clock gate 1 enable transistor Q705 is held off by CAS switch Q716. The collector of Q705 goes high enabling clock gate 1 and allowing the inverted clock pulses to be applied to the trigger input of channel FF U703. (Refer to Figure 2, Receiver Squelched Timing Diagram.)

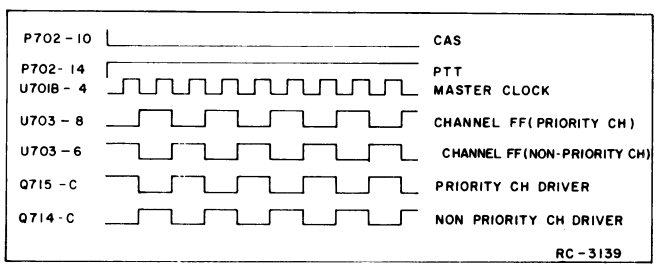

Figure 2 - Receiver Squelched, Timing Diagram

RECEIVING NON-PRIORITY

When a non-priority channel becomes active (signal received) the CAS line switches to +10 VDC. The PSLM will stop on that channel while monitoring the priority channel. The priority channel is monitored for 6-7 milliseconds at approximately 250 millisecond intervals (four times per second). If a signal is received on the priority channel, the PSLM will transfer operation from the non-priority channel to the priority channel for the duration of the message. Refer to Figure 3 for the timing diagram for receiving non-priority channels.

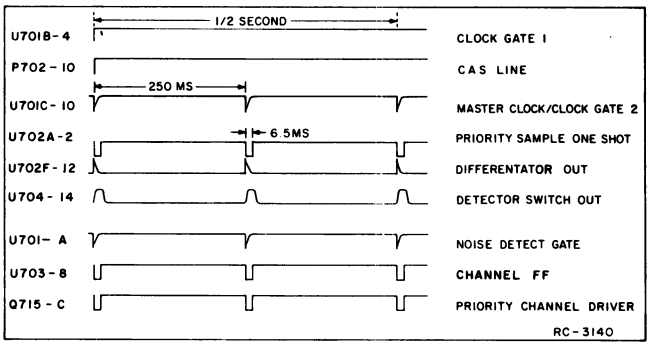

Figure 3 - Receiving Non-Priority/ Search Priority Timing Diagram

When the CAS line goes high diodes CR702, CR717 and CR718 in the diode isolation matrix are reverse biased. CAS switch Q716 turns on, applying A+ to the base of clock gate 1 enable transistor Q705. Q705 turns on and applies A- to one input of clock gate 1, turning it off to stop the channel FF on the active non-priority channel. In this condition Q714 is on and Q715 is turned off. Channel FF, U703, now operates under control of clock gate 2, U701C, and the priority channel noise detect gate U701A to monitor the priority channel at the proper time.

Inverter U702B, in series with C716, monitors the output of OR gate U701D. When a non-priority signal is received clock gate 1 is disabled and clock gate 2 becomes active. At this time the positive pulse from the OR gate is inverted and the negative transition applied to the trigger input of channel FF to enable immediate searching of the priority channel.

Approximately 6.5 milliseconds later a negative transition generated by the priority sample one-shot circuitry and noise detect state is applied to the channel FF to end the search of the priority channel. This sequence is repeated for each cycle of the slow speed clock.

At the same time, the positive voltage applied from CAS switch Q716 turns on clock speed control transistor Q706. When Q706 conducts, diode switch CR721 is reverse biased removing R721 from its parallel connection across R722, producing the slower clock speed. The master clock generator generates one negative going clock pulse every 250 milliseconds.

Clock gate 2 enable transistors Q702 and Q703 now switch states. With CR718 reverse biased Q702 turns on causing Q703 to turn off, thereby removing A- from the enable input (pin 8) of clock gate 2. With the enable input now at +5V, the clock pulses are passed through to the OR gate input, of the priority sample one-shot generator.

Priority Sample One-Shot and PSLM Hybrid

The 6.5 millisecond priority sample pulse is generated by OR gate U701D inverters U702B, C, and Q709. When a signal is received on a non-priority channel, slow speed clock pulses from clock gate 2 are applied to one input of OR gate U701D. The second input to the OR gate is high at this time since Q709 is normally in the "on" state until clock pulses from clock gate 2 are received. The negative transition of the input clock pulse is inverted by the OR gate and applied to inverter U702C and U702B. The negative going output of U702C turns Q709 off allowing the input of inverter U702A to go high and its output low. (This is the negative going transition of the priority sample pulse). The low output of inverter U702A is applied back to the input of OR gate U701D holding its output high. Approximately 6.5 milliseconds later capacitor C710 is charged up and allows Q709 to turn on causing the output of inverter U702A to go high (positive transition of priority sample pulse) and open the OR gate to the next clock pulse. At the same time the output of the OR gate is driven low (due to highs on both inputs) to complete the creation of a 6.5 millisecond pulse on the OR gate output.

At the same time, the positive going pulse from the output of OR gate U701D is applied to pin 2 of U704 (PSLM Hybrid). In the audio muting circuit, audio and noise from the receiver are coupled from pin 3 of U704, through the audio muting coupling circuit to pin 4. The positive pulse at pin 2 causes the priority channel audio to be muted during the priority channel search period. This prevents objectionable noise bursts from being heard at the speaker each time the priority channel is monitored. Refer to Figure 4 for a typical diagram of the PSLM Hybrid.

When the audio is muted, a negative going priority sample pulse is applied to the noise muting circuit and to the differentiator circuit (U704-pin 9). The noise muting circuit applied audio and noise to the fast squelch circuit. The fast squelch circuit is comprised of the noise mute circuit, noise filter, noise amplifier, and detector switch. When the priority channel is not being monitored, audio and noise is shunted to ground by the noise mute circuit, thus the detector switch output is at ground potential. This inhibits the priority channel noise detect gate U701A.

The differentiator applies a positive spike at the end of the 6.5 millisecond period to the base of Q718, turning it on. The low on the collector of Q718 is inverted by U702F and provides one input to priority channel noise detect gate U701A.

Priority channel search begins coincident with the positive output pulse of OR gate U701D. This positive pulse is inverted by U702B and applied to the trigger input of channel FF U703. The negative transition causes the output of the FF to change states and enable priority channel driver Q715.

Coincident with priority channel search time, the negative going pulse from the priority channel one-shot (U702A) is applied to the noise mute input of PSLM hybrid U704-9. This turns the noise mute circuit off, allowing the noise output of the noise filter to be applied to the noise amplifier. The output of the noise amplifier is rectified and fed to the detector switch, turning it off. Turning the detector switch off generates a positive going 10-12 millisecond pulse which is applied from U704-14 to one input of the priority channel noise detect gate (U701A). Thus, with positive inputs on noise detect gate U701A, a negative going pulse appears at its output. This negative pulse occurs coincident with the trailing edge of the priority pulse and is applied to the input of the channel FF. This changes the $\overline{Q}$ output of the channel FF back to the high state and reselects the active non-priority channel. This cycle is repeated once every 250 milliseconds or until a priority channel becomes active.

Priority Channel Transfer

If a priority signal is received during the 6.5 milliseconds search period, the priority signal quiets the receiver, inhibiting the operation of the fast squelch circuit in the PSLM hybrid so that the noise filter has no output. As a result, the detector switch remains on providing a ground at its output (pin 14). This inhibits the priority channel noise detect gate from generating a negative pulse to reset the channel FF.

The Q output then will remain high holding priority channel driver Q715 on for the duration of the priority message. The CAS line remains high indicating receipt of the priority message. Therefore, clock gate 1 is still turned off and no clock pulses are applied to the channel FF. With F1 assigned as the priority channel, A- from Q715C is applied to clock gate 2 enable transistor Q702 through H111-H7, S702-13, H114-H113, and diode CR720. Q702 then turns off, enabling Q703. Q703 drives one input of clock gate 2 low, inhibiting the slow speed clock pulses.

When a non-priority channel is receiving a message, the channel busy indicator will be off and blink on for 6 milliseconds, 4 times a second during the priority channel

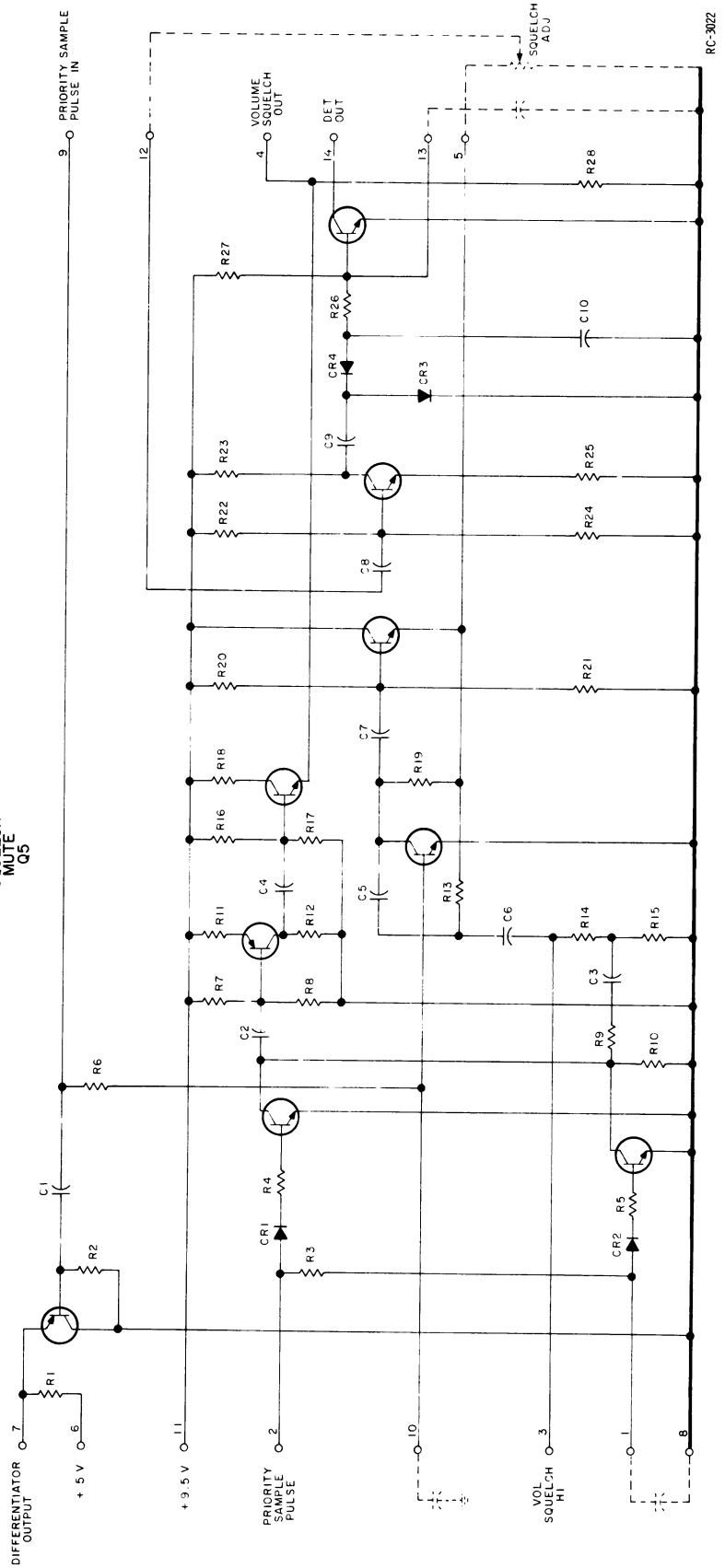

Figure 4 - Simplified Diagram PSLM Hybrid

search time. This occurs each time the collector of the priority channel driver is returned to A-.

RECEIVING PRIORITY

In the search mode when a priority channel becomes active (receives signal) the clock inputs are removed from the channel FF, causing it to select the priority channel. Refer to Figure 5, Receiving Priority. When the CAS lead goes high CAS switch Q716 turns on and as a result turns on Q705 which applies A- to the inhibit input of clock gate 1 (U701B). This inhibits the gate, removing fast clock pulses to the channel FF. Clock pulses to the priority sample one-shot also are inhibited simultaneously when the frequency select lead is grounded by the priority channel driver. A- is applied through diode CR720 to the base of Q702 turning it off and as a result, turns Q703 on. This inhibits clock gate 2, preventing slow clock pulses from triggering the channel FF and the priority sample one-shot generator.

A- is also applied to indicator control switch Q712 through diode CR723. Q712 turns off, allowing channel busy indicator switch Q701 to turn on. Q701 applies A+ to channel busy indicator CR706, turning it on.

LOCKED PRIORITY OPERATION

Locked priority operation prevents the operator from selecting the priority channel. The priority channel is designated by the user and physically strapped to that channel; however, the strapping arrangement provided permits the priority channel to be reassigned as desired.

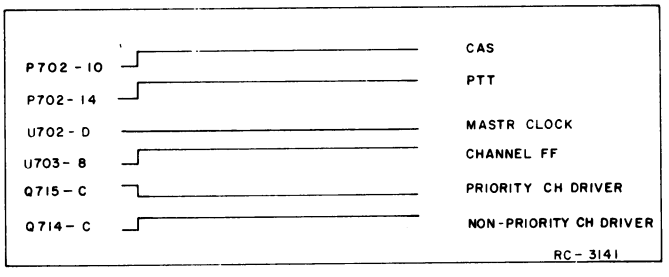

Figure 5 - Receiving Priority, Timing Diagram

Circuit operation is the same as in the other modes of operation. Messages are transmitted over the channel indicated by the channel selector switch. The CAS delay circuit must be disabled when the priority channel is locked on one channel (not selectable).

PUSH-TO-TALK AND TRANSMIT REVERT

When the microphone is keyed, the push-to-talk line goes low, A- is applied to transmit indicator CR705, PTT delay circuit, master clock generator, CAS delay circuit, channel drivers, indicator control switch/clock gate 2 enable and transmit revert circuits. This shuts down the master clock, shorts out CAS delay capacitor C702 and inhibits clock gate 2, channel drivers and indicator control circuits.

NOTE

The PTT delay circuit is active only in systems equipped with Channel Guard. If Channel Guard is not used PTT delay capacitor C708 is removed.

A- is applied to PTT switch Q710 through diodes CR726 and CR725, reverse biasing CR725. This causes Q710 to turn off. When Q710 stops conducting, its collector rises toward +5V. The base of transmit revert switch Q711, which is connected through R730 to the collector of Q710, follows this rise in voltage and, when the rise in voltage exceeds the threshold, turns Q711 on. Q711 grounds the frequency select common lead and selects the frequency of the transmitter to be keyed through the channel selector switch. PTT delay transistor Q720 is turned off by the positive voltage applied to its base through R747.

The positive voltage (high) on the collector of Q710 is applied to clock disable switch Q719, disabling the master clock generator and to search control transistor Q713. When the PTT switch is pressed Q713 is turned on and disables both channel drivers through diodes CR715 and CR713, and CR716 and CR714.

When the PTT switch is released, A- is removed from the junction of CR725 and CR726. The PTT dropout delay is controlled by R702 and C708. Approximately 250 milliseconds is required to charge C708 to the point where PTT delay switch Q710 will turn on (Q710 is held off by the charging current of C708). After this delay Q710 starts to turn on, turning Q720 on through C709 which in turn drives Q710 into saturation. At the same time transmit revert switch Q711 is turned off, releasing the ground on the frequency select common lead.

The fast on/slow off action of the PTT dealy circuit is required to maintain a ground on the frequency select common lead for the duration of the Channel Guard transmit phase reversal (for squelch tail elimination). If Channel Guard is not present, C708 is removed and there is no delay from the time the PTT switch is released and the PSLM resumes searching.

VOLTAGE REGULATOR

The 9.5 V regulator consists of Q717 and associated circuitry. It provides +9.5 V to the CAS switch and PSLM Hybrid (U704). Transistor Q717 is a series regulator whose base-emitter voltage is held constant by zener diode VR701 (10V zener). Q717 can be considered as a voltage controlled variable resistor whose resistance varies with a change in collector voltage.

With the base-emitter voltage constant, a drop in collector voltage will cause Q711 to conduct harder, thereby reducing the voltage drop across the collector to emitter and maintaining a constant +9.5 V at the emitter. Conversely, an increase in collector voltage will decrease conduction of Q711 which effectively increases the series resistance and prevents the emitter voltage from rising.

A 5-Volt regulator, VR702, provides +5V to operate the remaining PSLM circuitry.

NOTE

If the channel selector switch is set to the Locked Channel (Priority or non-priority), the PSLM will appear not to search. Under these conditions the collectors of both channel drivers are connected together through the channel selector switch, therefore the selected channel is monitored continuously.

FIELD MODIFICATIONS

LOCKED PRIORITY AND NON-PRIORITY CHANNELS

Any two of up to twelve channels may be selected for searching. Any one of these channels may be selected and hard wired by a strapping arrangement to provide a fixed priority or non-priority channel as desired. The second channel is then selectable. Refer to the Schematic diagram for details on the strapping arrangement.

CAS DELAY

The CAS delay capacitor (C702) is present only in radios not equipped with Channel Guard. When Channel Guard is provided in radios equipped with PSLM, capacitor C702 is removed.

PTT DELAY

The PTT delay function is used only in radios equipped with Channel Guard. The delay is provided by C708. If the radio is not equipped with Channel Guard C708 is removed. If Channel Guard is field installed in a radio equipped with PSLM, C708 must also be installed on the control module. Refer to Schematic Diagram.

DC CONVERTER MODIFICATIONS (MASTR II only)

In radios equipped with the DC converter, the power switch is modified so that the input voltage is applied directly to the DC converter. Instructions for the modification are shown on the Schematic Diagram.

CAUTION

When using the DC Converter, do not connect battery ground to Control Unit A-. To do so may cause failure of the current limiting circuit in the converter.

PRIORITY DISABLE

To disable the priority function on the PSLM and revert to search lock operation remove C710.

PSLM MAINTENANCE AND ADJUSTMENT

A control module extender board, 19D417768G1 is available for servicing the control module.

A troubleshooting procedure, including waveforms, is provided to aid the technician to isolate a malfunction.

A single adjustment control, R726 (Priority Squelch) is contained in the PSLM circuitry. Refer to the Troubleshooting Procedure to determine when adjustment of R726 is necessary.

PRIORITY SQUELCH ADJUSTMENT

Priority Squelch Adjust R726 is preset at the factory for 20-dB quieting sensitivity on the priority channel, and will normally require no further adjustment. If it should become necessary to readjust R726 use the following procedure. Two signal generators (M560 or equivalent) with a three way 6-dB pad are required. Insert the control module in the extender board and plug into control deck.

1. Set the channel selector switch to a non-locked frequency position and the SEARCH switch to the SEARCH (in) position.

2. Alternately squelch and unsquelch the receiver until the PSLM stops

on the non-priority channel. The PSLM searches when the receiver is squelched and may lock on either the priority or non-priority channel when the receiver is unsquelched. Therefore, several attempts may be required to stop the PSLM on the non-priority channel. Verify by observing that the channel busy light on the control unit flashes.

3. Apply a 1000 microvolt signal with standard modulation on the non-priority channel. Also apply a 20 dB quieting level (unmodulated) to the priority channel using the second generator.

4. Slowly turn priority squelch adjust control R726 counterclockwise until the priority channel pre-empts the non-priority channel. This should be at the 20-dB quieting level as measured previously.

5. If necessary, adjust the Priority Squelch control R726 until the PSLM switches channels at the 20-dB level. Check all channels for proper operation.

MOBILE RADIO DEPARTMENT
GENERAL ELECTRIC COMPANY • LYNCHBURG, VIRGINIA 24502

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PSLM TROUBLESHOOTING PROCEDURES

NOTE

The audio quality of the non-priority channel can best be checked with an unmodulated carrier or voice modulation. When the PSLM is on a non-priority channel, applying a constant tone to the receiver will result in a pulsed sound.

SYMPTOM	PROCEDURE
No receiver audio	1. Check the receiver in a different system (with or without PSLM). 2. Check waveforms at Test Points (J) and (H).
Fails to lock onto a non-priority channel	1. Check the setting of Priority Squelch Adjust R726. 2. Check waveforms at Test Points (A), (D), and (B). Check waveform for all selected channels. 3. Check system interconnections (refer to Interconnection Diagram in the Maintenance Manual for the control unit).
Does not transfer to priority channel	1. Check setting of Priority Squelch Adjust control R726. 2. Check voltage readings and waveforms at Test Points (A)(C)(D)(G)(F)(L)(M) and (N).
Incorrect channel assignment for locked priority or non-priority operation	1. Verify correct strapping for assigned channel. Refer to Schematic Diagram.
Missed syllables on the first part of transmissions	1. Check waveform at Test Point (A) for incorrect sample rate. Resistors R722 and R723 control the sample rate.
PSLM continues searching when PTT switch depressed	1. Check for 0.6 V or less at junction of CR725 and CR726 and Q713C. 2. Check test points (A), (R) and (P). 3. Verify proper operation of Q707, Q708, Q719, Q710 and Q713. 4. Check microphone.
Intermittent audio muting while receiving on a priority channel	1. Check waveforms and voltage levels at Test Points (C) and (E).

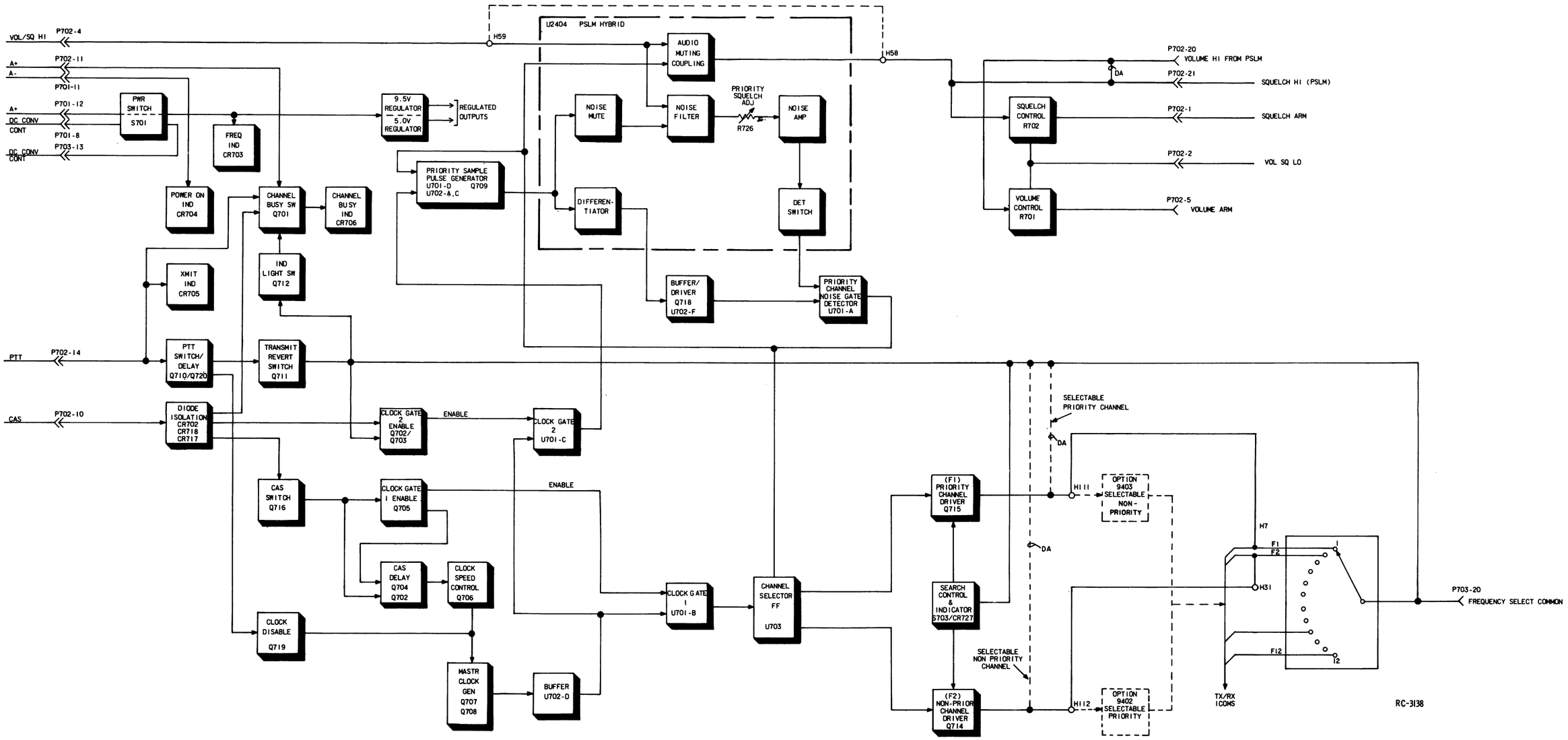
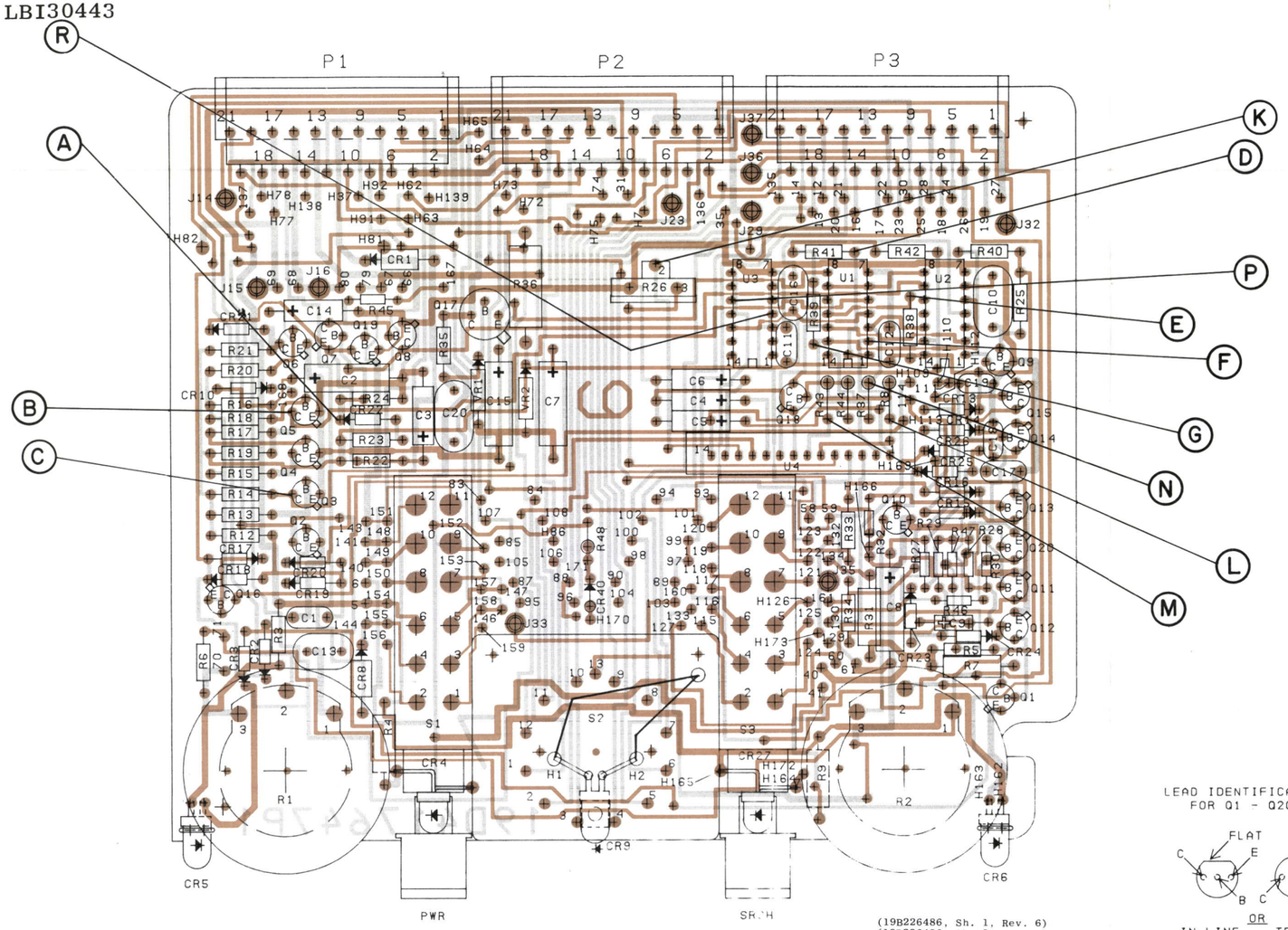


Figure 1 - Control Unit Block Diagram



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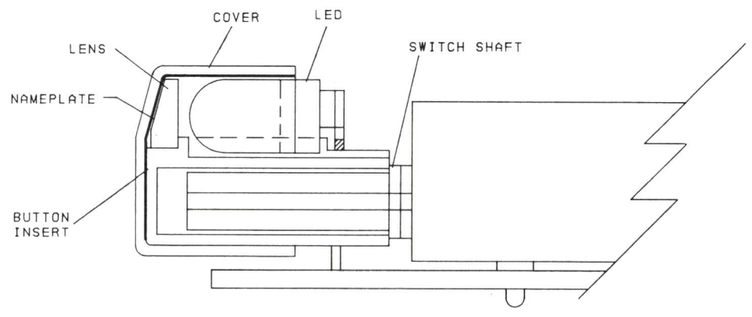

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OUTLINE DIAGRAM

TWO FREQUENCY PRIORITY SEARCH LOCK MONITOR

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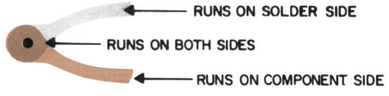


VOLTAGE READINGS

All voltage readings are DC readings measured with a 20,000 ohm-per-volt VOM with reference to system negative. The readings are taken with F1 assigned as the priority channel.

NOTE

Readings followed by a (P) are averages of pulsating meter deflections. These readings may vary widely due to the differences in meter ballistics, but may be used to determine that the circuit is operative (or switching) and not at a DC or ground potential.

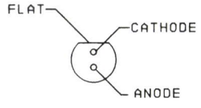
Preliminary Checks

NOTE - Voltages are nominal

1. Check for +9.5 volts at C2416 (+).
2. Check for +5 volts at C2407 (+).
3. Check for +5 volts at pin 14 of U701-U703.
4. Check for ground (A-) at pin 7 of U701-U703.

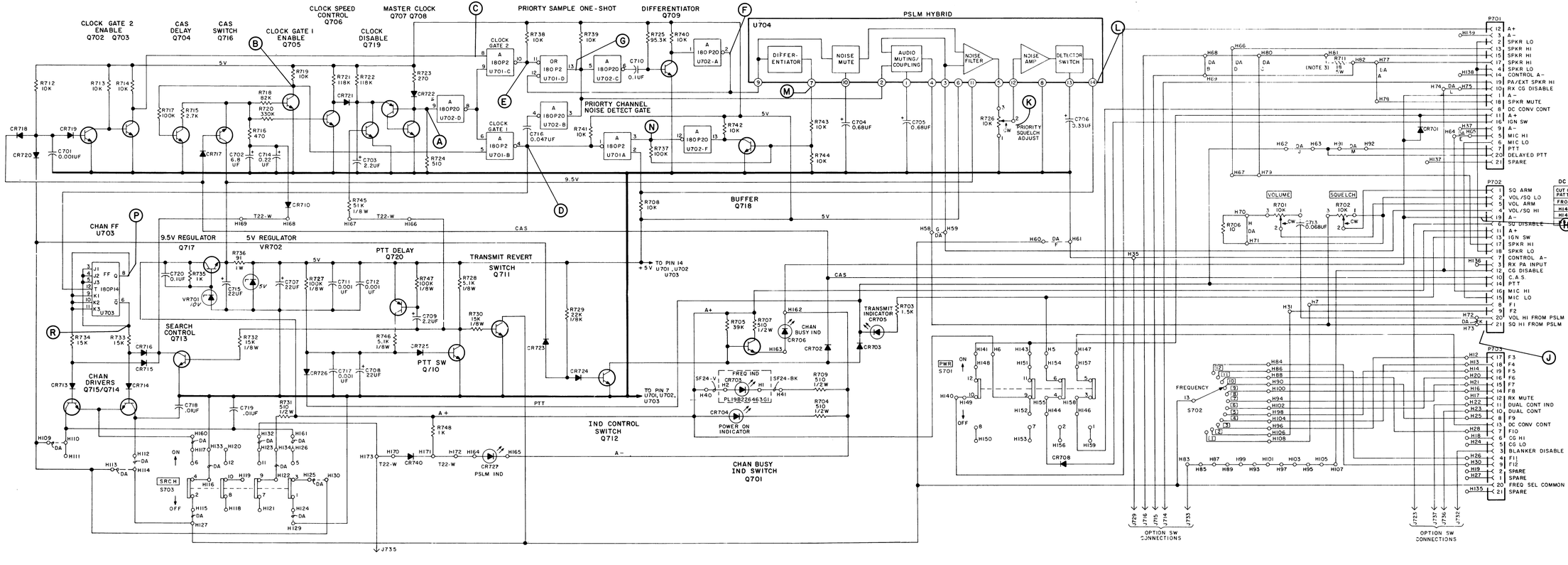
Test Point	Reading with Receiver Squelched	Reading with Receiver Unsquelched (on Non-Priority Channel)	Reading with Receiver Unsquelched (on Priority Channel)
A	2.8V	2.8V	2.8V
B	4.4V	0.2V	0.2V
C	0.2V	4.8V	0.2V
D	1.5V (P)	3.2V (P)	4.0V
E	4.0V	3.8V	4.0V
F	4.0V	3.2V (P)	4.0V
G	0.2V	0.3V (P)	0.2V
H	4.5V	4.5V	4.5V
J	4.5V	4.0V	4.0V
K	0.8V	0.8V	0.8V
L	0.2V	0.5V (P)	0.2V
M	0.6V	0.7V (P)	0.6V
N	0.2V	0.3V (P)	0.2V

NOTE: LEAD ARRANGEMENT, AND NOT CASE SHAPE, IS DETERMINING FACTOR FOR LEAD IDENTIFICATION.



LEAD IDENTIFICATION
FOR CR4, CR5, CR6, CR9, &CR27

PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFEX WITH 700 SERIES. EXAMPLE C1-C701, R1-R701, ETC.



OPTION CONNECTION CHART			
OPTION	FUNCTION	FROM	TO
9401	(SELECTABLE PRIORITY TWO FREQUENCY ONLY)	H111 H112 H113	H7 H31 H114
9402	(SELECTABLE PRIORITY MULTI-FREQUENCY ONLY)	H109 H112 H113	H110 PER TABLE I H114
9403	(SELECTABLE NON-PRIORITY MULTI-FREQUENCY ONLY)	H124 H125 H126 H112 H111	H129 H130 H161 H114 PER TABLE I

TABLE #1	
LOCKED CHANNEL	CONNECT TO
1	H7
2	H31
3	H112
4	H113
5	H114
6	H120
7	H121
8	H116
9	H125
10	H128
11	H126
12	H130

DC CONVERTER CHART			
CUT OR REMOVE PATTERN		SOLDER DA WIRE	
FROM	TO	FROM	TO
H141	H148	H5	H6
H143	H151	H147	H154
H154	H149	H149	H152

NOTES:
1. LETTERED DA JUMPERS ON PW BD ARE TO BE REMOVED WHEN SPECIFIED ON OPTIONS.
2. WHEN CHANNEL GUARD IS PRESENT, CAS DELAY CAPACITOR C702 IS REMOVED AND PTT DELAY CAPACITOR C708 MUST BE IN PLACE.
3. R711 (OPTIONAL) IS USED WITH INT/EXT SPEAKER OPTION.
4. UNLESS OTHERWISE SPECIFIED CHANNEL 1 IS ASSIGNED PRIORITY AS SHIPPED FROM FACTORY.
5. DA JUMPERS "A","C" AND "H" ARE REMOVED WHEN THE STANDARD HANDSET AND HOOKSWITCH ARE USED.
6. DA JUMPER "H" IS REMOVED WHEN THE UNIVERSAL TONE CONNECTOR (OPTION 9405) IS PRESENT.

ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY K=1000 OHMS OR MEG=1,000,000 OHMS. CAPACITOR VALUES IN MICROFARADS (EQUAL TO MICROMICROFARADS) UNLESS FOLLOWED BY UF=MICROFARADS, PICOFARADS VALUES IN MICROHENRYS UNLESS FOLLOWED BY MH= MILLIHENRYS OR H=HENRYS

IN ORDER TO RETAIN RATED EQUIPMENT PERFORMANCE, REPLACEMENT OF ANY SERVICE PART SHOULD BE MADE ONLY WITH A COMPONENT HAVING THE SPECIFICATIONS SHOWN ON THE PARTS LIST FOR THAT PART.

THIS ELEM DIAG APPLIES TO	
MODEL NO	REV LETTER
PLI9041775G2	A

(19862207G, Rev. 11)
(RC-3148)

SCHEMATIC DIAGRAM

TWO FREQUENCY PRIORITY SEARCH LOCK MONITOR

PARTS LIST

LBI-30444

CONTROL MODULE
19D41775G2

SYMBOL	GE PART NO.	DESCRIPTION
		- - - - - - - - - - CAPACITORS - - - - - - - - - -
C701	5494481P111	Ceramic disc: 1000 pf ±20%, 1000 VDCW; sim to RMC Type JF Discap.
C702	5496267P218	Tantalum: 6.8 µf ±10%, 35 VDCW; sim to Sprague Type 150D.
C703	5496267P413	Tantalum: 2.2 µf ±5%, 20 VDCW; sim to Sprague Type 150D.
C704 and C705	5496267P229	Tantalum: 0.68 µf ±10%, 35 VDCW; sim to Sprague Type 150D.
C706	5496267P227	Tantalum: 0.33 µf ±10%, 35 VDCW; sim to Sprague Type 150D.
C707	5496267P10	Tantalum: 22 µf ±20%, 15 VDCW; sim to Sprague Type 150D.
C708	5496267P210	Tantalum: 22 µf ±10%, 15 VDCW; sim to Sprague Type 150D.
C709	5491674P44	Tantalum: 2.2 µf 20%, 15 VDCW; sim to Sprague Type 162D.
C710	19A116080P207	Polyester: 0.1 µf ±5%, 50 VDCW.
C711 and C712	5494481P111	Ceramic disc: 1000 pf ±20%, 1000 VDCW; sim to RMC Type JF Discap.
C713	19A116080P106	Polyester: 0.068 µf ±10%, 50 VDCW.
C714	5496267P26	Tantalum: 0.22 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C715	5496267P10	Tantalum: 22 µf ±20%, 15 VDCW; sim to Sprague Type 150D.
C716	19A116080P5	Polyester: 0.047 µf ±20%, 50 VDCW.
C717	5494481P111	Ceramic disc: 1000 pf ±20%, 1000 VDCW; sim to RMC Type JF Discap.
C718 and C719	19A116080P1	Polyester: 0.01 µf ±20%, 50 VDCW.
C720	19A116080P7	Polyester: 0.1 µf ±20%, 50 VDCW.
		- - - - - - - DIODES AND RECTIFIERS - - - - - -
CR701	4037822P1	Silicon.
CR702 and CR703	19A115250P1	Silicon.
CR704	19A134407P7	Diode, optoelectronic: yellow.
CR705	19A134146P8	Diode, optoelectronic: red.
CR706	19A134407P7	Diode, optoelectronic: yellow.
CR708	4037822P1	Silicon.
CR709	19A134407P7	Diode, optoelectronic: yellow.
CR710	19A115250P1	Silicon.
CR713 thru CR726	19A115250P1	Silicon.
CR727	19A134407P7	Diode, optoelectronic: yellow.
CR740	19A115250P1	Silicon.
		- - - - - - - JACKS AND RECEPTACLES - - - - - - -
J714 thru J716	4033513P4	Contact, electrical: sim to Bead Chain L93-3.
J723	4033513P4	Contact, electrical: sim to Bead Chain L93-3.
J729	4033513P4	Contact, electrical: sim to Bead Chain L93-3.
J732 and J733	4033513P4	Contact, electrical: sim to Bead Chain L93-3.
J735 thru J737	4033513P4	Contact, electrical: sim to Bead Chain L93-3.
		- - - - - - - - - - PLUGS - - - - - - - - - -
P701 thru P703	19C321106P1	Connector, printed wiring: 20 terminals rated at 5 amps per terminal.
		- - - - - - - - - - TRANSISTORS - - - - - - - -
Q701 thru Q706	19A115910P1	Silicon, NPN; sim to Type 2N3904.
Q707	19A115852P1	Silicon, PNP; sim to Type 2N3906.
Q708 thru Q716	19A115910P1	Silicon, NPN; sim to Type 2N3904.
Q717	19A115300P2	Silicon, NPN; sim to Type 2N3053.
Q718 and Q719	19A115910P1	Silicon, NPN; sim to Type 2N3904.
Q720	19A115852P1	Silicon, PNP; sim to Type 2N3906.
		- - - - - - - - - - RESISTORS - - - - - - - - -
R701	19B209535P2	Variable, carbon film: 10,000 ohms ±20%, 1/4 w; sim to Mallory Style LCH-TM4.
R702	19B209535P1	Variable, carbon film: 10,000 ohms ±20%, 0.5 w; sim to Mallory Style LCH-TM4.
R703	3R152P152J	Composition: 1500 ohms ±5%, 1/4 w.
R704	3R77P511J	Composition: 510 ohms ±5%, 1/2 w.
R705	3R152P393J	Composition: 39,000 ohms ±5%, 1/4 w.
R706	3R152P100J	Composition: 10 ohms ±5%, 1/4 w.
R707	3R77P511J	Composition: 510 ohms ±5%, 1/2 w.
R708	3R152P103J	Composition: 10,000 ohms ±5%, 1/4 w.
R709	3R77P511J	Composition: 510 ohms ±5%, 1/2 w.
R712 thru R714	3R152P103J	Composition: 10,000 ohms ±5%, 1/4 w.
R715	3R152P272J	Composition: 2700 ohms ±5%, 1/4 w.
R716	3R152P471J	Composition: 470 ohms ±5%, 1/4 w.
R717	3R152P104J	Composition: 100,000 ohms ±5%, 1/4 w.
R718	3R152P823J	Composition: 82,000 ohms ±5%, 1/4 w.
R719	3R152P103J	Composition: 10,000 ohms ±5%, 1/4 w.
R720	3R152P334J	Composition: 330,000 ohms ±5%, 1/4 w.
R721 and R722	19C314256P21183	Metal film: 118,000 ohms ±1%, 1/4 w.
R723	3R152P271J	Composition: 270 ohms ±5%, 1/4 w.
R724	3R152P511J	Composition: 510 ohms ±5%, 1/4 w.
R725	19C314256P29532	Metal film: 95,300 ohms ±1%, 1/4 w.
R726	19B209358P106	Variable, carbon film: approx 300 to 10,000 ohms ±20%, 0.25 w; sim to CTS Type X-201.
R727	3R151P104J	Composition: 100,000 ohms ±5%, 1/8 w.
R728	3R151P512J	Composition: 5100 ohms ±5%, 1/8 w.
R729	3R151P223J	Composition: 22,000 ohms ±5%, 1/8 w.
R730	3R151P153J	Composition: 15,000 ohms ±5%, 1/8 w.
R731	3R77P511J	Composition: 510 ohms ±5%, 1/2 w.
R732	3R151P153J	Composition: 15,000 ohms ±5%, 1/8 w.
R733 and R734	3R152P153J	Composition: 15,000 ohms ±5%, 1/4 w.
R735	3R152P102J	Composition: 1000 ohms ±5%, 1/4 w.
R736	3R78P910J	Composition: 91 ohms ±5%, 1 w.
R737	3R152P104J	Composition: 100,000 ohms ±5%, 1/4 w.
R738 thru R744	3R152P103J	Composition: 10,000 ohms ±5%, 1/4 w.
R745	3R151P513J	Composition: 51,000 ohms ±5%, 1/8 w.
R746	3R151P512J	Composition: 5100 ohms ±5%, 1/8 w.
R747	3R151P104J	Composition: 100,000 ohms ±5%, 1/8 w.
R748	3R152P102J	Composition: 1000 ohms ±5%, 1/4 w.
		- - - - - - - - - - SWITCHES - - - - - - - - -
S701	19B209563P1	Push: 4PDT, momentary, 1.1 amp at 14 VDC; sim to Switchcraft Series 70,000.
S702	19B209559P1	Rotary: 1 section, 12 positions (adj stops); sim to Oak Mfg. 5-68511-411.
S703	19B209563P1	Push: 4PDT, momentary, 1.1 amp at 14 VDC; sim to Switchcraft Series 70,000.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - -
U701	19A116180P2	Digital, Quad 2-Input Nand Gate (Open Collector); sim to Texas Instrument Type SN7401.
U702	19A116180P20	Digital, Hex Inverter; sim to Texas Instrument Type SN7404.
U703	19A116180P14	Digital, J-K Master-Slave Flip-Flop; sim to Texas Instrument Type SN7472.
U704	19D424078G1	Mute Hybrid.
		- - - - - - - - VOLTAGE REGULATORS - - - - - - - -
VR701	4036887P11	Silicon, Zener.
VR702	4036887P56	Silicon, Zener.
		- - - - - - - - - - MISCELLANEOUS - - - - - - - - - -
	19B226484G1	Frequency Indicator Knob.
	19B226463G1	Component Board. (Locates CR709).
	19A121360P3	Spacer. (Located between component board and Housing at S702).
	19B226571G1	Knob. (Used with R701 and R702).
	NP276443	Nameplate, frequency. (1-12).
	19C321004P1	Lens. (S701-PWR).
	NP276459P19	Nameplate. (PWR).
	19A130261G1	Contact. (Located between P701, P702, P703 and Control Module Board).
	4036555P1	Insulator, washer: nylon. (Used with Q717).
	NP276459P10	Nameplate. (SRCH).
	19B226331P1	Actuator. (Used with S701, S703).
	19B226334P1	Pushbutton. (Used with S701, S703).

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by these revisions.

REV. A - Incorporated in initial shipment.

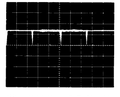
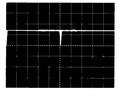
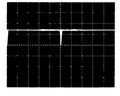
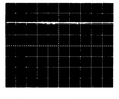
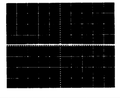
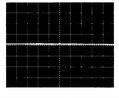
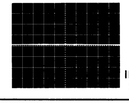
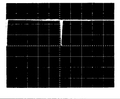
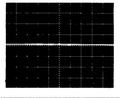
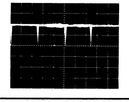
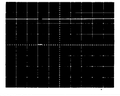
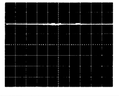
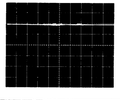
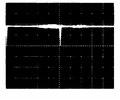
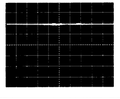
WAVEFORMS

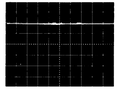
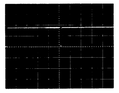
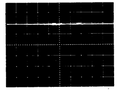
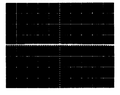
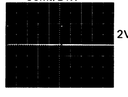
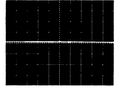
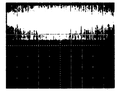
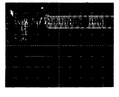
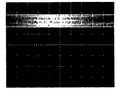
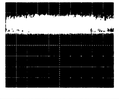
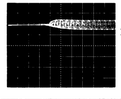
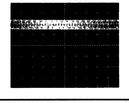
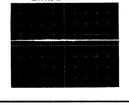
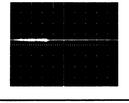
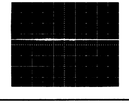
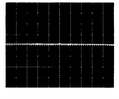
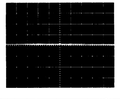
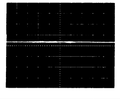
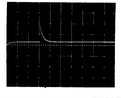
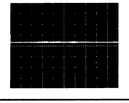
All waveforms were taken at Test Points (A) thru (R) as shown on the outline and schematic diagrams. When applicable, the waveforms are shown for three different modes of operation as follows:

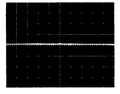
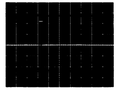
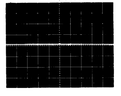
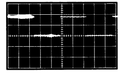
1. Receiver Squelched (PSLM Searching)
2. Receiver Unsquelched (Receiving Non-Priority Channel)
3. Receiver Unsquelched (Receiving Priority Channel)

NOTE

All waveforms are taken using Test Point A as the SYNC SOURCE (Trigger Pulse) except where NOTED.

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL	RECEIVING PRIORITY CHANNEL
(A)	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div.
(B)	 10ms/Div. 2V/Div.	 10ms/Div. 2V/Div.	 10ms/Div. 2V/Div.
(C)	 10ms/Div. 2V/Div. NOTE: INTERNAL SYNC	 50ms/Div. 2V/Div.	 10ms/Div. 2V/Div.
(D)	 50ms/Div. 2V/Div.	 10ms/Div. 2V/Div.	 10ms/Div. 2V/Div.
(E)	 10ms/Div. 2V/Div.	 50ms/Div. 2V/Div.	 10ms/Div. 2V/Div.

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL	RECEIVING PRIORITY CHANNEL
(F)	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div.
(G)	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div.	 50ms/Div. 2V/Div.
(H)	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.
(J)	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.
(K)	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.
(L)	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.
(M)	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.

TEST POINT	RECEIVER SQUELCHED	RECEIVING NON-PRIORITY CHANNEL	RECEIVING PRIORITY CHANNEL
(N)	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.	 2ms/Div. 2V/Div.
(P)	 50ms/Div. 2V/Div. INTERNAL SYNC	1ms/Div. 2V/Div. INTERNAL SYNC	50ms/Div. 2V/Div. NOTE: INTERNAL SYNC
(R)	50ms/Div. 2V/Div. INTERNAL SYNC	1ms/Div. 2V/Div. INTERNAL SYNC	50ms/Div. 2V/Div. NOTE: INTERNAL SYNC