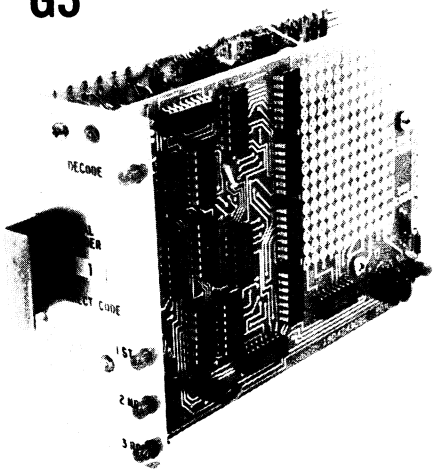
MOBILE RADIO

MASTR™ II MAINTENANCE MANUAL

DIGITAL DECODER MODELS 19C327520G1 - G3



SPECIFICATIONS *

Model Number	Tone Input
19C327520G1	590 Hz (Not Available)
19C327520G2	1500 Hz
19C327520G3	2805 Hz
Pulsing Speed	8 to 16 PPS (10 PPS Nominal)
Input Impedance	50K ohms
Audio Sensitivity	
590 & 1500 Hz	0.12 to 6.0 Volts @ 10 dB SINAD
2805 Hz	0.12 to 6.0 Volts @ 14 dB SINAD
Input Power	12.6 VDC at 175 milliamperes (add 20 milliamperes for relay)
Temperature Range	-30°C to +60°C (-22°F to +140°F)

These specifications are intended primarily for the use of the serviceman. Refer to the appropriate Specification Sheet for the complete specifications.

GENERAL ELECTRIC

Maintenance Manual LBI-30624
DATAFILE FOLDER DF-5046

DIGITAL DECODERS 19C327520G1-G3

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WARNING

No one should be permitted to handle any portion of the equipment that is supplied with voltage; or to connect any external apparatus to the units while the units are supplied with power. KEEP AWAY FROM LIVE CIRCUITS!

DESCRIPTION

The General Electric Digital Decoders Models 19C327520G1-G3 are solid-state, single-tone decoders that plug into the auxiliary jacks of the MASTR II Base Station Control Shelf mother board.

The decoder responds to a tone that is interrupted by a telephone-type dial to form a series of pulses corresponding to the digit dialed. A seven-digit code (Code 1) may be used for individual "station" calls; a four-digit code (Code 2) may be used for "group" calls; a four-digit code (Code 3) may be used for "all call".

A relay may be added to the decoder assembly whenever additional external control functions are desired.

PRELIMINARY ADJUSTMENTS

The decoder is normally shipped from the factory set to operate on the following codes:

- Code 1: 6-5-4-3-2-1
- Code 2: 0-9-8-7
- Code 3: 4-3-2-1

Before placing the decoder into operation, new code assignments and new code settings are normally required. Complete instructions for setting codes are provided in the Code Setting Procedure (see Table of Contents).

CIRCUIT ANALYSIS

(Refer to Figure 1)

The basic decoder consists of a tone receiver/pulse routing board and a counter board.

The decoder is fully transistorized, using both discrete components and Integrated Circuit Modules (IC's) for increased reliability. Typical schematic and logic diagrams of the IC's used in the decoder are listed in the Table of Contents.

TONE RECEIVER & PULSE ROUTING BOARD

TONE RECEIVER

Two different tone receiver and pulse routing boards are available for use in the decoder, depending on the system frequency. The operating frequency of each board is as follows:

- A1 - 590 Hz (not available)
- A2 - 1500 Hz
- A3 - 2805 Hz

Each tone receiver consists of an amplifier-limiter, a tuned circuit, a detector and regulator, and an output switch.

6-VOLT REGULATOR AND TONE RECEIVER

Operating voltage for the decoder is supplied by the 6-volt regulator. +13 volts

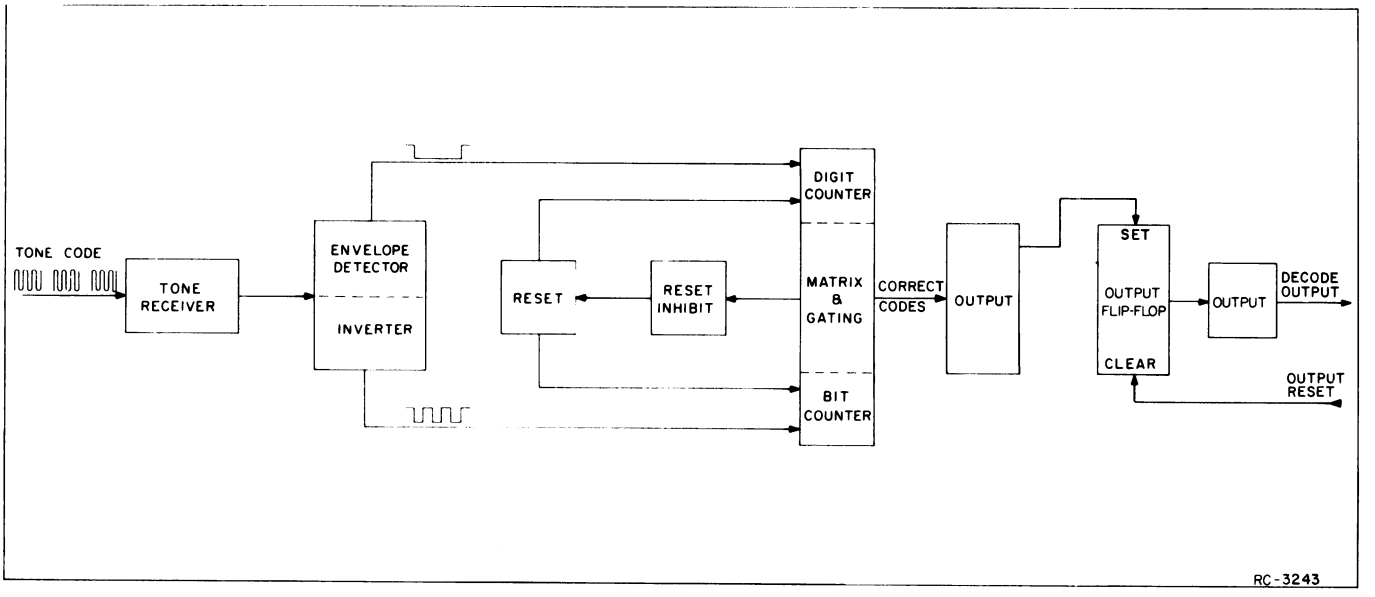


Figure 1 - Decoder Block Diagram

from the station power supply is applied to the zener diode-emitter follower regulator (VR1 and Q1). The +6-volt, 250-milliamp output is taken from the emitter of Q1.

A coded tone from the station receiver is coupled through DC blocking capacitor C2 to amplifier-limiters Q2 and Q3. A negative feedback path from the collector of Q2 to diode limiters CR4 and CR5 limits the signal applied to the base of Q3. Diodes CR2 and CR3 provide large-signal protection for Q2. The output of Q3 is applied to a tuned circuit consisting of C9/C10, C11/C12/C13 and L1/L2.

When an incorrect tone (or no tone) is applied to the tuned circuit, diode CR6 is forward biased by current through L1/L2. With CR6 conducting, detector Q4 is turned off. This allows diode CR7 to conduct, keeping output switch Q6 turned off.

Applying the correct tone to the tuned circuit increases the impedance of L1/L2, removing the bias on CR6. The diode now conducts only on the positive half-cycles of tone, and is cut off (reverse biased) on the negative half cycles. When a negative half cycle turns CR6 off, Q4 turns on. Turning on Q4 turns off CR7, which forward biases CR8 and CR9 and turns on output switch Q6. When a positive half cycle turns CR6 on (and Q4 off), C24 starts discharging through R18 and R19, keeping CR7 off and Q6 on. The output of Q6 is a positive pulse for each interruption in the tone code. Q5 acts as a regulator, keeping the emitter voltage of Q4 constant over the temperature range.

PULSE ROUTING

The pulse routing section contains the inverters, envelope detector, tone-off reset, reset, and output stages. Multiple-input Integrated Circuits (IC's) are used for the inverters, envelope detector, control latch flip-flop and reset circuits. Discrete transistors are used for the tone-off reset and output stages, and in the envelope detector.

Figure 2 contains a complete set of decoder timing waveforms. It is recommended that these waveforms be used in conjunction with the circuit analysis for a better understanding of the decoder circuitry.

1ST INVERTER

The output of the tone receiver is connected to input terminal 1 of the 1st inverter (U1A).

When no tone is applied to the decoder, the output of the tone receiver is high (positive) and the output of the inverter is low (zero). When tone is first applied the inverter output goes positive. The positive-going pulses (one for each interruption in the tone) from the tone receiver are changed to negative-going pulses by the inverter. These negative-going pulses are applied to the trigger of the BIT COUNTER input via P1-3.

The inverter output is also applied to the input of the envelope detector and the tone-off reset circuits.

ENVELOPE DETECTOR

With no tone applied, the zero inverter output of U1-A is applied to terminal 1 of the envelope detector OR gate, resulting in a positive output.

When tone is first applied to the decoder, the inverter output goes positive. This positive potential is applied to terminal 1 of the OR gate, and also turns on Q7 so that its collector drops to zero. This keeps the OR gate output positive for as long as Q7 conducts. Q7 conducts until C18 is fully charged, and then turns off. This causes the OR gate output to drop to zero.

The first negative-going pulse in the pulse train from the inverter switches the OR gate output to positive, and also causes C18 to rapidly discharge through CR10 and CR12. The trailing edge of the first pulse (now positive-going) turns on Q7, keeping the OR gate output positive. This cycle is repeated until the end of the digit pulse train and results in a positive pulse envelope for the digit pulses. This positive pulse envelope is applied via P1-4 to the DIGIT COUNTER input.

TONE-OFF RESET

When tone is first applied, the positive inverter output of the first inverter turns on Q8, and also charges C19 through CR11. Turning on Q8 turns off normally-on transistor Q9 so that its collector goes positive.

The negative-going digit pulses applied to the tone-off reset circuit causes C19 to discharge through R25 and the base-emitter junction of Q8, which keeps Q8 on. The output of Q9 remains positive until tone is removed from the decoder and C19 discharges. The output of Q9 is applied to the reset circuit.

RESET

The reset circuit consists of two NAND gates utilized as negative OR gates (U1B,C) driving a NAND gate (U2B). A simplified reset circuit and the truth table for all of the gates is shown in Figure 3. When both OR gate outputs are positive, the NAND gate output goes negative, resetting the counter logic.

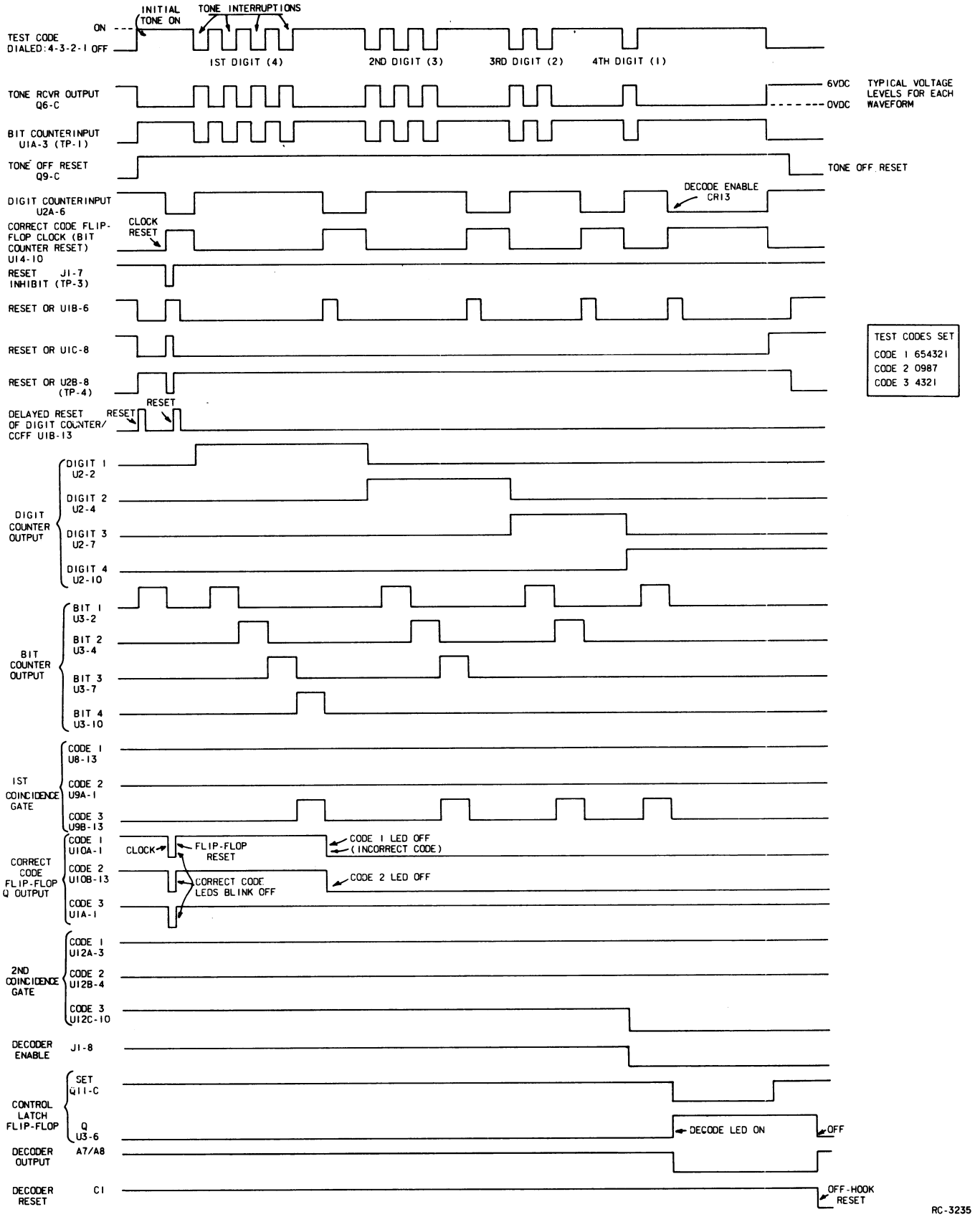


Figure 2 - Decoder Waveform Chart

With no tone applied to the decoder, input A to each OR gate is at zero, holding the NAND gate in the reset condition.

When tone is applied, the positive output of Q9 keeps terminal A of both OR gates positive. Terminal B of the first OR gate is kept positive through R30, and the output of OR gate is "0". In the second OR gate, terminal A is positive and terminal B is held at "0" by the correct code detector so that the second OR gate output is positive. The zero and positive inputs to the NAND gate keep its output high, preventing the counter logic from resetting.

At the end of the first digit, a negative pulse from the envelope detector is coupled through C21 to terminal 4 of the OR gate, causing its output to go positive momentarily. At the same time, if a correct code has been applied to the counter logic, the output of correct code detector (OR gate) remains positive and is applied to terminal B of the second OR gate. Now, the output of the first reset OR gate is positive, and the second OR gate is zero, keeping the NAND gate output positive (no reset).

If an incorrect code is dialed, the correct code detector output goes to zero and both OR gate outputs go positive at the end of the incorrect digit. This switches the NAND gate output to zero, resetting the counter logic.

OUTPUT

When no code is applied to the decoder, the positive output of the 2ND COINCIDENCE GATE on the counter board is connected through R32 to the base of output transistor Q10, keeping the transistor turned off. Dialing a correct code switches the output of the 2ND COINCIDENCE GATES to ground. This causes current to flow in the emitter-base junction of Q10, turning the transistor on (see Figure 4).

When Q10 is turned on, the positive voltage on its collector causes current to flow in the base-emitter junction of Q11, turning it on. Turning on Q11 applies ground to terminal 10 of the CONTROL LATCH FLIP-FLOP, setting the flip-flop. This causes terminal 6 to go positive, back biasing diode CR15. Back biasing CR15 removes the shunt from the base of Q12, permitting current to flow in the base-emitter junction of the transistor and turning it on. This forward biases CR16 turning on Q13. When turned on, Q13 completes a current path on the Channel Guard Control Board, disabling the Channel Guard function.

Coming off-hook at the remote control console disables the Channel Guard Board. Ground is applied to terminal 5 of the CONTROL LATCH FLIP-FLOP, removing the positive output at terminal 6. CR15 is now forward biased, turning off Q12 and Q13.

EXTERNAL CONTROL RELAY

A relay (5491595P12) and spike suppressor diode (4037822P1) may be mounted on the decoder Tone Receiver and Pulse Routing Board whenever external control functions are required. The relay provides two form-C, contacts for the desired switching functions.

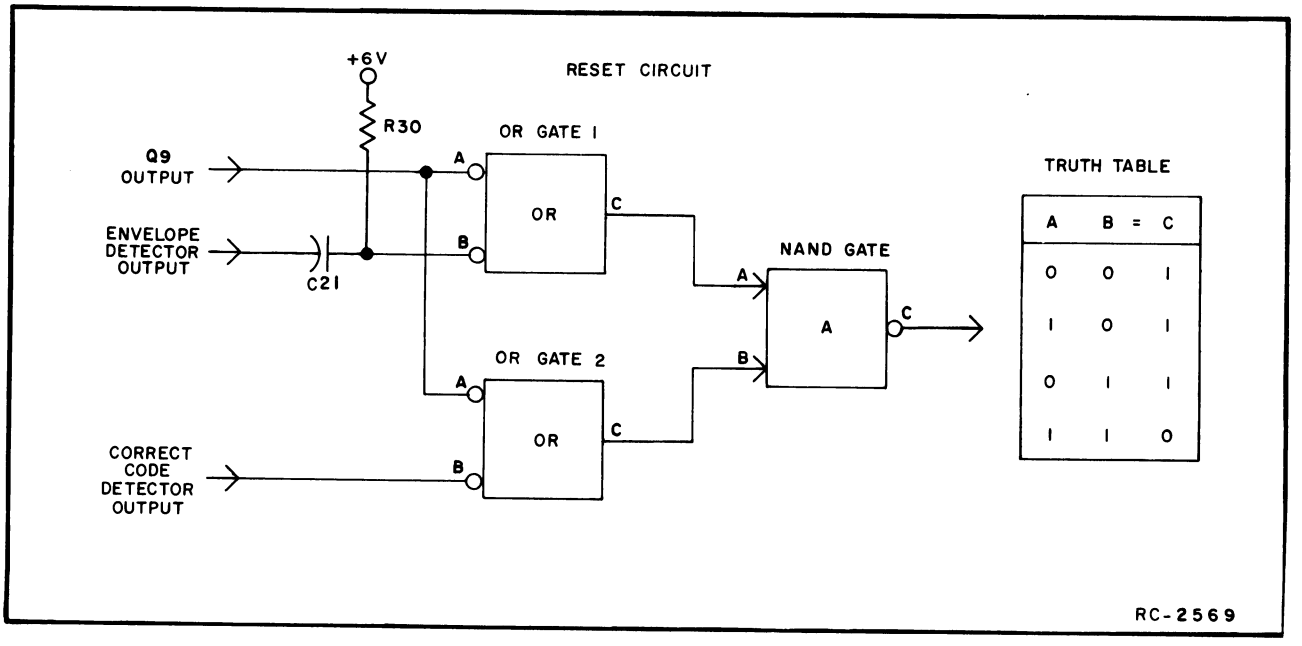


Figure 3 - Reset Circuit

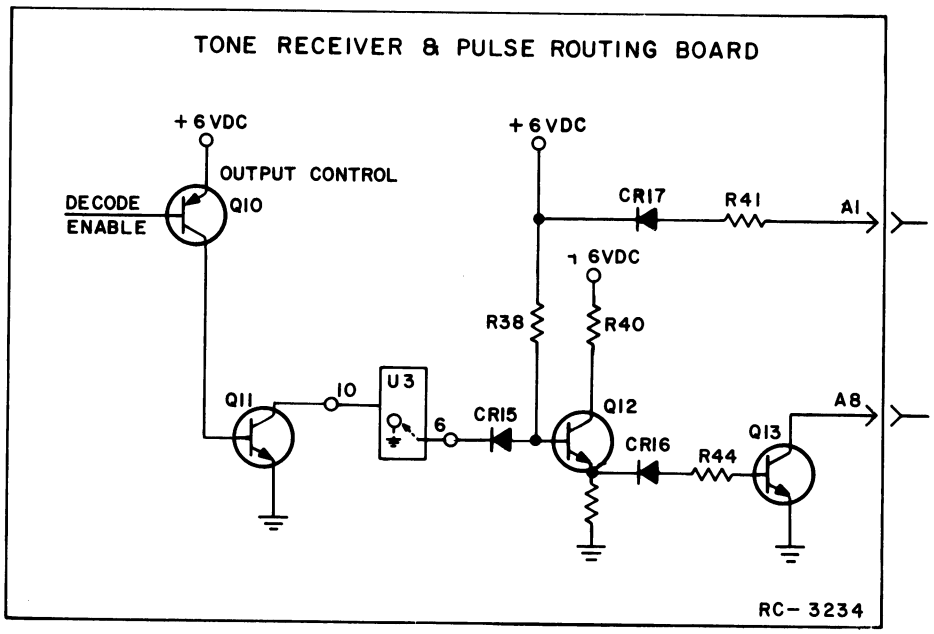


Figure 4 - Output Control Circuits

Mounting locations and connections for the relay and circuitry are shown on the decoder Outline and Schematic Diagrams.

COUNTER BOARD

The counter board consists of the Digit Counter IC (U2), the Bit Counter IC (U3), the 1st and 2nd Coincidence Gates (U8, U9 and U12), buffers (U11, U14 and U15), Correct Code Flip-Flops (U10), Reset Delay One-Shot (U1) and Output NOR Gates (U13). A simple solder-bridge matrix is used for programming the desired codes. A glance at the matrix indicates the programmed codes. Complete instructions for setting up to three different codes are provided in the Code Setting Procedure (see Table of Contents). One seven-digit code and two four-digit codes may be programmed on the matrix.

The counter board schematic diagram is shown programmed for a Code 1 six-digit code: 6-5-4-3-2-1; a Code 2 four-digit code: 0-9-8-7; a Code 3 four-digit code: 4-3-2-1. These are test codes set at the factory and the jumpers on the matrix must be clipped before soldering in new codes.

Four LED code indicators are provided on the counter board. The DECODE indicator (CR1) is turned on after the last digit of the correct code is decoded. The CORRECT CODE LEDs will be turned on when the decoder is reset.

After the first digit of the correct first code is decoded, the 1ST CORRECT CODE LED (CR2) should remain on while the 2ND and 3RD CORRECT CODE LEDs (CR3 and CR4) should turn off. After the last digit of the correct first code is decoded, the DECODE LED should be on, the 1ST CORRECT CODE LED should be on and the 2ND and 3RD CORRECT CODE LEDs should be off. When the second correct code is decoded, the DECODE LED should be on; the 2ND CORRECT CODE LED should be on and the other two CORRECT CODE LEDs should be off. When the third correct code is decoded, the DECODE LED should be on; the 3RD CORRECT CODE LED should be on and the other two CORRECT CODE LEDs should be off.

When the RESET pulse is applied to J1-5, the pulse is connected to the RESET One-Shot U1-B through buffer U15-B. The One-Shot delays the RESET applied to the digit counter and the Correct Code Flip-Flops. Assume that the third test code (4-3-2-1) is dialed into the decoder (refer to the timing waveforms in Figure 2). When the first digit (4) is received at the decoder, one pulse is applied to the Digit Counter (terminal 14) through buffer U15-A and four pulses are applied to the Bit Counter (terminal 14) through buffer U15-C. The end of the first digit count will make the 3RD CODE DIGIT 1 bus on the solder bridge matrix go high. This high will be applied to terminal 12 of NAND gate U6-D. Simultaneously, the Digit Counter will apply a high to terminal 13 of U6-D. The resultant low output of U6-D (terminal 11) will be applied to terminal 12 of NOR gate U9-B.

All other inputs to U9-B (the CODE 3 1ST COINCIDENCE GATE) are high. The

resultant high at U9B-13 is applied to the DATA terminal (5) of Correct Code Flip-Flop U1-A. The DIGIT COUNTER INPUT at J1-4 is inverted by U14-D and is applied to the CLOCK terminal (3) of all three Correct Code Flip-Flops (U1-A, U10-A, U10-B). The positive-going trailing edge of the digit count causes U10-A and U10-B to change state, turning off CORRECT CODE LEDs CR2 and CR3. The data input lines to U10-A and U10-B are both low. The positive data line input to U1-A prevents U1-A from changing state. 3RD CORRECT CODE LED CR4 thus remains on.

The $\overline{Q}$ outputs of U10-A and U10-B are now high and applied to two inputs of NOR gate U13-B. The $\overline{Q}$ output of U1-A is low and is applied to the third input of U13-B. The positive output of U13-B is applied to the reset circuit through buffer U11-E to inhibit the decoder reset.

After the last digit (1) of the code is decoded, the high at the Q output (terminal 1) of U1-A is applied to terminal 9 of 2ND COINCIDENCE gate U12-C. The digit count lead "P" (digit 4) is high and is connected via jumper H12-H14 to terminal 8 of U12-C. The resultant low at terminal 10 is applied to terminal 5 of NOR gate U13-A. The other two inputs to U13-A are high. The high output of U13-A is inverted by buffer U14-E and the resultant low is connected to the DECODE ENABLE lead to latch the Control Latch Flip-Flop in the decode mode. The high at terminal 6 of the Control Latch Flip-Flop on the decoder board is applied through J1-6 to the base of Q1, turning the transistor on. Conduction of Q1 operates the DECODE indicator LED CR1.

If an incorrect digit is decoded, the lack of a high applied to the DATA input of U1-A during its clock pulse will cause the Q output (terminal 1) to go low. This low will be inverted by U12-D, applying a high on the reset line of U1-A. The flip-flop will remain in this state until a high is received on the set lead which will reset U1-A. The RESET INHIBIT will be removed from J1-7, allowing the digit counter and correct code flip-flops to reset.

Three auxiliary output buffers (U14-B, U14-C and U14-F) are connected to the output of the 2ND COINCIDENCE gates. Each buffer output will deliver a maximum of 3 milliamps when in the high state (2ND COINCIDENCE gate output low) and 1 milliamp when in the low state.

MAINTENANCE

DISASSEMBLY

To service the Decoder board turn off the power switch on the Base Station Power Supply and unplug the Decoder board. The counter board is located on the right side of the Decoder for ease of code set up. The Tone Receiver and Pulse Routing Board is on the left side.

TROUBLESHOOTING

To troubleshoot the Decoder board remove the power as described above and unplug the Decoder board. Plug the Decoder board into the extender board (19D417458G1). The extender board extends the connections at the system board jacks to the pin jacks on the Decoder board so that the Decoder circuits on the card are beyond other cards mounted on the system board. This allows convenient access to the circuits for troubleshooting with all operating voltages applied.

Procedures for troubleshooting the decoder include DC readings and waveforms for the tone receiver, pulse routing and counter boards. Refer to the Troubleshooting Procedure as listed in the Table of Contents.

TONE RECEIVER ADJUSTMENT

Coil L1/L2 on the tone receiver and pulse routing board is the only adjustment on the decoder. This coil is set at the factory and will normally require no further adjustment unless it is necessary to replace L1/L2, C9/C10 or C11/C12/C13. If any of these components are replaced, adjust L1/L2 as follows:

1. Connect a VTVM across C9/C10 or C11/C12/C13.
2. Apply a continuous tone to the decoder at the proper operating frequency (590 Hz, 1500 Hz or 2805 Hz).
3. Tune L1/L2 for maximum meter reading.

TROUBLESHOOTING PROCEDURE

EQUIPMENT REQUIRED

- DC-triggered oscilloscope
- AC and DC VTVM
- A tone generator of the proper frequency and a telephone-type dial, or a TGS-735 or TGS-740 encoder on the proper frequency
- A 12-volts, DC power supply

PRELIMINARY INSTRUCTIONS

1. All waveforms shown are with the proper tone applied and the digit 5 dialed. Note: the digit 6 was dialed for the incorrect code reset waveform shown.
2. The oscilloscope setting for all waveforms is 5 volts/division vertical and 100 milliseconds/division horizontal except where noted.
3. Before starting the procedure, check for +6 volts DC at the emitter of regulator transistor Q1. Then check for +6 volts on the Counter Board.

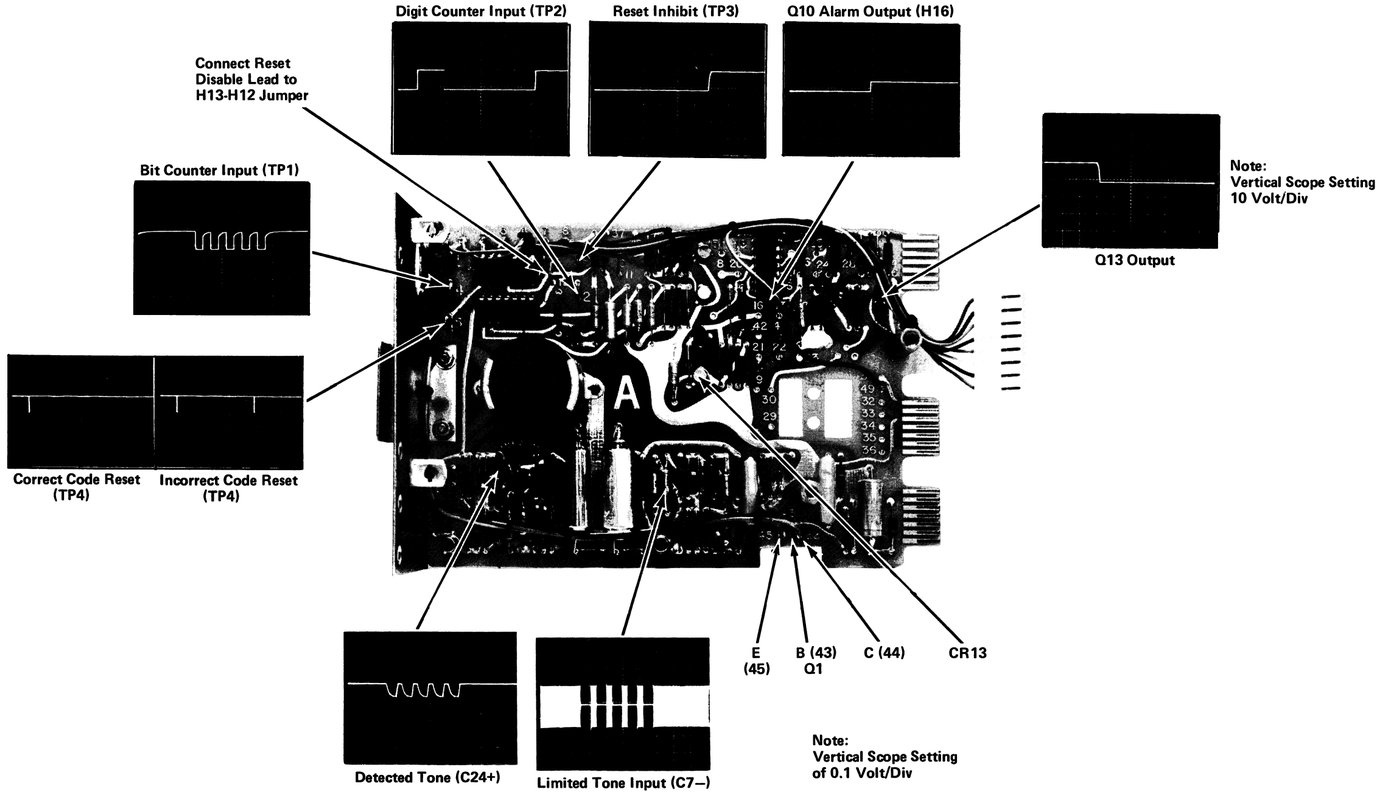
CAUTION

The CMOS Integrated Circuit devices used in this equipment can be destroyed by static discharges. Before handling one of these devices, the serviceman should discharge himself by touching the case of a bench test instrument that has a 3-prong power cord connected to an outlet with a known good earth ground. When soldering or de-soldering a CMOS device, the soldering iron should also have a 3-prong power cord connected to an outlet with a known good earth ground or a battery-operated soldering iron should be used.

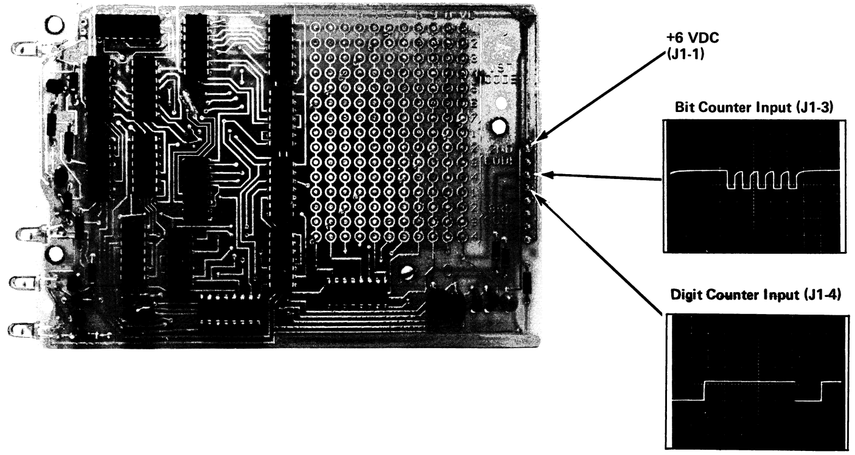
SYMPTOM	PROCEDURE
Decoder responds to wrong code.	1. Check the solder bridging for the correct code on the Counter Board (refer to the Code Setting Procedure as listed in the Table of Contents).
Decoder does not respond to correct code	1. Check the solder bridging on the Counter Board (refer to the Code Setting Procedure listed in the Table of Contents). Check continuity of solder bridge connections with ohmmeter. 2. Dial a correct code digit and check the waveforms at TP1 and TP2. (Note that the digit "5" was dialed to produce the waveforms shown.) If the proper waveforms are not present, check the tone receiver. If proper waveforms are obtained, proceed to Step 3. 3. Connect a jumper from pin 15 (RESET) of Bit Counter U3 to ground. **CAUTION** The jumper connected from pin 15 of U3 to ground should only be left connected for a period not to exceed 60 seconds to prevent possible damage to the CMOS device. 4. Dial the correct first digit for the code and keep the tone on after dialing. In row 1 of the code being tested, the solder bridge should measure approximately +6 VDC which indicates that the first digit was counted correctly.

SYMPTOM	PROCEDURE
Decoder does not respond to correct code (cont'd)	5. Remove the jumper from pin 15 of U3 to ground and dial a "1" to reset the counter. Reconnect the jumper from pin 15 of U3 to ground. 6. Dial each of the remaining digits of the code, checking the solder bridge in the correct row for each digit dialed. The solder bridge should read +6 VDC after each digit dialed if the digit was counted correctly. Repeat Step 5 after checking each digit. 7. If the digits are all counted correctly, refer to the waveform chart in Figure 2 and make waveform checks at all points indicated on the chart while dialing the correct code. 8. Connect the reset disable jumper (H12-H13) to ground to prevent the digit counter from re-setting while dialing (see illustration). Dial the correct code. If all codes are counted correctly, this indicates a fault in the reset circuit. Check the correct code, incorrect code reset and reset inhibit waveforms. Refer to the Circuit Analysis section for detailed operation of the reset circuits. 9. With the reset disable jumper (H12-H13) connected to ground, dial a correct code and check the waveforms at J1-3 and J1-4. If the waveforms are not correct, check the tone receiver or the envelope detector circuits.
No tone output from tone receiver	1. While applying 100 millivolts of on-frequency tone, dial a correct code digit and check the waveform at C7. If the proper waveform is not present, check the tone receiver input circuit. 2. With tone applied, dial a correct code digit and check waveform at C24. If the proper waveform is obtained, check CR7, CR8, CR9 and Q6. If proper waveform is not obtained, check for a sine wave across L1/L2. 3. If the sine wave is present across L1/L2, connect a jumper across L1/L2 and check for a near zero reading at the positive end of C24. If the reading is not near zero, check CR6, Q4 and Q5.
No tone output at high input levels but operates normally at low input levels	1. Check C5, C7, CR4, CR5, R5 and R6 in the limiter circuit.

TONE RECEIVER & PULSE ROUTING BOARD



COUNTER BOARD



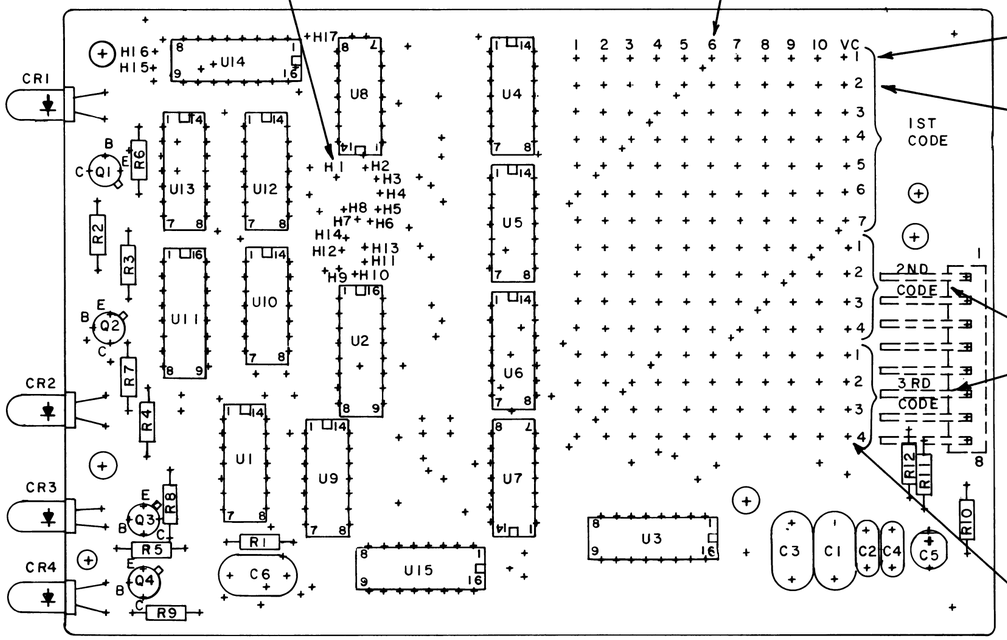
(8) THE TOTAL NUMBER OF DIGITS USED IN A CODE MUST BE SET BY CONNECTING JUMPERS BETWEEN THE DIGIT COUNT LEADS AND THE 2ND COINCIDENCE GATES. MAKE THESE JUMPER CONNECTIONS AS OUTLINED IN THE FOLLOWING TABLE.

NO. OF DIGITS	CONNECT	JUMPER
IN IST CODE	FROM	TO
1	H1	H2
2	H1	H3
3	H1	H4
4	H1	H5
5	H1	H6
6 *	H1	H7
7	H1	H8
IN 2ND CODE	FROM	TO
1	H9	H2
2	H9	H3
3	H9	H10
4 *	H9	H11
IN 3RD CODE	FROM	TO
1	H12	H2
2	H12	H3
3	H12	H13
4 *	H12	H14

* PRESET AT THE FACTORY FOR THE TEST CODE.

(1) CLIP ALL JUMPERS OF THE TEST CODE ON THE MATRIX.

(2) IN THE IST CODE SECTION OF THE MATRIX, LOCATE THE FIRST DIGIT OF THE DESIRED CODE UNDER THE NUMBER MARKED AT THE TOP OF THE MATRIX.



(3) MAKE A SOLDER BRIDGE BETWEEN THE CENTER AND OUTER RING IN ROW 1 OF THE FIRST CODE UNDER THE DIGIT LOCATED IN STEP 1

(4) LOCATE THE SECOND DIGIT OF THE IST CODE AT THE TOP OF THE MATRIX AND MAKE A SOLDER BRIDGE IN ROW 2 UNDER THE DIGIT LOCATION.

(5) CONTINUE THIS PROCEDURE FOR ALL DIGITS OF THE IST CODE.

(6) IN THE 2ND AND 3RD CODE SECTIONS OF THE MATRIX, FOLLOW THE SAME PROCEDURE AS OUTLINED ABOVE.

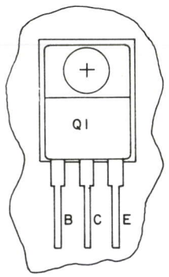
(7) ALL UNUSED INPUT LEADS TO THE COUNTERS MUST BE TERMINATED BECAUSE OF THE NATURE OF THE CMOS DEVICES USED. THEREFORE, MAKE A SOLDER BRIDGE IN THE VACANT CODE (VC) COLUMN OF THE MATRIX FOR ALL UNUSED DIGITS.

NOTE

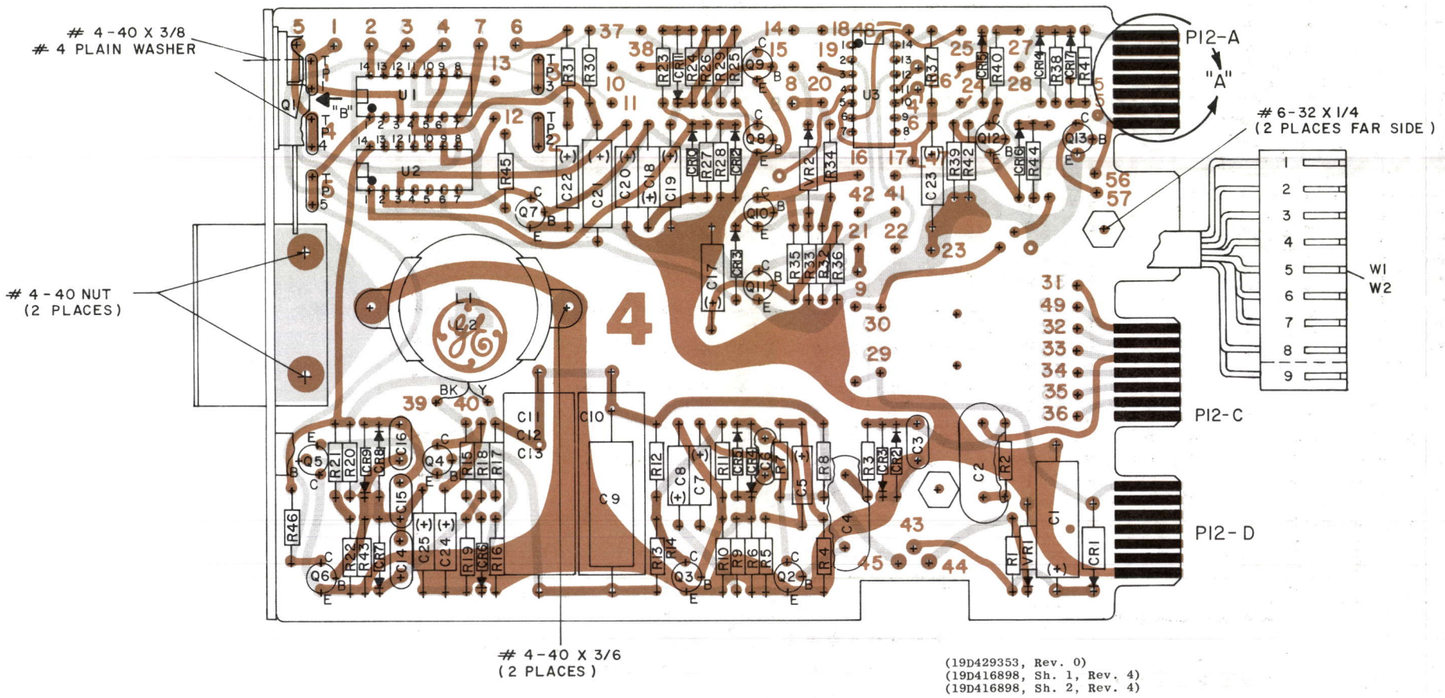
A CONTINUITY CHECK OF EACH SOLDER BRIDGE SHOULD BE MADE AFTER ALL CODES HAVE BEEN SET. USING A LOW NUMBER (SUCH AS "1") AS THE FIRST DIGIT IN A CODE IS NOT RECOMMENDED BECAUSE THE DELAY IN ATTACK TIME OF THE SYSTEM MAY CAUSE A MISCOUNT.

RC-3236

CODE SETTING PROCEDURE



VIEW AT "B"



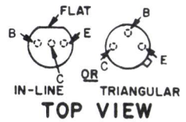
REFER TO WIRING DIAGRAMS FOR THE FOLLOWING CONNECTIONS			IN GRS	IN GRS
FROM	TO	WIRE	4,5,6	8,9,10
H12	H13	DA	X	X
H10	H11	DA	X	X
H25	H26	DA	X	X
H27	H28	DA	X	X
H37	H38	DA	X	X
H14	H15	DA	X	X
H41	H46	N22-R	X	
H47	H49	N22-R	X	
Q1-E	H45	SF24-BL	X	X
Q1-B	H44	SF24-G	X	X
Q1-C	H43	SF24-R	X	X
P1,P2-1	H2	SF24-R	X	X
P1,P2-2	H7	SF24-BK	X	X
P1,P2-3	H1	SF24-O	X	X
P1,P2-4	H3	SF24-BR	X	X
P1,P2-5	H5	SF24-BL	X	X
P1,P2-6	H48	SF24-Y	X	X
P1,P2-7	H6	SF24-V	X	X
P1,P2-8	H9	SF24-G	X	X
H55	H57	DA	X	
H41	H42	DA		X
H19	H20	DA		X
H21	H22	DA		X
P2-9	H8	SF24-W		X
H56	H57	DA		

(19D429353, Rev. 0)
(19D416898, Sh. 1, Rev. 4)
(19D416898, Sh. 2, Rev. 4)

8 9 10 11 12 13 14
7 6 5 4 3 2 1
SOLDER SIDE

DETAIL "A"
TYP. NUMBERING OF CONT. FINGERS

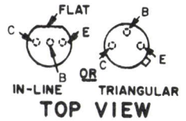
LEAD IDENTIFICATION
FOR Q3-Q6, Q8-Q11, & Q13



TOP VIEW

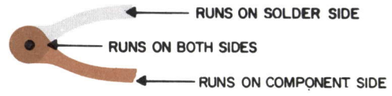
NOTE: LEAD ARRANGEMENT, AND NOT CASE SHAPE, IS DETERMINING FACTOR FOR LEAD IDENTIFICATION.

LEAD IDENTIFICATION
FOR Q2, Q7, & Q12



TOP VIEW

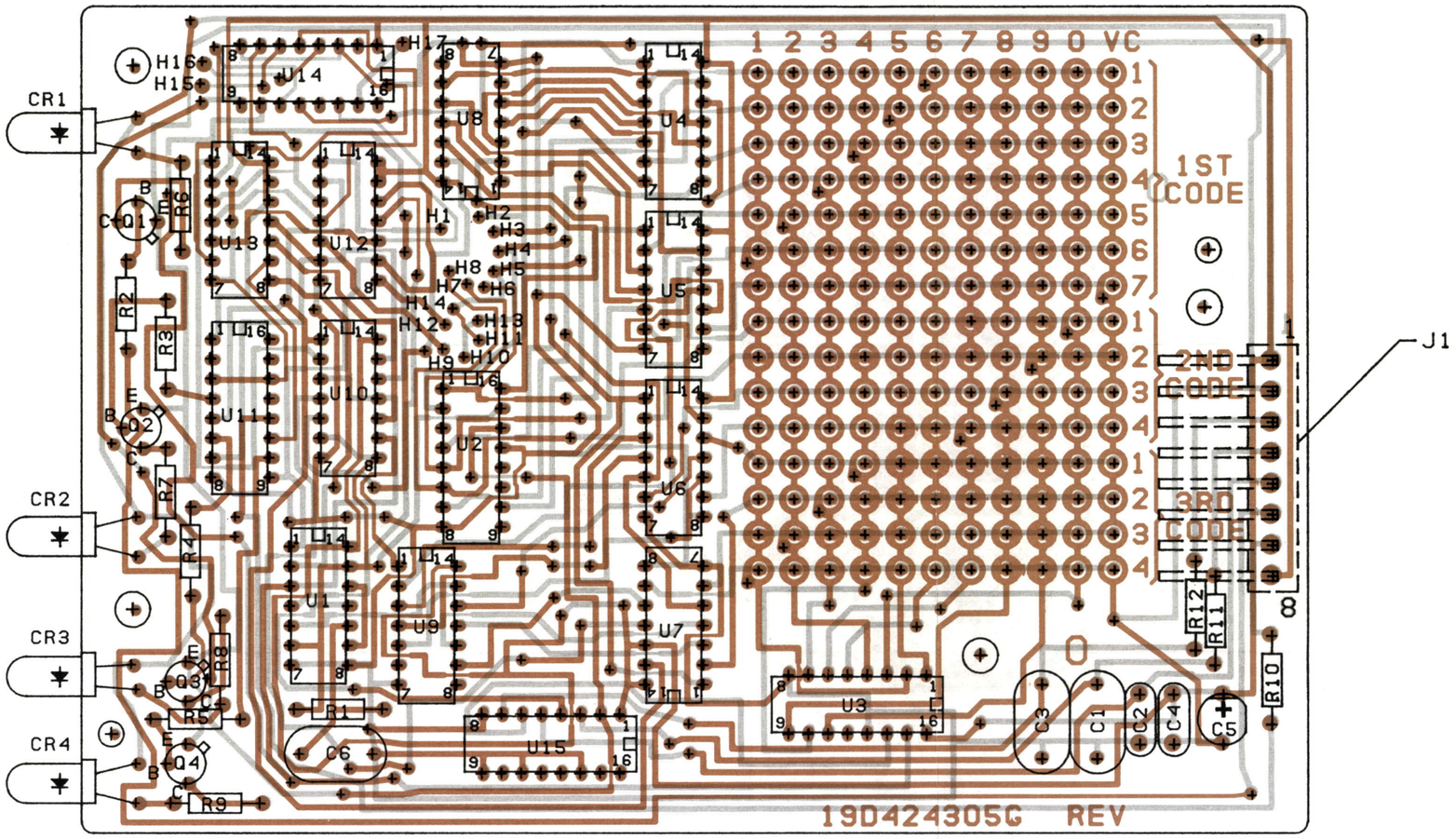
NOTE: LEAD ARRANGEMENT, AND NOT CASE SHAPE, IS DETERMINING FACTOR FOR LEAD IDENTIFICATION.



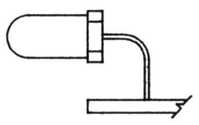
OUTLINE DIAGRAM

TONE RECEIVER AND PULSE ROUTING BOARD 19D416908G4-G6

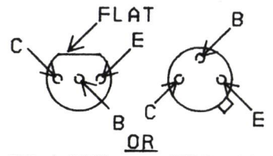
Issue 1



(19D424449, Rev. 1)
(19B227633, Sh. 1, Rev. 0)
(19B227633, Sh. 2, Rev. 0)



LEAD IDENTIFICATION
FOR Q1 THRU Q4

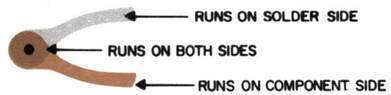


OR

IN-LINE TRIANGULAR

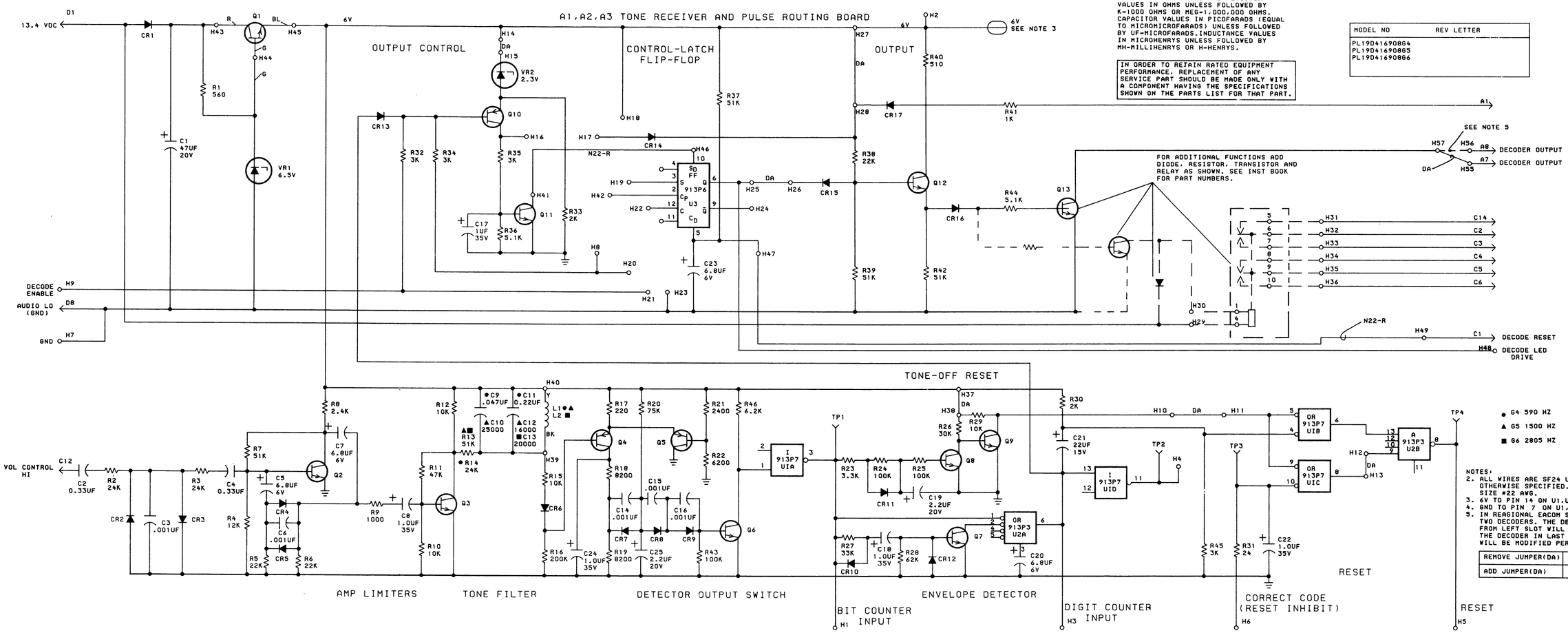
TOP VIEW

NOTE: LEAD ARRANGEMENT, AND NOT CASE SHAPE, IS DETERMINING FACTOR FOR LEAD IDENTIFICATION.



OUTLINE DIAGRAM

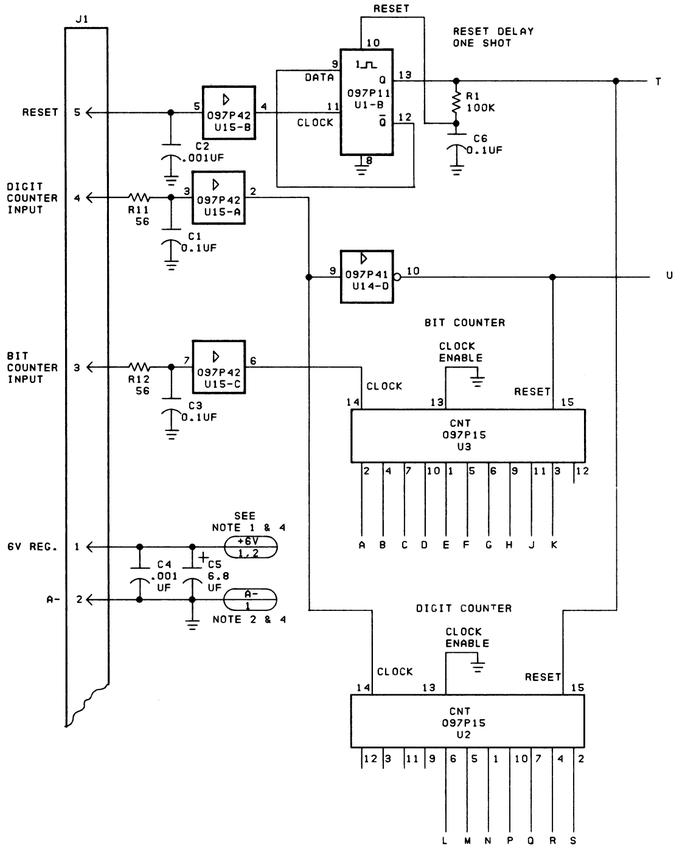
COUNTER BOARD 19D424305G1



(19R622253, Rev. 2)

SCHEMATIC DIAGRAM

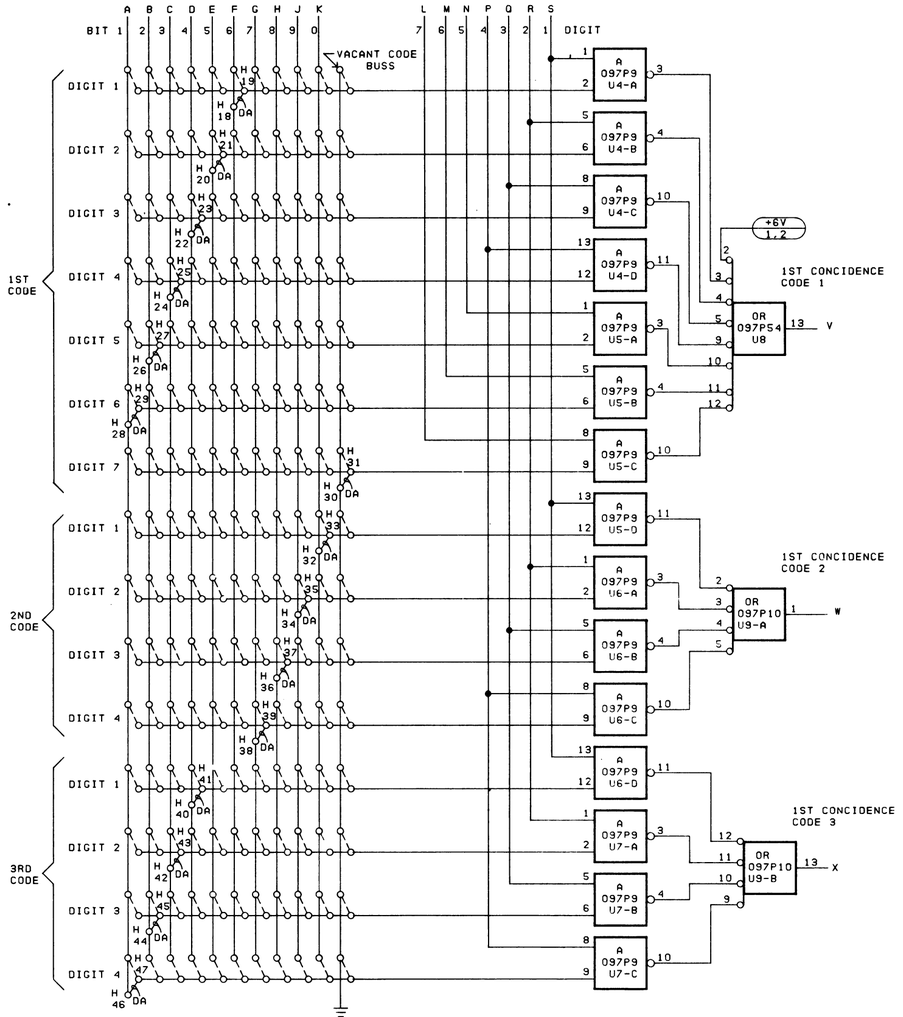
TONE RECEIVER AND PULSE ROUTING BOARD 19D416908G4-G6



IN ORDER TO RETAIN RATED EQUIPMENT PERFORMANCE, REPLACEMENT OF ANY SERVICE PART SHOULD BE MADE ONLY WITH A COMPONENT HAVING THE SPECIFICATIONS SHOWN ON THE PARTS LIST FOR THAT PART.

ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY K=1000 OHMS OR MEG=1,000,000 OHMS. CAPACITOR VALUES IN PICOFARADS (EQUAL TO MICROMICROFARADS) UNLESS FOLLOWED BY UF=MICROFARADS. INDUCTANCE VALUES IN MICROHENRYS UNLESS FOLLOWED BY MH=MILLIHENRYS OR H=HENRYS.

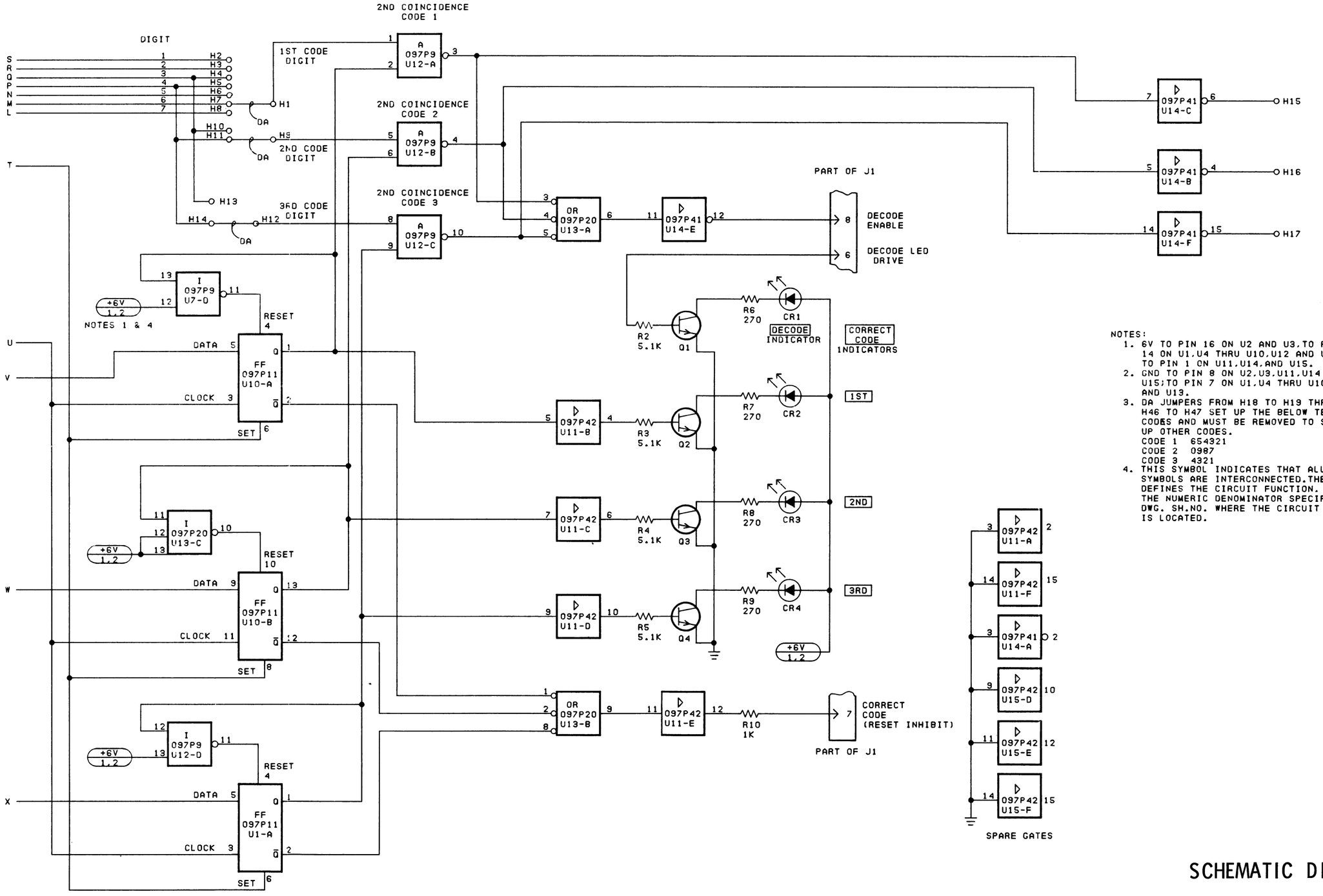
MODEL NO	REV LETTER
PL19D424305G1	



(19D424310, Sh. 1, Rev. 2)

SCHEMATIC DIAGRAM

COUNTER BOARD 19D424305G1



NOTES:
1. 6V TO PIN 16 ON U2 AND U3, TO PIN 14 ON U1, U4 THRU U10, U12 AND U13; TO PIN 1 ON U11, U14, AND U15.
2. GND TO PIN 8 ON U2, U3, U11, U14 AND U15; TO PIN 7 ON U1, U4 THRU U10, U12 AND U13.
3. DA JUMPERS FROM H18 TO H19 THRU H46 TO H47 SET UP THE BELOW TEST CODES AND MUST BE REMOVED TO SET UP OTHER CODES.
   CODE 1 654321
   CODE 2 0987
   CODE 3 4321
4. THIS SYMBOL INDICATES THAT ALL LIKE SYMBOLS ARE INTERCONNECTED. THE NUMERATOR DEFINES THE CIRCUIT FUNCTION. THE NUMERIC DENOMINATOR SPECIFIES THE DWG. SH.NO. WHERE THE CIRCUIT FUNCTION IS LOCATED.

(19D424310, Sh. 2, Rev. 1)

SCHEMATIC DIAGRAM

COUNTER BOARD 19D424305G1

PARTS LIST

LBI-30639

DIGITAL DECODER
19C327520G1 590 Hz
19C327520G2 1500 Hz
19C327520G3 2805 Hz

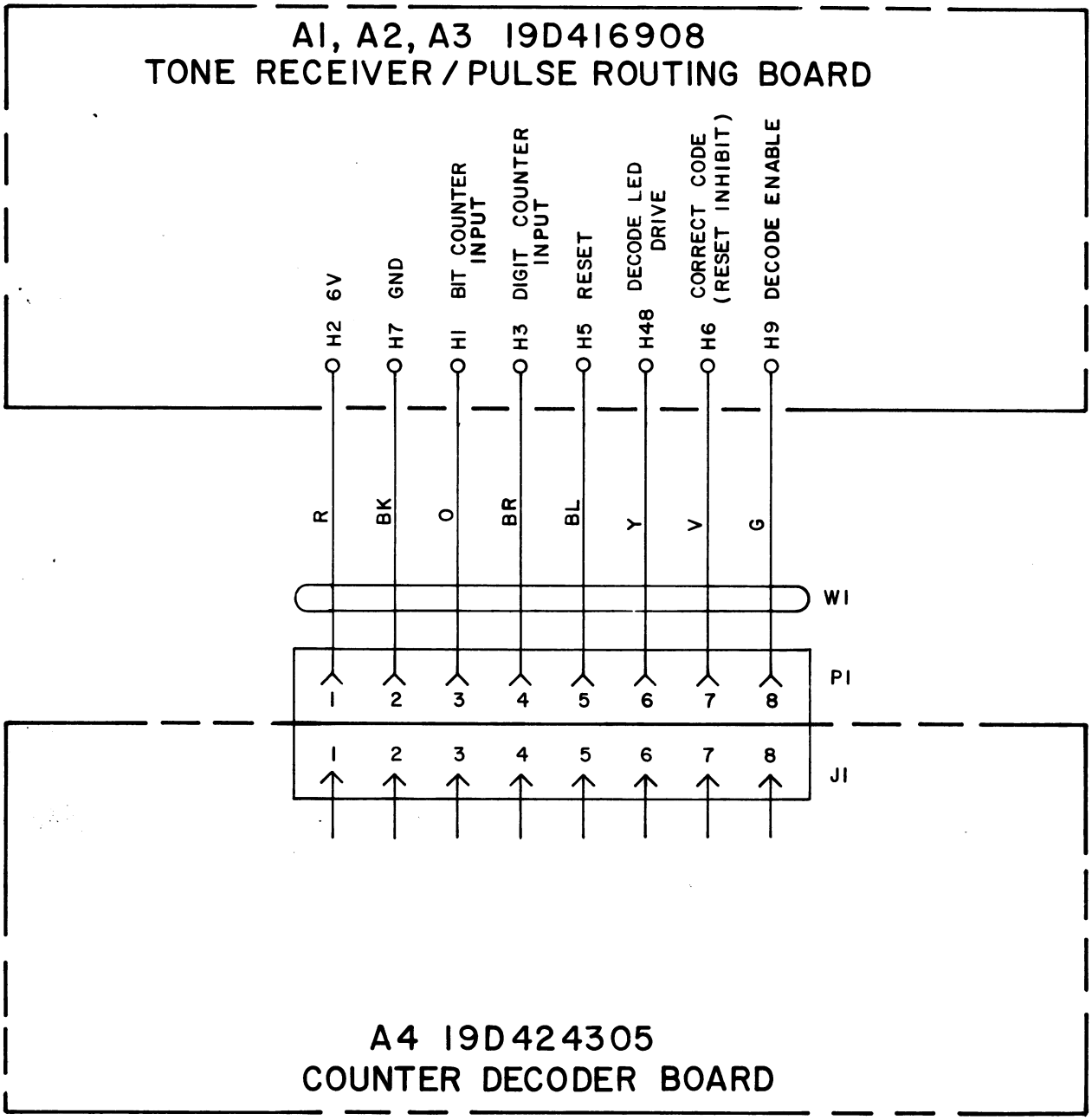
SYMBOL	GE PART NO.	DESCRIPTION
A1 thru A3		TONE RECEIVER BOARD A1 19D416908G4 590 Hz A2 19D416908G5 1500 Hz A3 19D416908G6 2805 Hz
		- - - - - - - - - - CAPACITORS - - - - - - - - - -
C1	5496267P15	Tantalum: 47 µf ±20%, 20 VDCW; sim to Sprague Type 150D.
C2	19B209243P14	Polyester: 0.33 µf ±20%, 250 VDCW.
C3	5494481P111	Ceramic disc: 1000 pf ±20%, 1000 VDCW; sim to RMC Type JF Discap.
C4	19B209243P14	Polyester: 0.33 µf ±20%, 250 VDCW.
C5	5496267P1	Tantalum: 6.8 µf ±20%, 6 VDCW; sim to Sprague Type 150D.
C6	5494481P111	Ceramic disc: 1000 pf ±20%, 1000 VDCW; sim to RMC Type JF Discap.
C7	5496267P1	Tantalum: 6.8 µf ±20%, 6 VDCW; sim to Sprague Type 150D.
C8	5496267P17	Tantalum: 1.0 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C9	19C300075P47001G	Polyester: 47,000 pf ±2%, 100 VDCW; sim to GE Type 61F.
C10	5496249P25000G	Polystyrene: 2500 pf ±2-1/2%, 125 VDCW.
C11	19C300075P22002G	Polyester: 220,000 pf ±2%, 100 VDCW; sim to GE Type 61F.
C12	5496249P16000G	Polystyrene: 1600 pf ±2-1/2%, 125 VDCW.
C13	5496249P20000G	Polystyrene: 2000 pf ±2-1/2%, 125 VDCW.
C14 thru C16	5494481P111	Ceramic disc: 1000 pf ±20%, 1000 VDCW; sim to RMC Type JF Discap.
C17 and C18	5496267P17	Tantalum: 1.0 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C19	5496267P13	Tantalum: 2.2 µf ±20%, 20 VDCW; sim to Sprague Type 150D.
C20	5496267P1	Tantalum: 6.8 µf ±20%, 6 VDCW; sim to Sprague Type 150D.
C21	5496267P10	Tantalum: 22 µf ±20%, 15 VDCW; sim to Sprague Type 150D.
C22	5496267P17	Tantalum: 1.0 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C23	5496267P1	Tantalum: 6.8 µf ±20%, 6 VDCW; sim to Sprague Type 150D.
C24	5496267P17	Tantalum: 1.0 µf ±20%, 35 VDCW; sim to Sprague Type 150D.
C25	5496267P13	Tantalum: 2.2 µf ±20%, 20 VDCW; sim to Sprague Type 150D.
		- - - - - - - DIODES AND RECTIFIERS - - - - - -
CR1	4037822P1	Silicon.
CR2 thru CR17	19A115250P1	Silicon.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - -
IC1	19A115913P7	Digital, Quad 2-Input Nand Gate; sim to DTL Series Type 946.
IC2	19A115913P3	Digital, Expandable Dual 4-Input Nand Buffer; sim to DTL Series Type 932.
IC3	19A115913P6	Digital, Clocked J-K/R-S Flip-Flop; sim to DTL Series Type 945.
		- - - - - - - - - - INDUCTORS - - - - - - - - -
L1	19B205354G2	Coil.
L2	19B205354G3	Coil.

SYMBOL	GE PART NO.	DESCRIPTION
		- - - - - - - - - - - PLUGS - - - - - - - - -
P1		(Part of W1). Includes:
	19A116659P20	Shell.
	19A116781P6	Contact, electrical: wire range No. 22-26 AWG; sim to Molex 08-50-0108. (Quantity 8).
P12		(Part of Printed Board 19D416898P1).
		- - - - - - - - - - TRANSISTORS - - - - - - - - -
Q1	19A116118P1	Silicon, NPN.
Q2	19A116774P1	Silicon, NPN; sim to Type 2N5210.
Q3	19A115889P1	Silicon, NPN.
Q4 and Q5	19A115768P1	Silicon, PNP; sim to Type 2N3702.
Q6	19A115889P1	Silicon, NPN.
Q7	19A116774P1	Silicon, NPN; sim to Type 2N5210.
Q8 and Q9	19A115889P1	Silicon, NPN.
Q10	19A115768P1	Silicon, PNP; sim to Type 2N3702.
Q11	19A115889P1	Silicon, NPN.
Q12	19A116774P1	Silicon, NPN; sim to Type 2N5210.
Q13	19A115889P1	Silicon, NPN.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1	3R152P561J	Composition: 560 ohms ±5%, 1/4 w.
R2 and R3	3R152P243J	Composition: 24K ohms ±5%, 1/4 w.
R4	3R152P123J	Composition: 12K ohms ±5%, 1/4 w.
R5 and R6	3R152P223J	Composition: 22K ohms ±5%, 1/4 w.
R7	3R152P513J	Composition: 51K ohms ±5%, 1/4 w.
R8	3R152P242J	Composition: 2.4K ohms ±5%, 1/4 w.
R9	3R152P102J	Composition: 1K ohms ±5%, 1/4 w.
R10	3R152P103J	Composition: 10K ohms ±5%, 1/4 w.
R11	3R152P473J	Composition: 47K ohms ±5%, 1/4 w.
R12	3R152P103J	Composition: 10K ohms ±5%, 1/4 w.
R13	3R152P513J	Composition: 51K ohms ±5%, 1/4 w.
R14	3R152P243J	Composition: 24K ohms ±5%, 1/4 w.
R15	3R152P103J	Composition: 10K ohms ±5%, 1/4 w.
R16	3R152P204J	Composition: 200K ohms ±5%, 1/4 w.
R17	3R152P221J	Composition: 220 ohms ±5%, 1/4 w.
R18 and R19	3R152P822J	Composition: 8.2K ohms ±5%, 1/4 w.
R20	3R152P753J	Composition: 75K ohms ±5%, 1/4 w.
R21	3R152P242J	Composition: 2.4K ohms ±5%, 1/4 w.
R22	3R152P622J	Composition: 6.2K ohms ±5%, 1/4 w.
R23	3R152P332J	Composition: 3.3K ohms ±5%, 1/4 w.
R24 and R25	3R152P104J	Composition: 100K ohms ±5%, 1/4 w.
R26	3R152P303J	Composition: 30K ohms ±5%, 1/4 w.
R27	3R152P333J	Composition: 33K ohms ±5%, 1/4 w.
R28	3R152P623J	Composition: 62K ohms ±5%, 1/4 w.
R29	3R152P103J	Composition: 10K ohms ±5%, 1/4 w.
R30	3R152P202J	Composition: 2K ohms ±5%, 1/4 w.
R31	3R152P240J	Composition: 24 ohms ±5%, 1/4 w.
R32	3R152P302J	Composition: 3K ohms ±5%, 1/4 w.
R33	3R152P202J	Composition: 2K ohms ±5%, 1/4 w.
R34 and R35	3R152P302J	Composition: 3K ohms ±5%, 1/4 w.

SYMBOL	GE PART NO.	DESCRIPTION
R36	3R152P512J	Composition: 5.2K ohms ±5%, 1/4 w.
R37	3R152P513J	Composition: 51K ohms ±5%, 1/4 w.
R38	3R152P202J	Composition: 2K ohms ±5%, 1/4 w.
R39	3R152P513J	Composition: 51K ohms ±5%, 1/4 w.
R40	3R152P511J	Composition: 510 ohms ±5%, 1/4 w.
R41	3R152P102J	Composition: 1K ohms ±5%, 1/4 w.
R42	3R152P513J	Composition: 51K ohms ±5%, 1/4 w.
R43	3R152P104J	Composition: 100K ohms ±5%, 1/4 w.
R44	3R152P512J	Composition: 5.1K ohms ±5%, 1/4 w.
R45	3R152P302J	Composition: 3K ohms ±5%, 1/4 w.
R46	3R152P622J	Composition: 6.2K ohms ±5%, 1/4 w.
		- - - - - - - - - - TEST POINTS - - - - - - - - -
TP1 thru TP5	19B211379P1	Spring (Test Point).
		- - - - - - - - VOLTAGE REGULATORS - - - - - - -
VR1	4036887P6	Silicon, Zener.
VR2	4036887P1	Silicon, Zener.
		- - - - - - - - - - CABLES - - - - - - - - - -
W1		CABLE ASSEMBLY 19D416908G7
		- - - - - - - - - - PLUGS - - - - - - - - - -
P1		Connector. Includes:
	19A116659P20	Shell.
	19A116781P6	Contact, electrical: sim to Molex 08-50-0108. (Quantity 8).
A4		COUNTER BOARD 19D424305G1
		- - - - - - - - - - CAPACITORS - - - - - - - - - -
C1	19A116080P107	Polyester: 0.1 µf ±10%, 50 VDCW.
C2	5494481P111	Ceramic disc: 1000 pf ±20%, 1000 VDCW; sim to RMC Type JF Discap.
C3	19A116080P107	Polyester: 0.1 µf ±10%, 50 VDCW.
C4	5494481P111	Ceramic disc: 1000 pf ±20%, 1000 VDCW; sim to RMC Type JF Discap.
C5	19A134202P15	Tantalum: 6.8 µf ±20%, 35 VDCW.
C6	19A116080P107	Polyester: 0.1 µf ±10%, 50 VDCW.
		- - - - - - - - DIODES AND RECTIFIERS - - - - -
CR1	19A134146P5	Diode, optoelectronic: green; sim to Opcoa LSM-16L.
CR2 thru CR4	19A134407P2	Diode, optoelectronic: yellow; sim to Mansanto MV5353.
		- - - - - - - - JACKS AND RECEPACLES - - - - - -
J1	19A116659P30	Connector, printed wiring: 8 contacts; sim to Molex 09-2373-8A.
		- - - - - - - - - - TRANSISTORS - - - - - - - - -
Q1 thru Q4	19A115910P1	Silicon, NPN; sim to Type 2N3904.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1	3R152P104J	Composition: 100K ohms ±5%, 1/4 w.
R2 thru R5	3R152P512J	Composition: 5.1K ohms ±5%, 1/4 w.
R6 thru R9	3R152P271K	Composition: 270 ohms ±10%, 1/4 w.

SYMBOL	GE PART NO.	DESCRIPTION
R10	3R152P102J	Composition: 1K ohms ±5%, 1/4 w.
R11 and R12	3R152P560K	Composition: 56 ohms ±10%, 1/4 w.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - - -
U1	19A134097P11	CMOS, Digital: Dual "D" Flip-Flop With Set/Reset.
U2 and U3	19A134097P15	CMOS, Digital: Decade Counter Divider.
U4 thru U7	19A134097P9	CMOS, Digital: Quad 2- Input Nand Gate.
U8	19A134097P54	CMOS, Digital: 8 Input Nand Gate.
U9	19A134097P10	CMOS, Digital: Dual 4- Input Nand Gate.
U10	19A134097P11	CMOS, Digital: Dual "D" Flip-Flop With Set/Reset.
U11	19A134097P42	CMOS, Digital: Hex Buffer/Converter (Non-Inverting).
U12	19A134097P9	CMOS, Digital: Quad 2-Input Nand Gate.
U13	19A134097P20	CMOS, Digital: Triple 3-Input Nand Gate.
U14	19A134097P41	CMOS, Digital: Hex Buffer/Converter (Inverting).
U15	19A134097P42	CMOS, Digital: Hex Buffer/Converter (Non-Inverting).
		- - - - - - - - - MISCELLANEOUS - - - - - - - - -
	19B219690G1	Handle assembly.
	5491541P308	Spacer, threaded. (Located between Tone Receiver and Counter Board).
	19A116022P1	Insulator, bushing. (Used with Q1).
	19A116023P3	Insulator, plate. (Used with Q1).

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES.



IN ORDER TO RETAIN RATED EQUIPMENT PERFORMANCE, REPLACEMENT OF ANY SERVICE PART SHOULD BE MADE ONLY WITH A COMPONENT HAVING THE SPECIFICATIONS SHOWN ON THE PARTS LIST FOR THAT PART.

NOTES:

1. ALL WIRES ARE SF24.

(19C327464, Rev. 1)

INTERCONNECTION DIAGRAM

DIGITAL DECODER 19C327520G1-G3

ORDERING SERVICE PARTS

Each component appearing on the schematic diagram is identified by a symbol number to simplify locating it in the parts list. Each component is listed by symbol number, followed by its description and GE Part Number.

Service parts may be obtained from Authorized GE Communication Equipment Service Stations or through any GE Radio Communication Equipment Sales Office. When ordering a part, be sure to give:

1. GE Part Number for component
2. Description of part
3. Model number of equipment
4. Revision letter stamped on unit

These instructions do not purport to cover all details or variations in equipment nor to provide for every possible contingency to be met in connection with installation, operation or maintenance.

Should further information be desired, or should particular problems arise which are not covered sufficiently for the purchaser's purposes, contact the nearest Radio Communication Equipment Sales Office of the General Electric Company.

MOBILE RADIO DEPARTMENT
GENERAL ELECTRIC COMPANY • LYNCHBURG, VIRGINIA 24502

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