INSTRUCTION MANUAL

SPEEDCALL MODEL 4503 DTMF

MULTI-ADDRESS STATION DECODER

(GENERAL ELECTRIC PART NO. 19B209685P1)
OPTION 9627, 9629, 9643, 9645 and 9659

January 1978

CAUTION

When Decoder PC boards are exposed, handle with special care to prevent damage to CMOS Integrated Circuits through discharge of static electricity with or without power applied. This condition ususally exists in dry atmosphere and especially around nylon or wool carpets and clothing.

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Model 4503 DTMF Decoder

SPECIFICATIONS

ELECTRICAL

INPUT

Format:	Standard 2-of-7 Touch-Tone®
Receive Audio	
Signal Level:	20mV to 10Vrms (2 tones measured with an average-reading rms-calibrated meter)
Noise Threshold:	12.0dB SINAD will provide 95% or greater probability of decoding a correct address
CTCSS Rejection:	20dB @ 100 Hz; 10dB @ 260 Hz
Impedance:	30K Ohms nominal, DC blocked
Frequency Acceptance:	±1.5% of nominal tone frequency
Tone Level Differential (Twist):	12dB if lesser tone is over 35mVrms
Data Rate:	0.4 to 12 digits per second with 68 ms tone duration minimum
Interdigit Interval:	2.5 seconds nominal
Code Capacity:	INDIVIDUAL CALL up to 7 digits ALL CALL one digit repeated up to 4 times GROUP CALL up to 4 digits

OUTPUT

Voltage:	Equal to or less than the supply voltage
Current:	500mA maximum

POWER REQUIREMENTS

Voltage:	13.8VDC ±20% (10.9 to 16.3VDC)
Current	
Operate:	120mA @ 13.8VDC
Standby:	45mA @ 13.8VDC

ENVIRONMENTAL

Temperature	
Operating:	-30°C to +85°C
Storage:	-65°C to +105°C
Humidity:	0 to 95%, non-condensing

® TOUCH-TONE IS A REGISTERED TRADEMARK OF AT&T CO

MODEL 4503 DTMF MULTI-ADDRESS STATION DECODER

DESCRIPTION

SPEEDCALL Model 4503 is a dual-tone multi-frequency (DTMF) Decoder designed for base station applications in Emergency and Administrative Communication (EACOM) systems. The Decoder is designed physically and electrically for installation in the decoder auxiliary slot(s) of the GENERAL ELECTRIC MASTR II Base Station tone control shelf. The 4503 Decoder uses standard Touch-Tone format, and is compatible with two-way radio and wireline systems.

Typical uses of the 4503 DTMF Decoder are to provide multi-level selective calling in EACOM and other signaling systems using Touch-Tone format; for repeater control; and to control remote ON/OFF functions.

The 4503 Decoder is capable of decoding three distinct code levels. These levels are for INDIVIDUAL CALLS, GROUP CALLS, and ALL CALLS. The three codes are field-programmable and may be used independently or in conjunction with each other.

The decode output will activate upon receipt of a correct code, and remain active until a reset is applied by placing ground potential at pin C1 on the PC board mating edge connector. The decode output will normally be used for Channel Guard disable or receiver mute control. The output may also be used in special applications for ON/OFF control of remote functions.

There are three Light Emitting Diodes (LED's) on the front panel. One LED indicates when an individual call is being decoded. The second LED indicates when either a group or all call is being decoded. These two LED's will illuminate during the decoding process and extinguish upon termination of the interdigit timer cycle (approximately 2.5 seconds after the last correct digit of the respective call has been received and decoded). The third LED indicates that an incoming call has been correctly received and decoded, and that the decode output has been activated. This LED will remain illuminated until the decode output is reset.

A Timer Control circuit is included for repeater control. This circuit is a decode output enable which will reset the 4503 Decoder after the repeater circuit has timed out.

An optional DPDT (2-Form C) relay output is available. This circuit is controlled by the decode output, and is physically connected to the PC board contacts.

INSTALLATION

The 4503 Decoder is constructed with two printed circuit (PC) boards and a front panel. PC board #1 contains the major electrical components, programming pin fields, and the mating edge contact fingers. PC board #2 contains the LED indicators and optional circuitry. The two PC boards are interfaced with jumper cables as detailed in Figure 10 of this manual.

Prior to installing and using the 4503 Decoder, perform the modifications on the G.E. MASTR II Backplane Assembly PL19D417214 (solder side) as detailed in Figure 1 below. Ensure that all code programming, strapping, and system adjustments are completed as outlined in the following sections of this manual before installing and operating the 4503 Decoder.

When used in LOCAL EACOM applications, the 4503 Decoder will occupy the 2nd from left slot in the tone control shelf, with edge contact fingers mating with J1212 on the backplane board. A wire jumper must be soldered between H18 and H19 on the backplane board for this application.

When used in REGIONAL EACOM applications, Decoder #1 will occupy the 2nd from left slot in the tone control shelf with edge contact fingers mating with J1212. Decoder #2 will occupy the outer left slot in the tone control shelf with edge contact fingers mating with J1213 on the backplane board. A trace must be cut on the backplane board as shown in Figure 1, and wire jumpers soldered between those points on the backplane board as listed under (2) in Figure 1.

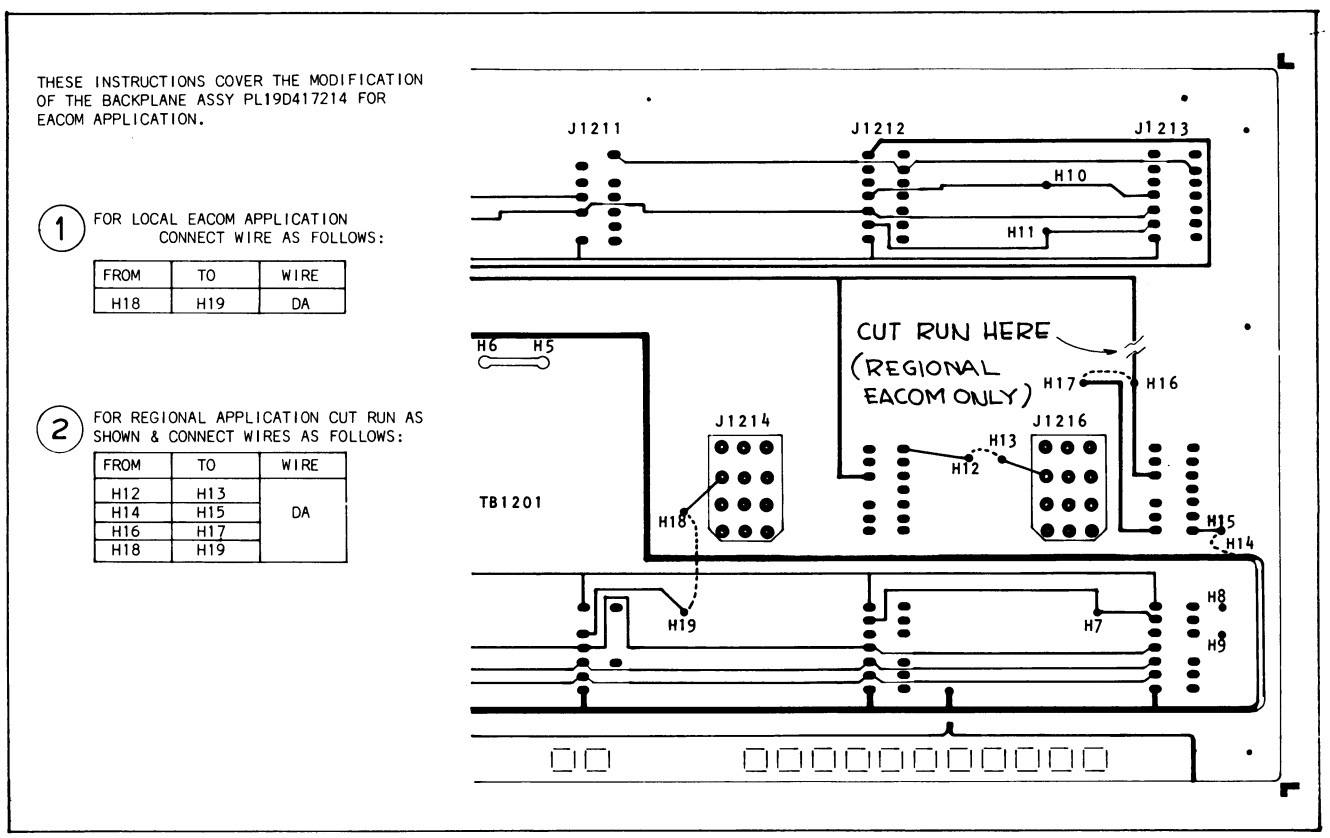


Figure 1 - Backplane Modifications for Use With the Model 4503 DTMF Decoder

PROGRAMMING INSTRUCTIONS

INTRODUCTION

Each 4503 Decoder must be programmed for the decoding level(s) to be used. This will permit the Decoder to respond only to programmed codes and to reject all other signals. Programming is accomplished by connecting jumper wires between appropriate pins within the respective code programming pin field, as illustrated in Figures 2 through 6. The programming pin fields are located on the component side of PC board #1. The three code levels contain different digits in the respective sequences. The INDIVIDUAL CALL code may contain 1 to 7 digits and is independent of the GROUP and ALL CALL codes in content and length. The GROUP and ALL CALL codes will ALWAYS be the same in length.

IMPORTANT NOTE: The digits to be used in all three codes should be determined before programming commences. This is necessary because the first digit used in the INDIVIDUAL CALL code MUST NOT be used in the ALL CALL code, or as the first digit of the GROUP CALL code. The ALL CALL code digit and the first digit of the GROUP CALL code will ALWAYS be the same.

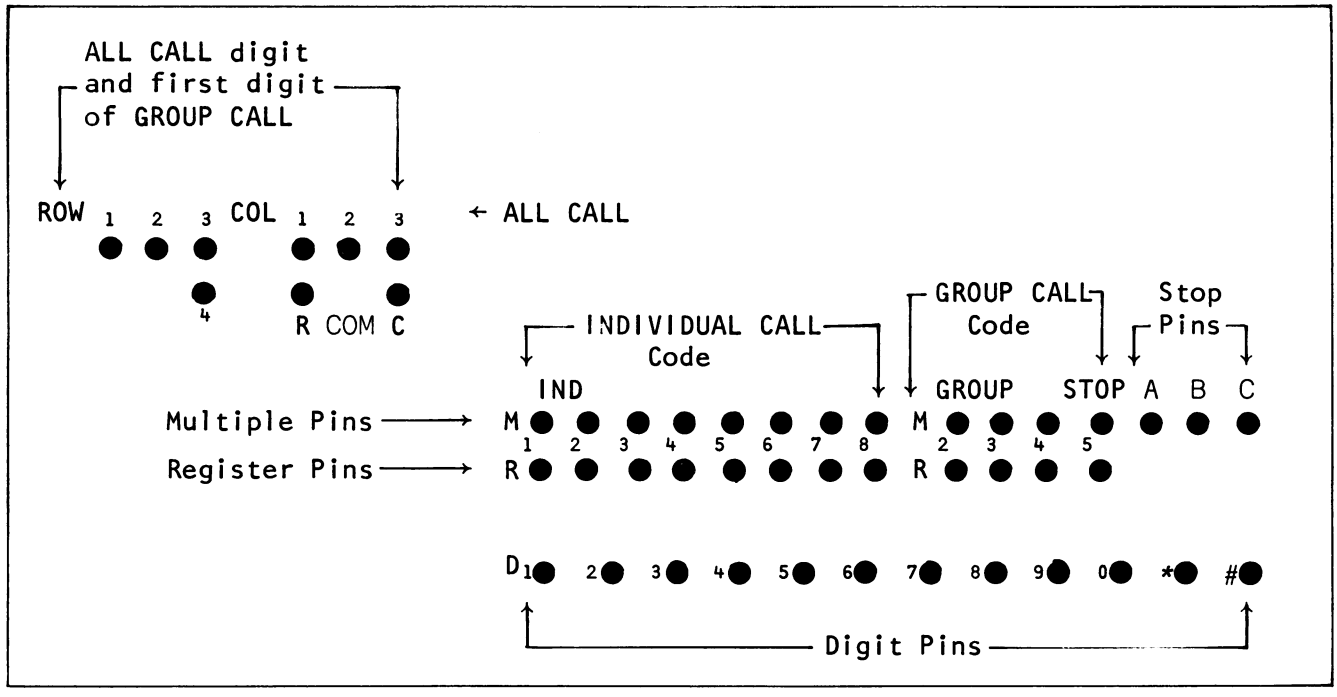


Figure 2 - Model 4503 Decoder Programming Pin Field for All Codes

The **"IND"** register pins (R1 - R8) represent the position of the digits in the INDIVIDUAL CALL sequence. The **"GROUP"** register pins (R2 - R5) represent the position of the digits in the GROUP CALL sequence. A multiple pin (M1 - M8 and M2 - M5) is connected by PC trace to the adjacent register pin to permit duplication of digits anywhere in the INDIVIDUAL and GROUP CALL codes.

The digit pins (D1 - D#) correspond to the numerical value of each digit in the INDIVIDUAL and GROUP CALL codes. The digit used for the ALL CALL code and for the first digit of the GROUP CALL code is programmed on the **"ALL CALL"** pin field. The **STOP** pins (A, B and C) permit the Decoder to recognize the last digit of a sequence. "A" is the stop pin for the INDIVIDUAL CALL code; "B" is the stop pin for the GROUP and ALL CALL codes; and "C" is the stop pin for the OFF command when the Decoder is used in remote control applications.

PROGRAMMING THE INDIVIDUAL CALL CODE

Figure 3 provides an example for programming the INDIVIDUAL CALL sequence of 1599. Only the applicable pins are shaded to illustrate the pin field used. It is recommended that the EIA Color Code be followed when programming the register pins. This will reduce the probability of errors and make it easier to check the code at a later time.

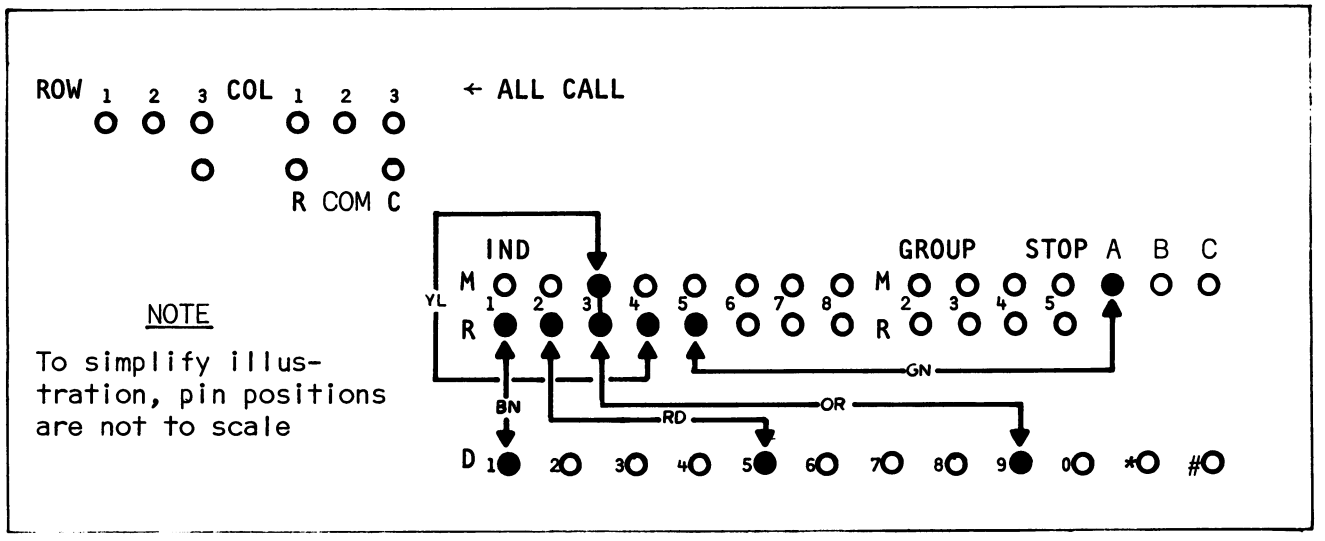


Figure 3 - Programming Example for the Individual Call Code (1599)

To program the sequence 1599 as the INDIVIDUAL CALL code, proceed as follows:

- Connect a brown jumper from R1 to D1
- Connect a red jumper from R2 to D5
- Connect an orange jumper from R3 to D9
- Connect a yellow jumper from R4 to M3. M3 is connected by PC trace to R3 which, in turn, is connected by the orange jumper to D9. This duplicates the number 9 at R3 and R4
- Connect a green jumper from R5 to STOP pin A. This jumper will always be from the next available register pin following the last digit of the

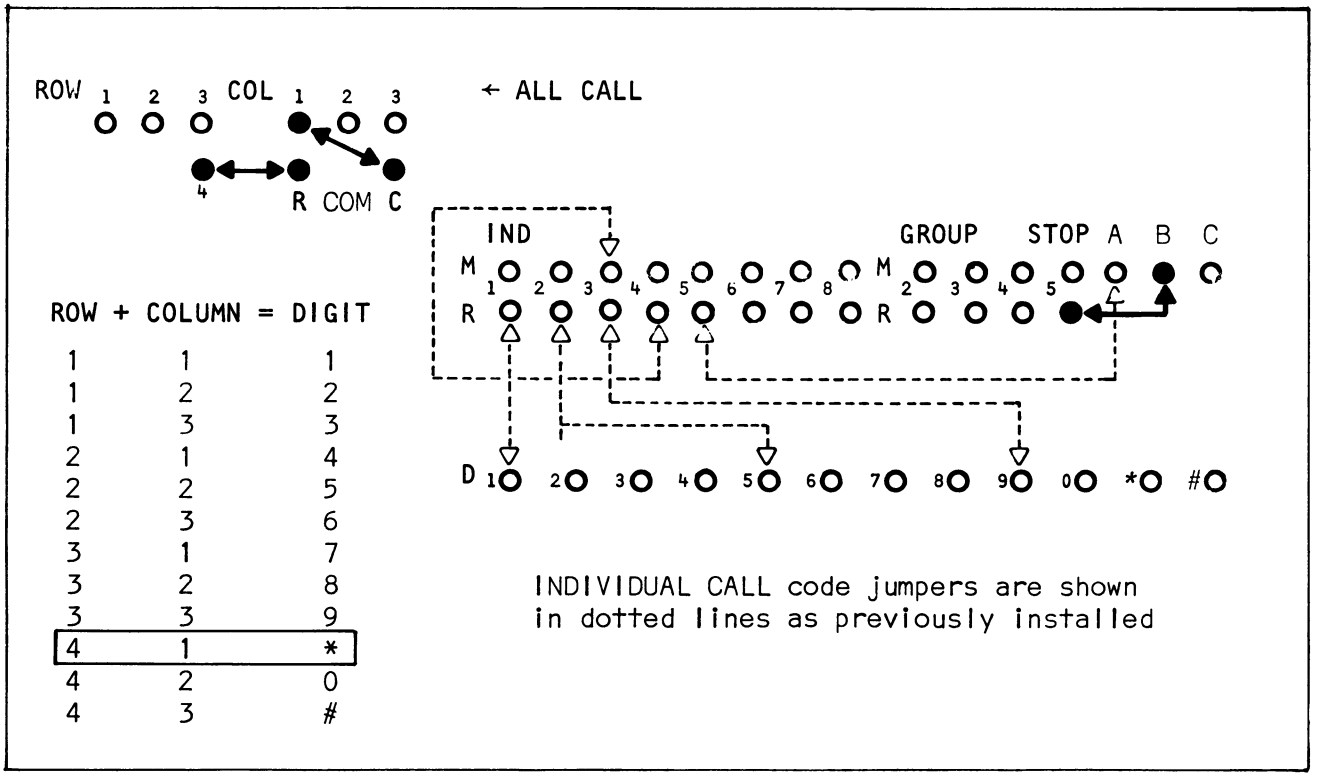
INDIVIDUAL CALL code to the STOP pin marked "A". This permits the Decoder to recognize the last digit of the sequence and to energize the decode output.

If ALL and GROUP CALL codes are not to be used, it will be necessary to disable the row and column detectors. This is done by removing the jumpers from the ROW (R) and COLUMN (C) common pins in the ALL CALL pin field, and reconnecting one of the jumpers between the ROW 1 and ROW 4 pins, and the other jumper between the COL 1 and COL 3 pins in the ALL CALL pin field. If either the ALL CALL or the GROUP CALL codes, or both, is to be used, continue the programming instructions in the following paragraphs.

PROGRAMMING THE ALL CALL CODE

Refer to Figure 4 for an example of how to program the ALL CALL code. This code will consist of a single digit repeated 1 to 4 times as determined by the STOP jumper position. The digit to be used is selected by connecting the row and column pins within the ALL CALL pin field. These connections correspond to the Touch-Tone keypad and frequency format (refer to "Circuit Analysis" in this manual). A cross-reference between row and column pins is given in Figure 4 to identify the digit selected for the ALL CALL code.

The example in Figure 4 shows the connections necessary to program the sequence **** for the ALL CALL code. Only the applicable pins are shaded in this example with the jumpers from the INDIVIDUAL CODE shown in dotted lines. The Touch-Tone asterisk (*) and hatch sign (#) are normally not used in the INDIVIDUAL CALL code, and are recommended as the ALL CALL code digit as this digit MUST NOT be the same as the first digit of the INDIVIDUAL CALL code.



ROW + COLUMN = DIGIT

1	1	1
1	2	2
1	3	3
2	1	4
2	2	5
2	3	6
3	1	7
3	2	8
3	3	9
4	1	*
4	2	0
4	3	#

Figure 4 - Programming example of the ALL CALL Code ****

The jumpers used to program the ALL CALL and GROUP CALL codes are two colors; primary white plus the EIA Code secondary color corresponding to the register pin number. As both row and column jumpers form the ALL CALL code digit, both jumpers will be white-brown. To program the ALL CALL code sequence of ****, proceed as follows:

- Connect a white-brown jumper from the common ROW pin (R) to Row pin 4
- Connect a white-brown jumper from the common COLUMN pin (C) to Column pin 1. The asterisk has now been programmed as the ALL CALL code digit. No other digits are to be programmed for this code. Only the number of times the digit is to repeat, or sequence length, will now be programmed
- Connect a white-green jumper from R5 in the GROUP pin field to the STOP pin marked "B". If the ALL CALL code digit is to be repeated N times, the jumper to the B-STOP pin will be from the GROUP register pin N+1. Thus, if the ALL CALL code digit is to repeat 4 times, the jumper will be on N+1, or R5. If the digit is to repeat 3 times, the jumper would be from R4 to B-STOP pin

If the GROUP CALL code is not to be used with the Decoder, it will be necessary to program the unused GROUP register pins with the ALL CALL code digit. If this is not done, the Decoder will not respond properly to the ALL CALL code under noise conditions as will be experienced on radio channels. The noise will appear as a steady digit and prevent clocking beyond the first digit of the code.

Refer to Figure 5 for an example of how to program the GROUP register pins when the GROUP CALL code is not used with the decoder. Only the applicable pins are shaded in this illustration. The INDIVIDUAL and ALL CALL programming leads are in dotted lines, as previously installed.

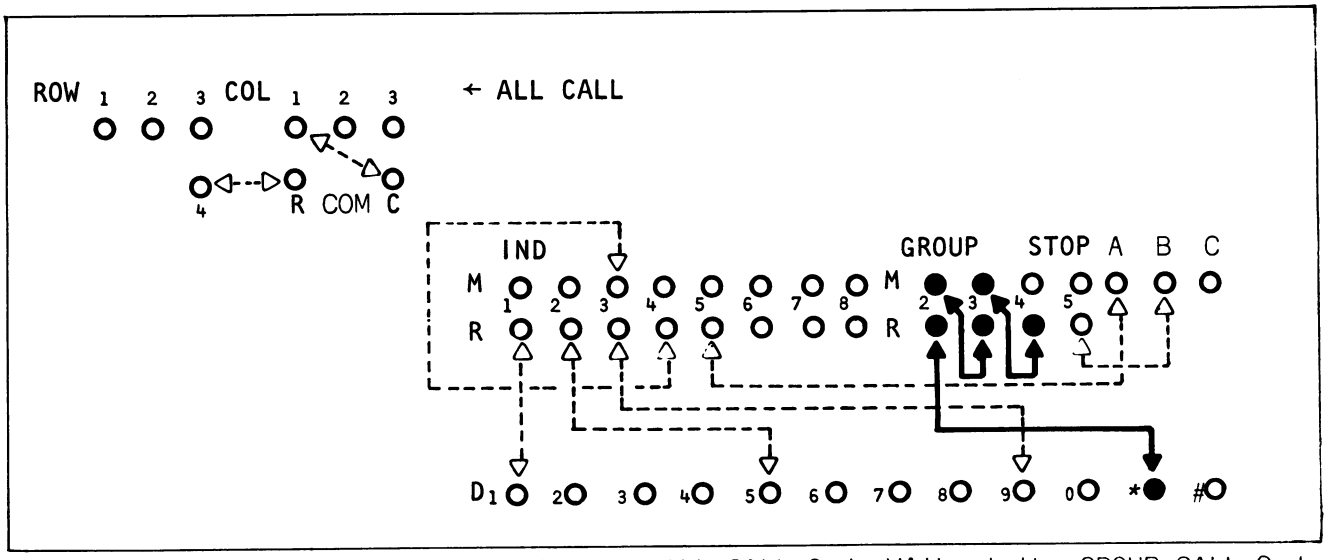


Figure 5 - Programming Example Using the ALL CALL Code Without the GROUP CALL Code

- With the ALL CALL Code programmed as previously described, connect a jumper from R2 in the GROUP pin field to D* in the Digit pin field

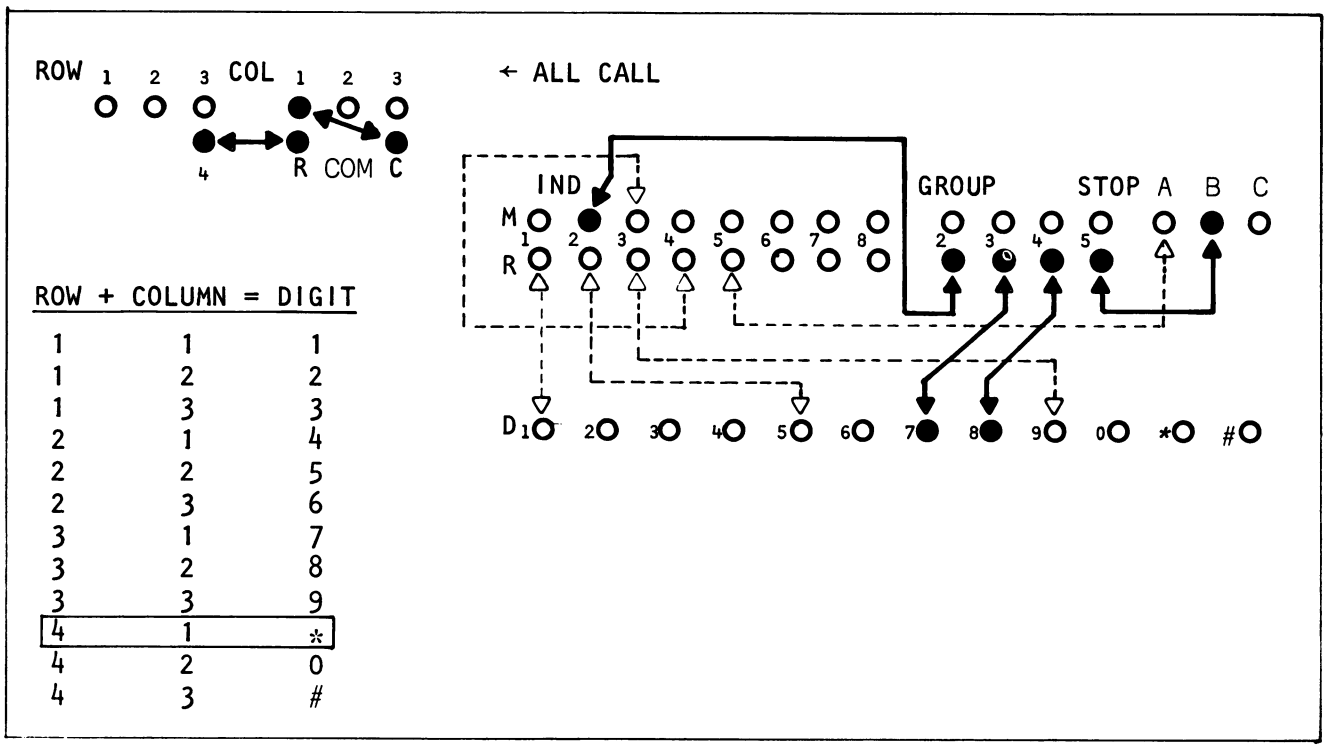
- Connect a jumper from R3 to M2 to duplicate the * digit at R3
- Connect a jumper from R4 to M3 to duplicate the * digit at R4. In this manner, R2, R3 and R4 are all connected in series with the D* pin

If the GROUP CALL code is to be used, omit the instructions immediately above and continue the programming actions in the following paragraphs.

PROGRAMMING THE GROUP CALL CODE

Refer to Figure 6 for an example of how to program the GROUP CALL code. This code will always commence with the same digit as programmed for the ALL CALL code, and will be equal in length to the ALL CALL code. The remaining digits after the first digit up to the STOP function will be programmed at the discretion of the user. All digits after the first digit are programmed by making the proper connections between the register pins in the GROUP pin field and the appropriate digit pins in the same manner as the INDIVIDUAL CALL code.

The example in Figure 6 shows the connections necessary to program the sequence *578 for the GROUP CALL code. Only applicable pins are shaded with the INDIVIDUAL and ALL CALL codes, previously installed, shown in dotted lines.



ROW + COLUMN = DIGIT

1	1	1
1	2	2
1	3	3
2	1	4
2	2	5
2	3	6
3	1	7
3	2	8
3	3	9
4	1	*
4	2	0
4	3	#

Figure 6 - Programming Example of the GROUP CALL Code (*578)

To program the sequence *578 as the GROUP CALL code, proceed as follows:

- Program the 1st digit (*) in the same manner as described for the ALL CALL code. This will include the jumper from R5 to the B-STOP pin

- Program the 2nd Digit (5) by connecting a white-red jumper from R2 to M2 in the IND pin field. This is necessary in order to duplicate the digit 5 which was used in the INDIVIDUAL CALL code. The D5 pin is already occupied by the red jumper from R2 in the IND pin field. The connection at M2 forms a series path to R2 by PC trace, and then to D5 by the red jumper

- Connect a white-orange jumper from R3 to D7 to program the digit 7

- Connect a white-yellow jumper from R4 to D8 to program the digit 8

- Ensure the white-green jumper is in place between R5 and the B-STOP pin

This completes all programming requirements for the INDIVIDUAL, GROUP, and ALL CALL codes. A change in the programming already accomplished will be required if the Decoder is to be used in a remote ON/OFF control application. The change in programming is described in the next section under "STRAPPING".

ADJUSTMENTS AND STRAPPING

ADJUSTMENTS

The 4503 Decoder does not require pre-operation adjustments. However, when used in FM or PM radio systems, the receiver must be properly netted. If it is not, the resulting distortion may cause erratic operation of the Decoder.

Touch-Tone encoders used to address the 4503 Decoders in a radio system should be adjusted for a signal output level with a maximum peak deviation of no more than 2/3 of full system deviation. If this level is exceeded, the distortion caused by clipping in the audio limiter stages of the transmitter may result in erratic operation of the Decoders. Refer to the adjustments procedures for the particular Touch-Tone encoder to be used.

STRAPPING

The 4503 Decoder must be strapped for the intended mode of operation. Strapping is accomplished by soldering jumper wires between designated pads on the PC boards. The modes of operation are:

- Local EACOM base station control

- Regional EACOM base station control (two decoders are required for this mode of operation)

- Repeater control (special application)

- ON/OFF control of remote functions (special application)

Strapping will affect two general areas of the Decoder:

- Local reset function
- Decode output

Local EACOM Operation:

Refer to Figure 7. In this mode of operation, the Decoder will have local reset and the decode output will disable Channel Guard. On PC Board #1,

- Connect a wire jumper between pads E1 and E2 to provide local reset at pin C1 on the edge contact fingers
- Connect a wire jumper between pads E4 and E5
- Connect a wire jumper between pads E7 and E8 to provide decode output at pin A7 on the edge contact fingers for Channel Guard disable

Regional EACOM Operation:

Refer to Figure 7. In this mode of operation, two decoders are used to perform Channel Guard disable (Decoder No. 1) and receiver mute (Decoder No. 2). On PC Board #1,

- Connect Decoder No. 1 for local EACOM operation as described above

Decoder No. 2:

- Connect a wire jumper between pads E1 and E2 for local reset at pin C1
- Connect a wire jumper between pads E4 and E5
- Connect a wire jumper between pads E7 and E9 to provide decode output at pin A8 on the edge contact fingers for receiver mute

Repeater Control:

Refer to Figure 7. This mode of operation is intended for special applications. The Decode output is at pin A8 on the edge contact fingers. To operate in this mode, perform the following modifications to PC Board #1:

- Connect a wire jumper between pads E2 and E3 to provide reset by the Timer Control circuit at pin A1 on the edge contact fingers
- Connect a wire jumper between pads E5 and E6
- Connect a wire jumper between pads E7 and E9 for output at A8

Remote ON/OFF Control Operation:

Refer to Figure 7. If the Decoder is to be used in this mode of operation, the ALL CALL or GROUP CALL codes may be used to reset the decode output rather than to activate it as in the normal mode of operation previously described. The INDIVIDUAL CALL code will be used as the ON command, and will not be changed.

To utilize the ALL CALL and/or GROUP CALL codes as the OFF (reset) command, remove the programming jumper from the B-STOP pin and place it on the C-STOP pin. If either of the two codes is used as an OFF command, the other code will automatically perform the same function as the STOP pin is common to both codes.

In addition to changing the STOP jumper from the B to the C pin, the following strapping is also required:

- Connect a jumper wire between pads E4 and E5 on PC Board #1
- Connect a jumper wire between pads E7 and E9 for decode output at pin A8 on the edge contact fingers on PC Board #1
- Connect a 10K, $\frac{1}{4}$ watt resistor between pads E10 and E11 on PC Board #2

Remote Control With Local Reset (Special Application):

When using Remote ON/OFF Control and requiring local reset capabilities, perform the strapping described above. Also connect a jumper between pads E1 and E2 with a normal-open switch to A- if optional reset at C1 is desired; or between E2 and E3 with a normal-closed switch to A+ if reset at A1 is desired. Instead of the resistor between pads E10 and E11 on PC Board #2, install a diode, similar to a 1N914, as shown in Figure 7.

	Strapping Between Pads										
	PC Board No.1									PC No.2	
MODE OF OPERATION	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11
Local EACOM	●	●	○	●	●	○	●	●	○	○	○
Regional EACOM:											
Decoder #1	●	●	○	●	●	○	●	●	○	○	○
Decoder #2	●	●	○	●	●	○	○	●	●	○	○
Repeater Control	○	●	●	○	●	●	○	●	●	○	○
Remote ON/OFF Control	○	○	○	●	●	○	○	●	●	●	●
Remote ON/OFF Control with Local Reset	○	○	○	●	●	○	○	●	●	●	●

Figure 7 - Operating Mode Strapping Requirements

CIRCUIT ANALYSIS

TOUCH-TONE FORMAT

The 4503 Decoder uses standard Touch-Tone format, originally developed by AT&T Co. for telephone dialing. Each digit is identified by a unique combination of two tones; one corresponding to the horizontal row, and the other to the vertical column of encoder pushbutton positions as illustrated in Figure 8. The frequencies are grouped about the geometric center of the 300 to 3000 Hz voice band used in telephone and radio systems. The two tones are generated simultaneously and remain on as long as a digit is being sent. Row tones are all in a lower frequency group than the column tones. The frequencies are non-harmonic to give high immunity to false identification from beat frequencies and distortion-produced overtones.

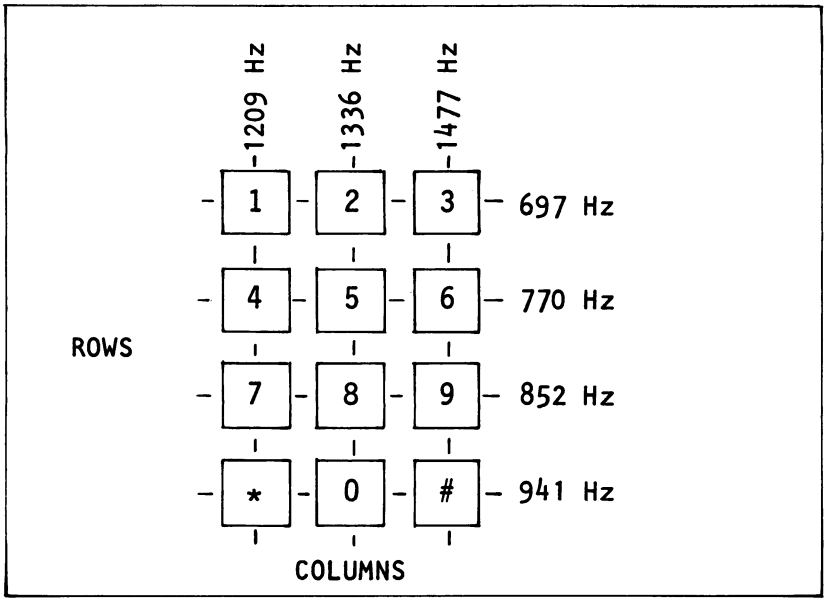


Figure 8 - Touch-Tone Keypad and Frequency Format

GENERAL CIRCUIT DESCRIPTION

Refer to the 4503 Block Diagram on page 14, and the Decoder Circuit Schematic on pages 20 and 21.

Initially, the Decoder is in the standby condition with the first stage of the shift counter applying a voltage to the coding matrix via the program field to set the programmable dectectors for the row and column frequencies of the first digit of the individual call address.

An incoming Touch-Tone pair will be applied through the row and column filters (L1/L2) to the row and column limiters (A1A/A1B). AFter limiting, the row and column tones are applied to the inputs of the tone detectors.

If the first digit of the INDIVIDUAL CALL is received, the row and column detectors will detect correct tones simultaneously. Outputs from the detectors will cause the AND gate to trigger the clock generator and reset the interdigit timer. The clock generator output will cause the shift counter to advance one position, and apply a voltage to the coding matrix to set the detectors for the row and column frequencies of the second digit of the INDIVIDUAL CALL address. Similarly, as each successive correct digit of the programmed address is received, the shift counter advances one position and sets the detectors for the next address digit.

If the ALL CALL digit is received, the A6B/A6C flip-flop sets so that the programmable detectors will detect GROUP or ALL CALL digits.

When the Decoder is in the standby condition, the A4 Interdigit Timer is timed out so that pin 3 is high. This applies a reset to A7 so that it is at its zero count (Q1 through Q7 are all low); resets the A6B/A6C flip-flop so that pin 4 is low and pin 3 is high; and forces the outputs of A10A and A10B low so that neither DS2 or DS3 are illuminated. The low level at pin 4 of A6 enables A8 and the high level at pin 3 disables A9. With A7 at its zero count, the positive voltage at pin 3 of A8 is connected to pin 13 and through CR33 and the INDIVIDUAL CALL R-1 programming lead to set the programmable tanks for the first digit of the INDIVIDUAL CALL.

A2 is the Schmitt Trigger for the "programmable" channel (i.e., the detectors and tank circuits that are programmed via the register pin fields). A3 is the Schmitt Trigger for the channel programmed for the ALL CALL code digit.

A8 and A9 are analog multiplexers. They are equivalent to an eight-throw single-pole switch. The common at pin 3 is connected to one, and only one, of the "0" through "7" lines according to the binary numer present at inputs A, B and C. A high level at pin 6 (inhibit) opens all circuits regardless of this binary number.

DETAILED THEORY OF OPERATION

Individual Call:

If the first digit of the INDIVIDUAL CALL code is received, pins 3 & 7 of A2 will go low. Pin 7, going low, turns on Q26 to charge C36 and pin 3 of A4 goes low, removing the reset from A7 and enabling A10A and A10B. Pin 4 of A10 goes high, causing Q29 to conduct and illuminate DS2. Pin 3 of A2, going low, causes pin 10 of A5 to go high. At the termination of the first digit, when pin 10 of A5 goes back low, A7 will advance one count and pin 3 of A8 will then be connected to pin 14 to program the tank circuits for the second digit of the call.

As each digit is received, A7 will advance one count, causing a positive voltage to be applied to the succeeding register lead. After the last digit of the sequence is received, the register lead connected to the A-STOP pin will be energized, causing pin 10 of A6 to go low and set the A5C/A5D flip-flop (E4 connected to E5) so that pin 3 of A5 goes high and Q27 and Q28 conduct. Q27 and Q28 will continue to conduct until A- is applied to the reset input at pin C1 (E1 connected to E2).

Group and All Calls:

If the first digit of the GROUP and ALL CALL codes is received while the 4503 is in a standby state, pins 3 & 7 of A3 will go low. Pin 7, going low, turns on Q26 to charge C36 and pin 3 of A4 goes low, removing the reset from A7, and enables A10A and A10B. Pin 3 of A10 goes high, causing Q30 to conduct and illuminate DS3. Pin 13 of A8 is high at this time and inverted by A5B so that pin 13 of A6 is low. When pin 3 of A3 goes low, pin 11 of A6 goes high to set the A6B/A6C flip-flop. This inhibits A8 and enables A9. At the termination of this first digit, A7 will advance one count and the GROUP CALL R-2 lead will go positive to set the programmable tanks for the second digit of the Group Call sequence.

As each ALL CALL digit, or the appropriate digit in the GROUP CALL sequence, is received, A7 will advance one count until the GROUP pin field register lead connected to the B-STOP pin goes high. Pin 10 of A6 then goes low to energize the output.

If the first digit of the INDIVIDUAL CALL code has been received, pin 13 of A8 will be low and A5B will invert this to provide a high level at pin 13 of A6 so that subsequent receipt of the first digit of the GROUP and ALL CALL codes cannot set the A6B/A6C flip-flop. Thus, if the unit has received any portion of the INDIVIDUAL CALL code, it cannot change over to the GROUP or ALL CALL code sequences.

Timing:

As explained above, receipt of the ALL CALL digit or the first digit of the INDIVIDUAL CALL, causes C36 to charge through Q26 so that pin 3 of A4 goes low. At the termination ot this digit, C36 begins to discharge through R52 and, if the next digit in the sequence is not received within approximately 2.5 seconds, C36 will discharge below the trigger point of A4 and pin 3 will go back high, resetting A7 to the zero count, and resetting the A6B/A6C flip-flop to return the unit to the standby condition.

Output Circuit:

E1 to E2 and E4 to E5

With E4 connected to E5, A5C and A5D form a flip-flop. When the A or B STOP pin goes high, pin 10 of A6 goes low to set this flip-flop so that Q27 and Q28 conduct. The unit then remains in this state until A- is applied to the reset line to reset the fli-flop. If A4 has not yet timed-out when the reset is applied, C36 is discharged through R53 and CR32.

E2 to E3 and E5 to E6

In this mode, A5D is connected as in inverter and A5C functions as a negative OR gate. The timer control input (from an external timer) is normally low so that pin 11 of A5 is high. When the A or B STOP pin goes high, pin 10 of A6 goes low and pin 3 of A5 goes high to energize the output (Q28 conducts). This initiates the external timer so that the Timer Control input goes high. A5D inverts this so that a low signal is applied to pin 2 of A5 to keep pin 3 high. When the external timer times-out, the Timer Control input goes back low to allow pin 3 of A5 to go low.

As there is no provision to override the A4 interdigit timer in this mode, the minimum output time is approximately 2.5 seconds. If the external timer is set for less than this, or if no external timer is connected, the minimum output time will be obtained.

ON/OFF Control:

E4 to E5, Resistor between E10 and E11

In this mode, one of the INDIVIDUAL CALL register leads is connected to the A-STOP pin, and the GROUP CALL register lead is connected to the C-STOP pin. When the INDIVIDUAL CALL sequence is received, the A5C/A5D flip-flop is set to energize the output. The output will remain energized until the GROUP CALL code is decoded to cause the C-STOP pin to go high. This is inverted by A10C and the low level at pin 11 of A10 is applied through the 10K resistor between E10 and E11 to reset the A5C/A5D flip-flop.

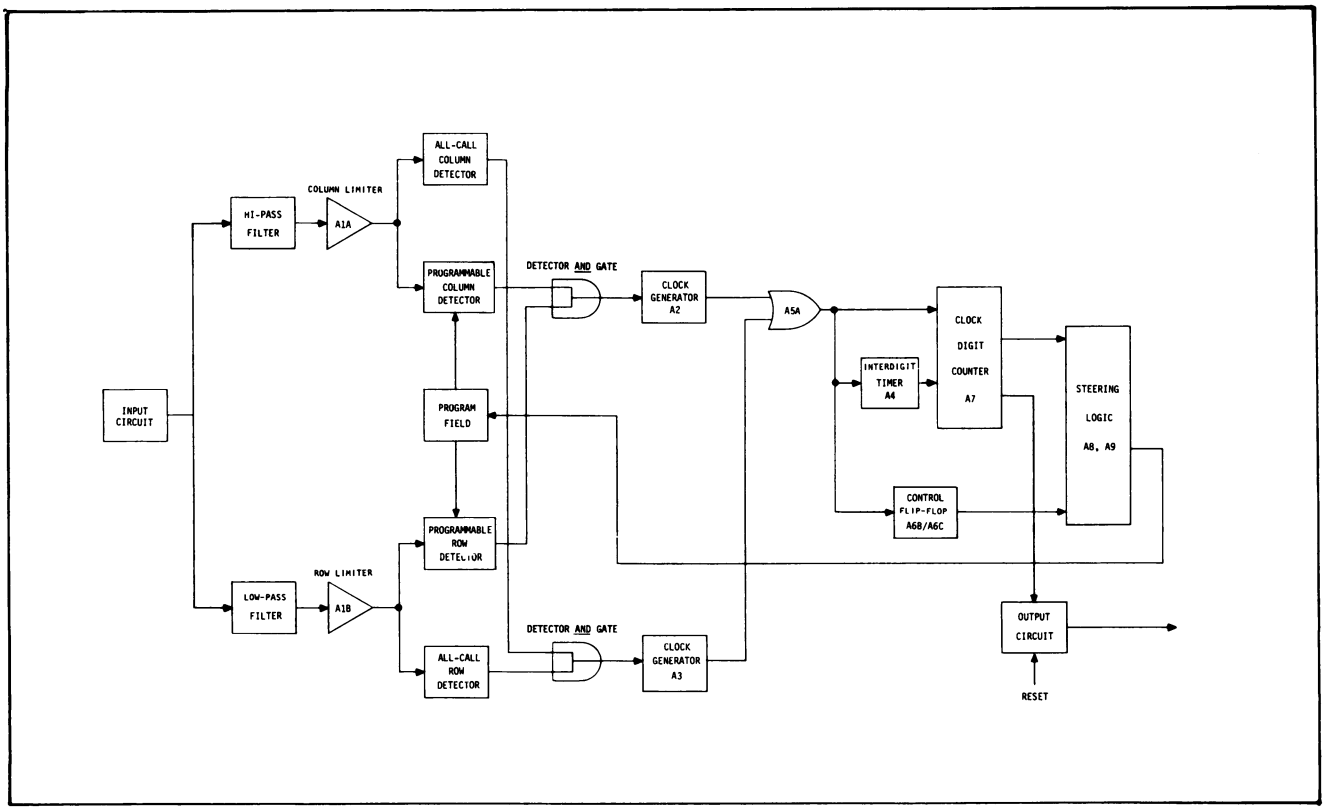


Figure 8A - Model 4503 Decoder Block Diagram

MAINTENANCE

The SPEEDCALL Model 4503 Decoder is designed for stable, trouble-free operation over long periods of time. Most of the parts used in the 4503 are standard, and are available at local distributor stores. The following guidelines are provided to trouble-shoot the unit if it should not operate properly:

- Check that the radios used in the system are properly netted and that the Decoder is properly interfaced
- Check all programming leads to ensure that the unit is programmed to receive the correct codes and that no leads are damaged or broken
- Check that the input power is within specifications and of correct polarity
- Substitute a known operational decoder in place of the suspected faulty decoder. If the substitute unit also fails to operate, the problem is most likely elsewhere in the system

If the Decoder proves faulty, the following steps are recommended to isolate the problem:

a. Voltage at pin 3 of J1 would be 7.5 to 9.0VDC. If not, Q1 or associated circuitry is probably defective.

b. Check programming jumpers and strapping options for proper placement, and for damaged wires. Normally, the Decoder will be tested using the INDIVIDUAL CALL code, or the same code that the unit is failing to decode. If the unit is being tested for use as a spare decoder, the code 1590 is recommended as it uses all row and column frequencies.

INDIVIDUAL CALL SEQUENCE

c. Using a Touch-Tone encoder with a minimum amplitude of 20mVrms, apply the first digit to the Decoder input. DS2 should light. If it does not, proceed to step e. If DS2 does light, release the digit. DS2 should extinguish within approximately 2.5 seconds. If it does not, proceed to step g.

d. If DS2 operates normal, enter the complete INDIVIDUAL CALL sequence. DS1 should light. If it does, but pin A7 or A8, as applicable, does not energize, Q28 is probably defective. If DS1 does not light, proceed to step h.

e. While inserting a Touch-Tone digit, check for minimum level of 300mVrms at TP1 and TP2. If both test points are low, the problem is likely in the audio input circuitry. If either point is good while the other is low, check the corresponding filter and A1 circuits.

f. While applying the first digit of the INDIVIDUAL CALL code, check for a minimum of 450mVrms at TP3 and TP4. If both points are low, check for at least 5VDC at the appropriate digit pin. If this voltage is low, proceed to step g. If only one of the points is low, check that the collector of the appropriate programming transistor (Q15-Q17 for TP3; Q18-Q21 for TP4) is pulled down to approximately 1VDC. If not, the transistor or associated diode is probably defective.

NOTE: If only one digit in a particular column or row provides the proper outputs at TP3 or TP4 while all other digits do not, one of the diodes (CR3-CR26) is probably shorted. For example, assume CR4 to be shorted. Digits 4, 7 and * would give a low output at TP4 while all other digits would check normal.

g. With the Decoder in standby condition with no input, the R-1 register pin should be high (5VDC min.) and the R-2 through R-8 pins should be low. If the R-1 pin is not high and pins 6, 9, 10 and 11 of A8 are low, or more than one register pin is high, A8 is probably bad. If pin 6 of A8 is high, A4, A6B/A6C is probably bad. If pin 9, 10 or 11 is high, check A7.

h. If step g is normal, insert the first digit of the INDIVIDUAL CALL code and release it. Upon release, the R-1 pin should go low and the R-2 pin should go high. If the unit does not count to R-2, check that pin 2 of A7 goes low when the digit is entered. If not, Q22, Q23, A2 or A4 is defective. Pin 1 of A7 should go high when the digit is entered, and return low upon release of the digit. If it does not, check A5A.

i. As each digit of the INDIVIDUAL CALL code is entered and released, each R-pin should go high in sequence. If any digit in the sequence fails to advance the register, repeat steps e and f using this digit.

j. If the register advances to the R-pin connected to the A-STOP pin and Q28 does not energize, check A6D, A5C/A5D and Q27.

GROUP AND ALL CALL CODE SEQUENCES

k. Using an encoder adjusted for 20mVrms minimum, connected to the Decoder audio input, enter the ALL CALL digit. DS3 should light and then extinguish approximately 2.5 seconds after the digit is released. If DS3 does not light, measure TP5 and TP6 for 500mVrms minimum while applying the digit. If low, check the programming leads, Q11 and Q12 or Q13, and Q14.

l. When the ALL CALL digit is entered and released, the GROUP register pin R-2 should go high (5VDC min.). If it does not, check Q24, Q25, A3, A6B/A6C and associated circuitry. If all of these are normal, A9 is probably defective.

m. Entering the ALL CALL code digit repeatedly should cause the register to advance through the GROUP register pins in sequence until the B-STOP pin is energized. If not, A9 is probably defective.

n. Similarly, enter the GROUP CALL sequence, checking that each register pin goes high in sequence. If any digit in the sequence fails to advance the register, repeat step f using this digit.

ALIGNMENT

If the voltage at any test point is abnormal and no other cause for abnormality is found, refer to the following paragraphs for filter and tank circuit alignment. Alignment should normally not be required unless a component in the filter or tank circuit has been replaced, or the glyptol seal has broken and permitted a tuning

to vibrate loose. If any of these events has occured, only the affected circuit should be aligned. In other cases, all possible causes of trouble should be eliminated before alignment is attempted.

A Touch-Tone encoder known to be generating the correct frequencies and having an adjustable output level, an ACVTVM, and a suitable DC power supply are required for filter and tank circuit alignment. Adjust the encoder output for 100mVrms and the power supply for 13.6VDC. Connect the encoder and power supply to the Decoder. Select the .03V range for all of the following alignments:

Filter Alignment:

1. High-Pass Filter: Connect the VTVM to TP1 and simultaneously key digits 7 and 8, or 8 and 9 on the encoder. Adjust L1 for a minimum reading on the VTVM.

2. Low-Pass Filter: Connect the VTVM to TP2 and simultaneously key digits 2 and 5, or 8 and 0 on the encoder. Adjust L2 for a minimum reading on the VTVM.

Tank Circuit Alignment:

From below, select the circuit to be aligned. Connect the VTVM to the test point indicated. Key the encoder for the selected row or column circuit, and adjust the indicated coil for a MAXIMUM reading on the VTVM (.03V range):

Tank Circuit to be Aligned	Connect VTVM to	Key Encoder Digit	Align Coil
Individual Call Column	TP3	1st digit in code	T2
Individual Call Row	TP4	1st digit in code	T3
All/Group Call Column	TP5	Col. jumper digit*	T4
All/Group Call Row	TP6	Row jumper digit**	T5

* This will be the jumper in the ALL CALL programming pin field from the common column pin to the appropriate column digit pin. Any digit appearing in the programmed column may be used.

** This will be the jumper in the ALL CALL programming pin field from the common row pin to the appropriate row digit pin. Any digit appearing in the programmed row may be used.

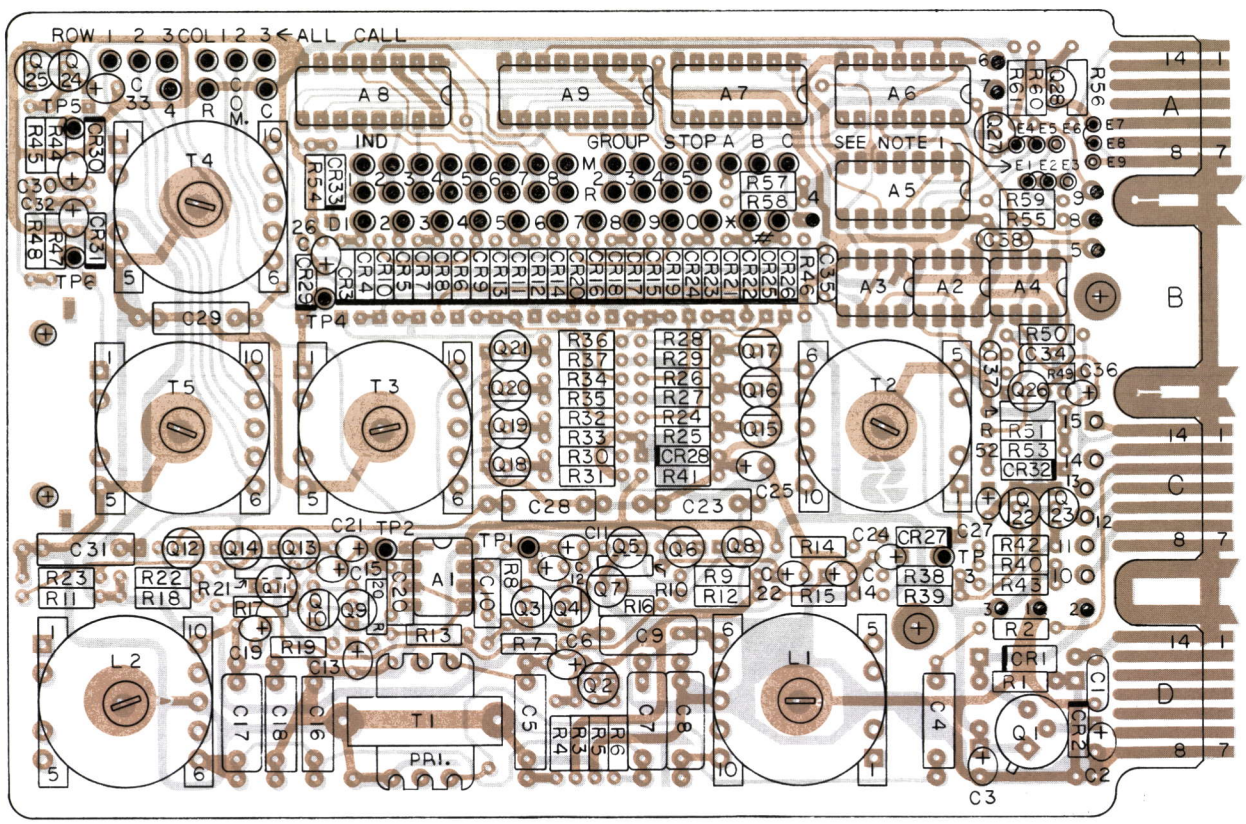


Figure 9 - Component Layout, Printed Circuit Board No. 1

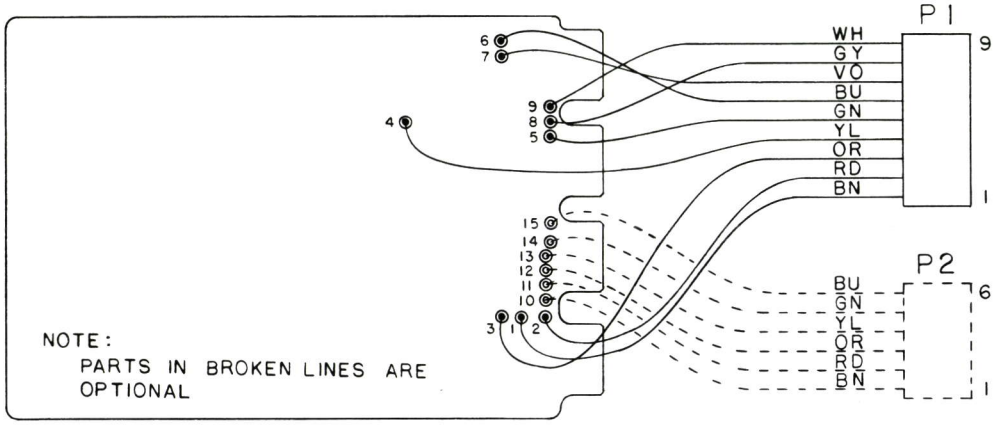


Figure 10 - Interconnect Wiring Diagram

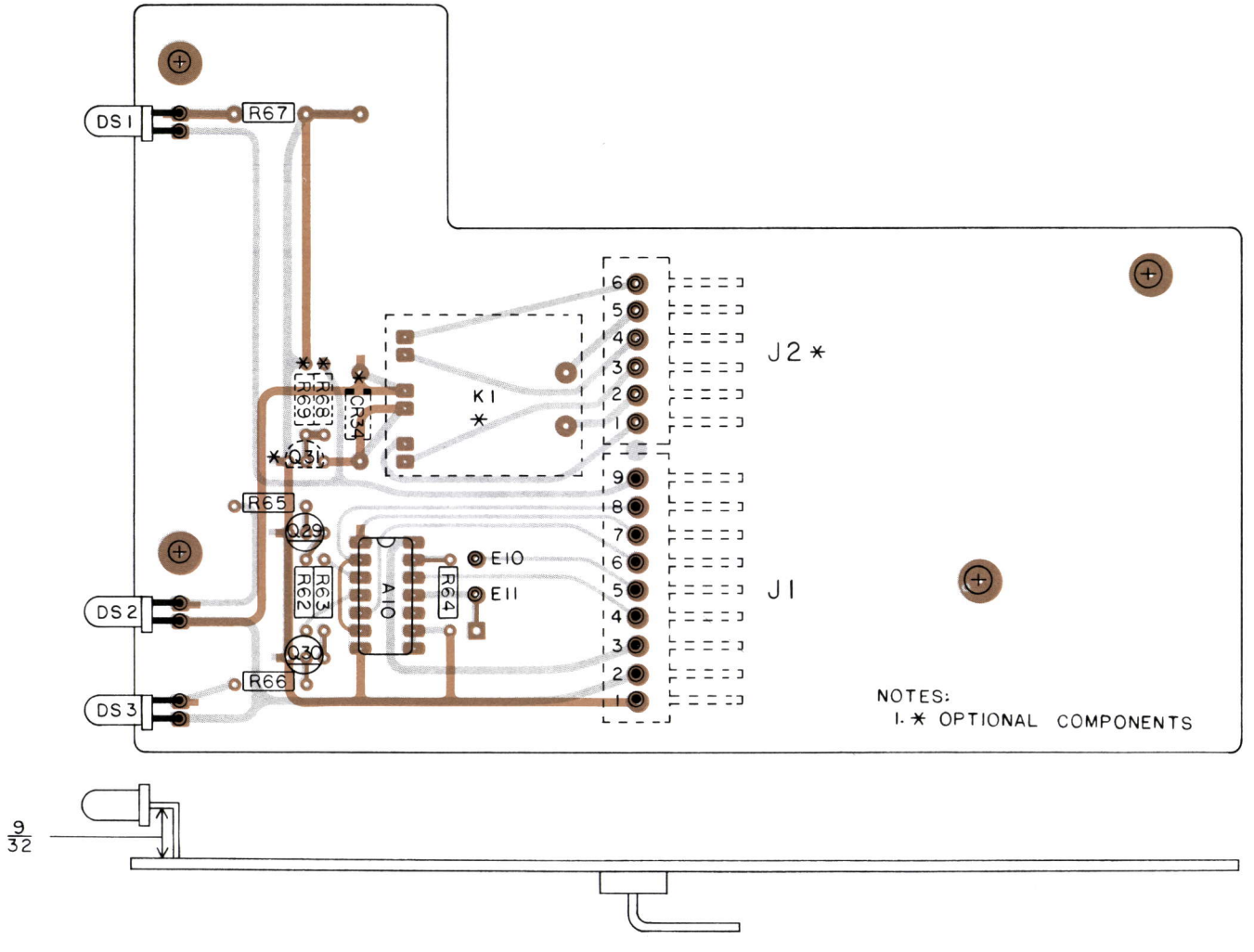


Figure 11 - Component Layout, Printed Circuit Board No. 2

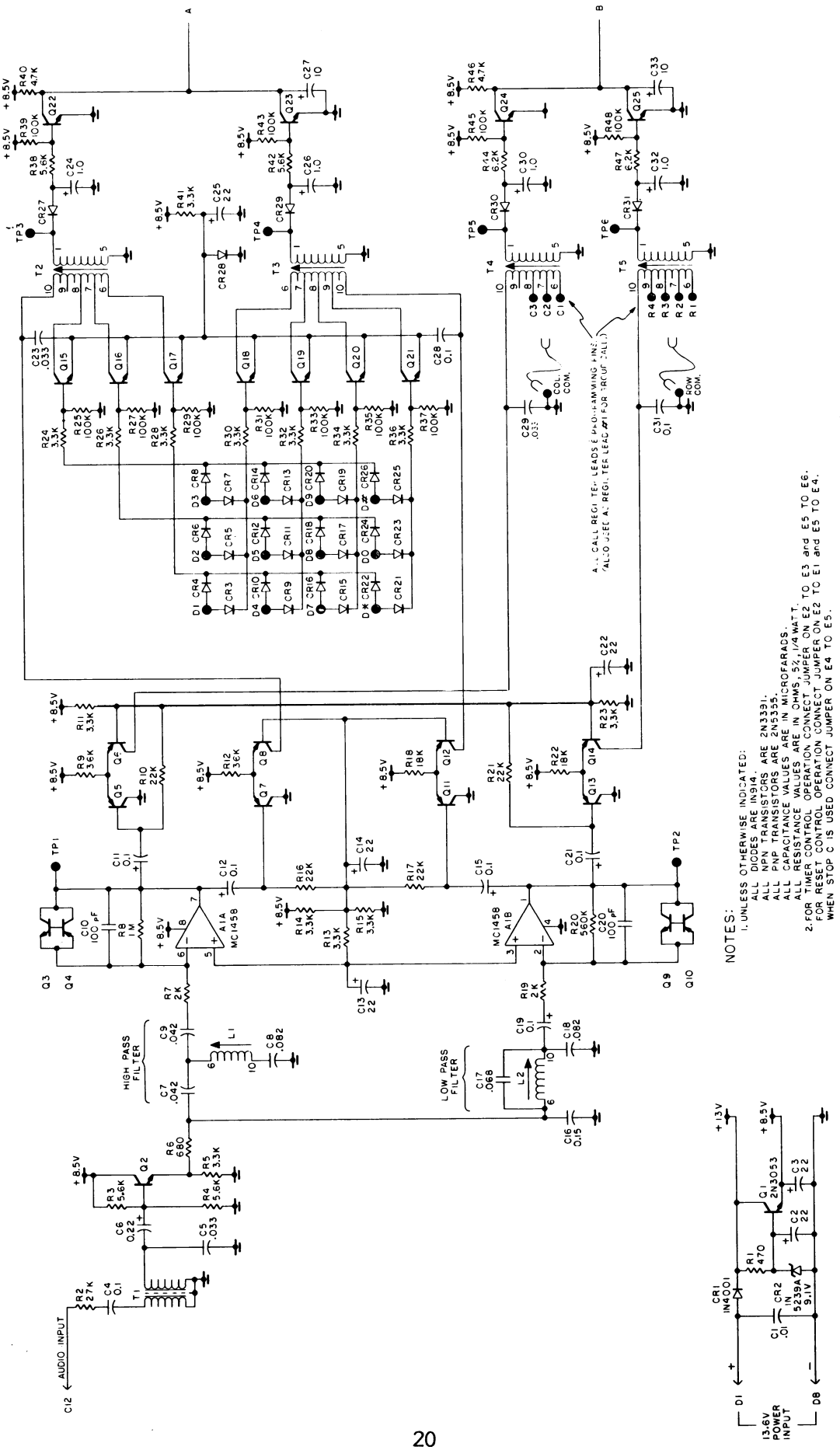


Figure 12 - Model 4503 Decoder Schematic Diagram (Part 1 of 11)

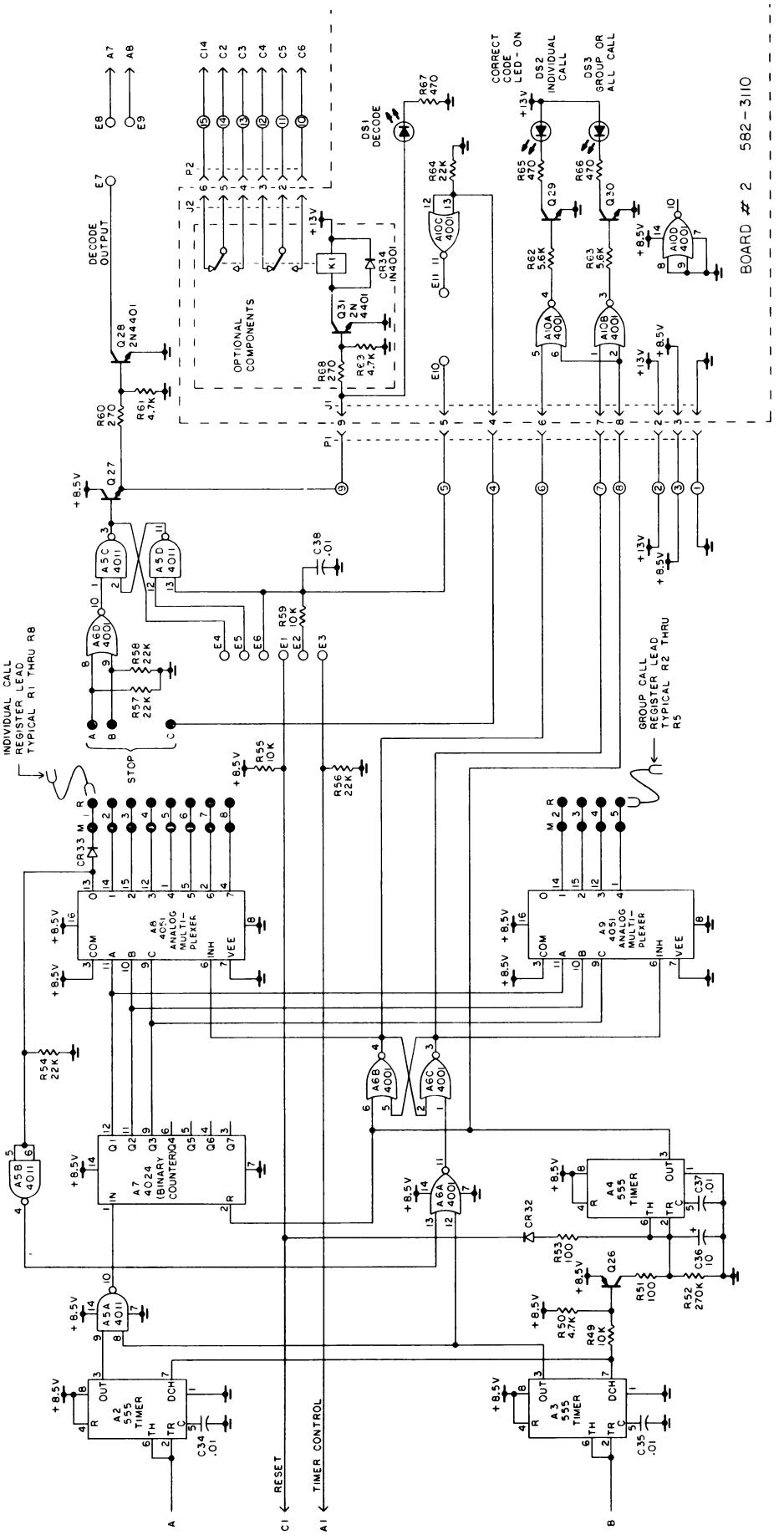


Figure 13 - Model 4503 Decoder Schematic Diagram (Part 11 of 11)

REPLACEABLE PARTS LIST

GENERAL

Comp No	*Description*	*Part No*
	Model 4503 Decoder Final Assembly	582-0000
	PC Board No.1 Final Assembly	582-3000
	PC Board No.2 Final Assembly	582-3100
	Front Panel Final Assembly	582-6000

INTEGRATED CIRCUITS

Comp No	*Description and Manufacturer's Type*	*Part No*
A1	8-Pin DIP, Dual Op. Amp. MC1458	163-0001
A2-3-4	8-Pin DIP, Linear Timer, NE555V	161-0001
A5	14-Pin DIP, Quad 2-Input NAND Gate CD4011AE	160-0022
A6	14-Pin DIP, Quad 2-Input NOR Gate CD4001AE	160-0064
A7	14-Pin DIP, 7-Stage Binary Counter CD4024AE	160-0046
A8-9	16-Pin DIP, Analog Multiplexer CD4051AE	160-0047
A10 *	14-Pin DIP, Quad 2-Input NOR Gate CD4001AE	160-0064

CAPACITORS

Comp No	*Value*	*V*	*%*	*Type*	*Part No*	*Comp No*	*Value*	*V*	*%*	*Type*	*Part No*
C1	0.01uF	1KV	20	Disc Cer	051-0006	C21	0.1uF	35		Tant Rad	053-0001
C2-3	22uF	15		Tant Rad	053-0008	C22	22uF	15		Tant Rad	053-0008
C4	0.1uF	100	10	Mylar	052-0019	C23	0.033uF	50	5	Polycarb	057-0010
C5	0.033uF	100	10	Mylar	052-0011	C24	1.0uF	35		Tant Rad	053-0005
C6	0.22uF	35		Tant Rad	053-0003	C25	22uF	15		Tant Rad	053-0008
C7	0.042uF	50	5	Mylar	052-0014	C26	1.0uF	35		Tant Rad	053-0005
C8	0.082uF	50	5	Mylar	052-0016	C27	10uF	15		Tant Rad	053-0007
C9	0.042uF	50	5	Mylar	052-0014	C28	0.1uF	50	5	Polycarb	057-0008
C10	100pF	100	5	Dip Mica	054-0029	C29	0.033uF	100	10	Mylar	052-0011
C11-12	0.1uF	35		Tant Rad	053-0001	C30	1.0uF	35		Tant Rad	053-0005
C13-14	22uF	15		Tant Rad	053-0008	C31	0.033uF	100	10	Mylar	052-0011
C15	0.1uF	35		Tant Rad	053-0001	C32	1.0uF	35		Tant Rad	053-0005
C16	0.15uF	50	5	Mylar	052-0026	C33	10uF	15		Tant Rad	053-0007
C17	0.068uF	50	5	Mylar	052-0015	C34-35	0.01uF	1KV	20	Disc Cer	051-0006
C18	0.15	50	5	Mylar	052-0026	C36	10uF	15		Tant Rad	053-0007
C19	0.1uF	35		Tant Rad	053-0001	C37-38	0.01uF	1KV	20	Disc Cer	051-0006
C20	100pF	100	5	Dip Mica	054-0029						

DIODES

Comp No	*Mfg's Type*	*Part No*	*Comp No*	*Mfg's Type*	*Part No*
CR1	1N4001	153-0006	CR3-33	1N914	153-0004
CR2	1N5239A, 9.1V Zener	154-0008	CR34 †	1N4001	153-0006

REPLACEABLE PARTS LIST (Continued)

RESISTORS, Carbon Deposit, 1/4 Watt, 5%

Comp No	*Value*	*Part No*	*Comp No*	*Value*	*Part No*	*Comp No*	*Value*	*Part No*
R1	470Ω	140-4700	R26	3.3K	140-3301	R46	4.7K	140-4701
R2	27K	140-2702	R27	100K	140-1003	R47	5.6K	140-5601
R3-4	5.6K	140-5601	R28	3.3K	140-3301	R48	100K	140-1003
R5	3.3K	140-3301	R29	100K	140-1003	R49	10K	140-1002
R6	680Ω	140-6800	R30	3.3K	140-3301	R50	4.7K	140-4701
R7	2K	140-2001	R31	100K	140-1003	R51	100Ω	140-1000
R8	1 Meg	140-1004	R32	3.3K	140-3301	R52	270K	140-2703
R9	36K	140-3602	R33	100K	140-1003	R53	100Ω	140-1000
R10	22K	140-2202	R34	3.3K	140-3301	R54	22K	140-2202
R11	3.3K	140-3301	R35	100K	140-1003	R55	10K	140-1002
R12	36K	140-3602	R36	3.3K	140-3301	R56-58	22K	140-2202
R13-15	3.3K	140-3301	R37	100K	140-1003	R59	10K	140-1002
R16-17	22K	140-2202	R38	5.6K	140-5601	R60	270Ω	140-2700
R18	18K	140-1802	R39	100K	140-1003	R61	4.7K	140-4701
R19	2K	140-2001	R40	4.7K	140-4701	R62-63*	5.6K	140-5601
R20	560K	140-5603	R41	3.3K	140-3301	R64*	22K	140-2202
R21	22K	140-2202	R42	5.6K	140-5601	R65-67*	470Ω	140-4700
R22	18K	140-1802	R43	100K	140-1003	R68 †	270Ω	140-2700
R23-24	3.3K	140-3301	R44	5.6K	140-5601	R69 †	4.7K	140-4701
R25	100K	140-1003	R45	100K	140-1003			

Transistors

Comp No	*Mfg's Type*	*Part No*	*Comp No*	*Mfg's Type*	*Part No*
Q1	2N3053 NPN	178-0004	Q15-25	2N3391 NPN	178-0001
Q2-3	2N3391 NPN	178-0001	Q26	2N5355 PNP	176-0002
Q4-8	2N5355 PNP	176-0002	Q27	2N3391 NPN	178-0001
Q9	2N3391 NPN	178-0001	Q29-30*	2N3391 NPN	178-0001
Q10-14	2N5355 PNP	176-0002	Q31 †	2N4401 NPN	178-0011

Misceilaneous

Comp No	*Description*	*Part No*
DS1 *	LED, Green	156-0005
DS2-3 *	LED, Orange	156-0009
J1 *	Connector, 9-Pin Molex, Right Angle Wafer, 09-66-1091	036-0012
J2 †	Connector, 6-Pin Molex, Right Angle Wafer, 09-66-1061	036-0011
K1 †	Relay, 12V, 2-Form C, PC Mount, R50-E2-Y2-12DC	042-0024
L1	Inductor Coil, High-Pass Filter	521-6400
L2	Inductor Coil, Low Pass Filter	521-6500
P1	Connector Assy, 9-Pin Molex 09-50-7091	039-0065
P2 †	Connector Assy, 6-Pin Molex 09-50-7061	039-0064
T1	Transformer, Audio Input, 10K:2K, PC Mount	024-0004
T2-5	Tone Coil	557-6400

* Components mounted on PC Board #2

† Included only with the optional relay output circuit, components will be mounted on PC board #2 when included

Warranty

SPEEDCALL warrants to Purchaser that all new equipment manufactured by SPEEDCALL for delivery hereunder shall conform to the published specifications and shall be free from defects in material, workmanship, and title.

THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES WHETHER WRITTEN, ORAL, OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR PURPOSE.

The Warranty period is as follows: printed circuit assemblies containing both active and passive components - two years; all other items except fuses, pilot lamps, and nonrechargeable batteries, which are warranted to be operable on arrival - 90 days. The warranty period shall commence upon date of shipment from factory.

If Purchaser notifies SPEEDCALL during the warranty period of a defect under this warranty, SPEEDCALL will correct any defect by (at its option) either repairing any defective part or making a repaired or replacement part available at SPEEDCALL's factory.

Purchaser shall promptly advise SPEEDCALL of such defect, and upon obtaining prior authorization of SPEEDCALL, ship the defective equipment to SPEEDCALL. Purchaser shall bear all expenses incurred in shipping such equipment to SPEEDCALL, and SPEEDCALL shall bear the expense of shipping the repaired or replaced equipment to Purchaser, within the continental United States, unless such equipment was not defective, in which case Purchaser shall bear all reasonable expenses incurred in inspecting, testing, and returning the equipment. Purchaser shall bear the risk of loss or damage during transit.

A service handling charge of $10.00 (ten dollars) and any applicable freight costs will be billed Purchaser for each item returned as defective or inoperable that is instead found to be in good working order and in conformance with published specifications.

Unless specifically noted otherwise in writing, return of equipment constitutes Purchaser's authorization for SPEEDCALL to repair equipment and to invoice Purchaser for any and all reasonable costs of repair labor, parts, and freight on items not covered by the terms of the warranty. Such authorization includes charges for handling of returned items not found defective.

SPEEDCALL shall not be obligated to repair or replace equipment rendered defective, in whole or in part, by causes external to the equipment, such as, but not limited to, catastrophe, power failure or transients, over-voltage on interface, environmental extremes, and improper use, maintenance or application of the equipment.

Equipment and accessory items not manufactured by SPEEDCALL carry the standard warranty of the manufacturer thereof.

SPEEDCALL's liability arising from the sale or use of the equipment, whether on warranty, contract, or negligence, shall not exceed the cost of correcting defects as provided herein and all such liabilities will terminate upon expiration of the warranty period.

The foregoing constitutes Purchaser's sole and exclusive remedy for the furnishing of non-conforming or defective goods and SPEEDCALL shall not in any event be liable for the cost of any labor expended on such goods or for any special, direct, indirect or consequential damages by reason of the fact that such goods shall have been non-conforming or defective.

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