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DESCRIPTION

The Area Select Option allows the user to inhibit Repeater Acquisition on a selected 10 of 20 channels comprising either Area A or Area B. The area is selected by the area select switch on the control unit. A TONE DET (busy signal) is provided on channels 17-26 when Area A is selected on the control unit, permitting communications over channels 1-10. The opposite is true when Area B is selected.

The area select option board is mounted on standoff posts beneath the logic board on the opposite side of the hinged panel. The interconnecting cable connects logic board J2401 to J1 on the area select option board.

Seven IC's are used on the area select option board three of which (U4, U5 and U6) are CMOS and require special handling to avoid damage by static discharges.

CAUTION

The CMOS Integrated Circuit devices used in this equipment can be destroyed by static discharges. Before handling one of these devices, the serviceman should discharge himself by touching the case of a bench test instrument that has a 3-prong power cord connected to an outlet with a known good earth ground. When soldering or de-soldering a CMOS device, the soldering iron should also have a 3-prong power cord connected to an outlet with a known good earth ground or a battery-operated soldering iron should be used.

CIRCUIT ANALYSIS

The area select board contains a timer U3, PROM U1, exclusive OR decoder U4 and U5, combiner U6, output driver Q3, Q4 and power control circuit Q1, Q2 and VR1.

The power control circuit enables the area select option only when the radio is

in the Tx WAIT Mode. When WAIT LIGHT signal is present at P1-11, Q2 and Q1 turn on to apply +10 V to 5 volt regulator VR1. VR1 supplies power to the option board circuitry.

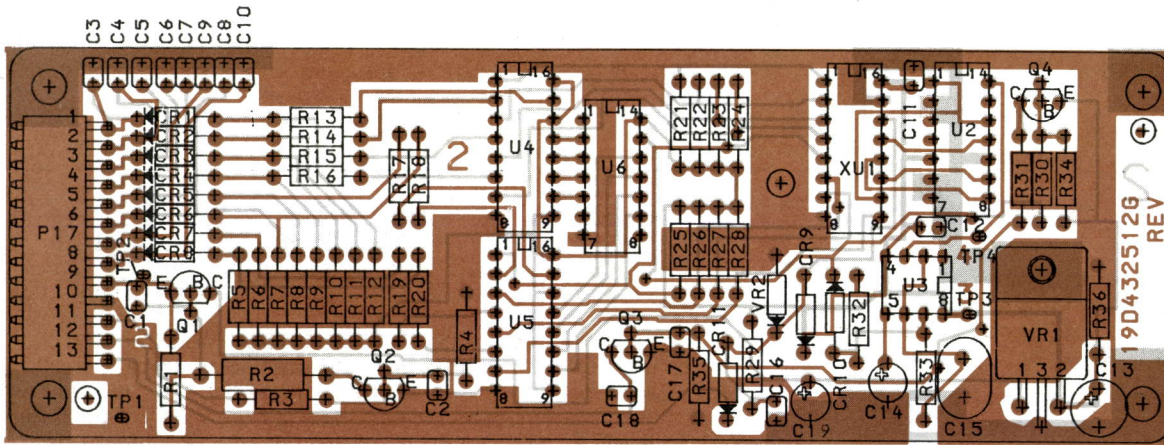
U1 is an 8 X 32 bit PROM and is divided into two pages. A page consists of 10 addressable locations with each location containing the 8-bit binary description of 1 of 10 assigned channel numbers. Area A contains channels 17-26 and Area B channels 1-10.

Timer U3 operates at a frequency of 150 Hz. The output of the timer is applied to the decode counter. The counter will advance thru all ten locations in less than 90 ms.

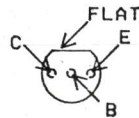
The decode counter sequentially advances the address counter through the 10 locations on the selected page. The page is selected by the AREA SELECT input from P1-13. When P1-13 is "0" LOCATION 1-10 is addressed and when P1-13 is "1" LOCATION 17-26 is addressed. The output of the FREQ PROM is the binary description of the channel numbers located in PROM addresses 1-10 or 17-26 and correspond to the user channel numbers. The output at any given time depends on the page and address sequenced by the decode counter.

Exclusive OR decode gates U5 and U6 compare the channel number received from the Logic board on P1-1-8 with the channel numbers stored in the PROM. If the channel numbers correspond a logic 1 will be present simultaneously on all input pins of combiner U6. A logic 0 is then applied to timer U2 to stop the clock while the valid input from the logic board is present and to output driver Q4, Q3.

Q4 turns Q3 on to provide TONE DET to the logic board. TONE DET indicates to the radio that the channel is busy and cannot be used for transmissions. The channel search generator in the logic board advances to the next channel thereby changing the input configuration on P1-1-8. There no longer is a valid decode and the combiner releases the timer to resume operation.



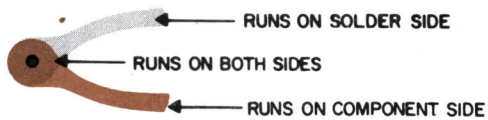
LEAD IDENTIFICATION
FOR Q1 - Q4



IN-LINE
TOP VIEW

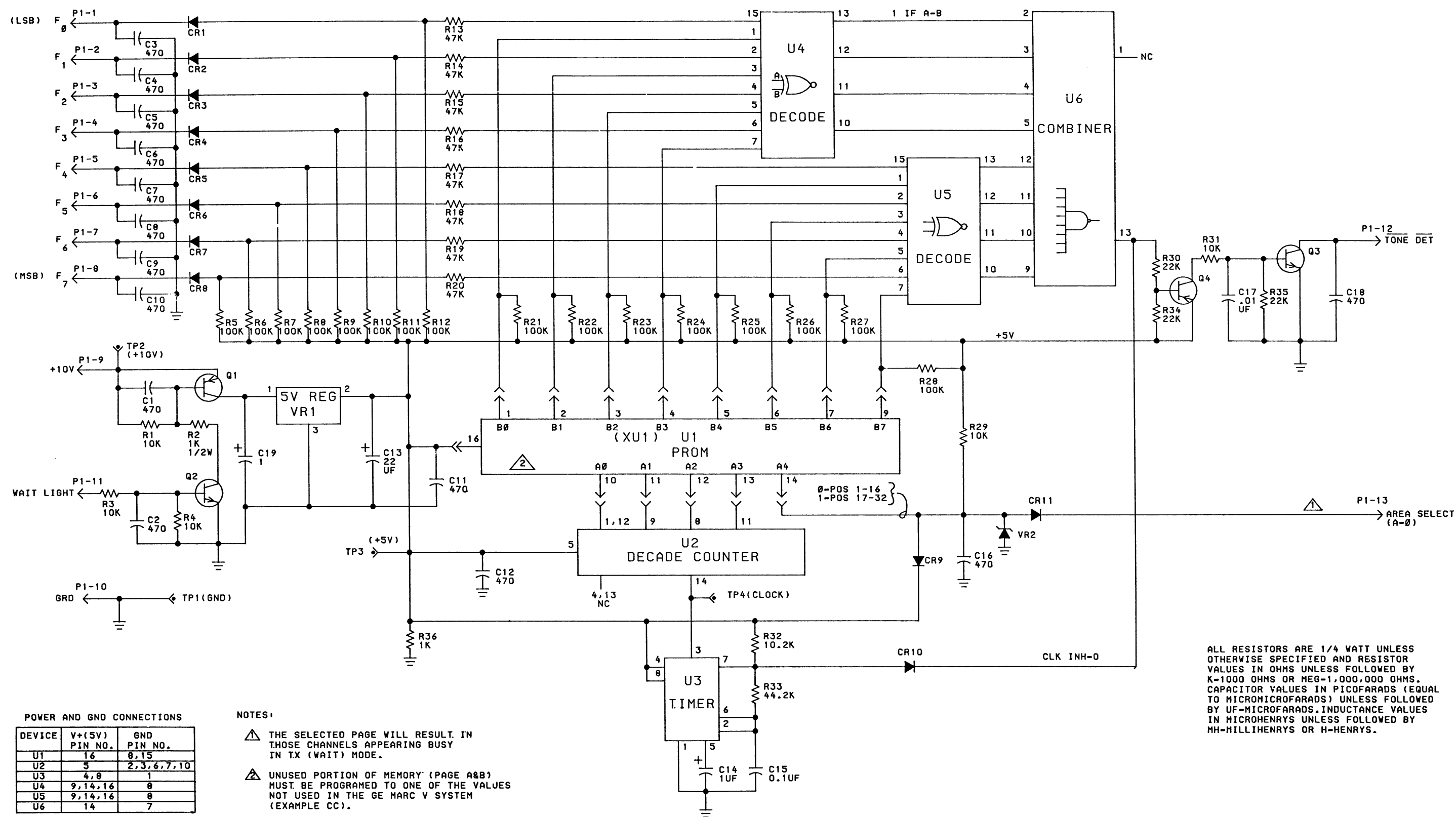
NOTE: CASE SHAPE, IS DETERMINING
FACTOR FOR LEAD IDENTIFICATION.

(19D432627, Rev. 2)
(19A143574, Sh. 1, Rev. 2)
(19A143574, Sh. 2, Rev. 2)



OUTLINE DIAGRAM

AREA SELECT OPTION
GE-MARC V



POWER AND GND CONNECTIONS

DEVICE	V+(5V) PIN NO.	GND PIN NO.
U1	16	8, 15
U2	5	2, 3, 6, 7, 10
U3	4, 8	1
U4	9, 14, 16	8
U5	9, 14, 16	8
U6	14	7

NOTES:

- ⚠ THE SELECTED PAGE WILL RESULT IN THOSE CHANNELS APPEARING BUSY IN TX (WAIT) MODE.
- ⚠ UNUSED PORTION OF MEMORY (PAGE A&B) MUST BE PROGRAMED TO ONE OF THE VALUES NOT USED IN THE GE MARC V SYSTEM (EXAMPLE CC).

ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY K=1000 OHMS OR MEG=1,000,000 OHMS. CAPACITOR VALUES IN PICO FARADS (EQUAL TO MICROFARADS) UNLESS FOLLOWED BY UF-MICROFARADS. INDUCTANCE VALUES IN MILLIHENRYS UNLESS FOLLOWED BY H-HENRYS.

SCHEMATIC DIAGRAM
AREA SELECT OPTION
GE-MARC V

(19D432534, Rev. 4)

PARTS LIST

AREA SELECT OPTION
19D432512G1 - REV. A
ISSUE 2

SYMBOL	GE PART NO.	DESCRIPTION
----- CAPACITORS -----		
C1 thru C12	19A116192P2	Ceramic: 470 pF ±20%, 50 VDCW; sim to Erie 811-A050-W5R-471M.
C13	19A701534P8	Tantalum: 0.47 uF ±20%, 35 VDCW.
C14	19A701534P4	Tantalum: 1 uF ±20%, 35 VDCW.
C15	19A702059P13	Polyester: 0.1 uF ±5%, 50 VDCW.
C16	19A116192P2	Ceramic: 470 pF ±20%, 50 VDCW; sim to Erie 811-A050-W5R-471M.
C17	19A116192P1	Ceramic: 0.01 uF ±20%, 50 VDCW; sim to Erie 8121 Special.
C18	19A116192P2	Ceramic: 470 pF ±20%, 50 VDCW; sim to Erie 811-A050-W5R-471M.
C19	19A701534P4	Tantalum: 1 uF ±20%, 35 VDCW.
----- DIODES AND RECTIFIERS -----		
CR1 thru CR11	19A700028P1	Silicon, fast recovery: fwd current 75 mA, 75 PIV; sim to Type 1N4148.
----- PLUGS -----		
P1	19A700072P143	Printed wire: 13 contacts rated at 2.5 amps; sim to Molex 22-05-3131.
----- TRANSISTORS -----		
Q1	19A115852P1	Silicon, PNP; sim to Type 2N3906.
Q2 and Q3	19A115910P1	Silicon, NPN; sim to Type 2N3904.
Q4	19A115852P1	Silicon, PNP; sim to Type 2N3906.
----- RESISTORS -----		
R1	19A700106P87	Composition: 10K ohms ±5%, 1/4 w.
R2	19A700113P63	Composition: 1K ohms ±5%, 1/2 w.
R3 and R4	19A700106P87	Composition: 10K ohms ±5%, 1/4 w.
R5 thru R12	19A700106P111	Composition: 100K ohms ±5%, 1/4 w.
R13 thru R20	19A700106P103	Composition: 47K ohms ±5%, 1/4 w.
R21 thru R28	19A700106P111	Composition: 100K ohms ±5%, 1/4 w.
R29	19A700106P87	Composition: 10K ohms ±5%, 1/4 w.
R30	19A700106P95	Composition: 22K ohms ±5%, 1/4 w.
R31	19A700106P87	Composition: 10K ohms ±5%, 1/4 w.
R32	19A701250P302	Metal film: 70.2K ohms ±1%, 1/4 w.
R33	19A701250P363	Metal film: 4.2K ohms ±1%, 250 VDCW, 1/4 w.
R34 and R35	19A700106P95	Composition: 22K ohms ±5%, 1/4 w.
R36	19A700106P63	Composition: 1K ohms ±5%, 1/4 w.
----- TEST POINTS -----		
TP1 thru TP4	19A701622P1	Cotter pin.

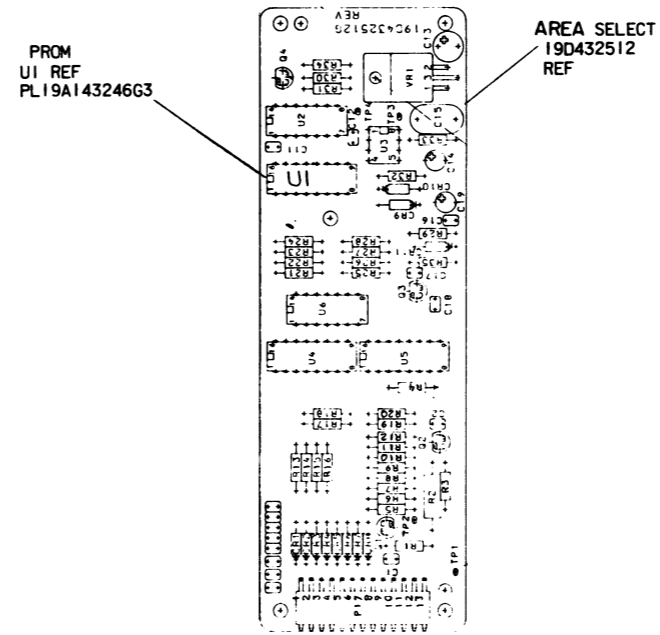
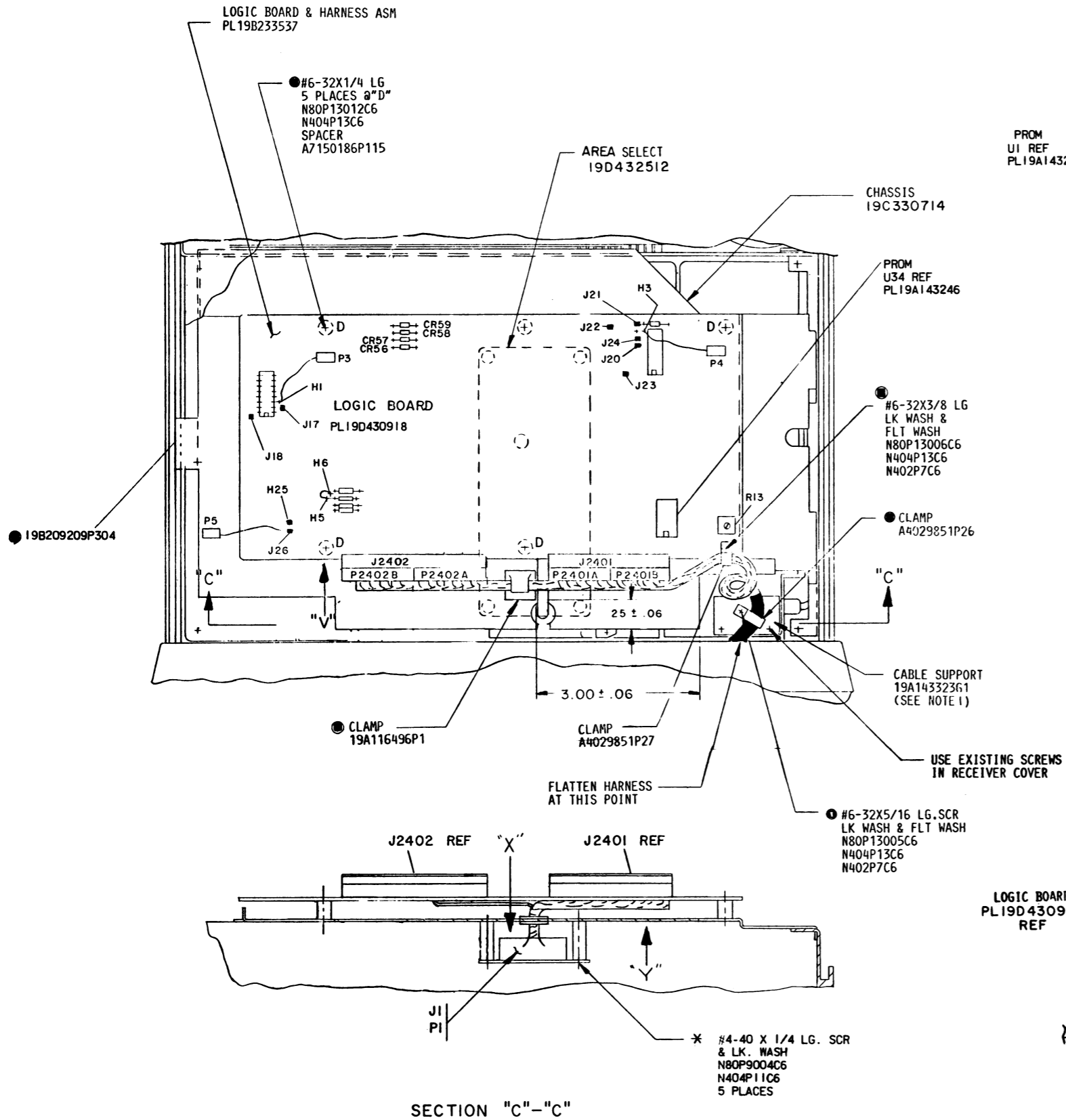
SYMBOL	GE PART NO.	DESCRIPTION
----- INTEGRATED CIRCUITS -----		
U2	19A134305P342	Digital, Decode Counter.
U3	19A134827P1	Linear, Dual In-Line 8 Pin Mini Dip Package; simto EXAR XR-L555CN.
U4 and U5	19A134097P212	Digital, 64-Bit And/Or Selector, (Quad 2-Channel Data Selector).
U6	19A134097P54	Digital: 8 Input NAND GATE.
----- VOLTAGE REGULATORS -----		
VR1	19A134717P1	Linear, Positive Voltage Regulator, 4K PROGRAMMED MEMORY.
VR2	19A700025P7	Silicon, zener: 400 mW max; sim to BZX55-C5V6.
----- SOCKETS -----		
XU1	19A134667P1	Socket, integrated circuit, 16 contacts.
ASSOCIATED PARTS		
U1	19A143246G3	Test PROM.

PRODUCTION CHANGES

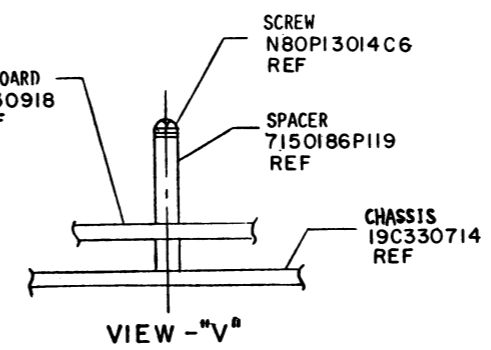
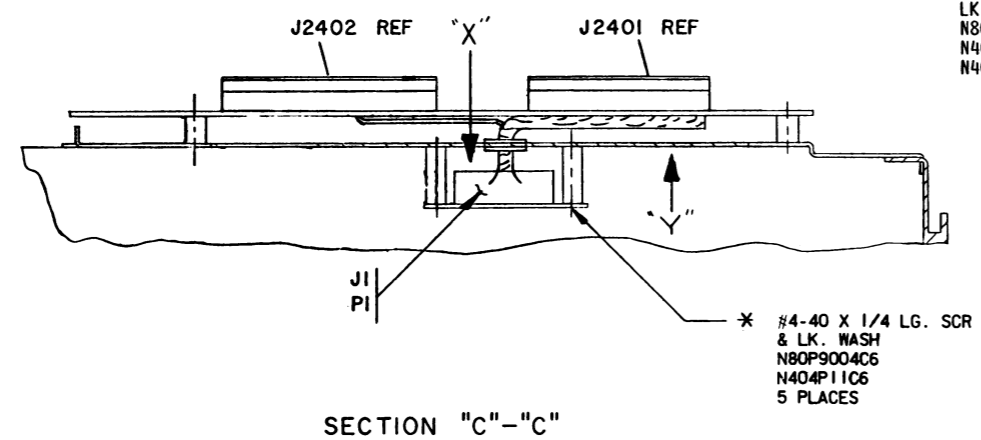
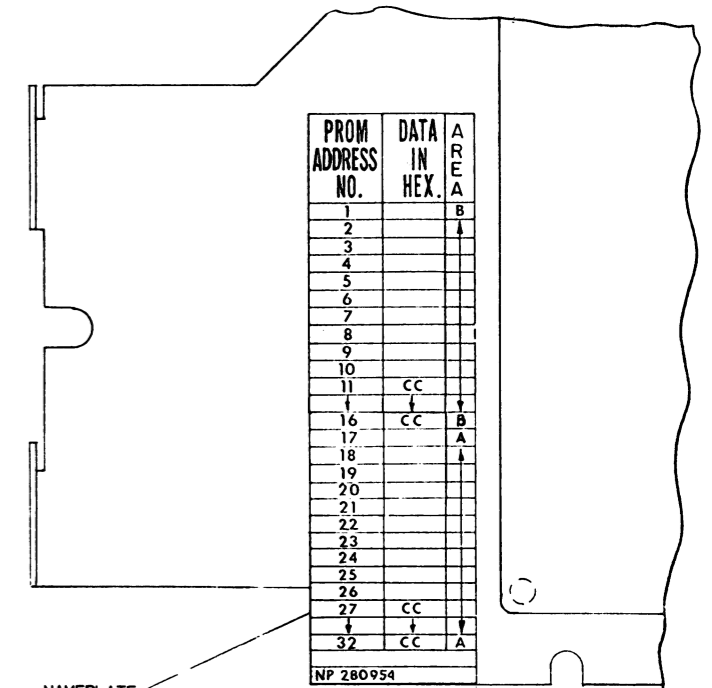
Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter," which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by these revisions.

REV. A - Area Select Option Board 19D432512G1

To provide negative spike protection for PROM A4 address line. Added VR2 and R36.



VIEW "X"
AREA SELECT OPTION BD.



AREA SELECT OPTION (SYNTH)

- NOTE:
1. MOUNT CABLE SUPPORT PRIOR TO TUNING RCVR.
 2. ●PART OF HARDWARE KIT PL19A142874G7
 3. *PART OF HARDWARE KIT PL19A142874G10

INSTALLATION INSTRUCTIONS

AREA SELECT OPTION
GE-MARC V