MAINTENANCE MANUAL

LOGIC BOARD

FOR

CMX-8630 SERIES

TWO-WAY MOBILE RADIOS

TABLE OF CONTENTS

DESCRIPTION

The logic board for the CMX-8630 mobile radio controls the operation of the radio. The logic board provides all of the necessary digital processing, tones and control functions. The logic circuitry controls channel acquisition, scan operation, RF frequency selection, tone generation and detection, timing functions, and operator interface functions. Interface functions include control panel displays and switch panel controls, microphone hookswitch, and programming functions.

The logic board contains the microprocessor, external memory EPROM for the microprocessor, the programmable personality EEPROM, three octal latches for the I/O microcomputer interface and the transmit and receive audio processing circuitry.

The logic board is mounted in the top section of the chassis above the transmitter/receiver/synthesizer (TRS) board. All power and control function interconnections are provided by cables CA11, CA12, CA13, CA3 and CA4.

Simplified diagrams and lead identification information on the Integrated Circuits are contained in the Service Sheet listed in the Table of Contents.

CIRCUIT ANALYSIS

The logic board contains the digital processing and initializing circuitry for the mobile radio.

Digital processing circuitry consists of microprocessor A1, octal latches A2, A11 and A21, EPROM A3 and EEPROM A4.

A3 is an 8K x 8 bit EPROM. It is used by the microcomputer to control all radio and system functions. Crystal Y1 A14 provides the time base to sequence the microcomputer through its internal software program, allowing it to execute the program stored in the program memory.

EEPROM A4 contains all data unique to the radio and is referred to as the Personality PROM. Information stored in the Personality PROM includes data for RF channels and Channel Guard tones as well as all radio options (e.g., carrier control timer, etc).

Power for the logic board is provided by a continuous 13.8 volts (A+), a switched 13.8 volts (SW A+), and a regulated +5 volts (Vcc) from the TRS board. A regulated +5 volts DC, and +8 volts DC (+8 AV) for the logic board audio circuitry is derived from the switched A+.

MICROPROCESSOR OPERATION

OCTAL LATCHES A2, A11 & A21

Octal latches A2 and A11 are used to exchange data passing between microprocessor A1 and the memory and control circuits, respectively.

Octal latch A11 provides the interface between the microprocessor and the control panel switches. A11 is connected so that the latch function is disabled (the "G" input A11-11 connected to 5

volts) and the octal latch operates as a buffer for the microprocessor input.

Latch A21 provides an output interface for the microprocessor. The latch controls the CCT, watchdog timer, SQ SW, XMIT/S LEDS, EXT ALARM EN, TX AUDIO LEVEL CONTROL and frequency band switching. The "G" latch control input is connected to decoder A8-6.

Octal latch A2 has the "G" input connected to the ALE (address latch enable) output of the microprocessor to provide a latched address interface between the microprocessor and program memory A3.

RESET/MEMORY BACKUP

The microprocessor reset and memory backup circuit consists of 5-volt regulator A16, zener diode CR2, switching transistors Q1 and Q2, and pass transistor Q3.

Microprocessor A1 is reset by switched A+ (13.6 volts) on/off, watchdog timer reset, or programmer reset. The microprocessor resets when +5 volts is applied to RST input A1-9 from regulator A16 through pass transistor Q3.

In a power-down state (A+ SW off), zener diode does not conduct, keeping Q1 turned off. When Q1 is off Q2 conducts, turning on Q3. Turning on Q3 applies +5 volts from the collector of Q3 to reset pin U1-9. The 5-volt supply provides the memory backup for microprocessor A1, and keeps A1 in the reset state.

When the radio is turned on (A+ SW on), zener diode CR2 conducts, turning on Q1. Turning on Q1 turns Q2 and Q3 off. The +5 volts to A1-9 decays to about 0 volts as determined by the time constant of C3 and R6. When the voltage at A1-9 drops to approximately 0 volts, the microprocessor starts executing its program memory approximately 12 milliseconds after Q1 turns on and Q2 and Q3 turn off.

WATCHDOG TIMER

The watchdog timer circuit consists of reset switch Q5 and timer A22. The timer monitors the operation of microprocessor A1 and generates a reset pulse if the microprocessor fails to function properly.

When the microprocessor is operating properly, reset pulses from octal latch A21-16 are applied to the base of reset switch Q5 through a delay network consisting of R50, R51 and C5. Turning on Q5 grounds the clock timer input at A22-7. This holds the clock timer output at A22-3 high, which holds the microcomputer reset line to the base of pass transistor high, turning off Q3. Turning off Q3 applies approximately 0 volts to A1-9, keeping microprocessor A1 in the operation state.

When the microprocessor is not operating properly, the reset pulses from A21-6 are not present. Q5 will turn off, and timer A22 will generate a square wave output at A22-3 to reset the micro processor.

MICROPROCESSOR A1

A1 directly interfaces with and controls the operation of all the digital processing circuitry. It also interfaces with the radio and control panel display functions through octal latch A11 and external buffer stages.

Microprocessor A1 responds to manual initiated functions of Push-To-Talk (PTT), frequency selection (ADD, DEL), MONITOR, and SCAN ADD and DEL. All other functions are performed automatically by the microprocessor.

The microprocessor controls the operation of the radio by performing the following major functions:

- System Timing
- Frequency Selection
- Receiver Scan (20 channels)
- Two-Channel Priority
- Tone Generation and Detection
- Transmit/Receive Control
- Front Panel Controls and Displays
- Audio Routing and Mute Control

Microprocessor A1 is sequenced through its program by an internal oscillator whose frequency is set by crystal Y1. The oscillator frequency is 8.192 MHz.

The microprocessor accesses its program memory from EPROM A3. Reading of the stored program at A3 occurs when the PSEN line of A1 is low. The upper eight address lines of A1 (A8-A15) are stationary during this access time. The lower eight address lines of A1 (AD0-AD7) are captured by octal latch A2 and held stationary. ALE (A1-30) is used to latch the lower eight address lines. The output of A3 is then read into the data bus (AD0-AD7) of A1.

The microprocessor interfaces with the microphone through MIC PTT and LOGIC HKSW. It also interfaces with the TQ2310 programmer through HKSW, MIC PTT, SER DAT and SP RESET, and with Personality EEPROM A4.

The microprocessor control signals include the following:

$\overline{EA}$ (Enable) - When low allows microcomputer to retrieve all instructions from external memory.

$\overline{RST}$ (Reset) - Resets microcomputer to beginning of software program when switched A+ is turned off, immediately following power interruptions or with low battery voltage. Also resets when a RST signal from the programmer is received.

SYN DATA - Data transferred to synthesizer representing RF frequencies.

SYN CLOCK - Timing output to synthesizer.

SYN LOCK - A status input signal from the synthesizer to indicate frequency lock status of VCO.

RX MUTE (Receiver Mute) - Turns receiver audio off while operating in wait mode and when transmitting.

$\overline{D\text{-}PTT}$ (Delayed PTT) - Energizes the antenna relay, turns D-PTT (high) off the receiver front end and 1st RF amplifier and turns on Q7 to apply Tx 8 Volts to the exciter. $\overline{D\text{-}PTT}$ switches the bilateral audio gates on the logic board in the transmit and receive mode.

$\overline{MIC\ PTT}$ - The microprocessor monitors the status of the switched PTT lead from the microphone. It also receives clock data on this line while the radio is being programmed.

$\overline{RD}$, $\overline{WR}$ (Read, Write) - Allows the microprocessor to read/write data to/from EEPROM A4 and read/write from/to octal latch A11 and A21.

PSEN (Program Send Enable) - Allows the processor to read instructions from program memory A3.

ALE (Address Latch Enable) - Allows microcomputer to hold the eight least significant lines (AD0-AD7) stable by using octal latch A2. This is necessary when reading from program memory A3 or reading/writing from/to EEPROM A4.

A8-A15 (Address Lines) - Eight most significant address line. These are used to address and access program memory A3 and EEPROM A4.

Push-To-Talk

Pressing the PTT switch on the microphone applies a ground through J2-1 on the logic board to A1-12 on microprocessor A1. The ground on A1-12 causes the D-PTT output at A1-1 to go low, and the RX MUTE output at A1-2 to go high.

The low D-PTT output is applied to inverter A12-5, and the high output at A12-6 is applied to the TRS board at J3-1 to key the transmitter by switching TX 8 Volts to the exciter, and energizing antenna relay K1. The high output at A12-6 is also applied to inverter A13-5 on the logic board. The low output at A13-12 ($\overline{D\text{-}PTT}$) is applied to bilateral switches A9 and A23, switching them from the receive mode to the transmit mode.

NOTE

Bilateral switches A9 and A23 are shown on the Schematic Diagram with the radio in the transmit mode $\overline{D\text{-}PTT}$ low.

Channel Select

When a channel is selected and the bit stream is loaded into the synthesizer, a strobe pulse at J3-5 is applied to the PLL module to allow the synthesizer to generate the correct RF frequency. The microprocessor immediately begins monitoring the LOCK DET LINE to verify that the synthesizer is 'on' frequency. If the synthesizer is not locked on the correct frequency, a low on the LOCK DET line will cause the microprocessor to reload the synthesizer in an attempt to lock it on frequency. If the synthesizer is locked on the correct frequency and MIC-PTT is low, the microprocessor will key the transmitter by applying a low to inverter A12-5, applying the high D-PTT output at A12-6 to the TRS board through J3-1.

Monitor

Pressing the MONITOR pushbutton applies a low to the microprocessor through octal latch A11-7. The low causes the microprocessor to open the receiver so the channel can be monitored.

Channel Guard

In the encode mode, the microprocessor selects the assigned CG tone information from the EEPROM memory for each transmit and receive channel, and generates the Channel Guard signal. This signal is applied as Walsh Bit 0 and 1 to summing amplifier A14. These two bits are summed together and filtered to provide a smooth sine wave for tone Channel Guard.

The output of summing amplifier A14 is controlled by bilateral switch A23. In the encode mode, the $\overline{D\text{-}PTT}$ is low, keeping A23 in the encode/transmit mode to prevent any input from the DISC OUT line from interfering with the encoded

tone. The output of A14 is applied to low pass filter A18. The filter shunts all frequencies above 300 Hz to ground, thereby preventing those frequencies from interfering with the encoded signal. The output of A18 is the assigned CG tone. The CG tone is then applied to the IDC module (A6) through CG deviation control VR5. Channel Guard deviation is normally set for 0.75 kHz.

In the decode mode, the D-PTT input to bilateral switches A9 and A23 is high, changing the switches to the receive mode. Audio and tone from the DISC OUT input at J3-12 is applied to low pass filter A18 through switch A23. This signal is filtered and only the CG tone (if present) is applied to hard limiter A7.

The square-wave output of A7 is coupled through inverter A12-1, 2 and applied to the microprocessor for comparison to determine if the CG tone is correct. If the microprocessor determines that the tone is correct, the RX MUTE line goes high at J3-8, turning the receiver audio on so that the message can be heard in the speaker. Potentiometer VR6 controls the symmetry of the square-wave output of A7.

CARRIER CONTROL TIMER

The Carrier Control Timer (CCT) is contained in and controlled by the microcomputer. Each time the PTT switch is activated, an internal counter begins to count down. If the counter times out, a 500 Hz tone is heard in the speaker for 5 seconds or until the microphone PTT is released. The timing cycle is programmable from 30 seconds to 7.5 minutes in 30-second increments.

EEPROM "WRITE" CONTROL

The EEPROM "WRITE" (WR) control consists of Q10 and Q11. When address bit A9 or A10 from the microprocessor is high, Q10 turns on and Q11 turns off. This applies +5 volts to the WR input which disables the "WRITE" function to protect the channel frequency information.

When address bit A9 or A10 goes low, Q10 turns off and Q11 turns on. This applies a low to the WR input, enabling the WRITE function (if E^2-PROM WR is low from decoder A8) which allows data to be written to the EEPROM. To WRITE to the memory, the WR input must be low, and the OE input must be high. In the RD mode, write is high , OE is low, and CS is low.

The WR function can also be enabled by a low from programmer TQ2310 via SP STORE.

AUDIO CIRCUITRY

Transmit and receive audio signals are routed to and from the logic board audio circuitry through three-stage bilateral switches A9 and A23. The switches are controlled by the D-PTT output of microprocessor A1. In the transmit mode, the $\overline{\text{D-PTT}}$ input to the switch control leads is low, switching the stages to the transmit mode as shown on the logic board Schematic Diagram. When the PTT switch is released, the switches revert back to the receive mode (D-PTT high).

The +8 AV from 8-Volt regulator A17 is applied to voltage dividers R37, R38, and A25 (operational amplifier). The +4-Volt output of A25 establishes the operating reference point for the op-amps (operational amplifiers). C39 provides an AC ground at the summing input of op-amp A7-4 and others.

Transmit Audio

Audio from the microphone at J3-13 (MIC IN) is coupled through C27 and A9-12 and -14 and applied to high-pass filter A20. The filter output is coupled through bilateral switches A9 and potentiometer VR7 to limiter-filter stage A6-11. VR7 controls the audio modulation sensitivity. A6 provides limiting and post-limiter filtering.

The Channel Guard tone (if present) from filter A18 is coupled through bilateral switch A23-14 and -12, and applied to the CG input of A6-5 through CG modulation adjust VR5. The CG tones and audio are combined and applied to summing amplifier A7-4 through VR9. The gain of amplifier A7 is set by switching resistors VR1, R65, VR3 or VR4 in parallel with resistor R59 in the feedback path of A7.

The binary outputs of inverters A13-11 and A13-10 change with frequency in each of the two frequency bands. The different inverter outputs switch different resistors (VR1-VR4, R65) in parallel with feedback resistor R59 to decrease the amplifier gain as the frequency increases. The operation of A5 provides two frequency levels per frequency band to keep the signal applied to the VCO more constant over the frequency ranges.

The amplified and summed output at A7-2 is applied to J3-11, and then coupled through Mod Adjust R64 on the TRS board to the VCO input.

Receive Audio

In the receive mode, the D-PTT input to the logic board goes high, switching A9 and A23 to the receive mode. The

D-PTT input to the TRS board goes low to enable the receiver. The RX MUTE lead remains high, keeping the audio amplifier turned off.

Audio and tone (if present) from the receiver detector is applied to the logic board at J3-12 where it is applied to three different receive circuits.

If the channel being received has been programmed for Channel Guard, both a CG tone and a noise squelch output must be applied to the microprocessor to turn on the receiver audio amp (RX MUTE lead low). First, the CG tone is coupled through A23-1 and -15 to low-pass filter A18. The filtered tone output is coupled through A23-14 and -13, limiter A7 and inverter AR12 and applied to the microprocessor. Next, the signal at J3-12 is coupled through Squelch control VR8 to squelch hybrid A19. The squelch output at A19-1 is applied to the microprocessor through octal latch A11-8 (noise squelch). The valid CG tone input and the squelch input cause the RX MUTE lead to go low, turning on audio amplifier A26 on the TRS board.

Audio from J3-12 is then coupled through A23-4 and -3, A9-13 and -14, and then applied to two high-pass filter stages (A20 and A24) to remove any CG tone. The filtered audio output is then coupled through A9-3 and -4, A9-15 and -1 and applied to audio amplifier A14-7. The amplifier output at J3-10 (RX AUDIO) is coupled through VOLUME control R1 on the front panel and applied to audio amplifier A26 and then to the speaker.

Squelch Switch

Squelch switch Q13 is controlled by the microprocessor output through octal latch A21-19 (CSW). When the radio is in the scan mode, the output at A21-19 (CSW) goes low, turning off Q13. The output at the collector of Q13 is applied to squelch hybrid A19-5, switching the hybrid to the fast squelch mode.

When the radio is not in the scan mode, A21-19 goes high, turning on Q13. This output switches A19 to the normal squelch mode (non-scan).

8-VOLT REGULATOR (+8 AV)

Eight-volt regulator A17 provides power (+8 AV) for the audio circuitry on the logic board. The regulator operates from the 13.6-volt ignition switch voltage. The +8 AV also powers the mobile microphone from J3-13 (MIC HI) on the logic board to J22-4 on the TRS board.

SCAN OPERATION

The scan operation is controlled by the microprocessor, and provides for scanning any or all of up to 20 channels. The scanned channels may be located anywhere within the frequency band of the radio, and can include two priority channels (P1 and P2).

If desired, all 20 channels can be scanned with or without priority level. When SCAN is enabled, scanning of the selected channels starts immediately. Scan time is approximately 50 to 450 milliseconds per channel, depending upon whether Channel Guard has been programmed for a particular scan channel. If a carrier is not detected, the scan time is 50 milliseconds. If a carrier is detected and Channel Guard is programmed for the channel, the time is 200-450 milliseconds, depending upon how close the Channel Guard tone is to the desired tone. Typical value is 250 milliseconds.

Priority 1 (P1) and Priority 2 (P2) channels, if present, are not part of the non-priority channel scan list (S1, S2, S3, ...) and are treated separately. If there is no activity on any of the scanned channels, then the scan sequence is as shown in the following examples.

Example 1: (More than four non-priority channels, i.e., six channels)

P1-P2-S1-S2-S3-S4-P1-P2-S5-S6-S1-S2-P1-P2-S3-S4-S5-S6-P1-P2-...

Example 2: (Four or less non-priority channels, i.e., three channels)

P1-P2-S1-S2-S3-P1-P2-S1-S2-S3-P1-P2-S1-S2-S3-P1-P2-S1-S2-S3-...

Therefore, the scan sequence is: Scan P1 and P2 if programmed. Then scan up to four non-priority channels before scanning P1 and P2 again. If more than 4 non-priority channels exist, then scan will wrap around, continuously scanning four channels of the non-priority list between each P1, P2 scan sequence. If the number

of non-priority channels is less than or equal to four, then all non-priority channels will be scanned between each P1, P2 scan.

As an added example, consider channels 1-8 to be the scanned channels, with P1 being Channel 1 and P2 being Channel 8. The scanning order then would be:

```
S1-S2-S3-S4-P1-P2-S5-S6-S1-S2-P1-P2-S3-S4-...
   7  6  5  4  1  8  3  2  7  6  1  8  5  4
```

Since it takes approximately 50 to 450 milliseconds to scan each channel, then each Priority channel is sampled every 0.3 to 2.7 seconds and the Non-Priority channels are sampled at least once every 0.4 to 3.6 seconds. If Channel Guard is programmed for a channel but no carrier is detected, the scan time for that channel is 50 milliseconds.

SCANNING (STOPPED ON A VALID SCAN CHANNEL)

Once a carrier is detected, the Receive Channel display will light up, indicating that channel. If the channel is a Non-Priority channel, and there are no Priority channels, then scanning is halted. If only a Priority 2 (P2) channel is present, then it is scanned every 5 seconds if it has Channel Guard programmed and carrier is detected, and every second otherwise. If there is only a Priority channel, then it is sampled every 2.5 seconds if it has Channel Guard 1 (P1) and carrier is detected, and every 500 milliseconds otherwise. If there are P1 and P2 Priority channels, the sample rate will vary.

In order to show the various scan conditions, the following conditions are used:

NOTE

The following conditions are shown while listening to a non-priority channel.

CONDITION 1: P1 AND P2 HAVE CHANNEL GUARD PROGRAMMED

a. No carriers detected

```
P1-P1-P2-P1-P1-P2-P1-P1-P2-...
```

tb (time between samples) = 500 msec
ts (time of sample) = 100 msec

Note: ts is the hole time placed in the signal being heard.

b. Carrier on P1 detected/wrong Channel Guard

```
P1-P2-P2-P2-P2-P2-P1-P2-P2-P2-P2-P2-P1-P2-...
```

tb = 1 second
ts = 100 msec for P2
250-500 msec for P1

c. Carrier on P2 detected/wrong Channel Guard

```
P1-P2-P1-P1-P1-P1-P1-P1-P1-P1-P1-P2-P1-...
```

tb = 500 milliseconds
ts = 100 milliseconds for P1
250-500 milliseconds for P2

d. Carrier on P1 and P2 detected/both wrong Channel Guard

```
P1-P1-P2-P1-P1-P2-P1-P1-P2...
```

tb = 2.5 seconds
ts = 250-500 msec

e. Carrier on P1 and right Channel Guard

Stop scan, display P1

f. Carrier on P2 and right Channel Guard

Display P2, scan P1

P1-P1-P1-P1-P1-P1-...

tb = 500 msec
ts = 100 msec

g. Carrier on P2 with right Channel Guard, carrier/wrong Channel Guard P1

P1-P1-P1-P1-P1-...

tb = 2.5 seconds
ts = 250-500 msec

CONDITION 2: PRIORITY 1 HAS CHANNEL GUARD PROGRAMMED, PRI 2 DOES NOT

a. No carriers detected

P1-P1-P2-P1-P1-P2-P1-P1-P2-...

tb (time between samples) = 500 msec
ts (time of sample) = 100 msec

b. Carrier on P1 detected/wrong Channel Guard

P1-P2-P2-P2-P2-P2-P1-P2-P2-P2-P2-P2-P1-P2-...

tb = 1 second
ts = 100 msec for P2
250-500 msec for P1

c. Carrier on P1 detected/right Channel Guard

Stop on P1, stop scan

d. Carrier on P2

Stop on P2, scan P1

P1-P1-P1-P1-...

tb = 500 msec
ts = 100 msec

e. Carrier on P2 and P1 with wrong Channel Guard on P1

Stop on P2, scan P1

P1-P1-P1-P1-P1-P1-...

tb = 2.5 seconds
ts = 250-500 msec

CONDITION 3: P2 HAS CHANNEL GUARD, P1 DOES NOT

a. No carriers detected

P1-P1-P2-P1-P1-P2-P1-P1-P2-...

tb (time between samples) = 500 msec
ts (time of sample) = 100 msec

b. Carrier on P2 detected/wrong Channel Guard

P1-P2-P1-P1-P1-P1-P1-P1-P1-P1-P1-P2-P1-...

tb = 500 milliseconds
ts = 100 milliseconds for P1
250-500 milliseconds for P2

c. Carrier on P2 detected/right Channel Guard

Stop on P2, scan P1

P1-P1-P1-P1-P1-P1-...

tb = 500 msec
ts = 100 msec

d. Carrier on P1 detected

Stop on P1, stop scan

CONDITION 4: P1 AND P2 WITH NO CHANNEL GUARD

a. No carriers detected

P1-P1-P2-P1-P1-P2-P1-P1-P2-...

tb (time between samples) = 500 msec
ts (time of sample) = 100 msec

b. Carrier on P2

Display P2, scan P1

P1-P1-P1-P1-P1-P1-...

tb = 500 msec
ts = 100 msec

c. Carrier on P1

Stop on P1, stop scan

HANG TIME

If the carrier on a Non-Priority channel disappears before a carrier is detected on a Priority channel, then a 5-second hang time is applied before Non-Priority scanning is resumed. However, during this time the Priority channels are still being sampled. The hang time is provided to prevent fades from causing big gaps in the audio signals. The transmitter may be keyed at any time during the hang time. The hang time is restarted when the transmitter is unkeyed.

If a carrier (or Channel Guard tone if programmed) is detected on a Priority channel during the sample period, then the channel is immediately switched to the Priority channel, and either the PRI-1 or PRI-2 indicator will turn on. If the carrier is on Priority 1 channel, scanning is stopped until the carrier goes away (plus the five second hang time). If the carrier is on the P2 channel, then P1 is still sampled every 500 milliseconds if no Channel Guard, and every 2.5 seconds if Channel Guard is programmed. If there is no P1 channel, then scanning is stopped until the carrier disappears (+5 seconds). Once a carrier is detected on the P1 channel, the channel is switched to Priority 1 regardless of what is being received on another channel (Non-Priority or P2).

OTHER CHARACTERISTICS

When the microphone is removed from the hookswitch, scanning will stop and revert to the Pre-Scan selected channel if the scan has not stopped on any channel. The scan light will blink. Transmit (if a valid Tx frequency is programmed) is possible on the pre-scan channel while off-hook. The channels can be changed during this mode, but when the microphone is returned to the hookswitch, hang time occurs on the pre-scan selected channel.

If a channel has been detected and the radio is hanging on this channel, then scanning stops and the radio will sit on the Received scan channel until the microphone is placed on the hookswitch or scan is disabled by pressing the SCAN button. If the microphone is replaced on the hookswitch scanning will resume five seconds later. Channel changes are allowed until the microphone is replaced in the hookswitch. When scan is disabled, the radio automatically reverts to the Pre-scan selected channel.

When the PTT is pressed, the channel that the scan was hanging on when the microphone was removed from the hookswitch will be the transmit channel. This is the displayed channel. If the PTT is pressed while on-hook and in SCAN, the transmitter is disabled until scan stops on a valid channel or scan is disabled.

Once stopped on a channel and the microphone removed from the hookswitch, the Channel Guard decode function is disabled until the microphone is returned to the hookswitch.

When in the scan mode and the channel display blinks while displaying a channel number, this indicates that one of the scan channels is not locking on frequency (not properly programmed, radio not properly aligned, etc.). Slowly stepping through the channels with scan disabled will reveal the bad channel because the channel display will blink on the bad channel only.

GENERAL ELECTRIC COMPANY • MOBILE COMMUNICATIONS DIVISION
WORLD HEADQUARTERS • LYNCHBURG, VIRGINIA 24502 U.S.A.

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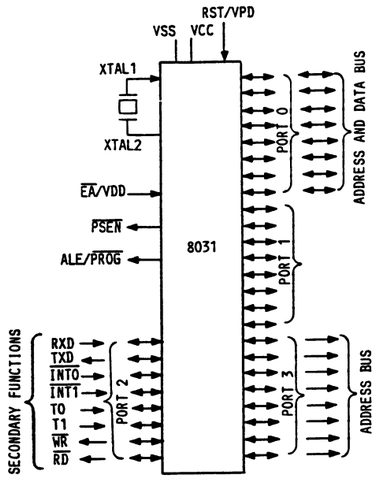
MICROPROCESSOR A1

LOGICAL SYMBOL



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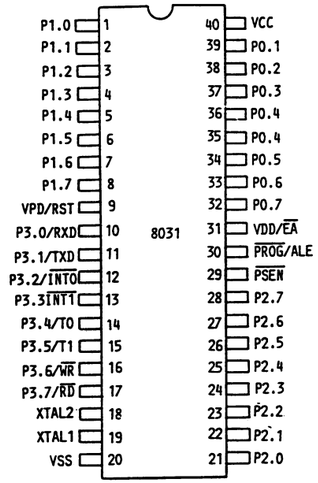
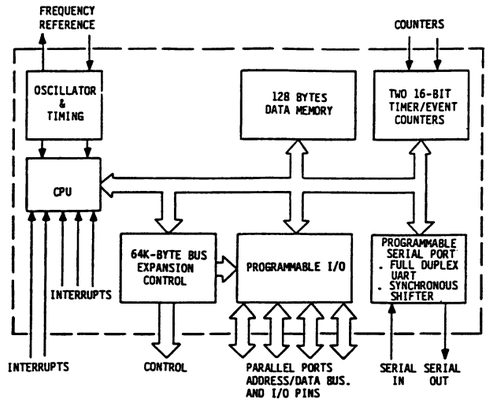


BLOCK DIAGRAM



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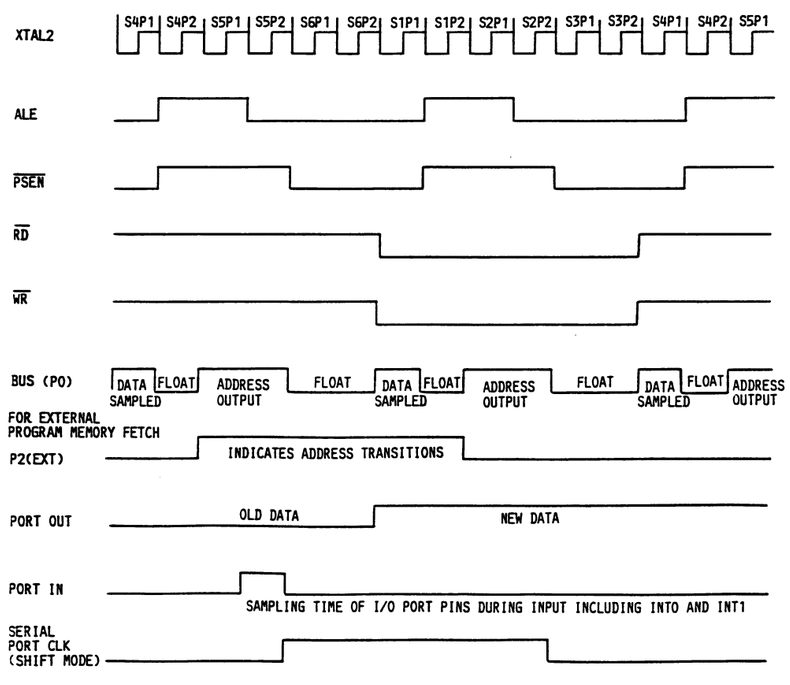
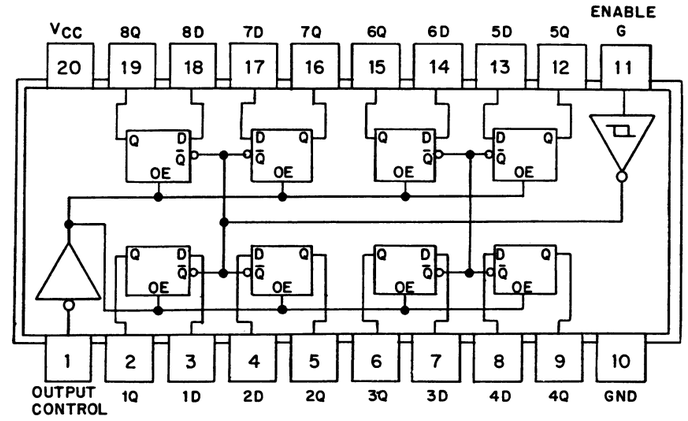


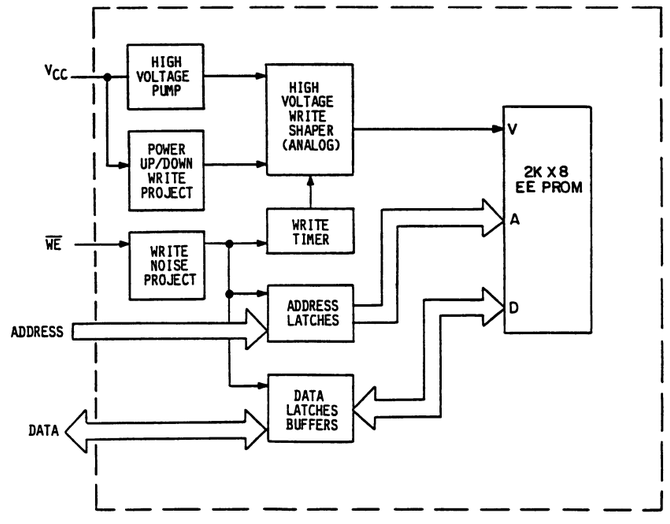
OCTAL LATCH A2 , A11 , A23

LBI-31616

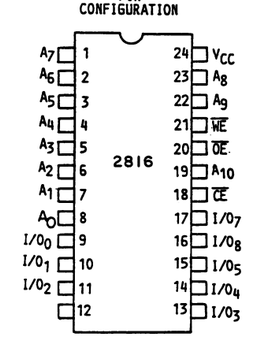


EE PROM A4

FUNCTIONAL DIAGRAM



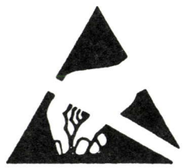
PIN CONFIGURATION



PIN NAMES

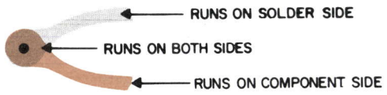
A_0-A_{10}	ADDRESS INPUTS
I/O_0-I/O_7	DATA INPUTS/OUTPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
V_{CC}	+5V
V_{SS}	GROUND

RC5218

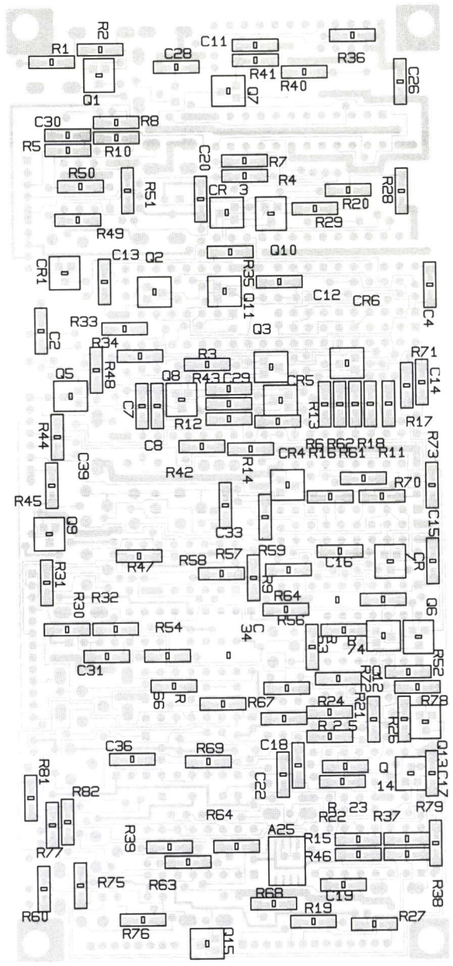


CAUTION

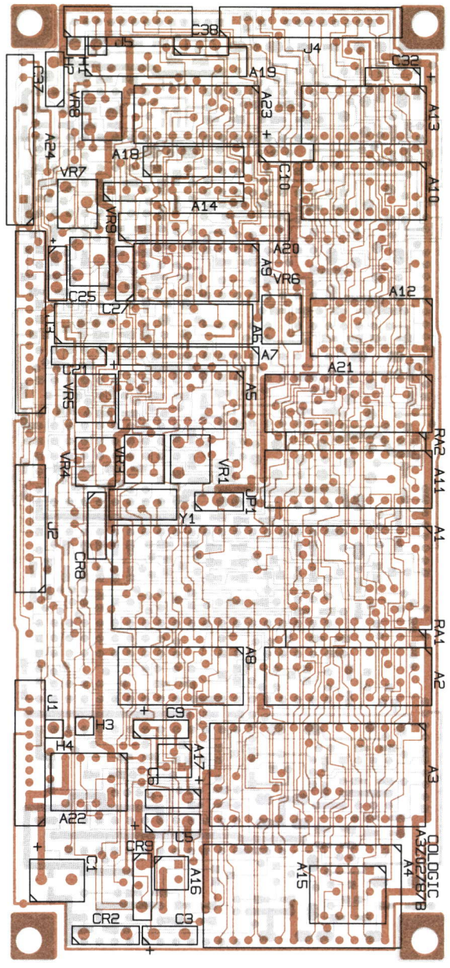
OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES



SOLDER SIDE



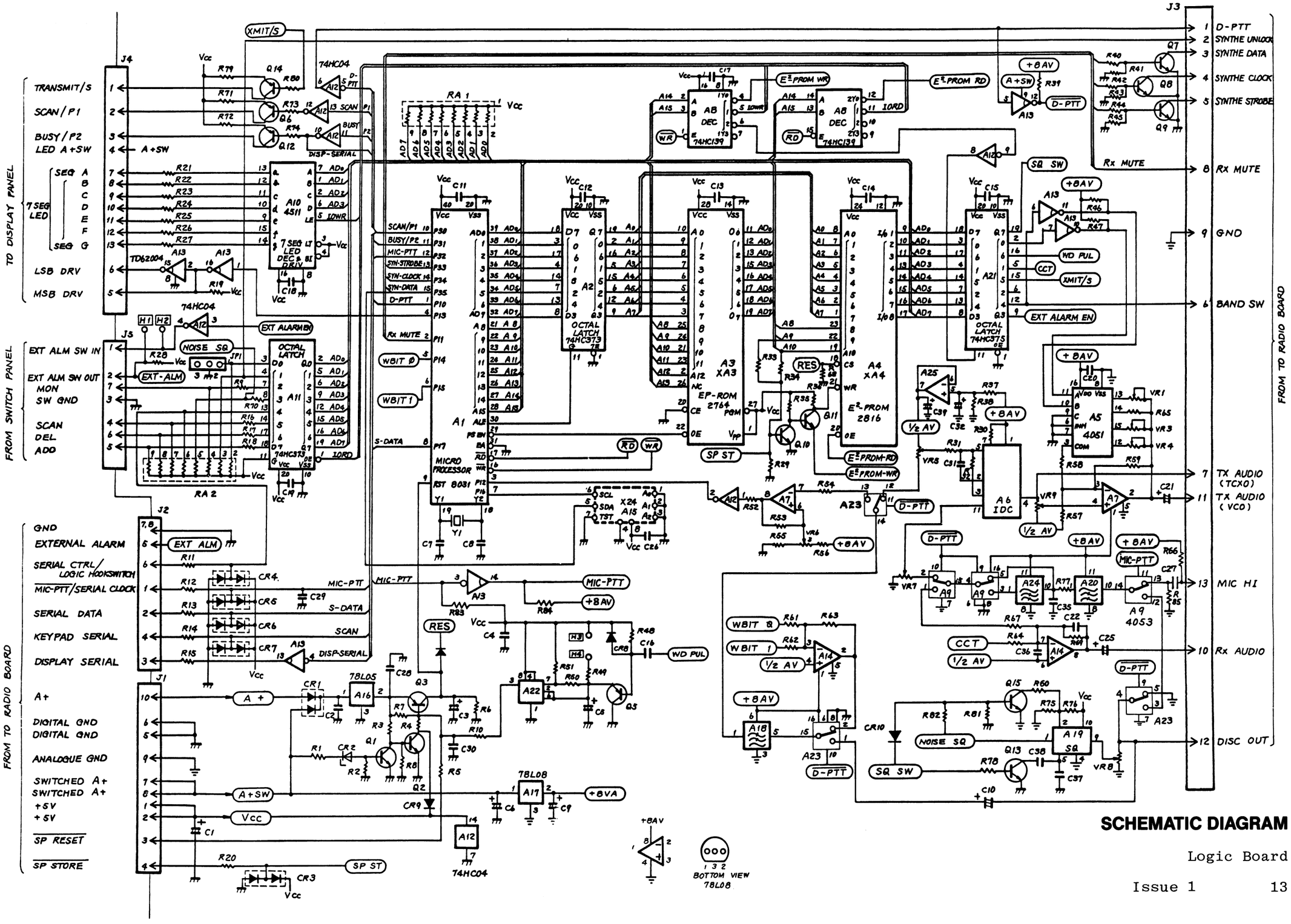
COMPONENT SIDE



OUTLINE DIAGRAM

Logic Board

12 Issue 1



SCHEMATIC DIAGRAM

Logic Board

PARTS LIST

LOGIC BOARD
FOR
CMX-8630

ISSUE 1

SYMBOL	PART NO.	DESCRIPTION
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - - -
A1	KEC/2ADA005179	Microprocessor, P8031AH
A2	KEC/2ABD018108	Octal Latch, TC74HC373P
A3	KEC/2ACA033108	EPROM, M5L 2764K (GE Part No. 19A704982G1)
A4	KEC/2ACA040087	EEPROM, X2816AP
A5	KEC/2ABC036028	TC4051BP
A6		HIC, Pre Amp, Limiter, PLF, AFM24F3300F2
A7	KEC/2AAB020017	Dual Op-Amp, BA718
A8	KEC/2ABD018074	Decoder, TC74HC139P
A9	KEC/2ABC037018	Bilateral Switch, TC4053BP
A10	KEC/2ABC057040	7-Segment LED Driver, TC4511BP
A11	KEC/2ABD018108	Octal Latch, TC74HC373P
A12	KEC/2ABD018165	Inverter, TC74HC04P
A13	KEC/2AAG021010	Inverter, TD62004P
A14	KEC/2AAB020017	Dual Op-Amp, BA718
A15		EEPROM, X2416
A16	KEC/2AAE049161	5-Volt Regulator, AN78L05
A17	KEC/2AAE049187	8-Volt Regulator, AN78L08
A18		Low Pass Filter, HIC
A19		Squelch Hybrid, HIC
A20		High Pass Filter, HIC
A21	KEC/2ABD018108	Octal Latch, TC74HC373P
A22	KEC/2AAH001029	Timer, HA17555PS
A23	KEC/2ABC037018	Bilateral Switch, TC4053BP
A24		High Pass Filter, HIC, AFH85F270A2
A25	KEC/2AAB004243	Microprocessor, 1251G2
		- - - - - - - - - - CAPACITORS - - - - - - - - -
C1	KEC/2CBJ001270	Electrolytic, TC04-KMA10VB100M
C2	KEC/2CAK005396	Ceramic chip, 0.01 uF
C3	KEC/2CCF001512	Tantalum, 204M3502-105MB
C4	KEC/2CAK005396	Ceramic chip, 0.01 uF
C5	KEC/2CCF001512	Tantalum, 204M3502-105MB
C6	KEC/2CBJ001288	Electrolytic, TC04-KMA25VB47M
C7	KEC/2CAK005115	Ceramic chip, RH 22P
C8	KEC/2CAK005115	Ceramic chip, CH 10P
C9		Tantalum, 204M3502-106MB
C10	KEC/2CCF001512	Tantalum, 204M3502-105MB
C11 thru C20	KEC/2CAK005396	Ceramic chip, 0.01 uF
C21	KEC/2CCF001553	Tantalum, 204M3502-106MB
C22	KEC/2CAK005388	Ceramic chip, 0.001 uF
C24		Film, ECQ-V1H104JZ9
C25	KEC/2CCF001553	Tantalum, 204L3502-106MB
C26	KEC/2CAK005396	Ceramic chip, 0.01 uF
C27	KEC/2CDC001125	Film, ECQ-V1H473JZ9
C28	KEC/2CAK005396	Ceramic chip, 0.01 uF
C29	KEC/2CAK005255	Ceramic chip, RH 100 PF
C30	KEC/2CAK005230	Ceramic chip, RH 47 PF
C31	KEC/2CAK005289	Ceramic chip, RH 270 PF
C32		Tantalum, 204M3502-106MB
C35 and C36	KEC/2CAK005388	Ceramic chip, 0.001 uF
C37		Film, ECQ-V1H333JZ9
C38	KEC/2CDC001018	Film, ECQ-V1H104JZ9
C39	KEC/2CCF004102	Tantalum, TESVA1A105M1-8R
		- - - - - - - - - - DIODES - - - - - - - - - -
CR1	KEC/2QBE005016	Silicon, DAN202K
CR2	KEC/2QBB001737	Zener, HZ-7B1
CR3 thru CR7	KEC/2QBE005032	Silicon, DA204K
CR8 and CR9	KEC/2QBA006166	Silicon, 1S2075K
CR10	KEC/2QBA001142	Silicon, 1SS97
CR11	KEC/2QBA006166	Silicon, 1S2075K
		- - - - - - - - - - JACKS - - - - - - - - - -
J1	KEC/2PDA012021	IL-S-10P-S2T2-EF
J2	KEC/2PDA012013	IL-S-8P-S2T2-EF
J3 and J4	KEC/2PDA012039	IL-S-13P-S2T2-EF
J5	KEC/2PDA012013	IL-S-8P-S2T2-EF
JP1	KEC/2PDD003779	PS-3PF-S4T1-PKL1
		- - - - - - - - - - PLUGS - - - - - - - - - -
P1	KEC/2PDE002051	PS-2SH4-1
		- - - - - - - - - - TRANSISTORS - - - - - - - - -
Q1 and Q2	KEC/2QAD001034	Silicon, 2SC2462LCTL
Q3	KEC/2QAD001026	Silicon, 2SA1121SBTL
Q5 and Q6	KEC/2QAD001026	Silicon, 2SC1121SBTL
Q7 thru Q11	KEC/2QAD001034	Silicon, 2SC2462LCTL
Q12	KEC/2QAD001026	Silicon, 2SC1121SBTL
Q13	KEC/2QAD001034	Silicon, 2SC2462LCTL
Q14	KEC/2QAD001026	Silicon, 2SA1121SBTL
Q15	KEC/2QAD001034	Silicon, 2SC2462LCTL
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1 thru R5	KEC/2RGC001270	Square chip, 1/8W, 47K ohm
R6	KEC/2RGC001247	Square chip, 1/8W, 22K ohm
R7	KEC/2RGC001304	Square chip, 1/8W, 100K ohm
R8	KEC/2RGC001270	Square chip, 1/8W, 47K ohm
R9	KEC/2RGC001213	Square chip, 1/8W, 10K ohm
R10	KEC/2RGC001270	Square chip, 1/8W, 47K ohm
R11 thru R15	KEC/2RGC001114	Square chip, 1/8W, 220 ohm
R16 thru R19	KEC/2RGC001213	Square chip, 1/8W, 10K ohm
R20	KEC/2RGC001114	Square chip, 1/8W, 220 ohm
R21 thru R27	KEC/2RGC001098	Square chip, 1/8W, 100 ohm
R28	KEC/2RGC001270	Square chip, 1/8W, 47K ohm
R29	KEC/2RGC001171	Square chip, 1/8W, 2.2K ohm
R30	KEC/2RGC001254	Square chip, 1/8W, 33K ohm
R31	KEC/2RGC001213	Square chip, 1/8W, 10K ohm
R32	KEC/2RGC001171	Square chip, 1/8W, 2.2K ohm
R33 thru R36	KEC/2RGC001213	Square chip, 1/8W, 10K ohm
R38 and R39	KEC/2RGC001270	Square chip, 1/8W, 47K ohm
R40	KEC/2RGC001247	Square chip, 1/8W, 22K ohm
R41 and R42	KEC/2RGC001270	Square chip, 1/8W, 47K ohm
R43	KEC/2RGC001247	Square chip, 1/8W, 22K ohm
R44	KEC/2RGC001270	Square chip, 1/8W, 47K ohm
R45	KEC/2RGC001247	Square chip, 1/8W, 22K ohm
R46 and R47	KEC/2RGC001270	Square chip, 1/8W, 47K ohm
R48	KEC/2RGC001213	Square chip, 1/8W, 10K ohm
R49	KEC/2RGC001270	Square chip, 1/8W, 47K ohm
R50	KEC/2RGC001304	Square chip, 1/8W, 100K ohm
R51	KEC/2RGC001254	Square chip, 1/8W, 33K ohm
R52	KEC/2RGC001213	Square chip, 1/8W, 10K ohm
R53	KEC/2RGC001379	Square chip, 1/8W, 680K ohm
R54	KEC/2RGC001155	Square chip, 1/8W, 1K ohm
R55 and R56	KEC/2RGC001189	Square chip, 1/8W, 3.3K ohm
R57	KEC/2RGC001163	Square chip, 1/8W, 1.5K ohm
R58	KEC/2RGC001197	Square chip, 1/8W, 4.7K ohm
R59	KEC/2RGC001346	Square chip, 1/8W, 470K ohm
R60 and R61	KEC/2RGC001254	Square chip, 1/8W, 33K ohm
R62	KEC/2RGC001221	Square chip, 1/8W, 15K ohm
R63	KEC/2RGC001197	Square chip, 1/8W, 4.7K ohm
R64	KEC/2RGC001304	Square chip, 1/8W, 100K ohm
R65	KEC/2RGC001171	Square chip, 1/8W, 2.2K ohm
R66	KEC/2RGC001130	Square chip, 1/8W, 470 ohm
R67 thru R70	KEC/2RGC001213	Square chip, 1/8W, 10K ohm
R71 and R72	KEC/2RGC001098	Square chip, 1/8W, 100 ohm
R73 and R74	KEC/2RGC001189	Square chip, 1/8W, 3.3K ohm
R75	KEC/2RGC001254	Square chip, 1/8W, 33K ohm
R76	KEC/2RGC001270	Square chip, 1/8W, 47K ohm
R77	KEC/2RGC001155	Square chip, 1/8W, 1K ohm
R78	KEC/2RGC001247	Square chip, 1/8W, 22K ohm
R79	KEC/2RGC001098	Square chip, 1/8W, 100 ohm
R80	KEC/2RGC001189	Square chip, 1/8W, 3.3K ohm
R81 and R82	KEC/2RGC001213	Square chip, 1/8W, 10K ohm
R83	KEC/2RGC001189	Square chip, 1/8W, 3.3K ohm
R84	KEC/2RGC001304	Square chip, 1/8W, 100K ohm
R85	KEC/2RGC001213	Square chip, 1/8W, 10K ohm
		- - - - - - - - - VOLTAGE REGULATORS - - - - - - -
VR1	KEC/2RFB017055	Variable, RGS6-FAN, 5K ohm
VR3 and VR4	KEC/2RFB017071	Variable, RGS6-FAN, 50K ohm
VR5 thru VR9	KEC/2RFB017063	Variable, RGS6-FAN, 10K ohm
		- - - - - - - - - - - - ALAY - - - - - - - - - -
RA1 and RA2	KEC/2REA020111	EXB-P88-473K
		- - - - - - - - - - - - IC SOCKET - - - - - - - - - -
XA3	KEC/2PDH001241	IC03T-2806S4
XA4	KEC/2PDH001282	IC03T-2406S4
		- - - - - - - - - - CRYSTALS - - - - - - - - - -
Y1	KEC/2YAA181632	8.192 MHz, A4WX01366
		- - - - - - - - - - - - DUMPER - - - - - - - - - -
ZY1	KEC/2YYZ001062	NB-0252-0.5t

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

ADDENDUM NO 1 TO LBI-31616
(PCCM)

This addendum provides a revised schematic diagram and parts list for this publication.

C23: KEC/2CCF001512 tantalum 204M3502-105MB
and
C24
C27: KEC/2CCF001512 tantalum 204M3502-105MB
C40: KEC/2CAJ023094 ceramic chip, 1000pF
CR12: KEC/2QBE005024 silicon DAP202KT
Q16: KEC/2QAD005027 silicon
R56: KEC/2RGC001304 square chip, 1/8W, 100K ohms
R57: KEC/2RGC001213 square chip, 1/8W, 10K ohms
R75: KEC/2RGC001205 square chip, 1/8W, 6.8K ohms
R83: KEC/2RAA002141 carbon film, 1/4W, 3.3K ohms
R84: KEC/2RAA002448 carbon film, 1/4W, 100K ohms
R85: NO PART NUMBER AVAILABLE 1/8W, 12K ohms
R86: KEC/2RGC001212 square chip, 1/8W, 10K ohms
R87: KEC/2RGC002265 carbon film, 1/4W, 10K ohms
R90: KEC/2RGC001221 square chip, 1/4W, 15K ohms
R91: KEC/2RGC001304 square chip, 1/8W, 100K ohms
R92: KEC/2RAA002414 carbon film, 1/4W, 68K ohms
R93: KEC/2RAA002182 carbon film, 1/4W, 4.7K ohms
R94: KEC/2RGC001213 square chip, 1/8W, 10k ohms

SCHEMATIC DIAGRAM
CMX LOGIC
A3WE03575 – 11