



GE Mobile Communications

RANGR™
29-50 MHz



INCLUDES

SERVICE SECTION LBI-31713D
BOARD ASSEMBLIES LBI-31714D

LBI

3 1 6 1 9

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FCC FILING NUMBER	AXA9HHTR-138-A	29-42 MHz	60W
	139-A	29-42 MHz	110W
	138-B	35-50 MHz	60W
	139-B	35-50 MHz	110W

WARNING

Although the highest DC voltage in Mobile Two-Way Radio equipment is supplied by the vehicle battery, high currents may be drawn under short circuit conditions. These currents can possibly heat objects such as tools, rings, watchbands, etc., enough to cause burns. Be careful when working near energized circuits!

High-level RF energy in the transmitter Power Amplifier assembly can cause RF burns upon contact. Keep away from these circuits when the transmitter is energized!

SYSTEM SPECIFICATIONS

FREQUENCY RANGE	29 to 42 MHz and 35 to 50 MHz
BATTERY DRAIN	
Receive	
Squelched	0.7 Amperes at 13.8 Volts
Unsquelched	2.2 Amperes at 13.8 Volts
Transmit	
60 Watts	15 Amperes at 13.6 Volts
110 Watts	29.5 Amperes at 13.4 Volts
FREQUENCY STABILITY	0.0005%
TEMPERATURE RANGE	-30°C (-22°F) to +60°C (140°F)
DUTY CYCLE	100% Receive, 20% Transmit (EIA)
DIMENSIONS, LESS ACCESSORIES (H x W x D)	67 mm x 240 mm x 339 mm (2.6 x 9.5 x 13.3 inches)
WEIGHT, LESS ACCESSORIES	4.3 kg (9.5 pounds)
TRANSMITTER	
TRANSMIT OUTPUT POWER	60W/110W
CONDUCTED SPURIOUS	-80 dB
MODULATION	+4.5 kHz
AUDIO SENSITIVITY	55 to 110 millivolts
AUDIO FREQUENCY CHARACTERISTICS	Within +1 dB to -4.5 dB of a 6 dB/octave pre-emphasis from 300 to 3000 Hz per EIA standards. Post-limiter filter per FCC and EIA
DISTORTION	Less than 2% (1000 Hz) Less than 5% (300 to 3000 Hz)
DEVIATION SYMMETRY	0.3 kHz maximum
MAXIMUM FREQUENCY SEPARATION	29-42 MHz 13 MHz 35-50 MHz 15 MHz
MICROPHONE LOAD IMPEDANCE	600 ohms
POWER ADJUST RANGE	100% to 50% of rated power
RF OUTPUT IMPEDANCE	50 ohms
FM NOISE	-60 dB
CARRIER ATTACK TIME	20 milliseconds
AUDIO ATTACK TIME	20 milliseconds

CHANNEL GUARD TX TONE DISTORTION

5%

RECEIVER

AUDIO OUTPUT (to 4.0 ohm speaker)	10 Watts with less than 3% distortion
SENSITIVITY 12 dB SINAD (EIA Method)	0.35 μ V
SELECTIVITY EIA Two-Signal Method (20 kHz channels)	-90 dB
SPURIOUS RESPONSE	-85 dB
INTERMODULATION 20 kHz	-80 dB
MODULATION ACCEPTANCE	+7.0 kHz
MAXIMUM FREQUENCY SEPARATION	29-42 MHz 13 MHz 35-50 MHz 15 MHz
FREQUENCY RESPONSE	Within +2 and -8 dB of a standard 6 dB per octave de-emphasis curve from 300 to 3000 Hz (1000 Hz reference)
RF INPUT IMPEDANCE	50 ohms
HUM/NOISE RATIO UNSQUELCHED SQUELCHED	-50 dB -70 dB
RECEIVER RECOVERY TIME	200 milliseconds
RECEIVER ATTACK TIME	150 milliseconds
CHANNEL SPACING	20 KHz

* These specifications are intended primarily for use of the serviceman.
Refer to the appropriate Specifications Sheet for the complete specifications.

LBI-3619D

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter" which is stamped on the label containing the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for descriptions of parts affected by these revisions.

Rev. A - LB Radio 19C852050P5-P8

To improve spurious response and adjacent channel intermodulation, a notch filter consisting of the components below was added in the input circuit of the Pulse Amplifier (TRI) on the Noise Blanker Board.

270 pF capacitor (B19/5CAAD00883)
27 pF capacitor (B19/5CAAD00793)
RF coil (B19/6LALD00050)
RF coil (B19/6LALD00049)

Rev. B - LB Radio 19C852050P5-P8

To improve intermodulation characteristics measured at a distance of two to four MHz from receiving frequency, an Automatic Gain Control (AGC) consisting of the components below was added in the Pulse Amplifier/Limiter (IC₁) on the Noise Blanker Board.

4700 pF capacitor (B19/5CAAD00957)
0.047 μ F capacitor (B19/5CAAD01092)
47 ohms resistor (B19/5REAC01722)
1K ohms resistor (B19/5RDAC02446)
47K ohms resistor (B19/5RDAC02439)
100K ohms resistor (B19/5RDAC02449)
Transistor MTM3904 (B19/5TCAB01234)
Transistor MTM3906 (B19/5TCAB01233)

Rev. A - RANGR LB RADIO 19C852050P1-P4

Rev. C - RANGR LB RADIO 19C852050P5-P8

SYSTEM CONTROL BOARD B19/CMC383

To eliminate S550 scan noise in speaker with radio squelched a capacitor C754 was added from SQ DSBL (J701-1) to ground

C754 - B19/5CAAD01237; Ceramic, 0.1 μ F $\pm$ 10%, 25 VDCW

DESCRIPTION

General Electric synthesized RANGR mobile radio combinations are completely solidstate utilizing micro-computer technology and integrated circuits to provide high-quality, high-reliability radios. Standard combinations may

- Microcomputer Controlled Frequency Synthesizer
- Up to 16 channels
- .0005% frequency stability
- Other structured options

The radio locks when the optional lock is installed but is not tamperproof. The cover can be removed in the locked or unlocked position.

The radio set is housed in a weather-resistant case only 6.7 centimeters high. The radio is secured to the vehicle by a bottom mounting plate. When unlocked, the radio may be pulled out of the mounting plate or the top cover removed for servicing.

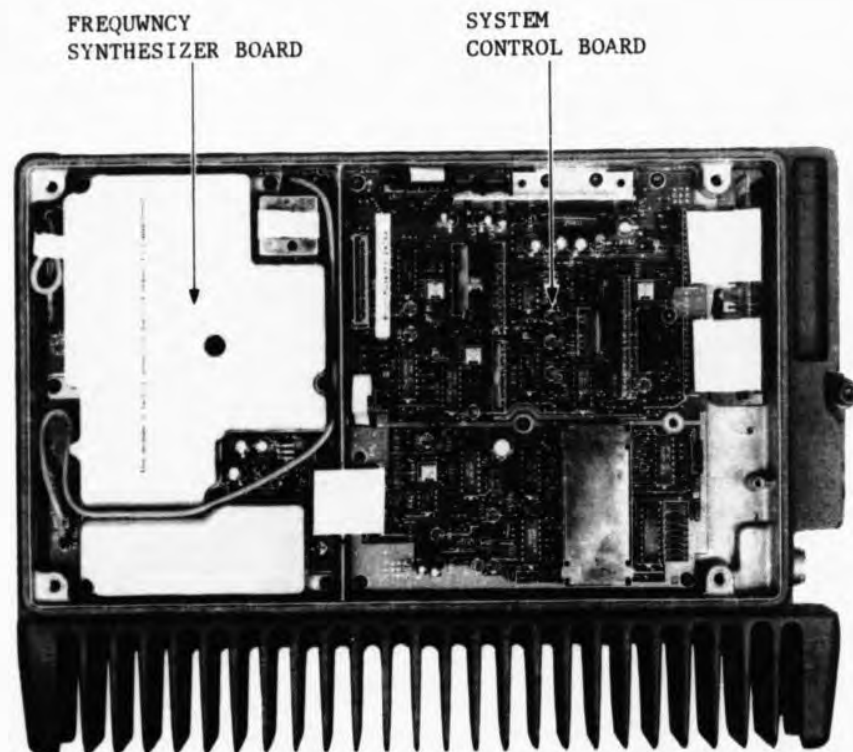
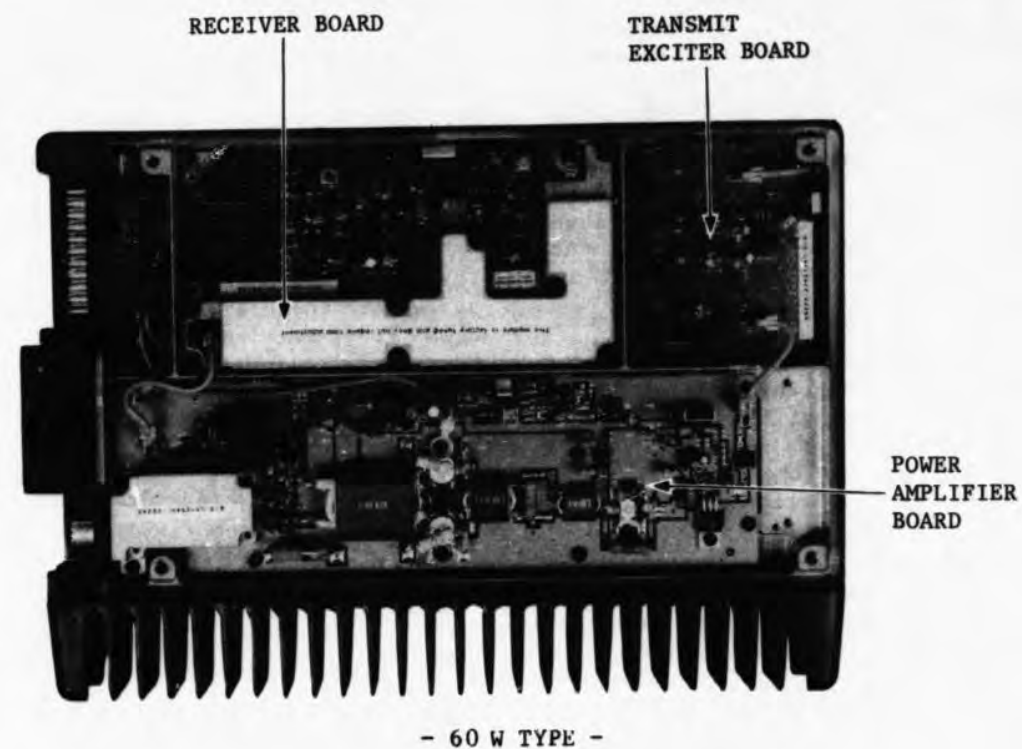
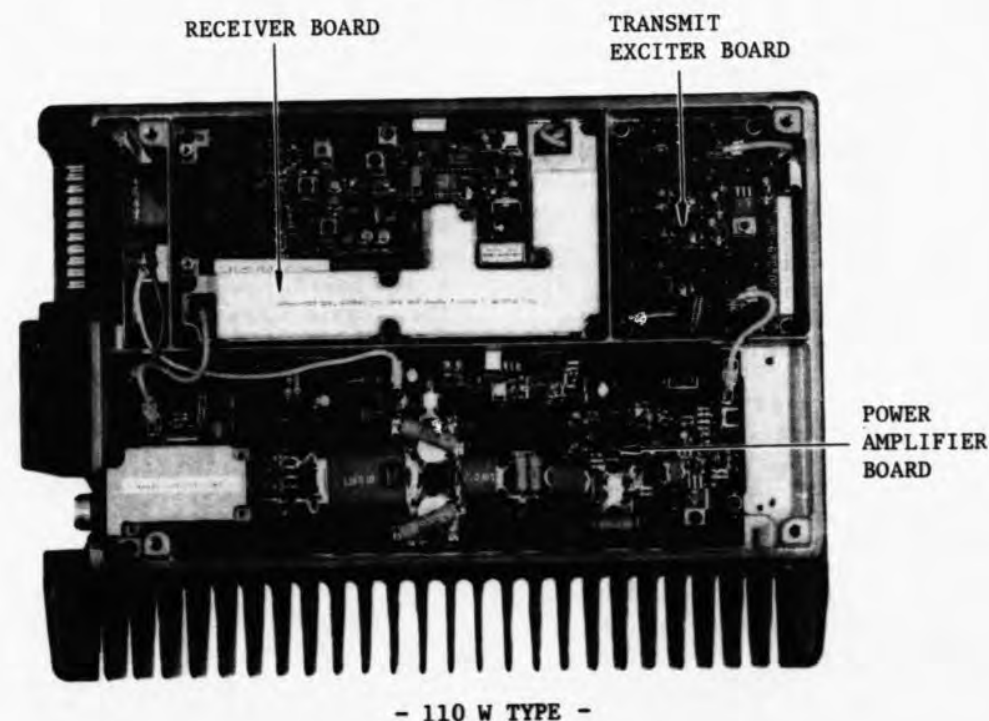


Figure 1. Typical Module Layout (Top View)



- 60 W TYPE -



- 110 W TYPE -

Figure 2. Typical Module Layout (Bottom View)

The basic radio consists of five printed wiring boards mounted in a cast aluminum frame. The five boards are the System Control board, the Frequency Synthesizer board, the Transmit Exciter board, the Power Amplifier board, and the Receiver board.

The radio is of double-layer construction with tuning adjustments easily accessible from the top of the radio.

The System Control board and the Frequency Synthesizer board are located on the top of the radio, while the Transmit Exciter board, the Power Amplifier board and the Receiver board are located on the bottom.

Interconnections are provided by ribbon cable between the boards. A power bus connects A+ and A- from the front connector to the PA assembly.

A centralized metering jack for the transmitter, receiver and system functions is provided for simplified alignment and troubleshooting.

SYNTHESIZER/INTERCONNECT

The synthesizer consists of a microcomputer, electrically-erasable PROM (EEPROM), a frequency synthesizer IC, transmit and receive VCO's and associated circuitry. The frequency synthesizer under control of the microcomputer generates all transmit and receive RF frequencies.

The EEPROM stores binary data for all RF frequencies, Channel Guard tones/digital codes, and the timing function of the carrier control timer(CCT). The microcomputer accesses the EEPROM and provides the correct WALSH bits to the Channel Guard circuitry to generate the correct Channel Guard tone or digital code on a per-channel basis.

PROGRAMMING

The EEPROM allows the radio to be programmed or reprogrammed as needed to adapt to changing system requirements. RF frequencies, Channel Guard tones and digital codes, and the CCT function can be reprogrammed.

The EEPROM can be reprogrammed through the radio front connector using the General Electric Universal PROM Programmer Model TQ2310. This programmer allows all information to be loaded simultaneously.

NOTE

When programming, remember that all RF frequencies must be divisible by 5 kHz. Also insure that P706 is connected to J706-2 and 3 to enable programming.

Programming instructions are provided in the respective Programmer Maintenance Manuals.

TRANSMITTER

The transmitter consists of the exciter, frequency synthesizer, transmit VCO, and a power amplifier (PA) assembly. The PA assembly consists of a PA board mounted along the side of the radio next to the heat sink assembly. The PA board also contains an antenna relay and a low-pass filter.

Audio and Channel Guard circuitry for the transmitter is located on the System Control board.

RECEIVER

The receiver consists of the frequency synthesizer, RX VCO, injection amplifiers, front end, IF, and limiter detector. Audio, squelch and Channel Guard circuitry for the receiver is located on the System Control board.

SYSTEM CONTROL FUNCTION

A microprocessor on the System Control board controls the frequency synthesizer, the TX on/off, the decoding of CTCSS tones, the generation of CTCSS tones, etc. The audio processor circuitry for the transmitter and the receiver are located on the System Control board. Squelch circuitry, a jack for central metering and the digital voice guard circuit are also located on the System Control board.

CONTROL UNITS

S-series control units are available and may be used directly with RANGR radio combinations.

Refer to the applicable Maintenance Manual for detailed description of the Control Unit used with the RANGR radio combinations.

OPERATION

Complete operating instructions for the Two-Way Radio are provided in the Operator's Manual for the control unit used.

MAINTENANCE

The use of microcomputer technology allows self-diagnostic maintenance routines to be incorporated in the microcomputer software. These routines are easy to run and provide a quick analysis of microcomputer and frequency synthesizer operation.

The service section of this manual contains the diagnostic routines and other maintenance information to service this radio. The service section includes:

- System interconnections
- Mechanical layout
- Disassembly procedures
- Replacement of IC's, chip capacitors and resistors
- Microcomputer self diagnostics
- Alignment procedures for the transmitter and receiver
- Troubleshooting Procedure and waveforms

GE Mobile Communications

General Electric Company
Lynchburg, Virginia 24502



MAINTENANCE MANUAL

29-42 MHz & 35-50 MHz SYNTHESIZED RANGE

TWO WAY FM RADIO

SERVICE SECTION

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DESCRIPTION

This section contains the information required to service the radio. Included are disassembly procedures, and procedures for replacing transistors, Integrated Circuits (IC's) and chip components. This section also includes alignment procedures and troubleshooting information (see Table of Contents).

INITIAL ADJUSTMENT

After the radio has been installed (as described in the Installation Manual), the following adjustments should be made by a certified electronics technician.

TRANSMITTER ADJUSTMENT

The adjustment for the transmitter includes measuring the forward and reflected power, and setting the transmitter to rated power output. Then, measure the frequency and modulation and record these measurements for future reference. For the complete transmitter adjustment, refer to the Alignment Procedure (see Table of Contents).

RECEIVER ADJUSTMENT

No adjustment for the input circuit is required. For complete receiver adjustment, refer to the Receiver Alignment Procedure (see Table of Contents).

MAINTENANCE

PREVENTIVE MAINTENANCE

To facilitate troubleshooting of problems on the printed circuit board assemblies, the following service accessories are available:

DESCRIPTION	PART NUMBER
EXTENSION CABLE 22 CONDUCTOR	B19/6JJFD00057
EXTENSION CABLE 10 CONDUCTOR	B19/6JJFD00058
EXTENSION CABLE 10 CONDUCTOR	B19/6JJFD00059
EXTENSION CABLE 4 CONDUCTOR	B19/6JJFD00060
EXTENSION CABLE 6 CONDUCTOR	B19/6JJFD00061
COAXIAL CABLE	B19/6JJFD00062
COAXIAL CABLE	B19/6JJFD00063
TUNING TOOL	B19/MPTC00448

To ensure high operating efficiency and to prevent mechanical and electrical failures from interrupting system operations, routine checks should be made of all mechanical and electrical parts at regular intervals. This preventive maintenance should include the checks as listed in Table 1 Maintenance Checks.

PA TRANSISTOR REPLACEMENT

WARNING

The RF Power Transistors used in the transmitter contain Beryllium Oxide, a TOXIC substance. If the ceramic or other encapsulation is opened, crushed, broken or abraded, the dust may be hazardous if inhaled. Use care in replacing transistors of this type.

To replace the PA RF transistors:

1. Unsolder one lead at a time with a 50 watt soldering iron. Use a scribe or X-acto® knife to hold the lead away from the printed circuit board until the solder cools. Remove the mounting screws.
2. Lift out the transistor. Remove any old solder from the printed circuit board with a vacuum desoldering tool. Special care should be taken to prevent damage to the printed circuit board runs because part of the matching network is included in the base and collector runs.
3. Trim the new transistor leads (if required) to the lead length of the removed transistor.
4. Apply a coat of silicone grease to the transistor mounting surface. Place the transistor in the mounting hole. Align the leads as shown on the Outline Diagram. Then replace the transistor mounting screws using moderate torque (9.4 kg.cm).
5. Solder the leads to the printed circuit pattern. Start at the inner edge of mounting hole and solder the remaining length of transistor lead to the board. Take care not to use excessive heat that causes the printed wire board runs

to separate from the board. Check for shorts and solder bridges before applying power.

CAUTION

Failure to solder the transistor leads as directed may result in the generation of RF loops that could damage the transistor or may cause low power output.

REMOVING IC's

Removing IC's (and most other soldered-in components) can be easily accomplished by using a vacuum desoldering tool. To remove an IC, heat each lead separately on the solder side and remove the old solder with the desoldering tool.

CAUTION



The CMOS Integrated Circuit devices used in this equipment can be destroyed by static discharges. Before handling one of these devices, the serviceman should discharge himself by touching the case of a bench test instrument that has a 3-prong power cord connected to an outlet with a known good earth ground. When soldering or desoldering a CMOS device, the soldering iron should also have a 3-prong power cord connected to an outlet with a known good earth ground. A battery-operated soldering iron may be used in place of the regular soldering iron.

REPLACING CHIP COMPONENTS

Replacement of chip components should always be done with a temperature-controlled soldering iron at 700°F (371°C). However, do not touch the black metal film of the resistors or the ceramic body of capacitors with the soldering iron.

NOTE

The metalized end terminations of the parts may be touched with the soldering iron without causing damage.

REMOVING CHIP COMPONENTS

1. Using two soldering irons heat both ends of the chip at the same time until solder flows, and then remove and discard the chip.
2. Remove excess solder with a vacuum solder extractor.
3. Carefully remove the epoxy adhesive and excess flux to prevent damage to the printed board.

REPLACING CHIP COMPONENTS

1. Using as little solder as possible, "tin" one end of the component and one of the pads on the printed wiring board.

2. Place the "tinned" end of the component on the "tinned" pad on the board and simultaneously touch the component and the pad with a well "tinned" soldering iron while pressing the component down on the board.

3. Place the "tinned" soldering iron on the other end of the component and the pad simultaneously. Apply solder to the top of the end of the component until the solder starts to flow. Use as little solder as possible while getting a good joint.
4. After the component has cooled, remove all flux from the component and printed wiring board area with alcohol.

TEST AND TROUBLESHOOTING PROCEDURES

Maintenance of the radio is facilitated by using the Self Test and Diagnostics routines and servicing techniques unique to this radio. Typical voltage readings are provided on the Schematic Diagram for reference when troubleshooting.

CAUTION

Before bench testing the radio, be sure of the output voltage characteristics of your bench power supply.

To protect the transmitter power output transistors from possible instant destruction, the following input voltages must not be exceeded:

Transmitter unkeyed:	16.5 Volts
Transmitter keyed (50 ohms resistive load):	16.3 Volts
Transmitter keyed (no load or non-resistive load):	14 Volts

These voltages are specified at the normal vehicle battery terminals of the radio and take the voltage drop of standard cables into account. The voltage limits shown for a non-optimum load is for "worst case" conditions. For antenna mismatches likely to be encountered in practice, the actual limit will approach the 16.3 Volt figure.

Routine transmitter tests should be performed at EIA Standard Test Voltages (13.6 VDC for loads of 6 to 16 amperes; 13.4 VDC for loads of 16 to 36 amperes). Input voltages must not exceed the limits shown, even for transient peaks of short duration.

Many commonly used bench power supplies cannot meet these requirements for load regulation and transient voltage suppression. Bench supplies which employ "brute force" regulation and filtering (such as Lapp Model 73) may be usable when operated in parallel with a 12 Volt automotive storage battery.

MICROCOMPUTER

When servicing the microcomputer/synthesizer circuitry it is sometimes desirable to force the microcomputer into specific operating modes. Following are tips that allow you to initiate these modes.

- Ground the lock-detect line at IC701-8 to force the microcomputer to continually try to reload the synthesizer. This mode will enable you to check the serial data, clock, channel change pulse and enable signals to the synthesizer.
- To stop the microcomputer from running, disable the watchdog timer by shorting the collector and emitter of TR701, and ground the single-step line at IC702-5.

MICROPHONICS

Synthesized radios tend to be sensitive to shock and vibration, creating microphonics. The construction of the RANGR radio with its die-cast aluminum frame, cast shield, and multiple board-mounting screws, provides a high degree of immunity. When removing printed circuit boards or shields, note the location of all mounting hardware.

When servicing the radio be sure that no solder build-up has occurred on the chassis or shield.

To assure a high degree of resistance to microphonics be sure to replace exactly, all hardware removed.

Be sure that all mounting screws are properly torqued and shields are in place. Refer to the Mechanical Layout Diagram.

NOTE

Loose or rubbing parts, especially in the VCO area are particularly sensitive and can cause microphonics. Again, be certain all hardware is properly installed and torqued.

MICROCOMPUTER DIAGNOSTICS

The microcomputer, in addition to operational programming, contains software for self-diagnostic routines to aid in troubleshooting the radio. Since the radio can not function with a defective microcomputer, the self diagnostic routines include internal tests as well as input/output tests to verify proper operation.

The internal tests include a ROM test which verifies that the proper program is stored in the microcomputer and a RAM test which checks for proper data transfer to and from all memory locations.

The input/output tests include a test which grounds one pin at a time on Port 1 and the data bus, and a test which mirrors the inputs PTT, CG DISABLE, ADVANCE CHANGE, and FB4 - FB1 on to the data bus.

These tests assure proper operation of the ports and data bus, in addition to checking the input/output instructions of the microcomputer. When troubleshooting the radio, if problems are suspected on the system board, the diagnostic routines should be performed first before going on to the test procedures and alignment instructions.

TEST EQUIPMENT REQUIRED

- 13.8 VDC supply, 500 mA (unless being tested in radio)
- DC Voltmeter (Data Tech 30L or equivalent)
- Oscilloscope (Tektronix 404 or equivalent)

TEST PROCEDURE

1. Connect oscilloscope to J801-18 (SPKR 1) and ground.
2. Enter the self-diagnostic mode as follows:

CAUTION

When using the radio with the S550, S950 or S990 control head, the ADVANCE CHANGE line should be disconnected from the control head by removing connector P3. Instead of keying the microphone, ground J606-10.

- Key the radio with the microphone on-hook. (Ground J801-11. Make sure that MONITOR Switch is OFF.)
- Apply A+ at J801-19 through a 10K resistor to J801-32.
- Turn radio on.

ROM AND RAM TESTS

Once power is supplied to the board, the microcomputer will jump to the self-diagnostic test and immediately begin execution of the ROM and RAM tests. Upon completion of the ROM and RAM test (less than a second) the display, data bus, or alert tone will indicate when the tests have been successfully completed. Test status is indicated as follows:

	D3	D2	D1	D0	ALERT TONE
ROM TEST FAILED	0	0	0	0	NONE
ROM TEST PASSED RAM TEST FAILED	0	0	0	1	NONE
ROM TEST PASSED RAM TEST PASSED	0	0	1	0	1 kHz

If the data bus is inaccessible then the alert tone can be used to indicate whether the radio passed the tests. If the tests are successfully completed there will be a 1 kHz tone on SPKR 1 and it will be heard on the speaker if the board is in a radio. If no alert tone is present, then either the ROM or RAM test has failed.

If the radio fails these tests, the microcomputer function is defective. Before replacing the microcomputer, exhaust all other possibilities. Check associated circuits for shorted or open printed wire runs and components.

INPUT/OUTPUT TESTS

If the ROM and RAM tests are completed satisfactorily, release the PTT switch and remove A+ from J801-32. Note that the data bus will still indicate 02 (Hex), however, the 1 kHz tone should no longer be displayed on the scope or heard on the speaker.

The I/O test grounds one pin at a time on Port 1 and the data bus and is stepped through the test sequence by operating the PTT switch (momentarily grounding J801-11). Port 1 and the data bus can be monitored using a voltmeter. Port 1 consists of pins 27-34 on microcomputer IC702. The data bus includes pins 12-19 on IC702. Refer to schematic diagram for data

bus and port identification for IC702.
For example:

P17 = port 1 bit 7.

1. Momentarily press and release the PTT switch (J801-11). Port 1 and data bus lines all will go high.
2. Momentarily press and release the PTT switch (J801-11). IC702-34 and IC702-19 will go low. All other outputs should be high.
3. Momentarily press and release the PTT switch (J801-11). IC702-33 and IC702-18 will go low. All other outputs should be high.
4. Momentarily press and release the PTT switch (J801-11). IC702-17 will go low. All other outputs should be high. Note that IC702-32 will remain high. This is because this output switches the radio into the transmit mode when grounded. Thus the output is bypassed so that the radio will never go into the transmit mode during self test.
5. Momentarily press and release the PTT switch (J801-11). IC702-31 and IC702-16 will go low. All other outputs should be high.
6. Momentarily press and release the PTT switch (J801-11). IC702-30 and IC702-15 will go low. All other outputs should be high.
7. Momentarily press and release the PTT switch (J801-11). IC702-29 and IC702-14 will go low. All other outputs should be high.
8. Momentarily press and release the PTT switch (J801-11). IC702-28 and IC702-13 will go low. All other outputs should be high.
9. Momentarily press and release the PTT switch (J801-11). IC702-27 and IC702-12 will go low. All other outputs should be high.

10. Momentarily press and release the PTT switch (J801-11). Port 1 outputs will all be set high.

NOTE

At this point the program advances to mirror the outputs PTT, CG DISBL, ADVANCE CHANGE, and FB4-FB1 onto the data bus IC702-12 through IC702-19, respectively.

11. Momentarily apply ground to the following points while observing the status of the associated data bus as indicated below. When ground is applied, the data bus should go low and then go high when ground is removed.

Momentarily Ground	Data Bus	Momentarily Ground	Data Bus
J801-30	IC702-18	J801-13	IC702-14
J801-10	IC702-17	J801-2	IC702-13
J801-32	IC702-16	J801-1	IC702-12
J801-4	IC702-15	J801-11	IC702-19

12. Exit the diagnostic routines by momentarily removing power from the radio.

TEST FREQUENCIES

If the EEPROM is not custom programmed to the customer specified personality, then a standard test program is provided. The EEPROM is programmed on several channels including tone and digital Channel Guard and carrier control timer. The test program is given in Table 3.

FREQ SPLIT	CHANNEL	TX Frequency RX Frequency (MHz)	Channel Guard	Carrier control Timer
29 - 42 MHz	1	29.025 29.075	71.9 Hz	
	2	32.025 32.075	023	
	3	35.025 35.075		30 sec
	4	38.075 39.025		
	5	41.025 41.975		
35 - 50 MHz	1	35.025 35.075	71.9 Hz	
	2	38.075 39.025	023	
	3	41.025 41.075		30 sec
	4	45.025 45.075		
	5	49.025 49.075		

TABLE 3 - TEST PROGRAM

PA TROUBLESHOOTING PROCEDURE

DC VOLTAGE CHECK

First, Check the meter readings for power supply voltage and various stabilized DC voltages, at J606. The typical readings for the test positions and test points are given in the chart below. The meter readings are typical using General Electric Test Set 4EX3A11 with Test Set Adapter 19C851532G1.

TEST POSITION	METERING POINT	FUNCTION MEASURED	SCALE	TYPICAL READING
B	J606-3	9V-RX	0-15V	9V
C	J606-4	5V	0-15V	5V
H	J606-8	EX9V	0-15V	9V
I	J606-9	+8V	0-15V	8V
J	J606-11	9V	0-15V	9V
K	J606-12	A+	0-15V	13.6V

TABLE 4 - READINGS AT J606

EXCITER QUICK CHECK

When troubleshooting the transmitter check for typical readings for the DC voltages across Exciter resistor R117, the Synthesizer output (J207), and the Exciter output (J102) as listed in Table 5.

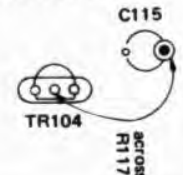
SYMPTOM	PROCEDURE	ANALYSIS
Little or No RF Output	Key transmitter and monitor EXCITER DC voltages across R117 for 0.7 VDC. The voltage should increase. 	If voltage does not increase, check TR101 to TR103 and associated components.
	Disconnect the coaxial cable ZC608 from the synthesizer board and measure TX INJECTION, J207. Should be -3 to +6 dBm.	If TX INJECTION is low, check TR220, TR221 and associated circuitry.
	Disconnect the coaxial cable ZC610 from the Exciter board and measure EXCITER OUTPUT, J102. Should be 0.4 watts or more.	If EXCITER OUTPUT is low, check TR101 to TR104, IC101 and associated components.

TABLE 5 - EXCITER QUICK CHECK

TYPICAL PERFORMANCE INFORMATION

SIGNAL LEVELS

SIGNAL	INDICATION	VOLTAGE LEVEL
CAS	High Level	9.0 VDC
	Low Level	0.15 VDC
RUS	High Level (Rx Un-sq)	9.0 VDC
	Low Level (Rx Squelched)	0.15 VDC
	Low Level (Rx Mute/PTT pulled low, Rx unsquelched)	0.6 VDC
	Logic Low (Sq. Dis)	0 VDC
SQ DSBL, Input	Logic High (Sq)	2.4 VDC
	Rx Un-Sq	0.14 VDC
CCT PA ENBL	Logic Low	0.35 VDC
	Logic High	5.5 VDC
TX ENB	Logic Low	2.0 VDC
	Logic High	9.0 VDC
PTT, Input	Logic Low	0 VDC
	Logic High	13 VDC

TABLE 6 - SIGNAL LEVELS

Front Connector	J801
System Metering	J606
RX RF	J401
RX INJ	J209
TX INJ	J207
EX Output	J102

TABLE 7 RADIO CONNECTOR IDENTIFICATION

TRANSMITTER ALIGNMENT

TEST PROCEDURES

These Test Procedures are designed to assist you in servicing a transmitter that is operating, but not properly. Once a defect is pinpointed, refer to the Transmitter Troubleshooting Procedure. Before starting, be sure that transmitter is tuned and aligned properly.

CAUTION

Before bench testing the radio, be sure of the output voltage characteristics of your bench power supply.

To protect the transmitter power output transistors from possible instant destruction, the following input voltages must not be exceeded:

Transmitter unkeyed:	16.5 Volts
Transmitter keyed (50 ohms resistive load):	16.3 Volts
Transmitter keyed (no load or non-resistive load):	14.0 Volts

These voltages are specified at the normal vehicle battery terminals of the radio and take the voltage drop of standard cables into account. The voltage limits shown for a non-optimum load is for "worst case" conditions. For antenna mismatches likely to be encountered in practice, the actual limit will approach the 16.3 Volt figure.

Routine transmitter tests should be performed at EIA Standard Test Voltages (13.6 VDC for loads of 6 to 16 amperes; 13.4 VDC for loads of 16 to 36 amperes). Input voltages must not exceed the limits shown, even for transient peaks of short duration.

Many commonly used bench power supplies cannot meet these requirements for load regulation and transient voltage suppression. Bench supplies which employ "brute force" regulation and filtering (such as Lapp Model 73) may be usable when operated in parallel with a 12 Volt automotive storage battery.

MODULATION LEVEL ADJUSTMENT

The MOD ADJUST controls are adjusted to the proper setting before shipment and normally do not require readjustment. This setting permits approximately 75% modulation for the average voice level. The audio peaks which would cause overmodulation are clipped by the modulation limiter. The limiter, in conjunction with the de-emphasis network, instantaneously limits the slope of the audio wave to the modulator, thereby preventing over-modulation while preserving intelligibility.

TEST EQUIPMENT

1. An audio oscillator (GE Model 4EX6A10)
2. Deviation Monitor
3. An output meter or a VTVM
4. GE Test Set Model 4EX3A11 with Test Set Adapter Cable 19C851532G1

PROCEDURE OF SYNTHESIZER TRANSMIT DEVIATION

NOTE

The transmit deviation has been properly set by the factory and should require no readjustment. Should it become necessary to adjust the deviation, please refer to the Maintenance Manual LBI-13714 and the section TX AUDIO PROCESSOR in SYSTEM CONTROL BOARD and MODULATION LEVEL CONTROL in FREQUENCY SYNTHESIZER BOARD. These will familiarize you with the modulation deviation and make the Alignment Procedure more understandable.

1. Select a center frequency channel. Remove P605
2. Rotate RV201 and RV603 fully counterclockwise.
3. Apply a 1 kHz tone at 1 Vrms through a 100 μ F capacitor to MIC HI at J701-16 (+ lead of capacitor).

Connect the deviation monitor to the antenna connector J3 via a 30-dB coupler, whose output is terminated in a 50-ohm load. Key the radio.

Set VCO DEVIATION ADJUST, RV202 for ± 3.75 kHz deviation.

4. Set RV603 fully clockwise. Apply a 400 Hz tone to J605-2 and with the radio keyed, vary its amplitude until the Deviation Monitor reads 1 kHz. Note the level.
5. Change the signal generator frequency to 10 Hz at the same level and set REF MOD ADJUST, RV201 for a deviation of 1 kHz. Unkey the radio.
6. Disconnect the signal generator and replace P605 in position 1-2.
7. Select a frequency with Tone Channel Guard (preferably close to the center frequency).

Key the radio and set CG DEVIATION ADJUST, RV603 for a deviation reading of ± 0.75 kHz.

NOTE: If Channel Guard is not used on any frequency, the VCO DEVIATION ADJUST RV202 may be set for a deviation of ± 4.5 kHz instead of ± 3.75 kHz.

AUDIO CHECKS

TEST EQUIPMENT REQUIRED

- Audio Oscillator
- Oscilloscope
- Voltmeter
- Deviation Monitor

AUDIO AC VOLTAGE

1. Connect audio oscillator output across J701-16 (or J801-9) and J701-3 (or J801-5).

		IC607-1	IC607-7
SCOPE SETTING	HORIZONTAL	200 μ SEC/DIV	200 μ SEC/DIV
	VERTICAL	2 VOLTS/DIV	2 VOLTS/DIV
SET AUDIO OSCILLATOR at 1000 Hz WITH OUTPUT OF 1.0 VRMS. MODULATION ADJUSTED FOR 4.5 kHz DEVIATION. NOTE: AN RMS OR PEAK READING VOLTMETER WILL READ 1/2 TO 1/3 OF PEAK-TO-PEAK READINGS.			

AUDIO SENSITIVITY

1. Connect audio oscillator output across J701-16 (or J801-9) and J701-3 (or J801-5). Adjust output for 1000 Hz at 1.0 VRMS.
2. Reduce generator output until deviation falls to 3.0 kHz for radios without Channel Guard or to 2.25 kHz for radios with Channel Guard. Voltage should be less than 120 millivolts.

SYNTHESIZER AND TRANSMITTER ALIGNMENT

TEST EQUIPMENT REQUIRED

1. Wattmeter, 50 ohm (capable of measuring 150 Watts & 1 Watt)
2. DC Voltmeter, 20,000 ohms per volt
3. Digital Voltmeter
4. Power supply, 13.8 VDC regulated
5. GE Test Set 4EX3A11 with Test Set Adapter Cable 19C851532G1

PRELIMINARY CHECKS AND ADJUSTMENTS

NOTE

Refer to Figure 3 for location of tuning and adjustment controls.

1. Apply DC power to radio.
2. Connect plug of GE Test Set to Metering jack J606. Set polarity to "+" and voltage range to the 1 volt position (Test 1).

NOTE

Before alignment or making any adjustments to the transmitter, be sure that power supply voltage (A+) and various stabilized DC voltages are proper. Refer to Table 4.

ALIGNMENT PROCEDURE

- SYNTHESIZER -

STEP	METERING POINT	TUNING CONTROL	METER READING	PROCEDURE
1.	TP201 (Control Voltage Monitor)	CV202	A:6.5 VDC B:7.0 VDC	NOTE The synthesizer is factory aligned and should not require further adjustment. Should it become necessary to adjust the synthesizer please refer to the Maintenance Manual LBI-31714 and the "Frequency Synthesizer" section. These will familiarize you with the operation of the VCO's and make the Alignment Procedure more understandable.
				NOTE The label on the cover of the Synthesizer must be removed, or holes made in it to gain access to the adjustable components, through the existing holes in the shield. These hole locations are shown in Figure 3.
				NOTE Should it become necessary to adjust the synthesizer, program a PROM to the highest frequency of the split (42 MHz for A board or 50 MHz for B board) for proper alignment.
				Select highest frequency transmit channel in the split (42 MHz - A, 50 MHz - B). With a 50 ohm load on the antenna connector J3, key the radio. Adjust CV202 until the lock detector indicator CD710 goes out. Monitor TP201 with a digital voltmeter and adjust CV202 for a reading of 6.5 +0.1 VDC for A board or 7.0 +0.1 VDC for B board. Check that CD710 remains out. Unkey the radio.

STEP	METERING POINT	TUNING CONTROL	METER READING	PROCEDURE
2.	TP201 (Control Voltage Monitor)	CV201	7.5VDC	Select highest receive channel in the split as in Step 1 (release PTT switch). Adjust CV201 until lock detector indicator CD710 goes out. Monitor TP201 with a digital voltmeter and adjust CV201 for a reading of 7.5+0.1VDC. Check that CD710 remains out.
3.	TP201 (Control Voltage Monitor)		3.5 to 7.5VDC	Select each receive and transmit channel. Voltage at TP201 should be between 3.5 and 7.5 VDC.
4.	J207 J209		-3 to +6 dBm	Monitor TX injection at J207 and Rx injection at J209. Tx injection -3 to +6 dBm Rx injection -3 to +6 dBm

- REFERENCE OSCILLATOR FREQUENCY -

STEP	METERING POINT	TUNING CONTROL	METER READING	PROCEDURE
5.	J207	FREQ TRIM Control on VC-TCXO	Channel Operating Frequency	NOTE This step assumes the frequency is measured when the transmitter is first keyed. If delayed, the rapidly rising ambient temperature must be taken into consideration. The oscillator frequency should be set at 25°C ambient temperature. Press the PTT switch while monitoring the Tx injection frequency at J207. Adjust FREQ TRIM Control on VC-TCXO for the assigned channel frequency within +0.5 ppm. Note: The receiver injection frequency will automatically be correct.

- EXCITER -

STEP	METERING POINT	TUNING CONTROL	METER READING	PROCEDURE
				NOTE The Exciter requires no adjustment. If it becomes necessary to check the Exciter, proceed as follows. NOTE The Exciter can be isolated from the rest of the radio for checking purposes, if desired. To isolate and set up for alignment, remove coaxial cables ZC608 and ZC610. Connect a (0-1 watt) wattmeter to J102. Apply a 0 dBm on-frequency signal to J101.
6.				Check output power on the wattmeter. It should be greater than 100 milliwatts. NOTE Disconnect wattmeter from J102. Reinstall Z608 and Z610 if removed. Connect a (0-150 watts) wattmeter set to antenna jack J3.
7.			RV1	Monitor the transmitter output power on each channel. Select the channel with the lowest output power and set RV1 for rated output power.

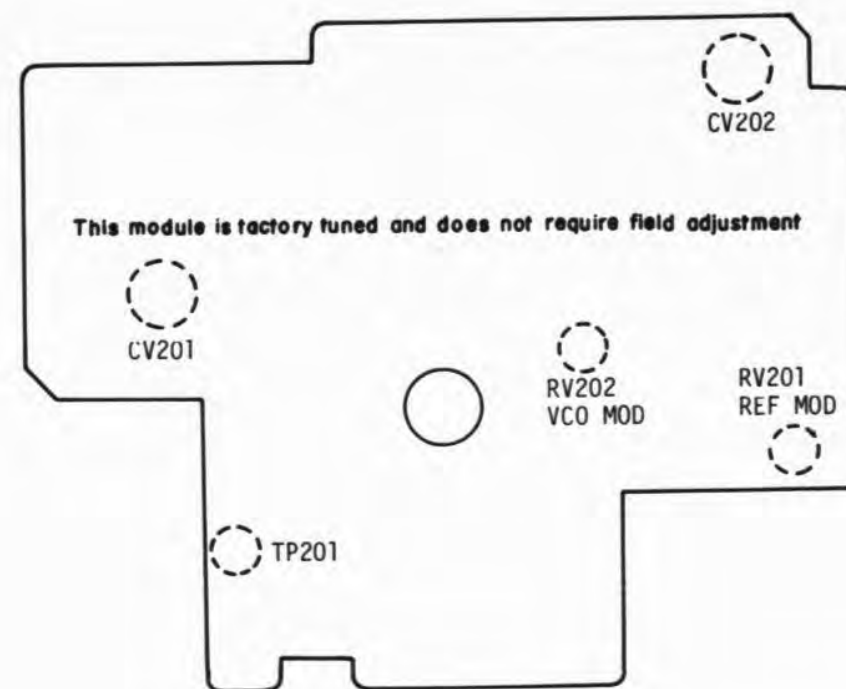


Figure 3 - Hole locations for synthesizer tuning and transmitter deviation adjustment

RECEIVER ALIGNMENT

TEST EQUIPMENT REQUIRED (or Equivalent)

- GE TEST Set 4EX3A11, 4EX8K12, or 20,000 ohms-per-volt multimeter.
- AC Voltmeter
- RF Signal Generator
- Frequency Counter
- 4-ohm 15 watt resistor
- Audio Isolation Transformer (1:1)
19A116736P1 or equivalent

PRELIMINARY CHECKS AND ADJUSTMENTS

NOTE

Before aligning the receiver or making any adjustments to the radio be sure that the output of 9 Volt Regulator is 9.0 ± 0.2 VDC

NOTE

If installing the Noise Blanker option board, cut jumper W402 and plug option board into J502 (be sure plug is installed on J503-2, 3 in receiver unit, and P707 is installed on J707-2, 3 in system control unit). Set the output signal level of the RF signal generator so as to obtain 12 dB SINAD at audio output. Adjust coils L503 and L504 to obtain best SINAD sensitivity reading.

IF/FM DETECTOR ALIGNMENT

Apply a 1000 microvolt, on-frequency test signal modulated by 1,000 Hz with ± 3.0 kHz deviation to antenna jack J3.

Connect a 4-ohm, 15-watt resistor in place of the speaker. Connect the isolation transformer input across the resistor. Connect the isolation transformer output to the Distortion Analyzer (See figure 5).

Adjust the VOLUME control for 5 Watts output (4.47 VRMS) using the Distortion Analyzer as a voltmeter.

Set the output signal level of the RF signal generator so as to obtain 12dB SINAD at audio output.

Adjust coils L503, 504, 506, 507 and 508 to obtain maximum SINAD SENSITIVITY.

Set the output signal level of the RF signal generator to 1000 microvolt.

Adjust L509 for maximum audio output.

Adjust RV602 for audio output level at TP1 of 300 mV rms.

FRONT-END ALIGNMENT

Select the lowest frequency channel. Set the frequency of the RF signal generator to the lowest channel frequency ± 10.4 MHz. ($= f_R + 1/21F$ spurious frequency). Adjust CV401 and CV402 to obtain worst SINAD SENSITIVITY (maximum spurious rejection in this condition).

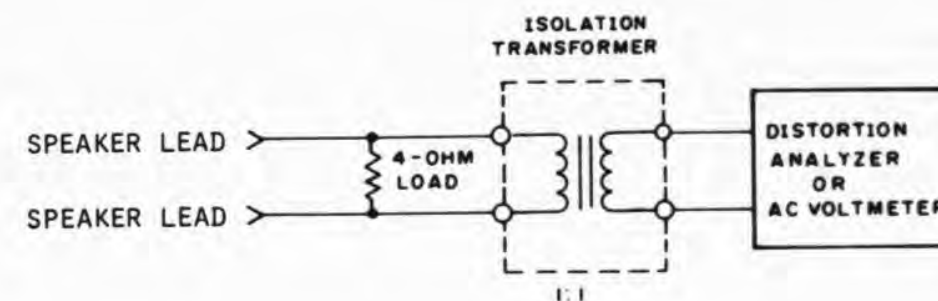


Figure 5 - Audio Isolation Transformer

RV605 ADJUSTMENT PROCEDURE

RV605 is used to set squelch amplifier gain to correct for noise variations between various bands of RANGR. This control does not require adjustment unless the squelch hybrid HC601 is changed or the systems board is exchanged between radios of different frequency bands.

- 1) Connect a signal generator to the antenna connector.
- 2) Set the squelch control on the Control Head fully clockwise.
- 3) Set RV605 on the System Control board fully clockwise.
- 4) Set the signal generator to the level to produce 20dB quieting.
- 5) Raise the generator level by 2dB.
- 6) Set the squelch control on the Control Head fully counterclockwise.
- 7) Adjust RV605 until the squelch just closes.
- 8) Set the modulation frequency to 1kHz with 3kHz deviation.
- 9) Check the signal generator level required to just open the squelch. It should be greater than the 20dB level and less than 1μV.

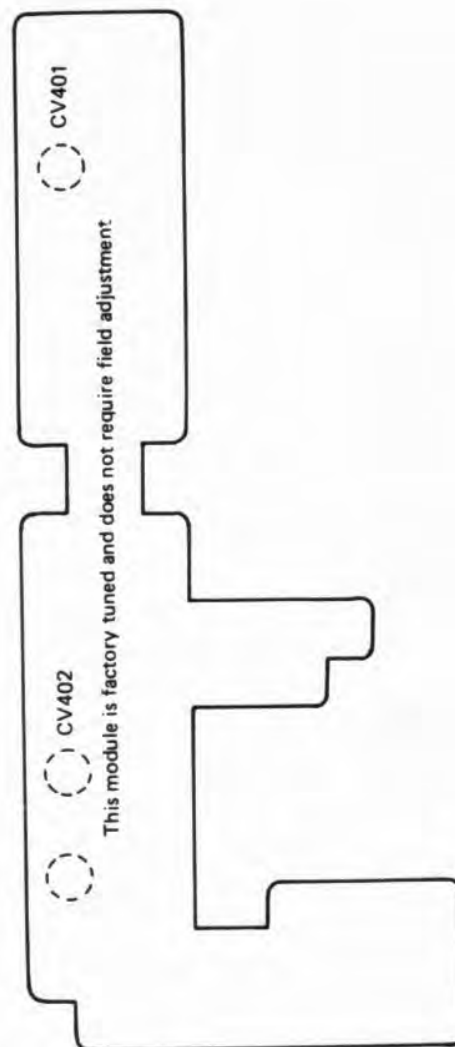


Figure 6 - Hole locations for receiver adjustment

RECEIVER AUDIO AND SQUELCH CHECKS

SQUELCH CIRCUIT TEST WITH 6kHz SIGNAL PRELIMINARY STEPS

1. Set the squelch on the control head to close at 8 dB SINAD level.
2. Quiet receiver with 1000 uV modulated signal applied to antenna jack J3.
3. Set modulation frequency to 6 kHz.
4. Set deviation to 3 kHz.
5. Use 10 megohm probe.

(A)

HOR .1 MSEC/DIV
VERT 0.1 V/DIV
(0.3 ~ 0.6 V P-P)



(B)

HOR .1 MSEC/DIV
VERT 0.1 V/DIV
(0.5 V P-P)



(C)

HOR .1 MSEC/DIV
VERT 2 V/DIV
(7.5 ~ 8.0 VDC)
BASE LINE 0 VDC



SQUELCH CIRCUIT CHECKS WITH NOISE PRELIMINARY STEPS

1. Set the squelch on the control head to close at 8 dB SINAD level.
2. Remove input signal.
3. Use 10 megohm probe.

(A)

HOR .5 MSEC/DIV
VERT 1 V/DIV
(3.5 ~ 4.0V P-P)



(B)

HOR .5 MSEC/DIV
VERT 1 V/DIV
(2 V P-P)



(C)

HOR .5 MSEC/DIV
VERT 2 V/DIV
(7.5 ~ 8.0 VDC)



AUDIO CIRCUIT PRELIMINARY STEPS

1. Apply 1000 uV on frequency signal with 1000 Hz modulation and 3 kHz deviation to antenna jack J3.
2. Output set to 10 Watts (6.3 VRMS) into 4-ohm load.
3. Use 1 megohm probe.

(D)

HOR .5 MSEC/DIV
VERT 50 mV/DIV
(160 mV P-P)



(E)

HOR .5 MSEC/DIV
VERT .2 V/DIV
(.84 V P-P)



(F)

HOR .5 MSEC/DIV
VERT .1 V/DIV
(.28 V P-P)



(G)

HOR .5 MSEC/DIV
VERT .1 V/DIV
(.28 V P-P)



(H)

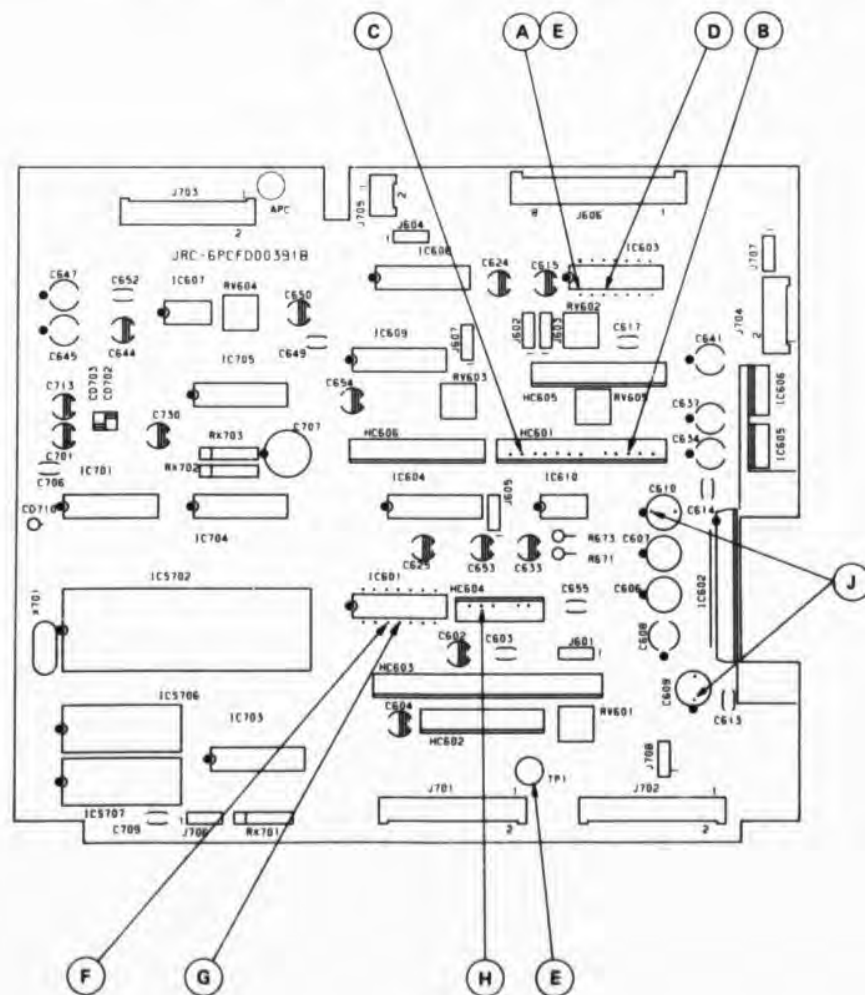
HOR .5 MSEC/DIV
VERT 50 mV/DIV
(280 mV P-P)



(J)

HOR .5 MSEC/DIV
VERT 2 V/DIV
(8.8 V P-P)





STEP 2
USABLE SENSITIVITY
(12 DB SINAD)

TEST PROCEDURE

If STEP 1 checks out properly, measure the receiver sensitivity as follows:

- A. Apply a 1000 microvolt, on-frequency signal modulated by 1000 Hz with 3.0 kHz deviation to J3.
- B. Place the RANGE switch on the Distortion Analyzer in the 200 to 2000 Hz distortion range position (1000 Hz filter in the circuit). Tune the filter for minimum reading or null on the lowest possible scale (100%, 30%, etc.)
- C. Place the RANGE switch to the SET LEVEL position (filter out of the circuit) and adjust the input LEVEL control for a +2 dB reading on a mid range (30%).
- D. Set signal generator output to 0.3 μ V. Switch the RANGE control from SET LEVEL to the distortion range. Readjust Distortion Analyzer SET LEVEL as required until a 12 dB difference (+2 dB to -10 dB) is obtained between the SET LEVEL and distortion range positions (filter out and filter in).
- E. The 12 dB difference (Signal plus Noise and Distortion to noise plus distortion ratio) is the "usable" sensitivity level. The sensitivity should be less than rated 12 dB SINAD specifications with an audio output of at least 5 Watts (4.47 Volts RMS across the 4.0 ohm receiver load using the Distortion Analyzer as a Voltmeter).
- F. Leave all controls as they are and all equipment connected if the Modulation Acceptance Bandwidth test is to be performed.

SERVICE CHECK

If the sensitivity level is more than rated 12 dB SINAD, check the alignment of the IF stages as directed in the Alignment Procedure.

STEP 3
MODULATION ACCEPTANCE
BANDWIDTH (IF BANDWIDTH)

TEST PROCEDURE

If STEPS 1 and 2 check out properly, measure the bandwidth as follows:

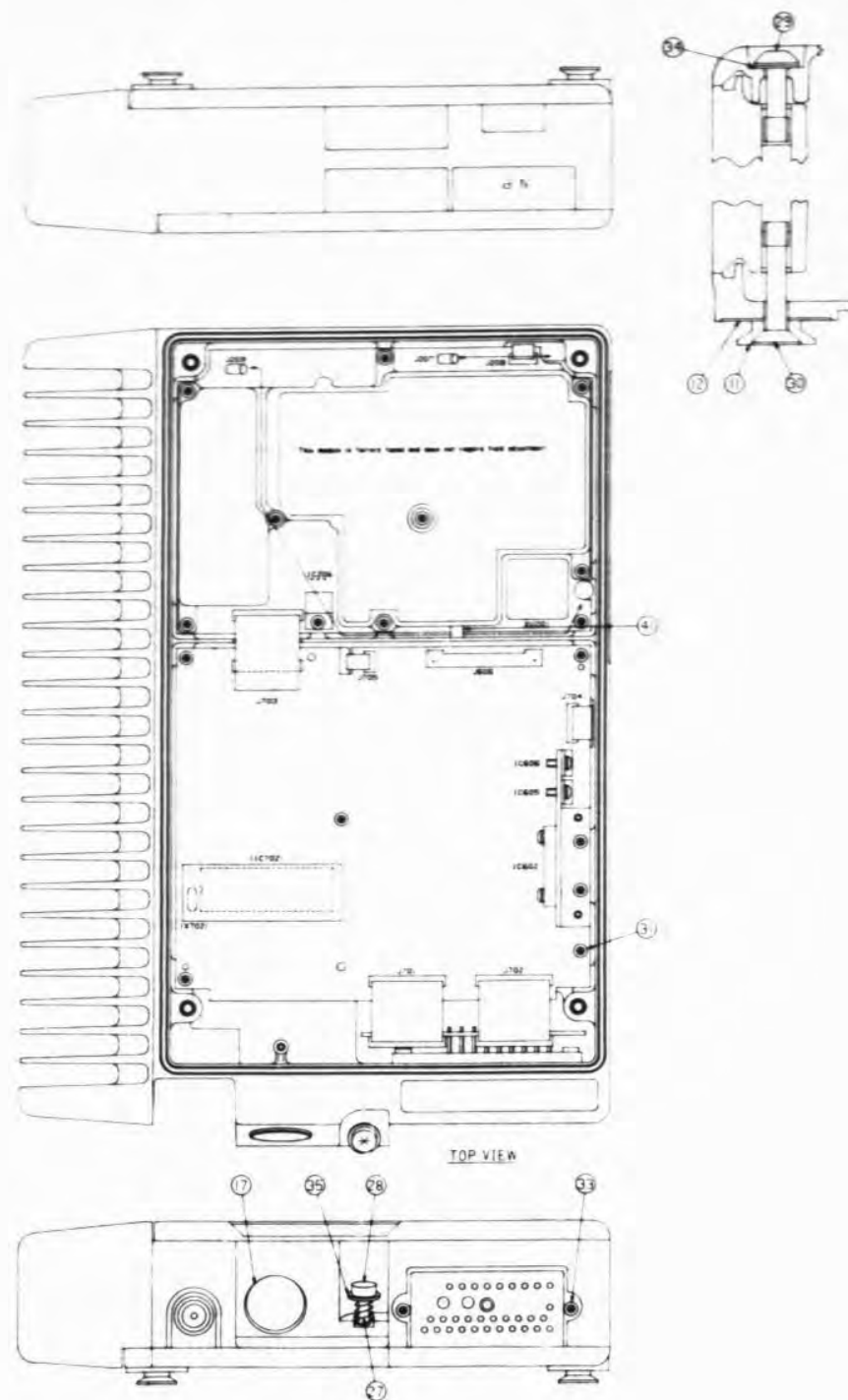
- A. Reduce audio output level to 10% of rated output.
- B. Set the Signal Generator output for twice the microvolt reading obtained in the 12 dB SINAD measurement.
- C. Set the RANGE control on the Distortion Analyzer to the SET LEVEL position (1000 Hz filter out of the circuit), and adjust the input LEVEL control for a +2 dB reading on the 30% range.
- D. While increasing the deviation of the Signal Generator, switch the RANGE control from SET LEVEL to distortion range until a 12 dB difference is obtained between the SET LEVEL and distortion range readings (from +2 dB to -10 dB).
- E. The deviation control reading for the 12 dB difference is the Modulation Acceptance Bandwidth of the receiver. It should be more than +7.0 kHz.

SERVICE CHECK

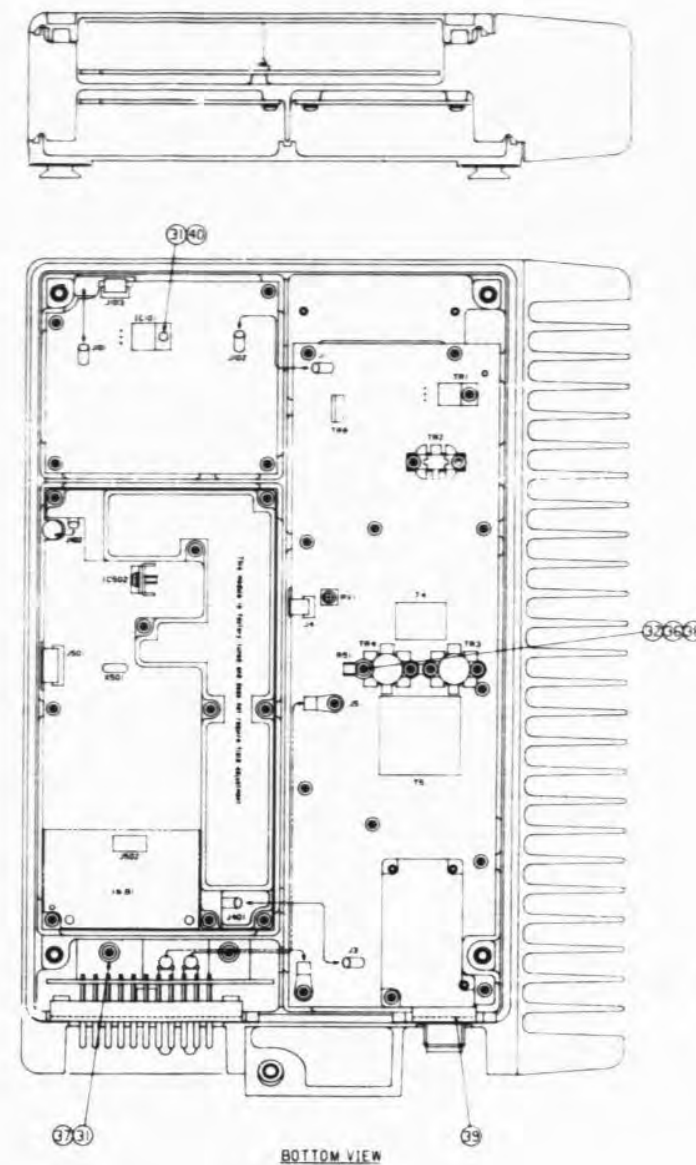
If the Modulation Acceptance Bandwidth test does not indicate the proper width, check the synthesizer frequency and then refer to the alignment of IF stages.

GE Mobile Communications

General Electric Company
Lynchburg, Virginia 24502



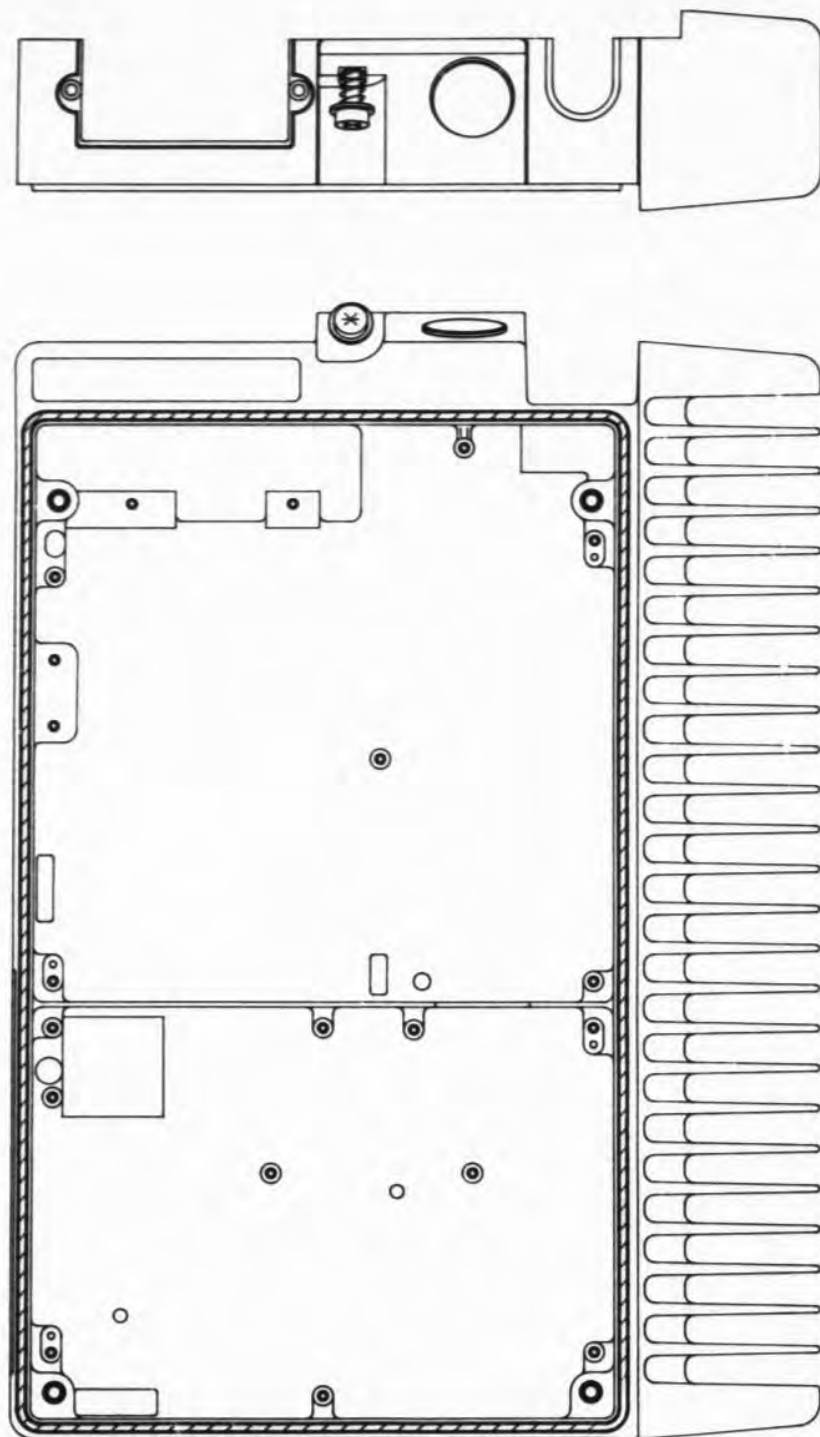
HARDWARE (SCREW) KIT
KIT CODE: B19/MPXP01954 1/2



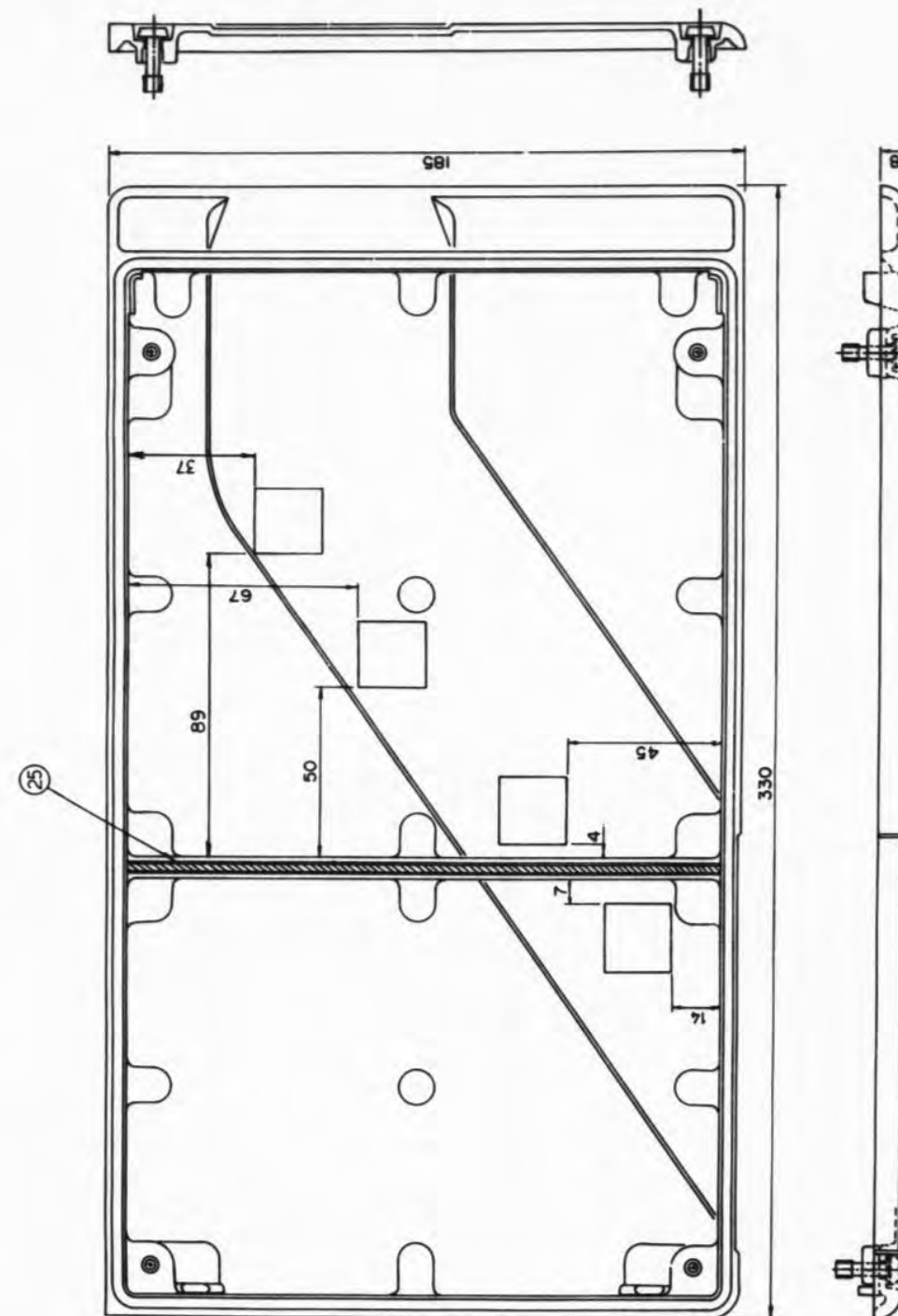
HARDWARE (SCREW) KIT
KIT CODE: B19/MPXP01954 2/2

NO	NOMENCLATOR	CODE	QTY PER KIT
11	FOOT	B19/MTL032906B	4
12	SPACER	B19/MTT021134A	4
17	COVER	B19/MTV002836	1
27	SPRING	B19/MPR02155A	1
28	SCREW	B19/MPG02014A	1
29	SCREW	B19/MPG02015	4
30	SCREW	B19/MPG02016	4
31	SCREW, PAN HEAD M3x8	B19/BRTG03830	62
32	SCREW, PAN HEAD M3x12	B19/BRTG03291	3
33	SCREW, FLAT HEAD M3x10	B19/BRTG03293	6
34	WASHER, THRUST	B19/BRTG0118	4
35	WASHER	B19/BRTG03301	1
36	SPACER	B19/MTL035255	1
37	WASHER	B19/B5FW030005	6
38	LOCK WASHER	B19/BRTG03493	3
39	SPACER	B19/MTB150011	1
40	NUT	B19/B5HW030005	1
41	CLAMP, CABLE	B19/MTT02114T	1

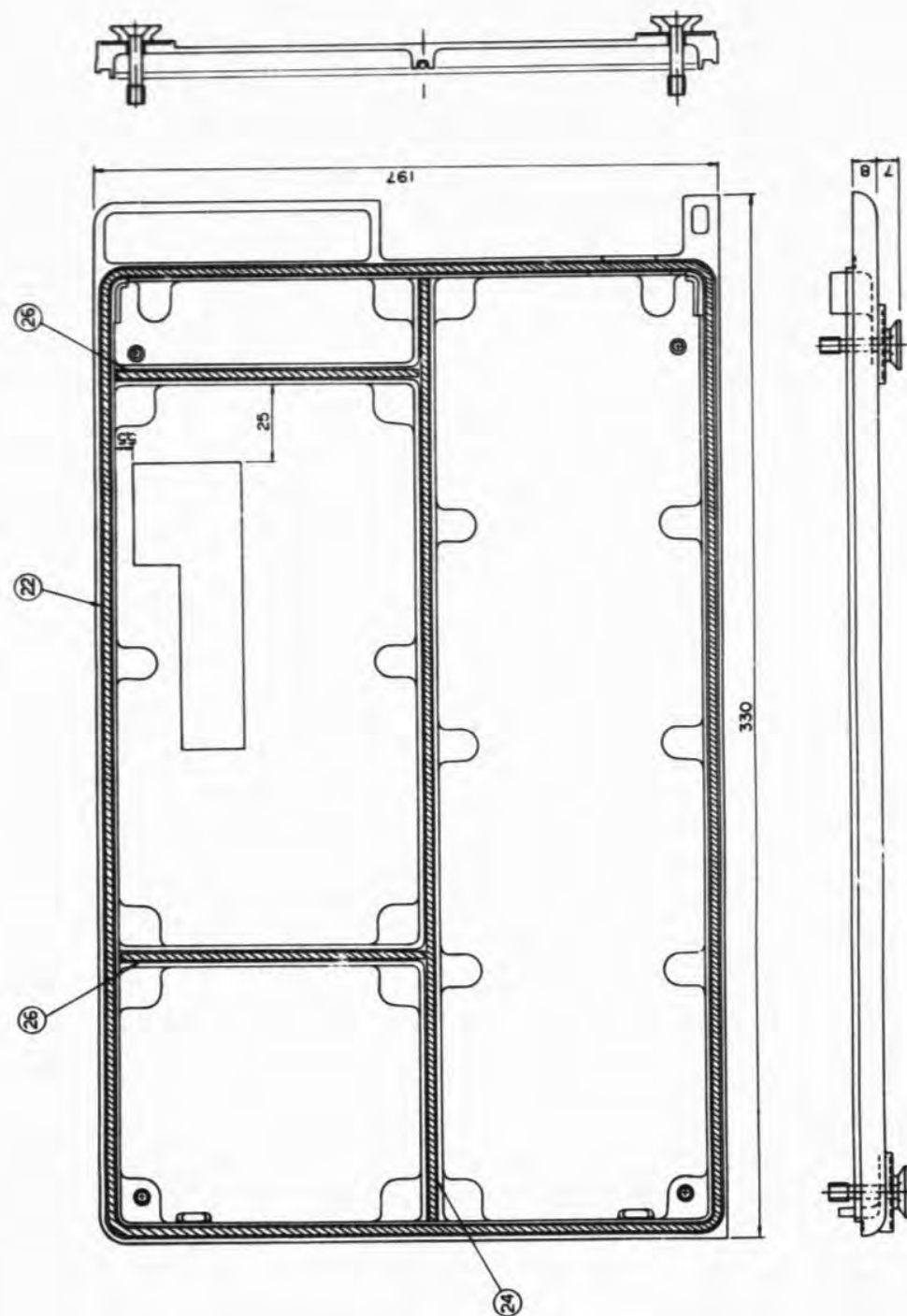
HARDWARE (SCREW) KIT
KIT CODE: B19/MPXP01954



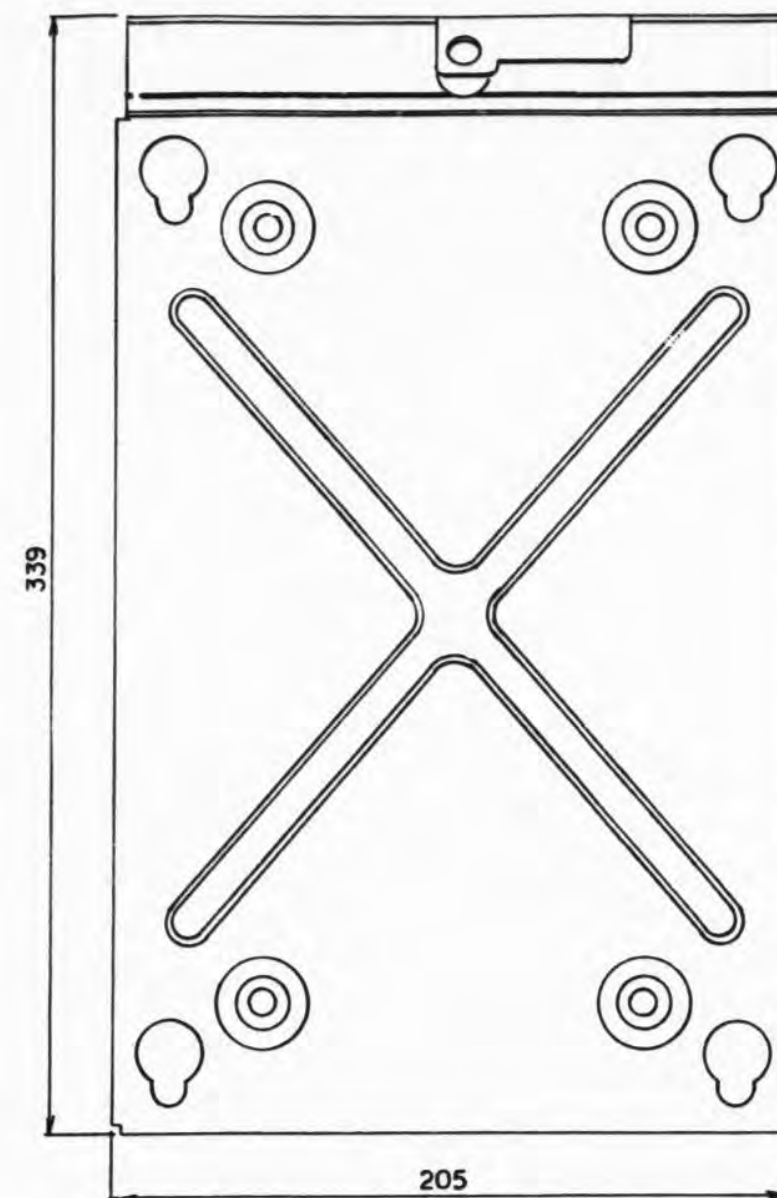
④③
FRAME ASSEMBLY
ASM CODE: B19/MPBC07182



④④
TOP COVER ASSEMBLY
ASM CODE: B19/MPBC07108



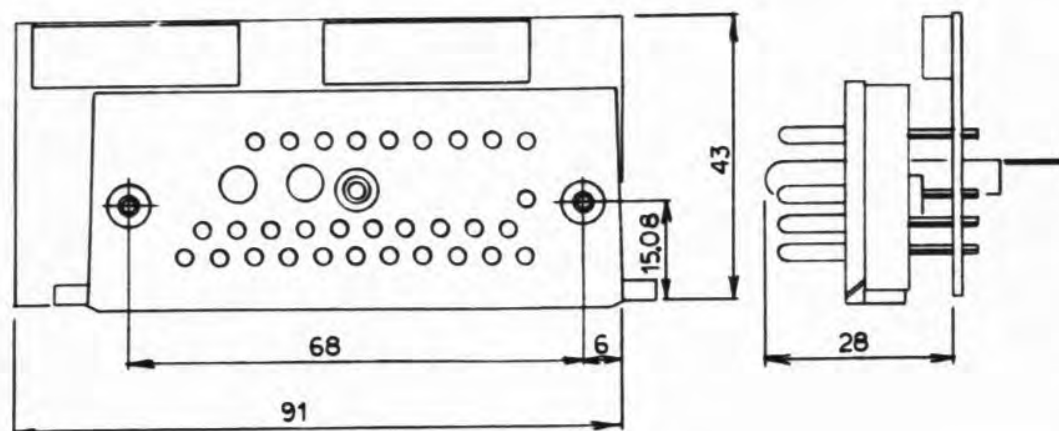
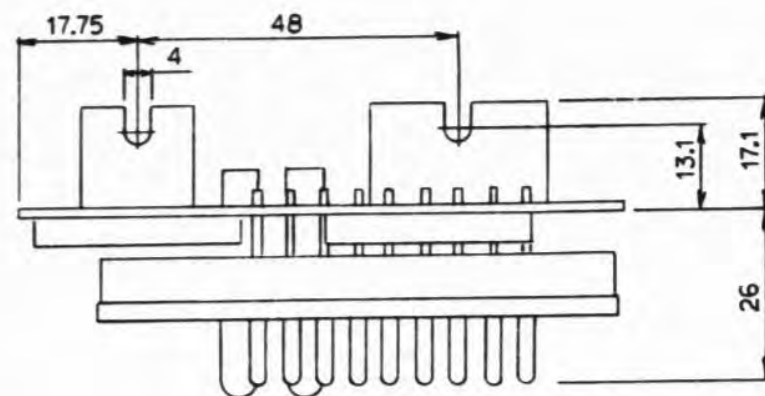
④⑤
BOTTOM COVER ASSEMBLY
ASM CODE: B19/MPBC07112



④⑥
MOUNTING BRACKET
CODE: B19/MPBX14964



④⑦
MOUNTING HARDWARE KIT
KIT CODE: B19/MPXP01744A



INTERFACE BOARD ASSEMBLY
ASM CODE: B19/CFQ-2223



MAINTENANCE MANUAL

29-50 MHz BOARD ASSEMBLIES

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DESCRIPTION

The System Control board for RANGR provides all functions necessary for two-way communications. This board is controlled by the control unit.

The System Control board interconnects with the power/control cable from the control unit.

The System Control board contains the audio circuitry, microcomputer, EEPROM and voltage regulators. The microcomputer controls all system functions, supplies frequency data to the frequency synthesizer, and tone/code data to the Channel Guard.

In addition to the normal radio functions, the microcomputer contains self-diagnostic maintenance routines to aid in troubleshooting the radio. Included are an internal test of the microcomputer and input/output tests to assure proper operation of the data port and data bus. Details and procedures are included in the Service Section of this manual.

Centralized metering jacks for servicing are accessible from the top of the radio.

The system control and interface circuits consist of the microcomputer, electrically erasable PROM, interface circuits for voltage shifting and protection, and a watchdog timer. The EEPROM gives the user the capability to program the radio's personality as desired. The EEPROM contains the receive and transmit frequency data, Channel Guard tone frequencies/digital codes and the CCT delay on a per-channel basis.

NOTE

The EEPROM may be programmed serially through the front connector using the General Electric Universal Radio Programmer Model TQ2310.

CIRCUIT ANALYSIS

SYSTEM CONTROL BOARD

MICROCOMPUTER AND CONTROL

The microcomputer interfaces with the control unit through J701/J702 and responds to all user commands and control functions originating from the control unit. It provides the transmit and receive data to the frequency synthesizer, switching information for tone and digital Channel Guard, and provides the carrier control timer (CCT) function when the radio is in the transmit mode.

When the microphone is keyed, the PTT line from the control unit goes low. This low is applied to the microcomputer through buffer TR702 and inverter TR703. TR702 is controlled by ignition switch A+. The ignition switch must be on and A+ applied to the base of TR702. TR702 must be turned on to permit keying of the transmitter. When Channel Guard is present, the release of the PTT signal is delayed by the microcomputer for approximately 160 milliseconds to eliminate any squelch tail.

The microcomputer immediately closes the antenna relay switch by applying a low level to DPTT at IC702-28. The microcomputer then delays 15 milliseconds before transmit 9V is switched on by applying a low level to TX ENB at IC702-32. This is done to guarantee that the antenna relay contacts are closed before the transmitter is energized. Once DPTT is low, the receive audio is muted. Buffers TR705 and TR704 provide DPTT to the audio control circuits, and antenna relay. IC704-B provides the DPTT signal to the Tx/Rx VCO's and the audio processor.

The TX ENB line is controlled by microcomputer port 1, bit 5 (IC702-32) through inverter TR710 and buffer TR712. A low level on IC702-32 turns TR710 off, allowing the base of TR712 to rise. TR712 turns on, and applies A- to the TX ENB line. Inverter TR711 is also turned on during this time to inhibit the alert tone PTT.

CHANNEL SELECTION

The microcomputer and EEPROM provide the radio with up to 16 independent transmit and receive frequencies. Each time the PTT switch is operated the microcomputer transfers channel data from the EEPROM and converts it to frequency data assigned to the selected channel. The frequency data is then loaded serially into the frequency synthesizer.

The microcomputer continually monitors the status of tri-state buffers IC703A-D. These buffers are periodically turned off by a positive 5 volt, one millisecond pulse from IC702-36. At the same time PROM power switch TR708 is turned on and applies +5 VDC to the EEPROM. When the buffers are turned on, channel select data is loaded into input/output ports of the microcomputer through ports P20-P23. Power is then applied to the EEPROM and the tri-state buffers are turned off. The microcomputer converts the channel select data into address information, accesses the EEPROM, and receives the frequency data stored in the addressed location. This data then passes through the I/O ports of the EEPROM and P20-P23 of the microcomputer. The conversion process is repeated eight times in rapid succession (eight locations are required for each channel) and the data loaded serially into the frequency synthesizer over the clock and data lines. This data also includes Channel Guard information, if present, and carrier control timer information on a per-channel basis. A 4-millisecond channel change pulse from port P16 of

the microcomputer is also sent to the frequency synthesizer to speed up channel acquisition.

WATCHDOG TIMER

The watchdog timer, consisting of a digital counter IC701-A and TR701, monitors the operation of the microcomputer. IC701-A generates a reset pulse in the unlikely condition that the microcomputer goes awry and does not execute the software properly.

A 6 MHz crystal X701 steps the microcomputer through the software. As programmed in software a random pulse appears at IC702-35 and is applied to the base of inverter TR701 momentarily turning it on and inhibiting any reset pulse from timer IC701-A. A discharging circuit consisting of R710 and C705 forces the microcomputer to toggle IC701-A. If the timer does not receive any inputs for a specified period of time, TR701 turns off and IC701-A times out and applies a reset pulse to pin 4 of the microcomputer. The watchdog reset will normally restore the microcomputer to normal operation so that only one pulse will occur. In the event the microcomputer is not restored to normal operation, a 6 Hz square wave will appear on the reset line and the indicator CD710 (normally unlit) will turn on. Refer to the self-diagnostic routine to determine the problem.

ADVANCE CHANGE PULSE

The advance change pulse is received from connector J702 and applied to the microcomputer interrupt port IC702-6 through inverter TR707. The advance change pulse is important in radios equipped with PSLM. When a call is received on a priority channel the advance change pulse interrupts the microcomputer, forcing it to service immediately the I/O circuits. The tri-state buffers are turned on and new channel select information read in.

CARRIER CONTROL TIMER

The carrier control timer function is executed by the microcomputer under software control on a per-channel basis. When the programmed time has elapsed an alert tone is generated from P13 (IC702-30) on the microcomputer, applied to the audio PA and heard on the speaker. The CCT may be programmed for 1 or 2 minutes or disabled (programmed for no CCT).

VOLTAGE TRANSLATION

Inverter buffers IC704B-F, TR713, and TR710 translate the 5 VDC levels required by the microcomputer to the +9 VDC level used by the frequency synthesizer. Inverter TR709 restores the proper polarity to the clock.

FREQUENCY SEGMENT CONTROL

To achieve rapid wideband VCO tuning extending over the 29-42 MHz range on the 35-50 MHz range, each Bandsplit is divided into four frequency segments.

By selecting one segment the operating frequency spread of the VCO is limited and frequency lock time reduced. Each segment is identified by two bits on a per-channel basis and programmed into the EEPROM. Capacitors are switched in and out of the VCO tank circuit to set the VCO tuning range to cover the correct frequency segment.

The frequency segment control circuit consists of a dual "D"-type flipflop operating under control of the microcomputer. The four frequency segment identification bits appear on the channel change and data lines and fed to dual "D" FF IC705. At the appropriate time the microcomputer applies the enable signal to clock the new segment data change through the FF. The output of the FF's is a binary expression identifying the frequency segment selected. Table 1 identifies the binary expression and the selected frequency segment.

The output of the frequency segment control circuit is applied to the modulation level control and the frequency segment selector circuits.

	SEGMENT	FREQUENCY SPLIT (MHz)	FF OUTPUT				GROUNDED MODULATION RESISTOR
			IC705-1 (INPUT TR216)	IC705-2 (INPUT TR217)	IC705-13 (INPUT TR218)	IC705-12 (INPUT TR219)	
29-42MHz	1	29-32	0	1	0	1	NONE
	2	32-35	0	1	1	0	R275
	3	35-38.5	1	0	0	1	R276, R296
	4	38.5-42	1	0	1	0	R275, R276 R281, R296
35-50MHz	1	35-38.5	0	1	0	1	NONE
	2	38.5-42	0	1	1	0	R275
	3	42-46	1	0	0	1	R276, R296
	4	46-50	1	0	1	0	R275, R276 R281, R296

TABLE 1 - Frequency Segment Selection

TX AUDIO PROCESSOR

The audio processor provides audio pre-emphasis with amplitude limiting and post limiter filtering and a total gain of approximately 24 dB. Approximately 27 dB gain is provided by IC607A, 4 dB by IC607B and -7 dB by R653, R654.

The 9 Volt regulator IC606 powers the audio processor and applies regulated 9 volts to a voltage divider consisting of R651, R655 and symmetry control, RV604. The +4.5 V output from the voltage divider establishes the operating reference point for operational amplifiers IC607A and IC607B. C647 provides an AC ground at the summing input of both operational amplifiers.

When the input signal to IC607A-2 is of a magnitude such that the amplifier output at IC607A-1 does not exceed 5 volts P-P, the amplifier provides a nominal 27 dB gain. When the audio signal level at IC607A-1 exceeds 5 volts P-P, the amplifier gain is reduced to 1. This limits the audio amplitude at IC607A-1 to 6 volts P-P.

Resistors R650, R652 and C646 comprise the audio pre-emphasis network that enhances the signal-to-noise ratio. R652 and C646 control the pre-emphasis curve below limiting. R650 and C646 control the cut-off point for high frequency pre-emphasis. As high frequencies are attenuated, the gain of IC607 is increased.

Audio from the microphone is coupled to the audio processor through R650 and C646.

The amplified output of IC607A is coupled through R653, C650, R656, R657, R658 and bilateral switch IC608C to a second operational amplifier IC607B. The bilateral switch is controlled by the DPTT line so that Tx audio is transmitted only when the PTT switch is pressed. IC607B provides a signal gain of approximately 4 dB.

The Channel Guard tone input is applied to bilateral switch IC608C and IC609 and controlled by the DPTT line. The CG tone then modulates the reference oscillator and VCO on the synthesizer board.

A post-limiter filter consisting of IC607B, R656-R659, C651 and C652 provides 12 dB per octave roll-off. R653 and C649 provide an additional 6 dB per octave roll-off for a total of 18 dB. The output of the post-limiter filter is coupled through the VG (Voice Guard) unit or directly to the synthesizer Tx MOD.

TX enable switch IC608-D shorts out operational amplifier IC607-B when the radio is in the receive mode. The TX ENABLE signal is generated by the microcomputer when the PTT switch is operated and is less than 2.7 VDC in the receive mode.

RX AUDIO

Received audio from the FM detector is applied to the input of audio pre-amplifier IC603-A. The audio output level of the audio preamplifier is adjusted by Volume/Squelch HI level control RV602 for 300 millivolts RMS. The audio of 300 millivolts RMS is applied to the audio preamplifier (IC603-B) through the Tone Reject filter (HC605). When VG is optionally added, this audio is applied to VG (Voice Guard) circuit (CH602, HC603). Audio output from the VG circuit is applied to Tone Reject filter (HC605) through pins J603-2 & 3. The audio is then applied to the volume and squelch controls in the control unit through connector J701-17.

Audio is returned on the VOL ARM through J701-18 and applied to audio gate (bilateral switch) IC601-B. The audio gate is controlled by DPTT (delayed Push-To-Talk) and PA KEY/CCT PA ENB and is turned on when the control input (pin 5) exceeds 7 VDC. The gate is turned off when the control input is less than 2 volts. Receipt of an on-frequency signal (if present) with

sufficient signal-to-noise level and the correct Channel Guard frequency will cause the audio control circuit to apply +9 volts to IC601-B turning the audio gate on.

Audio from the audio gate is applied to the de-emphasis network consisting of a low-pass filter and a high-pass filter.

The low-pass filter provides a 6 dB per octave roll-off between 300 and 3000 Hz. The high-pass filter attenuates frequencies below 300 Hz.

The audio output from the de-emphasis network is applied to the non-inverting input of the audio power amplifier. The audio power amplifier consists of IC602, and associated circuitry, and provides 10-watts (6.3 VRMS across a 4 ohm load) of audio output power at terminals J702-1 and 5. The gain of IC602 is determined by the value of R615.

SQUELCH CIRCUITS

The squelch circuit (HC601) monitors noise on the SQ ARM output line and allows the receiver to be unmuted when an on-frequency signal reduces the noise level below the squelch threshold setting.

The 300 millivolt output of the audio preamplifier is applied to the squelch circuit through the variable squelch control in the control unit. The squelch control sets the noise threshold level required to operate the squelch circuit. When the noise falls below the threshold level, the receiver is unmuted.

The squelch circuit (HC601) consists of a high-pass filter, an averaging detector, DC amplifier, and a Schmitt trigger shown in Figure 1. The high-pass filter consisting of HC601-A, removes all voice signals from the SQ ARM output and couples noise to HC601-B.

Noise in the 6-8 kHz range is applied to the averaging detector consisting of HC601-B. The noise is rectified and filtered to provide an average DC output level proportional to the noise input. The DC output level is adjusted by RV605.

The average DC level is amplified by HC601-C to a level ranging from 0 to 6.0 VDC, and applied to the non-inverting input of the Schmitt trigger, HC601-D. The inverting input of HC601-D is referenced to 4.5 VDC. IC603-C provides the stable 4.5 VDC reference voltage.

When the DC level exceeds 4.5 VDC, Schmitt trigger HC601-D switches and provides a positive voltage to the CAS (Carrier Activity Sensor) and RUS (Receiver Unsquelched Sensor) control transistors in the audio control circuits. The Schmitt trigger will remain on until the threshold level falls below approximately 4.3 VDC. This difference in voltage between the firing point and turn-off point provides sufficient hysteresis to eliminate "bubbling" -- i.e., noise popping in the speaker. The "bubbling" would normally be caused by transitional changes in the DC level around the reference point which allows the receiver to be unmuted.

When an on-frequency signal is received, there will be little or no noise present at the squelch input. This results in an absence of voltage at the output of the squelch circuit Schmitt trigger, allowing the receiver to be unmuted.

AUDIO CONTROL

The audio control circuits shown by Figure 2 control the operation of the audio gate (IC601-B) and the final audio PA and consist of TR601-605, inverter IC601-A and associated circuitry. The audio control circuit inputs consist of DPTT (Delayed Push-To-Talk), RX MUTE (Receiver Mute), PA KEY/CCT PA ENB (Public Address Key/Carrier Control Timer Public Address Enable), and the output of the squelch circuit.

When an on-frequency signal with the correct Channel Guard Tone is received, CAS control transistor TR601 and RUS control transistor TR602 are turned off by the absence of a positive voltage at their bases. The CAS line from the collector of TR601 rises to +9 VDC and is supplied to J702-21.

The collector of RUS Transistor TR602 also rises to +9 VDC and turns on inverter IC601-A. A- is then applied to the base of inverter TR603, turning it off and allowing its collector to go high. The positive voltage on the collector is applied to audio gate IC601-B, turning it on. TR604 is biased on but has no effect on audio switches TR605. The base of the transistor is connected to the output of audio control switch IC601A-2 which is at A-. Therefore TR605 turns off, allowing input audio to the PA which feed audio power to the speaker.

When the microphone is keyed, the DPTT input is low. This low is applied to audio gate IC601-B through CD604B, turning IC601-B off. It is also applied to audio control switch IC601-A (through CD604A) turning it off. TR603 is also off and TR604, TR605 are on. TR605 shorts out the audio input to the audio PA IC602.

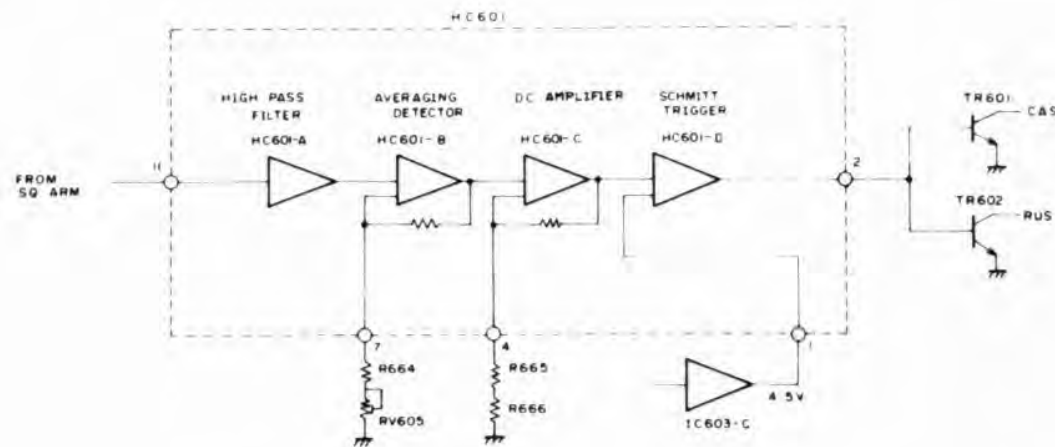


Figure 1 - Squelch circuits (HC601)

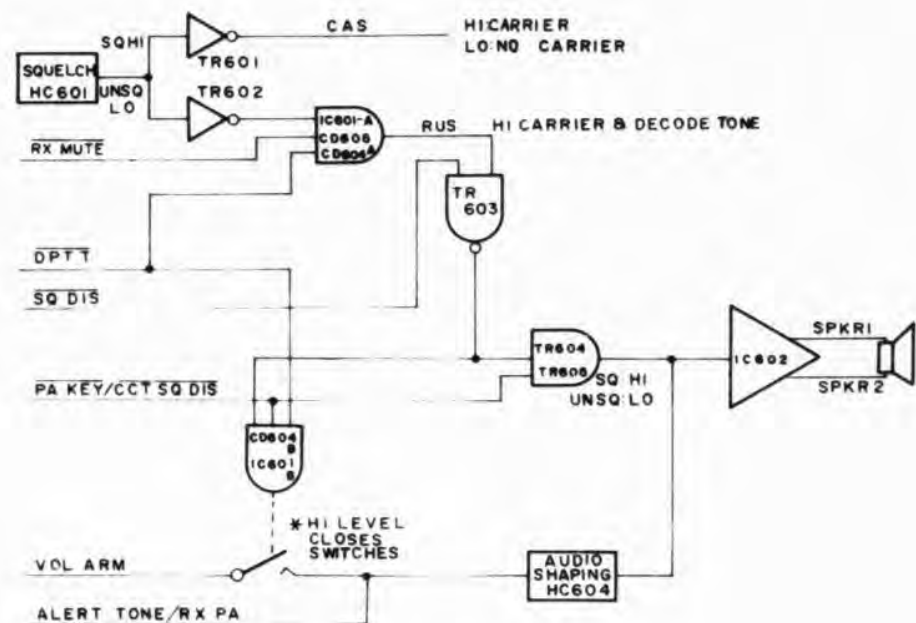


Figure 2 - Audio Control Circuit

POWER DISTRIBUTION

Battery supply A+ enters the radio through the front connector at J750-19. A- enters through J801. Figure 3 is a block diagram of the power distribution system. Two heavy connections are provided for transmit A+ and transmit A- and connect to two busses. The busses are connected to the PA through a special feedthrough arrangement. A second set of wires is routed through the control unit and supplies power to the audio amplifier and all other radio circuitry.

CAUTION



The CMOS Integrated Circuit devices used in this equipment can be destroyed by static discharges. Before handling one of these devices, the serviceman should discharge himself by touching the case of a bench test instrument that has a 3-prong power cord connected to an outlet with a known good earth ground. When soldering or desoldering a CMOS device, the soldering iron should also have a 3-prong power cord connected to an outlet with a known good earth ground. A battery-operated soldering iron may be used in place of the regular soldering iron.

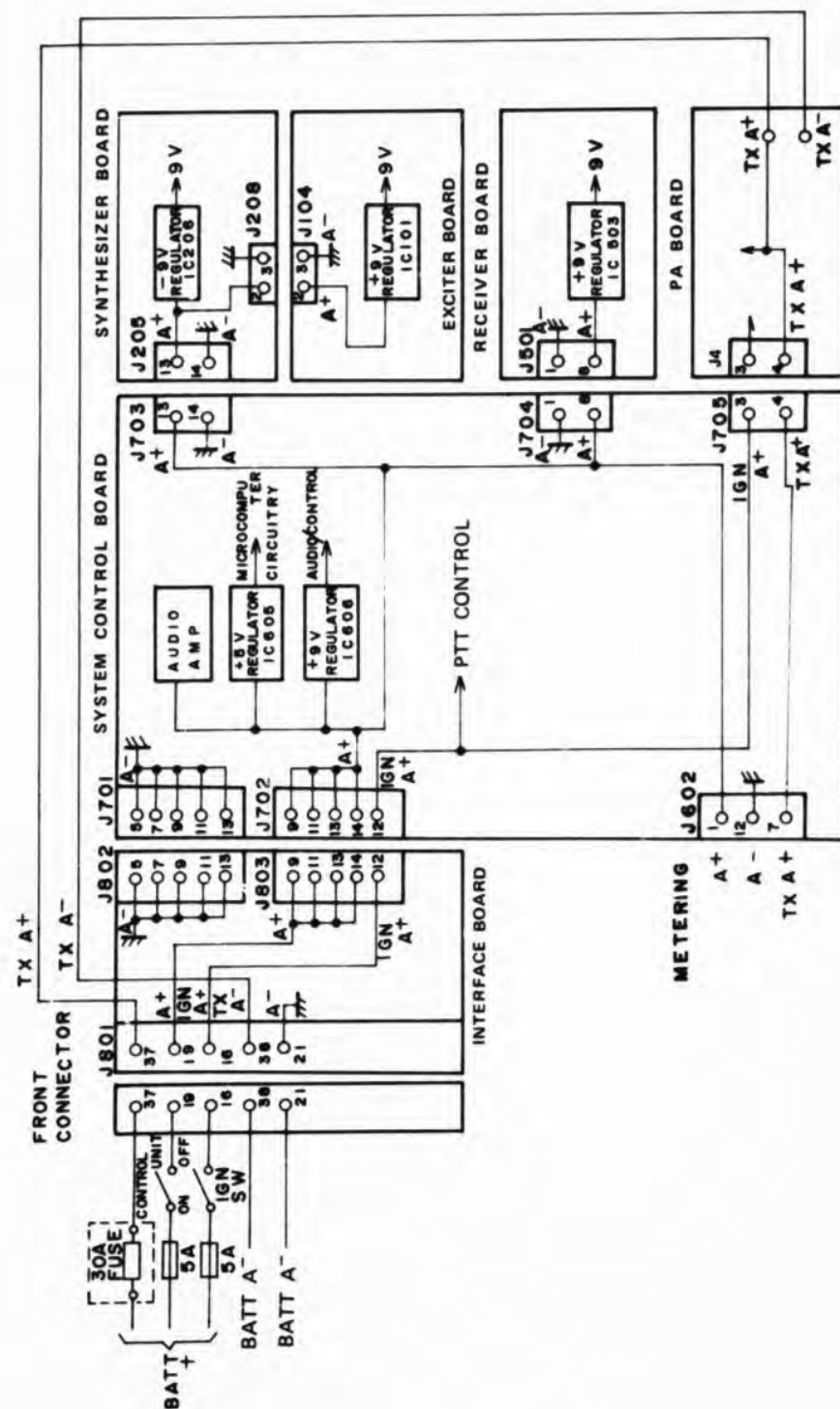


Figure 3 - Power Distribution

CHANNEL GUARD

Channel Guard provides a means of restricting calls to specific radios through the use of a continuous-tone or digitally-coded squelch system (CTCSS or CDCSS). Tone frequencies range from 67 Hz to 210.7 Hz, 33 standard tones and 83 unique digital codes are available. These tones/codes are identified in Tables 2 and 3.

STANDARD TONE FREQUENCIES Hz				
67.0	88.5	107.2	131.8	167.9
71.9	91.5	110.9	136.5	173.8
74.4	94.8	114.8	141.3	179.9
77.0	97.4	118.8	146.2	186.2
79.7	100.0	123.0	151.4	192.8
82.5	103.5	127.3	156.7	203.5
85.4			162.2	210.7

TABLE 2 - Channel Guard Tone Frequencies

PRIMARY CODE	EQUIVALENT CODE	PRIMARY CODE	EQUIVALENT CODE	PRIMARY CODE	EQUIVALENT CODE
023	340, 766	205	135, 610	464	237, 642, 772
025		223	350, 475, 750	465	056, 656
026	566	226	104, 557	466	144, 666
031	374, 643	243	267, 342	503	157, 312
032		244	176, 417	506	224, 313, 574
043	355	245	370, 554	516	067, 720
047	375, 707	251	236, 704, 742	532	161, 345
051	520, 771	261	227, 567	546	317, 614, 751
054	405, 675	263	213, 136	565	307, 362
065	301	265	171, 426	606	153, 630
071	603, 717, 746	271	427, 510, 762	612	254, 314, 706
072	470, 701	306	147, 303, 761	624	075, 501
073	640	311	330, 456, 561	627	037, 560
074	360, 721	315	321, 673	631	231, 504, 636
				745	
114	327, 615	331	372, 507	632	123, 657
115	534, 674	343	324, 570	654	163, 460, 607
116	060, 737	346	616, 635, 724	662	363, 436, 443,
				444	
125	172	351	353, 435	664	344, 471, 715
131	572, 702	364	130, 641	703	150, 256
132	605, 634, 714	365	107	712	136, 502
134	273	371	217, 453, 530	723	235, 611, 671
143	333	411	117, 756	731	447, 473, 474
					744
152	366, 415	412	127, 411, 711		
155	233, 660	413	133, 620	732	164, 207
156	517, 741	423	234, 563, 621	734	066
		713			
162	416, 553	431	262, 316, 730	743	312, 515, 663
165	354	432	276, 326	754	076, 203
172	057	445	222, 457, 575		
174	142, 270				

TABLE 3 - Primary and Equivalent Digital Codes (Octal)

The Channel Guard encode and decode functions are implemented in the microcomputer under software control. The microcomputer provides digital and/or tone Channel Guard with Squelch Tail Elimination (STE).

If the radio is in the receive mode, the Channel Guard tone/code is hard limited and inputted into the microcomputer through IC702-29 (LIM CG Tone Decode). If the correct tone code is present, the receiver is opened by the RX MUTE line. If the radio is in the transmit mode, the microcomputer generates the Channel Guard tone using WALSH BIT 1 and WALSH BIT 2. Those outputs are summed together and filtered on the System Control board to generate a smooth sine wave for tone Channel Guard or a digital waveform for digital Channel Guard.

The Channel Guard contains a summing amplifier IC604-A 8-pole active voice reject filter HC606 limiter IC604-C and tone/code reject filter HC605. A Channel Guard disable circuit TR606 allows the Channel Guard encode to be disabled. The Channel Guard decoder can be disabled at the microcomputer.

The microcomputer selects the assigned Channel Guard encode code/tone information from the EEPROM memory for each channel, transmit and receive, and generates the Channel Guard signal.

The output of audio preamplifier IC603-A is applied to the summing amplifier through bilateral switches IC601-C and D. In the encode mode DPTT is high applying A- from IC601-D to the control input of IC601-C turning it off and preventing any input from the output of audio preamplifier IC603-A from interfering with the encoding signal.

The output of summing amplifier IC604-A is applied to buffer/amplifier IC604-B through a two-pole active voice reject filter HC606. The active filter shunts all frequencies above 300 Hz to

ground, thereby preventing those frequencies from interfering with the encoded signal. The output of IC604-B is the assigned CG tone or digital signal. This signal is applied to the REF MOD line through CG deviation control RV603 and IC609. Channel Guard deviation is set for 0.75 kHz.

In the decode mode DPTT is low, turning bilateral switch IC601-D off, allowing the 9 V filtered supply to turn IC601-C on. The output of audio preamplifier IC603-A is then applied to the summing amplifier IC604-A through bilateral switch IC601-C. This signal is amplified and filtered by IC604A,B and HC606, so that only the CG signal (if present) is applied to hard limiter IC604-C. The CG signal is squared up for comparison by the microcomputer to determine if the CG signal is correct. If the microcomputer determines the CG signal to be correct, RX Mute transistor TR713, is turned off, applying +9 VDC to the RX MUTE line to open the receiver.

The Channel Guard Disable (CG DSBL) line has a double function. It can disable the encode or the decode CG function. The encode function is disabled by applying +19 V or more to J701-15. This will turn on TR606 and shunt the Channel Guard tone/code to ground while the decode function is disabled within the microcomputer software. To disable the decoder, ground the CG DSBL line at J701-15. The microcomputer will detect that the line is low, turn off TR713 and force the RX MUTE line high. The decode filter/limiter circuit is not affected, it continues to operate. The detection software also does not stop working. This allows the off-hook STE to function. When the CG DSBL line is pulled high (9.0 VDC) the microcomputer does not sense any changes. It is buffered by protection diode CD709. Channel Guard disable transistor TR606 will turn on when the CG DSBL line goes above 17 V and shorts the output of the filter to ground. This will prevent any signal from going out on CG HI and will also disable the decoder since no limited CG tone will

go to the microcomputer. The receiver will be muted since no CG is decoded. Disabling the decoder this way will never allow the audio to open up, while taking the radio off hook (pulling CG DSBL low) will always make the radio open up. Turning CG Disable transistor TR606 on causes the DC bias to change. It will take 2 or 3 seconds for the bias to restore itself after the encoder is disabled.

The Squelch Tail Elimination (STE) eliminates squelch tails when the radio is on-hook or off-hook. When Channel Guard is disabled (off-hook), the decoder is still looking at the received signal. The RX MUTE line is high, as would normally be expected. The Channel Guard decoder is looking for the STE burst (phase reversal in tone Channel Guard, STE tone in Digital Channel Guard). If an STE burst is detected, the RX MUTE line will go low for about 200 ms. This will prevent the squelch tail from being heard. After 200 ms, the RX MUTE line will go high again; by now the transmission has ended and the squelch will hold the audio closed. The off-hook STE does not affect the operation of the Channel Guard while on-hook. Another way of looking at it: the radio will go quiet for 200 ms any time STE is detected. If it was on-hook it will stay quiet after the 200 ms, if it was off-hook it will revert to noise squelch operation.

In some instances it is necessary to invert the polarity of the digital Channel Guard signal to enhance system compatibility. Inverted polarity normally results in a wrong code or one that cannot be used. When this occurs, move P604 connected between J604-1,2 to J604-2,3. The encode DCG codes may be inverted by reprogramming the EEPROM.

FREQUENCY SYNTHESIZER BOARD

The frequency synthesizer receives clock, data, and control information from the microcomputer and from this generates the Tx/Rx RF frequencies. It

also provides frequency lock status to the microcomputer. It consists of synthesizer chip IC201, low- and high-current buffers, loop filter, Tx & Rx voltage-controlled oscillators (VCO's), feedback amplifiers, the dual-modulus prescaler, and the reference oscillator. The VCO's are locked to the reference oscillator by a single direct-divide synthesis loop consisting of the feedback buffer, prescaler, and synthesizer. The TX VCO operates over a frequency range of 29 MHz to 50 MHz. The RX VCO operates over the range 49.8 to 70.8 MHz.

REFERENCE OSCILLATOR

The reference oscillator consists of a 5 PPM VC-TCXO (Voltage Controlled-Temperature Compensated Crystal Oscillator). The standard reference oscillator frequency is 13.2 MHz.

The 5 PPM VC-TCXO receives transmit CG tone from REF MOD CONTROL RV201. RV201 provides the required tone level and phase to modulate the VC-TCXO. The VC-TCXO is enclosed in an RF shielded can. Access to the oscillator trimmer is made through a hole in the top of the can. The VC-TCXO is compensated by an internal temperature-compensator circuit for both low and high temperatures. With no additional compensation the oscillators will provide 5 PPM stability from -30°C to +60°C.

CAUTION

VC-TCXOs are individually compensated at the factory and cannot be repaired in the field. Any attempt to repair or change the frequency of a VC-TCXO will void the warranty.

SYNTHESIZER

Synthesizer IC201 contains a programmable reference oscillator divider ($\div R$), phase detector, and programmable VCO dividers ($\div N$, A). The reference frequency, 13.2 MHz from the reference oscillator is divided by a fixed integer number to obtain a 5 kHz channel reference for the synthesizer. This divide value can be changed by PROM programming. The internal phase detector compares the output of the reference divider with the output of the internal $\div N$, A counter. The $\div N$, A counter receives as its input the VCO frequency divided by the dual-modulus prescaler and programmed by the microcomputer. This comparison results in a + error voltage when the phases differ and a constant output voltage when the phase-detector inputs compare in frequency and phase.

If a phase error is detected an error voltage is developed and applied to the VCO DC offset and high current buffers and loop-filter to reset the VCO frequency. The count of the $\div N$, A counters is controlled by the frequency data received on the clock and data lines from the microcomputer. Thus, when a different channel is selected or when changing to the transmit or receive mode an error voltage is generated and appears at the phase-detector output, APD OUT causing the phase-locked loop to acquire the new frequency.

The enable pulse from the microcomputer enables the synthesizer and allows frequency data to be internally stored.

DC OFFSET AND HIGH CURRENT BUFFERS

DC offset buffer TR201 and diode CD201 receive the error voltage from the synthesizer and increase this level by 1.8 VDC to extend the operating range of the high-current buffers. When the PLL is off-frequency due to a channel change or frequency drift, the error voltage from the synthesizer (APD) rises or falls, turning either TR202 or

TR203 on. These two transistors control high-current buffers TR204 and TR205. TR204 and TR205 complete a high-current rapid-charge or -discharge path for C207-C209.

If the error voltage decreases, TR203 is turned off and TR205 is turned on, completing a discharge path for C207-C209 through bilateral switches IC204. At the same time TR202 is turned on and TR204 is turned off, blocking the charge path. The opposite conditions exist when the error voltage goes positive. IC204 is turned on for 4 milliseconds when a channel is changed in the receive mode. The time is 20 milliseconds when in transmit mode and when changing from transmit to receive mode.

LOOP FILTER

The loop-filter consists of R209-R211, and C207-207. This filter controls the bandwidth and stability of the synthesizer loop. Bilateral switch IC204 is controlled by the 4 millisecond, 9 volt channel-change pulse. When the channel-change pulse is present, the bilateral switch shorts out the low-pass filter, greatly increasing the loop bandwidth to achieve the 4 millisecond channel acquisition time required for dual priority scan. The low-pass filter removes noise and other extraneous signals internal to the synthesizer chip.

The output of the filter is applied to the varicaps in the transmit and receive VCO's to adjust and maintain the VCO frequency.

The use of two VCO's allows rapid independent selection of transmit and receive frequencies across the frequency split.

RECEIVER VOLTAGE CONTROLLED OSCILLATOR

The receiver VCO consists of a low-noise JFET oscillator, TR210, followed by high-gain buffer TR211. TR211 prevents external loading and provides power gain. The VCO is a Colpitts oscillator with the various varactors, capacitors and coil forming the tank circuit.

The VCO is switched on and off under control of the DPTT line. When the DPTT line is low the Receiver VCO is turned on (TR213 is off, TR212 is on). Oscillator output is typically +10 dBm. The output is applied to the feedback buffers for VCO frequency control and as the Rx injection frequency to the receiver 1st mixer through L.O. buffers TR404, TR405 on the RX board. The Rx VCO also uses a high-Q resonator coil to achieve superior noise performance. The VCO operates over a frequency range of 49.8 to 70.8 MHz. The VCO voltage need only be set once at the highest frequency of the band split, after which it will operate over the entire split with no more tuning.

TRANSMITTER VOLTAGE CONTROLLED OSCILLATOR

The transmit VCO is basically the same as the receiver VCO. The wideband VCO allows frequency separation of 13 MHz or 15 MHz as determined by the bandsplit the radio is operating on, 29-42 MHz or 35-50 MHz. The varactors in conjunction with the frequency segment selector circuitry (TR216 - TR219, TR227, TR228, TR230 and pin diodes CD217, CD218 and CD221) provide a voltage-controlled adjustment range that extends across the entire frequency split. Buffer TR221 provides a typical output of +10 dBm to the feedback buffers for VCO frequency control and as the Tx Injection frequency to the exciter.

VCO control switch TR222 turns the Transmit VCO on when DPTT is high.

FEEDBACK BUFFERS

The Rx injection and Tx injection voltage output from the Rx VCO and Tx VCO are supplied to the receiver mixer and the exciter, respectively, and to the feedback buffers. Buffering is provided by TR206 and TR207 and the output applied to dual-modulus prescaler IC202.

DUAL-MODULUS PRESCALER

The dual-modulus prescaler completes the PLL feedback path from the synthesizer to loop filter, to the VCO's and feedback buffers and then back to the synthesizer through the prescaler. The prescaler divides the VCO frequency by 64 or 65 under control of M CONT from the synthesizer. The output of the prescaler is applied to the synthesizer where it is divided down to 5 kHz by an internal $\div N$, A counter and compared in frequency and phase with the divided-down frequency from the reference oscillator. The result of this comparison is the error voltage used to maintain frequency lock. The $\div N$, a counter is controlled by data received from the microcomputer. Depending on the operating frequency, the DC voltage at TP201 should be within the range 3.5 to 7.5 VDC when the PLL is locked.

LOCK DETECT

The lock-detect circuit consists of comparator IC203, diodes CD203 and CD204, and reference oscillator mute switch TR208 and TR209. It is used to quickly synchronize the phase relation of the divided-down VCO frequency and the reference oscillator if the loop loses lock. It also provides a fast lock-detect signal to the microcomputer to turn on the out-of-lock indicator. If a large change in frequency is required, the ramp capacitor output (C_R) of the synthesizer may increase to near 7.5 VDC and cause the comparator output to decrease. This decrease in voltage turns TR209 off and allows TR208 to be turned on by the

positive LD line from the synthesizer. Thus TR208 disables the reference oscillator and allows the PLL loop to be brought back to synchronization rapidly.

If a large frequency error exists, the LD positive lead from the synthesizer will carry negative spikes to the microcomputer through CD204 to activate the lock indicator circuit. Pulse shaper IC701 is a one-shot multivibrator which increases the pulse width to span 1 computer cycle. TR209 is turned on, keeping TR208 off thereby preventing TR208 from muting the reference oscillator.

MODULATION LEVEL CONTROL

The modulation level control circuit automatically sets the Tx audio level applied to the transmit VCO modulator CD212 through VCO deviation adjust control RV202. The modulation level control circuit consists of IC205, R274 - R282, varactor CD212, C245 and bypass capacitors C247 and C248. The modulation level is controlled by turning bilateral switches IC205 on or off (under control of IC705) to include attenuators R275, R276 and R281 in the circuit. R274, R275, R276 and R281 form an adjustable voltage divider to change the modulation level as required. Table 1 also identifies the resistor (if applicable) used for each frequency segment.

FREQUENCY SEGMENT SELECTOR

The frequency-segment selector switches capacitance in and out of the Tx and Rx VCO tank circuits to select the frequency segment containing the selected channel. The frequency segment selector consists of TR216 - TR219, TR227, TR228, TR230, CD209, CD210, CD217, CD218, CD220 and CD221 and operates under control of the microcomputer through FF's IC705A & B. Capacitors (C224, C227, C252, C255, C291 and C294) are selected or deselected for operation in a given

segment. Table 4 identifies the circuit conditions existing for selection of each segment and the capacitors used.

Reverse bias to turn the pin diode off is provided by the +8V filtered supply through R232, R234 and R286. Forward bias for the diode and power for the switching transistors are provided by the +8V source through R231, R233 and R285. When segment 3 is selected, transistors TR216, TR219 and TR227 are turned on. This applies ground to the anodes and +8V to the cathodes of pin diodes CD209, CD220 (Rx VCO) and CD217, CD221 (Tx VCO). CD210 and CD218 are forward biased causing them to turn on. This effectively places a short across C227 and AC grounds C228 in the Rx VCO and shorts C255 while AC grounding C256 in the Tx VCO.

With TR216, TR219 and TR227 still on DC ground is applied to the anodes of CD209, CD220, CD217 and CD221 through L206, L224, L218 and L225 while reverse bias is applied to their cathodes (TR217, TR228 and TR230 are off). L206, L224, L218 and L225 present a high impedance to RF frequencies. Therefore the anodes of CD209, CD220, CD217 and CD221 are near DC ground and not at AC ground.

Operation of the radio over the frequency ranges 29-42 MHz or 35-50 MHz is determined by the group number of the synthesizer board. Each frequency split is divided into four operating segments varying from 3 to 4 MHz wide.

EXCITER BOARD

The Exciter consists of three boardband negative feedback amplifier stages operating over a frequency range of 29-50 MHz. An attenuator pad (R101-R103) at the input of the exciter provides a constant load for the exciter VCO and attenuates the signal from the VCO to approximately 0 dBm. The exciter amplifies the 0 dBm signal from the VCO to provide 150 mW drive to the power amplifier.

SEGMENT	TRANSISTOR SWITCH*							PIN DIODES						GROUNDED CAPACITORS
	TR216	TR217	TR218	TR219	TR227	TR228	TR230	CD209	CD210	CD217	CD218	CD220	CD221	
1	0	1	0	1	0	1	1	ON	ON	ON	ON	ON	ON	ALL
2	0	1	1	0	1	0	0	ON	OFF	ON	OFF	OFF	OFF	C223 C251
3	1	0	0	1	1	0	0	OFF	ON	OFF	ON	OFF	OFF	C226 C254
4	1	0	1	0	1	0	0	OFF	OFF	OFF	OFF	OFF	OFF	NONE

* '1' indicates transistor is turned on.

TABLE 4 - Capacitor Selection

The injection frequency input from the TX VCO is applied to the base of amplifier TR101 through an attenuator pad and impedance matching components L101 and C101. The impedance matching network matches the VCO output to the base of TR101. R104 and R105 set the bias voltage for the TR101. C105 and C106 provide noise decoupling. T101 consists of broadband transformer (9:4 impedance ratio). R107 and R106 set the gain for TR101. The output of TR101 drives TR102, which is identical to TR101.

The output of TR102 is coupled to the base of amplifier TR103 through T102 and C111.

The 150 mW output of TR103 is coupled to the power amplifier board through impedance matching transformer T103, C120, a low-pass filter consisting of C121, C122, C123, L103, L104, and output connector J104. R114 and R115 set the bias voltage for TR103. R119 set the gain for TR103. T103 is a broadband transformer (4:1 impedance ratio).

Collector voltage for TR101, TR102 and TR103 is supplied by EX 9V through 9V TX switch TR104. EX 9V is regulated from the A+ to 9 VDC by IC101. When TX ENB is low TR104 is turned on, providing voltage to amplifier TR101, TR102 and TR103. When TX ENB goes high (receive mode) TR104 is turned off, isolating the TX VCO.

PA BOARD

The four power amplifiers covering the frequency ranges of 29-42 MHz and 35-50 MHz and power levels of 60 W and 110 W, are very similar in construction and operation. The only differences are in the transistor types and some component values. The following description applies to all four versions.

The PA assembly uses a driver and three RF power transistors to provide rated output power. The output power is adjustable over a range of 55 to 110

watts and 30 to 60 watts for the two power versions. Five transistors are used in the power control circuit.

Supply voltage for the PA is provided by power leads from the System Interface Board to J5 (A+) and (A-) on the PA board. C69, C70, C71 and C72 prevent RF from getting on the power leads. Diode CD10 will cause the main fuse in the fuse assembly to blow if the polarity of the power leads is reversed. CD9 is a surge protector to suppress voltage surges on the power leads.

RF AMPLIFIERS

The Exciter output is coupled through coaxial cable ZC610 to the PA input jack J1. The RF is coupled through an attenuator pad (R1-R3), impedance matching transformer T1 and frequency compensator C2 and R4 to the base of pre-driver TR1. L1, R5, CD1, and R7 set the bias voltage for TR1. C5 and R6 provide negative feedback to improve the stability of TR1. Collector voltage on pre-driver TR1 is controlled by the Power Control Circuit and is applied through a decoupling network which consists of C13, C14, C15, L2, C17 and C19.

The output of TR1 is coupled to the base of amplifier TR2 through impedance-matching transformer T2 and frequency compensator C12, R59 and R10. C10 and C83 provide matching between T2 and the base of TR2. C20 and R11 provided negative feedback and R12 improves the stability of TR2.

Collector voltage to driver TR2 is supplied through a decoupling network consisting of C27, C28, C29, L4, C31, C32 and C33.

The RF output from TR2 passes through impedance-matching transformer T3 and matching element C25. (Note: This is a 50 ohm point and may be used for checking power levels). From C84, RF passes through stabilizing resistors R55 and R56 and matching element C82 to input of 4:1 transformer, T4.

The Power Amplifier, consisting of TR3, TR4, T4 and T5 is a class-C push-pull power amplifier. T4 provides impedance-matching and power splitting to the bases of TR3 and TR4. C35 and C36 provide matching elements to T4. R21 and R22 provide the base loading to TR3 and TR4. C39, R20, C41 and R23 are negative feedback elements to improve the stability of TR3 and TR4. T5 provides impedance-matching and power combining for the collectors of TR3 and TR4. C44 and C45 provide matching elements to T4. C40 and C42 provide matching elements to the collector of TR3 and TR4.

Operating voltage for the power amplifier is supplied from the DC input through T5 and decoupling network consisting of C50, C51, C52, L5, C46, C47, C48 and C49.

The output of the power amplifier passes through T5 to the LPF network consisting of C86, C85, L17 and C87. (Note: This is a 50 ohm point and may be used for checking power levels.) The RF power passes through 50 ohm microstrip Z2 and Z3, directional coupler T6 and associated components and transmit/receive relay K1 to the low-pass filter.

The relay is energized by a low on DPTT from the System Control Board.

POWER CONTROL CIRCUIT

The power control circuit provides closed-loop RF power leveling and power turndown when it senses high VSWR load conditions.

When the transmitter is keyed, TR5 turns on and supplies current to zener diode CD11, which provides a constant control reference voltage.

TR6, TR8 and TR9 serve as DC amplifiers to supply voltage to the collector of TR1. The setting of RV1 determines the current supplied to the base of TR6. As the detected RF power increases, the current to the base of TR6 increases causing TR6 to pull

current away from the base of TR9. This cuts back the drive to TR9 and in turn TR8, which reduces the voltage at the collector of TR1, decreasing RF output power.

RF power is sensed by directional coupler T6 and its associated elements. Forward power is sensed by CD4 and reflected power by CD3. Forward power is determined by the setting of RV1. CD8, CD13, CD14 and CD15 set the level of reflected RF power at which the control circuit reduces the RF output.

Thermal protection is provided by R51 (posistor) and its associated elements. R51 is thermally connected to the body of TR4. As the temperature of TR4 rises above 90°C, the resistance of R51 increases, and TR7 turns ON. This diverts emitter current from TR6 to R52, which lowers the voltage at the collector of TR1, reducing the power output.

CAUTION

Do not operate the transmitter at levels higher than rated output. Operating at higher than rated output will shorten the life of the RF power transistors.

RECEIVER BOARD

The FM dual-conversion, superheterodyne receiver is designed for operation in the 29-42/35-50 MHz frequency ranges. A regulated 9.0 volts is provided to all receiver stages except the audio PA IC, which operates from the switched A+ supply.

The receiver has intermediate frequencies of 20.8 MHz and 455 kHz. Adjacent channel selectivity is obtained by using two band-pass filters: a 20.8 MHz crystal filter and a 455 kHz ceramic filter.

All of the receiver circuitry except the synthesizer, audio preamp, audio PA, and squelch circuit is mounted on the Rx board. The receiver consists of:

- Front End and Mixer
- 20.8 MHz 1st IF, 455 kHz 2nd IF and FM Detector
- Audio PA
- Squelch

RECEIVER FRONT END

An RF signal from the antenna is coupled through the low-pass filter, antenna relay, and band-pass filter (FL401) to the input of RF amplifier TR401. The output of TR401 is coupled through band-pass filter (FL403) and high-pass filters (FL402, FL404) to the input of 1st mixer HC401. Front-end selectivity is provided by these band-pass and high-pass filters.

RECEIVER INJECTION

Receiver RF injection (49.8-62.8 or 55.8-70.8 MHz) from the synthesizer VCO is applied to amplifier TR404 through J402. The input level at J402 will be between 0.5 and 1.0 milliwatts. The output of amplifier TR404 is coupled to the input of amplifier TR405. The output of amplifier TR405 is filtered by a band pass filter (FL405). This filter is tuned to pass frequencies in the 49.8-70.8 MHz passband.

1st MIXER

The first mixer is a double-balanced diode mixer (HC401) that converts a signal in 29-42 or 35-50 MHz range to the 20.8 MHz first IF frequency.

In the mixer stage, RF from the front-end RF filter is applied to one input of the mixer. Injection voltage

from the amplifier stages is applied to the other input of the mixer. The 20.8 MHz 1st IF output signal is coupled from the output of HC401 through C427 and R422 to the source input of IF AMPL TR402/403. TR402/403 are a JFET amplifier/buffer stage. The output of the JFET buffer is coupled through C429 to the optional noise blanker (W402 removed) or through impedance matching networks L503, L504 and associated circuitry (bypassing IF blanking FETs TR501 and TR502) to a 4-pole XTAL band-pass filter.

1st IF

The highly-selective Crystal filter consisting of FL501-1 and FL501-2 provides the first portion of the receiver IF selectivity. The output of the filter is coupled through impedance-matching network L506, C507 and C553 to the 1st IF amplifier TR503. The amplifier provides approximately 20 dB of IF gain. The output of TR503 is coupled through an impedance-matching network L507 to a 2-pole XTAL band-pass filter. The output of the XTAL band-pass filter is coupled through an impedance matching network L508 to the input of IC501. Diodes CD503 provides limiting for the 20.8 MHz IF signal (1.4Vp-p) to prevent high level overload of IC501.

2nd IF and DETECTOR

IC501 and associated circuitry comprise the 2nd oscillator/mixer, IF amplifier and FM detector. The 20.8 MHz IF input is applied to pin 18 of IC501 and mixed with a 20.8 MHz frequency supplied by crystal oscillator X501. Low-side injection is used. The output of the internal mixer is amplified and applied to a 6-pole ceramic filter, FL503 which provides the 455 kHz selectivity. The output of the 455 kHz filter is reapplied to IC501-5. The 2nd IF signal is amplified and limited. L509 shifts the IF signal by 90° and reapplies it to the internal FM detector. The FM detector compares the shifted IF signal

to the internal IF signal to recover the audio modulation. The audio output of IC501 is applied to the System Control board.

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BLOCK DIAGRAM	D2-D6
DRAWINGS	D7-D15
PRINTED CIRCUIT BOARD LAYOUT	D17-D28
HYBRID CIRCUIT	D29-D30
PARTS LIST	D31-D47

DRAWING SHEET No.

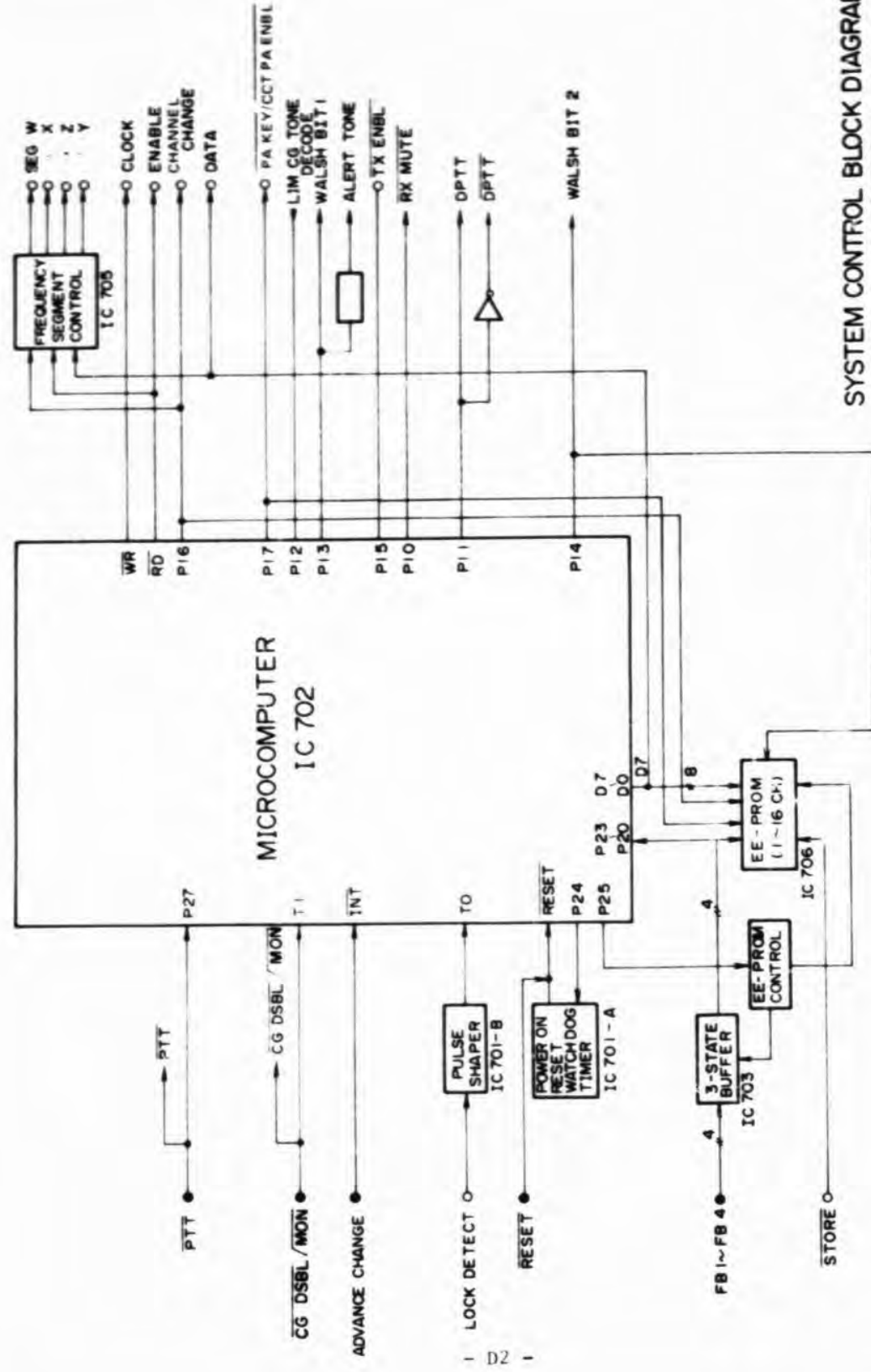
SECTION	BLOCK DIAGRAM
SYSTEM CONTROL	DA00-CMC-383B
SYNTHESIZER	DA00-CMG-130
EXCITER	DA00-CAF-254
POWER AMPLIFIER	DA00-CAH-254
RECEIVER	DA00-CMA-237
INTERFACE	DA00-CFQ-2223A

SECTION	SCHEMATIC DIAGRAM			
	A BAND 29 - 42 MHz		B BAND 35 - 50 MHz	
	60 W	110 W	60 W	110 W
INTERCONNECTION	DD00-JHM-151S60A	DD00-JHM-151S60B	DD00-JHM-151S110A	DD00-JHM-151S110B
SYSTEM CONTROL	DD00-CMC-383B	DD00-CMC-383B	DD00-CMC-383B	DD00-CMC-383B
SYNTHESIZER	DD00-CMG-130A	DD00-CMG-130A	DD00-CMG-130B	DD00-CMG-130B
EXCITER	DD00-CAF-254	DD00-CAF-254	DD00-CAF-254	DD00-CAF-254
POWER AMPLIFIER	DD00-CAH-254	DD00-CAH-254	DD00-CAH-254	DD00-CAH-254
RECEIVER	DD00-CMA-237	DD00-CMA-237	DD00-CMA-237	DD00-CMA-237
INTERFACE	DD00-CFQ-2223	DD00-CFQ-2223	DD00-CFQ-2223	DD00-CFQ-2223

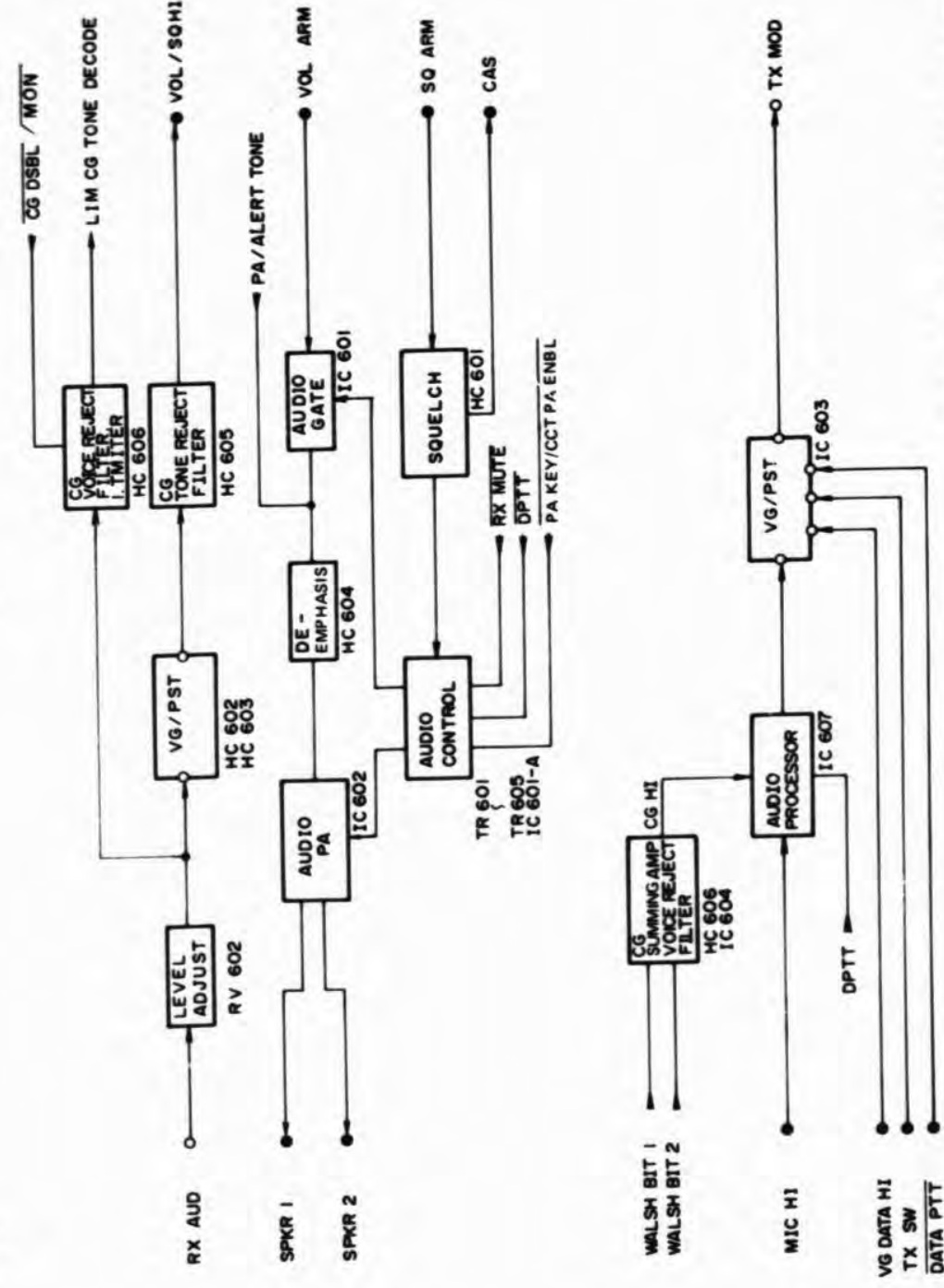


GE Mobile Communications

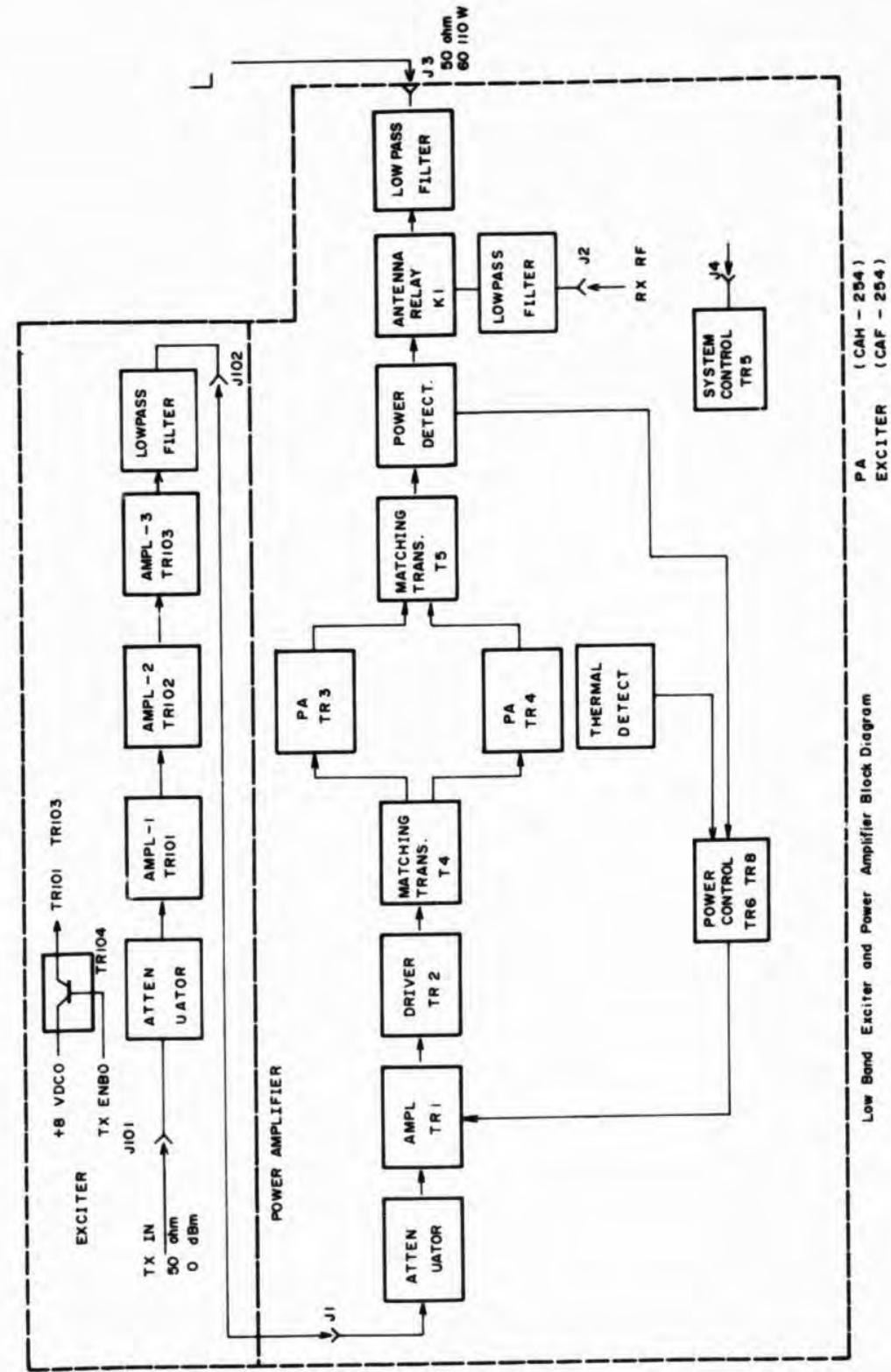
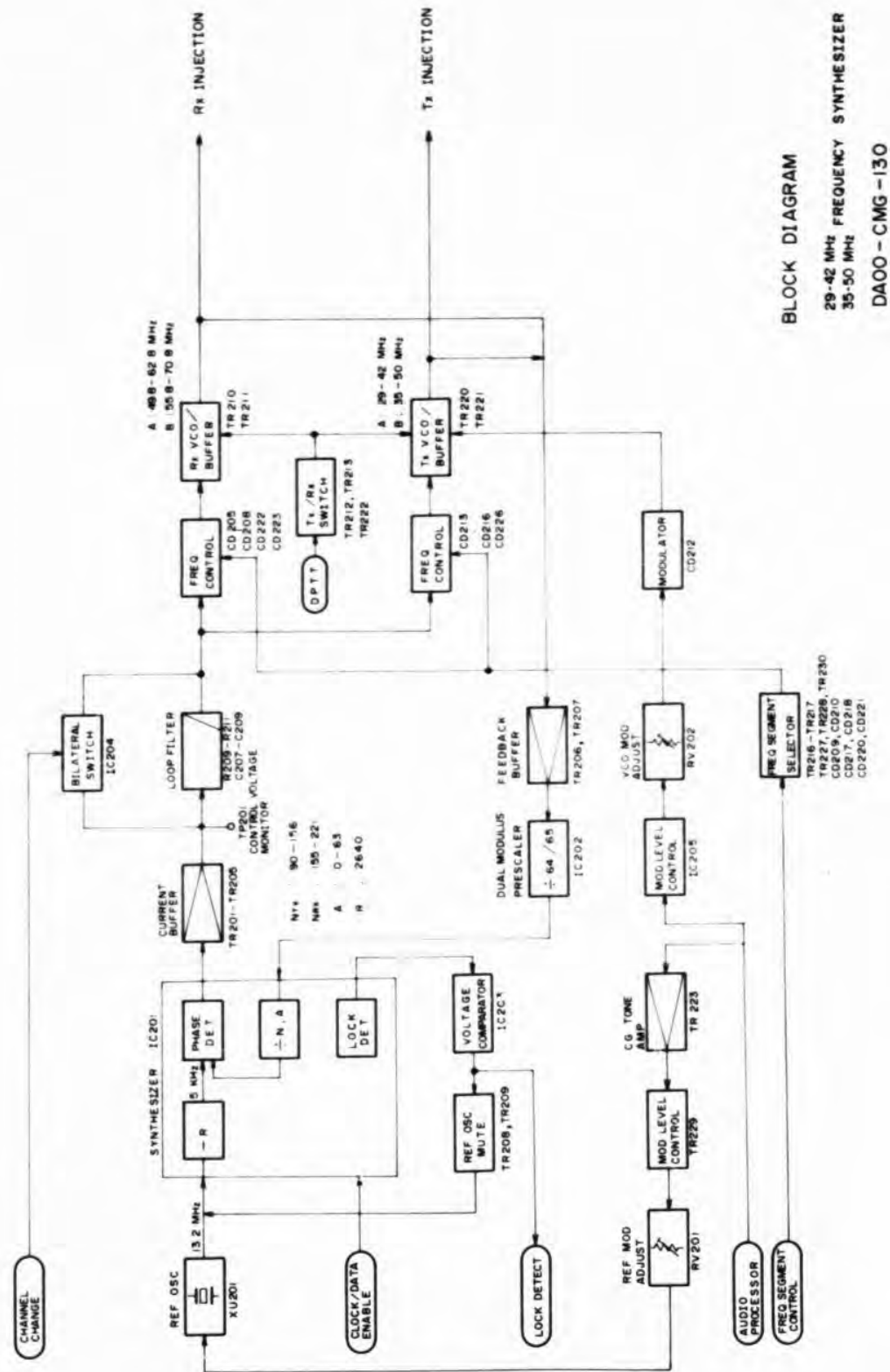
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Lynchburg, Virginia 24502

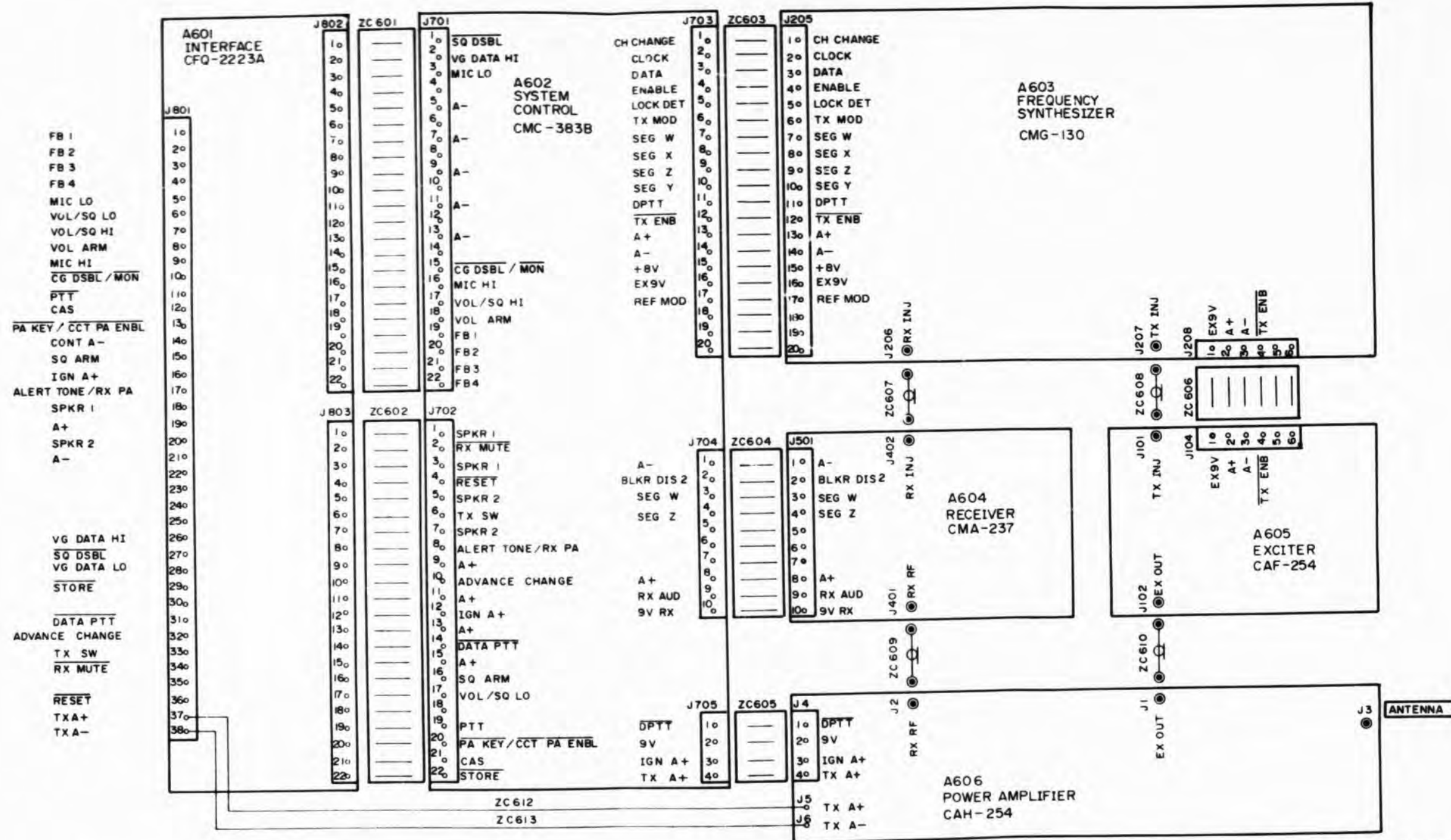


SYSTEM CONTROL BLOCK DIAGRAM
DA00 - CMC - 383B
1/2



SYSTEM CONTROL BLOCK DIAGRAM
DA00 - CMC - 383B





SECTION IDENTIFICATION CHART				
SECTION	JHM-151S60A (29~42 MHz 60W)	JHM-151S110A (29~42 MHz 110W)	JHM-151S60B (35~50 MHz 60W)	JHM-151S110B (35~50 MHz 110W)
A603	CMG-130A		CMG-130B	
A604	CMA-237A		CMA-237B	
A606	CAH-254AL	CAH-254AH	CAH-254BL	CAH-254BH

SCHEMATIC DIAGRAM
INTERCONNECTION
DD00-JHM-151S60
DD00-JHM-151S110

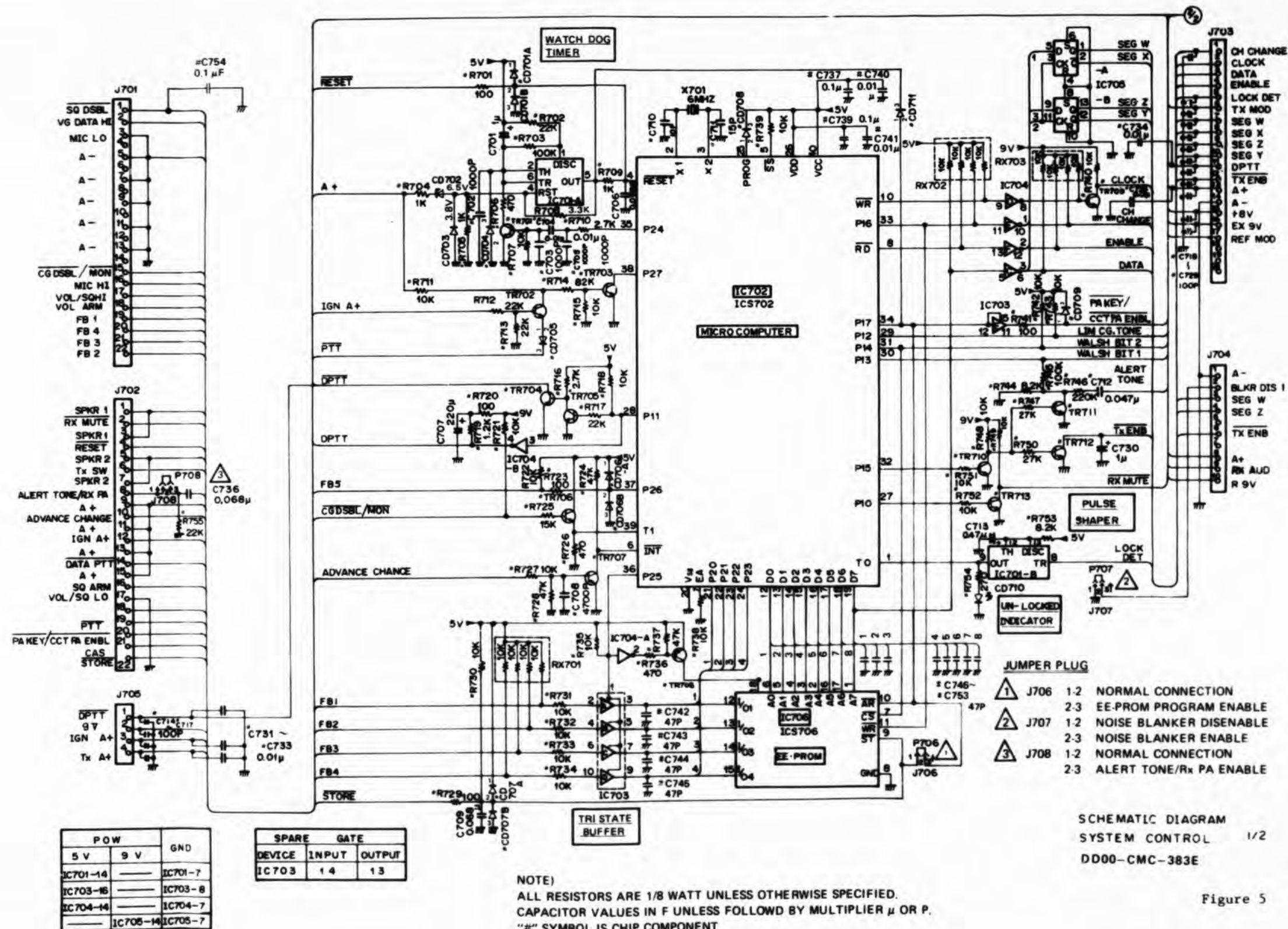
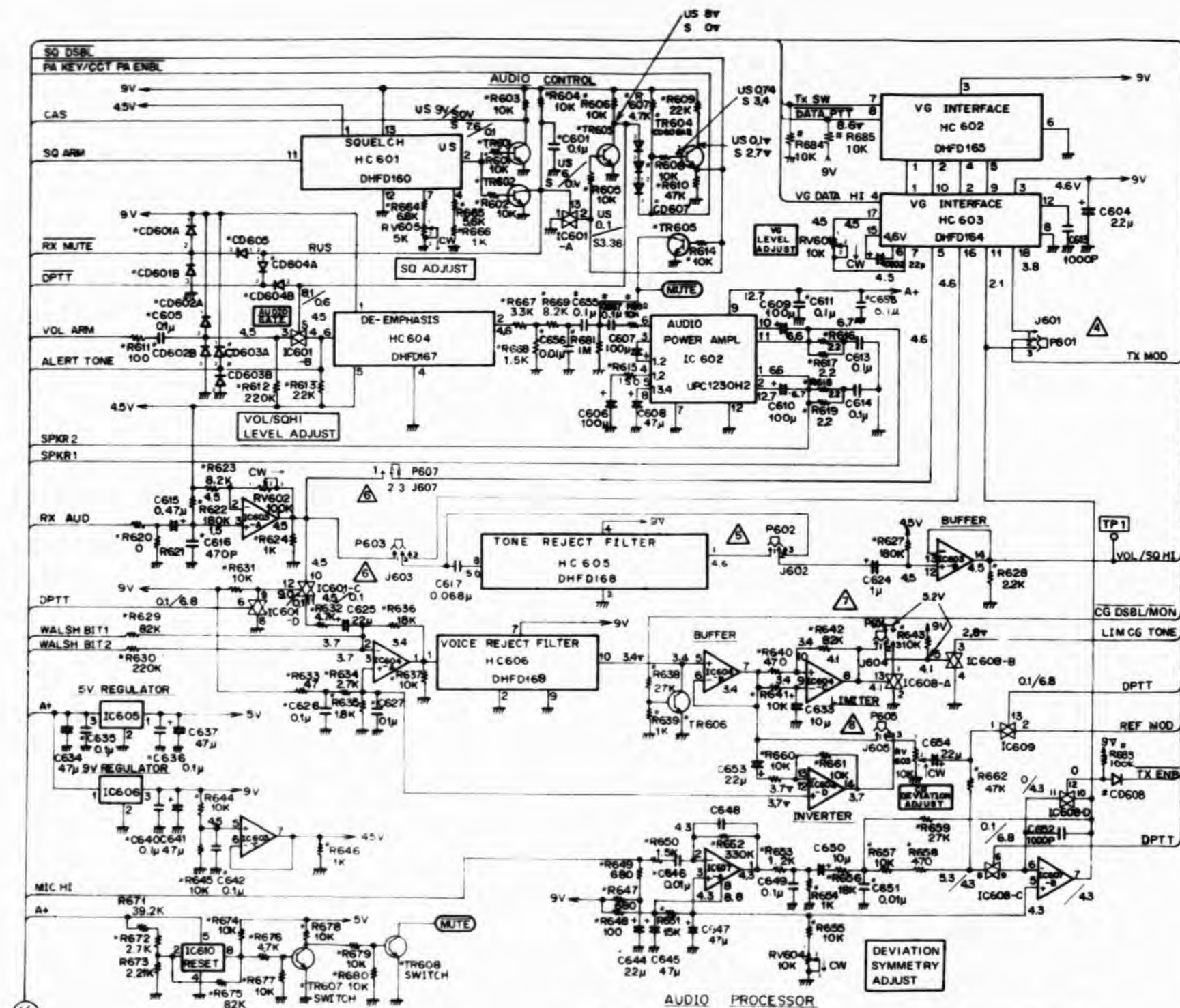


Figure 5



+9V	GND
IC601-14	IC601-7
IC603-4	IC603-11
IC604-4	IC604-11
IC607-4	IC607-7
IC608-14	IC608-7
IC609-14	IC609-7

SPARE		GATE	
DEVICE	INPUT	OUTPUT	CONTROL
IC609	3	4	5
	8	9	6
	10	11	12

J606 METERING
1 A-
2 TX MOD
3 R9V
4 5V
5 RX AUD
6 Tx A+
7 CG DSB/MON
8 Ex 9V
9 +8V
10 PTT
11 9V
12 A+

JUMPER PLUG

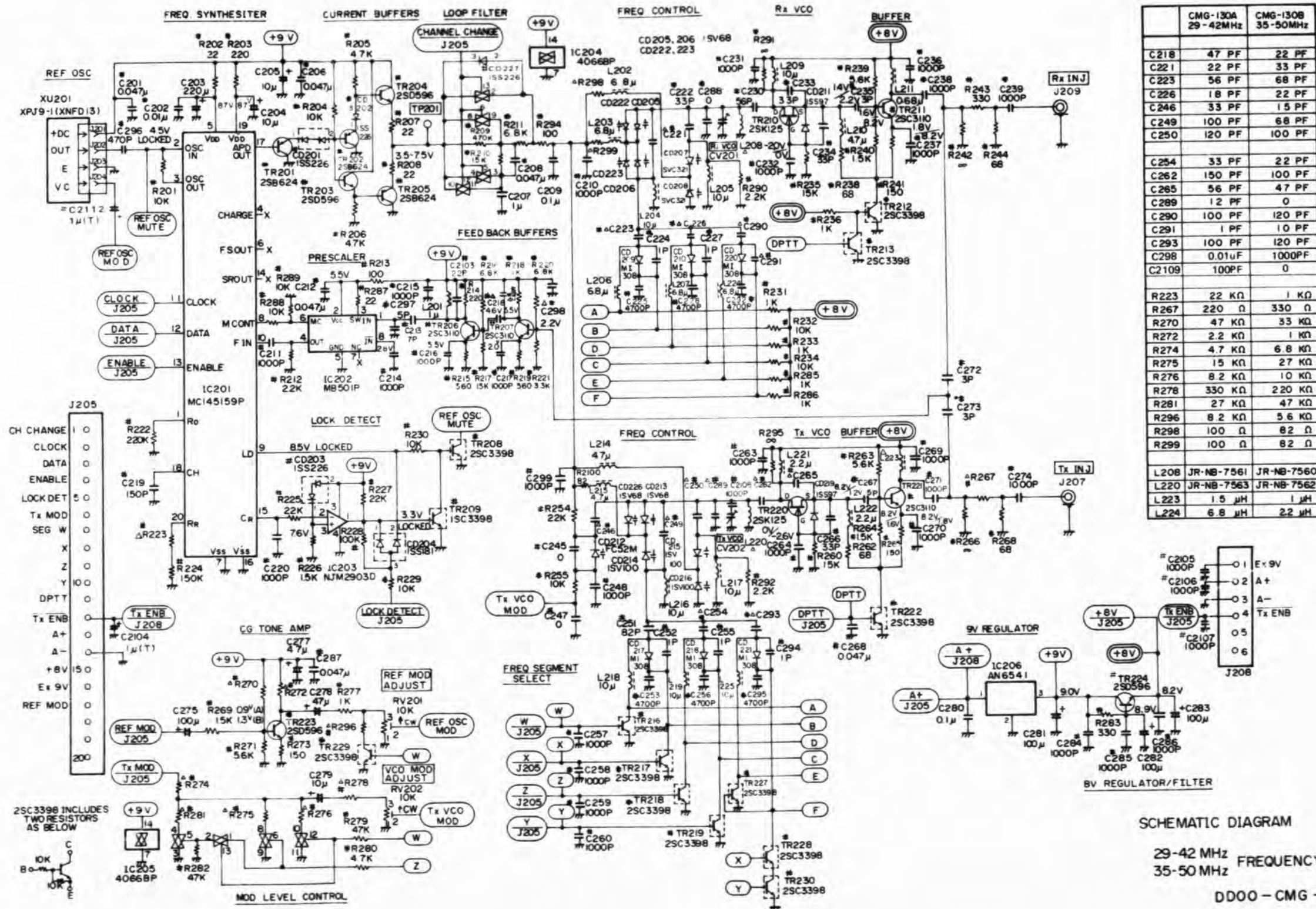
- △ J601 1-2 TRANSMIT VG USE
2-3 TRANSMIT VG NO USE
- △ J602 1-2 CG TONE REJECT FILTER USE
2-3 CG TONE REJECT FILTER NO USE
- △ J603 1-2 RECEIVE VG NO USE
2-3 RECEIVE VG USE
- △ J604 1-2 RECEIVE CG POLARITY NORMAL
2-3 RECEIVE CG POLARITY INVERT
- △ J605 1-2 TRANSMIT CG POLARITY NORMAL
2-3 TRANSMIT CG POLARITY INVERT

SCHEMATIC DIAGRAM
SYSTEM CONTROL
DD00-CMC-383E

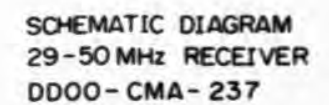
2/2

NOTE) ALL RESISTORS ARE 1/8 WATT UNLESS OTHERWISE SPECIFIED.
CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER μ
OR P. "##" SYMBOL IS CHIP COMPONENT.

Figure 6



	CMG-130A 29-42MHz	CMG-130B 35-50MHz
C218	47 PF	22 PF
C221	22 PF	33 PF
C223	56 PF	68 PF
C226	18 PF	22 PF
C246	33 PF	15 PF
C249	100 PF	68 PF
C250	120 PF	100 PF
C254	33 PF	22 PF
C262	150 PF	100 PF
C265	56 PF	47 PF
C289	12 PF	0
C290	100 PF	120 PF
C291	1 PF	10 PF
C293	100 PF	120 PF
C298	0.01uF	1000PF
C2109	100PF	0
R223	22 KΩ	1 KΩ
R267	220 Ω	330 Ω
R270	47 KΩ	33 KΩ
R272	2.2 KΩ	1 KΩ
R274	4.7 KΩ	6.8 KΩ
R275	15 KΩ	27 KΩ
R276	8.2 KΩ	10 KΩ
R278	330 KΩ	220 KΩ
R281	27 KΩ	47 KΩ
R296	8.2 KΩ	5.6 KΩ
R298	100 Ω	82 Ω
R299	100 Ω	82 Ω
L208	JR-NB-7561	JR-NB-7560
L220	JR-NB-7563	JR-NB-7562
L223	1.5 μH	1 μH
L224	6.8 μH	2.2 μH

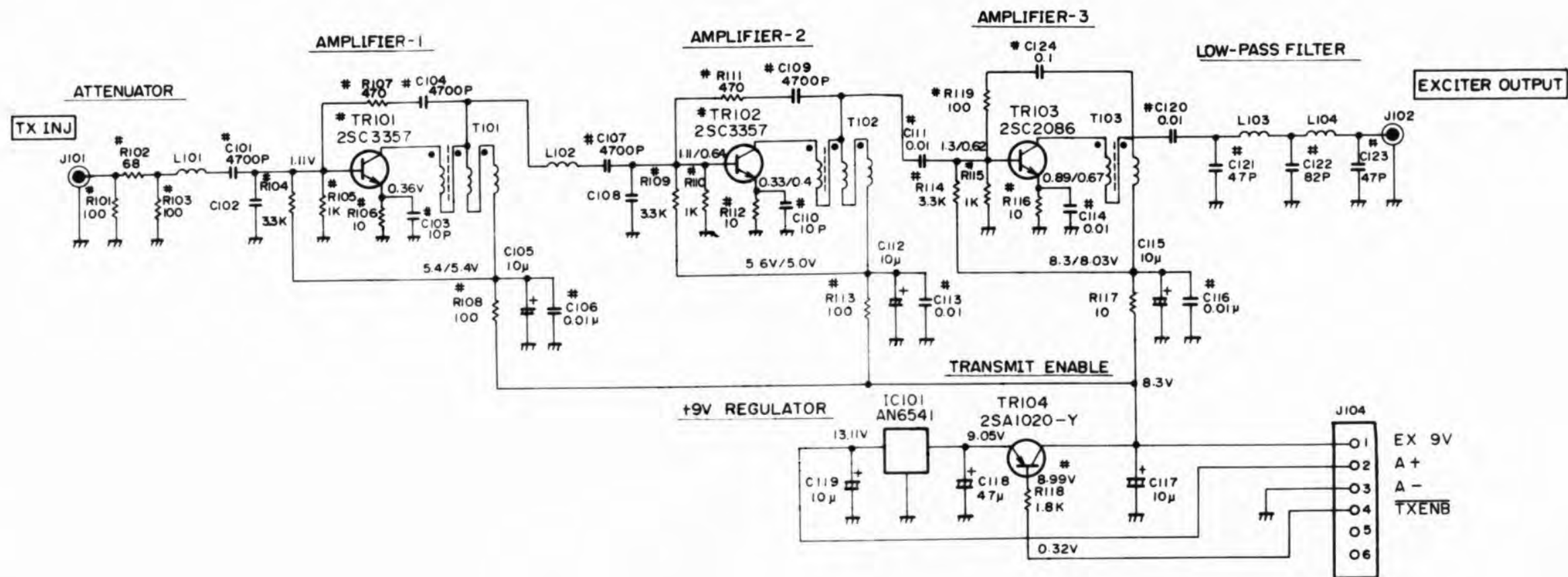


BAND PART	CMA-237A	CMA-237B
	29 ~ 42	35 ~ 50MHz
FL401,403	MBP29-42A1	MBP35-50A1
*C406	6 (PF)	5 (PF)
*C407	6	5
*C408	10	8
*C409	12	7
*C415	6	5
*C416	6	5
*C417	10	8
*C418	12	7

TO ADD NOISE BLANKER OPTION, REMOVE W402, AND PLUG
IN NOISE BLANKER BOARD INTO J502. TO DISABLE NOISE BLANKER
MOVE P501 FROM J503-2 & 3 TO J503-1 & 2 IN RECEIVER UNIT OF
P707 FROM J707-1 & 2 TO J707-2 & 3 IN SYSTEM CONTROL UNIT.

NOTES
"B" IDENTIFIES "CHIP" COMPONENTS
(EXAMPLE IC401) WHICH ARE LOCATED
ON SOLDER SIDE OF PWB.

ALL RESISTORS ARE 1/8 WATT UNLESS OTHERWISE SPECIFIED.
RESISTOR VALUES IN Ω UNLESS FOLLOWED BY MULTIPLIER K OR M.
CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER μ , n OR p.
INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER m OR μ .

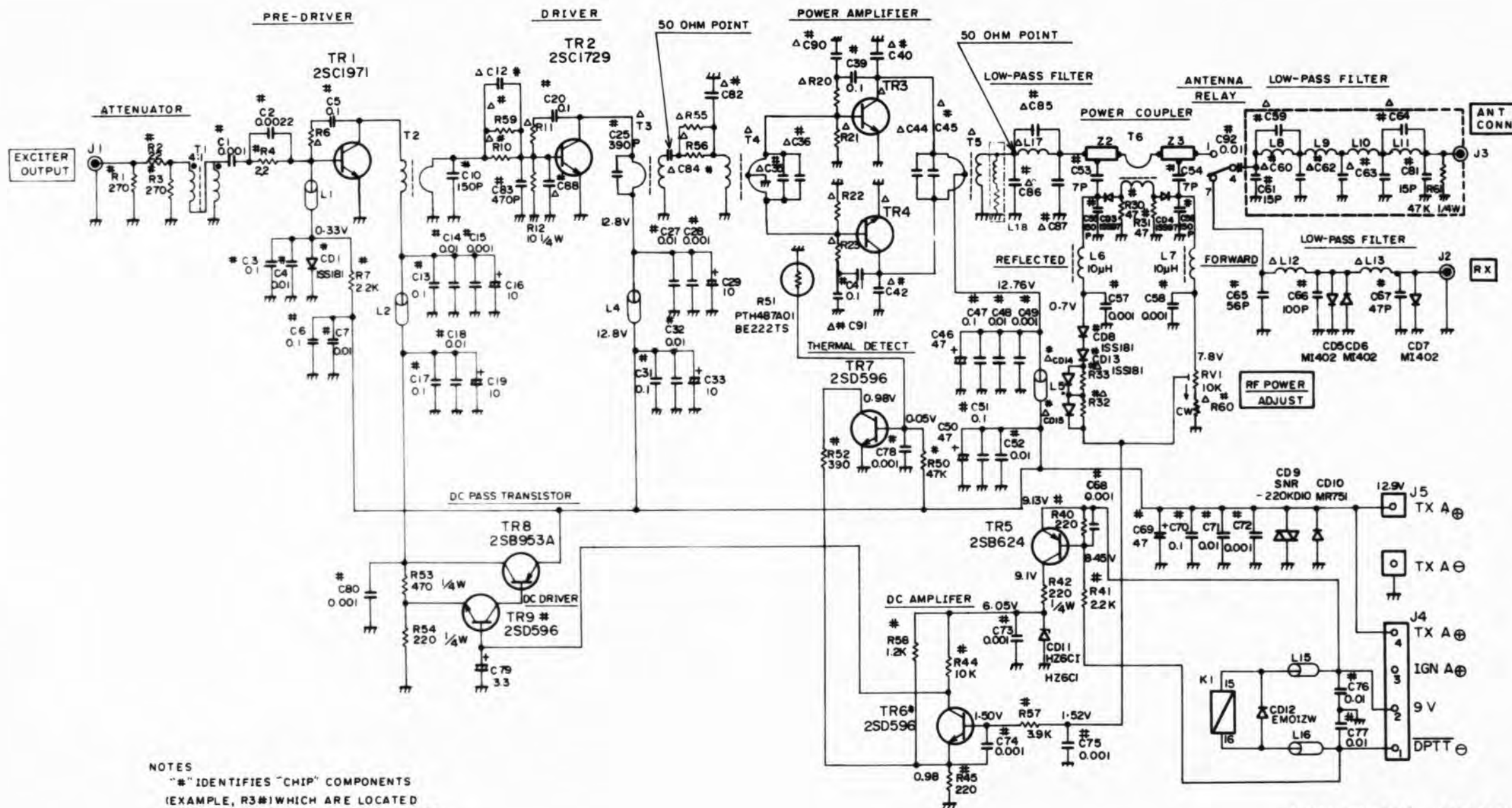


NOTES

"#" IDENTIFIES "CHIP" COMPONENTS
(EXAMPLE: R3#) WHICH ARE LOCATED
ON THE SOLDER SIDE OF THE BOARD.

ALL RESISTORS ARE 1/8 WATT UNLESS OTHERWISE SPECIFIED.
RESISTOR VALUES IN Ω UNLESS FOLLOWED BY MULTIPLIER K OR M.
CAPACITOR VALUES IN μ F UNLESS FOLLOWED BY MULTIPLIER n OR p.
INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER m OR μ .

SCHEMATIC DIAGRAM
29.0-50MHz EXCITER
DD00-CAF-254



NOTES

"*" IDENTIFIES "CHIP" COMPONENTS

(EXAMPLE, R3*) WHICH ARE LOCATED

ON THE COMPONENT SIDE OF THE BOARD.

ALL RESISTORS ARE 1/8 WATT UNLESS OTHERWISE SPECIFIED,

RESISTOR VALUES IN Ω UNLESS FOLLOWED BY MULTIPLIER K OR M.

CAPACITOR VALUES IN μ F UNLESS FOLLOWED BY MULTIPLIER n OR p.

INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER m OR μ .

SCHEMATIC DIAGRAM

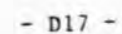
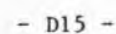
29.0-50MHz 60/110 WATT

POWER AMPLIFIER

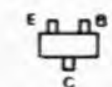
DD00-CAH-254

△ COMPONENT IDENTIFICATION CHART

PART	CAH-254AL		CAH-254AH		CAH-254BL		CAH-254BH	
	29-42MHz	60W	29-42MHz	110W	35-50MHz	60W	35-50MHz	110W
# C12	—		0.0022μ		—		0.0022 μ	
# C35	—		820P		—		820P	
C36	330P		470P		330P		330P	
# C40	220P		270P		220P		180P	
C42	"		"		"		"	
C44	270P		390P		270P		330P	
# C45	390P		470P		390P		820P	
# C59	78P		78P		56P		56P	
# C60	130P		130P		100P		100P	
# C62	185P		185P		130P		130P	
# C63	130P		270P		100P		100P	
# C64	56P		56P		45P		45P	
# C82	—		270P		—		22P	
# C84	0.1		0.1		0.1		120P	
# C85	70P		70P		56P		56P	
# C86	39P		39P		30P		30P	
# C87	18P		18P		15P		15P	
# C88	270P		—		270P		—	
L12	11.5T		11.5T		8.5T		8.5T	
L13	"		"		9.5T		9.5T	
L17	5.5T		5.5T		4.5T		4.5T	
R6	1K 1/4W		560Ω 1/4W		1K 1/4W		560Ω 1/4W	
# R10	6.8Ω 1/8W		22Ω 1/8W		6.8Ω 1/8W		22Ω 1/8W	
R11	56Ω 2W		47Ω 2W		56Ω 2W		47Ω 2W	
R20	47Ω 2W		47Ω 3W		47Ω 2W		47Ω 3W	
R21	47Ω 1/2W		22Ω 1/2W		47Ω 1/2W		22Ω 1/2W	
R22	"		"		"		"	
R23	47Ω 2W		47Ω 3W		47Ω 2W		47Ω 3W	
# R33	0Ω 1/8W		—		0Ω 1/8W		—	
# R32	0Ω 1/8W		—		0Ω 1/8W		—	
T3	1:16		1:4		1:16		1:16	
T4	16:1		4:1		16:1		9:1	
TR3	2SC2630		2SC2782		2SC2630		2SC2782	
TR4	"		"		"		"	
# CD14	—		1SS181		—		1SS181	
# CD15	—		"		—		"	
# R60	27K 1/8W		1.8K 1/8W		30K 1/8W		1.8K 1/8W	
# C90	—		150P		—		—	
# C91	—		150P		—		—	
R56	—		10Ω 2W		—		10Ω 2W	
R59	5.6Ω 1/8W		—		5.6K 1/8W		—	



LEAD IDENTIFICATION FOR TRANSISTOR



(TOP VIEW)

LEAD IDENTIFICATION FOR DIODES

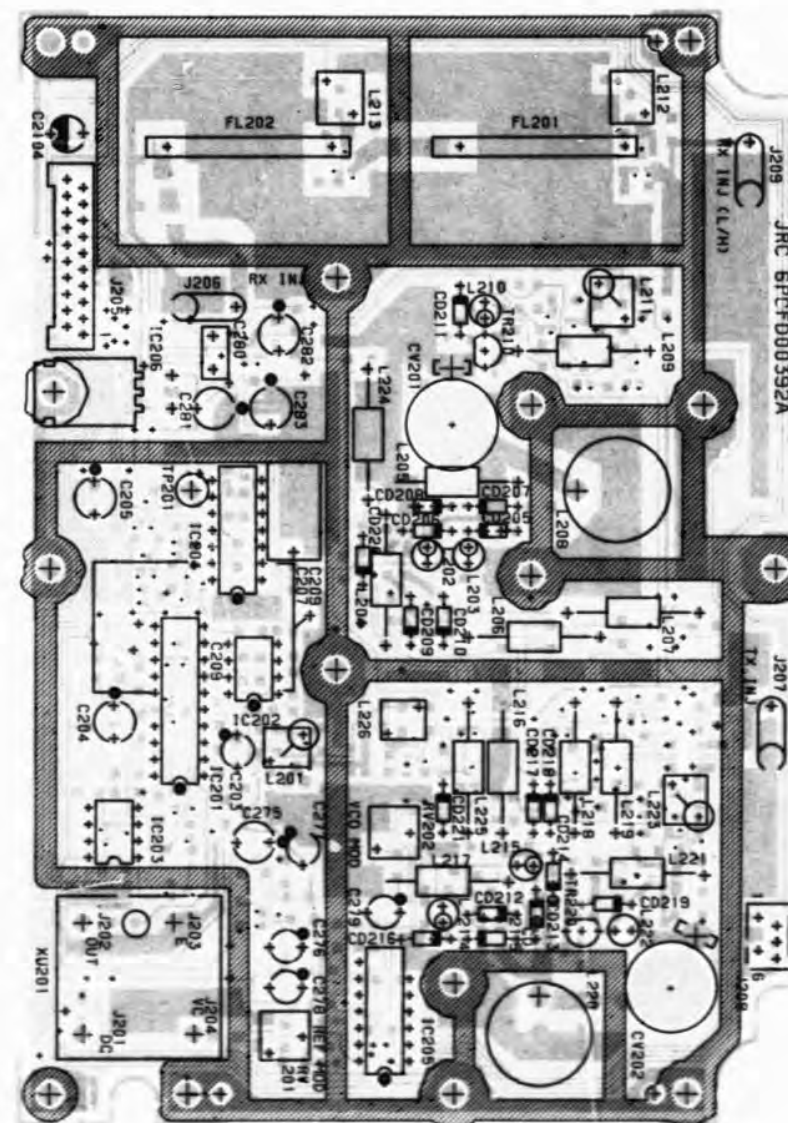


(TOP VIEW)

SYSTEM CONTROL BOARD



← RUNS ON SOLDER SIDE
← RUNS ON BOTH SIDES
← RUNS ON COMPONENT SIDE



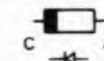
FREQUENCY SYNTHESIZER BOARD

LEAD IDENTIFICATION FOR TR210, TR220 (TOP VIEW)

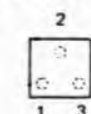


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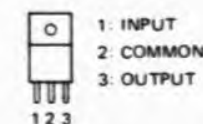
LEAD IDENTIFICATION FOR DIODES (TOP VIEW)

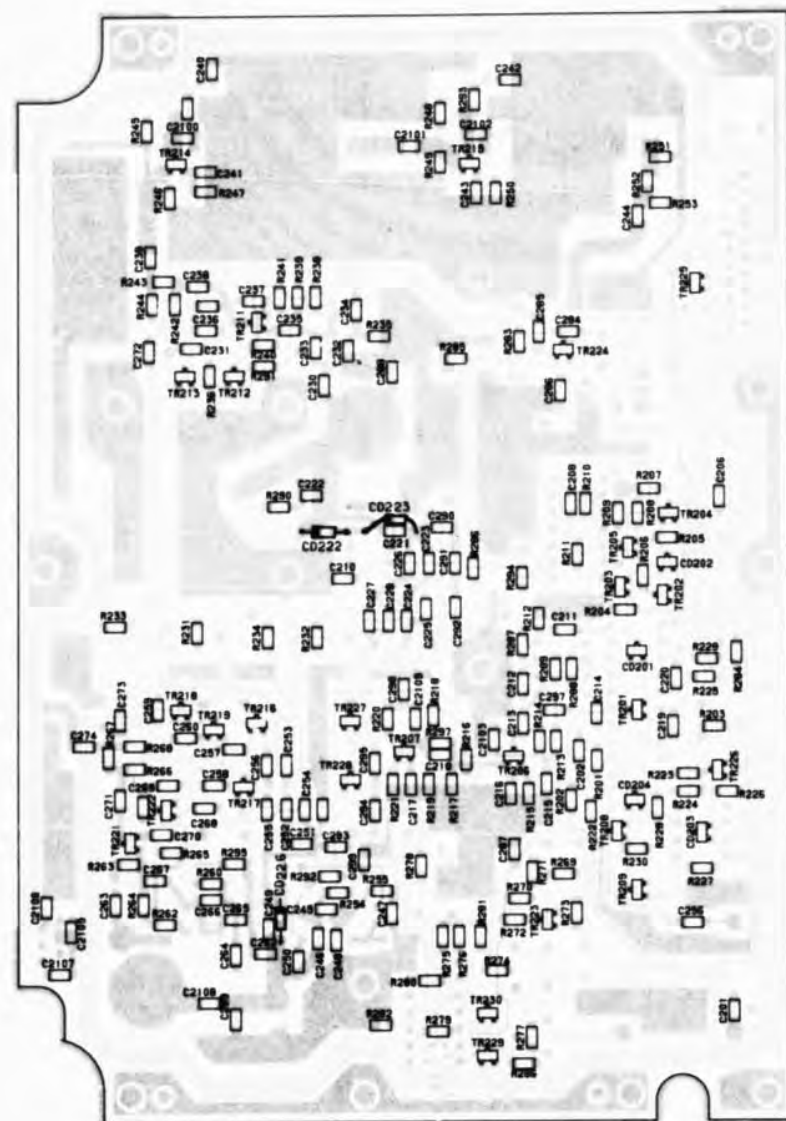


LEAD IDENTIFICATION FOR RV201, RV202 (TOP VIEW)



LEAD IDENTIFICATION FOR IC206 (TOP VIEW)

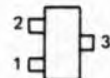




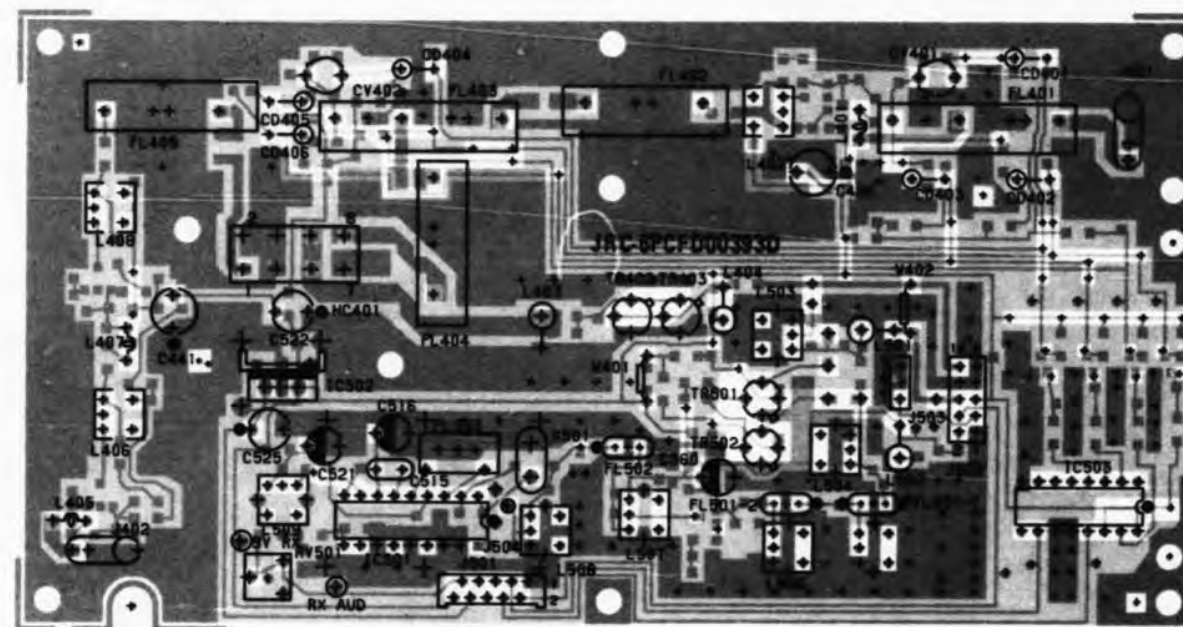
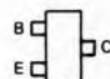
FREQUENCY SYNTHESIZER

(BACK VIEW OF COMPONENT BOARD)

LEAD IDENTIFICATION
FOR DIODES
(TOP VIEW)

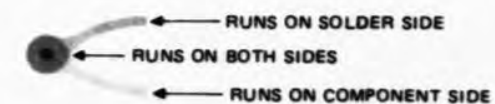
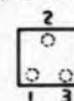


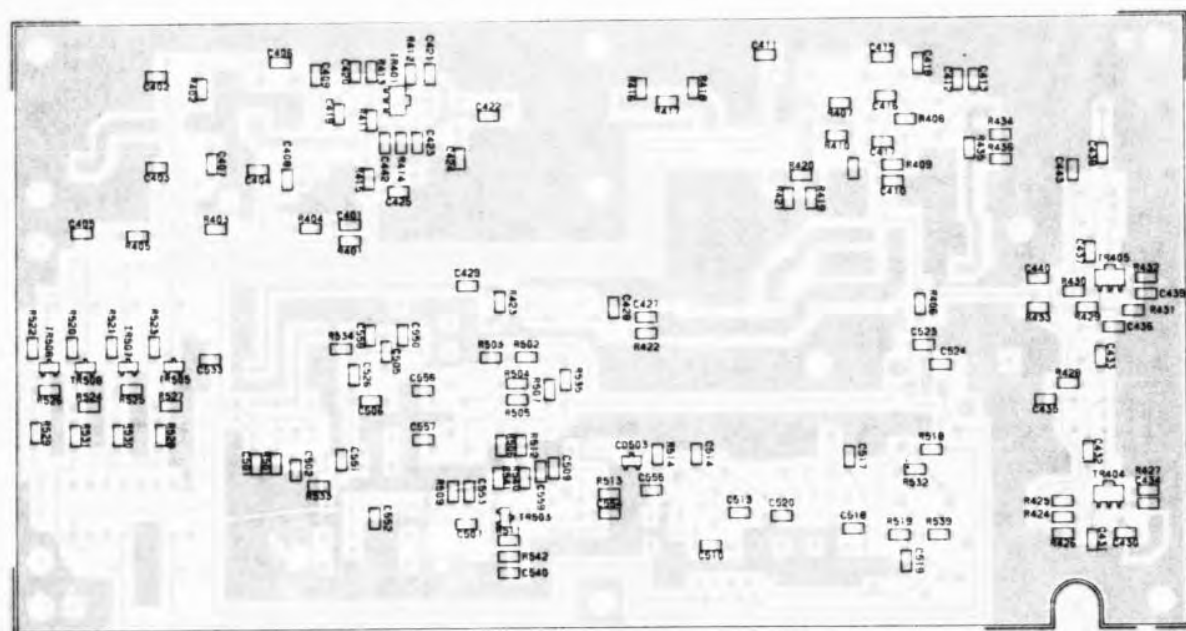
LEAD IDENTIFICATION
FOR TRANSISTORS
(TOP VIEW)



RECEIVER BOARD

LEAD IDENTIFICATION
FOR RV 501
(TOP VIEW)

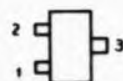




RECEIVER BOARD

LEAD IDENTIFICATION
FOR CD 501

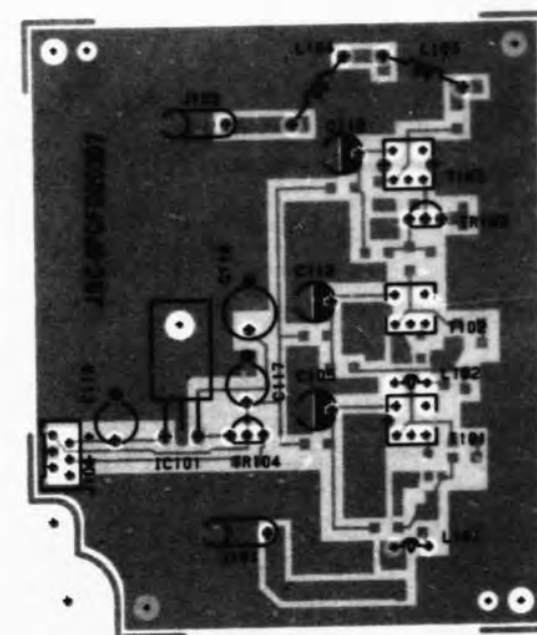
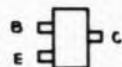
(TOP VIEW)



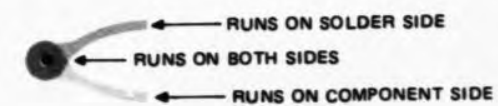
- D22 -

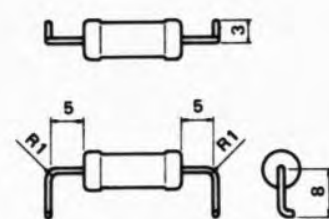
LEAD IDENTIFICATION FOR TRANSISTORS

(TOP VIEW)

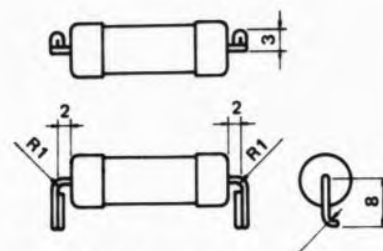


TRANSMIT EXCITER BOARD

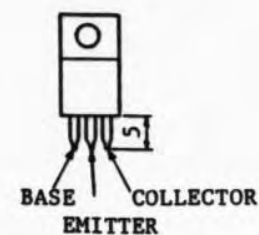




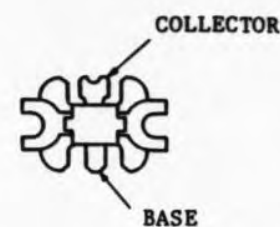
LEAD TRIMMING
FOR R20 AND R23
(Used in A60 and B60)



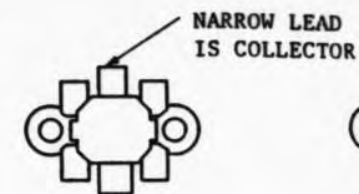
LEAD TRIMMING
FOR R20 AND R23
(Used in A110 and B110)



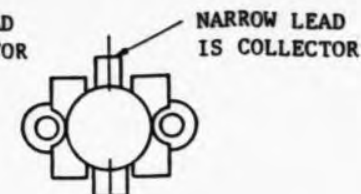
LEAD TRIMMING
FOR TR 1



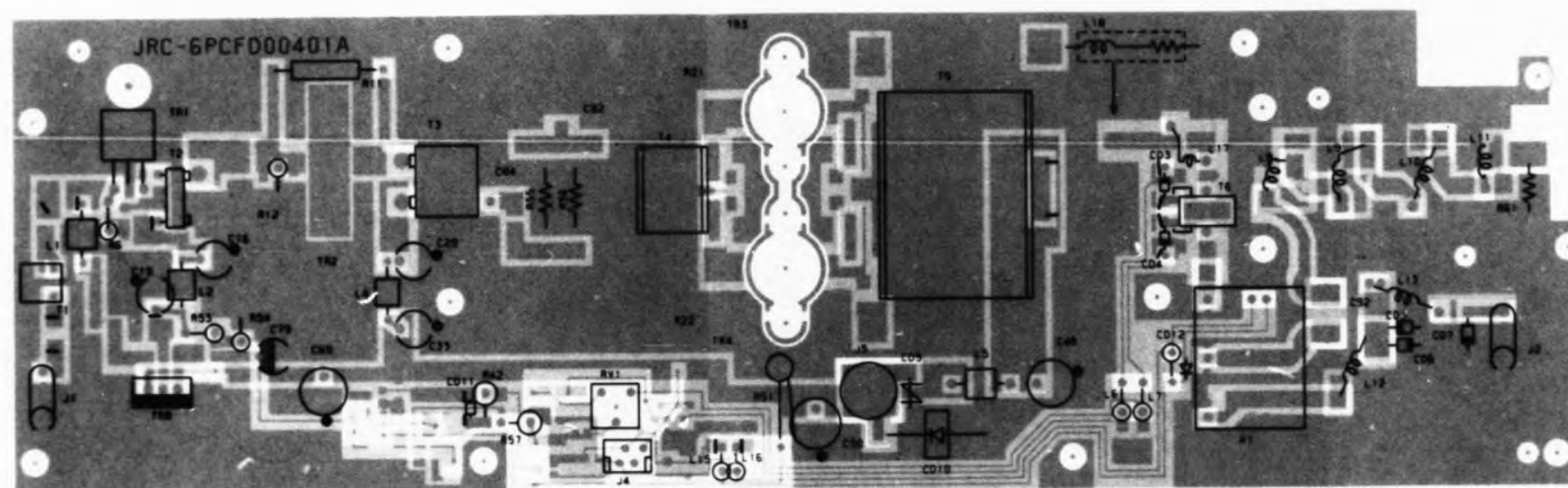
LEAD IDENTIFICATION
FOR TR 2

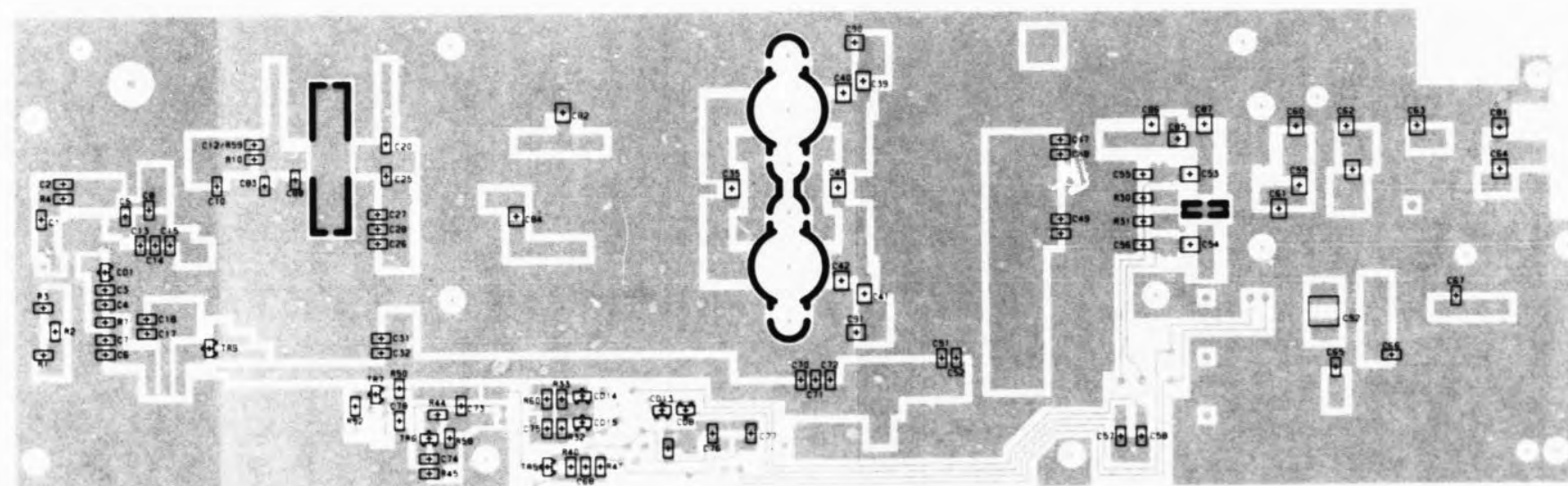


TYP LEAD TRIMMING
FOR TR 3 AND TR 4
(Used in A60 and B60)



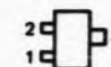
TYP LEAD TRIMMING
FOR TR 3 AND TR 4
(Used in A110 and B110)



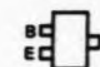


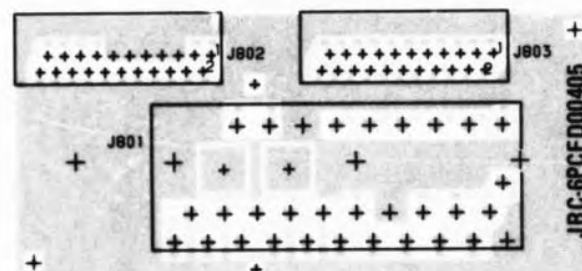
POWER AMPLIFIER BOARD
(BACK VIEW OF COMPONENT BOARD)

LEAD IDENTIFICATION
FOR CD1, CD8, CD13, CD14 and CD15
(TOP VIEW)

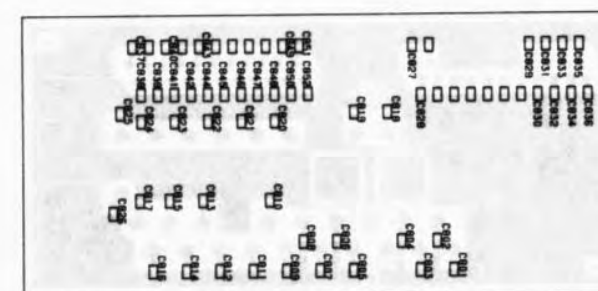
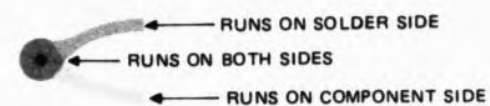


LEAD IDENTIFICATION
FOR TRANSISTORS
(TOP VIEW)





INTERFACE BOARD



INTERFACE BOARD

SYMBOL	JRC PART NO.	EQUIVALENT CIRCUIT
HC 601	JRC / 6DHFD00160	
HC 602	JRC / 6DHFD00165	
HC 603	JRC / 6DHFD00164	
HC 604	JRC / 6DHFD00167	DE-EMPHASIS

SYMBOL	JRC PART NO.	EQUIVALENT CIRCUIT
HC 605	JRC / 6DHFD00168	HPF AFH 85F 300A 4
HC 606	JRC / 6DHFD00169	LPF AFH 85F 220 C 1