GE Mobile Communications

DELTA-S,SX

CHANNEL GUARD/VOICE GUARD™ INTERFACE BOARD 19D901775G1 & G2

Maintenance Manual

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SPECIFICATIONS*

Input Voltage	9 Volts DC
Current Drain	30 Milliamperes Maximum
Programmable Digital Codes	83
Programmable Tones	33 (67-210.7 Hz) EIA Standard Tones or any tone ±0.5%
Rx Mute	Muted $\overline{<}$0.5 VDC Unmuted $\overline{>}$8.0 VDC
Encode Output Level	0-900 Millivolts P-P
Decode Response Time	250 Millisecond at 100 Hz
PTT Delay	160-190 Milliseconds
Walsh Bits	5 Volt P-P
Temperature Range	-30°C (-22°F) to +60°C (140°F)

* These specifications are intended primarily for the use of the serviceman.
Refer to the appropriate Specification Sheet for the complete specifications.

DESCRIPTION

The Channel Guard/Voice Guard Interface board is a self contained circuit board consisting of circuitry necessary to perform Channel Guard encoding/decoding and the interfacing of the Delta S/SX mobile radio to the Voice Guard unit. The board also provides protection from RF interference. The board is shipped "Voice Guard Ready" but jumpers must be moved on the board to make it "Voice Guard Operational". In addition to the moving of the jumpers, other modifications must be made to the older (floating ground) Delta S/SX T/R/S Boards. These modifications are covered in the "Modifications Section" of this manual.

The two sections will be discussed individually covering first the Channel Guard circuitry and then the Voice Guard Interface circuits.

Channel guard provides a means of restricting calls to specific radios through the use of a continuous tone or digitally coded squelch system (CTCSS or CDCSS).

The Channel guard circuitry provides amplification, filtering and limiting for the microcomputer generated Channel Guard signals. It also removes Channel Guard signals from the received audio in the decode mode.

The Voice Guard Interface section executes audio switching functions for the transmit and receive data signals and controls gating of VOL/SQ HI signals. It also switches the transmitter modulator input from the audio processor output to VG data during VG receptions.

The board is mounted inside the top cover of the radio and is connected to the T/R/S board via option connector J603. The +9 volts required for operation is supplied through J603 pin 2.

CIRCUIT ANALYSIS

CHANNEL GUARD

The tones used in the Channel Guard system range from 67 Hz to 210.7 Hz. There are 33 standard tones and 83 unique digital codes which are available. These tones/codes are identified in Tables 1 and 2.

NOTE

On radios using wideband software, any tone is available from 67.0 to 210.7 ±0.5%.

STANDARD TONE FREQUENCIES				
67.0	88.5	107.2	131.8	167.9
71.9	91.5	110.9	136.5	173.8
74.4	94.8	114.8	141.3	179.9
77.0	97.4	118.8	146.2	186.2
79.7	100.0	123.0	151.4	192.8
82.5	103.5	127.3	156.7	203.5
85.4			162.2	210.7

Table 1 - Channel Guard Tone Frequencies

The Channel Guard section contains a summing amplifier (U1A), 2-pole active voice reject filter (U2A-D), limiter (U1B,C) and tone/code reject filter (U3A,B). A TX Channel Guard disable circuit Q1 allows the Channel Guard encode to be disabled. The Channel Guard decoder is disabled via the radio microcomputer.

The microcomputer selects the assigned Channel Guard encode code/tone information from the EE PROM memory for each channel, transmit and receive, and generates the Channel Guard signal. This signal is applied as Walsh Bit 1 and 2 to summing amplifier U1A. The Walsh bits are summed together and filtered to provide a smooth sine wave for tone Channel Guard or a digital waveform for digital Channel Guard.

The switched volume/squelch Hi signal to the summing amplifier is controlled by bilateral switches U4A and B. In the encode mode DPTT is high applying A-from U4B to the control input of U4A turning it off and preventing any input from the SW Vol/Sq Hi line from interfering with the encoding signal.

The output of summing amplifier U1A is applied to buffer/amplifier U1B through a two-pole active voice reject filter consisting of U2A through D. The active filter shunts all frequencies above 300 Hz to ground, thereby preventing those frequencies from interfering with the encoded signal. The output of U1B is the assigned CG tone or digital signal. This signal is applied to the audio processor through CG deviation control R22. Channel Guard deviation is set for 0.75 kHz.

CG Decode

In the decode mode DPTT is low, turning bilateral switch U4B off, allowing the 9 V FLTRD supply to turn U4A on. Audio from the SW Vol/Sq Hi line is then applied to the summing amplifier U1A

PRIMARY CODE	EQUIVALENT CODE	PRIMARY CODE	EQUIVALENT CODE	PRIMARY CODE	EQUIVALENT CODE
023	340, 766	205	135, 610	464	237, 642, 772
025		223	350, 475, 750	465	056, 656
026	566	226	104, 557	466	144, 666
031	374, 643	243	267, 342	503	157, 312
032		244	176, 417	506	224, 313, 574
043	355	245	370, 554	516	067, 720
047	375, 707	251	236, 704, 742	532	161, 345
051	520, 771	261	227, 567	546	317, 614, 751
054	405, 675	263	213, 136	565	307, 362
065	301	265	171, 426	606	153, 630
071	603, 717, 746	271	427, 510, 762	612	254, 314, 706
072	470, 701	306	147, 303, 761	624	075, 501
073	640	311	330, 456, 561	627	037, 560
074	360, 721	315	321, 673	631	231, 504, 636 745
114	327, 615	331	372, 507	632	123, 657
115	534, 674	343	324, 570	654	163, 460, 607
116	060, 737	346	616, 635, 724	662	363, 436, 443 444
125	172	351	353, 435	664	344, 471, 715
131	572, 702	364	130, 641	703	150, 256
132	605, 634, 714	365	107	712	136, 502
134	273	371	217, 453, 530	723	235, 611, 671
143	333	411	117, 756	731	447, 473, 474 744
152	366, 415	412	127, 441, 711	732	164, 207
155	233, 660	413	133, 620	734	066
156	517, 741	423	234, 563, 621 713	743	312, 515, 663
162	416, 553	431	262, 316, 730	754	076, 203
165	354	432	276, 326		
172	057	445	222, 457, 575		
174	142, 270				

Table 2 - Primary and Equivalent Digital Codes (Octal)

through bilateral switch U4A. This signal is amplified and filtered by U1A,B and U2A-D, so that only the CG signal (if present) is applied to hard limiter U1C. The CG signal is squared up for comparison by the microcomputer to determine if the CG signal is correct. If the microcomputer determines the CG signal to be correct, RX Mute transistor Q721 (on the TRS board), is turned off applying +9 VDC to the RX MUTE line to open the receiver.

Channel Guard (CG) Disable

The CG DIS line has a double function. It can disable the encode or the decode CG function. The encode function is disabled by applying +20V or more to P1-9. This will turn on Q1 and shunt the Channel Guard tone/code to ground. To disable the decoder, ground the CG $\overline{\text{DSBL}}$ line at P1-9. The microcomputer will detect that the line is low, turn off Q721 and force the RX MUTE line high. The decode filter/limiter circuit is not affected, it continues to operate. The detection software also does not stop working.

Squelch Tail Eliminator (STE)

STE eliminates squelch tails when the radio is on hook or off hook. When Channel Guard is disabled (off hook) the decoder is still looking at the received signal. The RX MUTE line is high, as would be normally expected. The Channel Guard decoder is looking for the STE burst (phase reversal in tone Channel Guard, STE tone in Digital Channel Guard). If an STE burst is detected, the RX MUTE line will go low for about 200 ms. This will prevent the squelch tail from being heard. After 200 ms, the RX MUTE line will go high again; by now the transmission has ended and the squelch will hold the audio closed. The off hook STE does not affect the operation of the Channel Guard while on hook. Another way of looking at it: the radio will go quiet for 200 ms any time STE is detected. If it was on hook it will stay quiet after the 200 ms, if it was off hook it will revert to noise squelch operation.

Digital Channel Guard Polarity\Inversion

In some instances it is necessary to invert the polarity of the digital Channel Guard signal to enhance system compatability. Inverted polarity normally results in a wrong code or one that cannot be used. When this occurs on decode, move P2 to J2-2,3. The encode DCG codes may be inverted by moving P5 to J5-2,3.

VOICE GUARD INTERFACE

For Voice Guard applications, jumpers P6 and P7 should be moved to pins 2 and 3, and W1 should be connected to J612 on the Delta S/SX T/R/S board. The white wire connects to pin 2 and the black wire to pin 1.

The VOICE GUARD^{TM} interface section multiplexes transmit and receive data signals to the VG unit via one shielded cable (VG DATA HI). The encrypted data to be transmitted is injected into the radio transmitter modulator by J612. The clear (un-encrypted) transmit data is routed through the interface board also by J612.

Audio signals are controlled by two logic signals from the VG unit, TX SW and DATA PTT. The VG unit sets TX SW to logic 1 (approx. 4 VDC) during VG transmission or reception, and sets DATA PTT to logic 0 (<4 VDC) during VG transmission.

Clear Voice Receive (OFF)

When the VG unit is turned off the un-encrypted audio is routed from system board connector P1-14 via jumper to bilateral switch U52C on the interface board. U52C is enabled by the high logic level supplied by the logic switching circuits. The switched VOL/SQ HI signal from U52C is applied to unity gain op amp U51B. The output of U51B is routed to the channel guard section (P1-14) and jumper J6.

The channel guard circuit will return the signal (filtered) on P1-13 which is connected to the control unit VOL/SQ HI by jumpers in the radio.

Guarded RX

When the guarded receive mode of operation is selected, the TX SW line changes from a low logic level to a high level. This causes the logic switching circuits to apply a low level to the control pin of U52C, disabling VOL/SQ HI to the control unit during VG reception.

The received encrypted audio is applied to bilateral switch U52D and coupled to P11-1. The signal is then coupled through J601-26 to the VG unit.

Clear TX

In the clear transmit mode, transmit audio from the audio processor circuit of the radio is routed through the interface board via J53-2 (J612-1 system board). The signal is applied to buffer U51D and then to bilateral switch U2A.

The control pin of U2A is now at a high level. The un-encrypted transmit audio signal is coupled from U2A to buffer U51A. The signal is then injected into the modulator circuit through J53-1 (J612-2 system board).

Guarded TX

During the guarded transmit mode a low logic level is applied to the control pin of U52D disabling any receive audio signal from reaching the transmit line.

VG data is applied to J601-26 and is coupled through buffer U51C to bilateral switch U52B. U52B is now enabled and applies the signal to R62. R61 provides an adjustment of transmit data deviation. (Refer to Maintenance Manual Adjustment Procedure.) Op amp U51A buffers the signal before it is applied to the radio modulator.

U52A is disabled during the transmission of VG data. This prevents any un-encrypted transmit audio signals and channel guard from reaching the radio modulator.

MODIFICATIONS FOR VOICE GUARD

When an older styled Delta S/SX radio (radios with floating ground) is upgraded for Voice Guard operation, modifications must be made to the T/R/S board in the radio to make it compatible with the Channel Guard/Voice Guard Interface board. On radios that previously had no option boards, extender board 19B800739G1 must be installed on J603. Radios having Channel Guard and/or MASTR II Interface boards must first have these removed. The modifications are covered in more detail on the modification instructions drawing included in this manual.

GE Mobile Communications

General Electric Company
Lynchburg, Virginia 24502

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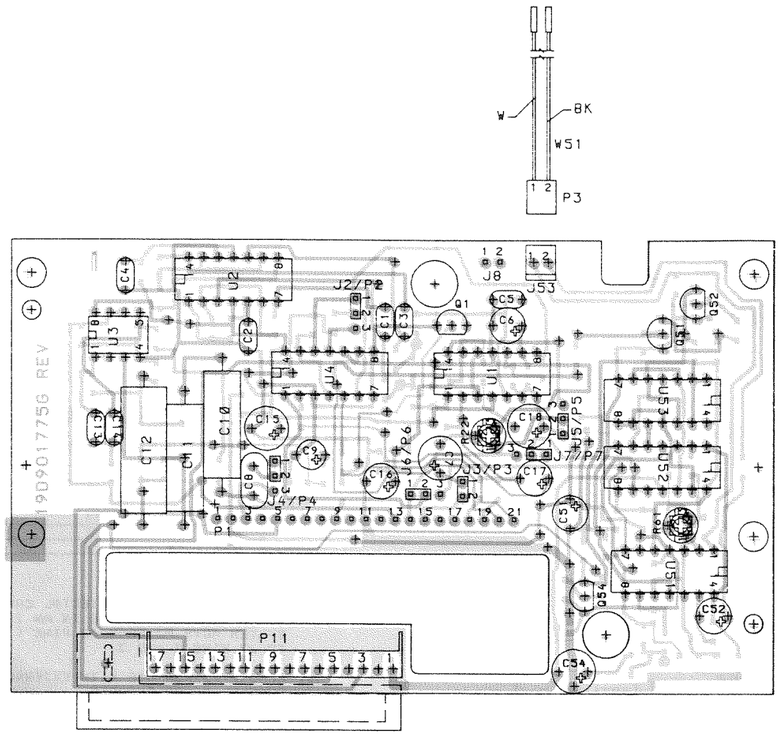
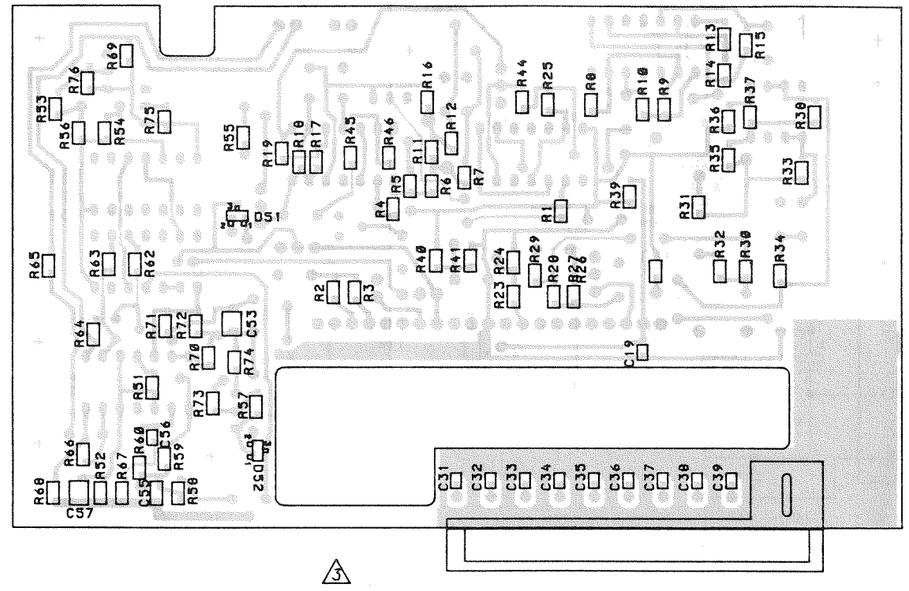
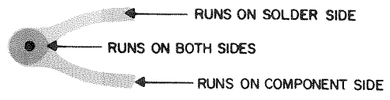


(19D901776, Sh.1, Rev.0)
(19A704992, Sh. 1, Rev. 1)
(19A704992, Sh. 2, Rev. 1)



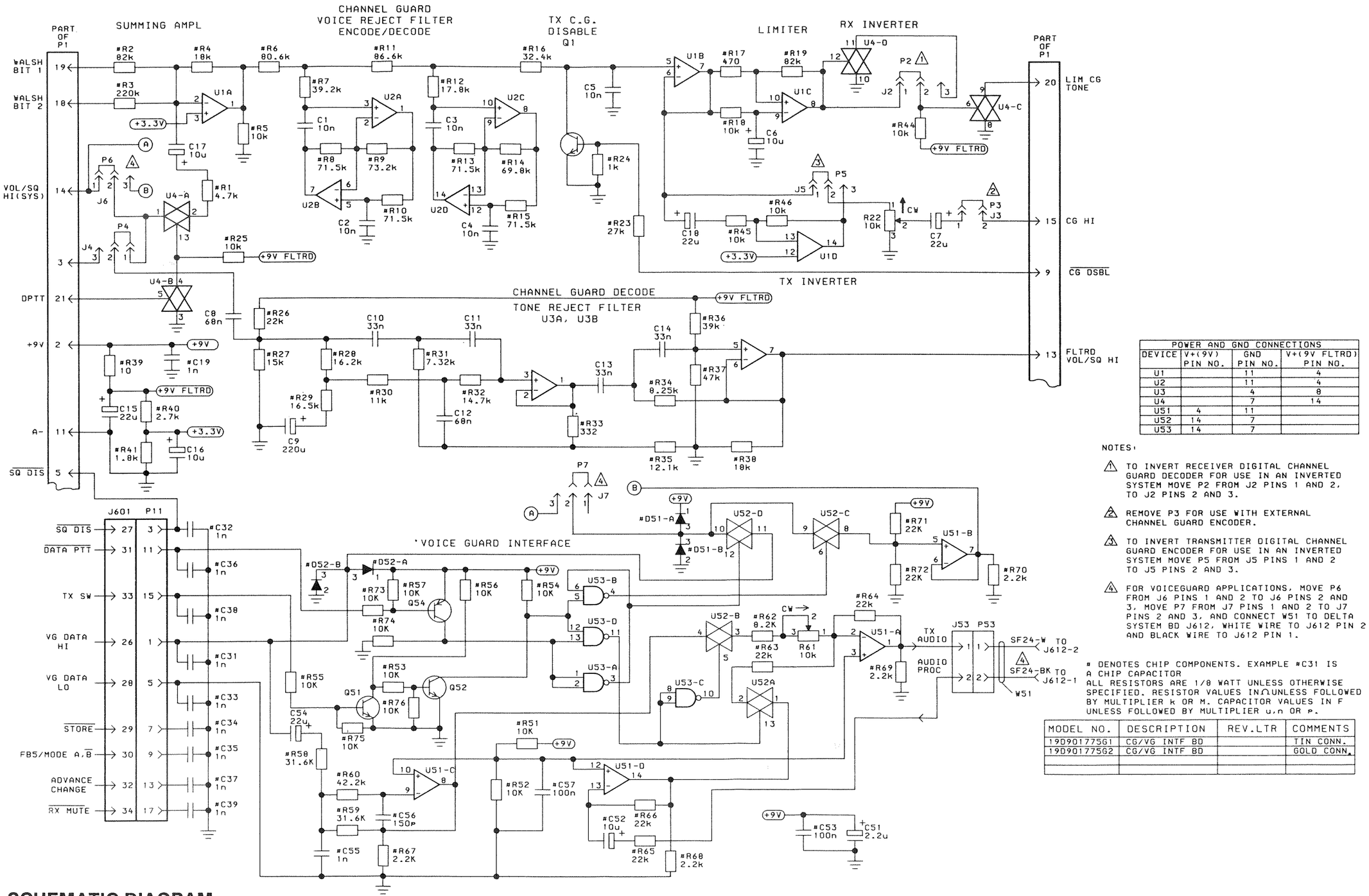
CHIPS AS VIEWED FROM SOLDER SIDE OF BOARD

(19D901775, Sh. 1, Rev. 2)
(19A704992, Sh. 2, Rev. 1)



OUTLINE DIAGRAM

DELTA CHANNEL GUARD/
VOICE GUARD INTERFACE BOARD



POWER AND GND CONNECTIONS			
DEVICE	V+(9V) PIN NO.	GND PIN NO.	V+(9V FLTRD) PIN NO.
U1		11	4
U2		11	4
U3		4	8
U4		7	14
U51	4	11	
U52	14	7	
U53	14	7	

NOTES:

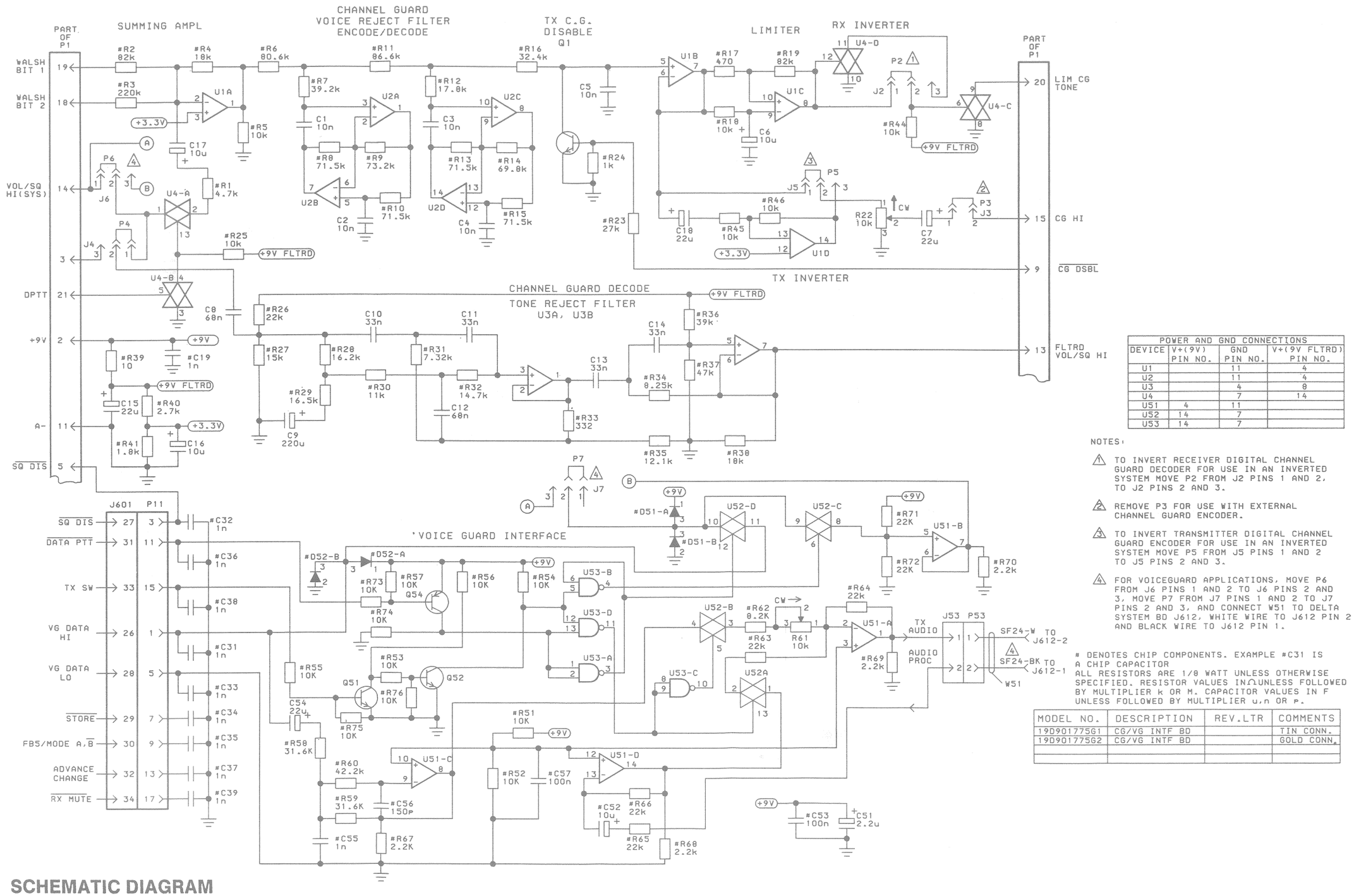
1. TO INVERT RECEIVER DIGITAL CHANNEL GUARD DECODER FOR USE IN AN INVERTED SYSTEM MOVE P2 FROM J2 PINS 1 AND 2, TO J2 PINS 2 AND 3.
2. REMOVE P3 FOR USE WITH EXTERNAL CHANNEL GUARD ENCODER.
3. TO INVERT TRANSMITTER DIGITAL CHANNEL GUARD ENCODER FOR USE IN AN INVERTED SYSTEM MOVE P5 FROM J5 PINS 1 AND 2 TO J5 PINS 2 AND 3.
4. FOR VOICEGUARD APPLICATIONS, MOVE P6 FROM J6 PINS 1 AND 2 TO J6 PINS 2 AND 3, MOVE P7 FROM J7 PINS 1 AND 2 TO J7 PINS 2 AND 3, AND CONNECT W51 TO DELTA SYSTEM BD J612, WHITE WIRE TO J612 PIN 2 AND BLACK WIRE TO J612 PIN 1.

# DENOTES CHIP COMPONENTS. EXAMPLE #C31 IS A CHIP CAPACITOR
ALL RESISTORS ARE 1/8 WATT UNLESS OTHERWISE SPECIFIED. RESISTOR VALUES IN Ω UNLESS FOLLOWED BY MULTIPLIER k OR M. CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER u,n OR p.

MODEL NO.	DESCRIPTION	REV.LTR	COMMENTS
19D901775G1	CG/VG INTF BD		TIN CONN.
19D901775G2	CG/VG INTF BD		GOLD CONN.

SCHEMATIC DIAGRAM

(19D901777, Rev. 2)



POWER AND GND CONNECTIONS			
DEVICE	V+(9V) PIN NO.	GND PIN NO.	V+(9V FLTRD) PIN NO.
U1		11	4
U2		11	4
U3		4	8
U4		7	14
U51	4	11	
U52	14	7	
U53	14	7	

NOTES:

1. TO INVERT RECEIVER DIGITAL CHANNEL GUARD DECODER FOR USE IN AN INVERTED SYSTEM MOVE P2 FROM J2 PINS 1 AND 2, TO J2 PINS 2 AND 3.
2. REMOVE P3 FOR USE WITH EXTERNAL CHANNEL GUARD ENCODER.
3. TO INVERT TRANSMITTER DIGITAL CHANNEL GUARD ENCODER FOR USE IN AN INVERTED SYSTEM MOVE P5 FROM J5 PINS 1 AND 2 TO J5 PINS 2 AND 3.
4. FOR VOICEGUARD APPLICATIONS, MOVE P6 FROM J6 PINS 1 AND 2 TO J6 PINS 2 AND 3, MOVE P7 FROM J7 PINS 1 AND 2 TO J7 PINS 2 AND 3, AND CONNECT W51 TO DELTA SYSTEM BD J612, WHITE WIRE TO J612 PIN 2 AND BLACK WIRE TO J612 PIN 1.

# DENOTES CHIP COMPONENTS. EXAMPLE #C31 IS A CHIP CAPACITOR
ALL RESISTORS ARE 1/8 WATT UNLESS OTHERWISE SPECIFIED. RESISTOR VALUES IN Ω UNLESS FOLLOWED BY MULTIPLIER k OR M. CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER u,n OR p.

MODEL NO.	DESCRIPTION	REV.LTR	COMMENTS
19D901775G1	CG/VG INTF BD		TIN CONN.
19D901775G2	CG/VG INTF BD		GOLD CONN.

SCHEMATIC DIAGRAM

Hi BAND NARROW BAND DELTA RADIO WITH VOICE GUARD

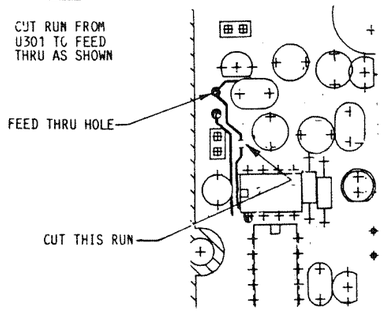
SYSTEM BOARD ASM: 19D900840
LEVEL ONE ASM: 19D900951

UHF NARROW BAND DELTA RADIO WITH VOICE GUARD

SYSTEM BOARD ASM: 19D900775
LEVEL ONE ASM: 19D900920

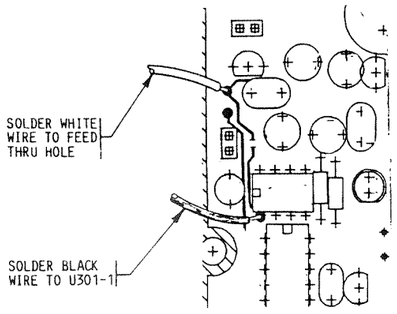
1

CUT RUN FROM U301 TO FEED THRU AS SHOWN



2

CUT OFF TERMINALS ON BLACK & WHITE WIRES



3

PLUG P3 OF W51 ONTO J53 OF VG BOARD.

Hi BAND WIDE BAND DELTA RADIO WITH VOICE GUARD

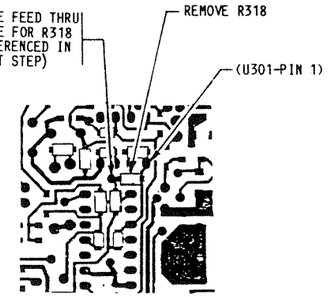
SYSTEM BOARD ASM: 19D901167
LEVEL ONE ASM: 19D901228

UHF WIDE BAND DELTA RADIO WITH VOICE GUARD

SYSTEM BOARD ASM: 19D901260
LEVEL ONE ASM: 19D901323

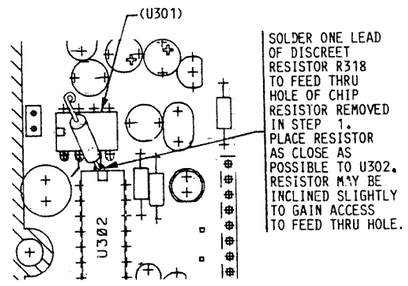
1

REMOVE R318 CHIP RESISTOR FROM SOLDER SIDE



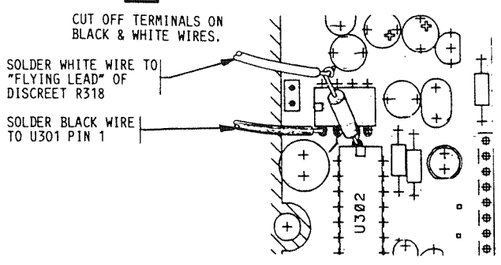
2

SOLDER ONE LEAD OF DESCREET RESISTOR R318 GE PT. NO. 19A701250P151 323 Ω , 1/4 W TO FEED THRU HOLE FOR R318



3

CUT OFF TERMINALS ON BLACK & WHITE WIRES.



4

PLUG P3 OF W51 ONTO J53 OF VG BD.

Hi BAND NARROW BAND DELTA RADIO WITH VOICE GUARD

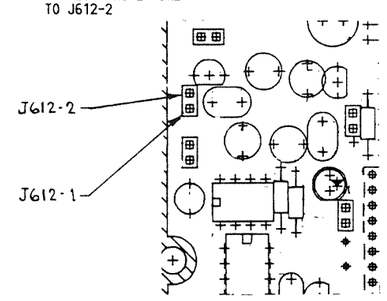
SYSTEM BOARD ASM: 19D901345
LEVEL ONE ASM: 19D901720

UHF NARROW BAND DELTA RADIO WITH VOICE GUARD

SYSTEM BOARD ASM: 19D901350
LEVEL ONE ASM: 19D901620

1

REMOVE P612
CONNECT BLACK WIRE TO J612-1
CONNECT WHITE WIRE TO J612-2



2

PLUG P3 OF W51 ONTO J53 OF VG BOARD.

Hi BAND WIDE BAND DELTA RADIO WITH VOICE GUARD

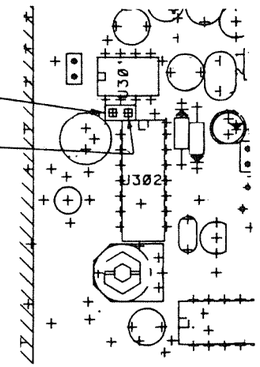
SYSTEM BOARD ASM: 19D901645
LEVEL ONE ASM: 19D901650

UHF WIDE BAND DELTA RADIO WITH VOICE GUARD

SYSTEM BOARD ASM: 19D901665
LEVEL ONE ASM: 19D901670

1

REMOVE P612
CONNECT BLACK WIRE TO J612-1
CONNECT WHITE WIRE TO J612-2

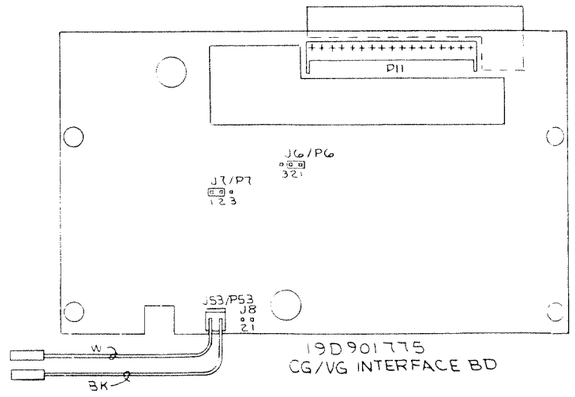


2

PLUG P3 OF W51 ONTO J53 OF VG BOARD.

(37) VOICE GUARD APPLICATION

- MOVE P6 FROM J6-182 TO J6-283
- MOVE P7 FROM J7-182 TO J7-283
- CONNECT BLACK AND WHITE WIRES OF W51 AS SHOWN DEPENDING ON RADIO BAND / SYSTEM BOARD.



MODIFICATION INSTRUCTIONS

T/R/S Board

PARTS LIST

CHANNEL GUARD/VOICE GUARD INTERFACE BOARD
19D901775G1
19D901775G2 (GOLD CONTACTS)
ISSUE 2

SYMBOL	GE PART NO.	DESCRIPTION
		NOTE: WHEN REPLACING BOARDS, CARE SHOULD BE TAKEN TO ASSURE THAT BOARDS WITH GOLD CONTACTS ARE NOT INTERMIXED WITH BOARDS HAVING TIN CONTACTS. REPLACE THE BOARD ONLY WITH ONE HAVING THE SAME GROUP NUMBER AS THE ORIGINAL.
		- - - - - - - - - - CAPACITORS - - - - - - - - - -
C1 thru C5	T644ACP310J	Polyester: .010 uF ±5%, 50 VDCW.
C6	19A701534P7	Tantalum: 10 uF ±20%, 16 VDCW.
C7	19A701534P8	Tantalum: 22 uF ±20%, 16 VDCW.
C8	T644ACP368J	Polyester: .068 uF ±5%, 50 VDCW.
C9	19A701534P2	Tantalum: 0.22 uF ±20%, 35 VDCW.
C10 and C11	19A701594P1	Polyester: 0.033 uF ±2%, 100 VDCW.
C12	19A701594P2	Polyester: 0.068 uF ±20%, 100 VDCW.
C13 and C14	T644ACP333J	Polyester: .033 uF ±5%, 50 VDCW.
C15	19A701534P8	Tantalum: 22 uF ±20%, 16 VDCW.
C16 and C17	19A701534P7	Tantalum: 10 uF ±20%, 16 VDCW.
C18	19A701534P8	Tantalum: 22 uF ±20%, 16 VDCW.
C19	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C31 thru C39	19A702052P5	Ceramic: 1000 pF ±10%, 50 VDCW.
C51	19A701534P5	Tantalum: 2.2 uF, ±20%, 35 VDCW.
C52	19A701534P7	Tantalum: 10 uF ±20%, 16 VDCW.
C53	19A702052P26	Ceramic: 0.1 uF ±10%, 50 VDCW.
C54	19A701534P8	Tantalum: 22 uF ±20%, 16 VDCW.
C55	19A702061P99	Ceramic: 1000 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C56	19A702061P65	Ceramic: 150 pF ±5%, 50 VDCW, temp coef 0 ±30 PPM/°C.
C57	19A702052P26	Ceramic: 0.1 uF ±10%, 50 VDCW.
		- - - - - - - - - - DIODES - - - - - - - - - -
D51 and D52	19A700053P2	Silicon, fast recovery (2 diodes in series).
		- - - - - - - - - - JACKS - - - - - - - - - -
J2 thru J8	19A703248P3	Contact, electrical. (Group 1 only).
J2 thru J8	19A703248P13	Contact, electrical. (Gold Contacts - Group 2 only).
J53	19A700072P28	Printed wire: 2 contacts rated @ 2.5 amps; sim to Molex 22-27-2021. (Group 1 only).
J53	19A704852P28	Printed wire: 2 contacts arated @ 2.5 amps. (Gold Contacts - Group 2 only).
		- - - - - - - - - - PLUGS - - - - - - - - - -
P1	19A703248P3	Contact, electrical. (Group 1 only).
P1	19A703248P13	Contact, electrical. (Gold Contacts - Group 2 only).
P2 thru P7	19A702104P1	Receptacle: 2 position, shorting, rated at 3 amps; sim to Berg 65474-002. (Group 1 only).
P2 thru P7	19A702104P2	Receptacle: gold plated, two position shorting; sim to Berg 65474-003. (Gold Contacts - Group 2 only).
P11	19A700041P66	Printed wire: 17 circuits rated at 2.5 amps each; sim to Molex 22-02-2175.
		- - - - - - - - - - TRANSISTORS - - - - - - - - - -
Q1	19A700023P2	Silicon, NPN: sim to 2N3904.
Q51 and Q52	19A700023P2	Silicon, NPN: sim to 2N3904.
Q54	19A700022P2	Silicon, PNP: sim to 2N3906.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1	19B800607P472	Metal film: 4.7K ohms ±5%, 200 VDCW, 1/8 w.
R2	19B800607P823	Metal film: 82K ohms ±5%, 200 VDCW, 1/8 w.
R3	19B800607P224	Metal film: 220K ohms ±5%, 200 VDCW, 1/8 w.
R4	19B800607P183	Metal film: 18K ohms ±5%, 200 VDCW, 1/8 w.
R5	19B800607P103	Metal film: 10K ohms ±5%, 200 VDCW, 1/8 w.
R6	19A702931P388	Metal film: 80.6K ohms ±1%, 200 VDCW, 1/8 w.
R7	19A702931P358	Metal film: 39.2K ohms ±1%, 200 VDCW, 1/8 w.
R8	19A702931P383	Metal film: 71.5K ohms ±1%, 200 VDCW, 1/8 w.
R9	19A702931P384	Metal film: 73.2K ohms ±1%, 200 VDCW, 1/8 w.
R10	19A702931P383	Metal film: 71.5K ohms ±1%, 200 VDCW, 1/8 w.
R11	19A702931P391	Metal film: 86.6K ohms ±1%, 200 VDCW, 1/8 w.
R12	19A702931P325	Metal film: 17.8K ohms ±1%, 200 VDCW, 1/8 w.
R13	19A702931P383	Metal film: 71.5K ohms ±1%, 200 VDCW, 1/8 w.
R14	19A702931P382	Metal film: 69.8K ohms ±1%, 200 VDCW, 1/8 w.
R15	19A702931P383	Metal film: 71.5K ohms ±1%, 200 VDCW, 1/8 w.
R16	19A702931P350	Metal film: 32.4K ohms ±1%, 200 VDCW, 1/8 w.
R17	19B800607P471	Metal film: 470 ohms ±5%, 200 VDCW, 1/8 w.
R18	19B800607P103	Metal film: 10K ohms ±5%, 200 VDCW, 1/8 w.
R19	19B800607P823	Metal film: 82K ohms ±5%, 200 VDCW, 1/8 w.
R22	19B800779P10	Variable: 10K ohms ±25%, 100 VDCW, .3 watt.
R23	19B800607P273	Metal film: 27K ohms ±5%, 200 VDCW, 1/8 w.
R24	19B800607P102	Metal film: 1K ohms ±5%, 200 VDCW, 1/8 w.
R25	19B800607P103	Metal film: 10K ohms ±5%, 200 VDCW, 1/8 w.
R26	19B800607P223	Metal film: 22K ohms ±5%, 200 VDCW, 1/8 w.
R27	19B800607P153	Metal film: 15K ohms ±5%, 200 VDCW, 1/8 w.
R28	19A702931P321	Metal film: 16.2K ohms ±1%, 200 VDCW, 1/8 w.
R29	19A702931P322	Metal film: 16.5K ohms ±1%, 200 VDCW, 1/8 w.
R30	19A702931P305	Metal film: 11K ohms ±1%, 200 VDCW, 1/8 w.
R31	19A702931P284	Metal film: 7320 ohms ±1%, 200 VDCW, 1/8 w.
R32	19A702931P317	Metal film: 14.7K ohms ±1%, 200 VDCW, 1/8 w.
R33	19A702931P151	Metal film: 332 ohms ±1%, 250 VDCW, 1/8 w.
R34	19A702931P289	Metal film: 8250 ohms ±1%, 200 VDCW, 1/8 w.
R35	19A702931P309	Metal film: 12.1K ohms ±1%, 200 VDCW, 1/8 w.
R36	19B800607P393	Metal film: 39K ohms ±5%, 200 VDCW, 1/8 w.
R37	19B800607P473	Metal film: 47K ohms ±5%, 200 VDCW, 1/8 w.
R38	19B800607P183	Metal film: 18K ohms ±5%, 200 VDCW, 1/8 w.
R39	19B800607P100	Metal film: 10 ohms ±5%, 200 VDCW, 1/8 w.
R40	19B800607P272	Metal film: 2.7K ohms ±5%, 200 VDCW, 1/8 w.
R41	19B800607P182	Metal film: 1.8K ohms ±5%, 200 VDCW, 1/8 w.
R44 thru R46	19B800607P103	Metal film: 10K ohms ±5%, 200 VDCW, 1/8 w.
R51 thru R57	19B800607P103	Metal film: 10K ohms ±5%, 200 VDCW, 1/8 w.
R58 and R59	19A702931P349	Metal film: 31.6K ohms ±1%, 200 VDCW, 1/8 w.
R60	19A702931P361	Metal film: 42.2K ohms ±1%, 200 VDCW, 1/8 w.
R61	19B800779P10	Variable: 10K ohms ±25%, 100 VDCW, .3 watt.
R62	19B800607P822	Metal film: 8.2K ohms ±5%, 200 VDCW, 1/8 w.
R63 thru R66	19B800607P223	Metal film: 22K ohms ±5%, 200 VDCW, 1/8 w.
R67 thru R70	19B800607P222	Metal film: 2.2K ohms ±5%, 200 VDCW, 1/8 w.
R71 and R72	19B800607P223	Metal film: 22K ohms ±5%, 200 VDCW, 1/8 w.
R73 thru R76	19B800607P103	Metal film: 10K ohms ±5%, 200 VDCW, 1/8 w.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - - -
U1 and U2	19A701789P1	Linear, Low Power OP AMP; sim to LM324N.
U3	19A701789P2	DUAL OP AMP; sim to LM358.
U4	19A700029P44	Digital: BILATERAL SWITCH.
U51	19A701789P1	Linear, Low Power OP AMP; sim to LM324N.
U52	19A700029P44	Digital: BILATERAL SWITCH.
U53	19A700029P7	Digital: QUAD 2-INPUT NAND GATE.
		- - - - - - - - - - CABLES - - - - - - - - - -
W51	19A149188G1	Interconnect Cable.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES