GE MOBILE RADIO

29.7-50 MHz NOISE BLANKER

JRC/CFR-72

DESCRIPTION

The noise blanker option for the RANGR synthesized radio consists of a plug-in printed wire board which plugs into J502 on the Receiver Board. The noise blanker is designed to improve receiver performance by blanking out impulse noise emanating from the alternator, ignition system, etc. This is accomplished by delaying the IF signal for 200 nanoseconds while generating a blanking gate (pulse) having the same characteristics as the noise pulses. These blanking pulses then are used to turn off the delayed IF signal precisely where the noise occurs, resulting in noise-free audio reception.

The noise blanker may be disabled, if desired, by relocating a ground plug P501 on the Receiver board and P707 on the System Control board. An alternate method (if the noise blanker is to be permanently disabled) is to remove the noise blanker board from the radio, reconnect W402 and remove TR501 and TR502 on the receiver board. The alternate method results in improved intermodulation performance.

INSTALLATION

The noise blanker plugs into J502 on the Receiver unit. If the board is installed after the receiver has been aligned (or installed in the field), cut jumper wire W402 on the Receiver board. Be sure that P501 is plugged into J503-2, 3 and P707 is plugged into J707-2, 3 on the System Control board. Refer to Receiver Alignment Procedure in the Service Section of the Maintenance Manual (Preliminary Checks and Adjustment) and tune accordingly.

─────── NOTE ───────

If the noise blanker is installed prior to receiver alignment, simply plug the noise blanker into J503 and perform standard receiver Alignment Procedures. Be sure P501 is plugged into J503-2, 3 on the receiver board and P707 is plugged into J707-2, 3 on the System Control board.

GENERAL ELECTRIC

The noise blanker consists of a 200 ns fixed delay line, three pulse amplifiers, a pulse amplifier/limiter, gate driver and blanker disable switch as shown in Figure 1.

The 20.8 MHz IF signal from JFET buffer TR402/403 on the Receiver board is applied to gate 1 of pulse amplifier TR1 and to delay line Z1. Z1 delays the IF signal by 200 ns and returns it to the two JFET gating switches on the receiver board. The undelayed IF signal is amplified by pulse amplifier TR1. TR1 provides approximately 20 dB of amplification. Bias for TR1 is established by R1, R2. The IF output of TR1 is further amplified and limited by pulse amplifier/limiter IC1. IC1 provides approximately 50 dB of amplification.

The output of the limiter is applied to pulse detector TR2. DC bias for TR2 is set at the threshold of conduction so that all noise pulses regardless of magnitude or duration will be detected.

Threshold bias is established by R8-R11, and CD1. R9 is a negative temperature compensating resistor whose temperature characteristics complement IC1 to adjust the threshold level of TR2 with changes in temperature.

The detected pulse is taken from the collector of TR2 and further amplified by pulse amplifiers TR3 and TR5. C14 in the emitter circuit of TR3 provides a low frequency bypass to ground and also maintains a full charge to allow TR3 to be switched on and off more rapidly. The output of pulse amplifier TR5 is applied to gate driver TR6. TR6 provides drive to operate the two JFET switches (TR501 TR502) located just ahead of the crystal filters on the Receiver board. The delayed IF signal from delay line Z1 arrives at TR501 and TR502 at the same time as the gating pulses from the blanker switch. The gating pulse switches TR501 and TR502 on coincident with the noise pulses on the IF signal, shunting all noise pulses to ground.

BLANKER DISABLE

Two blanker disable inputs are provided to assure complete turn off of the noise blanker function while allowing the delayed IF signal to be processed through the receiver. BLKR DIS 1 is applied to pulse amplifier TR1 gate 2. This will nearly turn off TR1. BLKR DIS 2 is applied to the base of TR4 turning it on. TR4 shorts the emitter and collector of pulse amplifier TR3, preventing any remaining noise pulses from passing.
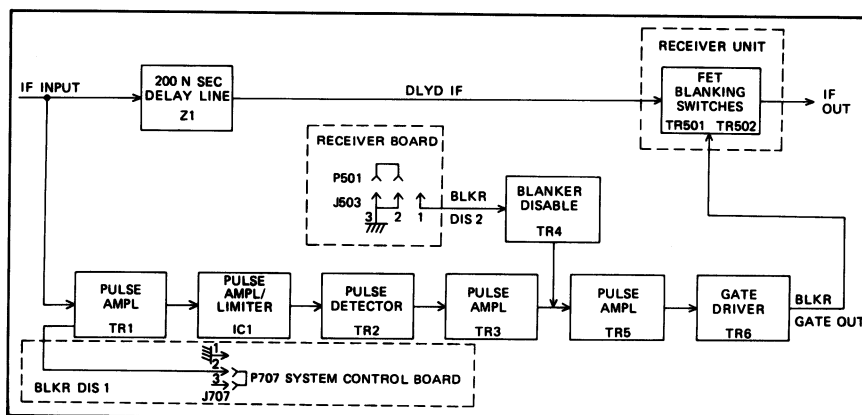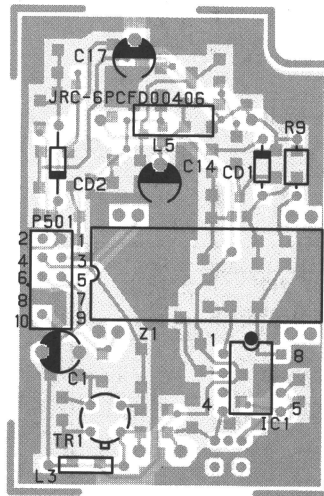

Figure 1

GENERAL ⟨GE⟩ ELECTRIC*

U.S.A.

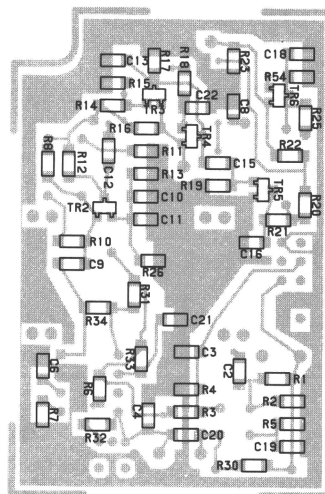* Trademark of General Electric Company U.S.A.
Printed in JAPAN

NOISE BLANKER BOARD

←— RUNS ON SOLDER SIDE

←— RUNS ON BOTH SIDES

←— RUNS ON COMPONENT SIDE
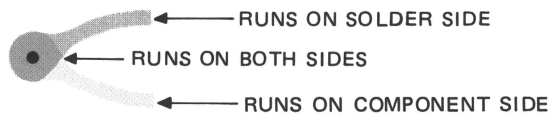
NOISE BLANKER BOARD
(BACK VIEW OF COMPONENT BOARD)
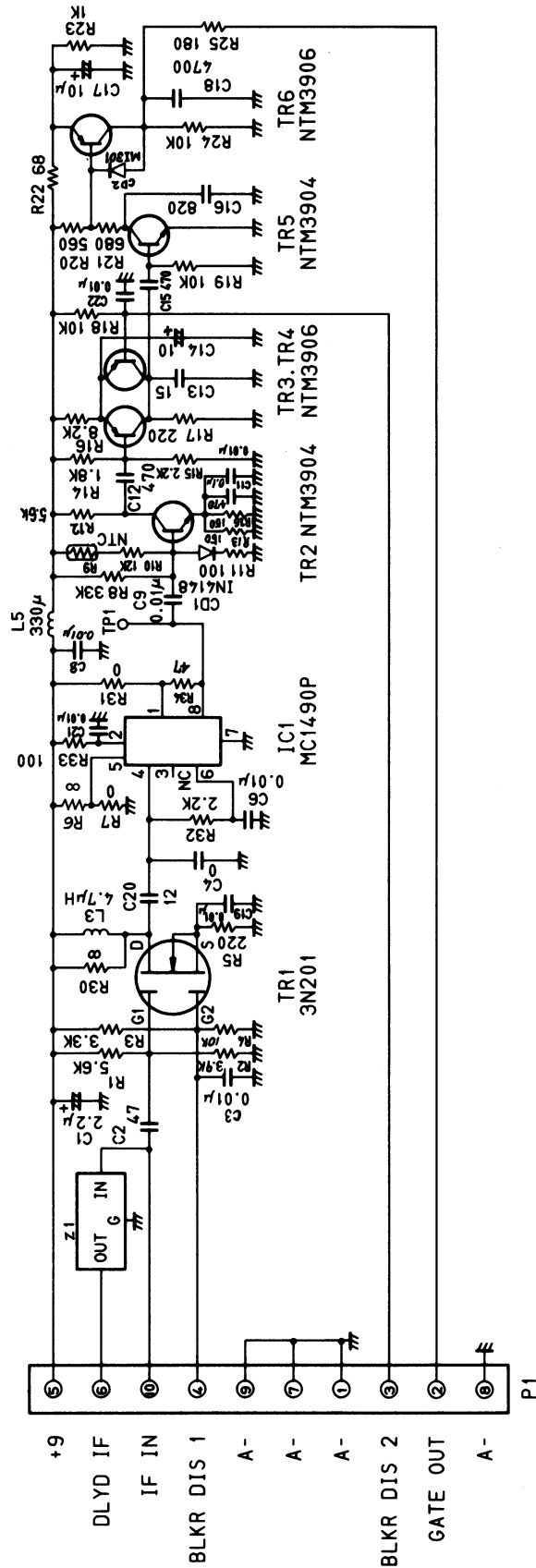
SCHEMATIC DIAGRAM NOISE BLANKER
DD00-CFR-72

SYMBOL	PART NO.	DESCRIPTION
C1	JRC/5CSAC00826	Tantalum: 2.2µF ±20%, 25VDCW
C2	JRC/5CAAD00864	Ceramic: 47pF ±5%, 50VDCW, temp coef 0±60ppm.
C3	JRC/5CAAD00877	Ceramic: 0.01µF ±10%, 25VDCW, temp coef ±10%.
C6	JRC/5CAAD00877	Ceramic: 0.01µF ±10%, 25VDCW, temp coef ±15%.
C8 and C9	JRC/5CAAD00877	Ceramic: 0.01µF ±10%, 25VDCW, temp coef ±15%.
C10	JRC/5CAAD00797	Ceramic: 470pF ±5%, 50VDCW, temp coef 0±60ppm.
C11	JRC/5CAAD01237	Ceramic: 0.1µF ±10%, 25VDCW, temp coef ±15%.
C12	JRC/5CAAD00797	Ceramic: 470pF ±5%, 50VDCW, temp coef 0±60ppm.
C13	JRC/5CAAD00787	Ceramic: 15pF ±5%, 50VDCW, temp coef 0±60ppm.
C14	JRC/5CSAD00326	Tantalum: 10µF ±20%, 16VDCW.
C15	JRC/5CAAD00797	Ceramic: 470pF ±5%, 50VDCW, temp coef 0±60ppm.
C16	JRC/5CAAD01068	Ceramic: 820pF ±5%, 50VDCW, temp coef +350 -1000ppm.
C17	JRC/5CSAC00326	Tantalum: 10µF ±20%, 16VDCW.
C18	JRC/5CAAD00783	Ceramic: 4700pF ±10%, 50VDCW, temp coef ±10%.
C19	JRC/5CAAD00877	Ceramic: 0.01µF ±10%, 25VDCW, temp coef ±10%.
C20	JRC/5CAAD00784	Ceramic: 12pF ±5%, 50VDCW, temp coef ±10%.
C21 and C22	JRC/5CAAD00789	Ceramic: 0.01µF ±10%, 25VDCW, temp coef ±10%.
CD1	JRC/5TXDA00001	Silicon, rectifier: Sim to Thomson 1N4148.
CD2	JRC/5TXAR00004	Silicon, RF switching: sim to Mitsubishi: MI301.
IC1	JRC/5DAAJ00341	Linear, Wide band amplifier: sim to Motorola MC1490P.
L3	JRC/5LCAC00421	Choke coil: 4.7µH ±10%.
L5	JRC/5LCAC00206	Choke coil: 330µH ±10%.
P1	JRC/5JFAL00010	Connector.
PC1	JRC/6PCFD00406	Printed wiring board.
R1	JRC/5REAG00625	Metal film: 5.6K ohms ±5%, ±200VDCW, 1/8W.
R2	JRC/5REAG00624	Metal film: 3.9K ohms ±5%, ±200VDCW, 1/8W.
R3	JRC/5REAG00589	Metal film: 3.3K ohms ±5%, ±200VDCW, 1/8W.
R4	JRC/5REAG00576	Metal film: 10K ohms ±5%, ±200VDCW, 1/8W.
R5	JRC/5REAG00594	Metal film: 220 ohms ±5%, ±200VDCW, 1/8W.

SYMBOL	PART NO.	DESCRIPTION
R7	JRC/5REAG00590	0 ohms
R8	JRC/5REAG00592	Metal film: 33K ohms ±5%, ±200VDCW, 1/8W.
R9	JRC/5RZBX00002	Thermistor.
R10	JRC/5REAG00681	Metal film: 12K ohms ±5%, 200VDCW, 1/8W.
R11	JRC/5REAG00586	Metal film: 100 ohms ±5%, 200VDCW, 1/8W.
R12	JRC/5REAG00625	Metal film: 5.6K ohms ±5%, 200VDCW, 1/8W.
R13	JRC/5REAG00583	Metal film: 150 ohms ±5%, 200VDCW, 1/8W.
R14	JRC/5REAG00582	Metal film: 1.8K ohms ±5%, 200VDCW, 1/8W.
R15	JRC/5REAG00575	Metal film: 2.2K ohms ±5%, 200VDCW, 1/8W.
R16	JRC/5REAG00584	Metal film: 8.2K ohms ±5%, 200VDCW, 1/8W.
R17	JRC/5REAG00594	Metal film: 220 ohms ±5%, 200VDCW, 1/8W.
R18 and R19	JRC/5REAG00576	Metal film: 10K ohms ±5%, 200VDCW, 1/8W.
R20	JRC/5REAG00571	Metal film: 560 ohms ±5%, 200VDCW, 1/8W.
R21	JRC/5REAG00591	Metal film: 680 ohms ±5%, 200VDCW, 1/8W.
R22	JRC/5REAG00621	Metal film: 68 ohms ±5%, 200VDCW, 1/8W.
R23	JRC/5REAG00572	Metal film: 1K ohms ±5%, 200VDCW, 1/8W.
R24	JRC/5REAG00576	Metal film: 10K ohms ±5%, 200VDCW, 1/8W.
R25	JRC/5REAG00908	Metal film: 180 ohms ±5%, 200VDCW, 1/8W.
R26	JRC/5REAG00583	Metal film: 150 ohms ±5%, 200VDCW, 1/8W.
R31	JRC/5REAG00590	0 ohms
R32	JRC/5REAG00575	Metal film: 2.2K ohms ±5%, 200VDCW, 1/8W.
R33	JRC/5REAG00586	Metal film: 100 ohms ±5%, 200VDCW, 1/8W.
R34	JRC/5REAG00580	Metal film: 47 ohms ±5%, 200VDCW, 1/8W.
TR1	JRC/5TCAS00032	N-channel dual gate (MOS FET): sim to Motorola 3N201.
TR2	JRC/5TCAB01231	Silicon, NPN: sim to NEC NTM3904-T2.
TR3	JRC/5TCAB01232	Silicon, PNP: sim to NEC NTM3906-T2.
TR4	JRC/5TCAB01233	Silicon, PNP: sim to NEC NTM3906-T1.
TR5	JRC/5TCAB01234	Silicon, NPN: sim to NEC NTM3904-T1.
TR6	JRC/5TCAB01233	Silicon, PNP: sim to NEC NTM3906-T1.
Z1	JRC/5NDAB00035	Delay Line JPC SDL300-201T-24S

PARTS LIST CHANGES

The prefix of Service Parts replacement part numbers listed in the various Parts Lists included in this maintenance manual have been changed from "JRC/" to "B19/". All other characters remain the same as displayed. When this manual is next reprinted, all replacement parts lists will show only the "B19/" prefix.

When ordering replacement parts listed in this manual from the GE Mobile Communications Service Parts Operation, please use only the "B19/" prefix. The "B19/" prefix will be the only one shown in any future SERVICE PARTS PRICE LIST.

MODIFICATION INSTRUCTIONS

These Modification Instructions cover installation of the Noise Blanker Kit in a RANGR Low Band Radio.

PARTS REQUIRED-Modification Kit JRC/CFR-72-I KIT consisting of;

1. Noise Blanker PCB Assy MDNW05875.
2. Threaded spacer MTK004208; qty.2
3. Split lockwasher BRTG03493; qty.4
4. Mounting screw BRTG03290; qty.2
5. Label MPNN19522.
6. Clear Label overlay MPNN19349.
7. Manual Request Card ECR3224.

TOOLS REQUIRED

1. Screwdriver TORX (T-25 and T-10)
2. Tuning tool (supplied with radio)

PROCEDURE

1. Remove the bottom cover from the radio.
2. Mount spacer in locations "A", with one lockwasher each, see figure 1.
3. Plug in the Noise Blanker PCB assembly in location "B".
4. Secure the Noise Blanker using two mounting screws with lockwashers in location "A".
5. Cut wire link W402.

LABELING

1. On the blank label supplied, enter the serial number of the radio, Enter the last six characters of the FCC ID number (include dashes), See figure 2.
2. Enter the part number as follows.

From	To
19C852050P1	19C852050P5
19C852050P2	19C852050P6
19C852050P3	19C852050P7
19C852050P4	19C852050P8

3. Peel the label from its backing and attach over existing label.
4. Peel the clear overlay from its backing and attach over the new label.

TEST

1. Refer to the Maintenance Manual LBI-31619 for the measurement of SINAD sensitivity.
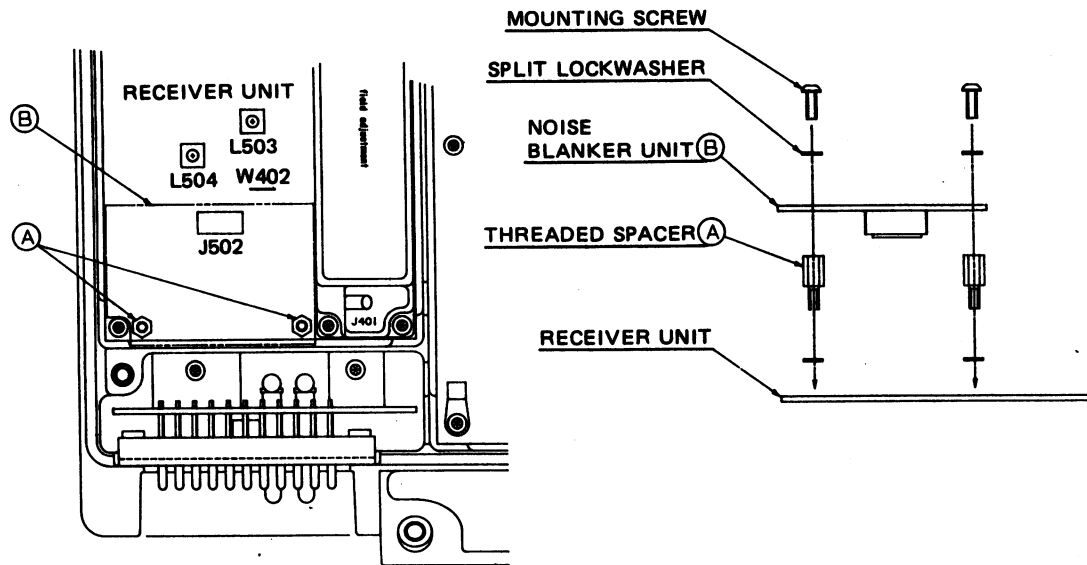2. Adjust L503 and L504 for maximum SINAD sensitivity.
3. Replace the bottom cover on the radio.

FIGURE 1 BOTTOM VIEW OF RADIO

FIGURE 2 NEW LABEL