SERVICE SECTION
FOR
EDACS 900 MHz GETC SHELF

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INTRODUCTION

This manual contains the information required for testing and servicing the General Electric Trunking Card (GETC) station shelf. Included are adjustment and trouble shooting procedures, GETC shelf Interconnection Diagram, Outline and Schematic Diagrams, and Parts List for the GETC logic board and the Regulator Assembly.

The adjustments cover the GETC shelf. Service information includes four areas of GETC test: off-site test (bench lab stand-alone test), on-site test (limited test with minimum equipment in a station), station test (test in a station), and trunking test (test with a mobile or portable acquiring the station).

INSTALLATION

The GETC is installed in a station cabinet. A slide mount supports the GETC shelf assembly, and also allows for easy access during setup and servicing. The GETC Logic card assembly may be removed from the Shelf Assembly by disconnecting the connecting cables and removing the card assembly from the shelf slide. Installation of the GETC shelf assembly in a station is as follows:

1. Mount the GETC Shelf Assembly in the desired rack position, using the hardware provided. Extend the shelf to the servicing position.
2. Connect the harness assembly (19C320811) plug P26 to GETC Logic card connector J6.
3. Connect the harness assembly (19C320811) plug P27 to GETC Logic card connector J7.
4. Connect the harness assembly (19C320811) plug P10 to GETC Logic card connector J10.
5. Connect the harness assembly (19C320811) plug P19 to GETC Logic card connector J19.
6. Connect the harness assembly (19C336863) plug P8 to GETC Logic card connector J8.
7. Connect the harness assembly (19C336863) plug P19 to GETC Logic card connector J19.
8. Slide the GETC shelf back into the cabinet.
9. If a site controller is present, connect the Site Controller cable (from RS-232 Distribution Panel to connector J100 at the back of the GETC Shelf Assembly.
10. Connect the Backup Serial Link cable (from Failsoft Distribution Panel) to connector J102 at the back of the GETC Shelf Assembly.

STATUS INDICATION

There are seven LED indicators on the front of the GETC shelf that indicate the status of the panel. The LEDs indicate whether the repeater is operating as a control channel, idle voice channel or active voice channel. In addition, the GETC is capable of detection ROM failure, RAM failure, synthesizer lock error, or an RF power amplifier failure. If any of these faults are detected, the GETC will automatically notify the site controller (if present), take the station off-line, and begin flashing a combination of LEDs on the front panel to indicate the exact failure. The operation and description of the front panel status indicators is shown in Figure 1.

ADJUSTMENTS

Adjustments in this section are necessary when the GETC shelf is installed in a station. The adjustments properly configure the GETC (DIP switches and jumpers), balance the telephone line, and set high speed, low speed, and audio modulation.

DIP SWITCHES

There are three dual-in-line (DIP) switches on the GETC logic board that must be configured for the proper transmitter frequency, desired channel number, and default mode for trunking operation. It is also possible to invoke test mode operation with the DIP switches.

Selecting Channel Number

Switches S3-1 through S3-5 configure the GETC with the channel number. Allowable channel numbers range from 1(0001 binary) to 20 (10100 binary) for control and working channels. Channel numbers 0, 21 thru 25, and 27-30 are reserved, and channel number 31 (11111 binary) is used in the terminal test mode. Switch S3-5 is the most significant bit (MSB), and S3-1 is the least-significant bit (LSB) of the GETC channel number. Also, a logic 0 is defined as a closed (on) switch setting, and a logic 1 is defined as an open (off) switch setting. Table 1 lists the allowable channel numbers and their binary equivalents.

Selecting RF Transmit Frequency

The RF transmit frequency is set by S1-1 thru S1-7 and S2-1 thru S2-4. These eleven bits encode the transmitter and receiver frequency, in the range from 935 to 940 MHz(TX) and 896 to 901 MHz(RX), at a 12.5 kHz channel spacing. At power up, reset, or out-of-lock condition of the synthesizer, the GETC will attempt to load the transmit frequency code to the synthesizer. The allowable transmit frequencies and their corresponding switch settings are listed in Appendix A.

FRONT PANEL LED STATUS							DESCRIPTION
L1	L2	L3	L4	L5	L6	L7	
∅	○	●	○	○	●	●	CONTROL CHANNEL
∅	○	●	○	○	○	●	IDLE VOICE CHANNEL
∅	○	●	○	○	●	○	ACTIVE VOICE CHANNEL
∅	○	●	●	●	⊕	○	SYNTHESIZER FAILURE
∅	○	●	○	○	⊕	○	SYNTHESIZER RECOVERING
∅	○	●	○	○	⊗	○	PA FAILURE
○	○	○	○	○	⊕	⊕	POWER UP RAM / ROM FAILURE (L6, L7, BLINK TOGETHER)

● = ON
○ = OFF
⊙ = QUICK FLASHING, OFF (REPEATED)
⊛ = BLINKING ON, OFF, ON, OFF
∅→ : L1 IS OFF IF SITE CONTROLLER IS ACTIVE. L1 IS ON IF IN FAILSOFT MODE.

Figure 1 - Front Panel Status Indicators

Selecting Default Failsoft Operation

Default failsoft operation is defined by S3-8. Setting S3 to open on a control channel will force failsoft operation at the next reset. This switch is set open only if the system is operating without a site controller.

Selecting Trunking Mode

In failsoft mode, S3-7 controls the trunking mode. Setting S3-7 open will select transmission trunked operation for all group dispatch calls. With S3-7 closed, calls are processed with a 5 second hang time on the voice channel.

Selecting Test Mode

S3-6 open selects test mode. Two test mode types are available: DIP switch mode and interactive terminal mode. All station alignment and checks can be done using DIP switch test mode. Terminal mode is selected by setting S3-1 through S3-6 all open and is used for testing the GETC board on the bench. DIP switch test mode is selected by setting S3-1 though S3-6 for the appropriate test and then resetting the GETC shelf. The DIP switch tests are used to align the station data and audio levels. The available test settings are shown in Table 4.

NOTE

A manual reset or power-up is required to insure that the DIP switch settings have been read and activated after any switch change.

JUMPER CONFIGURATION

The jumpers on the GETC logic board are configured for EDACS 900 applications. Table 2 describes the functions of the jumpers. Other jumper configurations enable the GETC to be used in other applications and functions.

SERVICE AND TEST

This section describes four test procedures that are used to test the GETC. These include the off site test, the on site test, the station test, and the Trunking test.

The off site test is used to test the GETC in a laboratory environment or under bench test. On site testing is used to test the GETC at the site location using a limited set of tools or equipment. Station testing is used to test the GETC in a station and to perform adjustments. The Trunking test is used to test the GETC as part of a functional system.

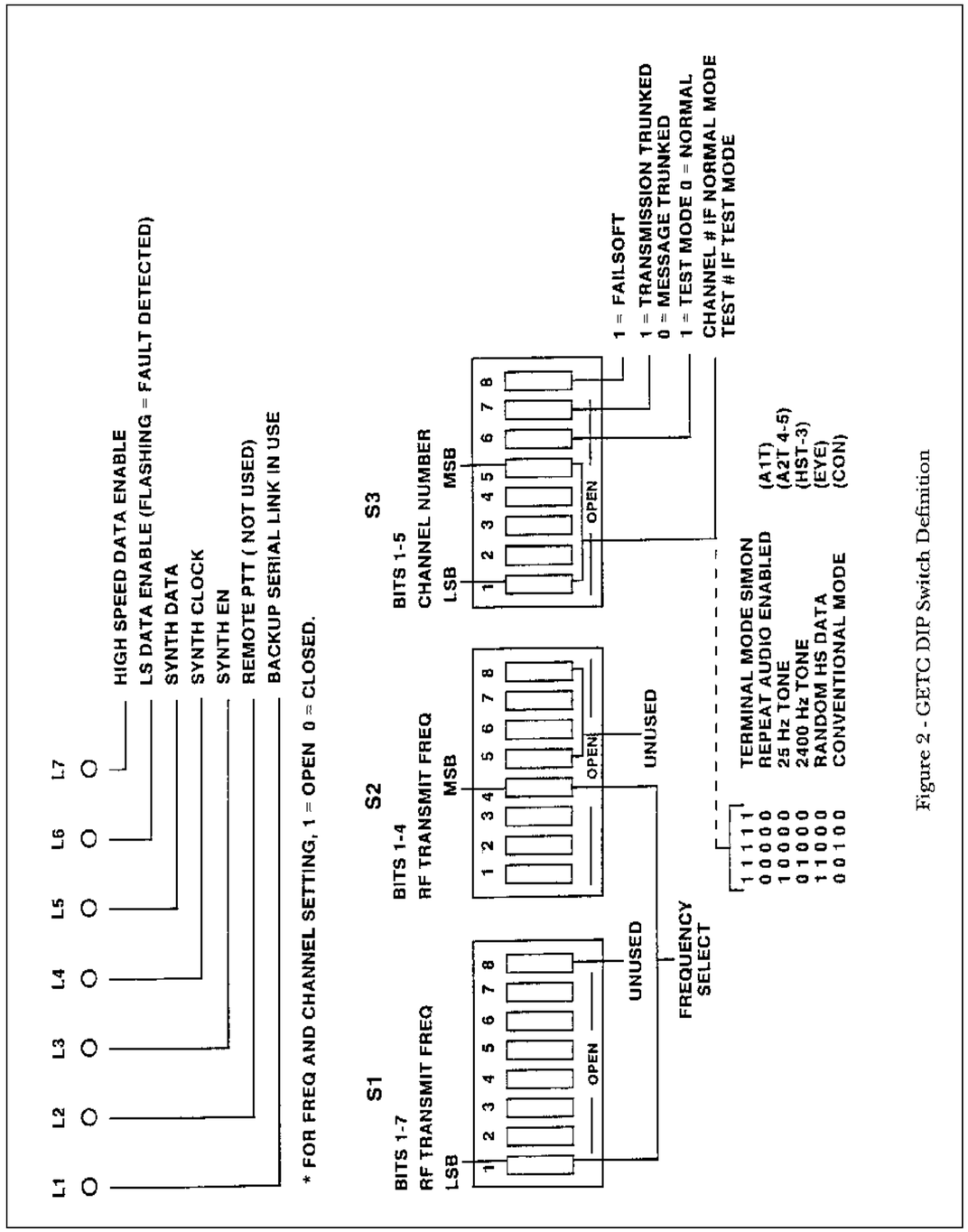

Figure 2 - GETC DIP Switch Definition

TERMINAL CONNECTION

An ASCII terminal or computer with terminal emulation program and RS-232 port is used to communicate with the GETC in the test mode of operation. The terminal should be configured for a 2400 baud link, odd parity, full duplex, and uppercase characters. Figure 3 shows a sample connection cable. Terminal and GETC pin assignments are listed in Table 3.

Table 1 - GETC Channel Number Settings

CHANNEL NUMBER	SWITCH SETTINGS S3-1 THRU S3-6	COMMENTS
0	000000	RESERVED
1	100000	CONTROL OR WORKING
2	010000	CONTROL OR WORKING
3	110000	CONTROL OR WORKING
4	001000	CONTROL OR WORKING
5	101000	CONTROL OR WORKING
6	011000	CONTROL OR WORKING
7	111000	CONTROL OR WORKING
8	000100	CONTROL OR WORKING
9	100100	CONTROL OR WORKING
10	010100	CONTROL OR WORKING
11	110100	CONTROL OR WORKING
12	001100	CONTROL OR WORKING
13	101100	CONTROL OR WORKING
14	011100	CONTROL OR WORKING
15	111100	CONTROL OR WORKING
16	000010	CONTROL OR WORKING
17	100010	CONTROL OR WORKING
18	010010	CONTROL OR WORKING
19	110010	CONTROL OR WORKING
20	001010	CONTROL OR WORKING
21	101010	RESERVED
22	011010	RESERVED
23	111010	RESERVED
24	000110	RESERVED
25	100110	RESERVED
26	010110	DOWNLINK
27	110110	RESERVED
28	001110	RESERVED
29	101110	RESERVED
30	011110	RESERVED
31	111111	TEST MODE (TERMINAL)

Table 2 - Jumper Setup & Functions

JUMPER	GE-NET TRUNKING	FUNCTION
P11	J11-1 & 2	Receive data from 9600 baud Modem board
P12	J12-1 & 2	Clear to send from 9600 baud Modem board
P13	J13-1 & 2	Route backup serial link tx output to backup serial link rx input
P14	J14-1 & 2	Master site controller path selection enable
P15	J15-1 & 2	Site controller path selection enable
P16	J16-1 & 2	Backup serial link selection enable
P17	J17-1 & 2	Low-speed data encode path enable
P18	J18-1 & 2	Low-speed data decode path enable
P20	J20-1 & 2	Combined ptt from station disable
P21	J21-1 & 2	High-speed, data-acquisition rate control
P22	J22-2 & 3	4800 Hz tone notch filter (disable)
P24	J24-1 & 2	Backup serial link selection enable
P25	J25-1 & 2	Low-speed data encode path enable
P26	J26-1 & 2	Lock-detect input path enable
P28	J28-1 & 2	Sync line input path enable
P29	J29-1 & 2	No function
P30	J30-2 & 3	Enable clock drive to
P30	J30-4 & 5	microcomputer for CMOS configuration
P44	J44-1 & 2	Selects A14 for 27C256 and 27C512 EPROM
P45	J45-2 & 3	Selects 6064 RAM
P46	J46-1 & 2	INTO for voter concentrator
P47	J47-1 & 2	Backup serial link select
P48	J48-1 & 2	Backup serial link select
P50	J50-1 & 2	Tone control for voted system
P51	J51-1 & 2	Morse code ID attenuator enable
P52	J52-1 & 2	TXD polarity select
P53	J53-1 & 2	RXD polarity select
52	J52-1 & 2	TXD polarity select
P53	J53-1 & 2	RXD polarity select
P54	J54-1 & 2	Enables control input to U15-A
P55	J55-1 & 2	Enables WALSH bit 1
P60	J60-1 & 2	Enables high-speed data path
P61	J61-2 & 3	Selects A15 for 27C512 EPROM U2
P62	J62-2 & 3	Selects proper clock frequency for U4 obtain 4800 Baud data rate.
P63	1 & 2	Sets TX data filter for 4800 baud
P64	1 & 2	Sets TX data filter for 4800 baud
P65	1 & 2	Sets TX data filter for 4800 baud
P66	1 & 2	Sets TX data filter for 4800 baud
P67	Omit	Receive telephone line termination (not used)
P68	J68-1 & 2	Enables delayed PTT
P69	J69-1 & 2	Enables COMB PTT IN
P70	J70-1 & 2	Enables COMB PTT IN
P71	J71-1 & 2	Configures telephone line modem RTS

Table 3 - GETC and RS-232C Pin Assignments

SIGNAL FROM GETC	GETC LOGIC BD PIN NUMBER	GETC SHELF PIN NUMBER	TERMINAL EIA RS-232C D-TYPE CONNECTOR PIN NUMBER
TXD	J8-1 (MASTER)	J100-3 (MASTER)	PIN 3
TXD	J19-1 (BACKUP)	J101-3 (BACKUP)	PIN 3
RXD	J8-2 (MASTER)	J100-2 (MASTER)	PIN 2
RXD	J19-2 (BACKUP)	J101-2 (BACKUP)	PIN 2
GND	J8-3 (MASTER)	J100-1 (MASTER)	PIN 7
GND	J19-3 (BACKUP)	J101-1 (BACKUP)	PIN 7

This connection cable may be used any time the terminal is used during a GETC test procedure. Characters that are typed from the keyboard are followed by RETURN(ENTER). A key press on the keyboard (such as ESC, TAB, or RETURN) is indicated by the key name enclosed in square brackets [KEY PRESS]. Control functions are indicated by CTRL - (CONTROL CHARACTER), such as CTRL-Z to indicate the Z is pressed while holding down the CTRL key. If variable data or commands are to be entered, they will be enclosed in angle brackets <VARIABLE DATA>. Variable data depends on your particular application or test. Type the appropriate response (do not include brackets) and follow by a return if required.

POWER SUPPLY TEST (Bench Test)

1. Connect power supply to GETC connector J10 (pin 1 is +13.8 V and pin 2 is ground).

2. Turn on the power supply and verify the current drawn does not exceed 700 mA (1.2 A with modem board installed). If current is exceeded, check power supply circuitry before proceeding.

3. Connect a frequency counter or oscilloscope to TP104 and verify the presence of the 4800 Hz clock. If the clock is missing, check modem U4 and associated circuitry.

4. Verify the presence of the following voltages:

MONITOR POINT	VOLTAGE	CHECK IF MISSING OR INCORRECT
TP110	+5.0+/-0.25	Regulator board
TP111	+5.0+/-0.25	Regulator board
TP108	-12.0 +/ 1.2	-12-volt power supply
TP109	+12.0 +/ 1.2	+12-volt power supply

MICROCOMPUTER CLOCK TEST

Equipment Required

- Frequency Counter

Test Procedure

1. Connect frequency counter to J30-3.

2. Verify the microcomputer clock frequency is 11.0592 MHz ± 500 Hz.

OFF-SITE TEST

The off site test is used to test the GETC in a laboratory environment or under bench test. This section outlines the testing of the GETC as a stand alone unit outside of the station. However, these same tests can be done with the unit installed in the station if connectors J6, J7, J8, and J19 are disconnected from the GETC board during the tests.

Equipment Required

The equipment necessary for the off site test includes:

1. HP-6286A (or equivalent) DC power supply with current limit.

2. Tektronix-468 (or equivalent) digital storage scope.

3. HP-3312A (or equivalent) Function Generator.

4. Fluke-1920A (or equivalent) Frequency Counter.

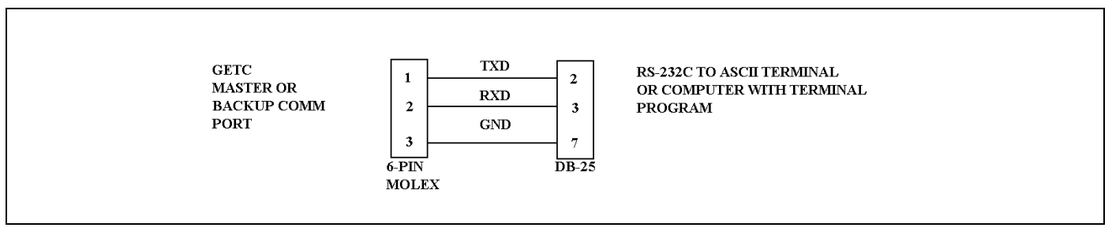

Figure 3 - Terminal-To-GETC Connection Cable

5. Data Technology Model 30 digital Multimeter or equivalent.

6. Triplett Model 630-PL Type 5 VOM or equivalent.

7. ASCII Terminal or Computer with terminal connection program.

8. HP-334A (or equivalent) Distortion Analyzer.

Preliminary Setup

1. Set switches S3-1 thru S3-6 to their off (open) positions.

2. Connect the terminal or computer to the GETC master communication link (J8). Refer to Table 3 for GETC and RS-232C pin assignments.

3. Configure jumpers as shown in Table 2 if not already set up.

4. Move jumpers from J46-1&2 to J46-2&3 and from J51-1&2 to J51-2&3.

Serial Link Test

1. Apply power to the GETC (or press RESET switch S4 if power is already applied). The terminal will display the SIMON welcome message. If the welcome message does not appear, check the following:
   - Check terminal hookup
   - Check for +5 volts at U14-4 (SITE RX EN)
   - Check reset circuitry
   - Check for serial data on the TX and RX lines
2. Execute the <BCL> command (backup communications link) on the terminal. Press [RETURN] and verify that terminal communication on the master link is inoperative.
3. Move the terminal from the master (J8) to the backup link (J19). Press [RETURN] and verify that terminal communication on the backup link is operative by executing the command.
4. Execute the <MCL> command (master communications link) on the terminal. Press [RETURN] and verify that terminal communication on the backup link is inoperative.
5. Move the terminal from the backup (J19) to the master (J8) link. Press [RETURN] and verify that terminal communication on the master link is operative by executing the command.

EPROM Test

Execute the command CHK O-FFFF. Verify the terminal response of "CHECKSUM=OO".

RAM Test

Execute the command <TMX OOO-1FFF> to check U4. Verify the terminal response of "SIX PATTERNS TO CHECK OK".

Reset Circuit Test

1. Lower the input power to 6 volts.

2. Raise the input power to 9 volts. Verify the GETC welcome message to the terminal.

Watchdog Timer Test

1. Execute the command <WAT> to verify Watchdog Timer (U4).

2. Verify the GETC response of the welcome message to the terminal after 5 seconds.

Input Buffer and Port Test

1. Move jumper P20 from J20-1&2 to J20-2&3.

2. Move jumper P26 from J26-1&2 to J26-2&3.

3. Move jumper P28 from J28-1&2 to J28-2&3.

4. Move jumper P12 from J12-1&2 to J12-2&3.

5. Connect J7-7, J7-9, J7-11, J7-13, and J3-25C to ground.

6. Execute the command <POR1>, and verify the terminal response of 10101010.

7. Execute the command <POR3>, and verify the terminal response of XX01XXXX, where X is any state.

8. Remove the ground from J7-7, J7-9, J7-11, J7-13, and J3-25C.

9. Connect J7-6, J7-8, J7-10, J7-12, and J7-14 to ground.

10. Execute the command <POR1>, and verify the terminal response of 01010101.

11. Execute the command <POR3>, and verify the terminal response of XX10XXXX, where X is any state.

12. Remove the ground from J7-6, J7-8, J7-10, J7-12 and J7-14.

13. Move jumper P20 from J20-2&3 to J20-1&2.

14. Move jumper P26 from J26-2&3 to J26-1&2.

15. Move jumper P28 from J28-2&3 to J28-1&2.

16. Move jumper P12 from J12-2&3 to J12-1&2.

High Speed Data Test

1. Jumper J7-2 to J7-4.

2. Execute the command <MDS 0>.

3. Execute the command <BER DE-00=10>, and verify the terminal response of:

   "RECEIVE ERROR COUNT=0000 RECEIVE CHECK-SUM=00188123"

   which continually updates every 20 seconds.

4. Enter CTRL-Z or [ESC] to end the test. Remove the jumper from J7-2 and J7-4.

Low-Speed Data Encode/Decode Test

1. Move jumper on J15 to 2&3.

2. Place a 10K pullup on J15-1 to 5 volts.

3. Execute the command <XBY B800=B6>.

4. Monitor the following points using an oscilloscope.

MONITOR POINT	LOGIC LEVEL
U38-2	0
U38-5	1
U34-10	0
J19-6	1
J15-1	0
U38-15	1
U38-16	0
U38-19	1

5. Enter CTRL-Z or [ESC].

6. Execute the command <XBY B800=49>.

Output Latch and Buffer Test

NO.	STEP	TEST POINT	LOGIC LEVEL
1.	Move jumper P14 from J14-1&2 to J14-2&3.		
2.	Move jumper P24 from J24-1&2 to J24-2&3.		
3.	Move jumper P25 from J25-1&2 to J25-2&3.		
4.	Move jumper P20 from J20-1&2 to J20-2&3.		
5.	Install a 10K resistor from J7-14 to ground.		
6.	Install a 10K resistor from the open collector points (OC) to +13.8 volts.		
	NOTE: Unless otherwise specified, a logic one is defined as 13.8 ± 0.5 volts, and a logic zero is defined as 0 ± 0.5 volts.		
7.	Execute the command <XBY A800=52>.		
8.	Execute the command <XBY B000=42>.		
9.	Connect J7-6 to ground.		
		J6-1	1
		J6-2	1
		J6-3	1
		J6-4	0
		J6-5	1
		J6-10	1
		J6-11	0
		J6-12	1
		J6-13	0
		J6-14	1
		J6-15	1
		J6-16	1
		J7-14	<0.5V
		J7-15	<0.5V
		J7-16	0
		J9-1	>10V
		J3-25A	<0.5V
		J3-13C	1
	Indicators	H1 (L7)	OFF
		H2 (L6)	ON
		H3 (L5)	OFF
		H4 (L4)	ON
		H5 (L3)	ON
		H6 (L2)	OFF
		H7 (L1)	OFF
	NOTE: Reset the GETC to terminate this test		

NO.	STEP	TEST POINT	LOGIC LEVEL
10.	Execute the command <XBY B000=B9>.		
11.	Execute the command <XBY A800=AD>.		
12.	Connect J7-6 to ground.		
		J6-1	0
		J6-2	0
		J6-3	0
		J6-4	1
		J6-5	0
		J6-10	0
		J6-11	1
		J6-12	0
		J6-13	1
		J6-14	0
		J6-15	1
		J6-16	0
		J7-14	>7V
		J7-15	>7V
		J7-16	1
		J9-1	<-10V
		J3-25A	>3.5V
		J3-13C	0
	Indicators	H1 (L7)	ON
		H2 (L6)	OFF
		H3 (L5)	ON
		H4 (L4)	OFF
		H5 (L3)	OFF
		H6 (L2)	ON
		H7 (L1)	ON
13.	Execute the command <XBY A800=00>.		
14.	Execute the command <XBY B000=OC>. Do not connect J7-6 to ground.		
		J6-1	1
		J6-2	1
		J6-3	1
		J6-4	1
		J6-5	1
		J6-10	1
		J6-11	1
		J6-12	1
		J6-13	1
		J6-14	1
		J6-15	1
		J6-16	1
		J7-14	>7V
		J7-15	>0.5V
		J7-16	1
		J9-1	10V
		J3-25A	<0.5V
		J3-13C	0

NO.	STEP	TEST POINT	LOGIC LEVEL
	Indicators	H1 (L7)	OFF
		H2 (L6)	OFF
		H3 (L5)	OFF
		H4 (L4)	OFF
		H5 (L3)	OFF
		H6 (L2)	OFF
		H7 (L1)	OFF
	NOTE: Reset the GETC to terminate this test		
15.	Execute the command <XBY B000=08>.		
16.	Execute the command <XBY A800=80>. Do not connect J7-6 to ground.		
		J6-1	1
		J6-2	0
		J6-3	1
		J6-4	1
		J6-5	1
		J6-10	1
		J6-11	1
		J6-12	1
		J6-13	1
		J6-14	1
		J6-15	1
		J6-16	1
		J7-14	>7V
		J7-15	>7V
		J7-16	1
		J9-1	>10V
		J3-25A	<0.5V
		J3-13C	0
	Indicators	H1 (L7)	OFF
		H2 (L6)	OFF
		H3 (L5)	OFF
		H4 (L4)	OFF
		H5 (L3)	OFF
		H6 (L2)	OFF
		H7 (L1)	OFF
17.	Move jumper P20 from J20-2&3 to J20-1&2.		
18.	Move jumper P14 from J14-2&3 to J14-1&2.		
19.	Move jumper P24 from J24-2&3 to J24-1&2.		
20.	Move jumper P25 from J25-2&3 to J25-1&2.		

7. Monitor the following points using an oscilloscope.

MONITOR POINT	LOGIC LEVEL
U38-2	1
U38-5	0
U34-10	1
J19-6	0
J15-1	1
U38-15	0
U38-16	1
U38-19	0

8. Jumper J19-5 to J7-2.

9. Connect an oscilloscope to J19-5.

10. Execute the commands and verify the responses listed below.

COMMAND	FREQUENCY ON J19-5(HZ)	AMPLITUDE ON J19-5(VP-P) CENTERED AT	FREQUENCY OF SQUARE-WAVE ON J18-1 (HZ)
LSH 1-1	10	2.0 ± 0.25	10
LSH 1-2	100	2.0 ± 0.25	100
LSH 1-3	200	2.0 ± 0.25	200
LSH 1-4	1000	-32 dB of 2.0	UNDEFINED
LSH 2-1	10	1.0 ± 0.25	10
LSH 2-2	100	1.0 ± 0.25	100
LSH 2-3	200	1.0 ± 0.25	200
LSH 2-4	1000	-32 dB of 1.0	UNDEFINED
LSH 3-1	10	3.5 ± 0.5	10
LSH 3-2	100	3.5 ± 0.5	100
LSH 3-3	200	3.5 ± 0.5	200

11. Enter CTRL-Z or [ESC] to end the test.

12. Move jumper P15 back to J15-1&2.

DIP Switch Test

1. Execute the <DSW> command and verify the settings of DIP switches, S1, S2, and S3. The terminal display is as shown:

```
"------      ------      ------"
 1    8      1    8      1    8
   S1          S2          S3
```

An open (or OFF) on the DIP switch is displayed as a "1", while a closed (or ON) is displayed a "0".

This test continually updates the terminal display at each DIP switch setting change. Verify all switches are functional by testing both the open and closed positions.

2. Enter CTRL-Z or [ESC] to end the test. Set S3-1 thru S3-6 to open.

High Speed Data Filter Test

1. Monitor J7-4 as the output.

2. Execute the command

<FNT1>. Verify 600 Hz signal on J7-4.

3. Execute the command <FNT2>. Verify 1200 Hz signal on J7-4.

4. Execute the command <FNT3>. Verify that the generated 2400 Hz signal has approximately the same amplitude as in steps 3 and 4 and closely approximates a sinusoid. Typical output level is 1 volt RMS when R31 is adjusted for rated deviation.

Test Completion

Reposition all jumpers as shown in Table 2 before placing the GETC back in service.

ON-SITE TEST

This test is used to test the GETC at the system site location using limited tools and equipment. This procedure is a quick in-circuit functional test of the GETC in the station. DIP switch test modes are normally used to set up the station data, audio, and power levels. However, these can also be used to check basic operation of the GETC as well. Table 4 shows the available DIP switch tests.

Equipment Required

The equipment necessary for the on-site test includes:

1. Tektronix 468 (or equivalent) digital storage scope.

2. Triplett Model 630-PL Type 5 VOM or equivalent.

Preliminary Setup

1. Make sure station power is on and all jumpers are set according to Table 2.

2. Slide the GETC shelf out to gain access to the DIP switches located near the front panel.

3. Select the desired test frequency using S1 and S2. See Appendix A for frequency codes.

4. Take the station "off-line" by setting S3-1 through S3-6 to the open position and then momentarily pushing the GETC reset button.

Power Supply Test

1. Check to see that 13.8 volt power is present to the GETC on J10 (pin 1 is +13.8 V and pin 2 is ground).

2. Connect a frequency counter or oscilloscope to TP104 and verify the presence of the 4800 Hz clock. If the clock is missing, check modem U4 and associated circuitry.

3. Verify the presence of the following voltages:

MONITOR POINT	VOLTAGE	CHECK IF MISSING OR INCORRECT
TP110	**+5.0+/-0.25**	**Regulator board**
TP111	**+5.0+/-0.25**	**Regulator board**
TP108	**-12.0 +/ 1.2**	**-12-volt power supply**
TP109	**+12.0 +/ 1.2**	**+12-volt power supply**

Microcomputer & System Clock Test

1. Check for a clock frequency of 11.0592 MHz on J30-3 and J62-1.

2. Check for a 5.5296 MHz clock signal on J62-2&3.

3. Verify a 4800 Hz clock signal is present on TP104.

Low-speed Data Encode/Decode Test

1. Set up S3 for Test (B) as shown in Table 4, and reset the GETC. Make sure the receiver is squelched.

2. Check for a 25 Hz digital square wave on U38-2 and U38-5.

3. Check for a 2 volt peak-to-peak 25 Hz filtered square wave at J19-5 (Subaudible data encode port). See Figure 5 for expected output.

4. Inject an on channel RF signal into the receiver modulated with a 150 Hz tone at ± 0.2 kHz deviation.

5. Check for a 150 Hz digital square wave on J18-1&2 (Subaudible RX data).

High-speed Data Encode/Decode Test

1. Set up S3 for Test (C) as shown in Table 4, and reset the GETC.

2. Check for a 2400 Hz digital square wave on TP101 (Modem TX data).

3. Check for a 2.8 volt peak-to-peak 2400 Hz sine wave at J7-4 (Modulation port). This level may vary slightly depending on the the data deviation pot R31.

4. Inject an on channel RF signal into the receiver modulated with a 2400 Hz tone at ± 0.5 kHz deviation.

5. Check for a 2400 Hz digital square wave on TP103 (Modem RX data).

Test Completion

1. Set the GETC DIP switches back to the operational configuration for the station.

2. Reset the GETC to put the station back on line. Verify that the station comes back up as either a voice channel or a control channel.

3. Slide the GETC back into the station shelf.

STATION TEST AND ADJUSTMENT

The station test is used to test the station and to perform repeat audio, high speed data, and low speed data adjustments. This section describes the adjustments of the GETC as part of a station.

Equipment Required

The equipment necessary for the station test includes:

1. HP-8920A Communications Test Set or equivalent.

2. Tektronix 468 (or equivalent) digital storage scope.

3. HP-3312A (or equivalent) Function Generator.

4. Fluke-1920A (or equivalent) Frequency Counter.

5. Data Technology Model 30 (or equivalent) digital Multimeter.

6. Triplett Model 630-PL Type 5 (or equivalent) VOM.

7. HP-334A (or equivalent) Distortion Analyzer

The GETC can be DIP switch programmed to enter simple test mode operation. In this mode, single test function commands can be executed without need of a video terminal. Entering any of the test functions will load the synthesizer with the channel setting from DIP switches S1, S2 and then execute a function selected with DIP switches S3-1 through S3-6. Each test function is invoked by setting DIP switches S3-1 through S3-6 to the desired test function and then resetting the GETC. Table 4 lists the available tests.

Setup

Connect the test equipment to the station unit as shown in Figure 4. Select the desired test frequency using DIP switches S1 and S2 located on the GETC shelf (see Appendix A). The remaining DIP switch settings must be selected for each test. A logic '1' corresponds to an 'OPEN' switch while a logic '0' is selected by the 'CLOSED' position.

Table 4 - DIP Switch Test Configuration

TEST	S3-1 S3-6	FUNCTIONS PERFORMED
(A)	000001	Key transmitter and enable repeat audio path.
(B)	100001	Key transmitter, enable repeat audio path and send continuous 25 Hz data.
(C)	010001	Key transmitter, enable high speed data path and send continuous 2400 Hz tone.
(D)	110001	Key transmitter, enable high speed data path and send continuous random high speed data.
(E)	001001	Conventional mode, key transmitter and enable repeat audio when carrier is present.
	101001	UNDEFINED
	011111	UNDEFINED

Low Frequency Adjustment

1. Remove all signals from the receiver input and make sure the squelch is fully muted.
2. Set up DIP switches for test "A" and reset GETC.
3. Connect function generator (5 Hz square wave, 3 V peak) to exciter module J902 pin 2.
4. Set R83 (TONE DATA ADJ.) on the exciter module fully clockwise for maximum subaudible data deviation.
5. View the demodulated 5 Hz square wave on a HP8920A communications test set with its output connected to a DC coupled oscilloscope. The HP8920A should be configured as an FM demodulator with settings as follows: filter-1 <20 Hz HPF, filter-2 3 kHz LPF, de-emphasis off, scope to input. Detailed instructions for the HP8920A follow:

   A Apply power. This configures the instrument with its default settings. DO NOT PRESS THE BASE KEY AT ANY TIME. THIS WILL CHANGE THE DEFAULT SETTINGS AND AFFECT TEST CONFIGURATION!.

   B Press the **TX** key. This configures the analyzer for transmitter tests and displays the **TX TEST** screen.

   C Turn the CURSOR CONTROL knob until the cursor is positioned next to the **Tune Mode** selections (Auto/Manual). Pressing the knob toggles between choices by underlining the preferred mode. Select Manual (Auto/Manual).

   D In a similar manner, move the cursor to the **Input Port** position and select RF in.

   E Move the cursor to the **AF Anal In** position and press the knob; a menu will be displayed. Move the cursor to FM Demod and select it BY pressing the knob again.

   F In a similar manner, set **Filter 1** to <20 Hz HPF and **Filter 2** to 3 kHz LPF.

   G Toggle the **De-emphasis** setting to Off.

   H Set the **Detector** to Pk+-Max.

   I Move the cursor to the **To Screen** menu and select **AF ANL**. The display will change to the **AF ANALYZER** screen.

   J Move to the **Scope To** selection and select Input.

   K Move the cursor to the **To Screen** menu and select **RF ANL**. The display will change to the **RF ANALYZER** screen.

   L Move the cursor to the **Tune Freq** position. Press the knob to highlight the frequency then press the **INCR SET** button. Enter 500Hz using the numerical key pad and the **Hz** button.

   M This completes the entry of the test configuration. The configuration can now be saved for recall by pressing **SHIFT** then **SAVE**, and selecting an option from the **Save** menu or by using the numerical key pad. To use the numerical key pad, enter one or more digits followed by the **ENTER** key.

   N This completes the setup of the HP-8920A.

6. Adjust R78 (DATA SYN ADJ) on the exciter module until the best square wave (5 Hz) is obtained.
7. Remove function generator from the exciter module J902 pin 2. Set up DIP switches for test "B" and reset the GETC.
8. Adjust R83 (TONE DATA ADJ) on the exciter module for 0.5 ± 0.05 kHz deviation.

High Speed 4800 Baud Data Adjustment

1. Set up DIP switches for test "C" and reset the GETC.
2. Adjust R31 on the GETC shelf assembly to obtain 1.5 ± 0.1 kHz deviation. Verify the generated 2400 Hz tone nearly approximates a sine wave.
3. Set up DIP switches for test "D" and reset the GETC.
4. Verify the 4800 baud EYE pattern is generated and that the output is between ± 1.4 kHz and ± 1.7 kHz deviation. See Figure 6 for typical EYE pattern.

Repeat Audio Adjustment

1. Set up DIP switches for test "A" and reset the GETC.
2. Inject an on channel carrier (-50 dBm) with a 1 kHz tone @ ± 1.5 kHz deviation.
3. Check the audio level at the Volume Squelch HI signal on the audio board output located inside the receiver/exciter door. Adjust R608 on the audio board if necessary to obtain 1 volt RMS ± 50 mV at the output.
4. Adjust R60 (REPEAT AUDIO) on the control shelf assembly fully clockwise in order to overdrive the modulator and cause the exciter limiter to become active.
5. Adjust R71 (VOICE LVL ADJ) on the Exciter assembly to produce between 1.9 and 2.0 kHz deviation measured by the service monitor.
6. Readjust R60 (REPEAT AUDIO) on the control shelf to achieve ± 1.5 kHz deviation.
7. Raise the input deviation to ± 2.5 kHz. Verify the output deviation does not exceed ± 2.0 kHz.

Repeater Operation

1. Set up DIP switches for test "E" and reset the GETC.
2. Inject a 1 kHz tone at 1.5 kHz deviation into the receiver input and set the squelch for 10 dB SINAD opening level.
3. Raise the RF input level to -50 dBm and verify the repeated tone is 1000 Hz at 1.5 ± 0.1 kHz deviation at the transmitter output.
4. Remove the signal input and verify that the station unkeys. Insert the signal input and verify that the station keys.

TRUNKING TEST

The trunking test is used to test the GETC as part of a functional system.

Equipment Required

- Single-channel trunked system (control channel and working channel).
- Trunked mobiles or portables.

Test Procedure

1. Set the mobile or portable and the site controller to the frequencies and channel numbers used for the control and working channels.
2. Configure the control and working channels for transmission trunked operation and forced select failsoft operation (S3-7 and S3-8 open).
3. Key the mobile or portable on a standard group call.
4. Verify the mobile/portable unit keys once on the control channel and then keys a second time followed by open voice communication.
5. Disconnect drive to the RF PA on the control channel. Verify L6 begins flashing and the other channel becomes control (see Figure 1).
6. Reconnect the PA drive on the station being tested. Verify L6 stops flashing within 30 seconds and the station becomes a working channel.
7. Repeat steps (4), (5), and (6).
8. Set the DIP switches as needed to achieve normal system operation before resetting the GETC to put it back in full service.

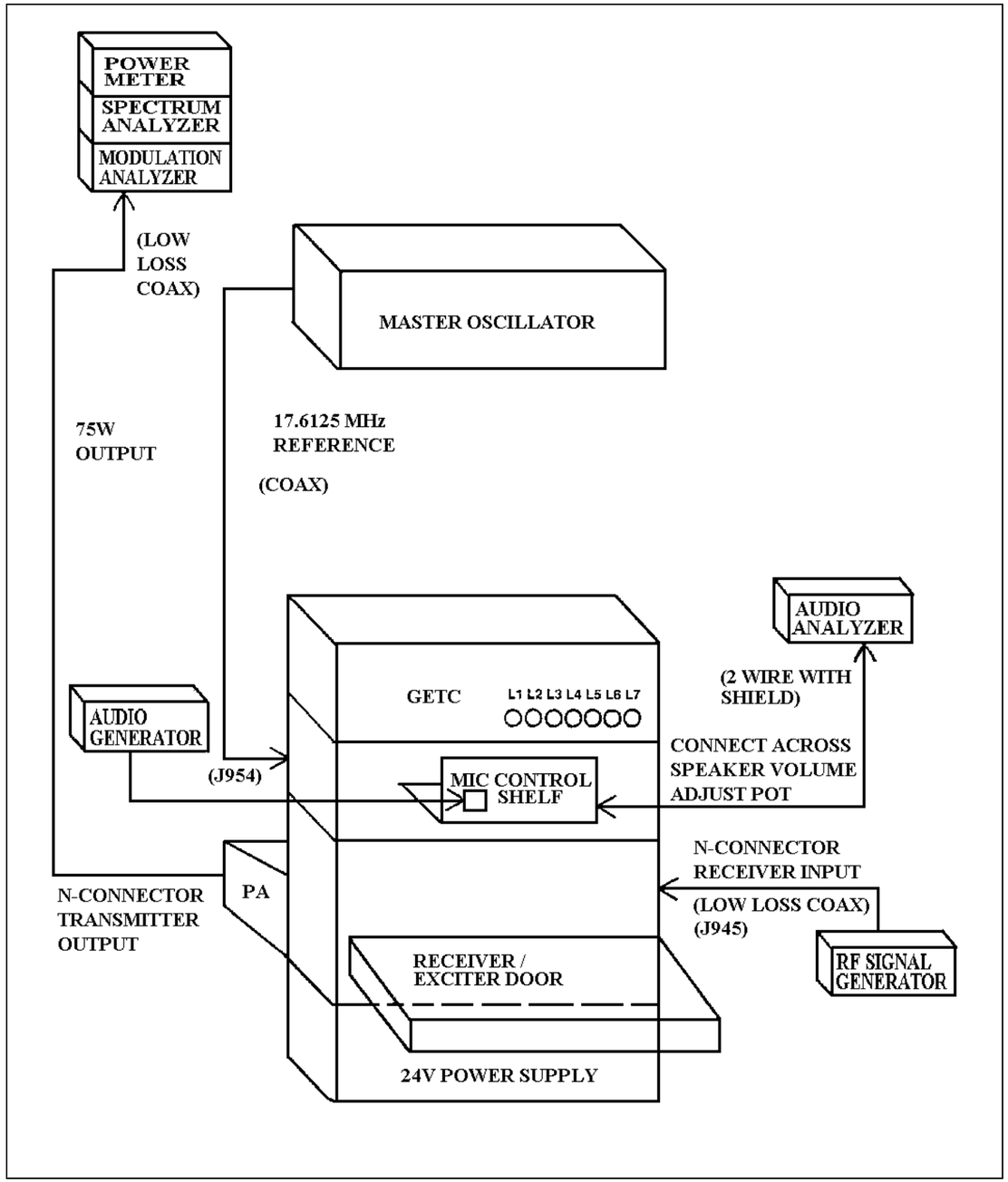

Figure 4 - Station Test Setup

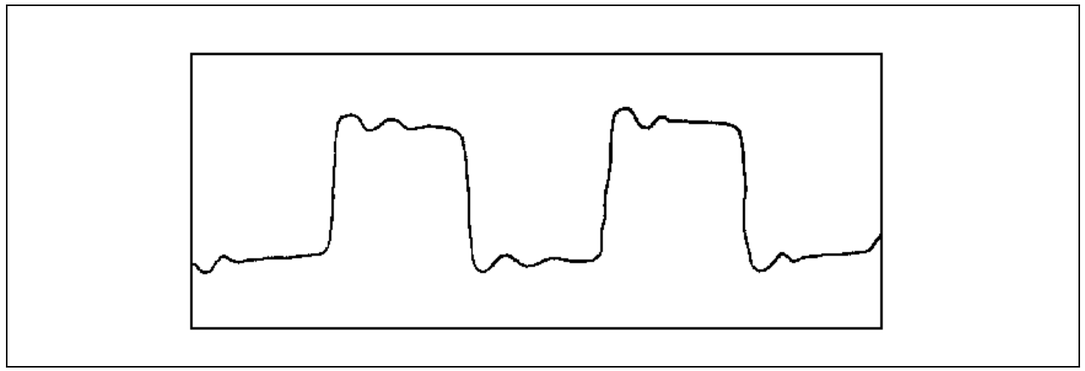

Figure 5 - 25 Hz Squarewave (Typical)

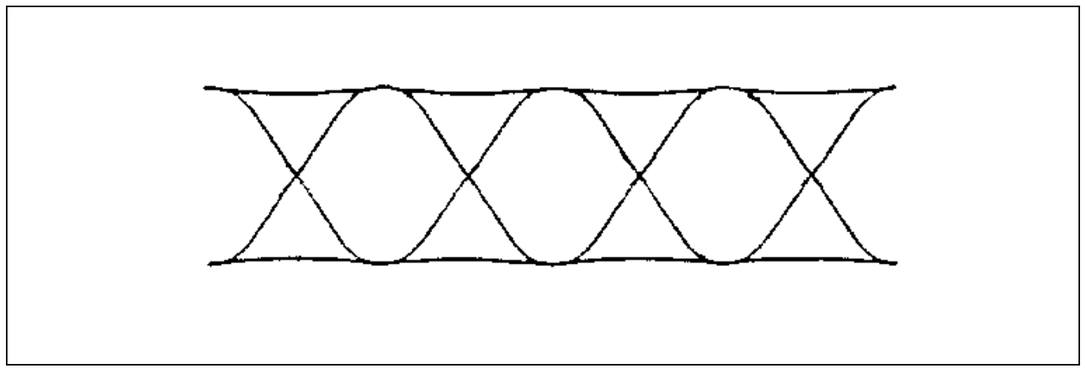

Figure 6 - Typical EYE Pattern

APPENDIX A

GETC FREQUENCY SELECTION SWITCH SETTINGS

TX(MHZ)	S1,1-7 S2,1-4	TX(MHZ)	S1,1-7 S2,1-4	TX(MHZ)	S1,1-7 S2,1-4
935.0125	1000000 0000	935.5125	1001010 0000	936.0125	1000101 0000
935.0250	0100000 0000	935.5250	0101010 0000	936.0250	0100101 0000
935.0375	1100000 0000	935.5375	1101010 0000	936.0375	1100101 0000
935.0500	0010000 0000	935.5500	0011010 0000	936.0500	0010101 0000
935.0625	1010000 0000	935.5625	1011010 0000	936.0625	1010101 0000
935.0750	0110000 0000	935.5750	0111010 0000	936.0750	0110101 0000
935.0875	1110000 0000	935.5875	1111010 0000	936.0875	1110101 0000
935.1000	0001000 0000	935.6000	0000110 0000	936.1000	0001101 0000
935.1125	1001000 0000	935.6125	1000110 0000	936.1125	1001101 0000
935.1250	0101000 0000	935.6250	0100110 0000	936.1250	0101101 0000
935.1375	1101000 0000	935.6375	1100110 0000	936.1375	1101101 0000
935.1500	0011000 0000	935.6500	0010110 0000	936.1500	0011101 0000
935.1625	1011000 0000	935.6625	1010110 0000	936.1625	1011101 0000
935.1750	0111000 0000	935.6750	0110110 0000	936.1750	0111101 0000
935.1875	1111000 0000	935.6875	1110110 0000	936.1875	1111101 0000
935.2000	0000100 0000	935.7000	0001110 0000	936.2000	0000011 0000
935.2125	1000100 0000	935.7125	1001110 0000	936.2125	1000011 0000
935.2250	0100100 0000	935.7250	0101110 0000	936.2250	0100011 0000
935.2375	1100100 0000	935.7375	1101110 0000	936.2375	1100011 0000
935.2500	0010100 0000	935.7500	0011110 0000	936.2500	0010011 0000
935.2625	1010100 0000	935.7625	1011110 0000	936.2625	1010011 0000
935.2750	0110100 0000	935.7750	0111110 0000	936.2750	0110011 0000
935.2875	1110100 0000	935.7875	1111110 0000	936.2875	1110011 0000
935.3000	0001100 0000	935.8000	0000001 0000	936.3000	0001011 0000
935.3125	1001100 0000	935.8125	1000001 0000	936.3125	1001011 0000
935.3250	0101100 0000	935.8250	0100001 0000	936.3250	0101011 0000
935.3375	1101100 0000	935.8375	1100001 0000	936.3375	1101011 0000
935.3500	0011100 0000	935.8500	0010001 0000	936.3500	0011011 0000
935.3625	1011100 0000	935.8625	1010001 0000	936.3625	1011011 0000
935.3750	0111100 0000	935.8750	0110001 0000	936.3750	0111011 0000
935.3875	1111100 0000	935.8875	1110001 0000	936.3875	1111011 0000
935.4000	0000010 0000	935.9000	0001001 0000	936.4000	0000111 0000
935.4125	1000010 0000	935.9125	1001001 0000	936.4125	1000111 0000
935.4250	0100010 0000	935.9250	0101001 0000	936.4250	0100111 0000
935.4375	1100010 0000	935.9375	1101001 0000	936.4375	1100111 0000
935.4500	0010010 0000	935.9500	0011001 0000	936.4500	0010111 0000
935.4625	1010010 0000	935.9625	1011001 0000	936.4625	1010111 0000
935.4750	0110010 0000	935.9750	0111001 0000	936.4750	0110111 0000
935.4875	1110010 0000	935.9875	1111001 0000	936.4875	1110111 0000
935.5000	0001010 0000	936.0000	0000101 0000	936.5000	0001111 0000

0 = CLOSED or ON 1 = OPEN or OFF

TX(MHZ)	S1,1-7 S2,1-4	TX(MHZ)	S1,1-7 S2,1-4	TX(MHZ)	S1,1-7 S2,1-4
936.5125	1001111 0000	937.0125	1000010 1000	937.5125	1001001 1000
936.5250	0101111 0000	937.0250	0100010 1000	937.5250	0101001 1000
936.5375	1101111 0000	937.0375	1100010 1000	937.5375	1101001 1000
936.5500	0011111 0000	937.0500	0010010 1000	937.5500	0011001 1000
936.5625	1011111 0000	937.0625	1010010 1000	937.5625	1011001 1000
936.5750	0111111 0000	937.0750	0110010 1000	937.5750	0111001 1000
936.5875	1111111 0000	937.0875	1110010 1000	937.5875	1111001 1000
936.6000	0000000 1000	937.1000	0001010 1000	937.6000	0000101 1000
936.6125	1000000 1000	937.1125	1001010 1000	937.6125	1000101 1000
936.6250	0100000 1000	937.1250	0101010 1000	937.6250	0100101 1000
936.6375	1100000 1000	937.1375	1101010 1000	937.6375	1100101 1000
936.6500	0010000 1000	937.1500	0011010 1000	937.6500	0010101 1000
936.6625	1010000 1000	937.1625	1011010 1000	937.6625	1010101 1000
936.6750	0110000 1000	937.1750	0111010 1000	937.6750	0110101 1000
936.6875	1110000 1000	937.1875	1111010 1000	937.6875	1110101 1000
936.7000	0001000 1000	937.2000	0000110 1000	937.7000	0001101 1000
936.7125	1001000 1000	937.2125	1000110 1000	937.7125	1001101 1000
936.7250	0101000 1000	937.2250	0100110 1000	937.7250	0101101 1000
936.7375	1101000 1000	937.2375	1100110 1000	937.7375	1101101 1000
936.7500	0011000 1000	937.2500	0010110 1000	937.7500	0011101 1000
936.7625	1011000 1000	937.2625	1010110 1000	937.7625	1011101 1000
936.7750	0111000 1000	937.2750	0110110 1000	937.7750	0111101 1000
936.7875	1111000 1000	937.2875	1110110 1000	937.7875	1111101 1000
936.8000	0000100 1000	937.3000	0001110 1000	937.8000	0000011 1000
936.8125	1000100 1000	937.3125	1001110 1000	937.8125	1000011 1000
936.8250	0100100 1000	937.3250	0101110 1000	937.8250	0100011 1000
936.8375	1100100 1000	937.3375	1101110 1000	937.8375	1100011 1000
936.8500	0010100 1000	937.3500	0011110 1000	937.8500	0010011 1000
936.8625	1010100 1000	937.3625	1011110 1000	937.8625	1010011 1000
936.8750	0110100 1000	937.3750	0111110 1000	937.8750	0110011 1000
936.8875	1110100 1000	937.3875	1111110 1000	937.8875	1110011 1000
936.9000	0001100 1000	937.4000	0000001 1000	937.9000	0001011 1000
936.9125	1001100 1000	937.4125	1000001 1000	937.9125	1001011 1000
936.9250	0101100 1000	937.4250	0100001 1000	937.9250	0101011 1000
936.9375	1101100 1000	937.4375	1100001 1000	937.9375	1101011 1000
936.9500	0011100 1000	937.4500	0010001 1000	937.9500	0011011 1000
936.9625	1011100 1000	937.4625	1010001 1000	937.9625	1011011 1000
936.9750	0111100 1000	937.4750	0110001 1000	937.9750	0111011 1000
936.9875	1111100 1000	937.4875	1110001 1000	937.9875	1111011 1000
937.0000	0000010 1000	937.5000	0001001 1000	938.0000	0000111 1000

0 = CLOSED or ON 1 = OPEN or OFF

TX(MHZ)	S1,1-7 S2,1-4	TX(MHZ)	S1,1-7 S2,1-4	TX(MHZ)	S1,1-7 S2,1-4
938.0125	1000111 1000	938.5125	1001100 0100	939.0125	1000001 0100
938.0250	0100111 1000	938.5250	0101100 0100	939.0250	0100001 0100
938.0375	1100111 1000	938.5375	1101100 0100	939.0375	1100001 0100
938.0500	0010111 1000	938.5500	0011100 0100	939.0500	0010001 0100
938.0625	1010111 1000	938.5625	1011100 0100	939.0625	1010001 0100
938.0750	0110111 1000	938.5750	0111100 0100	939.0750	0110001 0100
938.0875	1110111 1000	938.5875	1111100 0100	939.0875	1110001 0100
938.1000	0001111 1000	938.6000	0000010 0100	939.1000	0001001 0100
938.1125	1001111 1000	938.6125	1000010 0100	939.1125	1001001 0100
938.1250	0101111 1000	938.6250	0100010 0100	939.1250	0101001 0100
938.1375	1101111 1000	938.6375	1100010 0100	939.1375	1101001 0100
938.1500	0011111 1000	938.6500	0010010 0100	939.1500	0011001 0100
938.1625	1011111 1000	938.6625	1010010 0100	939.1625	1011001 0100
938.1750	0111111 1000	938.6750	0110010 0100	939.1750	0111001 0100
938.1875	1111111 1000	938.6875	1110010 0100	939.1875	1111001 0100
938.2000	0000000 0100	938.7000	0001010 0100	939.2000	0000101 0100
938.2125	1000000 0100	938.7125	1001010 0100	939.2125	1000101 0100
938.2250	0100000 0100	938.7250	0101010 0100	939.2250	0100101 0100
938.2375	1100000 0100	938.7375	1101010 0100	939.2375	1100101 0100
938.2500	0010000 0100	938.7500	0011010 0100	939.2500	0010101 0100
938.2625	1010000 0100	938.7625	1011010 0100	939.2625	1010101 0100
938.2750	0110000 0100	938.7750	0111010 0100	939.2750	0110101 0100
938.2875	1110000 0100	938.7875	1111010 0100	939.2875	1110101 0100
938.3000	0001000 0100	938.8000	0000110 0100	939.3000	0001101 0100
938.3125	1001000 0100	938.8125	1000110 0100	939.3125	1001101 0100
938.3250	0101000 0100	938.8250	0100110 0100	939.3250	0101101 0100
938.3375	1101000 0100	938.8375	1100110 0100	939.3375	1101101 0100
938.3500	0011000 0100	938.8500	0010110 0100	939.3500	0011101 0100
938.3625	1011000 0100	938.8625	1010110 0100	939.3625	1011101 0100
938.3750	0111000 0100	938.8750	0110110 0100	939.3750	0111101 0100
938.3875	1111000 0100	938.8875	1110110 0100	939.3875	1111101 0100
938.4000	0000100 0100	938.9000	0001110 0100	939.4000	0000011 0100
938.4125	1000100 0100	938.9125	1001110 0100	939.4125	1000011 0100
938.4250	0100100 0100	938.9250	0101110 0100	939.4250	0100011 0100
938.4375	1100100 0100	938.9375	1101110 0100	939.4375	1100011 0100
938.4500	0010100 0100	938.9500	0011110 0100	939.4500	0010011 0100
938.5625	1010100 0100	938.9625	1011110 0100	939.4625	1010011 0100
938.4750	0110100 0100	938.9750	0111110 0100	939.4750	0110011 0100
938.4875	1110100 0100	938.9875	1111110 0100	939.4875	1110011 0100
938.5000	0001100 0100	939.0000	0000001 0100	939.5000	0001011 0100

0 = CLOSED or ON 1 = OPEN or OFF

TX(MHZ)	S1,1-7 S2,1-4	TX(MHZ)	S1,1-7 S2,1-4	TX(MHZ)	S1,1-7 S2,1-4
939.5125	1001011 0100	939.6750	0110111 0100	939.8375	1100000 1100
939.5250	0101011 0100	939.6875	1110111 0100	939.8500	0010000 1100
939.5375	1101011 0100	939.7000	0001111 0100	939.8625	1010000 1100
939.5500	0011011 0100	939.7125	1001111 0100	939.8750	0110000 1100
939.5625	1011011 0100	939.7250	0101111 0100	939.8875	1110000 1100
939.5750	0111011 0100	939.7375	1101111 0100	939.9000	0001000 1100
939.5875	1111011 0100	939.7500	0011111 0100	939.9125	1001000 1100
939.6000	0000111 0100	939.7625	1011111 0100	939.9250	0101000 1100
939.6125	1000111 0100	939.7750	0111111 0100	939.9375	1101000 1100
939.6250	0100111 0100	939.7875	1111111 0100	939.9500	0011000 1100
939.6375	1100111 0100	939.8000	0000000 1100	939.9625	1011000 1100
939.6500	0010111 0100	939.8125	1000000 1100	939.9750	0111000 1100
939.6625	1010111 0100	939.8250	0100000 1100	939.9875	1111000 1100

0 = CLOSED or ON 1 = OPEN or OFF

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APPENDIX B

PARTS LIST
OUTLINE & SCHEMATIC DIAGRAMS
ADJUSTMENT AND TEST POINTS

TABLE OF CONTENTS

GETC SHELF ASSEMBLY
19D901868G3
(EDACS 900 APPLICATIONS)

ISSUE 1

SYMBOL	PART NO.	DESCRIPTION
		GETC LOGIC BOARD 19D902104G1
		- - - - - - - - - - CAPACITORS - - - - - - - - - -
C1 and C2	19A701624P118	Ceramic: 27 pF ±5%, 500 VDCW, temp coef N80 ±30 PPM/°C.
C3	19A702250P111	Polyester: .047 uF ±10%, 50 VDCW.
C5	19A701534P3	Tantalum: 0.47 uF ±20%, 35 VDCW.
C6	T644ACP247J	Polyester: .0047 uF ±5%, 50 VDCW.
C7	T644ACP310J	Polyester: .010 uF ±5%, 50 VDCW.
C8	T644ACP210J	Polyester: .0010 uF ±5%, 50 VDCW.
C9	T644ACP310J	Polyester: .010 uF ±5%, 50 VDCW.
C10	19A701534P19	Tantalum: 47 uF ±20%, 10 VDCW.
C11 thru C13	19A701534P8	Tantalum: 22 uF ±20%, 16 VDCW.
C14 thru C26	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
C28	19A701534P7	Tantalum: 10 uF ±20%, 16 VDCW.
C30 thru C34	T644ACP310J	Polyester: .010 uF ±5%, 50 VDCW.
C35	19A701534P7	Tantalum: 10 uF ±20%, 16 VDCW.
C36	19A701534P9	Tantalum: 47 uF ±20%, 6.3 VDCW.
C37 thru C41	T644ACP310J	Polyester: .010 uF ±5%, 50 VDCW.
C43 thru C46	T644ACP247J	Polyester: .0047 uF ±5%, 50 VDCW.
C47	19A701534P7	Tantalum: 10 uF ±20%, 16 VDCW.
C48	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
C49	19A701534P7	Tantalum: 10 uF ±20%, 16 VDCW.
C51	19A701534P7	Tantalum: 10 uF ±20%, 16 VDCW.
C52	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
C53	19A701534P7	Tantalum: 10 uF ±20%, 16 VDCW.
C54 *	5496267P16	Tantalum: 100 uF ±20%, 20 VDCW; sim to Sprague Type 150D.
C55	19A701534P2	Tantalum: 0.22 uF ±20%, 35 VDCW.
C56	19A701534P4	Tantalum: 1 uF ±20%, 35 VDCW.
C57	19A701534P8	Tantalum: 22 uF ±20%, 16 VDCW.
C58	19A701534P6	Tantalum: 4.7 uF ±20%, 35 VDCW.
C59	19A701534P6	Tantalum: 22 uF ±20%, 16 VDCW.
C60	19A701534P6	Tantalum: 4.7 uF ±20%, 35 VDCW.
C61 and C62	19A701534P8	Tantalum: 22 uF ±20%, 16 VDCW.
C63	19A701534P6	Tantalum: 4.7 uF ±20%, 35 VDCW.
C64	19A701534P8	Tantalum: 22 uF ±20%, 16 VDCW.
C65 *	5496267P16	Tantalum: 100 uF ±20%, 20 VDCW; sim to Sprague Type 150D.
C66 thru C68	19A703314P4	Electrolytic: 47 uF -10+50%, 16 VDCW; sim to Panasonic LS Series.
C70 thru C83	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
C84	T644ACP247J	Polyester: .0047 uF ±5%, 50 VDCW.
C85	T644ACP310J	Polyester: .010 uF ±5%, 50 VDCW.
C86	T644ACP210J	Polyester: .0010 uF ±5%, 50 VDCW.
C87	T644ACP310J	Polyester: .010 uF ±5%, 50 VDCW.
C88	19A701534P19	Tantalum: 47 uF ±20%, 10 VDCW.
C89 *	19A701534P7	Tantalum: 10 uF ±20%, 16 VDCW.
C100 * thru C103 *	T644ACP310K	Polyester: .010 uF ±10%, 50 VDCW.
		- - - - - - - - - - DIODES - - - - - - - - - -
D3 thru D8	19A700028P1	Silicon: 75 mA, 75 PIV; sim to 1N4148.
D9	19A700025P2	Silicon, zener: 400 mW max; sim to BZX55-C2V7.
D10 thru D13	19A700630P2	Silicon: sim to 1N4736A.
D14 thru D17	19A700028P1	Silicon: 75 mA, 75 PIV; sim to 1N4148.
D19 thru D21	19A700028P1	Silicon: 75 mA, 75 PIV; sim to 1N4148.
D22 and D23	T324ADP1041	Silicon: General Purpose Rectifier; sim to 1N4004.
D24 thru D28	19A700028P1	Silicon: 75 mA, 75 PIV; sim to 1N4148.
D29 thru D35	T324ADP1041	Silicon: General Purpose Rectifier; sim to 1N4004.
D36	19A700028P1	Silicon: 75 mA, 75 PIV; sim to 1N4148.
D37 *	19A700025P7	Silicon, zener: 400 mW max; sim to BZX55-C5V6.
D38 *	19A700028P1	Silicon: 75 mA, 75 PIV; sim to 1N4148.
		- - - - - - - - - - LEDS - - - - - - - - - -
H1 thru H7	162B3011P0002	Light Emitting Diode: Red; sim to GE 22L-2.
		- - - - - - - - - - JACKS - - - - - - - - - -
J3 *	19A705181P1	Connector: 64 contacts; sim to Burndx Cat. RP196B32B160S3.
J6 and J7	19A704852P146	Connector, printed wire, two part: 16 contacts; sim to Dupont Berg 22-12-2164.
J8 and J9	19A704852P136	Connector, printed wire, two part: 6 contacts; sim to Dupont Berg 22-12-2064.
J10	19A116659P173	Printed wire, two part: 4 contacts, sim to Molex 09-75-1041.
J11 thru J18	19A703248P12	Post: Gold Plated, 13 mm length.
J19	19A704852P136	Connector, printed wire, two part: 6 contacts; sim to Dupont Berg 22-12-2064.
J20 thru J22	19A703248P12	Post: Gold Plated, 13 mm length.
J24 thru J26	19A703248P12	Post: Gold Plated, 13 mm length.
J27	19A704852P136	Connector, printed wire, two part: 6 contacts; sim to Dupont Berg-22-12-2064.
J28 and J29	19A703248P12	Post: Gold Plated, 13 mm length.
J40	19A703248P12	Post: Gold Plated, 13 mm length.
J44	19A703248P12	Post: Gold Plated, 13 mm length.
J46 * thru J48	19A703248P17	Post: Gold Plated, 13 mm length.
J49	19A704779P59	Connector, printed wiring: 10 contacts; sim to Molex 22-18-2103.
J50 thru J55	19A703248P12	Post: Gold Plated, 13 mm length.
J60 * thru J73	19A703248P12	Post: Gold Plated, 13 mm length.
Q2 thru Q6	19A700023P2	- - - - - - - - - - TRANSISTORS - - - - - - - - - - Silicon, NPN: sim to 2N3904.
Q7	19A702503P2	Silicon, NPN.
Q8 thru Q10	19A700023P2	Silicon, NPN: sim to 2N3904.
Q11	19A700022P2	Silicon, PNP: sim to 2N3906.
Q12	19A116375P1	Silicon, PNP.
Q13	19A700054P1	Silicon, NPN: sim to BD-201.
Q14 and Q15	19A700023P2	Silicon, NPN: sim to 2N3904.
Q16	19A702503P2	Silicon, NPN.
Q17	19A700022P2	Silicon, PNP: sim to 2N3906.
Q18	19A700023P2	Silicon, NPN: sim to 2N3904.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1	19B800784P106	Variable: 5K ohms ±20%, 1/2 w.
R2	19B800784P105	Variable: 1K ohms ±20%, .5 w.
R6 and R7	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R8 and R9	19A701630P2	Network: 9 resistors rated 10K ohms ±2%, 50 VDCW; sim to Bourns 4310R-101-103.
R10	H212CRP510C	Deposited carbon: 1M ohms ±5%, 1/4 w.
R12	19A701537P1	Composition: 10M ohms ±5%, 1/4 w.
R13	19A701250P446	Metal film: 294K ohm ±1%, 1/4 w.
R14	H212CRP322C	Deposited carbon: 22K ohms ±5%, 1/4 w.
R15	19A701537P1	Composition: 10M ohms ±5%, 1/4 w.
R16	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R17	19A701250P273	Metal film: 5.6K ohms ±1%, 1/4 w.
R18	H212CRP147C	Deposited carbon: 470 ohms ±5%, 1/4 w.
R19	19A701250P301	Metal film: 10K ohms ±1%, 1/4 w.
R20 and R21	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R22	19A701537P1	Composition: 10M ohms ±5%, 1/4 w.
R25 and R26	H212CRP347C	Deposited carbon: 47K ohms ±5%, 1/4 w.
R27	19A701250P269	Metal film: 5.11K ohms ±1%, 1/4 w.
R28	19A701250P201	Metal film: 1K ohms ±1%, 1/4 w.
R29	19A701250P327	Metal film: 16.5K ohms ±1%, 1/4 w.
R30	19A701250P210	Metal film: 1240 ohms ±1%, 1/4 w.
R31	19B235029P8	Variable: 10K ohms, ±10%, 1/2 w.
R32	H212CRP510C	Deposited carbon: 1M ohms ±5%, 1/4 w.
R33	H212CRP239C	Deposited carbon: 3.9K ohms ±5%, 1/4 w.
R36	19A701250P176	Metal film: 604 ohms ±1%, 1/4 w.
R38	H212CRP122C	Deposited carbon: 220 ohms ±5%, 1/4 w.
R39 and R40	19A701630P2	Network: 9 resistors rated 10K ohms ±2%, 50 VDCW; sim to Bourns 4310R-101-103.
R41	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R42	H212CRP222C	Deposited carbon: 2.2K ohms ±5%, 1/4 w.
R43	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R44 thru R53	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R54 thru R59	H212CRP356C	Deposited carbon: 560 ohms ±5%, 1/4 w.
R60 *	H212CRP312C	Deposited carbon: 12K ohms ±5%, 1/4 w.
R61	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R62 *	H212CRP147C	Deposited carbon: 470 ohms ±5%, 1/4 w.
R63	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R64 *	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R67	H212CRP247C	Deposited carbon: 4.7K ohms ±5%, 1/4 w.
R68	H212CRP318C	Deposited carbon: 18K ohms ±5%, 1/4 w.
R69	19A701250P388	Metal film: 80.6K ohms ±1%, 1/4 w.
R70	19A701250P358	Metal film: 2.7 ohms ±5%, 1/4 w.
R71	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R72	19A701250P384	Metal film: 73.2K ohms ±1%, 1/4 w.
R73	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R74	19A701250P391	Metal film: 86.6K ohms ±1%, 1/4 w.
R75	19A701250P325	Metal film: 17.8K ohms ±1%, 1/4 w.
R76	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R77	19A701250P382	Metal film: 69.8K ohms ±1%, 1/4 w.
R78	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R79	19A701250P350	Metal film: 32.4K ohms ±1%, 1/4 w.
R80 thru R83	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R84	H212CRP382C	Deposited carbon: 82K ohms ±5%, 1/4 w.
R85	H212CRP318C	Deposited carbon: 18K ohms ±5%, 1/4 w.
R86	19A701250P388	Metal film: 80.6K ohms ±1%, 1/4 w.
R87	19A701250P358	Metal film: 2.7 ohms ±5%, 1/4 w.
R88	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R89	19A701250P384	Metal film: 73.2K ohms ±1%, 1/4 w.
R90	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R91	19A701250P391	Metal film: 86.6K ohms ±1%, 1/4 w.
R92	19A701250P325	Metal film: 17.8K ohms ±1%, 1/4 w.
R93	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R94	19A701250P382	Metal film: 69.8K ohms ±1%, 1/4 w.
R95	19A701250P383	Metal film: 71.5K ohms ±1%, 1/4 w.
R96	19A701250P350	Metal film: 32.4K ohms ±1%, 1/4 w.
R97 and R98	H212CRP310C	Deposited carbon: ohms ±5%, 1/4 w.
R99	H212CRP347C	Deposited carbon: 47K ohms ±5%, 1/4 w.
R100	H212CRP410C	Deposited carbon: 100K ohms ±5%, 1/4 w.
R101	H212CRP368C	Deposited carbon: 68K ohms ±5%, 1/4 w.
R103 thru R105	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R106	19A701250P224	Metal film: 1740 ohm ±1%, 1/4 w.
R107	19A701250P312	Metal film: 13K ohms ±1%, 1/4 w.
R108	19A701250P401	Metal film: 100K ohms ±1%, 1/4 w.
R109	19A701250P341	Metal film: 26.1K ohms ±1%, 1/4 w.
R110	19B800784P106	Variable: 5K ohms ±20%, 1/2 w.
R111	19A701250P224	Metal film: 1740 ohm ±1%, 1/4 w.
R112	19A701250P312	Metal film: 13K ohms ±1%, 1/4 w.
R113	19A701250P401	Metal film: 100K ohms ±1%, 1/4 w.
R114	19A701250P341	Metal film: 26.1K ohms ±1%, 1/4 w.
R115	19B800784P106	Variable: 5K ohms ±20%, 1/2 w.
R116	19A701250P201	Metal film: 1K ohms ±1%, 1/4 w.
R117 and R118	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R119	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R120	H212CRP133C	Deposited carbon: 330 ohms ±5%, 1/4 w.
R121	19A701630P2	Network: 9 resistors rated 10K ohms ±2% 50 VDCW; sim to Bourns 4310R-101-103.
R123 thru R125	H212CRP210C	Deposited carbon: 1K ohms ±5%, 1/4 w.
R126	19A700113P63	Composition: 1K ohms ±5%, 1/2 w.
R127	3R77B511J	Composition: 510 ohms ±5%, 1/2 w.
R128	19A700113P19	Composition: 15 ohms ±5%, 1/2 w.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

SYMBOL	PART NO.	DESCRIPTION
R129	19A701250P434	Metal film: 732K ohms ±1%, ½ w.
R130	19A700050P13	Wirewound: 1 ohm ±10%, 2 w.
R131	19A701250P301	Metal film: 10K ohms ±1%, 1/4 w.
R132	19A701250P266	Metal film: 4.75K ohms ±1%, 1/4 w.
R133	H212CRP330C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R134	H212CRP239C	Deposited carbon: 3.9K ohms ±5%, 1/4 w.
R135	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R136	5493035P2	Wirewound: 1 ohm ±5%, 5 w.
R137	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R138	H212CRP315C	Deposited carbon: 15K ohms ±5%, 1/4 w.
R139 and R140	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R141	19EB00784P108	Variable: 10K ohms ±20%, 1/2 w.
R142	H212CRP322C	Deposited carbon: 22K ohms ±5%, 1/4 w.
R143	19A701537P1	Composition: 10M ohms ±5%, 1/4 w.
R144	H212CRP347C	Deposited carbon: 47K ohms ±5%, 1/4 w.
R145	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R146	H212CRP222C	Deposited carbon: 2.2K ohms ±5%, 1/4 w.
R147	H212CRP368C	Deposited carbon: 68K ohms ±5%, 1/4 w.
R148 *	H212CRP310C	Deposited carbon: 10K ohms ±5%, 1/4 w.
R149	19A700384P1	Jumper.
R150 * thru R152 *	H212CRP312C	Deposited carbon: 12K ohms ±5%, 1/4 w.
R153 *	H212CRP239C	Deposited carbon: 3.9K ohms ±5%, 1/4 w.
		- - - - - - - - - - SWITCHES - - - - - - - -
S1 thru S3	19B800010P2	Dual-Inline-Package: 8 Circuits; sim to CTS 206-8.
S4	19A7D1324P1	Pushbutton: sim to IEE/Schadows 210091.
		- - - - - - - - - - TRANSFORMERS - - - - - -
T1 and T2	19A703656P1	Audio Frequency: sim to Nova Magnetics 5577-06-0001.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - -
U1	19A705557P1	Digital: Microcomputer; sim to P80C32.
U2	19A705595G6	Digital: 64K EPROM; sim to 27C512. (Programmed).
U3	19A705558P1	Digital: 8K x 8 RAM; sim to MCM6064P-12.
U4	19A704727P2	Digital: CMOS Modem.
U5	19A703471P2	Digital: Octal Data Latch; sim to 74HC373.
U6	19A703471P8	Digital: Octal Tri-State Transceiver; sim to 74HC245.
U7 thru U9	19A703471P1	Digital: Octal Tri-State Buffer; sim to 74HC244.
U10	19A700037P363	Digital: Dual 2 line to 1 line Decoder/Demultiplexer; sim to 74LS155.
U11 thru U13	19A700176P1	Digital: CMOS Hex Inverting Buffer/Converter; sim to 40490B.
U14	19A116704P1	Digital: Quad Line Driver; sim to 1488.
U15	19A700029P38	Digital: CMOS Triple 2 Channel Multiplexer.
U16	19A704883P1	Linear: Quad Op Amp; sim to MC3303P.
U17	19A134764P2	Linear: Dual Voltage Comparator; sim to LM393N.
U18	19A700086P4	Linear: Dual Op Amp; sim to 4558.
U19	19A704727P2	Digital: CMOS Modem.
U20 and U21	19A704380P11	Digital: Octal Data Flip-Flop; sim to 74HC273.
U22	19A703483P1	Digital: CMOS Quad 2-Input NOR Gate; sim to 74HC02.
U23 thru U26	19A116180P75	Digital: Hex Open Collector Inverter; sim to 7406.
U27	19A116704P2	Digital: Quad Line Receiver; sim to 1489.

SYMBOL	PART NO.	DESCRIPTION
U28	19A116704P1	Digital: Quad Line Driver; sim to 1488.
U29	19A700177P1	Digital: CMOS Hex Inverting Buffer/Converter; sim to 40490B.
U30	19A704883P1	Linear: Quad Op Amp; sim to MC3303P.
U31	19A134764P2	Linear: Dupl Voltage Comparator; sim.to LM393N.
U32 and U33	19A704883P1	Linear: Quad Op Amp; sim to MC3303P.
U34	19A700029P38	Digital: CMOS Triple 2 Channel Multiplexer.
U37	19A704883P1	Linear: Quad Op Amp; sim to MC3303P.
U38	19A704380P11	Digital: Octal Data Flip-Flop; sim to 74HC273.
U39	19A134718P2	Linear: -12 Volt Regulator; sim to uA7912U.
U40	19A134717P2	Linear: 12 Volt Regulator; sim to MC7812CT.
U41	19A700037P335	Digital: Dual Data Flip-Flop; sim to 74LS74A.
		- - - - - - - - - - SOCKETS - - - - - - - - - -
XU1	19A700156P5	Integrated circuit: 40 contacts; sim to Augat 540-AG39D.
XU2 thru XU4	19A700156P3	Integrated circuit: 28 contacts; sim to AMP 640362P3.
XU19	19A700156P3	Integrated circuit: 28 contacts; sim to AMP 640362P3.
XU35	19A700156P15	Integrated circuit: 8 positions; sim to Burndy 01LB 8P-108.
		- - - - - - - - - - CRYSTALS - - - - - - - - - -
Y1	19A702511G15	Quartz: 11.059200 MHz.
		- - - - - LOGIC BOARD MISCELLANEOUS - - - - -
		U39 and U40 Mounting Hardware:
5	N402P35B6	Washer: Flat.
7	N80P9005B6	Machine screw: pan head, steel.
8	N404P11B6	Lockwasher; internal: No. 4.
9	7141225P2	Hex nut: No. 4-40.
13	19A702917P7	Heat Sink.
6	19A703248P12	Post: Gold Plated, 13 mm length.
11	19A134521P1	Lens, red. (Used with H1 - H7).
12	19A134521P6	Support. (Used with H1 - H7).
14	19E232901P2	Support/Heat Sink. (Used with Q12 and Q13).
A2		**REGULATOR ASSEMBLY 19C336816G2**
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1 and R2	5493035P1	Wirewound: 5 ohms ±5%, 5 watt; sim to Hamilton Hall Type HR-5W.
		- - - - - - - - - - TERMINAL BOARDS - - - - - - - - - -
TR1 and TR2	7775500P11	Phen: 5 terminals.
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - -
U1 and U2	19A134717P1	Linear: 5 Volt Regulator; sim to MC7805CT.
		- - - - - - - - - - CABLES - - - - - - - - - -
W1	19E234898G2	Cable Assembly. (includes P1).
		- - - - - REGULATOR ASSEMBLY MISCELLANEOUS - - - - -
2	19E234903G1	Heat Sink Assembly.
3	4038930P1	Clip. (Secures R1, R2).
7	7141225P2	Hex nut: No. 4-40.
8	N404P11B6	Lockwasher; internal: No. 4.
9	N80P9005B6	Machine screw: pan head, steel.

SYMBOL	PART NO.	DESCRIPTION
		- - - - - - SHELF ASSEMBLY MISCELLANEOUS - - - - - -
	19C851553G1	Tray Assembly.
	19C851587G1	Shelf.
	19A115594P2	Grommet.
	19A115204P1	Grease.
	19B235048P1	Ground Cable.

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuitry are identified by a "Revision Letter", which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the descriptions of parts affected by these revisions.

REV. A - GETC LOGIC BOARD 19D902104G1
To update board for FST and simulcast operation, made the following changes near Q15: Added D37, 5.6 volt zener diode, added R148 and changed R67 from 820 to 470 ohms. Also added various interconnections to the board needed for FST and simulcast operation.

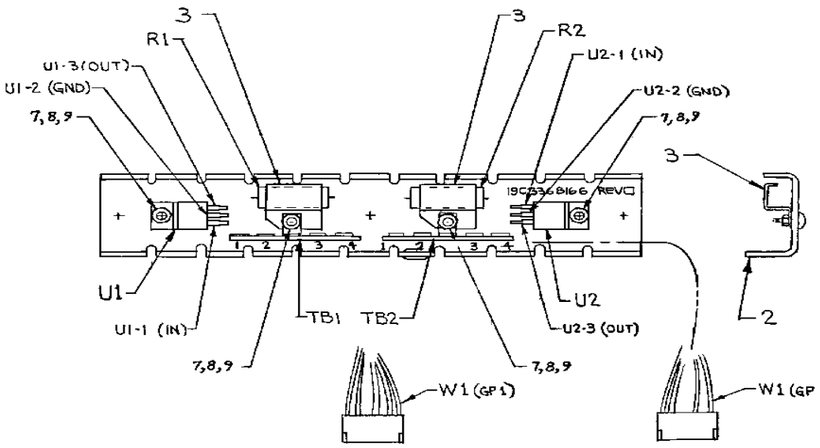
REV. B - GETC LOGIC BOARD 19D902104G1
To improve reset operation, added C99 in parallel with S4 RESET switch and R19. Also updated VG Voting Tone Board interconnections on schematic.

REV. C - GETC LOGIC BOARD 19D902104G1
Added pull-up R151 to the Reset line from J7 pin 3 to the 13.8 supply. Also added U37-C buffer to the Volume/Squelch High input at J7 pin 2.

REV. D - GETC LOGIC BOARD 19D902104G1
To update board for simulcast operation, eliminate RP1 in Inverter Supply circuit, and improve BSY waveform, made the following changes: Added J72 and J73; deleted pin 3 of J3, J45 and J68; changed K64 to 1K ohms; changed C54 and C65 to 100 uF; added R150, R152 and R153; and added D38.

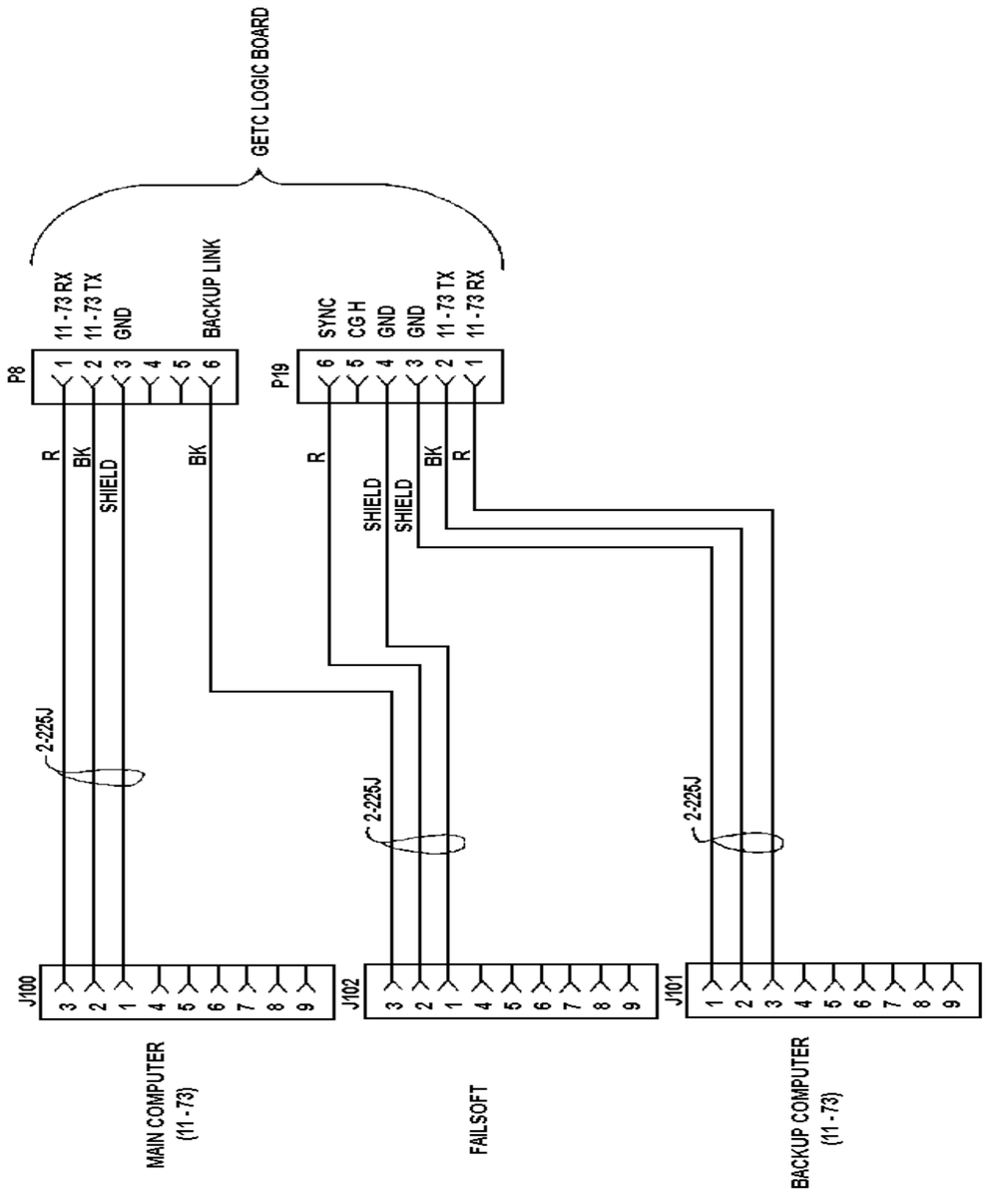
REV. E - LOGIC BOARD 19D902104G1
To stabilize low speed data encode and decode filters, added C100 and C101 (.01 uF capacitors) at H30-C and H33-D respectively.

REV. F - LOGIC BOARD 19D902104G1
To improve inbound data signalling changed R60 at U15 pin 5 from 1.5K ohms (H212CRP215C) to 12K ohms (H212CRP312C).

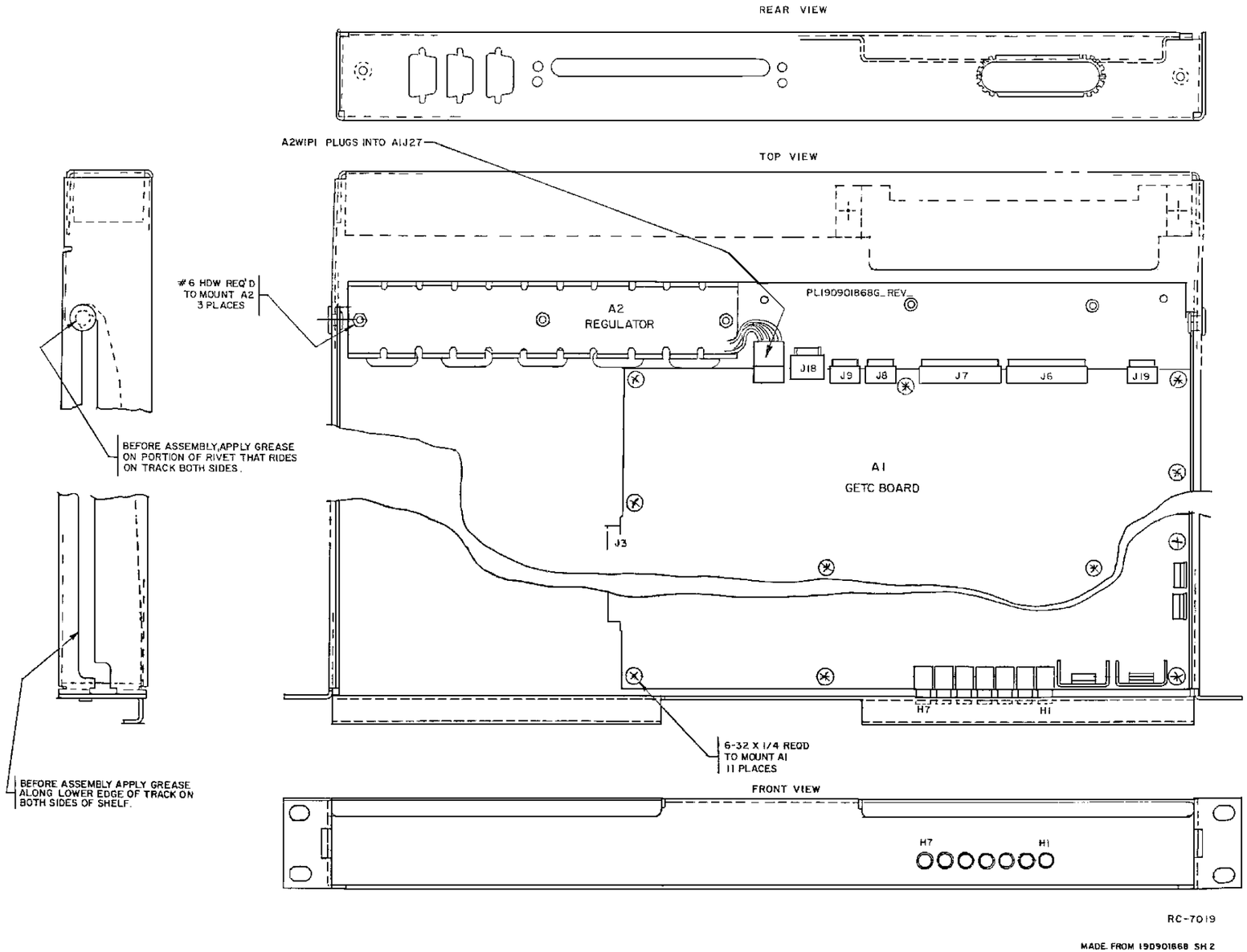


WIRING CHART			
WIRE	FROM	TO	REMARKS
ST22-W	U1-1	TB1-1	+5V R.M. INPUT
R1	TB1-1	TB2-1	
W1-W	W1P1-2	TB1-1	+5V R.M. INPUT
ST22-BK	U1-2	TB1-2	GND
ST22-BK	TB1-2	TB2-2	
ST22-BK	U2-2	TB2-2	
W1-BK	W1P1-3	TB1-2	
ST22-R	U1-3	TB1-3	+5V R.M.
W1-R	W1P1-1	TB1-3	
ST22-W	U2-1	TB2-4	+5V INPUT
R2	TB2-1	TB2-4	
W1-W	W1P1-5	TB2-4	+5V INPUT
ST22-BR	U2-3	TB2-3	+5V
W1-BR	W1P1-6	TB2-3	
W1-O	W1P1-4	TB2-1	+13.8V

REGULATOR ASSEMBLY
19C336816G2
(19C336816, Sh. 1, Rev. 6)

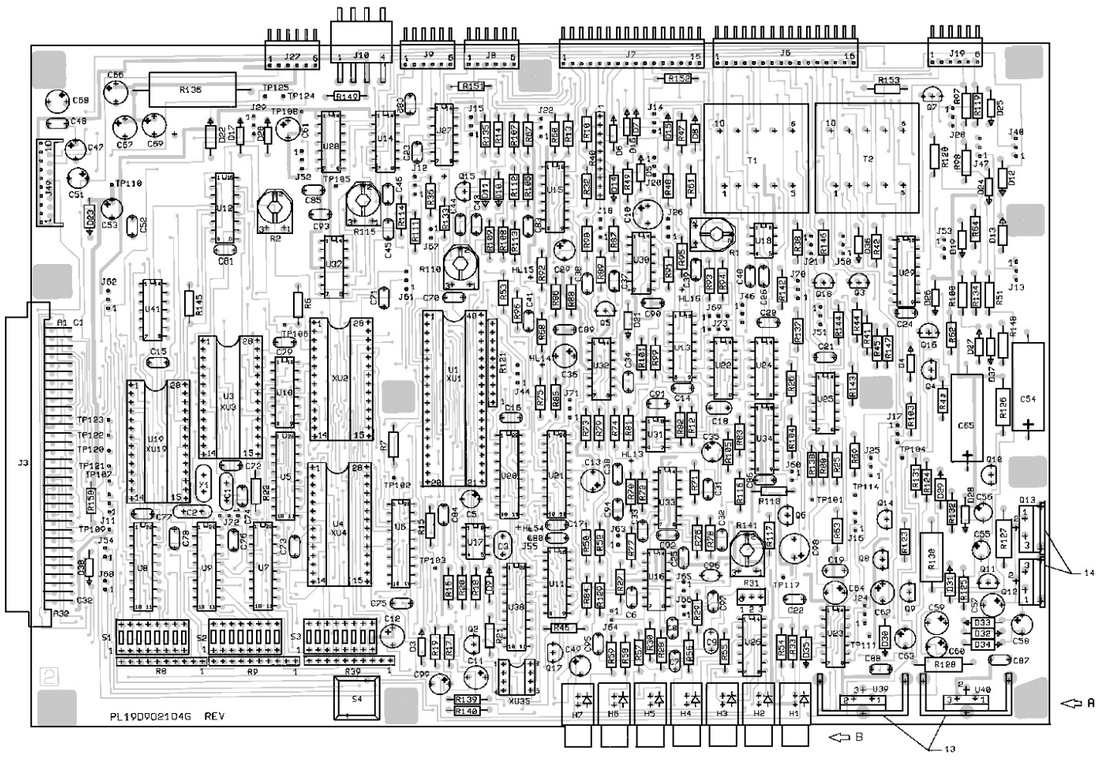


CABLE ASSEMBLY 19C336863G1
(19C336866, Sh. 1, Rev. 0)



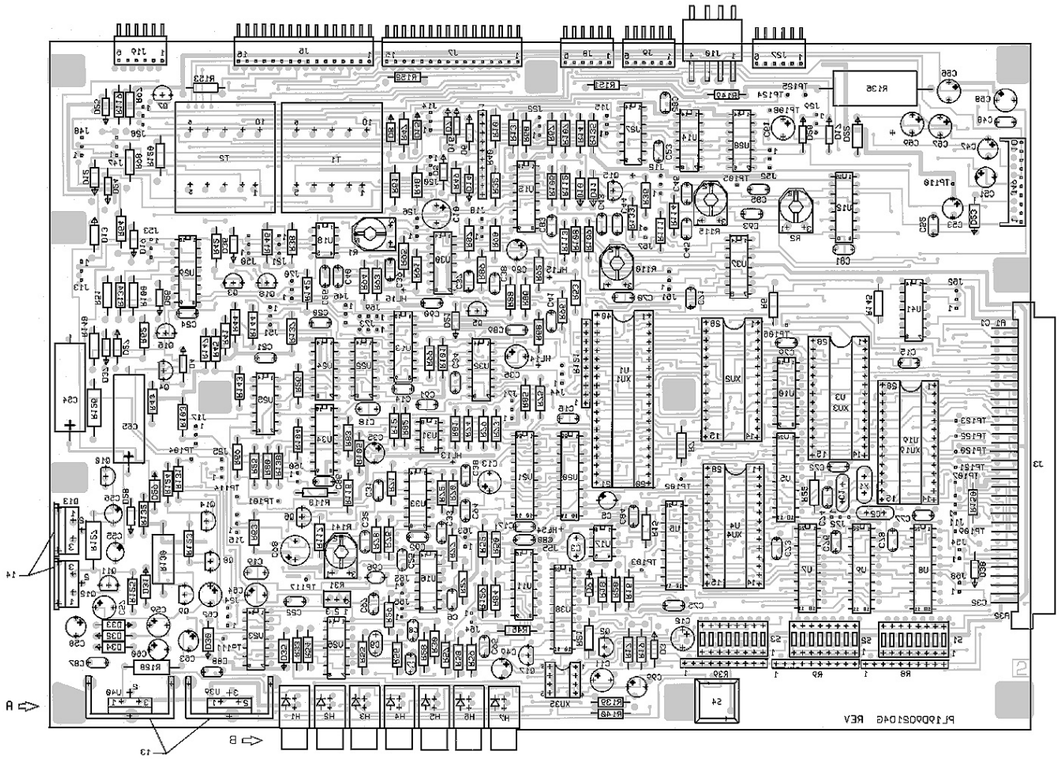
GETCSHELF 19D901868G3

COMPONENT SIDE

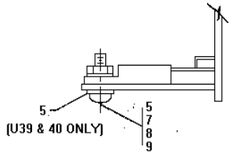


(19D902106, Rev. 4)
(19A705536, Sh. 2, Rev. 2)

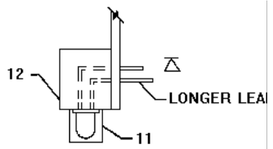
SOLDER SIDE



(19D902106, Rev. 4)
(19A705536, Sh. 3, Rev. 2)

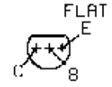


VIEW AT "A"
TYPICAL MOUNTING FOR
Q12, Q13, U39 & U40



VIEW AT "B"
TYPICAL MOUNTING FOR
H1 THRU H7

LEAD IDENTIFICATION
FOR Q2 - Q11 AND Q14 - Q18



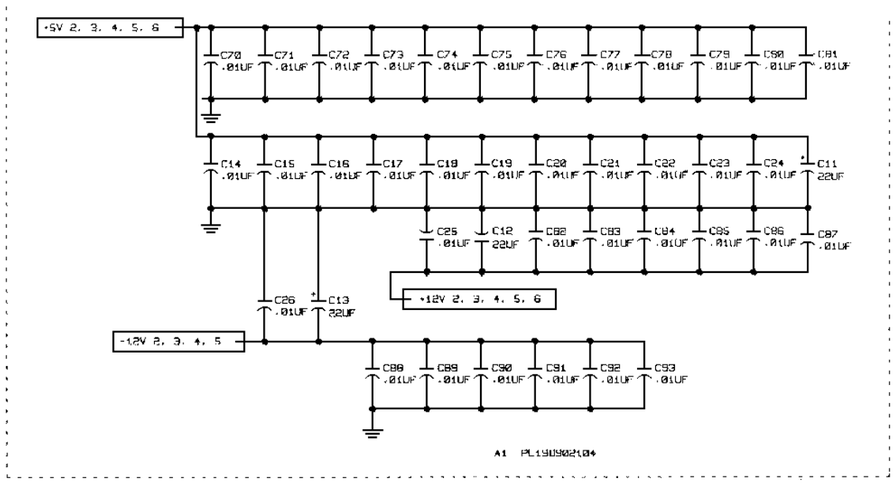
IN-LINE
TOP VIEW

NOTE: CASE SHAPE IS DETERMINING
FACTOR FOR LEAD IDENTIFICATION

CAUTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

GETC BOARD 19D902104G1

JUMPER	VG E/D, VG REM, VG RPT, VG REM/RPT, VG SAT RX, VG VOTED REM/RPT	VG VOTER SELECTOR	VG VOTER RX	PST TSIN, PST DOWNLINK, PST CC/WC	PST VOTER SELECTOR	PST VOTER DIG RX	PST SAT RX	PST SIMULCAST REMOTE	PST SIMULCAST CONTROL	800 MHZ TRUNKED
P11	1&2	1&2	1&2	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P12	1&2	1&2	1&2	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P13	2&3	2&3	2&3	1&2	2&3	2&3	2&3	1&2	1&2	1&2
P14	2&3	2&3	2&3	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P15	2&3	2&3	2&3	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P16	1&2	1&2	2&3	1&2	2&3	2&3	2&3	1&2	1&2	1&2
P17	2&3	2&3	2&3	1&2	1&2	1&2	1&2	2&3	1&2	1&2
P18	2&3	2&3	2&3	1&2	2&3	2&3	1&2	1&2	1&2	1&2
P20	2&3	2&3	2&3	1&2	1&2	1&2	1&2	OMIT	OMIT	1&2
P21	2&3	2&3	2&3	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P22	2&3	2&3	2&3	1&2	1&2	1&2	1&2	1&2	1&2	2&3
P24	2&3	2&3	2&3	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P25	2&3	2&3	2&3	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P26	2&3	2&3	2&3	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P28	2&3	2&3	2&3	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P29	1&2	OMIT	1&2	1&2	OMIT	OMIT	OMIT	1&2	1&2	1&2
P44	2&3	2&3	2&3	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P46	1&2	1&2	1&2	1&2	1&2	2&3	1&2	1&2	1&2	1&2
P47	1&2	1&2	2&3	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P48	1&2	2&3	1&2	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P50	1&2	2&3	1&2	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P51	2&3	2&3	2&3	2&3	2&3	2&3	1&2	2&3	2&3	1&2
P52	2&3	2&3	2&3	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P53	2&3	2&3	2&3	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P54	1&2	1&2	1&2	1&2	1&2	1&2	1&2	OMIT	OMIT	1&2
P55	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	1&2	OMIT	OMIT
P60	1&2	1&2	1&2	1&2	1&2	1&2	1&2	OMIT	1&2	1&2
P61	1&2	1&2	1&2	2&3	1&2	1&2	2&3	2&3	2&3	2&3
P62	1&2	1&2	1&2	1&2	1&2	1&2	1&2	OMIT	OMIT	2&3
P63	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	1&2
P64	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	1&2
P65	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	1&2
P66	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	OMIT	1&2
P67	OMIT	OMIT	OMIT	1&2	1&2	1&2	1&2	1&2	1&2	OMIT
P68	1&2	1&2	1&2	1&2	1&2	1&2	1&2	OMIT	1&2	1&2
P69	1&2	1&2	1&2	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P70	1&2	1&2	1&2	1&2	1&2	1&2	1&2	1&2	1&2	1&2
P71	1&2	1&2	1&2	1&2	1&2	1&2	1&2	2&3	1&2	1&2
P72	1&2	1&2	1&2	1&2	1&2	1&2	1&2	2&3	1&2	1&2
P73	1&2	1&2	1&2	1&2	1&2	1&2	1&2	2&3	2&3	1&2



MODEL NO.	REV LETTER
PI.19D902104G1	F

ALL RESISTORS ARE 1/4 WATT UNLESS OTHERWISE
RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY MULTIPLIER K OR M.
CAPACITOR VALUES IN F UNLESS FOLLOWED BY MULTIPLIER U,N OR P.
INDUCTANCE VALUES IN H UNLESS FOLLOWED BY MULTIPLIER M OR U.

NOTES:

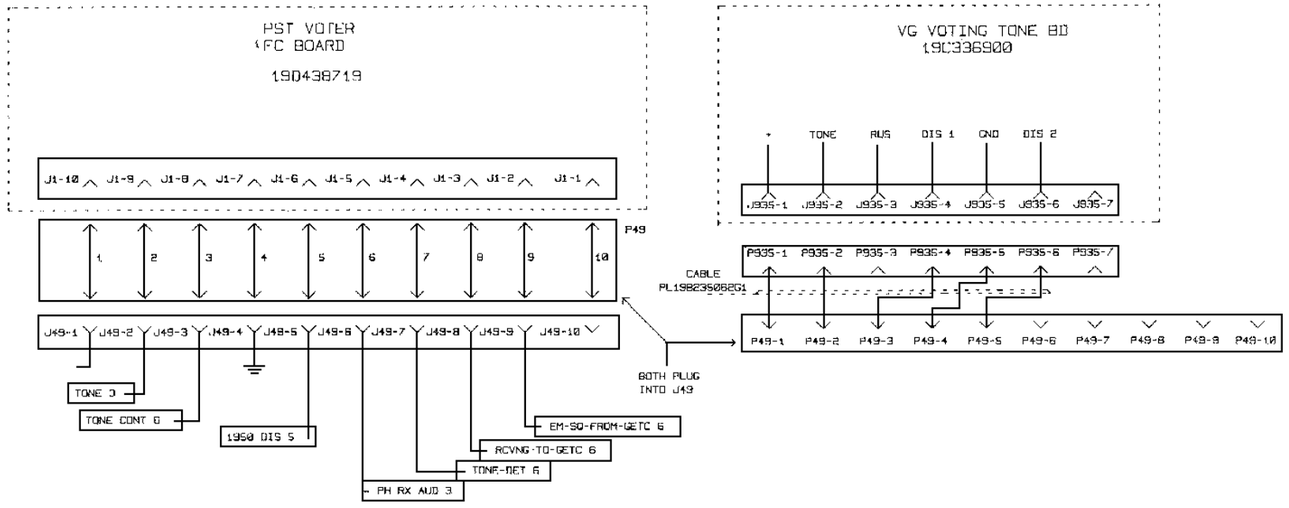
4 FOR JUMPER PLACEMENT, SEE JUMPER CHART.

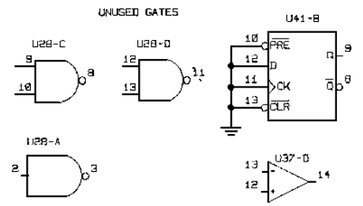
5 FOR A 6116 RAM (24 PINS), OFFSET DOWNWARD IN THE 28 PIN SOCKET.

6 U35 NOT PRESENT. FOR FUTURE USE.

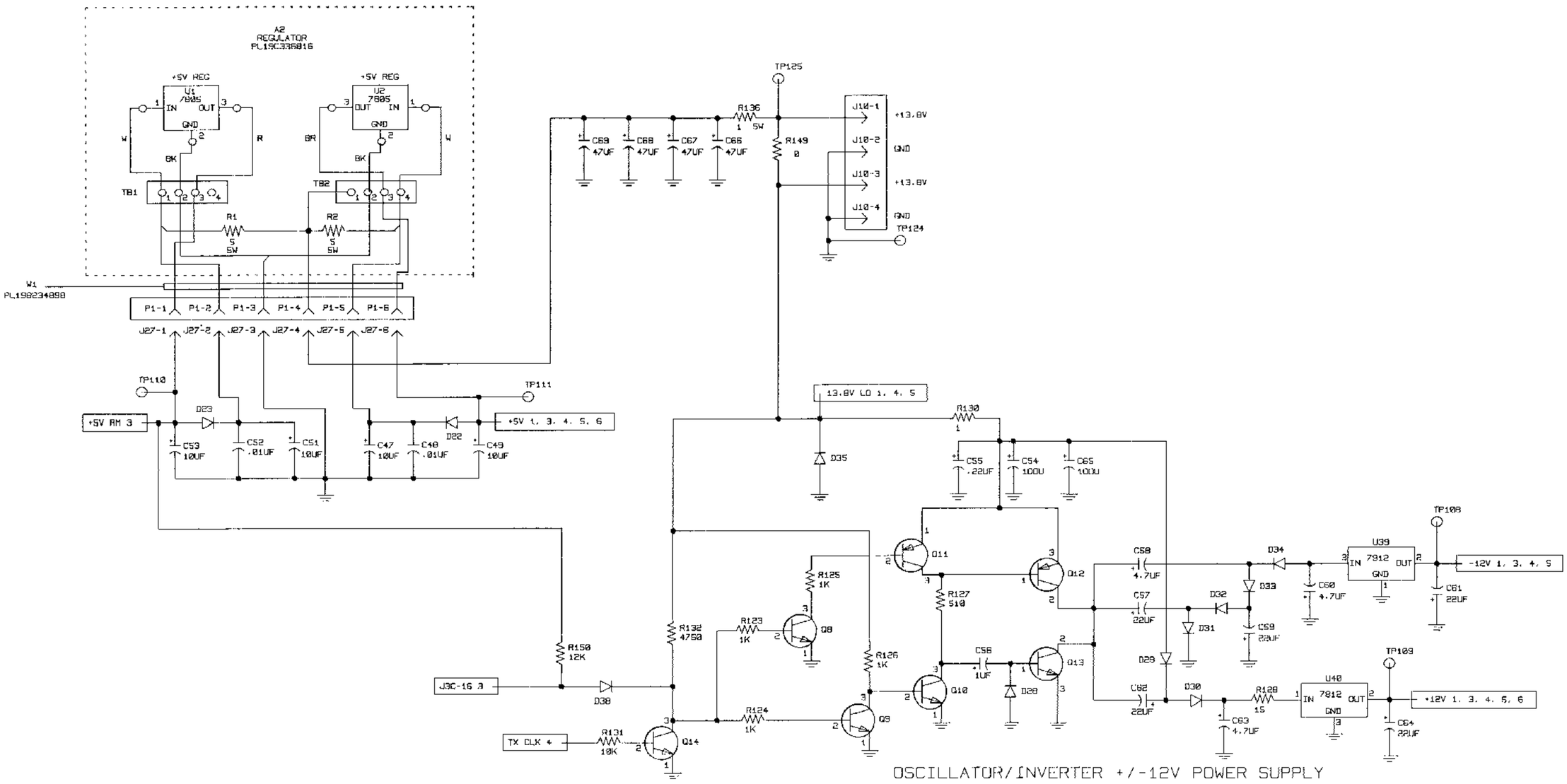
8 CONNECTIONS SHOWN FOR ROCKWELL MODEM COMMUNICATION. FOR RS232 COMMUNICATION CONNECT J11&J12 TO P11&P12-2&3.

DEVICE	GND PIN NO	+5V PIN NO	+12 PIN NO	-12 PIN NO
U1	20	40		
U2	14	28		
U3	14	26,28		
U4	13	15		
U5	10	20		
U6	10	20		
U7	10	20		
U8	10	20		
U9	10	20		
U10	8	16		
U11	8	1		
U12	8	1		
U13	8	1		
U14	7		14	1
U15	6,8		16	7
U16			4	11
U17	4		8	
U18			8	4
U19	13	15		
U20	10	20		
U21	10	20		
U22	7	14		
U23	7	14		
U24	7	14		
U25	7	14		
U26	7	14		
U27	7	14		
U28	7		14	1
U29	8	1		
U30			4	11
U31			8	4
U32	3,5		4	11
U33			4	11
U34	6,8		16	7
U35	4			
U37			4	11
U38	10	20		
U41	7	14		



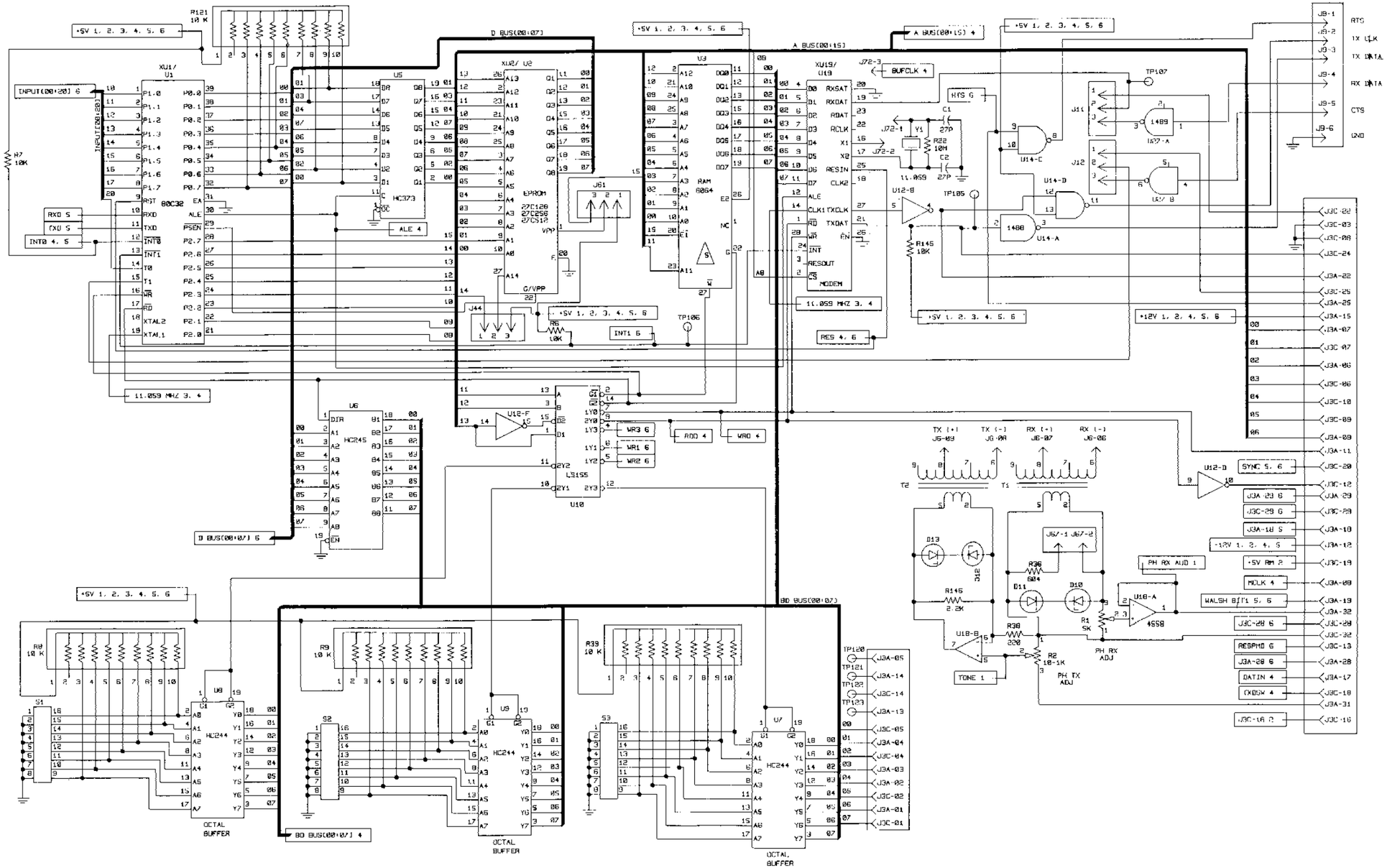


GETC SHELF 19D901868G3



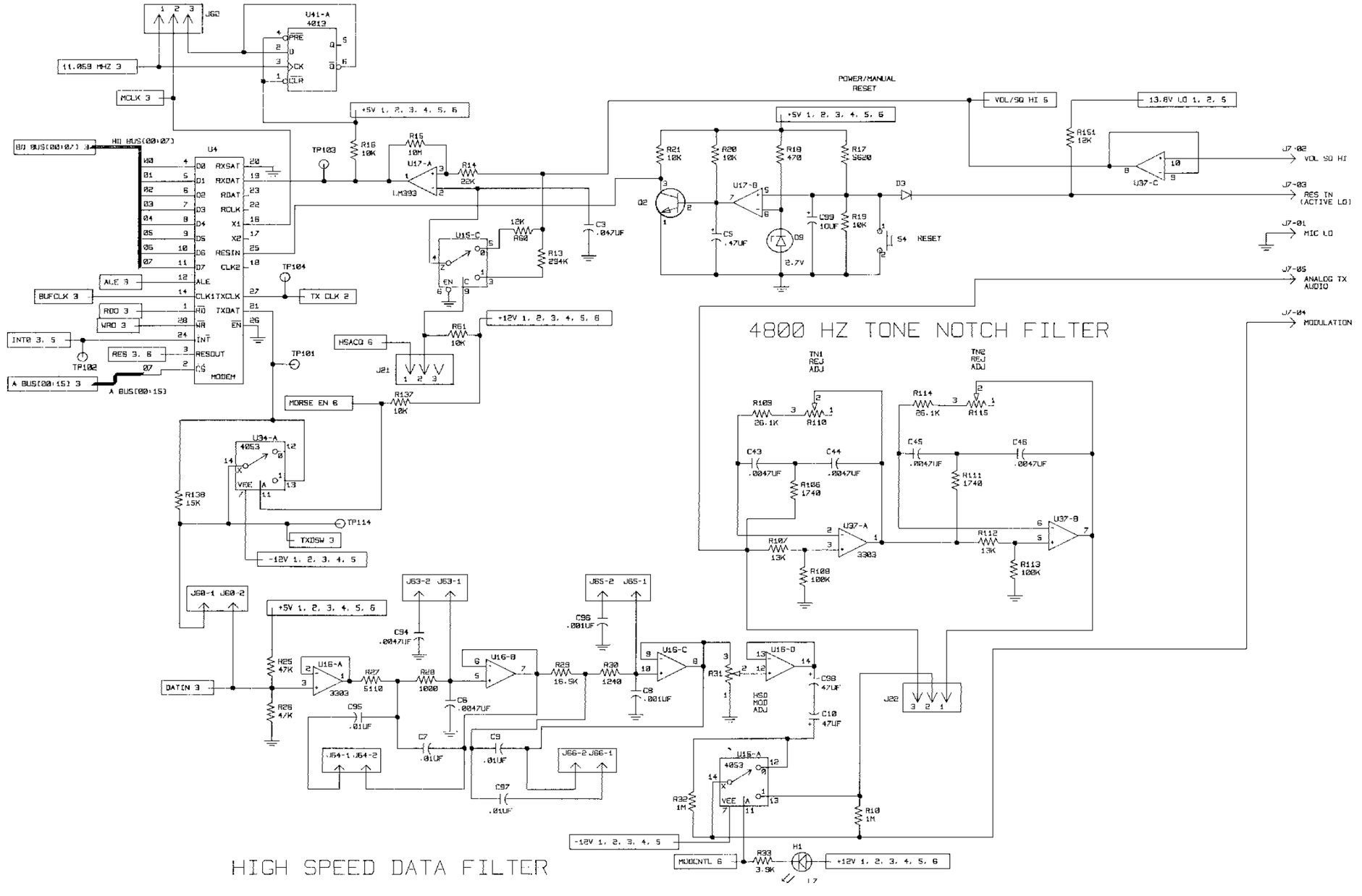
GETC SHELF 19D901868G3

(19D902106, Sh. 2, Rev. 3)



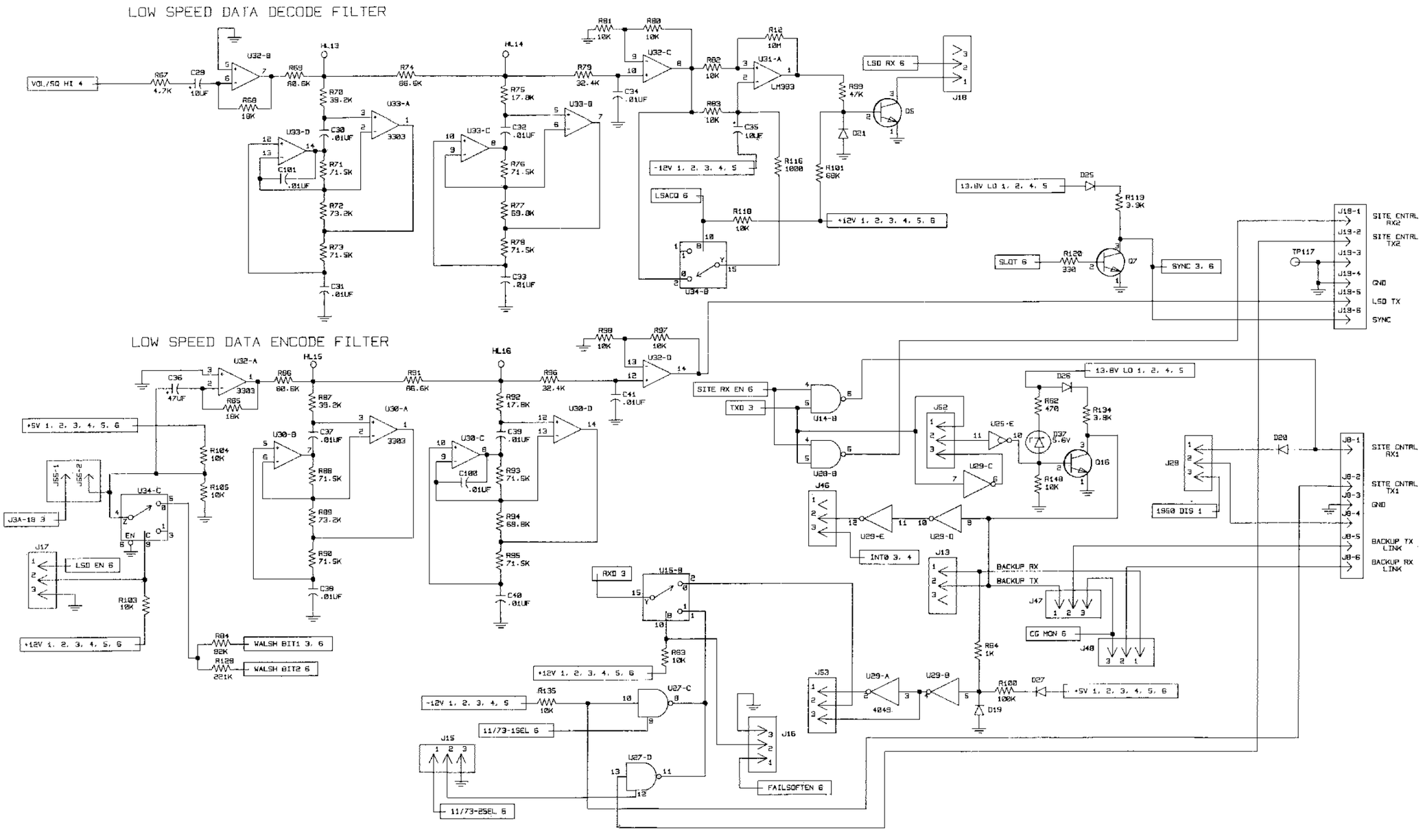
GETC SHELF19D901868G3

(19D902106, Sh. 3, Rev. 2)



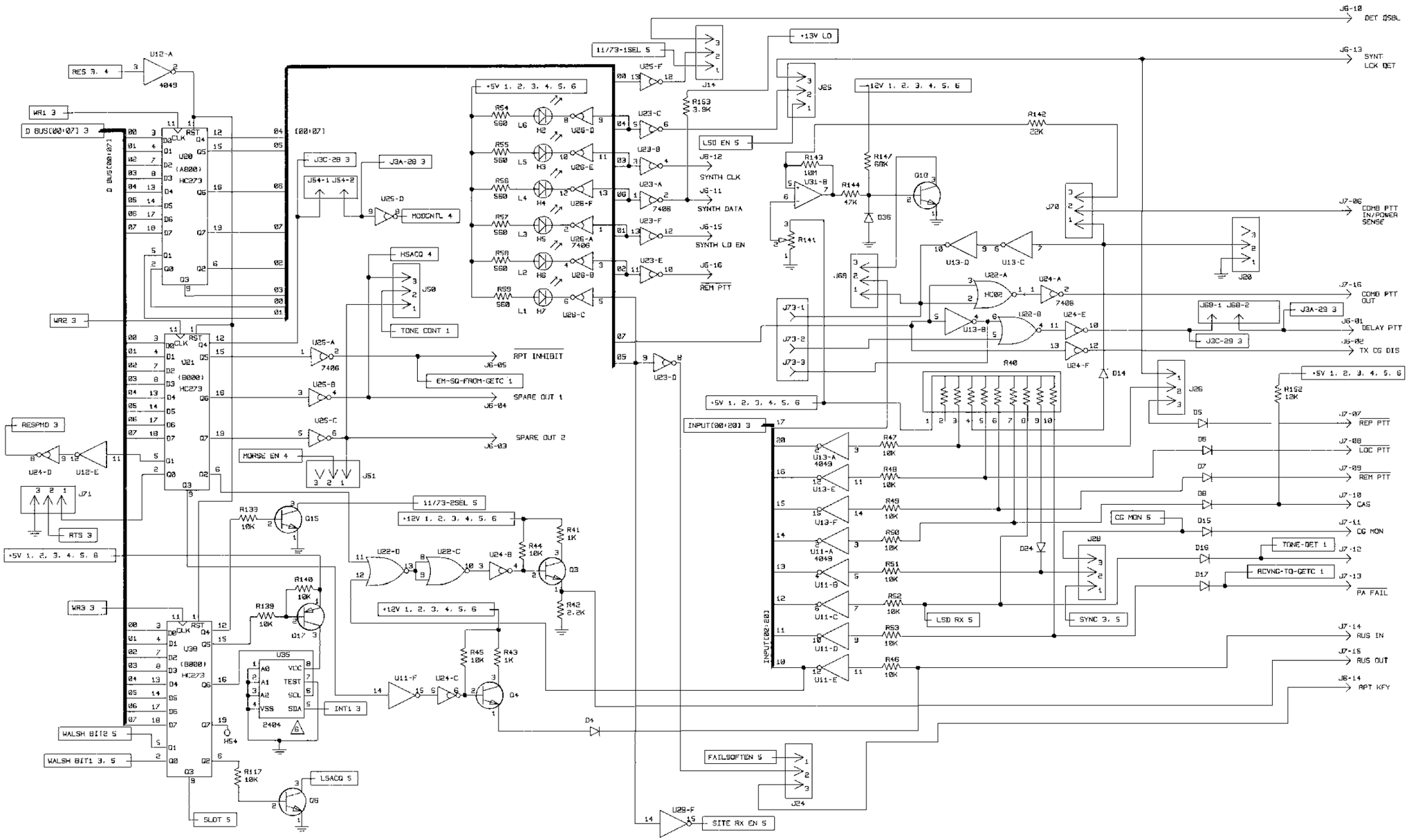
GETC SHELF 19D901868G3

(19D902106, Sh. 4, Rev. 5)



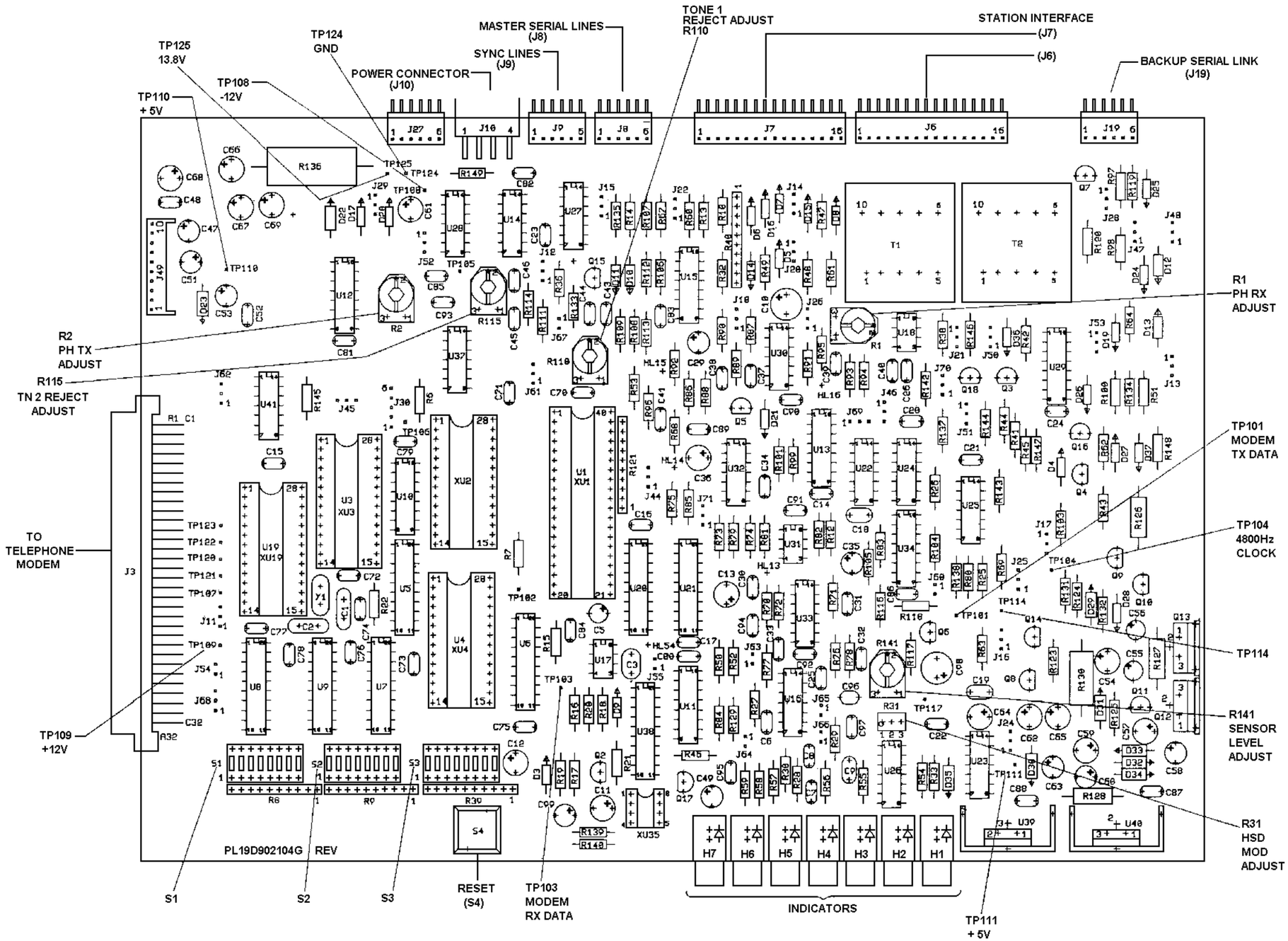
GETC SHELF 19D901868G3

(19D902106, Sh. 5,Rev. 3)



GETC SHELF 19D901868G3

(19D902106, Sh. 6, Rev. 2)


TONE 1
REJECT ADJUST
R110
STATION INTERFACE
(J7)
(J6)
MASTER SERIAL LINES
(J8)
SYNC LINES
(J9)
POWER CONNECTOR
(J10)
BACKUP SERIAL LINK
(J19)
TP125
13.8V
TP124
GND
TP108
-12V
TP110
+ 5V
R1
PH RX
ADJUST
R2
PH TX
ADJUST
R115
TN 2 REJECT
ADJUST
TP101
MODEM
TX DATA
TP104
4800Hz
CLOCK
TP114
R141
SENSOR
LEVEL
ADJUST
R31
HSD
MOD
ADJUST
TO
TELEPHONE
MODEM
TP109
+12V
S1
S2
S3
RESET
(S4)
TP103
MODEM
RX DATA
INDICATORS
TP111
+ 5V
PL19D902104G REV

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