MAINTENANCE MANUAL FOR MICROCOMPUTER BOARD 19D902571G1, S-825 19D902571G3, S-825 16PLUS

TABLE OF CONTENTS

SPECIFICATIONS*

Input Power		
A +	(J6-23)	13.8 VDC ±20%
SW A +	(J6-24)	13.8 VDC ±20%
+5V	(J6-25)	5.0 VDC ±5%
Maximum Current Drain		
A +		
RELAY-CTRL HIGH		10 Milliamperes
RELAY-CTRL LOW		5 Milliamperes
SW A +		300 Milliamperes
+5V		250 Milliamperes
Temperature Range		-30°C to +70°C (-22°F to +158°F)
Logic Levels		
High (1)		4.0 ±1.0 VDC
Low (0)		0.5 ±0.5 VDC
Rise Time		100 Nanoseconds
Fall Time		100 Nanoseconds
EL Driver Output (13.8 VDC SW A +)		
Voltage		125 Volts RMS
Frequency		700 Hz
Current		15 Milliamperes RMS
Power Relay Control		
High Level		9 Volts Minimum
Low Level		2 Volts Maximum
Light Level Detect		
Upper Hysteresis (Maximum)		2.6 VDC
Lower Hysteresis (Minimum)		2.4 VDC
Watchdog Timer Reset		
Pulse Width		250 ±50 Milliseconds
Continuous Duty Cycle		500 ±50 Milliseconds
Minimum Reset Pulse Input		10 Milliseconds

DESCRIPTION

Microcomputer Board 19D902571 provides the intelligent interface to the Display Board and the I/O Board. The microcomputer board also provides the intelligence necessary to interface with the mobile radio, siren/light/PA unit, the vehicular repeater unit, dual control head, and Voice Guard unit.

The Microcomputer board contains an 8032 microcontroller with external program memory in an EPROM. The Microcomputer also contains an EEPROM that contains the control unit (radio system) personality along with the user control settings.

Power up/down control of the control unit and the rest of the radio system is performed by a flip-flop. This flip-flop switches the A + power to the rest of the radio system through a relay.

AC power for the electroluminescent panel is generated by the EL driver device. This power is duty-cycled modulated to provide the intensity control of the EL backlighting.

The fast squelch detector is comprised of an analog filter/limiter circuit. The fast squelch detector provides a quick indication of carrier activity on a receive radio channel.

Ambient light level from the phototransistor on the Display Boards is limited by a comparator. This is used to automatically turn on the EL backlighting and reduce the LED brightness.

An optional limited channel guard signal from the radio is re-limited by a comparator. The microcomputer board performs the channel guard (tone or digital) decoding in the radio system.

A holding register is used to buffer data to the Display Boards. This provides isolation and drive of the signals to the Display Boards.

A second holding register is used to buffer data to the I/O Board. This provides isolation and drive of the signals to the I/O board.

A multiplexer is used to generate a gated write pulse to the holding registers on the microcomputer board and other registers on the I/O Board.

The watchdog timer is included to provide a control unit reset pulse. The watchdog timer is used to monitor the microcomputer software execution.

CIRCUIT ANALYSIS

The microcomputer board represents the heart of the control unit. It contains the microcomputer, firmware, and personality data required to operate the unit. Display data is output to the display board and keyboard inputs are received through J1. Interface to the I/O board is through a 26-pin ribbon cable (connector J6).

Figure 1 shows a block diagram of the digital input/output devices. The data bus (U1-32 thorough U1-39) acts as a parallel port when writing to U5 and U6. U7 is an audio mux that is used to provide the memory mapping of U5, U6 and addition I/O on the I/O board.

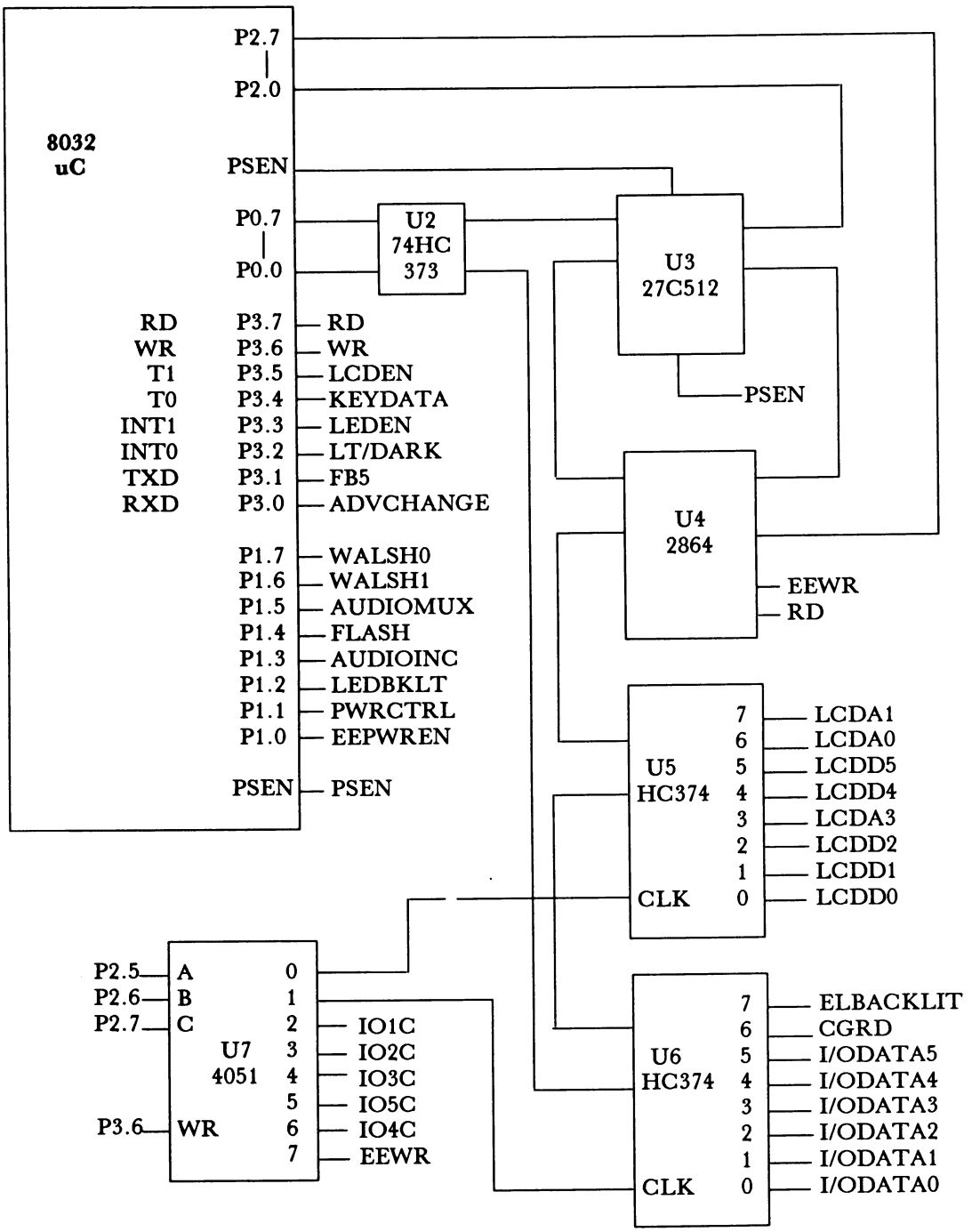

Figure 1 - Digital Block Diagram

POWER RELAY CONTROL CIRCUIT

The power control for the control unit is performed by flip-flop U8A and associated circuitry. The power control flip-flop turns on and off the power relay on the I/O board which supplies the switched battery power (SW A +) from the raw continuous battery power (A +).

The output control signal to route A + to SW A + on the I/O board is RELAY-CTRL (J6-12). When RELAY-CTRL is high, the relay on the I/O board is turned on (closed) and supplies power to SW A + . When RELAY-CTRL is low, the relay on the I/O is turned off (opened) and no power is supplied on SW A + .

The relay control flip-flop is powered from the continuous battery power (A +). This ensures that starting from a powered down condition, the control unit can be powered up through the front panel (keypad board).

When the control unit is initially powered down (SW A + , + 5V, and RELAY-CTRL are at zero volts but continuous battery power is running on A +), then the board is turned on by grounding the PWRSW (J1-3). This turns off transistor Q3. The collector of Q3 is pulled up to A + causing a rising edge to the clock input of flip-flop U8 and changing the state of RELAYCTRL from a low to a high. The change in state in the output of the flip-flop to a high level causes the relay on the I/O board to be closed which subsequently supplies to the + 5 volt regulator and hence powering up the entire control unit.

When the control unit is initially powered up (SW A + and + 5V specified power levels present), any further presses on the PWR button is sampled by the microcomputer which is the only functional entity that can turn the power to the control unit off. This is accomplished by + 5V power now being present which turns on transistor Q3 through resistor R38 irrespective of the sense of the PWR button (PWRSW). At this point, the only way that Q3 can be turned off in order to generate a rising edge on the clock input to U8, is if the microcomputer grounds the direct output line, PWRCTRL (U1-2).

Since RESET (J6-26) is high during normal microcomputer operation, transistor Q2 can only be turned on if PWRCTRL is low. When PWRCTRL is low (and RESET high) the collector of Q2 (which is tied to the base of Q3) is pulled low. This action turns off Q3, which generates a rising edge on the clock input of U8 and thereby changes the state of the flip-flop output from a high to a low. This will open the relay on the I/O board and remove the SW A + power (and subsequently the + 5V power).

The input of RESET to the base of transistor Q2 is needed to prevent possible chatter in the power up and power down of the control unit due to microcomputer and other hardware lines toggling until power becomes stable. The RESET signal goes low during power up and power down conditions (below 4.75 volts on the + 5V power or below 6.5 volts on the SW A + power) and thereby disables transistor Q2 from chattering and erroneously changing the state of the relay control flip-flop.

Resistor R35 and capacitor C33 provide a hysteresis feedback to the input of the flip-flop. This hysteresis provides debounce on the PWR button (PWSW) in order to prevent chatter on the power up and power down due to mechanical switch bounce.

Resistor R31, diode D1, and capacitor C31 provide filtering on the A + power to the relay control flip-flop. This filtering prevents the ignition noise and spurious battery supply voltage drops from changing the state of the relay control flip-flop.

Capacitor C32 and resistor R34 provide additional protection on ignition noise and spurious battery supply voltage drops by forcing the relay control flip-flop to default to the power on state (RELAYCTRL high). This is necessary to prevent a sizable ignition battery power drop from erroneously powering down the control unit.

With A + power instantaneously applied to the control unit, the relay control flip-flop will set RELAY-CTRL high, thereby turning the power on to the microcomputer. The microcomputer will quickly monitor the sense of the PWR button and the saved value in the EEPROM to ascertain whether the control unit is to remain on. If it determines that the radio system needs to be turned off, the microcomputer will ground PWRCTRL which will subsequently turn off the control unit and radio.

MICROCOMPUTER, LATCH, EPROM, AND EEPROM CIRCUITS

The intelligence of the control unit is contained in the microcomputer, U1. The microcomputer is an 8032 - 8 bit controller. This part is a high performance NMOS-processed part, utilizing two internal timers and a serial interface on a two level priority interrupt structure. The internal CPU handles the boolean processing, internal bit and byte RAM addressing, instruction fetching and execution, and interface to the external world by means of 16 dedicated I/O lines along with an 8 bit bussed memory-mapped I/O.

Microcomputer U1 operates at an internal clock instruction cycle time of 11.0592 MHz (nominal). The clock frequency is determined by the quartz crystal, Y1, which provides a fundamental mode of operation, and capacitors, C51 and C52, which provide start up time and frequency stability over the specified temperature range.

The microcomputer accesses program memory information from the EPROM, U3. The EPROM is a 32K by 8 bit or 64K by 8 bit ultra-violet erasable programmable read-only-memory device. This device contains both the operational instruction code for the CONTROL UNIT normal mode of operation as well as the test code necessary to implement the test and control functions described herein.

Each access to the EPROM for program memory information is preceded by an address setup to the EPROM. The high order 8 bits of the address are held stable on lines A8 through A15. Lines A8 through A14 are routed to the EPROM, U3, high order address inputs. The low order 8 bits of the address latched and held stable by the address holding latch, U2. The low order address lines are latch on a high to low going pulse on the ALE line. After the address is held stable, the microcomputer issues a low going pulse on PSEN to read the 8 bit program memory information contained in the EPROM at the specified address.

Settings for the radio personality and control unit are contained in the EEPROM, U4. The EEPROM is an 8K by 8 bit electrically erasable programmable read-only-memory. This device provides nonvolatile storage of radio personality and user controlled settings. Each access to the EEPROM for personality information is preceded by an address setup to the EEPROM.

The high order 8 bits of the address are held stable on lines A8 through A15. Lines A8 through A10 are routed to the EEPROM, U4, high order address inputs. The low order 8 bits of the address latched and held stable by the address holding latch, U2. The low order address lines are latch on a high to low going pulse on the ALE line. After the address is held stable, the microcomputer issues a low going pulse on RD (to read) or WR (to write) the 8 bit personality information from or to EPROM at the specified address.

Devices Q16, Q17 and associated circuitry provide the gated write pulse to the eeprom, WRGATE (U4-27). The gated write pulse is generated from the microcomputer on the signal line, WR (U1-16). As long as the microcomputer board is not in the process of being reset, the signal, RESET, will be at a logic high level (5 volts). Therefore, the collector of Q16 will rise to 2.5 volts allowing Q17 to be turned on if the emitter is brought to a logic low. This would allow the collector of Q17 to go low thereby sending the active low gated write pulse to the eeprom.

Transistors Q22, Q4, and associated circuitry allow the write pulse from the microcomputer (WR) to be passed to the collector of Q17 through the analog switch, U7. The inhibit control to the analog switch is generated from the microcomputer address lines, A9 through A12. When any of these address lines are high, transistor Q22 is on, thereby turning transistor Q4 off. This generates a high to the INH control of U7 and disables the WR pulse from being passed to WRGATE. In the control unit, the eeprom can be written only in the first 512 byte locations (addresses E000 - E1FF HEX).

In order to write in the remaining locations, a PC programmer cable must be installed whereby the control line EEWREN (J6-14) is grounded, thereby allowing writing to all EEPROM locations. When EEWREN is low, Q22 is turned off at all times, thereby turning Q4 on and pulling the inhibit control to U7 low.

Holding register, U5, interfaces with the keypad boards to read keypad closure information, activate LED's, and update the LCD display. U5 is accessed via a memory-mapped write to address location, 0000 hex.

Holding register U6 interfaces with the I/O board to read radio status and input information, to write radio control information, and to route audio paths between the radio and the control unit. U6 is accessed via a memory-mapped write to address location, 2000 hex.

KEYBOARD INTERFACE CIRCUITS

In addition to U5, there are five lines on the microcomputer that interface with the keypad boards. They are LEDBKLT (U1-3), FLASH (U1-5), LEDEN (U1-13), LCDEN (U1-15), and KEYBDDATA (U1-14).

The holding register, U5, latches the data lines to the keypad board. This eight bit data is used to turn on and off LED's, set up characters to be written to the LCD display, and clock out the sampled keypad closure information to the microcomputer.

WATCHDOG TIMER CIRCUIT

The watchdog timer is used to monitor the operation of the microcomputer software. It generates a reset pulse in the unlikely condition that the microcomputer goes awry and does not execute the program memory software properly.

In the absence of any service to the watchdog timer via I/O-DATA-0 (U6-2), the comparator U10C will oscillate with about a 50 percent duty cycle. The rate of oscillation is determined by R45, R46, and C34. Resistor R46 provides the hysteresis control to the comparator. The negative input of the comparator U10C is generated from the RC time constant consisting of R45 and C34. The positive input of the comparator U10C is a nominal 2.5 volts as set up by resistors R47 and R48 with resistor R46 setting up the hysteresis range.

The following describes the circuit behavior in the steady state mode of operation. When the negative input of the comparator is initially less than the positive input, the output of the comparator (U10C-14) will be at +5 volts, which is supplied through the pull up resistor R52 (U10C provides an open collector output).

Capacitor C34 charges through resistor R45 until the voltage on the capacitor (or negative input of U10C) reaches the value of the level set up on the positive input of U10C. At this point, the comparator will flip and the output (U10C-14) will go to ground. Resistor R46 provides the hysteresis and will drag the positive input slightly below the nominal setup level of 2.5 volts on the positive input of the comparator.

Capacitor C34 will now discharge through resistor R45 until the voltage on the capacitor (or negative input of U10C) reaches the value of the level set up on the positive input of U10C. At this point, the comparator will flip and the output (U10C-14) will go to +5 volts. Resistor R46 provides the hysteresis and will drag the positive input of the comparator slightly above the nominal setup level of 2.5 volts on the positive input of the comparator. The cycle will continue to repeat in the absence of any watchdog service from the microcomputer.

The microcomputer services the watchdog timer on the negative edge of I/O-DATA-0. On each falling edge of I/O-DATA-0, transistor Q5 is turned on for a short period of time. The short turn on time is accomplished when the base current of Q5 is pulsed out through R41 and C11 on the falling edge of I/O-DATA-0.

This short burst of base current turns on the pass transistor Q5 which passes the +5 volts over to transistor Q6 and associated circuitry. Transistor Q6 turns on for a short period of time and discharges the capacitor C34 to ground. This puts this negative input of the comparator at ground thereby forcing the output of the comparator (U10C-14) to +5 volts.

When the watchdog timer is serviced by the microcomputer, the output of the comparator is at a continuous +5 volts.

Note that when the microcomputer services the watchdog timer, the charge on capacitor C34 is brought to ground. This provides a longer time to flip the state of the comparator than that which exits for a steady state mode of oscillation. The microcomputer has to service the watchdog timer periodically (before the comparator has time to change state and reset the microcomputer).

Resistors R42 and R44 set up the steady state DC voltage to the base and prevents noise current from turning on the appropriate transistor. Diode D2 provides a DC path for the current produced on the rising edge of I/O-DATA-0 and protects the base of transistor Q5.

The output of the comparator U10C is coupled to the base of Q2 and Q7 as well as to the I/O board.

LIGHT/DARK SENSOR CIRCUIT

The outside ambient light level is detected by the microcomputer via the LT/DARK (U1-12) signal derived from the light level detect circuitry consisting of comparator, U10A, and associated circuitry.

LT/SENSOR is an analog signal (0 to 5 volts) inputted to the negative input of U10A. As the ambient light level increases in intensity, the LT/SENSOR signal increases in level. Resistor R61 provides a load for the analog level derived from the emitter of the phototransistor on the keypad board. Capacitor C21 provides light level filtering. The load value of R61 was chosen to obtain a nominal ambient light threshold detect at approximately 4 to 5 milliwatts/(cm*cm).

The positive input of U10A is set up with a nominal DC bias level of 2.5 volts. The bias level fixes the nominal threshold point.

Resistor R62 provides a small level of hysteresis for the detection of the ambient light level. This is used to prevent the comparator from oscillating at light levels near the nominal threshold detect setting. The value of R62 was chosen to provide a hysteresis range from 4 to 5 milliwatts/(cm*cm).

As the light level increases from a dark condition to a strong light level (0 towards 5 volts), LT/DARK will start at +5 volts (due to the internal pull up on the microcomputer) and will flip to 0 volts as the LT/SENSOR signal passes the 2.5 volt reference. As the light level decreases from a strong light to a dark condition (5 volts toward 0 volts), LT/DARK will start at 0 volts and will flip to +5 volts when the LT/SENSOR signal passes the 2.5 volt reference.

CHANNEL GUARD LIMITER CIRCUIT

The microcomputer detects the channel guard information on the receiver radio frequency channel. The limited channel guard signal is derived from the radio and is again limited by U10B and buffered by Q9. The microcomputer samples the channel guard signal through AUDIOMUX (U1-6) and is controlled by Q8.

Bias on U10B is set at a nominal 2.5 volts for detecting the channel guard signal from the radio. U10B serves to buffer and re-threshold the signal received from the radio over the long cable.

FAST SQUELCH DETECTOR CIRCUIT

The fast squelch detect circuit on the microcomputer board is used to provide a quick detection of carrier activity on a receiver radio frequency channel. This quick detection is used in SCAN operation to lock onto a high priority incoming call. The basis used in the detection of carrier activity is noise squelch.

The fast squelch circuit consists of a three-pole high pass filter, an averaging detector, a DC amplifier, and a Schmitt trigger. The fast squelch circuit is used to provide a fast indication of carrier activity on a channel by monitoring the channel received noise component in the 6000 to 8000 Hz range.

A high pass filter, consisting of C61, C62, R81, R82, and U9C, removes all voice signals (0 to 3000 Hz) from the incoming received signal on FASTSQ (J6-17). The output signal out of the high pass filter (which consists of noise outside of the voice audio band in the range from 6000 to 8000 Hz) is sent to the averaging detector stage.

Noise in the 6000 to 8000 Hz band is applied to the averaging detector which consists of R83, R84, R85, R86, R87, C63, C71, C64, and U9D. The noise is rectified to provide an average DC output level proportional to the noise input. A larger noise level provides a larger DC output level.

The average DC level is amplified by C72, R88, R89, and U9A to produce a level ranging from 0 to 5 volt DC. This amplifier buffers the amplified DC level to the input of the Schmitt trigger.

The Schmitt trigger consists of R90, R91, C73, and U9B. The inverting input of U9B is referenced to BIAS (2.5 volt DC). When the DC level exceeds 2.5 volts, the Schmitt trigger, U9B, switches and provides a positive voltage to transistor Q11 (if enabled by transistor Q10). For a large noise component in the 6000 to 8000 Hz range, U9B-7 saturates at the high level. The output of Q11 is read by the microcomputer on AUDIOMUX (U1-6) when selected (during audio mux read multiplexing).

HORNRING CIRCUIT

The hornring circuit allows the software to look for either a positive (A+) active or negative (A-) active signal. PC programming denotes which polarity is the active state. Note that the audio mux line at the connector (J6-16) must be floating, I/ODATA4 = 0, I/ODATA5 = 1, and CGRD = 1 in order to read the input.

The following describes the proper setup to read the HORNRING input correctly.

Positive active (AUDIOMUX = 1 as input):

HORNRING	P1.6	P1.7	AUDIOMUX
A	0	1	0
float	0	1	1

Negative active (P1.7 = 1 as input):

A-	1	0	na
float	1	1	na

ELECTROLUMINESCENT (EL) PANEL DRIVER CIRCUIT

The electroluminescent (EL) panel driver is a voltage converter that transforms the SW A+ input to a 125 RMS volt AC signal.

CAUTION

This transformer must be terminated in an equivalent circuit in order not to cause damage. The equivalent circuit is a 3.0 K ohm resistor in parallel with a 0.068 μf capacitor.

The intensity of the EL panel backlighting is changed by varying the duty cycle of ELBACKLT (U6-19). The duty cycle varies from 100 percent (fully on) to 0 percent (fully off) with a cycle time of about 20 milliseconds.

When ELBACKLT is high, transistor Q12 is turn on, thereby turning on the pass transistor Q13 which supplies SW A+ power to the EL driver U12. The EL driver accepts the SW A+ input power and generates the nominal AC power required for the EL panel on the keypad board. The negative side of the output AC power is grounded on the keypad board. The EL driver U12 generates the AC power at a specified frequency.

Compensation is provided in the EL driver for degradations over time in the capacitive load of the EL panel. Resistor R114 and capacitor C36 provides input filtering to the EL driver.

MEMORY MAPPING USING MUX U7

The upper three address lines A13, A14, and A15 (U1-26 thorough U1-28) are used as address inputs (U7-11 thorough U7-9) for U7. The inhibit line (U7-6) is decoded to prevent writing to the eeprom (U4) address above E1FF Hex. The OUT/IN (U7-3) signal is the microcomputer WR (U1-16) signal that is memory mapped to address the various I/O devices (U5, U6, and IO1C through IO5C).

Table 1 shows the control unit external device memory-mapping of the microcomputer.

WRITING TO PARALLEL OUTPUT REGISTER U5 & U6

Writing to U5 & U6 (74HC374 OCTAL D FLIP-FLOP) is accomplished by providing data on the address bus A0 through A7 (U1-39 through U1-32) and then activating the C signal (WR from U7). The truth table for U5 & U6 is as follows:

OPERATING MODE	INPUTS		OUTPUTS
	CP	Dn	Qn
LOAD "1"	^	1	1
LOAD "0"	^	0	0

^ = LOW TO HIGH CLOCK TRANSITION
Dn = LOGIC LEVEL PRIOR TO CLOCK TRANSITION

TEST PROCEDURES

A functional System Test Procedure for the microcomputer board consists of exercising the board using a standard "dumb" terminal and the test software called MONITOR. This test uses the MONITOR software that is part of the microprocessor on the microcomputer board to make power and continuity checks, check the display panel and keypad, and provide functional checks for the microprocessor and I/O boards.

Complete instructions for using the MONITOR test software are contained in Combination Maintenance Manual (LBI-38445 for the S-825 16^{PLUS}, or LBI-38244 for the S-825 only).

An additional test procedure is available (where applicable) that uses the S-800 Automatic Tester. For complete information on this procedure, refer to the S-800 Automatic Tester Maintenance Manual, LBI-38166.

MEMORY ADDRESS (HEX)	PSEN	RD	WR	DEVICE ACCESSED
0000 - 7FFF	0	1	1	EPROM, U3
E000 - FFFF	1	0	1	EEPROM, U4
E000 - E1FF	1	1	0	EEPROM, U4
0000	1	1	0	REGISTER, U5
2000	1	1	0	REGISTER, U6
4000	1	1	0	I/O BD, IO1C
6000	1	1	0	I/O BD, IO2C
8000	1	1	0	I/O BD, IO3C
C000	1	1	0	I/O BD, IO4C
A000	1	1	0	I/O BD, IO5C

Table 1 - Microcomputer Memory Mapping

ERICSSON

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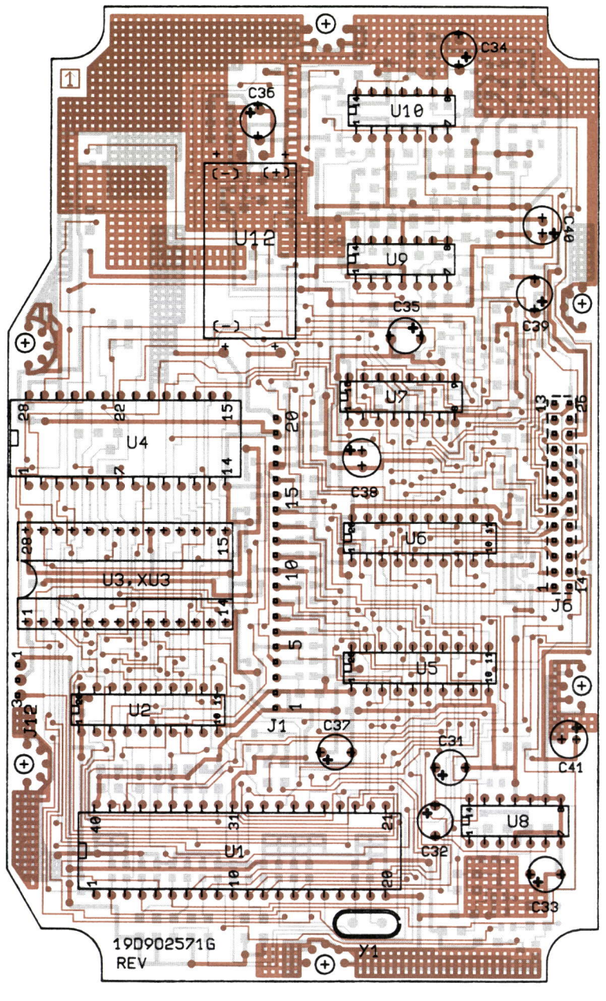
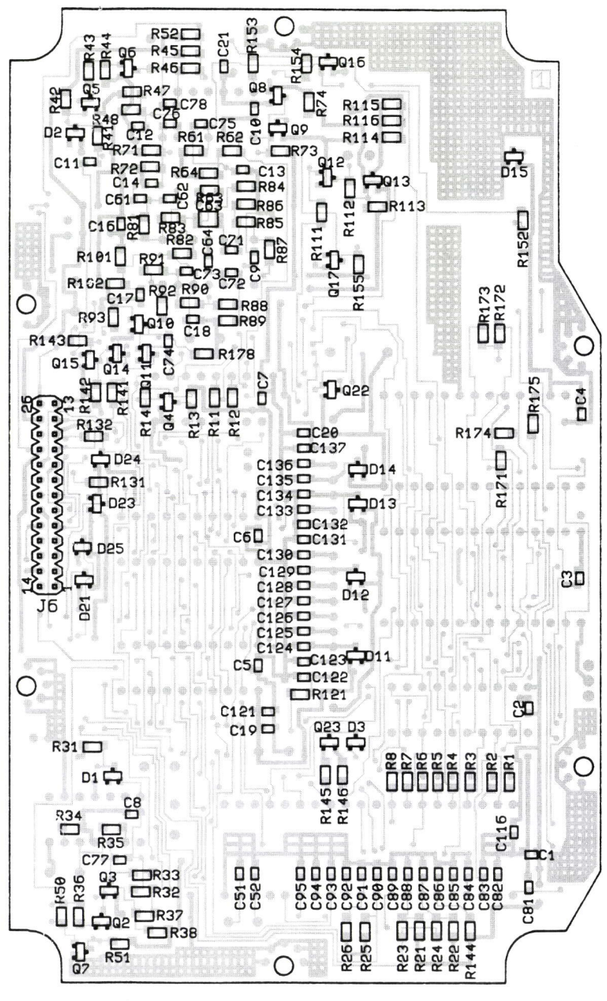
COMPONENT SIDE



(19D902571, Rev. 1)
(19D902570, Rev. 1 Component Side)
(19D902570, Rev. 1, Solder Side)

SOLDER SIDE



(19D902571 Rev. 1)
(19D902570, Rev. 1, Solder Side)

MICROCOMPUTER BOARD
19D902571G1, G3

CAUTION

OBSERVE PRECAUTIONS FOR HANDLING

ELECTROSTATIC SENSITIVE DEVICES

THE FOLLOWING ITEMS ARE MOS DEVICES REQUIRING SPECIAL CARE:
U1, U2, U5, U6, U7, U8

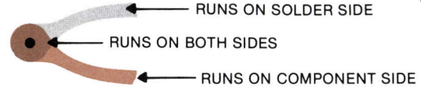
JUMPER CONNECTIONS		DESCRIPTION
PLUG	JUMPER	
P12	J12-2&3	OPTIONAL U3 27C512 EPROM
P12	J12-1&2	STANDARD U3 27C256 EPROM

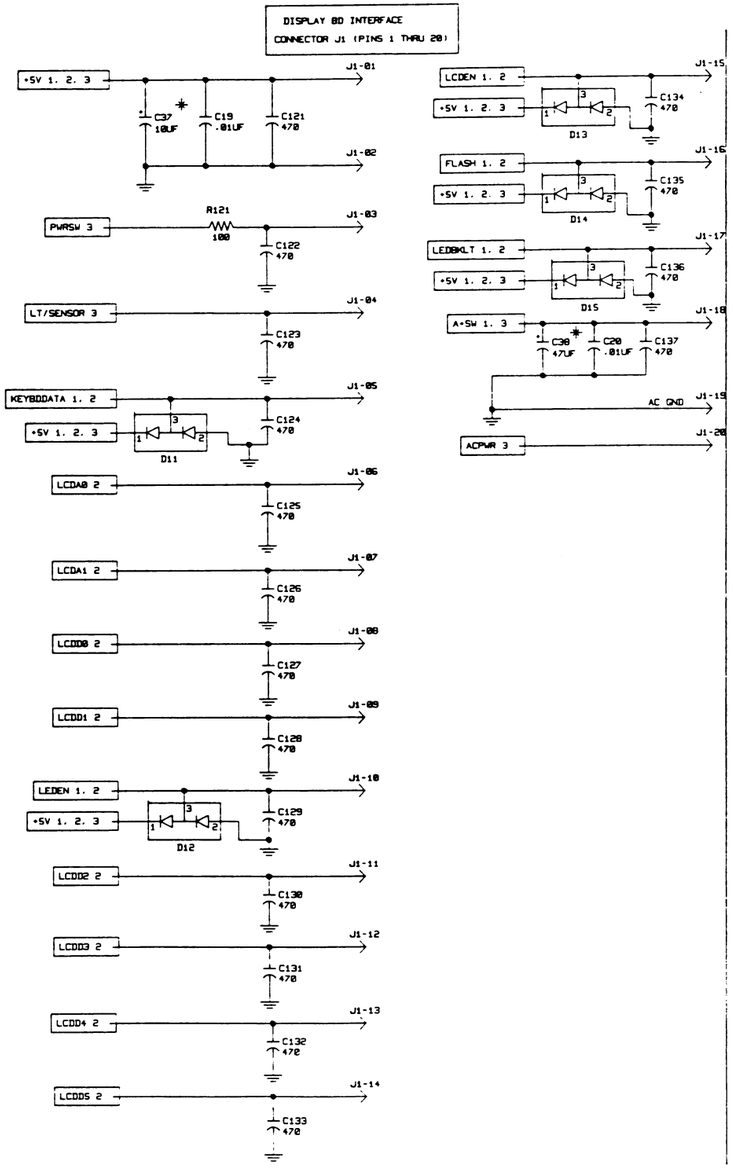
LEAD IDENTIFICATION FOR
D1,D2,D3,D11 THRU D15,D21 THRU D25

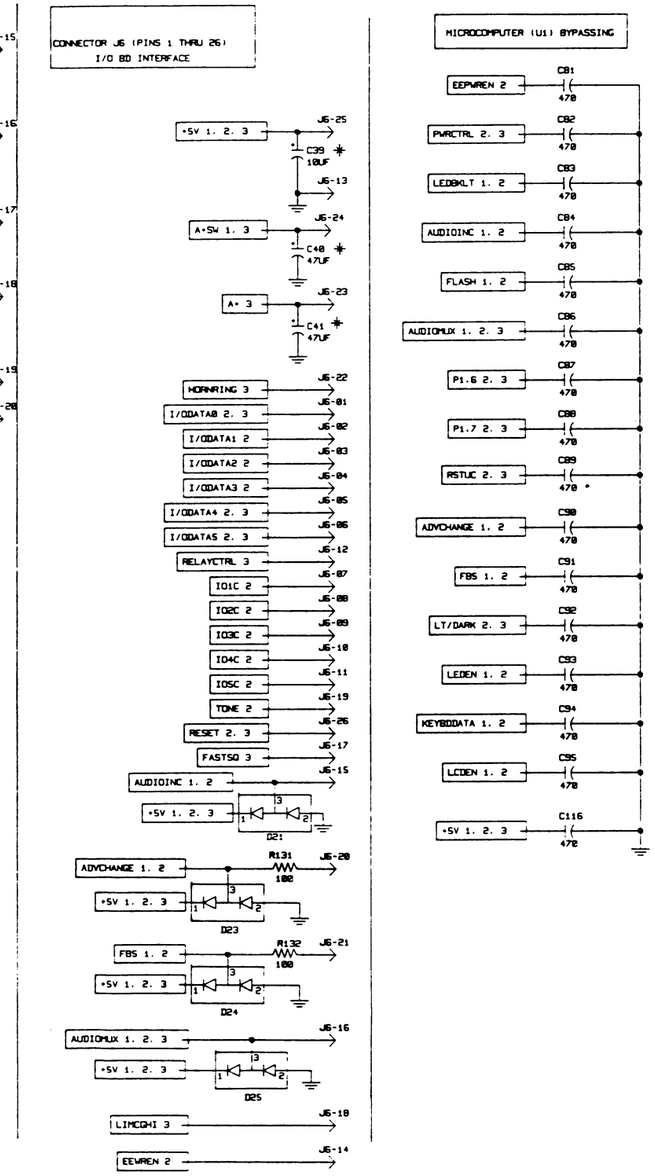
VIEW FROM SOLDER SIDE

LEAD IDENTIFICATION FOR
Q1 THRU Q23

VIEW FROM SOLDER SIDE







ALL RESISTORS ARE 1/8 WATT UNLESS OTHERWISE SPECIFIED AND RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY K=1000 OHMS OR MEG=1,000,000 OHMS. CAPACITOR VALUES IN PICOFARADS (EQUAL TO MICROMICROFARADS) UNLESS FOLLOWED BY UF=MICROFARADS. INDUCTANCE VALUES IN MICROHENRYS UNLESS FOLLOWED BY MH=MILLIHENRYS OR H=HENRYS.

ALL DIODES, CAPACITORS, RESISTORS AND TRANSISTORS ARE CHIP COMPONENTS ON SOLDER SIDE OF BOARD UNLESS FOLLOWED BY *

TABLE 1

POWER AND GROUND CONNECTIONS

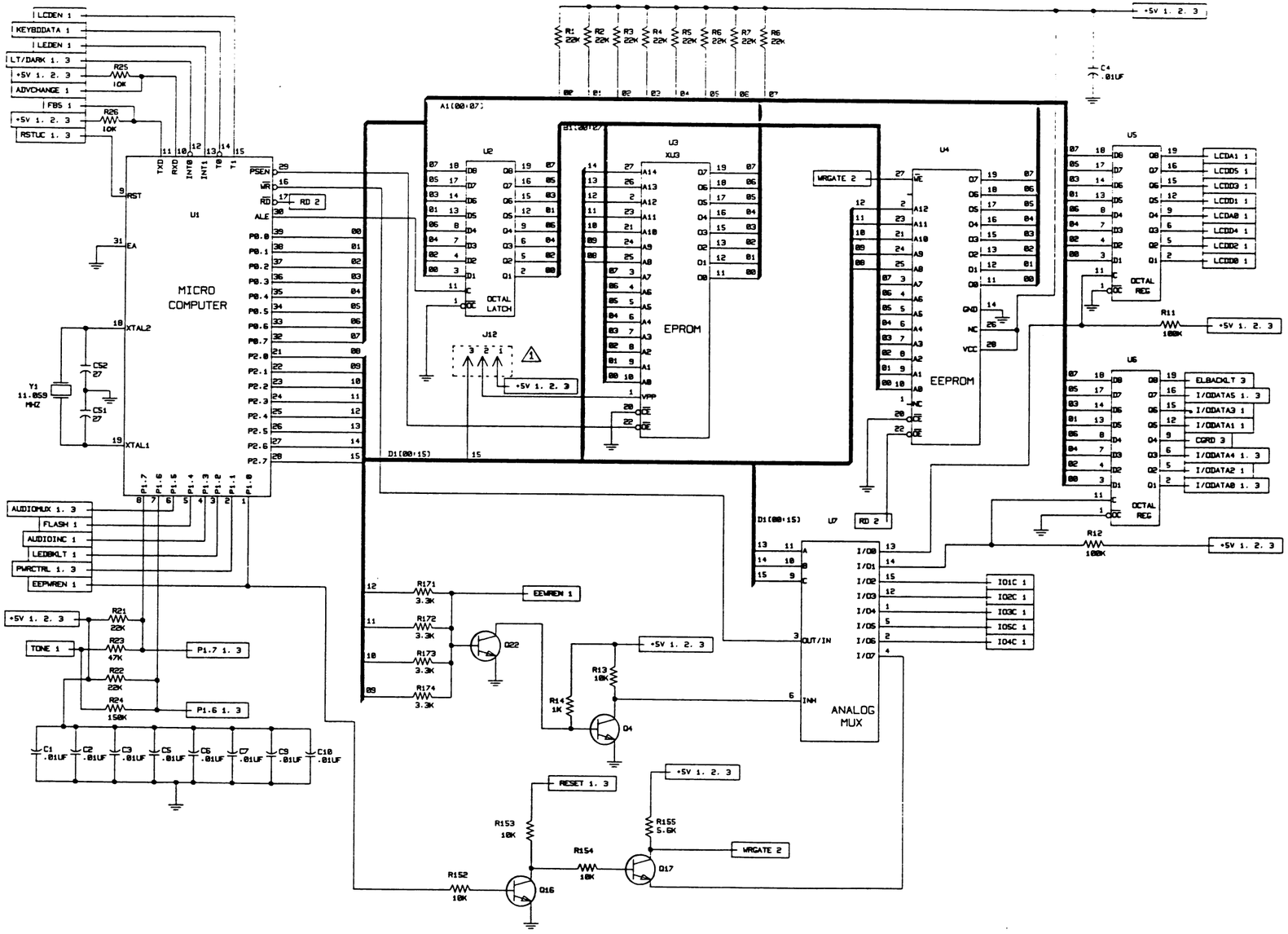
DEVICE	+5V PIN	GND PIN
U1	40	20
U2	20	10
U3	28	14
U5	20	10
U6	20	10
U7	16	7,8
U8		4,7,8,9,10,11
U9	4	11
U10	3	12

⚠1 JUMPER PLUG SETTINGS

PLUG	CONNECTION	DESCRIPTION
P12	J12-2&3	OPTION 64K EPROM
P12	J12-1&2	STANDARD 32K EPROM

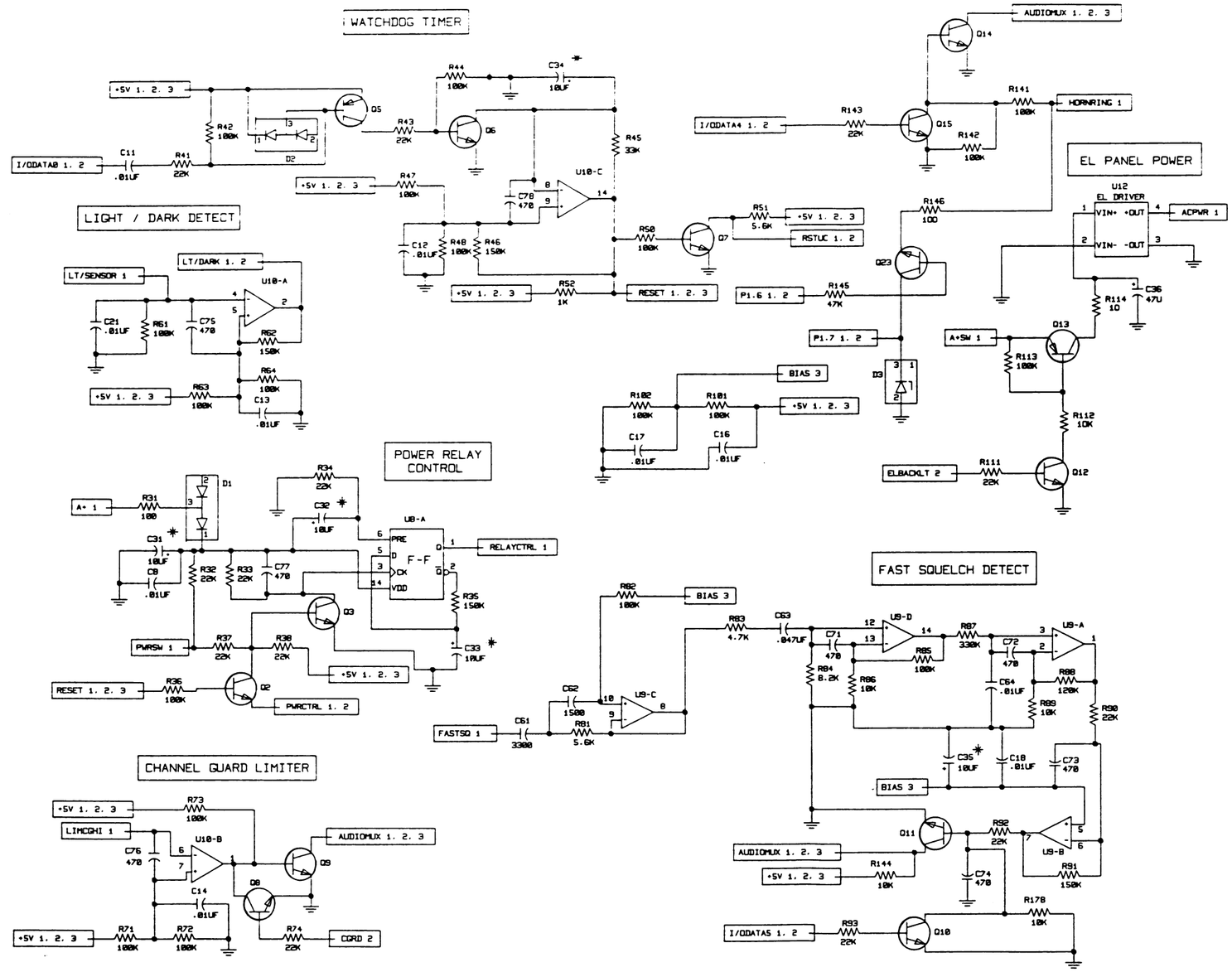
(19D902574, Sh. 1, Rev. 0)

MICROCOMPUTER BOARD
19D902571G1, G3
Sheet 1



MICROCOMPUTER BOARD
19D902571G1, G3
Sheet 2

(19D902574, Sh. 2, Rev. 0)



(19D902574, Sh. 3, Rev. 0)

MICROCOMPUTER BOARD
19D902571G1, G3
Sheet 3

PARTS LIST

MICROCOMPUTER BOARD
19D902571G1,3
ISSUE 1

SYMBOL	GE PART NO.	DESCRIPTION
		- - - - - - - - - - CAPACITORS - - - - - - - - - -
C1 thru C14	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C16 thru C21	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C31 thru C35	19A701534P7	Tantalum: 10 uF + or -20%, 16 VDCW.
C36	19A703314P4	Electrolytic: 47 uF -10+50% tol, 16 VDCW; sim to Panasonic LS Series.
C37	19A701534P7	Tantalum: 10 uF + or -20%, 16 VDCW.
C38	19A704879P2	Electrolytic: 47 uF + or -20%, 16 VDCW.
C39	19A701534P7	Tantalum: 10 uF + or -20%, 16 VDCW.
C40 and C41	19A704879P2	Electrolytic: 47 uF + or -20%, 16 VDCW.
C51 and C52	19A702061P33	Ceramic: 27 pF + or -5%, 50 VDCW, temp coef 0 + or -30 PPM/°C.
C61	19A702052P8	Ceramic: 3300 pF + or - 10%, 50 VDCW.
C62	19A702052P6	Ceramic: 1500 pF + or - 10%, 50 VDCW.
C63	19A702052P22	Ceramic: 0.047 uF + or - 10%, 50 VDCW.
C64	19A702052P14	Ceramic: 0.01 uF + or - 10%, 50 VDCW.
C71 thru C78	19A702052P3	Ceramic: 470 pF + or - 10%, 50 VDCW.
C81 thru C95	19A702052P3	Ceramic: 470 pF + or - 10%, 50 VDCW.
C116	19A702052P3	Ceramic: 470 pF + or - 10%, 50 VDCW.
C121 thru C137	19A702052P3	Ceramic: 470 pF + or - 10%, 50 VDCW.
		- - - - - - - - - - DIODES - - - - - - - - - -
D1 and D2	19A700053P2	Silicon, fast recovery (2 diodes in series).
D3	19A700083P1	Silicon.
D11 thru D15	19A700053P2	Silicon, fast recovery (2 diodes in series).
D21	19A700053P2	Silicon, fast recovery (2 diodes in series).
D23 thru D25	19A700053P2	Silicon, fast recovery (2 diodes in series).
		- - - - - - - - - - JACKS - - - - - - - - - -
J1	19A703248P15	Post: Gold Plated, 21 mm length.
J6	19A702333P54	Connector, printed wiring, two part: 26 pins rated at 1 amp; sim to Dupont 78207-110.
J12	19A703248P11	Post: Gold Plated, 10 mm length.
		- - - - - - - - - - PLUGS - - - - - - - - - -
P12	19A702104P2	Connector: 2 Position Shorting, Gold Plated; sim to Berg 65474-003.
		- - - - - - - - - - TRANSISTORS - - - - - - - - - -
Q2 and Q3	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q4	19A700236P4	Silicon, NPN.
Q5	19A700059P2	Silicon, PNP.
Q6 thru Q12	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q13	19A703197P2	Silicon, PNP; sim to MMBT4403 Low Profile Pkg.
Q14 and Q15	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
Q16 and Q17	19A700236P4	Silicon, NPN.
Q22	19A700236P4	Silicon, NPN.
Q23	19A700076P2	Silicon, NPN: sim to MMBT3904, low profile.
		- - - - - - - - - - RESISTORS - - - - - - - - - -
R1 thru R8	19B800607P223	Metal film: 22K ohms + or -5%, 1/8 w.
R11 and R12	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R13	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R14	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R21 and R22	19B800607P223	Metal film: 22K ohms + or -5%, 1/8 w.
R23	19B800607P473	Metal film: 47K ohms + or -5%, 1/8 w.
R24	19B800607P154	Metal film: 150K ohms + or - 5%, 1/8 w.
R25 and R26	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R31	19B800607P101	Metal film: 100 ohms + or -5%, 1/8 w.
R32 thru R34	19B800607P223	Metal film: 22K ohms + or -5%, 1/8 w.
R35	19B800607P154	Metal film: 150K ohms + or - 5%, 1/8 w.
R36	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R37 and R38	19B800607P223	Metal film: 22K ohms + or -5%, 1/8 w.
R41	19B800607P223	Metal film: 22K ohms + or -5%, 1/8 w.
R42	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R43	19B800607P223	Metal film: 22K ohms + or -5%, 1/8 w.
R44	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R45	19B800607P333	Metal film: 33K ohms + or -5%, 1/8 w.
R46	19B800607P154	Metal film: 150K ohms + or - 5%, 1/8 w.
R47 and R48	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R50	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R51	19B800607P562	Metal film: 5.6K ohms + or -5%, 1/8 w.
R52	19B800607P102	Metal film: 1K ohms + or -5%, 1/8 w.
R61	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R62	19B800607P154	Metal film: 150K ohms + or - 5%, 1/8 w.
R63 and R64	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R71 thru R73	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R74	19B800607P223	Metal film: 22K ohms + or -5%, 1/8 w.
R81	19B800607P562	Metal film: 5.6K ohms + or -5%, 1/8 w.
R82	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R83	19B800607P472	Metal film: 4.7K ohms + or -5%, 1/8 w.
R84	19B800607P822	Metal film: 8.2K ohms + or -5%, 1/8 w.
R85	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R86	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R87	19B800607P334	Metal film: 330K ohms + or - 5%, 200 VDCW, 1/8 w.
R88	19B800607P124	Metal film: 120K ohms + or -5%, 1/8 w.
R89	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R90	19B800607P223	Metal film: 22K ohms + or -5%, 1/8 w.
R91	19B800607P154	Metal film: 150K ohms + or - 5%, 1/8 w.
R92 and R93	19B800607P223	Metal film: 22K ohms + or -5%, 1/8 w.
R101 and R102	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R111	19B800607P223	Metal film: 22K ohms + or -5%, 1/8 w.
R112	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R113	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R114	19B800607P100	Metal film: 10 ohms + or -5%, 1/8 w.
R121	19B800607P101	Metal film: 100 ohms + or -5%, 1/8 w.
R131 and R132	19B800607P101	Metal film: 100 ohms + or -5%, 1/8 w.
R141 and R142	19B800607P104	Metal film: 100K ohms + or -5%, 1/8 w.
R143	19B800607P223	Metal film: 22K ohms + or -5%, 1/8 w.
R144	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R145	19B800607P473	Metal film: 47K ohms + or -5%, 1/8 w.
R146	19B800607P101	Metal film: 100 ohms + or -5%, 1/8 w.
R152 thru R154	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
R155	19B800607P562	Metal film: 5.6K ohms + or -5%, 1/8 w.
R171 thru R174	19B800607P332	Metal film: 3.3K ohms + or -5%, 1/8 w.
R178	19B800607P103	Metal film: 10K ohms + or -5%, 1/8 w.
		- - - - - - - - - - INTEGRATED CIRCUITS - - - - - - - - - -
U1	19A703714P1	Digital: HMOS 8-bit Microcomputer; sim to TP8032AM.
U2	19A703471P2	Digital: Octal Data Latch; sim to 74HC373.
U3	19A705710G7	EPROM Kit. (Used with S-825).
U3	19A149935G1	EPROM Kit. (Used with S-825 16 Plus).
U4	19A705466P1	EEPROM: 8K x 8; sim to 2864A-20.
U5 and U6	19A704380P12	Digital: CMOS Octal Tri-State Data Flip-Flop; sim to 74HC374.
U7	19A700029P36	Digital: SINGLE 8-CHANNEL MULTIPLEXER.
U8	19A700029P9	Digital: Dual Data Flip-Flop; sim to 4013B.
U9	19A704883P1	Linear: Quad Op Amp; sim to MC3303P.
U10	19A134764P1	Linear: Quad Voltage Comparator; sim to LM339N.
U11	19A700029P231	Digital: 8-INPUT NOR GATE. 4078B.
U12	19A149417P2	Driver.
		- - - - - - - - - - SOCKETS - - - - - - - - - -
XU3	19A700156P3	Integrated circuit: 28 contacts; sim to AMP 640362P3.
		- - - - - - - - - - CRYSTALS - - - - - - - - - -
Y1	19A702511G15	Quartz: 11.059200 MHz.

*COMPONENTS ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES