MAINTENANCE MANUAL
DIGITAL SELECTOR MODULE
19D902519G1
INCLUDING
DIGITAL SELECTOR 1 (150 BAUD DATA)
AND
DIGITAL SELECTOR 2 (9600 Hz CLOCK)

TABLE OF CONTENTS

SPECIFICATIONS

- Tables 1 through 4 depict the specifications of the Digital Selector Module used in the **EDACS™** Simulcast System.
- Table 1 outlines the general specifications.
- Table 2 outlines the power drain specifications.
- Table 3 outlines the P1 connector interface to the cross connect panel.
- Table 4 outlines the jumper definition and default configurations.
- Figures 2 through 4 depict the specifications as it relates to the actual operation as part of the **EDACS** Simulcast System.

Continued

SPECIFICATIONS

(Continued)

Table 1 - General Specifications

ITEM	SPECIFICATION
INPUT VOLTAGE	+5 VOLTS ± 10%
TEMPERATURE	0 TO +60 DEGREES C
DIMENSION	8.0 (L) BY 4.0 (W) IN
WEIGHT	10 OUNCES
DATA- INPUT/OUTPUT	VRS-232C
ALARM OUTPUT	TTL

Table 2 - Power Specification

VOLTAGE	CONNECTOR POINT	TOLERANCE ± %	CURRENT **DRAIN TYPICAL mA**	CURRENT **DRAIN MAXIMUM mA**	CURRENT **DRAIN STANDBY mA**
GND	P1-A2 P1-C2 P1-A31 P1-C31	NA	NA	NA NA NA NA	NA
+5	P1-A1 P1-C1 P1-A32 P1-C32	5	1200	2000 2000 2000 2000	NA

Continued

SPECIFICATIONS

(Continued)

Table 3 - Connector P1 Definition

CONNECTOR PIN	SIGNAL NAME	INPUT/ OUTPUT	LEVEL DIGITAL DC-VOLT AC-VRMS
P1-A1	+5	I/O	+5V
P1-C1	+5	I/O	+5V
P1-A2	GND	I/O	0V
P1-C2	GND	I/O	0V
P1-A3	IN1	I	RS-232C
P1-C3	IN2	I	RS-232C
P1-A4	IN3	I	RS-232C
P1-C4	IN4	I	RS-232C
P1-A5	IN5	I	RS-232C
P1-C5	IN6	I	RS-232C
P1-A6	IN7	I	RS-232C
P1-C6	IN8	I	RS-232C
P1-A7	IN9	I	RS-232C
P1-C7	IN10	I	RS-232C
P1-A8	IN11	I	RS-232C
P1-C8	IN12	I	RS-232C
P1-A9	IN13	I	RS-232C
P1-C9	IN14	I	RS-232C
P1-A10	IN15	I	RS-232C
P1-C10	IN16	I	RS-232C
P1-A11	IN17	I	RS-232C
P1-C11	IN18	I	RS-232C
P1-A12	IN19	I	RS-232C
P1-C12	IN20	I	RS-232C
P1-A13	IN21	I	RS-232C
P1-C13	IN22	I	RS-232C
P1-A14	IN23	I	RS-232C
P1-C14	IN24	I	RS-232C
P1-A15	IN25	I	RS-232C
P1-C15	IN26	I	RS-232C
P1-A16	IN27	I	RS-232C
P1-C16	IN28	I	RS-232C
P1-A17	IN29	I	RS-232C
P1-C17	IN30	I	RS-232C
P1-A18	IN31	I	RS-232C
P1-C18	IN32	I	RS-232C
P1-A24	OUT1	O	RS-232C
P1-C24	OUT2	O	RS-232C
P1-A25	OUT3	O	RS-232C
P1-C25	OUT4	O	RS-232C
P1-A26	OUT5	O	RS-232C
P1-A30	SELALARM	O	TTL
P1-A31	GND	I/O	0V
P1-C31	GND	I/O	0V
P1-A32	+5	I/O	+5V
P1-C32	+5	I/O	5V

Continued

SPECIFICATIONS

(Continued)

Table 4 - Jumper Definition And Configuration

JUMPER	SHORTING PLUG	POSITION	DESCRIPTION
J2	P2	1 & 2 2 & 3	150 BUAD DATA SELECTION 9600 HZ XLOCK SELECTION
J3	P3	1 & 2 2 & 3	150 BUAD DATA SELECTION 9600 HZ XLOCK SELECTION
J4	P4	1 & 2 2 & 3	150 BUAD DATA SELECTION 9600 HZ XLOCK SELECTION

DESCRIPTION

The Digital Selector Module is used in the **EDACS** Simulcast System. It is used and configured as Digital Selector 1 (150 baud data selector) and Digital Selector 2 (9600 Hz clock selector). The Digital Selector Module is used to automatically select a data stream and manually advance to the next source containing a valid data stream. The source is displayed on the front of the module (2 digit LED display.) Digital Selector 1 is a low speed data (150 bits per second) selector. Digital Selector 1 is used only at the control site. It is used to select a low speed data serial stream from one of twenty-five **EDACS** stations. All **EDACS** stations at a site generate identical low speed data. The low speed data (150 baud) is generated in the GETC logic module of the GETC shelf assembly.

Digital Selector 2 is a high speed data (9600 Hz clock) selector. Digital Selector 2 is used only at the control site. It is used to select the master oscillator that generates the high speed data clock (two oscillators exist on each Digital Selector Module.)

Digital Selector 1 and Digital Selector 2 are physically located in the sync unit assembly of the control simulcast site. The Digital Selector 1 Module plugs into slot 3 (J3) of the sync unit assembly. The Digital Selector 2 Module plugs into slot 12 (J12) of the sync unit assembly.

Clock and control circuitry on the Digital Selector Module provides the scanning mechanism to select a channel or source that contains a valid data stream. The scan rule used is the presence of an active falling edge on the RS-232C input within ten clock cycles. The clock cycle corresponds to 75 Hz for Digital Selector 1 (150 baud source) and 4800 Hz for Digital Selector 2 (9600 Hz squarewave source). Should the channel or source fail, the Digital Selector Module will automatically advance to the next channel and scan for a valid stream during 10 clock cycle times. This is continued until a valid stream is found.

A jumper is located on the Digital Selector Module to configure it for 150 baud selection (Digital Selector 1) or 9600 Hz clock selection (Digital Selector 2).

A momentary switch (SW1) is provided to enable the manual advance function.

A single pole, double throw switch (SW2) is provided to enable the test mode of operation. In the test mode a fixed 75 Hz or 4800 Hz is used as the data stream input for the test.

Two LED character displays are used to visually indicate the selected channel or source.

The Digital Selector generates an alarm output when it is not locked onto a channel or source.

CIRCUIT AND FUNCTIONAL DESCRIPTION

The Digital Selector Module provides the functions for the Digital Selector 1 Module and the Digital Selector 2 Module. Digital Selector 1 Module selects the 150 baud data source, from up to 25 **EDACS** stations at the control point, to be sent to the transmit sites for low speed sub-audible transmissions. Digital Selector 2 Module selects the 9600 Hz reference clock, one of two oscillators located on this module, to be sent to the **EDACS** station for synchronous operation.

Digital Selector 1 receives the 150 baud data from the **GETC** logic module of the **EDACS** station (through the **GETC** Interface Module and the cross connect panel). Digital Selector 1 selects one of the data sources (of up to 25 stations) to be sent to the **FSK** Modem Module of the Sync Unit. The **FSK** Modem Module encodes the low speed data stream (150 baud) using a frequency shift keyed signal. The rule used to select the 150 baud data (from up to 25 stations) is the existence of falling edge on the sampled low speed data signal during a 133 msec time period. If no falling edge is detected, the next station in the sequence is scanned for a falling edge of the low speed data within the 133 msec sample period. This process continues until a valid station is found. At this point, the low speed data is sampled for 133 msec on the locked-on station. If the data disappears for 133 msec, scanning is resumed at the next station.

All **EDACS** stations generate identical low speed data. The low speed data encodes group information to allow mobile users to quickly respond to high priority calls.

Digital Selector 1 is used at the control site only. The transmit sites receive the low speed data (150 baud) from the control site and transmit it from the **EDACS** stations.

Digital Selector 2 selects one of the two clock sources to be sent to the **EDACS** stations. The 9600 Hz selected clock is used to synchronize the system. The **GETC** Interface Module of each **EDACS** stations uses a phase lock loop to generate a synchronous 11.0592 MHz operating clock from the selected 9600 Hz reference clock. The 11.0592 MHz synchronous clock from the **GETC** Interface Module is sent to the **GETC** logic module to provide the timing clock for all data signalling and station control. The rule used to select the 9600 Hz selected clock is the existence of falling edge on the sampled reference clock signal during a 2.1 msec time period. If no falling edge is detected, the next channel bank card in the sequence is scanned for a falling edge of the reference clock within the 2.1 msec sample period. This process continues until a valid channel bank card is found. At this point, the reference clock is sampled for 2.1 msec on the locked-on channel bank card. If the clock disappears for 2.1 msec, scanning is resumed.

The momentary switch (SW1) on the Digital Selector Module enables a manual advance to the next valid channel (150 baud data or 9600 Hz clock). This switch bypasses a portion of the scanning circuitry and allows a forced increment in the channel number. The data selection is thereby moved to the signal until a valid lock is established.

A toggle switch (SW1) is included on the Digital Selector Module to place the channel selection is a test mode of operation. This allows the user to manually step through the 32 positions of the data selector. An LED is included on module to depict the test mode of operation.

Two numeric LED displays are used to depict the number of the valid (locked on) signal. A **PROM** is used for the table look up in generating the LED matrix display lines from the binary address of the locked on channel. The display on Digital Selector 1 will be from 1 to the number of channels in the system. The display on Digital Selector 2 will be either 31 or 32 depending on which reference 9600 Hz clock is selected.

A 19.2 kHz oscillator (U23) is used to provide the timing for the scanning circuitry on the Digital Selector Module.

RS-232C drivers (U14) are used to buffer the selected channel (data or clock) to the **FSK** Modem Module (from Digital Selector 1) or to the **GETC** Interface Module (from Digital Selector 2).

RS-232C receivers (U1 - U8) are used to buffer the one of 32 sources to the Digital Selector Module. The sources are the **GETC** Interface low speed data (to Digital Selector 1) or clocks (to Digital Selector 2).

A flip flop (U25) generates an alarm output (TTL high level) whenever the Digital Selector Module is not locked on a valid channel.

A Block Diagram of the Digital Selector Module is shown in Figure 1.

The Digital Selector consists of the following hardware components:

- Five (5) 8:1 digital muxes (U9 - U13) to multiplex one of 32 sources to be scanned.
- One (1) RS-232C diver (U14) to buffer the selected channel (150 data or 9600 clock).
- Eight (8) RS-232C receivers (U1 - U8) to buffer the incoming channel information.
- One (1) 555 timer (U23) for the 19.2 KHz oscillator.
- One (1) binary counter (U15) for the sampling scanning interval sample period.
- One (1) decade counter (U16) to derive the sample period width.

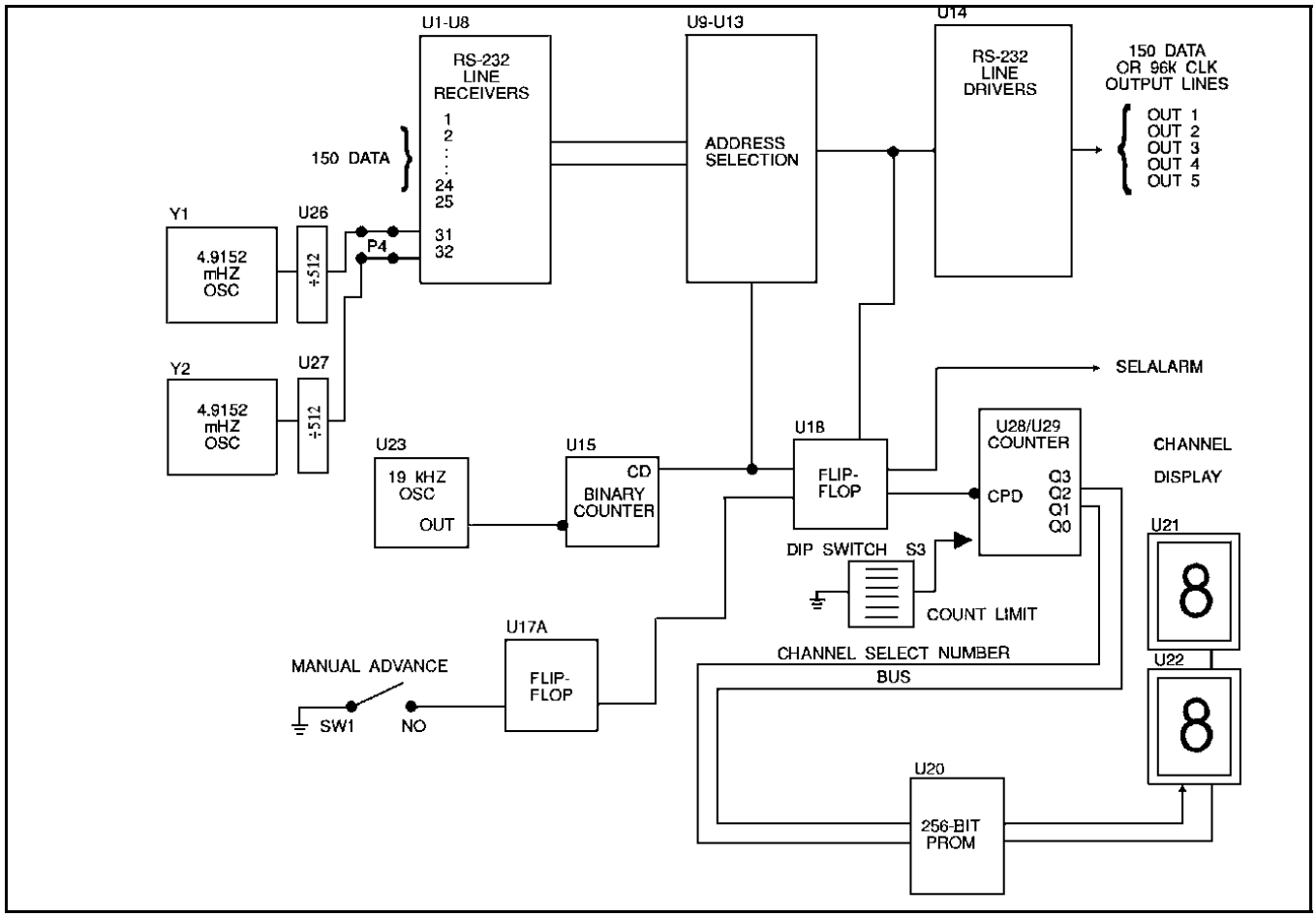


Figure 1 - Digital Selector Block Diagram

- One (1) Up-Down counter (U28, U29 & U30) to count the present channel number.
- Two (2) flip flops (U17) for manual advance override and next channel increment.
- One (1) **PROM** (U20) for channel number table lookup to drive the led displays.
- Two (2) LED matrix displays (U21 - U22) to visually depict the channel number.
- One (1) flip flop (U25) to generate the alarm output for no valid channel.

CONNECTORS AND SYSTEM INTERFACE

There is one connector used on the Digital Selector Module, P1. Connector P1 is used to mate the Digital Selector Module to the Sync Unit Assembly. The Digital Selector plugs into slot 3 (J3) (150 baud selection) or slot 13 (J13) (9600 Hz selection) of the Sync Unit. A description of the various signals, data, and clocks used between the Digital Selector Module and the Sync Unit is summarized in Table 3.

DIGITAL SELECTOR MODULE AND CROSS CONNECT PANEL SIGNAL FLOW

IN1 Through IN32

IN1 through **IN32** are RS-232C compatible inputs derived from the GETC low speed data (Digital Selector 1 operation) or from the 9600 Hz clock (Digital Selector 2 operation). Digital Selector 1 receives the low speed data from the **GETC** logic modules (through the **GETC** Interface Module and the cross connect panel) of up to twenty-five Control Point **GETC**'s. Digital Selector 2 receives 9600 Hz clocks from two reference oscillators located on the Digital Selector Module.

OUT1 Through OUT5

OUT1 through **OUT5** are identical RS-232C outputs from the Digital Selector Module. These outputs are derived from the valid channel data (150 baud data for Digital Selector 1) or clock (9600 Hz clock for Digital Selector 2) and are sent to the FSK Modem Module (from Digital Selector 1) or to up to 25 GETC Interface Module's (from Digital Selector 2) for synchronous operation.

SELALARM

SELALARM is a TTL output from the Digital Selector Module and is sent to the Subsystem Alarm Module of the Sync Unit. This signal indicates the loss of a locked channel (that is, the data selector is in the process of scanning).

JUMPER DEFINITION AND CONFIGURATION

Table 4 summarizes the jumper configuration for the two modes of operations.

Switch SW1 provides a manual advance onto the next valid channel. This switch is used to force the data selector module to lock onto alternate valid channel. The normal position of this switch is manual advance disable.

Switch SW2 provides the test mode of operation. This switch is used to step through all 32 position of the Scan Circuitry, using the manual advance switch.

POWER DISTRIBUTION AND FILTERING

The +5 volt power supply used by the Digital Selector Module is derived from the simulcast power supply. The +5 volt power input (+5) is used to power all active components on the Digital Selector Module. The active components include the 8:1 digital muxes, the RS-232C driver and receivers, the 19.2 KHz oscillator, the scanning circuitry, the **PROM**, and the LED matrix displays.

There are power bypass capacitors on the Digital Selector Module to filter any power noise transients or spikes from affecting circuit operation and module performance. The capacitors are 0.1 μF in value and are numbered C3 through C28.

DIGITAL MULTIPLEXER

The digital multiplexers consist of U9, U10, U11, U12, and U13. These devices are used to scan up to 32 sources. The data is derived from **IN1** through **IN32** and buffered through the **RS-232C** receivers, U1 through U8, before arriving at muxes, U9 through U12.

The 8:1 muxes, U9 through U12 derive their steering (address or select inputs) from the lowest three bits of the channel address counter, U28, U29 & U30. The 32 sources enter the muxes, U9 through U12. Data mux U13 select one of the four 8:1 muxes or a fixed 75 Hz from the clock divider, U15.

The select control for U13 is derived from the most significant two bits of the channel address and the test mode switch position. If test mode is enabled, LED D1 is lit, and a high is impressed on the C input to U13. This steers the 75 Hz to the **SELOUT** line. If test mode is disabled, the two channel address lines, **SEL16** and **SEL8**, select the 4 data muxes.

The 4 data muxes use the select lines, **SEL4**, **SEL2**, and **SEL1** from the channel address counter (U28, U29 & U30) to select one of 8 inputs per device.

DIGITAL SELECT OSCILLATOR

The digital select oscillator consists of a free running 19.2 kHz clock derived from a 555 timer, U23. Resistors and capacitors set up the nominal free running frequency.

The 19.2 kHz output, U23 pin 3, is input to the dual stage binary counter, U15. Both sections of U15 are coupled such that the falling edge of the first QD output (pin 8) is input to the next stage as an input (pin 1). This coupling forms an 8 bit ripple counter.

Selected taps off of U15 are used to generate the nominal 4800 Hz and 75 Hz clocks for the sampling circuitry.

The 4800 Hz clock is used for the Digital Selector 2 configuration to sample the 9600 Hz clock.

The 75 Hz clock is used for the Digital Selector 1 configuration to sample the 150 baud data from the **GETC** Interface Module.

Jumper J2 and shorting plug P2 configure the data selector module for 9600 Hz clock sampling (positions 2 and 3) or 150 data sampling (positions 1 and 2). The appropriate clock, 4800 Hz or 75 Hz is sent to the decade counter, U16, to set up the sample period.

DIGITAL SELECT SAMPLER AND CHANNEL SELECTOR

The digital sampler consists of the decade counter U16 (which generates a sample period of 10 clock periods long), data sampling flip flop U18 (which captures a rising edge of **SELOUT** within the sample period as well as enables continued counting of the channel counter U28, U29 & U30 if a valid channel is not found), and nor gates U24 to perform the required gating for the sampling.

The clock input to the sample period decade counter U16 is generated from the data select oscillator, 1 counter (U15 and U23) and selected via jumper J2. The clock input is 4800 Hz for 9600 Hz clock selection and 75 Hz for low speed data selection.

The decade counter U16 is a free running counter that counts from 0 to 9 and rolls back to 0. During the count from 7 to 8, the **SELOUT** line sampled for a rising edge during the sample period. If a rising edge had occurred, U18 pin 5 will be logic low which is sent through gates U24 to the input U18 pin 12. The count from 7 to 8 on the decade counter U16 samples the state of U18 pin 12. If a low is present (**SELOUT** had a rising edge), the output U18 pin 8 will be a logic high (or remain a logic high). If **SELOUT** is ever detected to have no rising edges during the sample period, U18 pin 8 will go to a logic low, thereby generating a clock edge to the channel address counter, U28, U29 & U30, and decrementing the count to the next channel for subsequent sampling.

The manual advance switch and flip flop U17 is coupled into the **NOR** gates, U24. This provides a manual channel decrement by forcing the input of flip flop U18 pin 12 to a logic high. The manual advance switch resets flip flop U17 pin 6. Upon release of the momentary switch, a rising edge is generated on U17 pin 11. This sets U17 pin 9 high to perform the manual advance function. U17 pin 9 is subsequently reset via the channel decrement pulse from U18 pin 8, thereby allowing only one channel advance per switch toggle.

Figures 2, 3 and 4 depict the timing diagram for a valid lock on channel, no valid channel, and manual advance from a lock on channel, respectively.

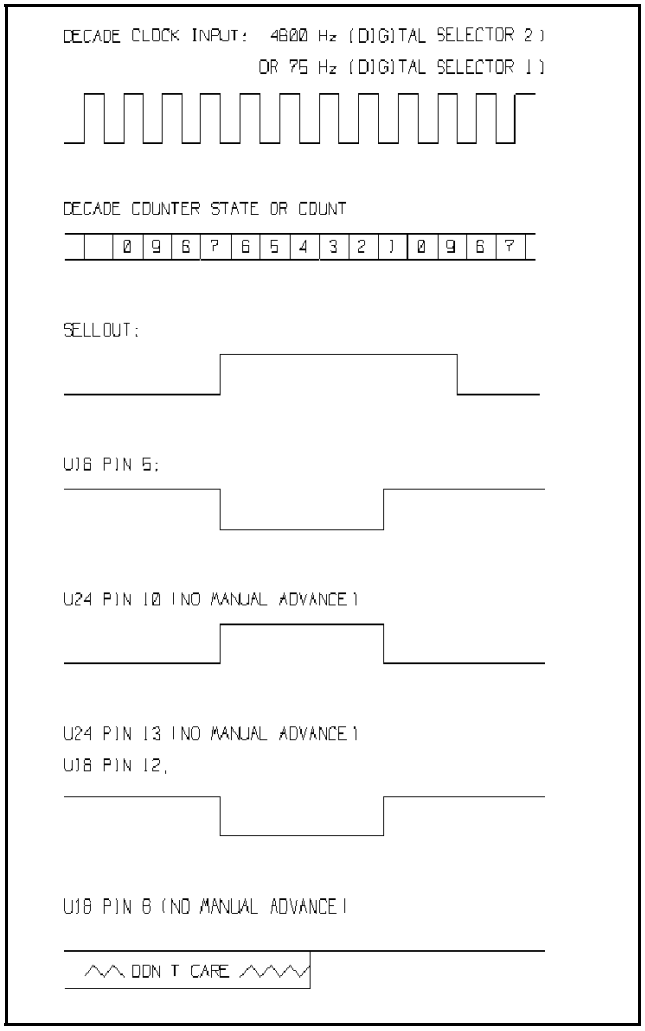


Figure 2 - Timing Diagram For A Valid Locked On Channel Without Manual Advance

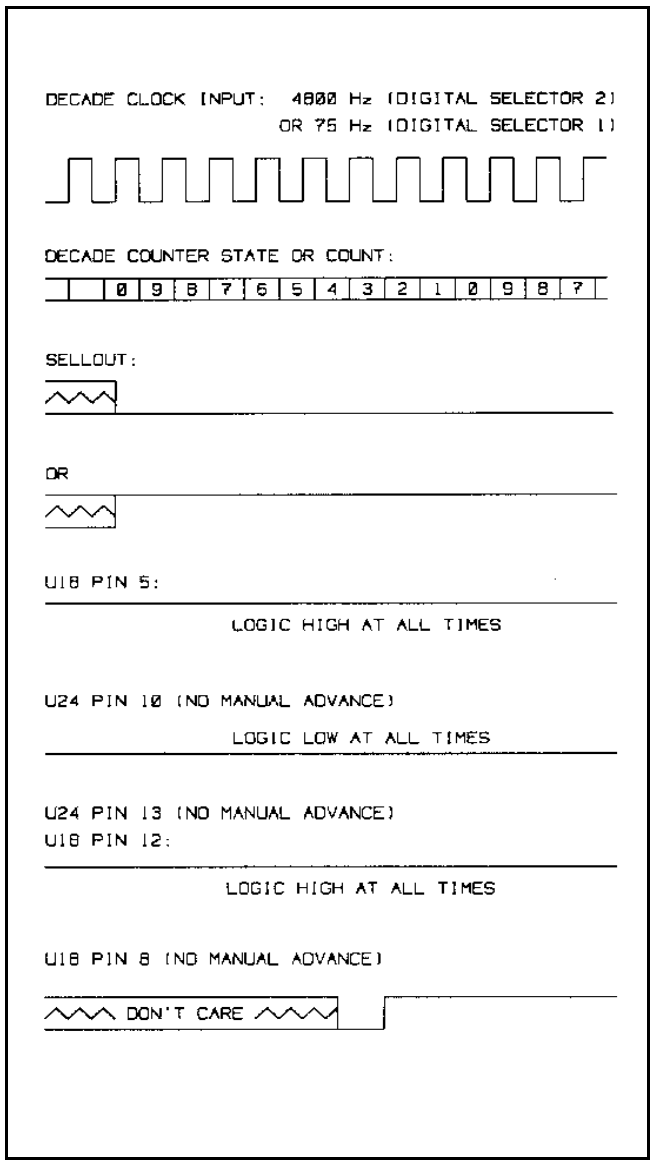


Figure 3 - Timing Diagram For A Non-Valid Channel Without Manual Advance

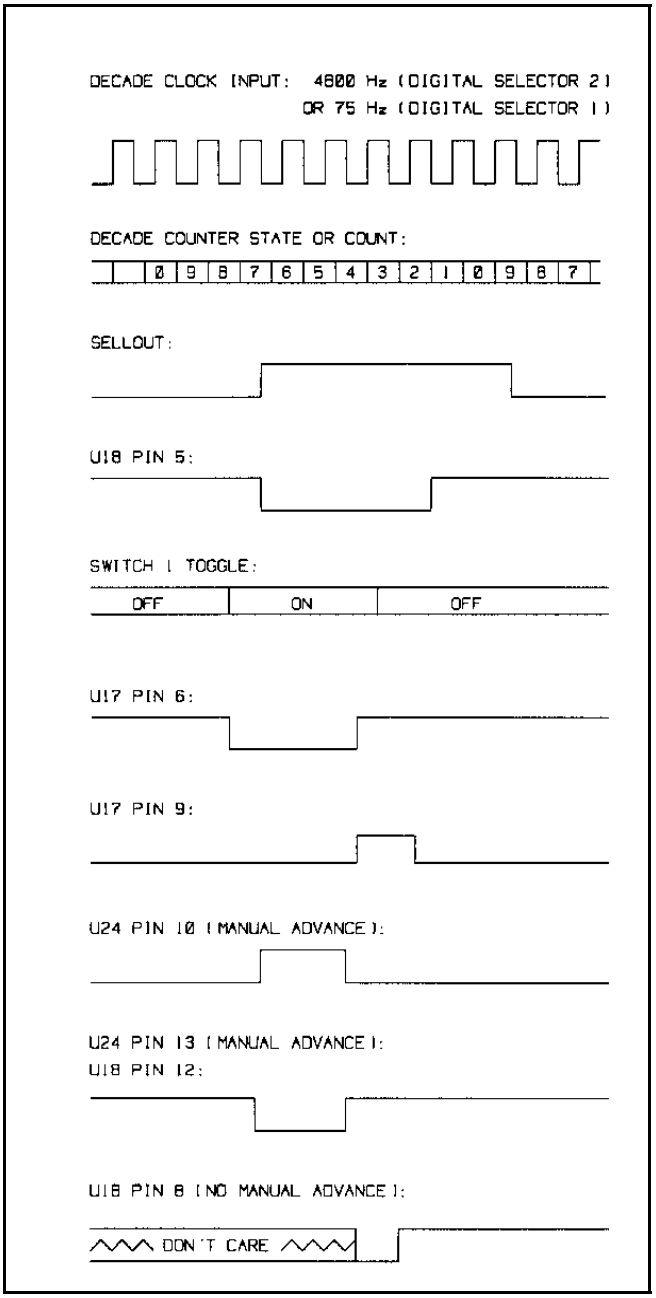


Figure 4 - Timing Diagram For A Valid Locked On Channel with Manual Advance

TEST, DISPLAY, AND ALARM FUNCTIONS

For the Digital Selector 1 configuration, the 75 Hz clock is the clocking input to the decade counter. The 75 Hz clock is also the **SELOUT** line when the test enable switch is set to the test position. The decade counter period therefore will always have transitions of the 75 Hz clock within its sample period. The channel selector will lock onto the present channel (unless the manual advance switch is thrown to manually force the channel selection to the next decrement).

For the Digital Selector 2 configuration, the 4800 Hz clock is the clocking input to the decade counter. The 75 Hz clock is the **SELOUT** line when the test enable switch is set to the test position. The decade counter period will not have a single transition of the 75 Hz clock will 10 clock periods of the 4800 Hz clock input to the counter. The Digital Selector 2 configuration will thereby continually decrement the channel selection and never find a valid channel.

The channel number selection is performed by counter U28, U29 & U30, configured as an 8 bit ripple counter. The count of U28, U29 & U30 is sent to the digital multiplexers to select one of 32 possible sources for the data select input. A dip switch allows search to be restricted to a subset of channels (1 dip switch setting) so that LSD search will not linger in unavailable channels.The channel number is also sent to the look up PROM, U20.

The PROM is used to generate the logic signals to the channel displays, U21 and U22. U21 is the most significant channel display and U22 is the least significant channel display. The PROM has a simple lookup such that the binary channel number from 0 to 31 (decimal) is encoded to the displays as 1 to 32, respectively. The PROM U20, also generates a blanking output to U21 to blank the display if the binary count input is less than 9 (or less than 10 at the PROM output).

The Digital Selector Module also generates an alarm output indicating whether the Digital Selector Module is presently scanning for the next valid channel. This function is performed by flip flop U25. The operation of flip flop U25 is similar to flip flop U18 which generates the clock input to the channel counter, U28, U29 & U30.

Both U25 and U18 have the same clock input. The D input to U25 and U18 are identical when the manual advance is not used. U25 does not register an alarm condition based on the manual advance switch override, rather it only generates an alarm based on the absence of a rising edge on **SELOUT** within the sample period. The alarm output is a minimum of one sample period long and can change state only at the end of each sample period.

CRYSTAL CONTROLLED OSCILLATORS

Two crystal controlled oscillators (Y1 - Y2) operating at 4.9152 MHz provides the reference for generating the two 9600 Hz reference clocks. The output of the oscillator is divided by 512 by counter (U26, U27). Jumpers J3 and J4 are used to connect these oscillators to **IN31**, **IN32** inputs when the module is used as Digital Selector 2.

MAINTENANCE

The Digital Selector Module has jumpers that must be configured for the normal mode of operation (See below).

The switches SW1 and SW2 are to be configured for the normal mode of operation. SW1 is a momentary switch that performs the manual advance function. SW2 is a toggle switch that enables the test mode of operation. The normal positions of these switches for system operation are shown below:

Jumper	Shorting Plug	Position	Definition
J2	P2	1 & 2	Digital Selector 1 (150 baud selection)
		2 & 3	Digital Selector 2 (9600 Hz selection)

There are no other adjustments on the Digital Selector Module.

Switch	Position	Definition
SW1	down	manual advance disabled
SW2	up	test mode disabled

TEST AND SERVICE

The following test equipment is necessary to test the Digital Selector Module as part of the simulcast system.

1. Extender Card
2. Tektronix R5223 Digital Storage Scope or equivalent
3. Triplett Model 630-PL Type 5 or equivalent

4. Test Cables as required

5. HP 8116 Pulse/Function Generator or equiv-alent.

The following steps are necessary to test the Digital Selector as part of the simulcast system.

1. Configure the jumpers for the desired mode of operation (150 baud data or 9600 Hz clock selection).

2. Install the Digital Selector Module as part of the simulcast system (slot 3 for 150 baud data selection or slot 15 for 9600 Hz clock selection).

3. Verify the presence of +5 volt power (+5).

4. Digital Selector 1 (150 baud data selection)

   Verify 150 baud data on **IN1** through **IN32** as per site configuration.

   Verify 150 baud data on **SELOUT**.

   Verify 150 baud data on **OUT1** through **OUT5**.

   Verify the operation of the manual advance switch to search for other channels of valid low speed data.

   Verify the operation of the test enable switch to lock onto the present channel, followed by the manual advance switch to increment to the next channel irrespective of whether it contains valid low speed data.

   Digital Selector 2 (9600 Hz selection)

   Verify 9600 Hz clock on **IN31** and **IN32**.

   Verify 9600 Hz clock on **SELOUT**.

   Verify 9600 Hz clock on **OUT1** through **OUT5**.

   Verify the operation of the manual advance switch to search for other channels of valid 9600 Hz clocking.

   Verify the operation of the manual advance switch to search for other channels of valid low speed data.

   Verify the operation of the test enable switch to lock onto the present channel, followed by the manual advance switch to increment to the next channel irrespective of whether it contains valid low speed data.

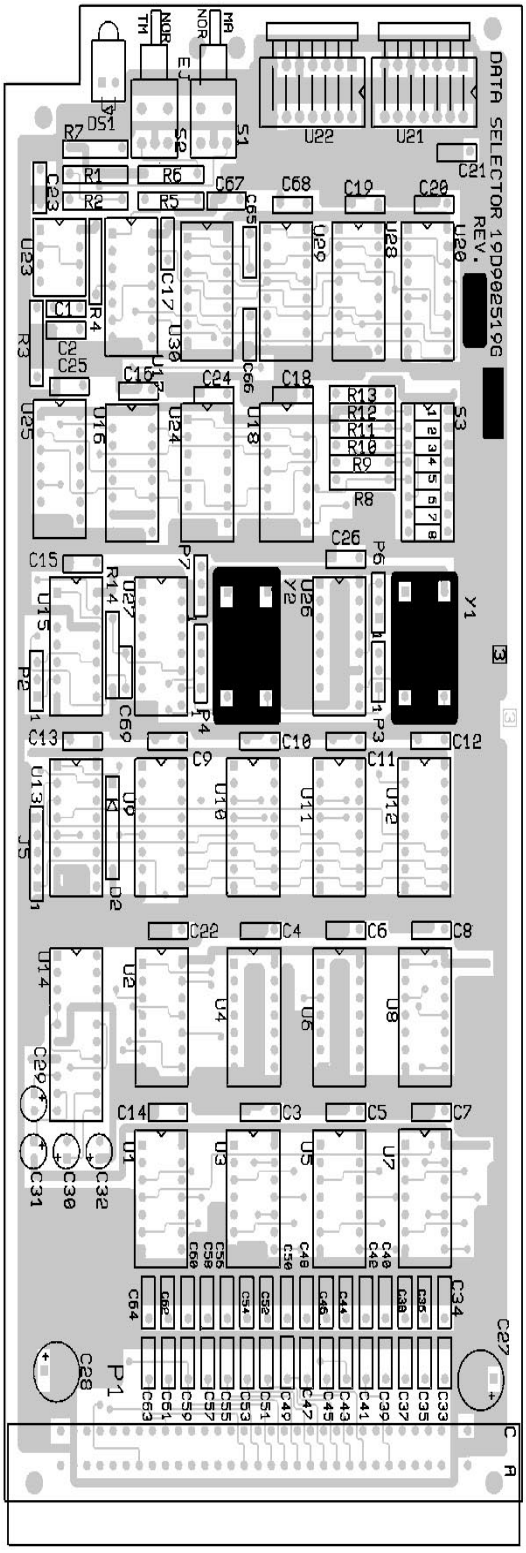
5. Reconfigure the module back to normal system operation and install back into the proper slot of the Sync Unit Assembly.

ERICSSON

Ericsson GE Mobile Communications Inc.
Mountain View Road• Lynchburg, Virginia 24502

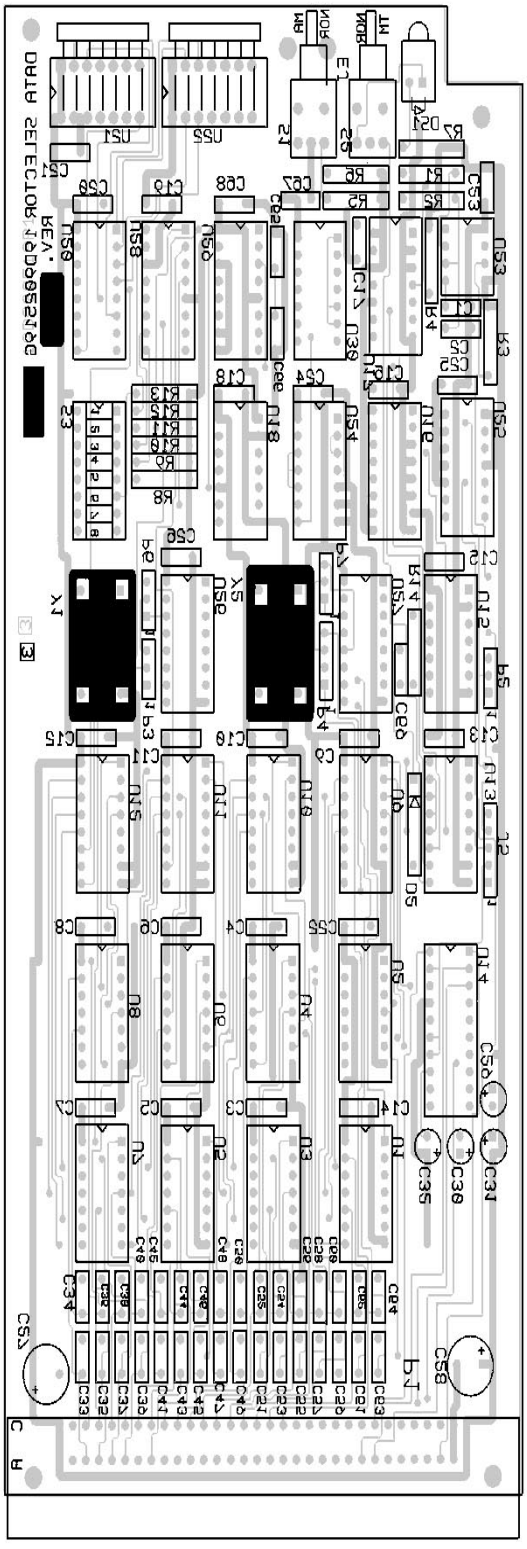
Printed in U.S.A.

Component Side

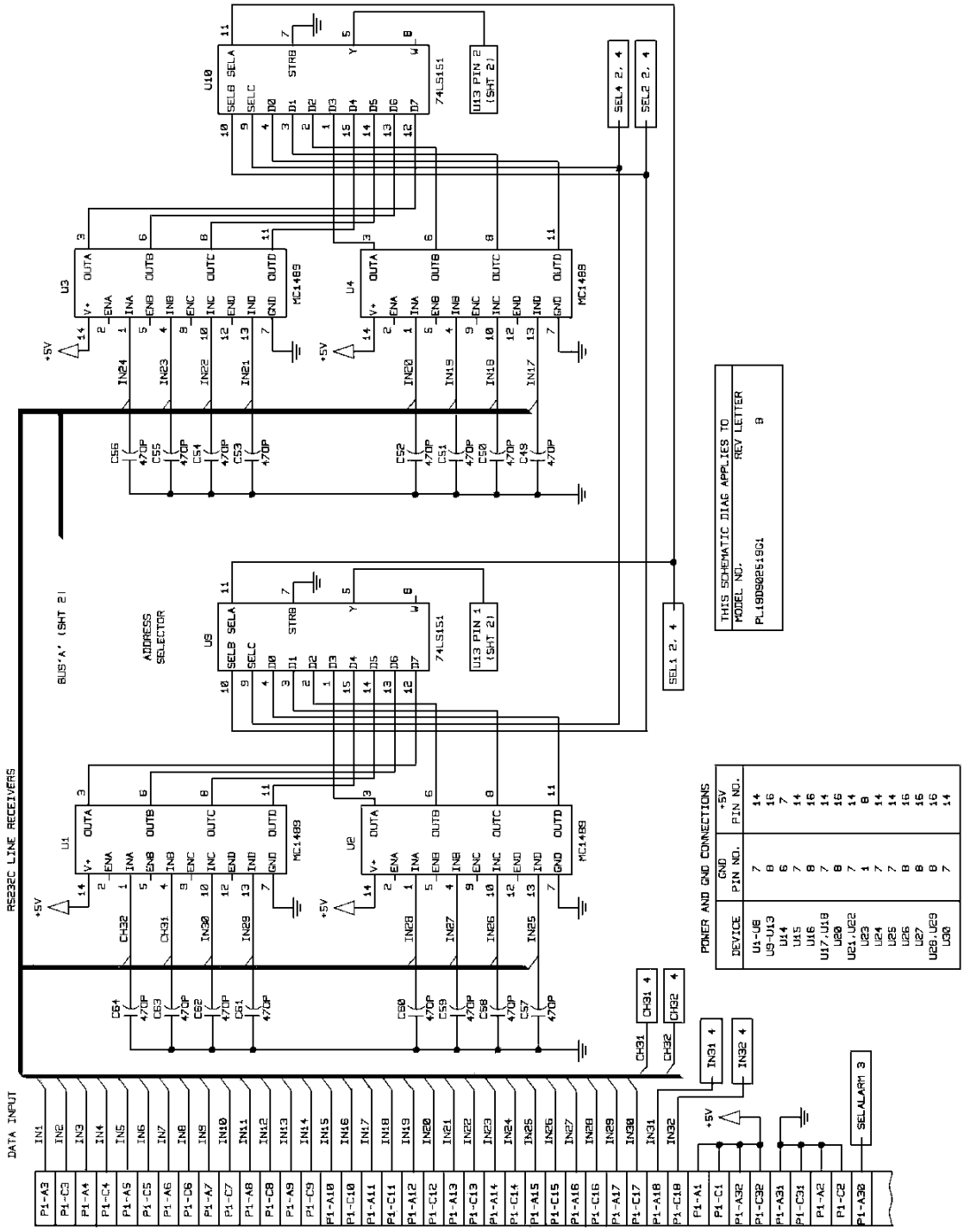


19D902518, Component Side, Rev. 2

Solder Side

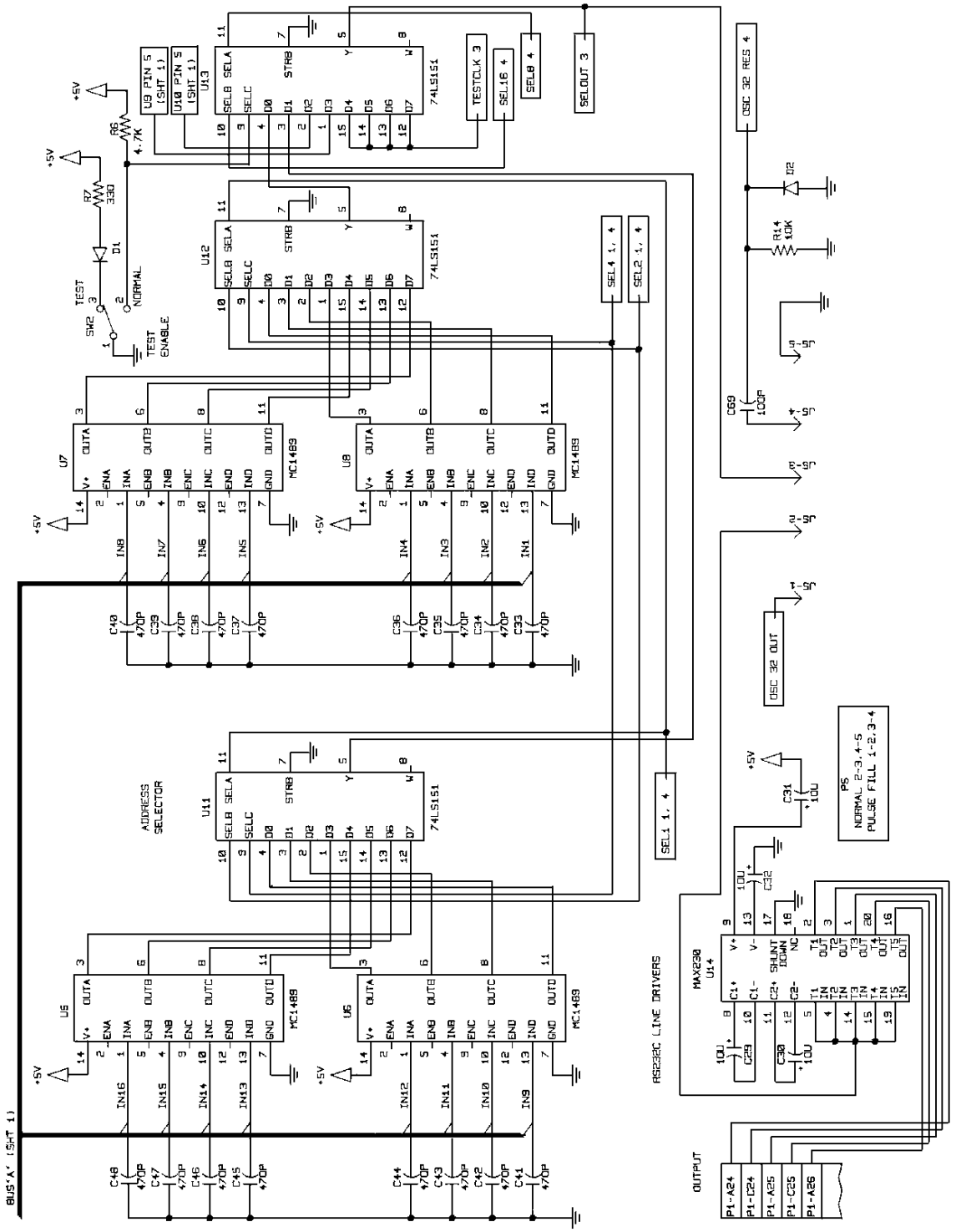


19D902518, Solder Side, Rev. 2



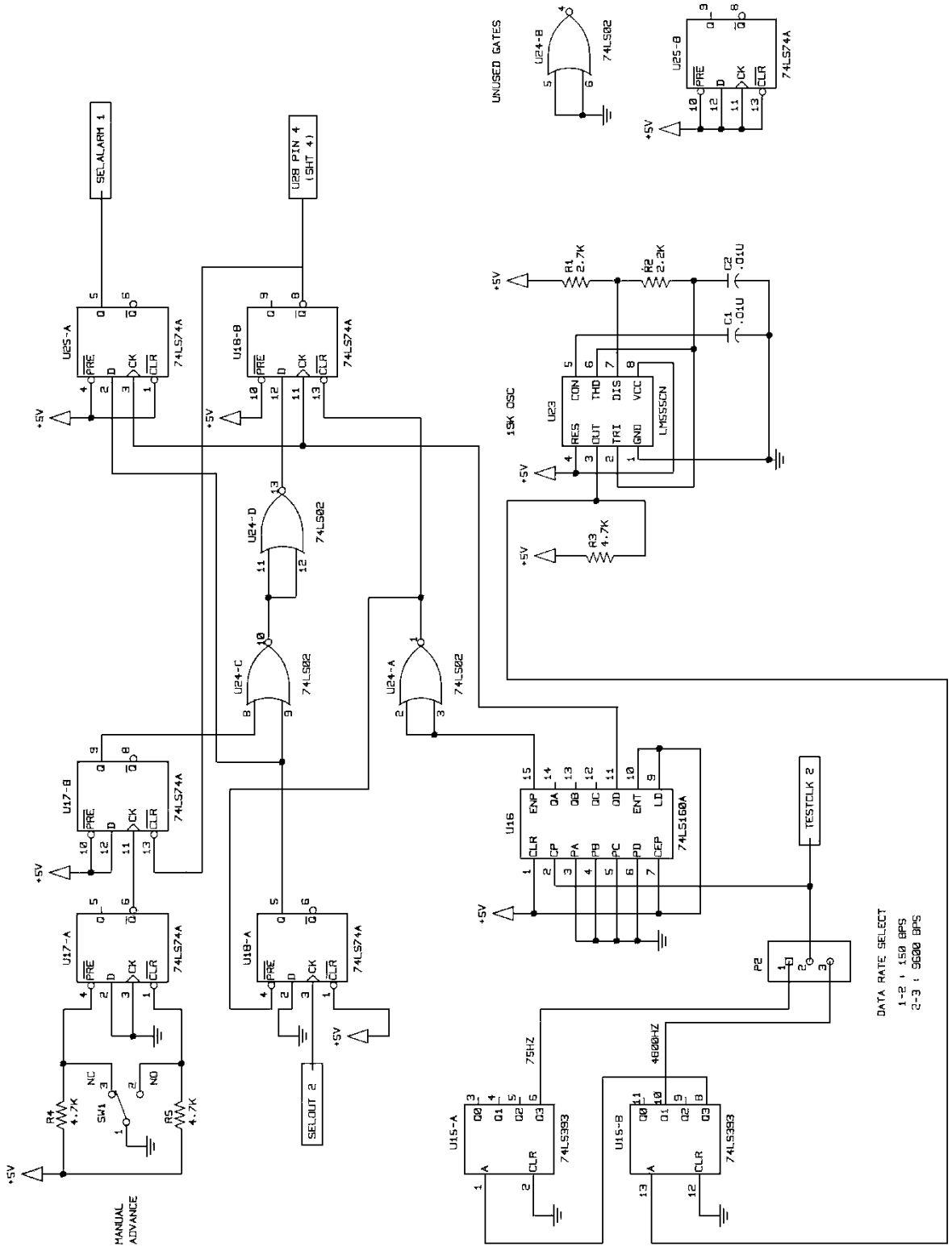
DIGITAL SELECTOR
19D902519G1

(19C851934, Sh. 1, Rev. 3)



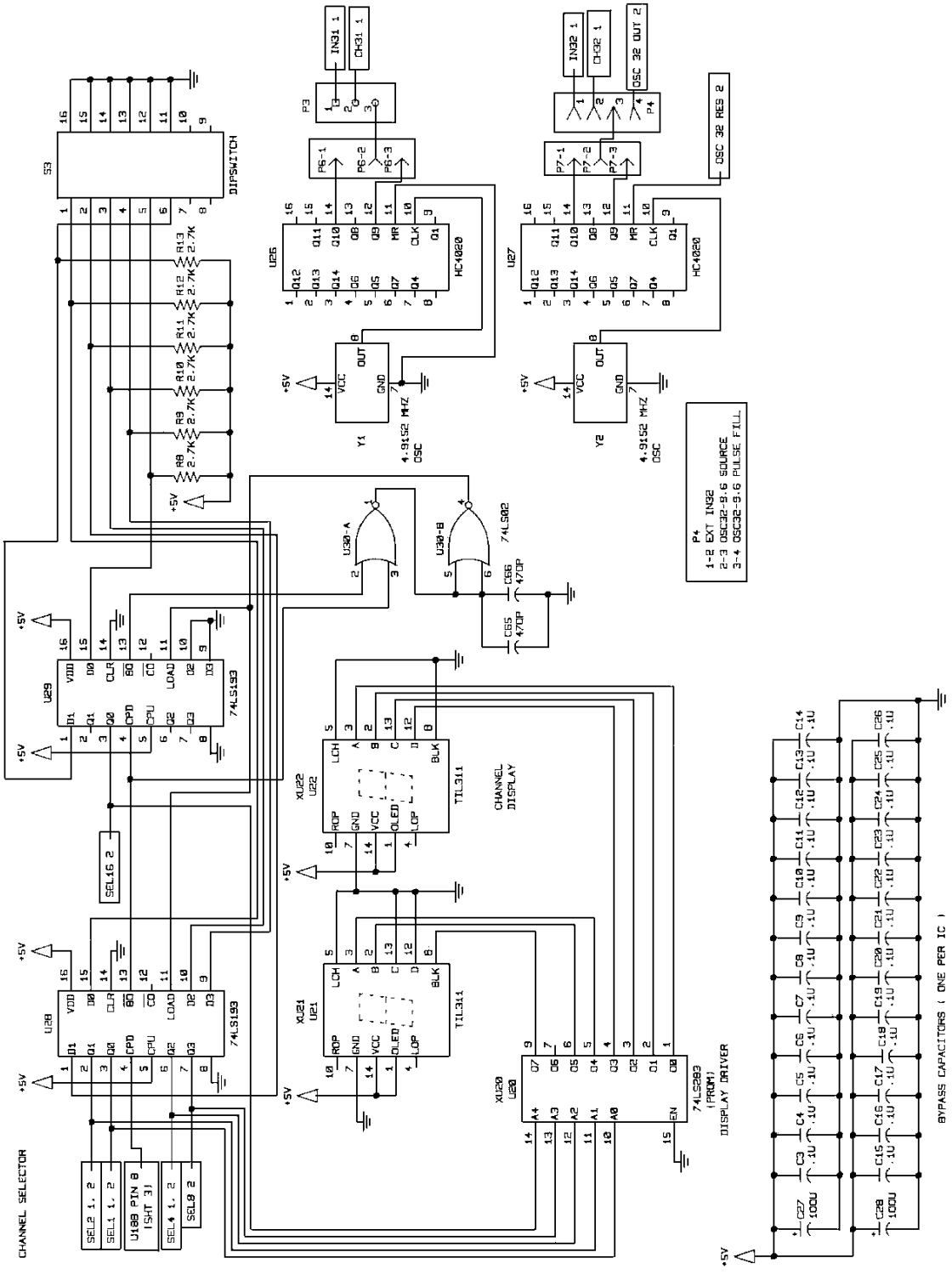
DIGITAL SELECTOR
19D902519G1

(19C851934, Sh. 2, Rev. 2)



DIGITAL SELECTOR
19D902519G1

(19C851934, Sh. 3, Rev. 3)



DIGITAL SELECTOR
19D902519G1

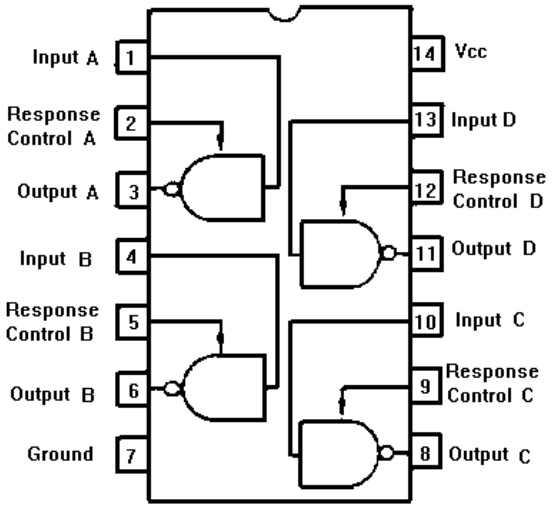
(19C851934, Sh. 4, Rev. 2)

DIGITAL SELECTOR MODULE
19D902519G1
ISSUE 2

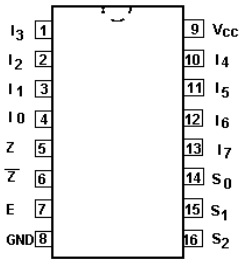
SYMBOL	PART NUMBER	DESCRIPTION
		— — — — CAPACITORS — — —
C1 and C2	T644ACP310K	Polyester: 0.01 μF.
C3 thru C26	7644ACP410K	Polyester: 0.1 μF.
C27 and C28	19A703314P1	Electrolytic: 100 μF, 10 VDCW.
C29 thru C32	19A701534P7	Tantalum: 10 μF, 16 VDCW.
C33 thru C66	19A700233P5	Ceramic 470 pF ±5%, 50 VDCW.
C67 and C68	T644ACP410K	Polyester: 0.1 μF.
		— — — — — DIODES — — — —
DS1		Opto electric, sim to DIALIGHT 550-5106.
		— — — — — JACKS — — — —
J2 and J4	19A704852P2	Printed wire connector.
		— — — — — PLUGS — — — —
P1	19B801587P1	Connector, two part.
P2 thru P4	19A702104P2	Connector
		— — — — RESISTORS — — —
R1	H212CRP227C	Carbon film: 2.7K ohms ±5%, 1/4 w.
R2	H212CRP222C	Carbon film: 2.2K ohms ±5%, 1/4 w.
R3 thru R6	H212CRP247C	Carbon film: 4.7K ohms ±5%, 1/4 w.
R7	H212CRP133C	Carbon film: 330 ohms ±5%, 1/4 w.
R8 thru R13	H212CRP227C	Carbon film: 2.7K ohms ±5%, 1/4 w.
		— — — — SWITCHES — — —
S1		Switch; sim to AT1F-RA-1-MON.
S2		Switch; sim to AT1DGRA1-SPDT.
S3	19B800010P2	Switch, push.

SYMBOL	PART NUMBER	DESCRIPTION
		— — INTEGRATED CIRCUITS —
U1 thur U8	19A116704P2	Linear, digital.
U9 thru U13	19A700037P361	Digital.
U14		Integrated Circuit: sim to Maxim MAX230CPP.
U15	19A7000374P421	Digital.
U16	19A700037P367	Digital.
U17 and U18	19A700037P335	Digital.
U20	19J706246P2	Digital.
U21 and U22		Integrated Circuit; sim to Texas Instruments TIL311-DISPLAY.
U23	19A701865P1	Linear.
U24	19A700037P303	Digital.
U25	19A700037P335	Digital.
U26 and U27	19A703987P16	Digital Logic.
U28 and U29	19A700037P381	Digital.
U30	19A700037P303	Digital.
		— — — — SOCKETS — — — —
XU20	19A700156P9	Socket.
XU21 and XU22		Socket, 14 pin; sim to Aries-14-822-90C
		— — — — CRYSTALS — — — —
Y1 and Y2		Crystal CTS Knight; sim to MX0-55GA-2C-4.9152 MHz.
		— — — MISCELLANEOUS — —
		Card Handle; sim to VERO 21-0243G PULL.

* COMPONENTS, ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES



RS-232C LINE RECEIVERS U1-U8
MC1489AN

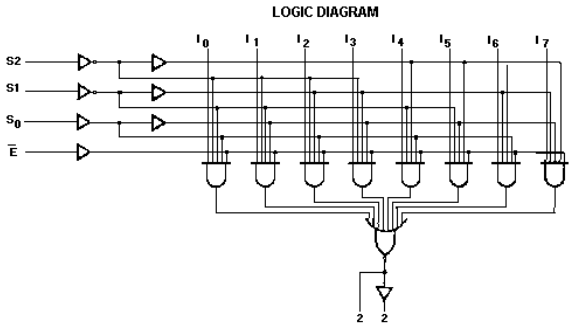


TRUTH TABLE

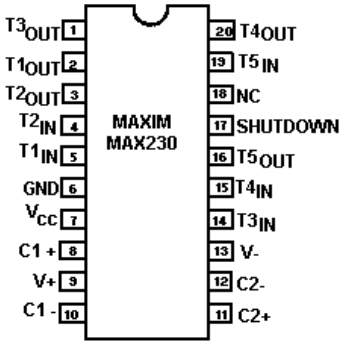
	INPUTS			OUTPUTS	
$\bar{E}$	S_2	S_1	S_0	$\bar{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\bar{I_0}$	I_0
L	L	L	H	$\bar{I_1}$	I_1
L	L	H	L	$\bar{I_2}$	I_2
L	L	H	H	$\bar{I_3}$	I_3
L	H	L	L	$\bar{I_4}$	I_4
L	H	L	H	$\bar{I_5}$	I_5
L	H	H	L	$\bar{I_6}$	I_6
L	H	H	H	$\bar{I_7}$	I_7

H = HIGH Voltage Level
L= LOW Voltage Level

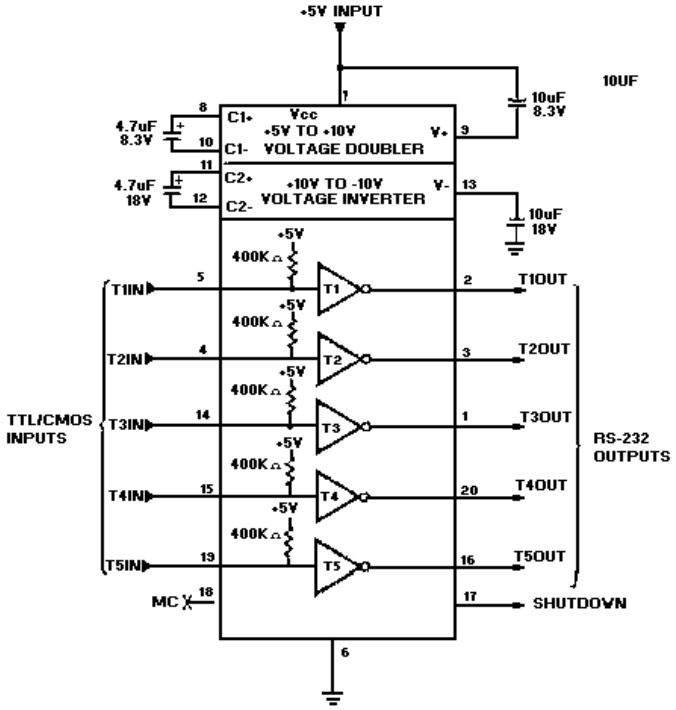
LOGIC DIAGRAM



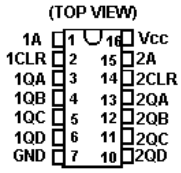
ADDRESS SELECTORS U9-U13
74LS151N



20 Lead Small Outline
also available.

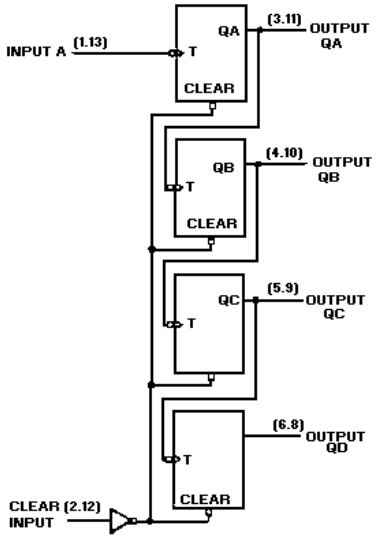


RS-232 LINE DRIVERS U14
MAX230CPP

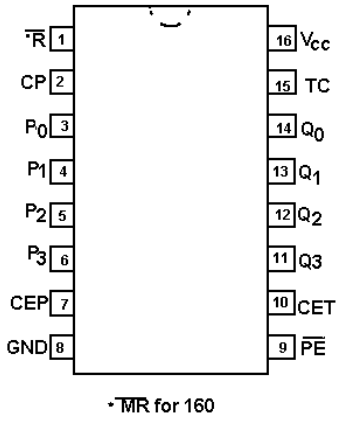


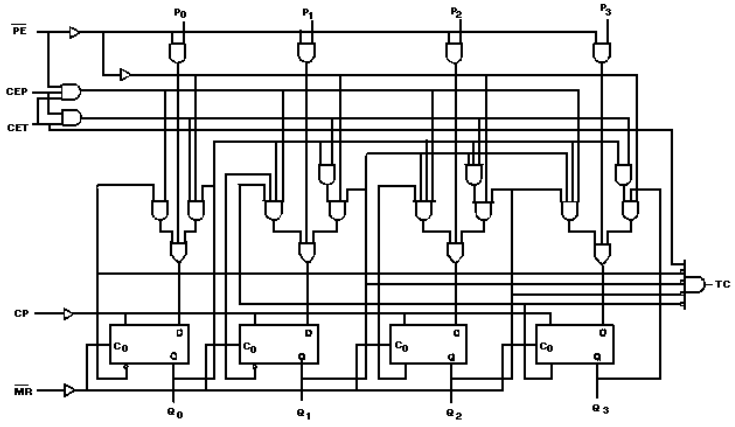
COUNT SEQUENCE
(EACH COUNTER)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H



COUNTERS U15, U19
SN74LS393N

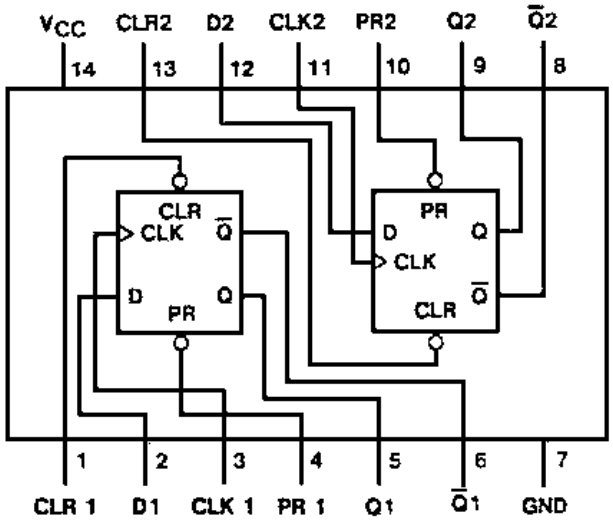




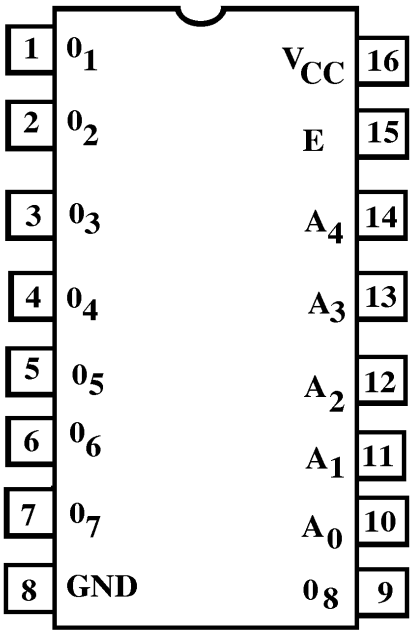
DECADE COUNTER U16
74L9160AN

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

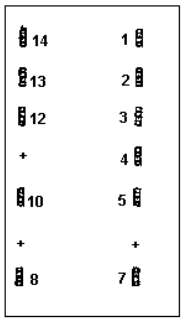
Notes: Q0 = the level of Q before the indicated input conditions were established.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



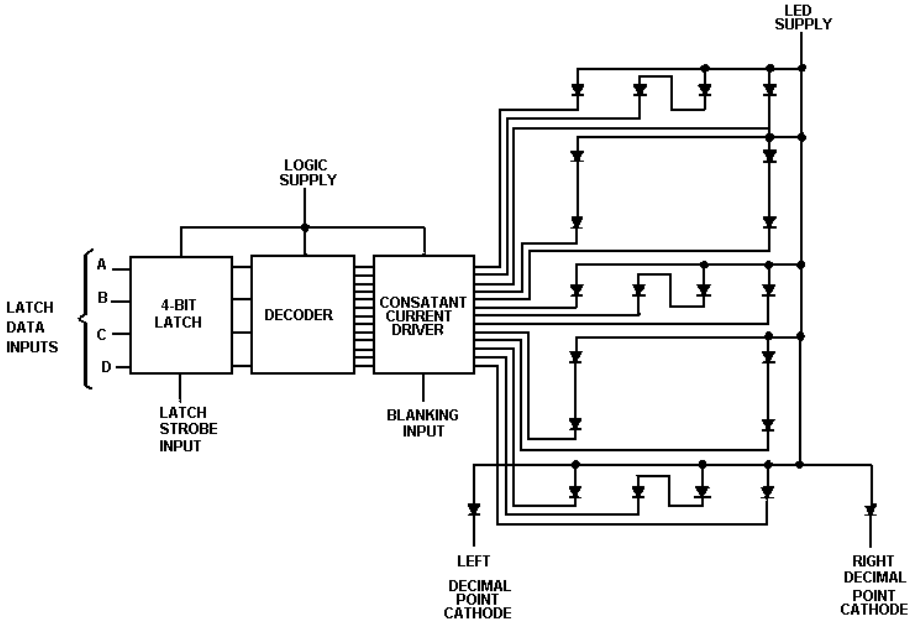
FLIP-FLOPS U17, U18 AND U25
SN74LS74AN



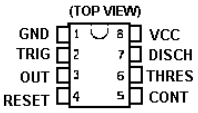
DISPLAY DRIVER 32 x 8 PROM U20
19J706247P2



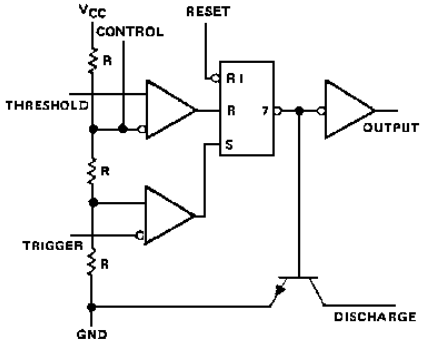
PIN 1 LED SUPPLY VOLTAGE
PIN 2 LATCH DATA INPUT B
PIN 3 LATCH DATA INPUT A
PIN 4 LEFT DECIMAL POINT CATHODE
PIN 5 LATCH SROBE INPUT
PIN 6 OMITTED
PIN 7 COMMON GROUND
PIN 8 BLANKING INPUT
PIN 9 OMITTED
PIN 10 RIGHT DECIMAL POINT CATHODE
PIN 11 OMITTED
PIN 12 LATCH DATA INPUT D
PIN 13 LATCH DATA INPUT C
PIN 14 LOGIC SUPPLY VOLTAGE, V_{CC}



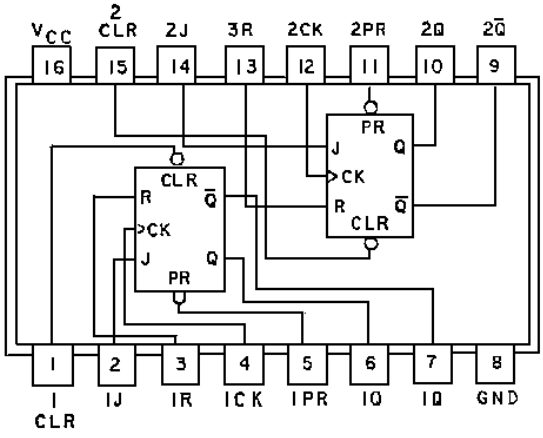
LED DISPLAY U21 AND U22
T1L311



functional block diagram

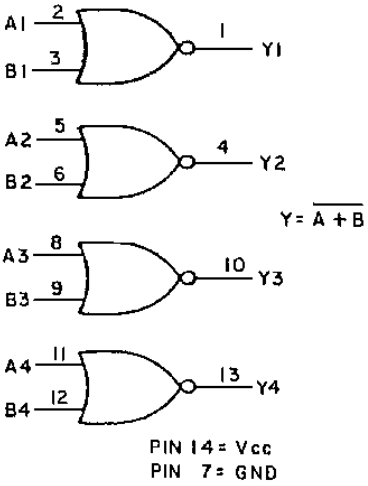


TIMER U23
ME55SN



COUNTERS U28, U29
74LS193

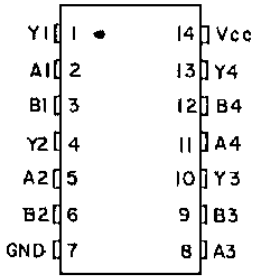
LOGIC DIAGRAM



$Y = \overline{A + B}$

PIN 14 = Vcc
PIN 7 = GND

PIN ASSIGNMENT

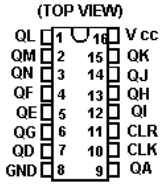


FUNCTION DIAGRAM

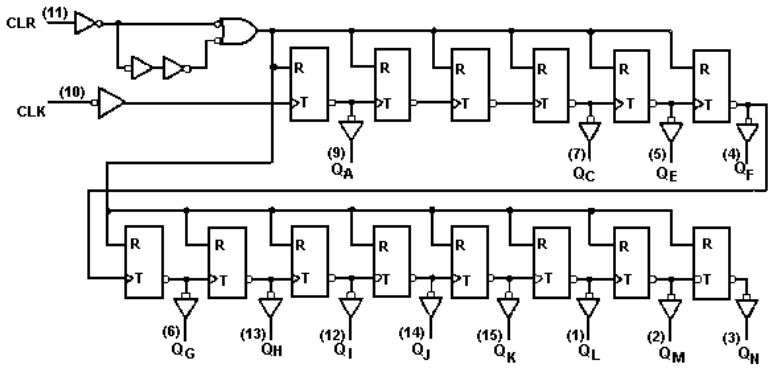
INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

NOR GATE U24, U30
SN74LS02N

(TOP VIEW)



logic diagram (positive logic)



COUNTER U26 AND U27
SN74HC4020N