MAINTENANCE MANUAL
GETC INTERFACE MODULE
19D902342G1 & G3

TABLE OF CONTENTS

	Page
SPECIFICATIONS	1
GENERAL DESCRIPTION	1
CIRCUIT AND FUNCTIONAL DESCRIPTION	1
CONNECTORS AND SYSTEM INTERFACE	1
CONTROL POINT SIGNAL FLOW	1
9.6Reference (J2-49)	1
11.0592 MHz Clock (J1A-8)	1
9.6CLKIN (J1A-17, 9.6CLKOUT (J2-42)	1
9.6DATAIN (J1A-17), 9.6OUT232 (J2-41)	1
150DATAIN (J1A-19), 150OUT232 (J2-36), 15OUTB232 (J2-43)	1
RXD - (J1C-22, RXD232 - (J2-29)	2
PTTOUT (J1C-29), PTTOUT232 (J2-19), PTTOUT + (J2-11), PTTOUT - (J2-12)	2
A/DOUT (J1C-28), A/DOUT232 (J2-23), A/DOUT + (J2-13), A/DOUT - (J2-14)	2
TRANSMIT SITE SIGNAL FLOW	2
PTTIN (J1A-29), PTTINPUT, PTTSEL, PTTIN232 - (J2-17), PTTOUT232 - (J2-19)	2
A/DIN (J1A-28), A/DINPUT, A/DSETL, A/DIN232 - (J2-18), A/DOUT232 - (J2-23)	2
RS-232 Level Clamping Levels (J2-20/22)	2
CLOCKTXD - (J1A-22), CLKTXD232 - (J2-31)	2
TXD - (J1C-24), TXD232 - (J2-33)	2
RTS - (J1A-25), RTS232 - (J2-25)	2
CTS - (J1C-25), CTS232 - (J2-27)	2
BYPASS CONTROL - (J2-9)	2
POWER DISTRIBUTION AND FILTERING	2
PHASE LOCKED 11.0592 MHz CLOCK	4
MAINTENANCE	5
CONNECTOR PIN DEFINITIONS	5
Table 1 - P1 Connector (GETC To GETC Interface Module)	5
Table 2 - P2 Connector Definition	6
Table 3 - Digital Clocks And Data Rate	7
Table 4 - Jumper Definition And Configuration	7
TEST AND SERVICE	7
OUTLINE DIAGRAM	8
SCHEMATIC DIAGRAM	9
PARTS LIST	11
PRODUCTION CHANGES	11
OUTLINE DIAGRAM	11
IC DATA	12

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SPECIFICATIONS*

GENERAL	
INPUT VOLTAGE	+5 Volts ±5% +12 Volts -12 Volts
CURRENT DRAIN (maximum)	
+5 Volts	150 mA.
+12 Volts	80 mA.
-12 Volts	20 mA.
TEMPERATURE	-30° to -60° C
DIGITAL DATA/TYPE	TTL & RS-232C
ANALOG/AUDIO TYPE	VOICE GRADE AUDIO CIRCUITS (EQUAL TO 3002)
DIMENSIONS	4.5" (L) X 4.0 (W)
Weight	10 Ounces

* These specifications are primarily for the use of the service technician. Refer to the appropriate Specification Sheet for the complete specifications.

GENERAL DESCRIPTION

The GETC (General Electric Trunking Card) interface module is used in the EDACS Simulcast System to provide signal level conversion, clock synchronization, bypass, and remote control functions for those signals whose source or destination is the GETC. Group 1 is used in MASTR II and IIe applications. Group 3 is used in MASTR III applications.

The GETC interface module is physically mounted in the GETC shelf assembly of the EDACS trunked radio system. The GETC interface module plugs into the GETC logic board at GETC connector J3. (This is the location where the 9600 baud modem option of the GETC shelf assembly normally mounts.)

The GETC Interface module buffers signals between the GETC logic board and the rest of the simulcast modules. The buffered signals include the 9600 Hz data clock (in and out), 9600 baud data (in and out), 150 baud data (in and out), modem handshaking lines, audio/digital path select line (in and out, push-to-talk line (in and out) and the A/D lines (in and out).

The GETC interface module uses the 9600 Hz reference clock generated on the data selector 2 module to phase lock the 11.0592 MHz clock that is used to drive the GETC logic board. This provides the stable and synchronized clock source for the system at the Control Point.

The GETC interface module can switch the tip and ring audio interface at the Transmit Site. An adjustment to match the audio level of the two paths is also provided. The GETC interface module is used in different/compatible modes at the Transmit and Control Point Sites.

CIRCUIT AND FUNCTIONAL DESCRIPTION

The GETC interface module provides signal, data, and clock level conversion (TTL to RS-232C and RS-232C to TTL), an alternate path for local control, data and clock lines (via the W0BYPASS line), and a GETC clock that is phase locked to the reference clock.

The GETC interface module converts RS-232C level signals from the cross connect panel of the simulcast system to TTL signals for the GETC logic board. It also converts TTL signals from the GETC logic board to RS-232C for the cross connect panel for intersite use.

The GETC interface module generates a synchronized 11.0592 MHz clock from a reference 9600 Hz clock. This is accomplished using a Phase-Locked Loop (PLL) and a voltage controlled oscillator with a divide-by N prescaler.

Three relays are used on the GETC interface module. One relay provides a contact closure based on the GETC PTT output. A second relay provides a contact closure based on the GETC A/D (audio and low speed data/high speed data control line) control line. The third relays switches audio lines TXTIP, TXRING, RXTIP, and RXRING to an alternate source.

Jumpers on the GETC interface module allow it to be configured for various modes of operation. The hardware on the GETC interface module is comprised of the following:

- Two quad four line drivers to buffer signals from the GETC logic board to the cross connect panel
- Two quad four line receivers to buffer signals from the cross connect panel to the GETC logic board
- Two peripheral drivers to buffer signals to the relays and push-to-talk to the GETC logic board
- Two reed relays to provide contact closure on push-to-talk and audio/digital control to the cross connect panel for E/M compatibility
- One four pole relay for an alternate audio line bypass path
- One quad two to one mux to select alternate paths for bypass control
- Two eight bit counters used for the PLL prescaler
- One D type flip flop used for the PLL
- One digital PLL/VCO
- One multivibrator for the 9600 baud tristate control
- One tristate driver

A block diagram of the GETC interface module is shown in Figure 1.

There are three connectors used to connect the GETC interface module to components of the Simulcast System, J1, J2, and J9. J1 provides the interface with the logic board. A description of the various signals, data and clocks used between the two modules is summarized in Table 3. J2 provides the interface with the cross connect panel of the Simulcast System. A description of the various signals, data, and clocks used between the GETC interface module and the cross connect panel is summarized in Table 4. J9 is used to connect a remote set of audio lines, TXTIP, TXRING, RXTIP, AND RXRING to (CBTXTIP, CBTXRING, CBRXTIP AND CBRXRING) through voice bypass relay K1. It also provides the interface for BYPASS control from J2-9 to control relay K1.

A series of 100 ohm and 10 ohm resistors are connected in series with the GETC interface board I/O lines to provide protection against surge currents that may occur.

CONTROL POINT SIGNAL FLOW

9.6Reference (J2-49)

A 9.6REF. clock, generated on digital selector #2 card, is distributed to the GETC interface board through the cross connect panel. This reference clock operates at 9600 Hz and is used by the GETC interface module to generate the 11.0592 MHz clock which is sent to the GETC to provide the clock used to synchronize the simulcast system.

11.0592MHz Clock (J1A-8)

The 11.0592MHz clock is generated on the GETC interface board by a phase locked loop oscillator referenced to the 9.6REF. clock for system stability. The 11.0592 MHz clock is then input to the GETC logic board. The corresponding clock on the GETC logic board is called MCLK.

9.6CLKIN (J1A-17), 9.6CLKOUT (J2-42)

The 9.6CLKIN is a 9600 Hz square wave output from the GETC. The clock is derived from the RF modem on the GETC. 9.6CLKIN is converted from TTL to RS-232C and sent to the cross connect panel, as 9.6CLKOUT.

9.6DATAIN (J1A-17), 9.6OUT232 (J2-41)

The 9.6DATAIN is a 9600 bps data stream output from the GETC. This data is derived from the RF modem, U4, on the GETC. 9.6DATAIN is converted from TTL to RS-232C and sent to the cross connect panel as 9.6OUT232.

150DATAIN (J1A-19), 150OUT232 (J2-36), 150OUTB232 (J2-43)

The 150DATAIN is a 150 bps data stream output from the GETC. This data is derived from a WALSH BIT generator on the GETC. 150DATAIN is converted from TTL to RS-232C and sent to the cross connect panel as 150DATAOUT232 and to the FSK modem module in the sync unit assembly at the Control Point.

RXD (J1C-22), RXD232 (J2-29)

RXD data is a 9600 bps data stream input to the GETC. This data is derived from the cross connect panel data line, RXD232. RXD232 is converted from RS-232C to TTL and sent to the GETC. RXD232 is generated from the digital voter, sent to the cross connect panel, and subsequently sent to GETC interface module. RXD232 is used only at the Control Point.

PTTOUT (J1C-29), PTTOUT232 (J2-19), PTTOUT + (J2-11), PTTOUT - (J2-12)

PTTOUT is derived from the GETC. This signal is output from the GETC. The microcomputer produces the delayed PTT output. PTTOUT is input to a peripheral relay driver which drives relay K2. K2 provides a contact closure and connects PTTOUT + to PTTOUT -. These two signals, PTTOUT + and PTTOUT - are sent to the cross connect panel at the Transmit Site and to the transmit control panel at the Control Point.

PTTOUT is also converted from TTL to RS-232C and sent to the cross connect panel at the Transmit Site as PTTOUT232. PTTOUT232 is looped back to jumper J6 for possible selection in the generation of PTTIN. Currently, PTTOUT232 is not used.

A/DOUT (J1C-28), A/DOUT232 (J2-23), A/DOUT + (J2-13), A/DOUT- (J2-14)

A/DOUT is output from the GETC to produce the modulation path control to select the audio and low speed data or the high speed data path. A/DOUT is converted from TTL to RS-232C and sent to the cross connect panel as A/DOUT232. A/DOUT232 is sent from the cross connect panel to the transmit control panel at the Control Point. It is also looped back to jumper J5 for possible selection in the generation of A/DIN. A/DOUT is also input to a peripheral relay driver which drives relay K3. Relay K3 provides a contact closure and connects A/DOUT + to A/DOUT-. These two signals, A/DOUT + and A/DOUT-, are sent to the cross connect panel. A/DOUT232 is used in applications where RS-232 levels are required and A/DOUT is used where contact closure is desired.

TRANSMIT SITE SIGNAL FLOW

PTTIN (J1A-29), PTTINPUT, PTTSEL, PTTIN232 (J2-17), PTTOUT232 (J2-19)

The signal, PTTIN, is an input to the GETC. This is the return signal corresponding to PTTOUT from the GETC. It is used to provide the delayed PTT control line to the transmitter of the EDACS station. This signal is derived from one of two sources. One is from the PTTINPUT signal from the cross connect panel. This TTL signal is received from the channel bank at the transmit site. The second, PTTSEL, is the looped back signal and is taken from the input of TTL to RS232 line driver U8A. The source selected is controlled by the state of the BYPASS control line at U4-1.

A/DIN (J1A-28), A/DINPUT, A/DSEL, A/DIN232 (J2-18), A/DOUT232 (J2-23)

The signal, A/DIN, is an input to the GETC at the Transmit Site. This is the return signal corresponding to A/DOUT from the control point GETC. It is used to provide the audio/digital path control line to the station GETC. This signal is derived from one of two sources. One source is the A/DINPUT, and is derived from the cross connect panel which originates from the channel bank at the transmit site. Jumper J12 allows selection of this source as either RS232 or contact closure to ground.

The second source is the TTL signal A/DSEL as the bypass A/D input control line. A/D SEL is originally derived from the GETC audio/digital path control line.

The source selected is controlled by the state of the BYPASS control line at U4-1. Jumper J13 is used to enable or disable the routing of the A/DIN control line to the GETC.

RS-232 Level Clamping Levels (J2-20/22)

There are two clamping (pull-up or pull-down) voltages which are generated by diodes D2 and D3 and resistors R13 and R14. A pull-up to +12 volts is formed by D2 and R13. this pull-up voltage is sent to the cross connect panel. A pull-down to -12 volts is formed by D3 and R14. This pulldown voltage also is sent to the cross connect panel.

CLOCKTXD (J1A-22), CLKTXD232 (J2-31)

The CLOCKTXD clock is a 9600 Hz square wave output from the GETC. This clock is generated on the GETC phone modem U19 and converted from TTL to RS-232C (CLKTXD232) and sent to the transmit site cross connect panel.

TXD (J1C-24), TXD232 (J2-33)

TXD data is a 9600 bps data stream output from the GETC. This data is derived from the phone modem U19 on the GETC. TXD is converted from TTL to RS-232C (TXD232) and sent to the cross connect panel.

RTS (J1A-25), RTS232 (J2-25)

The request To Send (RTS) signal is a handshake signal derived from an output signal on the GETC. This signal, RTS, is converted from TTL to RS-232C and sent to the transmit cross connect panel as RTS232. RTS232 is also passed by jumper J11 where it can be selected and routed to provide CTS232.

CTS (J1C-25), CTS232 (J2-27)

The signal, Clear To Send (CTS), is a handshake signal input to the GETC. This signal is derived from one of two sources. The first is the line CTS232 from the transmit cross connect panel. The second source is the signal RTS232 which is routed to CTS232 on the module via the jumper J11. Figure 7 shows the RTS/CTS select option. Optionally, CTS can be held on continuously by positioning jumper J11 between pins 1 & 2.

BYPASS CONTROL (J2-9)

The active low bypass control line, BYPASS, is used to re-route certain paths on the GETC interface module. It serves to re-route the 9600 bps data, the 150 bps data, the A/D control line, and the PTT control line, all of which are directed back to the GETC logic board. In addition, it turns off the DATARTN signals for the 9.6 K baud data line. There is also a voice bypass circuit which allows the audio to be interrupted and receive voice (RXTIP and RXRING) to be sent to the transmitter (TXTIP and TXRING) via relay K1. The bypass modes are described under Signal Flow. Figures 2 through 6 show the bypass modes of operation.

POWER DISTRIBUTION AND FILTERING

The dc voltages used by the GETC interface module are received from the GETC logic board. These supplies are +5 Vdc, +12 Vdc, -12 Vdc and GND (0 volts or logic ground). The supplies, +12 Vdc and -12 Vdc are used as pull-up and pull-down clamps for RS232C levels used by circuits of the simulcast system. These supplies also power the TTL to RS-232C level translators on the module. The + 5 Vdc is used to power the circuits on the GETC interface module. There are power bypass capacitors on the GETC interface module to filter any power noise transients or spikes from affecting circuit operation and module performance. These capacitors are 0.1 µF in value and are numbered C11 through C22.

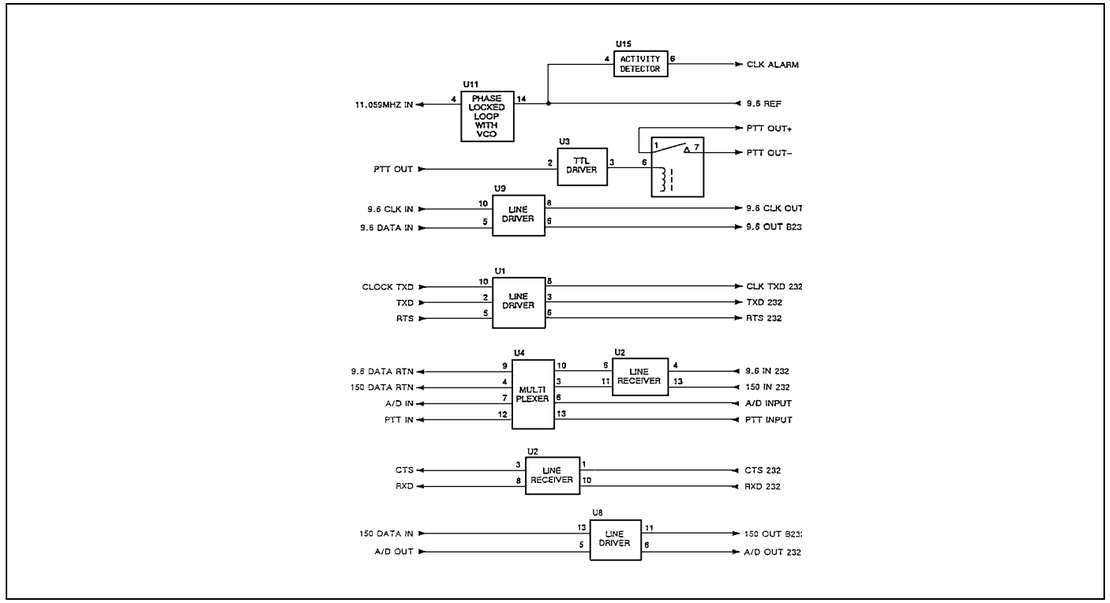


Figure 1 - GETC Interface Module Block Diagram

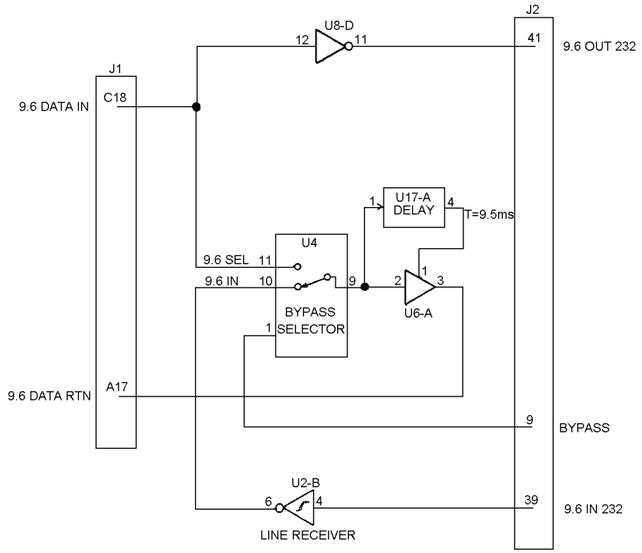


Figure 2 - 9.6K Bypass

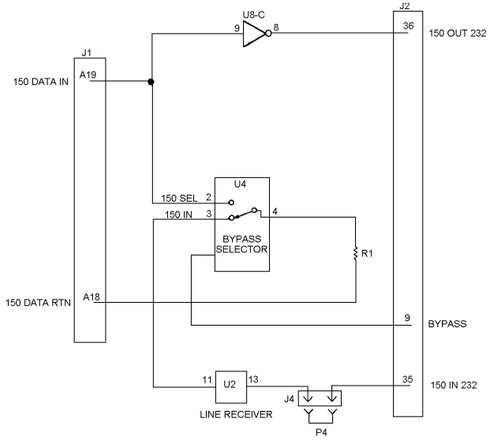


Figure 3 - 150 Data Bypass

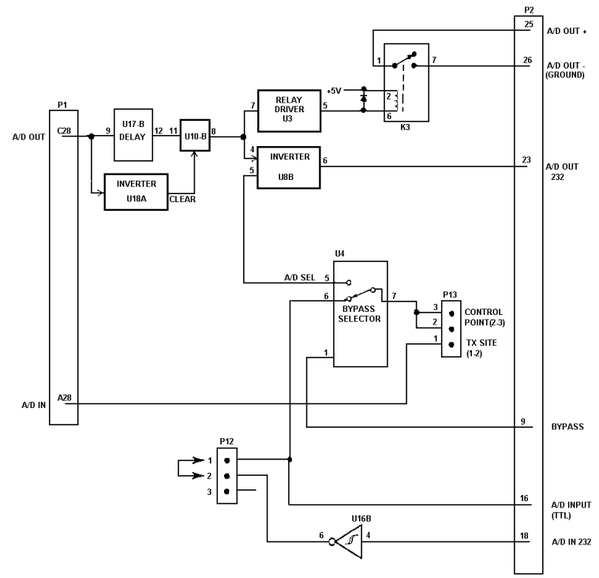


Figure 4 - A/D Input/Output Bypass

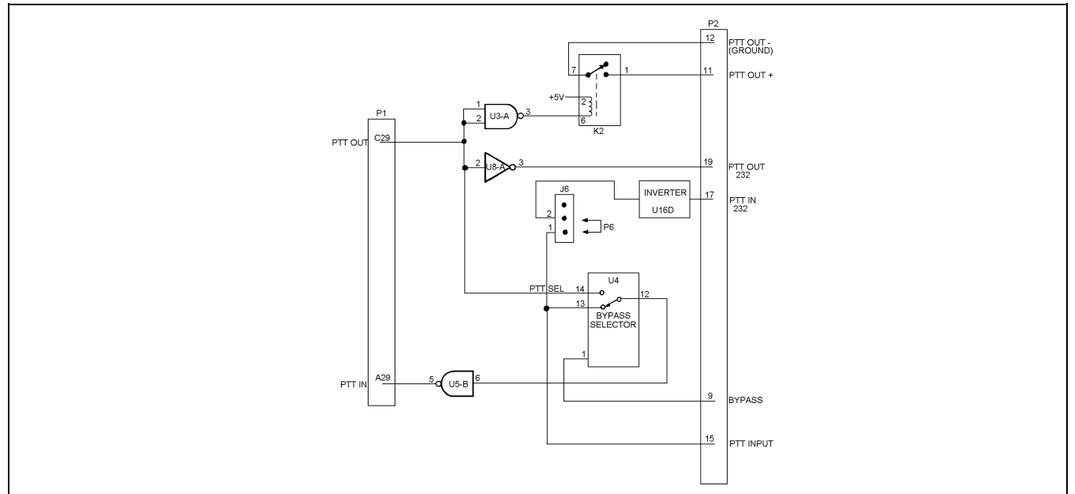


Figure 5 - PTT Input/Output Bypass

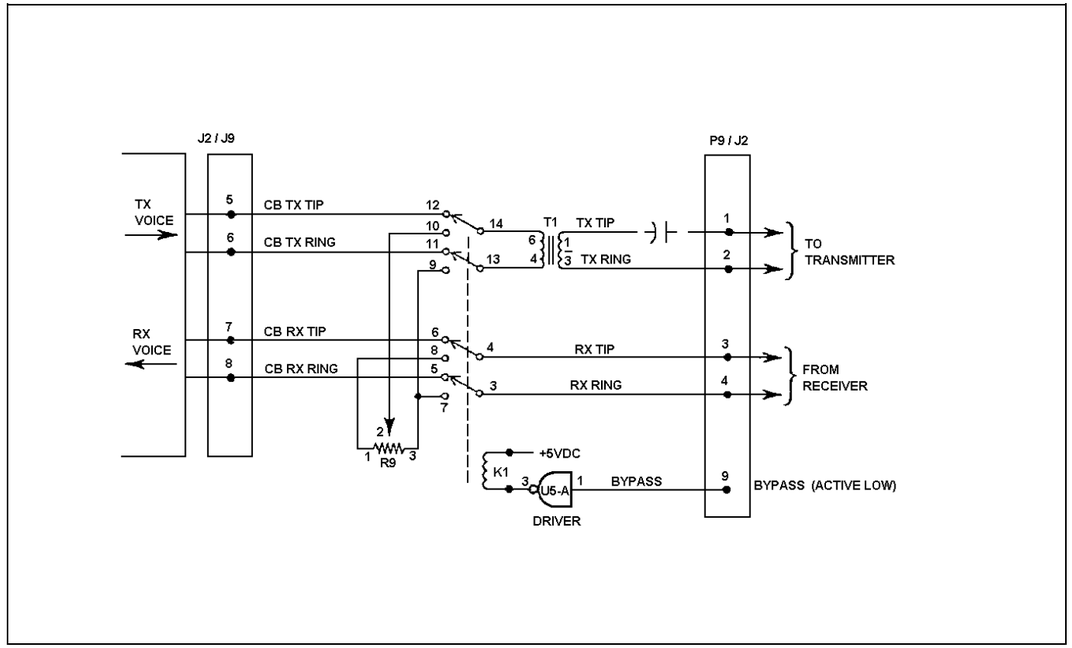


Figure 6 - Voice Bypass

PHASE LOCKED 11.0592 MHZ CLOCK

The GETC interface module generates an 11.0592 MHz clock from a reference 9600 Hz clock. This is accomplished by the digital Phase-Lock-Loop (PLL) and voltage controlled oscillator, U11. A divide by N prescaler consisting of 8-bit counters, U12 and U13, along with the synchronizing register, U10, perform the proper divide down of the 11-0592 MHz generated clock to compare against the reference 9600 Hz clock from the channel bank.

The reference clock, 9.6REF, is converted from RS-232C to TTL via the level translator U16. Resistor R5 and capacitor C7 provide filtering and delay of the reference TTL clock for input to the PLL and VCO, U11. The other compare input to the PLL and VCO is the output of synchronizing register, U10.

The PLL and VCO, U11, is a self contained digital phase-lock-loop and voltage controlled oscillator. Resistor R6 and capacitor C8 set up the center running frequency of the voltage controlled oscillator. Resistors R7, R8, R15, R16, R17 and capacitors C9 and C26 comprise the loop filter of the PLL which sets up the capture range (frequency lock range).

The generated 11.0592 MHz clock is input to 8-bit counters, U12 and U13, along with the synchronizing register, U10. The counters are asynchronously reloaded via the active low output of register U10.

In a free running mode of operation (with the inputted 9600 reference clock), components U12, U13, and U10 go through the following count sequence in order to provide the divide by ratio as shown in the following table:

COUNTER U12 (HEX COUNT)	COUNTER U13 (HEX COUNT)	REGISTER U10 (BIT VALUE)
FA	82	1
FA	83	1
FA	FF	1
FB	00	1
FB	FF	1
FC	00	1
FC	FF	1
FD	00	1
FD	FF	1
FE	00	1
FE	FF	1
FF	00	1
FF(FA)	01 (82)	0
FA	82	1
ETC.....(REPEATS)		

The total number of counts per cycle needed to produce the compare pulse (output of register U10) for input to the PLL is calculated below:

INITIAL	COUNT	- FA82
FINAL	COUNT BEFORE REPEAT	+ FF01
ADD	ONE	+ 1
TOTAL		480

The quantity 480 (HEX) is equal to 1152 (DEC). This value compares with the desired divide by number (where 11.0592 MHz divided by 1152 equals 9600 Hz).

Jumper J7 allows the selection of an external or internal source to generate the 11.0592 MHz clock for the GETC or to disable the GETC I/F clock so that the clock on the GETC can be used. Figure 8 shows the 11.0592 MHz clock selection scheme.

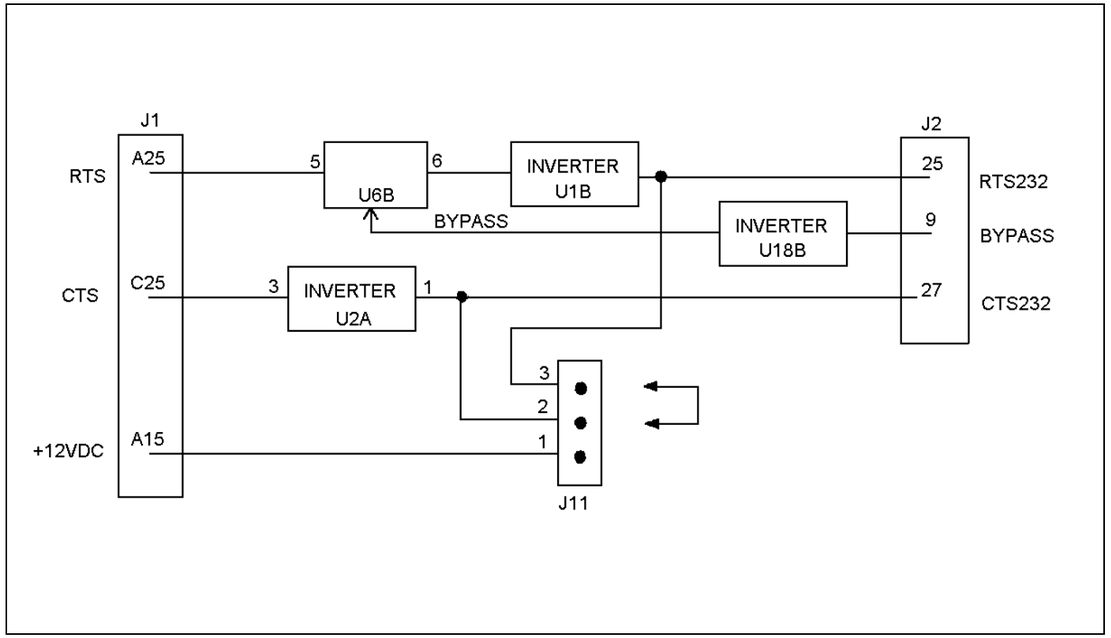


Figure 7 - RTS/CTS Select Option

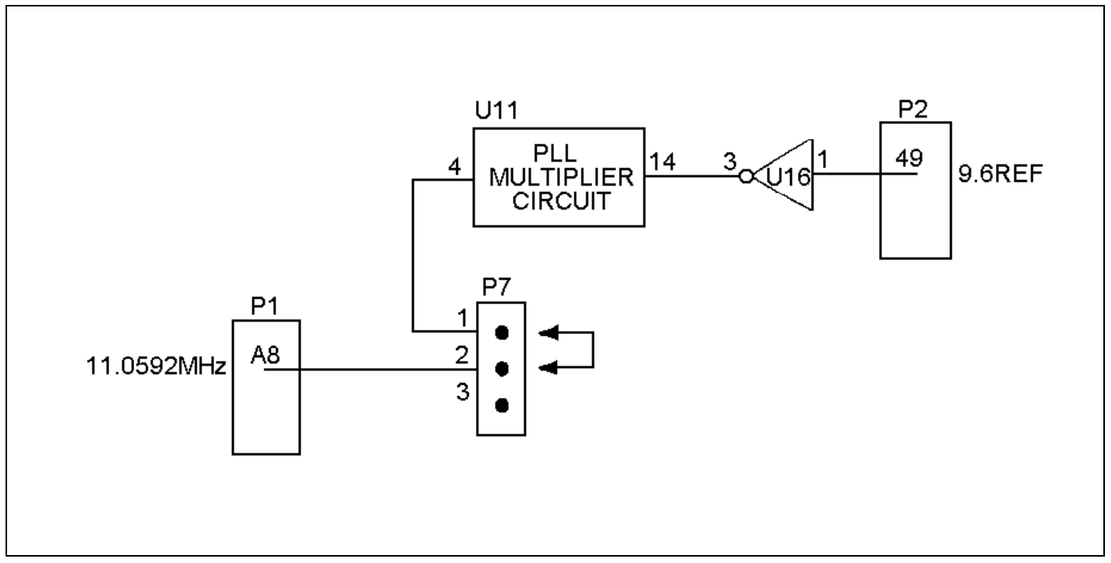


Figure 8 - 11.0592 MHz Clock Selection

MAINTENANCE

CONNECTOR PIN DEFINITIONS

Two connectors, P1 and P2, provide the interface connections for the GETC interface module: P1 interfaces the GETC with the GETC interface module and P2 provides the interface to the simulcast equipment. Tables 1 thru 3 identify each pin and provide such information as the signal name, whether or not it is an input or output signal, analog or digital, level - TTL, RS232, etc., and where used - Control Point or Transmit Site. Table 4 defines the jumpers used on the GETC. It also identifies the jumper, the shorting plug, the position required for proper operation at the Transmitter Site or the Control Point (they're not always the same) and also the signal present at each jumper location.

Table 1 - P1 Connector (GETC To GETC Interface Module)

CONNECTOR PIN	SIGNAL NAME	INPUT/ OUTPUT	ANALOG/ DIGITAL	LEVEL DIGITAL DC-VOLT AC-VRMS	CONTROL/ TS-SITE
P1-C3	GND	I/O	D	0 V	C/T
P1-A5	GND	I/O	D	0 V	C/T
P1-A8	11.0592MHZIN	O	D	TTL	C/T
P1-C8	GND	I/O	D	0 V	C/T
P1-A10	GND	I/O	D	0 V	C/T
P1-A12	-12 V	O			C/T
P1-A15	+12 V	O			C/T
P1-C16	9.6CLKIN		D	TTL	C/T
P1-A17	9.6DATARTN	O	D	TRI-STATE	C/T
P1-A18	150DATARTN	O	D	TTL	C/T
P1-C18	9.6DATAIN	I	D	TTL	C/T
P1-A19	150DATAIN	I	D	TTL	C/T
P1-C19	+5	I	D	5 V	C/T
P1-A22	CLKTXD	I	D	TTL	C/T
P1-C22	RXD	O	D	TTL	C/T
P1-C24	TXD	I	D	TTL	C/T
P1-A25	RTS	I	D	TTL	C/T
P1-C25	CTS	O	D	TTL	C/T
P1-A28	A/DIN	O	D	TTL	C/T
P1-C28	A/DOUT	I	D	TTL	C/T
P1-A29	PTTIN	O	D	TTL	C/T
P1-C29	PTTOUT	I	D	TTL	C/T

Table 2 - P2 Connector Definition

CONNECTOR PIN	SIGNAL NAME	INPUT/ OUTPUT	ANALOG/ DIGITAL	LEVE DIGITAL DC-VOLT AC-VRMS	CONTROL/ TX SITE
P2-1	TXTIP	O	A	0 dBm	
P2-2	TXRING	OP	A	0 dBm	
P2-3	RXTIP	I	A	-10 dBm	
P2-4	RXRING	I	A	-10 dBm	
P2-5	CBTXTIP	I	A	0 dBm	T
P2-6	CBTXRING	I	A	0 dBm	T
P2-7	CBRXTIP	O	A	-10 dBm	T
P2-8	CBRXRING	O	A	-10 dBm	T
P2-9	BYPASS	I	A	0, FLOAT	C/T
P2-10	GND	I/O	D	0 V	C/T
P2-11	PTTOUT +	O	D	0, FLOAT	C
P2-12	PTTOUT -	O	D	0 V	C
P2-13	A/DOUT +	O	D	0, FLOAT	
P2-14	A/DOUT -	O	D	0 V	
P2-15	PTTINPUT	I	D	TTL	T
P2-16	A/DINPUT	I	D	TTL	
P2-17	PTTIN232	I	D	RS-232C	
P2-18	A/DIN232	I	D	RS-232C	T
P2-19	PTTOUT232	O		RS-232C	
P2-20	+12 V	O	D	12 V	C
P2-21					
P2-22	-12 V	O	D	-12 V	
P2-23	A/DOUT232	O	D	RS-232C	C
P2-24	GND	I/O	D	0 V	C/T
P2-25	RTS232	O		RS-232C	

Table 2 - P2 Connector Definition (cont'd)

CONNECTOR PIN	SIGNAL NAME	INPUT/ OUTPUT	ANALOG/ DIGITAL	LEVE DIGITAL DC-VOLT AC-VRMS	CONTROL/ TX SITE
P2-26	GND	I/O	D	0 V	C/T
P2-27	CTS232	I		RS-232C	
P2-28	GND	I/O	D	0 V	
P2-29	RXD232	I		RS-232C	C
P2-30	GND	I/O	D	0 V	C/T
P2-31	CLKTX232	O		RS-232C	T
P2-32	GND	I/O	D	0 V	C/T
P2-33	TXD232	O		RS-232C	T
P2-34	GND	I/O	D	0 V	C/T
P2-35	150IN232	I		RS-232C	T
P2-36	150OUT232	O		RS-232C	C
P2-37	(Not used)				
P2-38	GND	I/O	D	0 V	C/T
P2-39	9.6IN232	I		RS-232C	T
P2-40	GND	I/O	D	0 V	C/T
P2-41	9.6OUT232	O		RS-232C	C
P2-42	9.6CLKOUT	O		RS-232C	C
P2-43	9.6CLKOUT			RS-232C	C
P2-44	GND	I/O	D	0 V	C/T
P2-45	(Not used)				
P2-46	GND	I/O	D	0 V	C/T
P2-47	(Not used)				
P2-48	(Not used)				
P2-49	9.6REF	I	D	RS-232C	C/T
P2-50	GND	I/O	D	0 V	C/T

Table 3 - Digital Clocks And Data Rate

CONNECTOR PIN	SIGNAL PIIN	CLOCK/DATA AND LEVEL		RATE Hz (C) BPS (D)
P1C-16	9.6CLKIN	C	TTL	9600
P1A-17	9.6DATARTN	D	TTL	9600
P1A-18	150DATARTN	D	TTL	150
P1-C18	9.6DATAIN	D	TTL	9600
P1A-19	150DATAIN	D	TTL	150
P1A-22	CLKTXD	C	TTL	9600
P2-29	RXD232	D	RS-232C	9600
P2-31	CLKTXD232	C	RS-232C	9600
P2-33	TXD232	D	RS-232C	9600
P2-35	150IN232	D	RS-232C	150
P2-36	150OUT232	D	RS-232C	150
P2-39	9.6IN232	D	RS-232C	9600
P2-41	9.6OUT232	D	RS-232C	9600
P2-42	9.6CLKOUT	D	RS-232C	9600
P2-43	9.6CLKOUT	D	RS-232C	9600
P2-49	9.6REF	C	RS-232C	9600

Table 4 - Jumper Definition And Configuration

JUMPER	SHORTING PLUG	POSITION	DESCRIPTION	CONTROL/TX SITE C	T
J3	P3	1 & 2 2 & 3	GETC 9600 DATA BYPASS REMOTE 9600 DATA BYPASS	1-2	1-2
J4	P4	1 & 2 2 & 3	GETC 150 DATA BYPASS REMOTE 150 DATA BYPASS	1-2	1-2
J5	P5	1 & 2 2 & 3	A/D CONTROL DIS BYPASS A/D CONTROL EN BYPASS	2-3	2-3
J6	P6	1 & 2 2 & 3	PTT CONTROL RS-232 PTT CONTROL TTL	2-3	2-3
J7	P7	1 & 2 2 & 3	EXT REF CLOCK INT REF CLOCK	1-2	1-2
J8	P8	1 & 2 2 & 3	T1 LINE DC COUPLING T1 LINE AC COUPLING	1-2	1-2
J11	P11	1 & 2 2 & 3 OPEN	CTS RETURNED EXT. CTS ENABLED VIA RTS EXTERNAL CTS-232	2-3	2-3
J12	P12	1 & 2 2 & 3	A/D RS-232 CONTROL A/D TTL CONTROL	2-3	2-3
J13	P13	1 & 2 2 & 3	A/D EN FOR CONTROL SITE A/D DIS FOR REMOTE SITE	1-2	2-3

The following adjustments/connections are required when installing the GETC interface module in an operational simulcast system:

A. Install jumpers per system requirements.

B. Adjust resistor R9 at the transmit site to set deviation (3 kHz) in the voice bypass mode.

TEST AND SERVICE

The following equipment is necessary to test the GETC interface module:

1. Tektronix 2430A Digital Storage Scope or equivalent
2. HP 8116 Pulse/function Generator or equivalent
3. Triplett model 630-PL Type 5 or equivalent
4. Test Cables as required

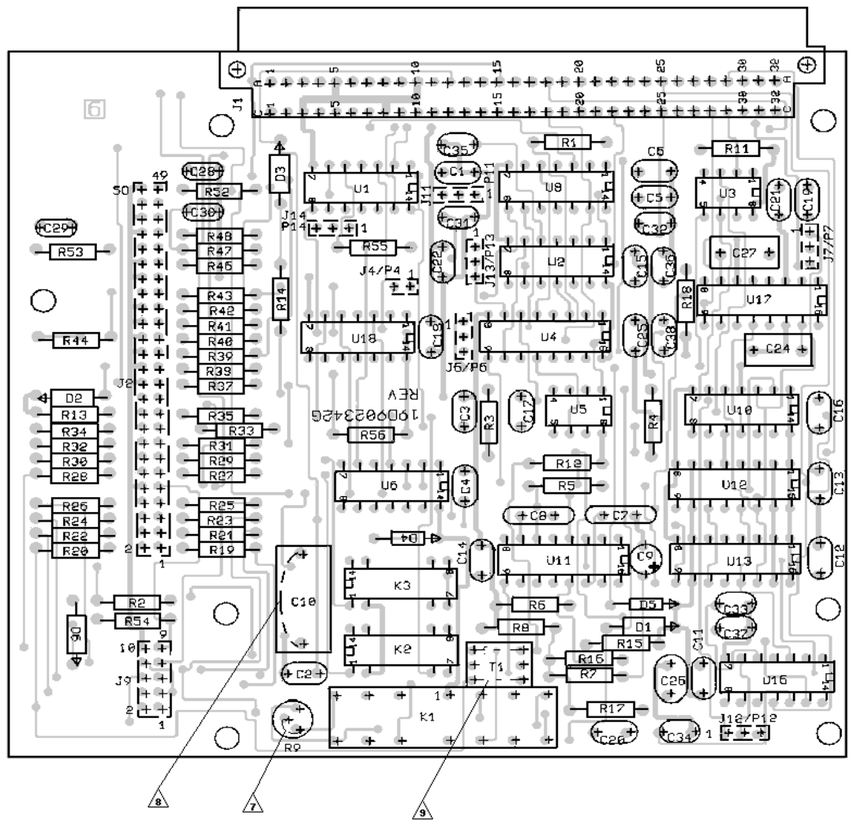
The following steps are necessary to test the GETC interface module as part of the Simulcast System.

1. Configure the jumpers on the GETC interface module for the desired modes of operation.
2. Install the GETC interface module in the GETC shelf assembly of the Simulcast System.
3. Verify that the +5, +12, and -12 Vdc source voltages on the GETC interface module are within the tolerances specified.
4. Verify correct operation of the PLL and VCO, if the 9.6 REF channel bank clock is used. Verify the 11.0592 MHz external clock, if used.
5. Verify the presence of 9.6CLKIN and 9.6DATAIN from the GETC.
6. Verify the presence of 150DATAIN from the GETC.
7. Verify the clock, CLOCKTXD, from the GETC.
8. If the modem control lines, TXD, CTS, and RTS are used, verify the presence of activity on these lines.
9. To check low speed data and high speed data control lines, verify activity on A/DOUT and contact closure to ground on A/DOUT +.
10. To check transmit control functions, verify activity on PTTOUT and contact closure to ground on PTTOUT +.
11. To check high speed data return from the channel bank, verify the presence of 9600 bps data on 9.6 RTN.
12. To check low speed data return from the channel bank, verify the presence of 150 bps data on 150DATARTN.
13. To check the A/D control line from the channel bank, verify activity on A/DIN.

14 To check PTT control line from the channel bank, verify activity on PTTIN.

15. To check voice bypass, verify voice loopback on the T1 lines and away from the channel bank lines.
16. To check remote bypass, verify that PTTIN, A/DIN, 150DATARTN, and 9.6DATARTN are generated from one of the loopback (or bypass) modes as configured by the jumpers.

COMPONENT SIDE



(19D902341, Rev. 6A)

19D902342G3

7 WIRE INSTALLED FROM P-1 TO P-2 IN PLACE OF R9.

8 WIRE INSTALLED IN PLACE OF C10.

9 TWO WIRES INSTALLED IN PLACE OF T1.
ONE FROM T1-1 TO T1-6
ONE FROM T1-3 TO T1-4.

CAUTION
OBSERVE PRECAUTIONS FOR HANDLING
ELECTROSTATIC SENSITIVE DEVICES

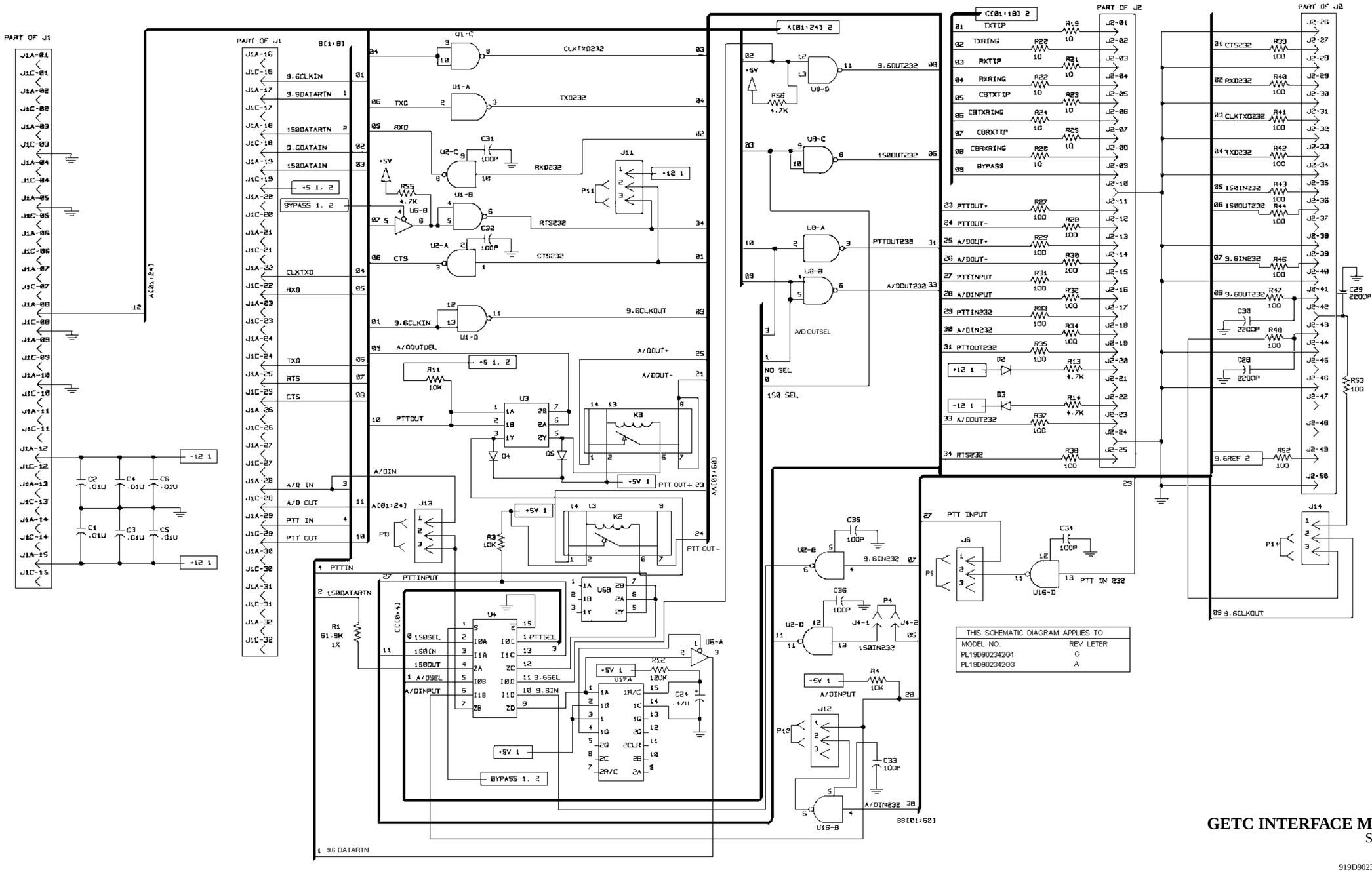
GETC INTERFACE MODULE

19D902342, Sh. 1, Rev. 11)

JUMPER DEFINITION AND SETUP

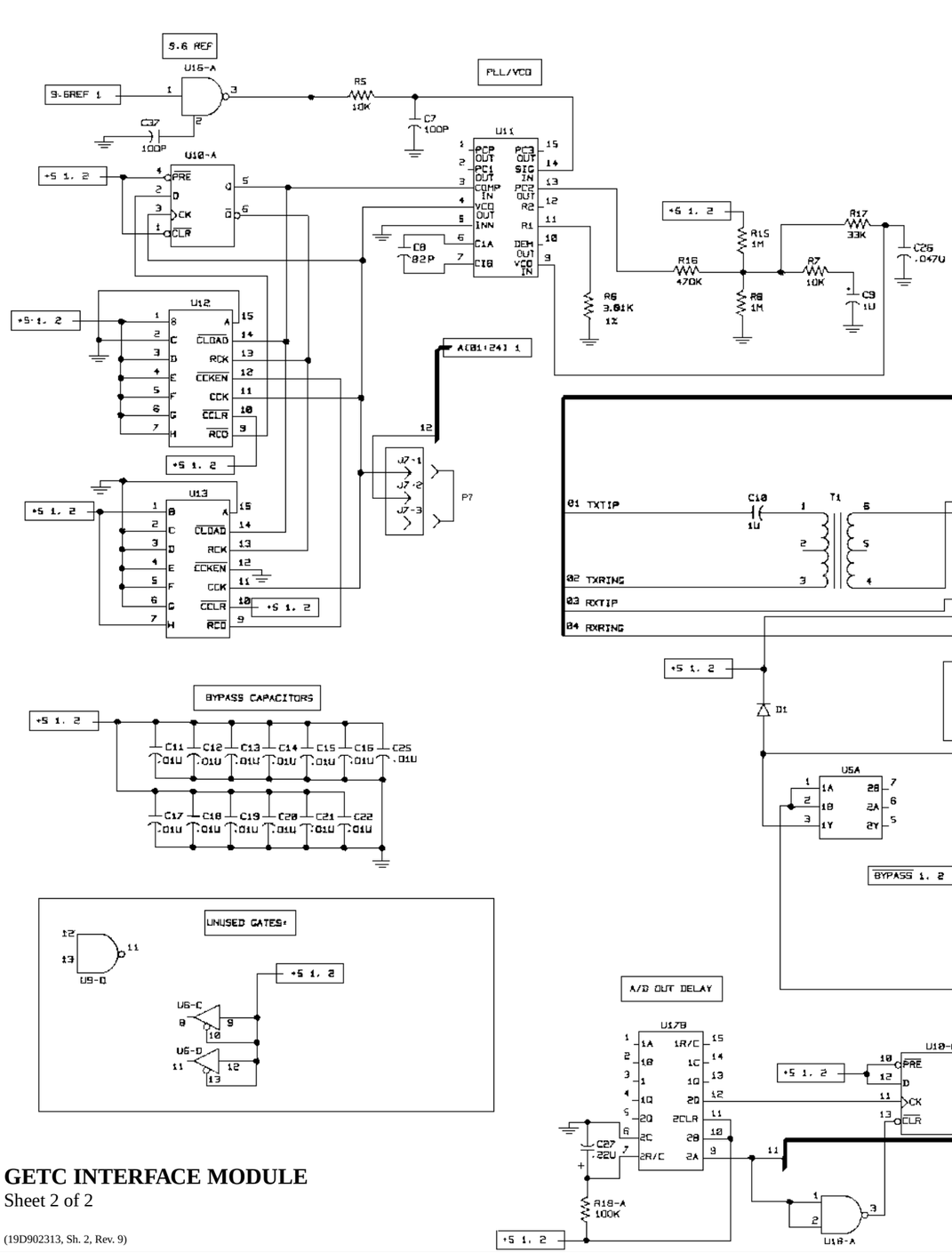
JUMPER DEFINITION AND CONFIGURATION TABLE						
JUMPER	SHORTING PLUG	POSITION	DESCRIPTION	CONTROL/ TRANSMITTER SITE		GP1
				T	C	
J6	P6	1 & 2 2 & 3	PTT CONTROL RS-232 PTT CONTROL TTL	2-3	2-3	2-3
J7	P7	1 & 2 2 & 3	EXT REF CLOCK INT REF CLOCK	1-2	1-2	1-2
J11	P11	1 & 2 2 & 3	CTS RETURNED EXT. CTS ENABLED VIA RTS	2-3	2-3	2-3
J12	P12	1 & 2 2 & 3	A/D RS-232 CONTROL A/D TTL CONTROL	2-3	2-3	2-3
J13	P13	1 & 2 2 & 3	A/D EN A/D DIS	1-2	2-3	1-2
J14	P14	1 & 2 2 & 3	PASLO/PELO OTHER	2-3	2-3	2-3

NOTE: FOR P14: J14,P14 JUMPER SHOULD BE POSITIONED BETWEEN PIN 1 & 2 IF MODULE IS USED TO REPLACE A 501-63177 MODULE - OTHERWISE JUMPER BETWEEN PINS 2 & 3.



GETC INTERFACE MODULE
Sheet 1 of 2

919D902313, Sh. 1, Rev. 8)



TEST

JUMPER DEFINITION AND SETUP

JUMPER DEFINITION AND CONFIGURATION TABLE

JUMPER	SHORTING PLUG	POSITION	DESCRIPTION	CONTROLL/TRANSMITTER SITE		GP1
				T	C	
J6	P6	1&2 2&3	PTT RS232 CONTROL PTT TTL CONTROL	2-3	2-3	2-3
J11	P11	OPEN 1&2 2&3	CTS RET FROM EXT MODEM CTS ENABLED CTS ENABLED VIA RTS	2-3	2-3	2-3
J12	P12	1&2 2&3	A/D RS232 CONTROL A/D TTL CONTROL	2-3	2-3	2-3
J13	P13	1&2 2&3	A/D EN A/D DIS	1-2	2-3	1-2
J14	P14	1&2 2&3	PASCO/PECO CLOCK PINOUT OTHER	2-3	2-3	2-3
J7	P7	1&2 2&3	EXT REF INT REF	1-2	1-2	1-2
J4	P4	1&2 OFF	GETC 150 DATA TEST 150 DATA	1-2	1-2	1-2

POWER AND GROUND CONNECTIONS

DEVICE	GND PIN NO.	+5V PIN NO.	+12V PIN NO.	-12V PIN NO.
U1.U8	7		14	1
U2	7	14		
U3.U5	4	8		
U4	8	16		
U6	7	14		
U10	7	14		
U11	8	16		
U12.U13	8	16		
U16	7	14		
U17	8	16		
U18	7	14		

NOTES:

1. TO SELECT 11.0592 MHZ SOURCE, JUMPER P7-1 TO P7-2.
2. CONNECTOR P9 IS USED FOR BYPASS OPERATION.
3. CLEAR-TO-SEND (CTS) IS SELECTED BY JUMPERS ON P11. FOR A CONSTANT CTS HI, JUMPER P11-1 TO P11-2. FOR A CTS HI WHEN RTS IS HI, JUMPER P11-2 TO P11-3. OMIT P11 TO CTS RETURN FROM MODEM.

GETC INTERFACE MODULE

Sheet 2 of 2

(19D902313, Sh. 2, Rev. 9)

GETC Interface Module 19D902342G1 & G3

SYMBOL	PART NUMBER	DESCRIPTION
		- - - - - - - - - -CAPACITORS - - - - - - - - -
C1 thru C6	T644ACP310K	Capacitor, polyester: .01µF ±10%, 50 VDCW.
C7	19A700235P25	Capacitor, ceramic: 100 pF ±5%, 50 VDCW.
*C8	19A116288P11	Capacitor, ceramic: 82 pF ±5%, 50 VDCW.
C9	19A701534P4	Capacitor, tantalum: 1 µF ±20%, 35 VDCW.
C10	19A700004P8	Capacitor, metalized polyester: 1 µF±10%, 63 VDCW. (G1 only).
C11	T644ACP310K	Capacitor, polyester: .01µF ±10%, 50 VDCW.
C24	19A700004P6	Capacitor, metalized polyester: 0.47 µF±10%, 63 VDCW.
C25	T644ACP310K	Capacitor, polyester: .01 µF ±10%, 50 VDCW.
C26	19A702250P111	Capacitor, polyester: .047µ F ±10%, 50 VDCW.
C27	19A700004P6	Capacitor, metalized polyester: 0.47 µF±10%, 63 VDCW.
C28	T644ACP222K	Capacitor, polyester: .0022 µ F ±10%, 50 VDCW.
C31	19A700233P1	Capacitor, ceramic: 100 pF ±20%, 50 VDCW.
C38	T644ACP310K	Capacitor, polyester: .01 µF ±10%, 50 VDCW.
		- - - - - - - - - - - - - DIODES - - - - - - - - - - - - -
D1 thru D3	T324ADP1041	Rectifier, silicon: sim to 1N4004.
D4 and D5	19A700028P1	Rectifier, silicon: 75 mA, 75 PIV; sim to 1N148.
D6	19A700047P3	Rectifier, silicon: , Schottky barrier; sim to 1N6263.
		- - - - - - - - - - - - -JACKS - - - - - - - - - - - - -
J1		Connector: 64 pin, Panduit 100-964-023.
J2		Connector: Amp 2-103240-5.
J4	19A704852P1	Connector: 2 Pin male header.
J6 and J7	19A704852P2	Connector: 3 Pin male header
J9		103240-5Amp.
J11 thru J14	19A704852P2	
		- - - - - - - - - - - -RELAYS - - - - - - - - - - - - -
K1		4PDT: Aromat DS4E-M-DCV.
K2 and K3	19B235939P1	Reed.
		- - - - - - - - - - - - - PLUGS - - - - - - - - - - - - - - -
P6 and P7 and P11 thru P14	19A702104P2	Connector: Shorting Jumper, Gold plated. (Housing Color: White).

*COMPONENTS, ADDED, DELETED OR CHANGED BY PRODUCTION CHANGES

SYMBOL	PART NUMBER	DESCRIPTION
		- - - - - - - - - - - - -RESISTORS - - - - - - - - - - - -
R1	19A701250P377	Resistor, metal film, 23.7K ohms ±1%. 1/4 w.
R2	H212CRP247C	Resistor, deposited carbon, 4.7K ohms ±5%. 1/4 w.
R3 thru R5	H212CRP310C	Resistor, deposited carbon, 10K ohms ±5%. 1/4 w.
*R6	19A701250P247	Resistor, metal film, 3.01K ohms ±1%. 1/4 w.
R7	H212CRP310C	Resistor, deposited carbon, 10K ohms ±5%. 1/4 w.
R8	H212CRP510C	Resistor, deposited carbon, 1 M. ohms ±5% 1/4 w.
R9	19A700016P1	Resistor, variable: 10 - 1K ohms. (G1 only).
R11	H212CRP310C	Resistor, deposited carbon, 10K ohms ±5%. 1/4 w.
R12	H212CRP412C	Resistor, deposited carbon, 0.12 M ohms ±5%. 1/4 w.
R13 and R14	H212CRP247C	Resistor, deposited carbon, 4.7K ohms ±5%. 1/4 w.
R15	H212CRP510C	Resistor, deposited carbon, 1 M. ohms ±5% 1/4 w.
R16	H212CRP447C	Resistor, deposited carbon, 470K ohms ±5%. 1/4 w.
R17	H212CRP333C	Resistor, deposited carbon, 33K ohms ±5%. 1/4 w.
R18	H212CRP410C	Resistor, deposited carbon, 100K ohms ±5%. 1/4 w.
R19 thru R35 and R37 thru R44 and R46 thru R48	H212CRP010C	Resistor, deposited carbon, 10 ohms ±5%. 1/4 w.
R52 and R53	H212CRP110C	Resistor, deposited carbon, 100 ohms ±5%. 1/4 w.
R54	H212CRP047C	Resistor, deposited carbon, 47 ohms ±5%. 1/4 w.
R55	H212CRP247C	Resistor, deposited carbon, 4.7K ohms ±5%. 1/4 w.
R56	H212CRP347C	Resistor, deposited carbon, 47K ohms ±5%. 1/4 w.
		- - - - - - - - -TRANSFORMERS - - - - - - - - - -
T1		Microtran: PM34-M. (G1 only).
		- - - - - - - - INTEGRATED CIRCUITS - - - - - - - - -
U1	19A116704P1	Digital: Quad Line Driver; sim to 1488.
U2	19A116704P2	Digital: Quad Line Receiver; sim to 1489.
U3		Digital: Dual Peripheral Driver, 75451T1.
U4	19A700037P365	Digital Quad 2-line to 1 line Data Selector.
U5		Digital: Dual Peripheral Driver, 75451T1.
U6		Digital: Quad Tri-state buffer, 74HCT125RCA.
U8	19A116704P1	Digital: Quad Line Driver; sim to 1488.
U10	19A700037P335	Digital: Dual Data FF; sim to 74LS74A.
U11		Phase Lock Loop: 74HCT4046RCA.
U12 and U13		Digital: 8-bit binary counter; sim to 74LS592T1.
U16	19A116704P2	Digital: Quad Line Receiver; sim to 1489.
U17	19A700037P354	Digital: Dual retriggerable monostable; sim to 74LS123.
U18	19A700037P301	Digital: Quad 2-input NAND gate; sim to 74LS00.

PRODUCTION CHANGES

Changes in the equipment to improve performance or to simplify circuits are identified by a "Revision Letter" which is stamped after the model number of the unit. The revision stamped on the unit includes all previous revisions. Refer to the Parts List for the description of parts affected by these revisions.

REV. A - **GETC INTERFACE MODULE 19D902342G1**
Incorporated into initial shipment.

REV. B - Incorporated into initial shipment.

REV. C - To improve noise immunity and remove unused jumpers. Added C28-C30, R55, R56, U18. Deleted J3-J5, J8, P3-P5, P8, R36, R49-R51 , U7, and changed K2, K3, R19-R26. Old part numbers were:

J3-J5, J8 - 19A704852P2, Connector: 3-pin male header.
K2, K3 - 19B209716P1, Relay reed.
P3-P5, P8 - 19A702104P2, Connector: Shorting jumper, gold plated (Housing color: White).
R19-R26, R36, R49-R51 - H212CRP110C, Deposited carbon: 100K ohms ±5%, 1/4 w.
U7 - 19D116704P2, Digital: Quad Line driver; sim to 1489.

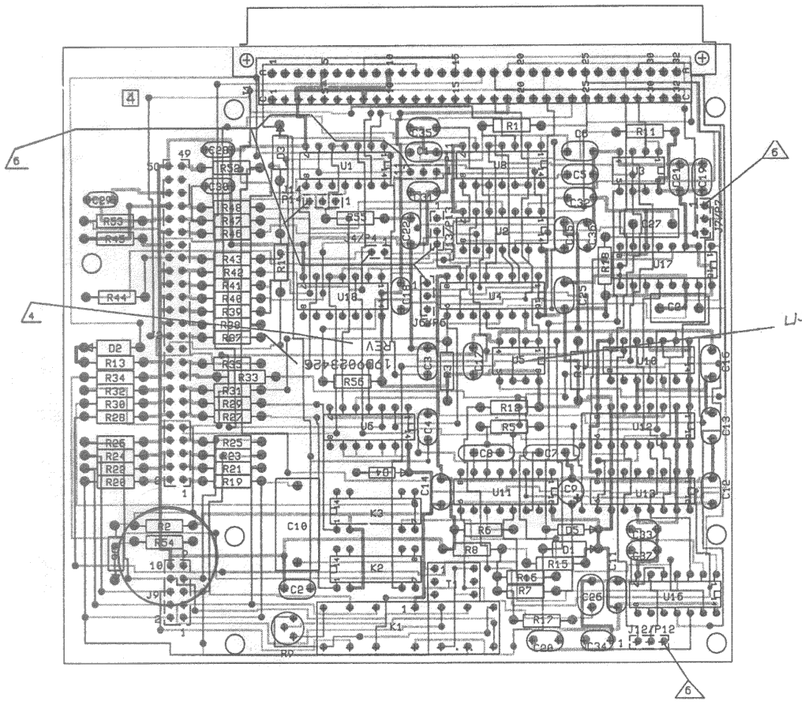
REV. D - To correct documentation. Added C35-C37, J4 and connection between U4-11 and U8-12. Deleted U9 and changed C24. Old part number was:

C24 - 19A700004P4, Capacitor, metalized polyester: 0.22 µF 10%, 63 VDCW.
U9 - 19A116704P1, Digital: Quad Line Driver; sim to 1488.

REV. E - To correct wiring shown on PWB. To improve operation of bypass function and transient protection. Refer to Outline Diagram below and modify PWB as directed. R45 is deleted.

1. Cut run at junction of R2, D6 (solder side to J2-9).
2. Cut run from J2-9 to feed thru on solder side (was going to U5-1).
3. Install white wire from J2-9 feedthrough to R54. (J9-9 on solder side).
4. Install white wire from U5-1 feedthrough to junction of R2, D6 on solder side.

OUTLINE DIAGRAM



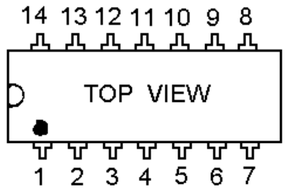
REV. F - To improve noise immunity on bypass line. Changed D6 and R54. Added C38 on solder side between the anode of D6 and ground (J9-10). Old part numbers were:

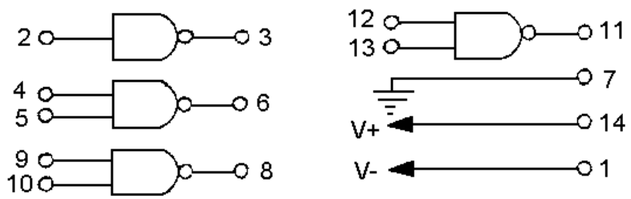
D6 - 19A700028P1: 75 mA, 75 PIV; sim to 1N4148.
R54 - H212CRP110C: Resistor, deposited carbon: 100 ohms ±5% 1/4 w.

REV. G - To improve start up stability. C8 was 220 pF (19A700235P29) and R6 was 1.47k ohms (19A701250P217).

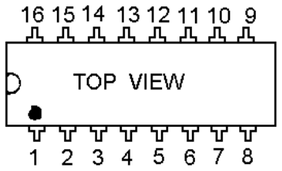
REV. A - **GETC INTERFACE MODULE 19D902342G3**
To improve start up stability. C8 was 220 pF (19A700235P29) and R6 was 1.47k ohms (19A701250P217).

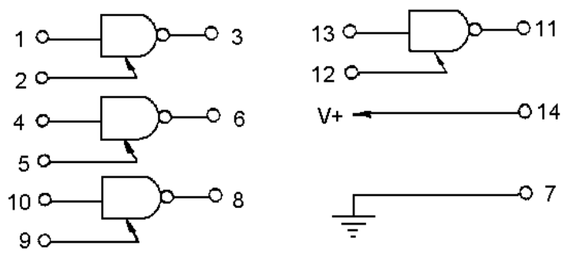
QUAD LINE DRIVER
19A116704P1



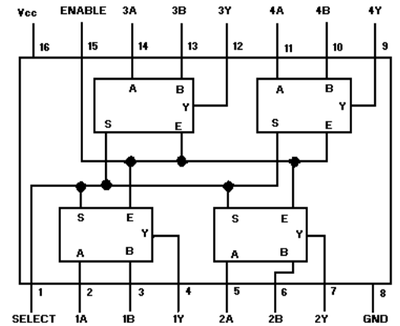


QUAD LINE RECEIVER
19A116704P2





U4 QUAD 2-LINE TO 1-LINE DATA SELECTOR
19A700037P365



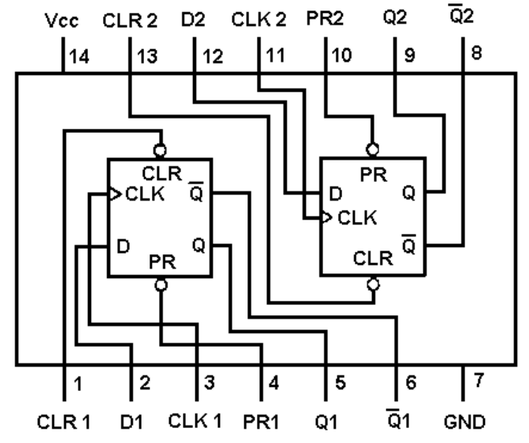
Truth Table

ENABLE	SELECT	A	B	OUTPUT Y
1	X	X	X	0
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1

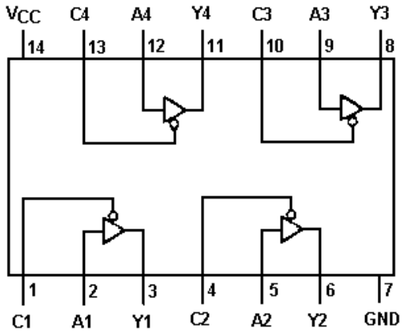
FLIP-FLOPS
19A700037P335

INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

Notes: Q0 = the level of Q before the indicated input conditions were established.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



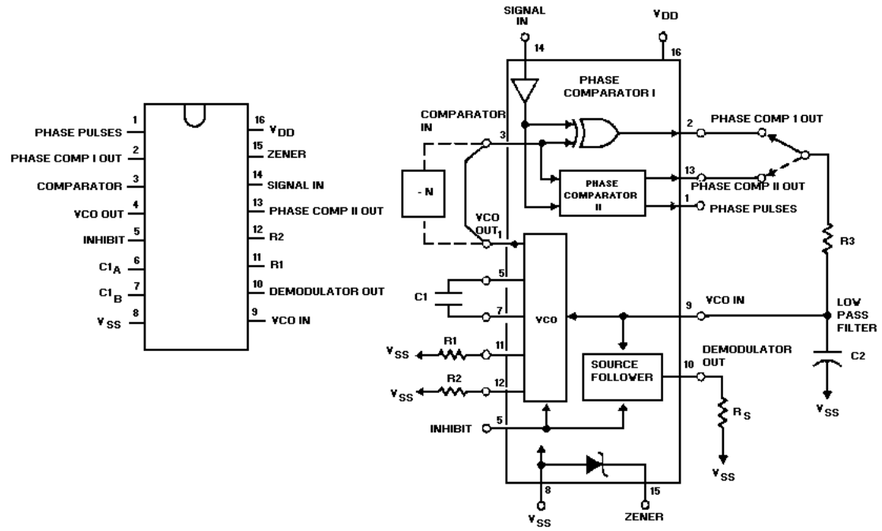
QUAD TRI-STATE BUFFERS
74HCT125



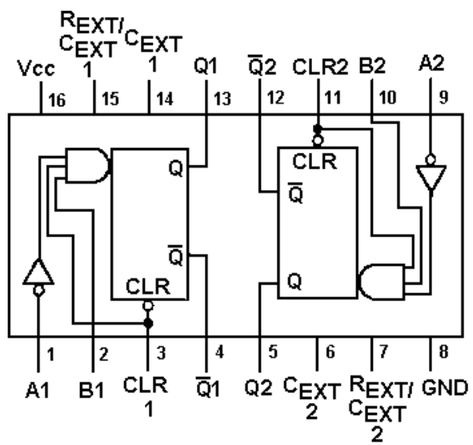
Truth Table

Inputs		Outputs
A	C	Y
L	L	L
H	L	H
X	H	HI-Z

PHASE-LOCKED LOOP
74HCT4046



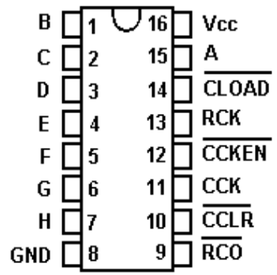
U17 DUAL RETRIGGERABLE MONOSTABLE



Truth Table

Inputs			Outputs	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	1	⎍	⎍
H	1	H	⎍	⎍
1	L	H	⎍	⎍

8-BIT BINARY COUNTER
74LS592



COUNTER CLOCK ENABLE CONTROL

CCKEN	$\overline{CCKEN}$	EFFECT ON CCK
L	L	ENABLE
L	H	DISABLE
H	L	ENABLE
H	H	ENABLE

U3, U5 DUAL PERIPHERAL DRIVER

LOGIC DIAGRAM